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Multistage Decimation Filters

Multistage Decimation Filters

- Decimation filter #2 can be realized with a accumulator rate of 57MHz, shift register, and coefficient ROM
  - A multiplier is not needed
- Multi-rate decimators can achieve the same result with even lower processing cost
- We will:
  - Illustrate how multistage decimation requires substantially lower multiply-accumulate rates than single stage decimation
  - Introduce very specific filter architectures that are specialized just for decimation/interpolation and can further reduce hardware complexity

Multistage Decimation Filters

- In multistage decimation, implement the sharpest transition bands at the lowest sampling frequency

- For our 3MHz audio modulator, we'll decimate by 64 in 3 stages
  - 8X in the first stage
  - 4X in the second stage
  - 2X in the third stage

Multistage Decimation Filters

- Datapath precision is important here
  - Stage 1 has 1-bit input data and doesn't need a hardware multiplier
  - Intermediate rounding operations between stages 1 and 2 and between stages 2 and 3 add quantization noise which must be modeled in a "bit true" fashion
  - Final rounding to the 20-bit ADC output adds negligible noise

- Coefficient precision is also important
  - 24b precision for 135dB stopband attenuation

Parks-McClellan Decimation

- In the first pass with synthesize the three stages with the Parks-McClellan algorithm and stick with floating point numbers
  - The results provide an estimate of aggregate multiply accumulate rates

- Each stage will specify 0.0000±0.0033dB ripple from 0-20kHz
  - Passband ripple in the 3 stages may add
  - The goal is a "fair" comparison to filter #2

Parks-McClellan Decimation

- Stages 1 and 2 prevent decimation from aliasing noise and tones into frequencies below 27kHz
- Stage 1 stopbands:
  - 375±27kHz, 750±27kHz, 1125±27kHz, 1473-1500kHz
- Stage 2 stopbands:
  - 93.75±27kHz, 160.5-187.5kHz
- Stage 3 stopband: 27-46.875kHz
- For each stage we specify 135dB stopband attenuation

Parks-McClellan Decimation

- MATLAB's Parks-McClellan front end doesn't handle lowpass filters like stage 1 very easily
  - The low pass filter we want has a single passband, multiple stopbands, and interspersed don't care bands

- We'll waste zeroes and implement stages 1 and 2 as single-stopband LPFs:
  - Stage 1 stopband 348-1500kHz
  - Stage 2 stopband 66.75-187.5kHz
  - Stage 3 stopband still 27-46.875kHz

Parks-McClellan Decimation

- These Parks-McClellan designs yield:
  - Stage 1: Length 57 (21.375MHz)
  - Stage 2: Length 50 (4.688MHz)
  - Stage 3: Length 84 (3.938MHz)

- Multiply-accumulate rates are shown in red above
  - Total multiply-accumulate frequency is 30MHz
  - Exploiting linear phase coefficient symmetry can reduce this to 15MHz
  - The filter #2 design required 57MHz

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Comb Filters

Comb Filters

- Let's look at the a "rectangular" transfer function,

$$H(z) = \sum_{i=0}^{N-1} z^{-i}$$
$$= 1 + z^{-1} + z^{-2} + z^{-3} + z^{-4} + z^{-5} + z^{-6} + z^{-7} + \ldots$$
$$= \frac{1 - z^{-N}}{1 - z^{-1}}$$

- This filter has N-1 evenly spaced zeros on the unit circle, except at z=1 → LPF

- A N=8 rectangular window is the simplest filter candidate for a decimate-by-8 stage 1 design

Comb Filters

- A single comb filter obviously will not meet the specification … but a cascade of K of them might

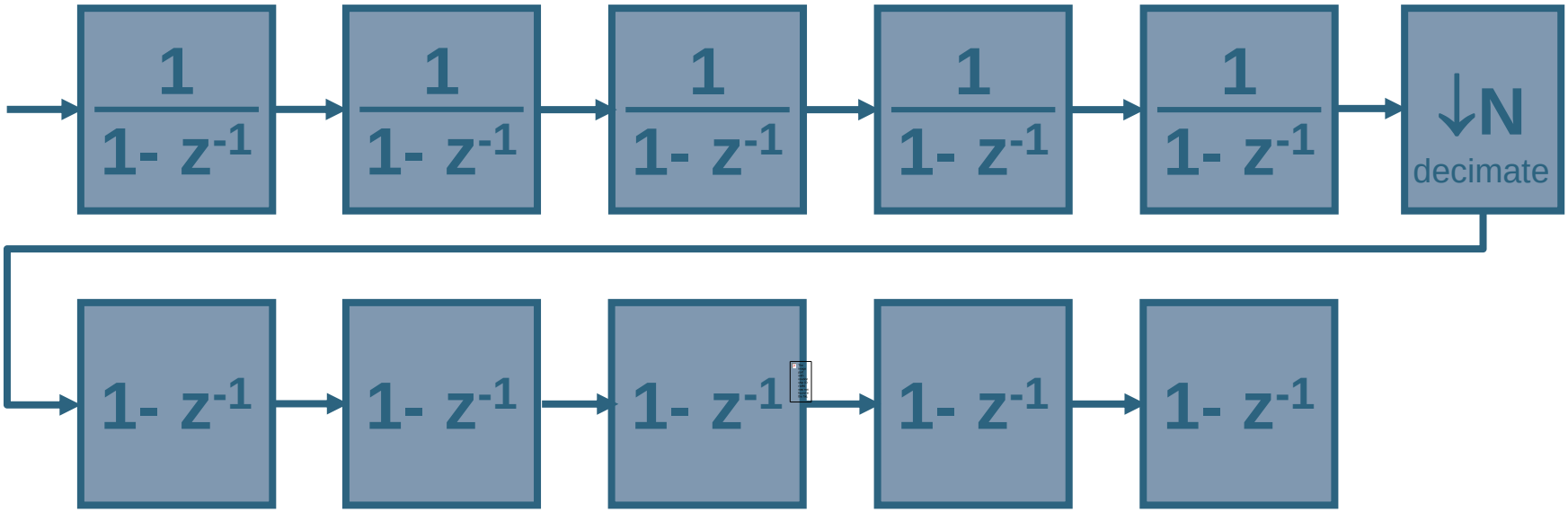
- The resulting filter is not very good (significant in-band droop), but a "trick" due to Hogenauer leads to an extraordinarily simple implementation

$$H(z) = \left[\sum_{i=0}^{N-1} z^{-i}\right]^K = \left[\frac{1-z^{-N}}{1-z^{-1}}\right]^K$$

$$= \left[\frac{1}{1-z^{-1}}\right]^K \left[1-z^{-N}\right]^K$$

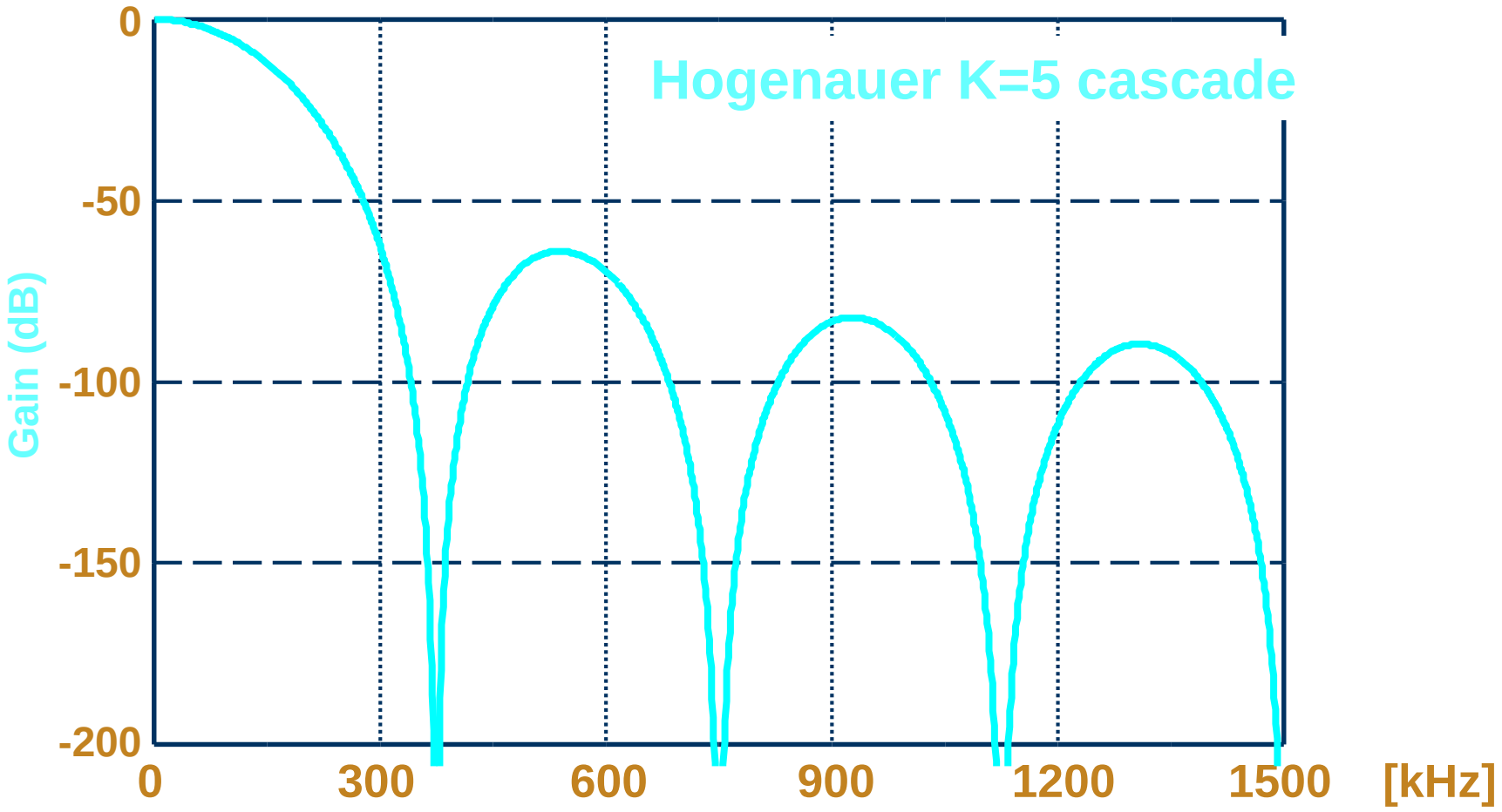
- Let's see how this looks in hardware …

Hogenauer Filter, K=5



- The integrators operate at f_{SIN}, the differentiators at f_{SOUT}
- The decimate block throws away N−1 of every N integrator output samples
- z^{-1} at f_{SOUT} is equivalent to z^{-N} at f_{SIN}

Hogenauer K=5 Cascade



[Eric Swanson]

Hogenauer Filters

- The Hogenauer 5-cascade doesn't come close to meeting our 135dB antialiasing specification near 375kHz
  - A higher value of K is needed (typically L+1 or more)

- Hogenauer implementations aren't without difficulty
  - The high-speed integrators integrate offsets to infinity and must "roll over" gracefully
  - Word-width requirements grow through the cascade

Ref: Eugene Hogenauer, "An Economical Class of Digital Filters for Decimation and Interpolation", IEEE Trans. Acoustics, Speech, and Signal Processing, ASSP-29, April 1981.

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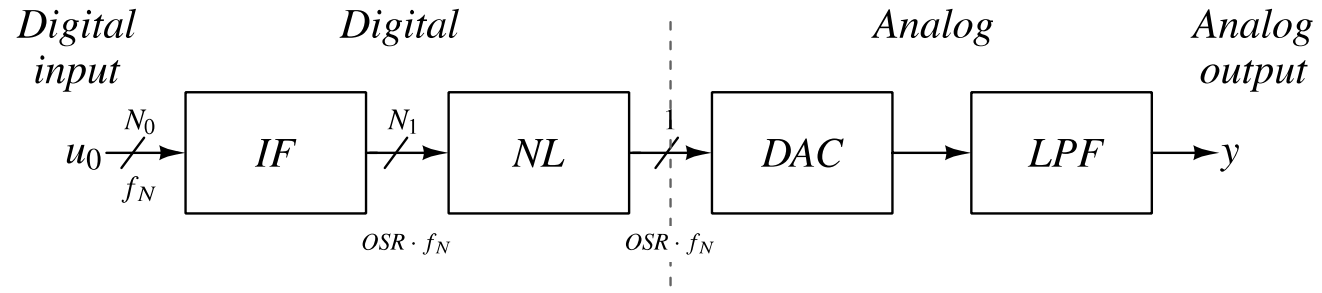
Other ΣΔ Topics

ΣΔ DACs

- Can build high-SNDR DAC using:
  - Digital interpolator (to increase sample rate by OSR)
  - Digital ΣΔ DAC modulator
    - Often error-feedback sigma-delta modulator
  - 1 bit DAC
  - Low-pass reconstruction filter



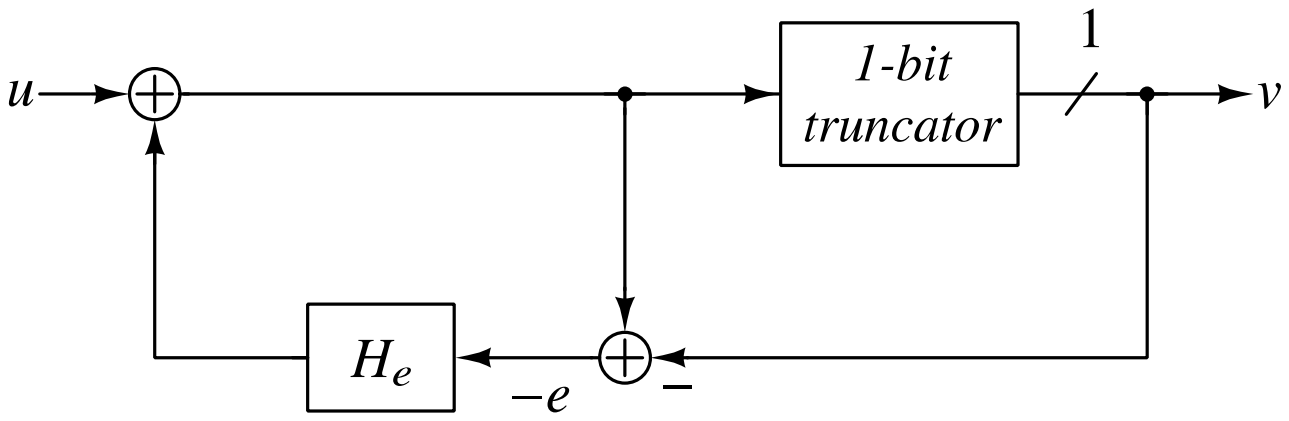
IF: Interpolation filter

NL: Noise-shaping Loop

DAC: Digital-to-Analog Converter

LPF: Lowpass Filter

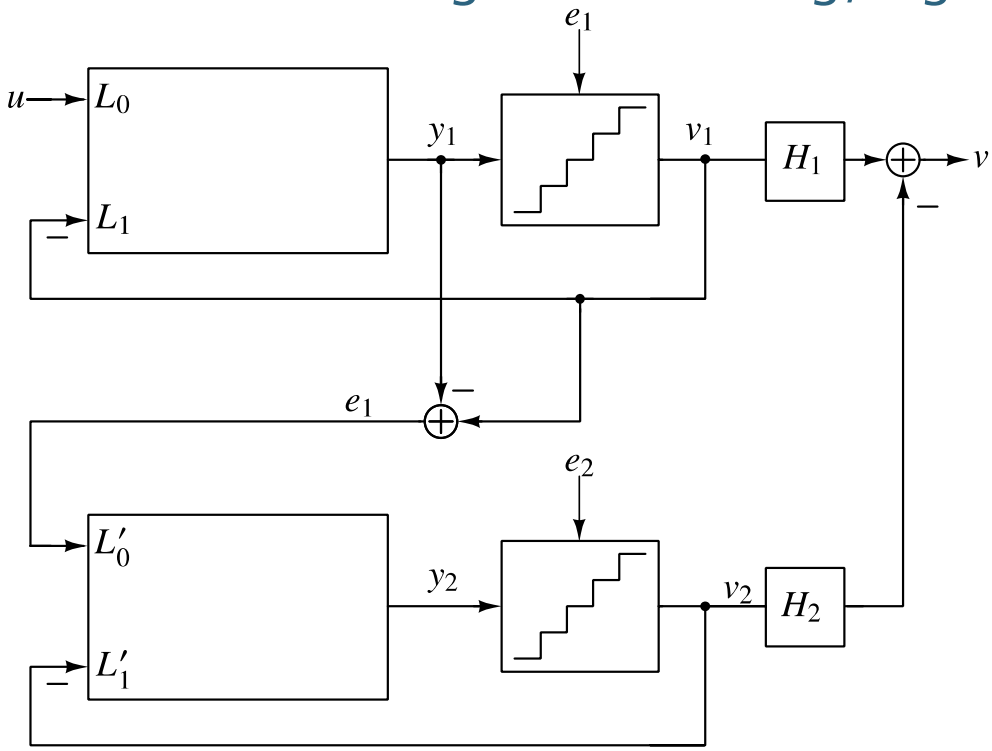
ΣΔ DACs: Error-Feedback Modulator



- Quantize to 1 bit → keep MSB
  Quantization error → LSBs
- $V(z) = U(z) + \left(1 - H_e(z)\right) E(z)$
- For 1st order loop: $H_e(z) = z^{-1}$
  For 2nd order loop: $H_e(z) = z^{-1}(2 - z^{-1})$
- Error-feedback structure not practical for analog ΣΔ ADCs

Multi-Stage ΣΔ ADCs

- Cancel quantization noise of first stage(s) using additional stages
- Issue: noise leakage from analog/digital mismatch



Figur 5.3 A two-stage MASH structure.

$$V_1(z) = \mathrm{STF}_1(z)\,U(z) + \mathrm{NTF}_1(z)\,E_1(z)$$
$$V_2(z) = \mathrm{STF}_2(z)\,E_1(z) + \mathrm{NTF}_2(z)\,E_2(z)$$
$$V(z) = H_1(z)V_1(z) - H_2(z)V_2(z)$$

$E_1(z)$ term in is canceled if:
$H_1(z)\,\mathrm{NTF}_1(z) = H_2(z)\,\mathrm{STF}_2(z)$

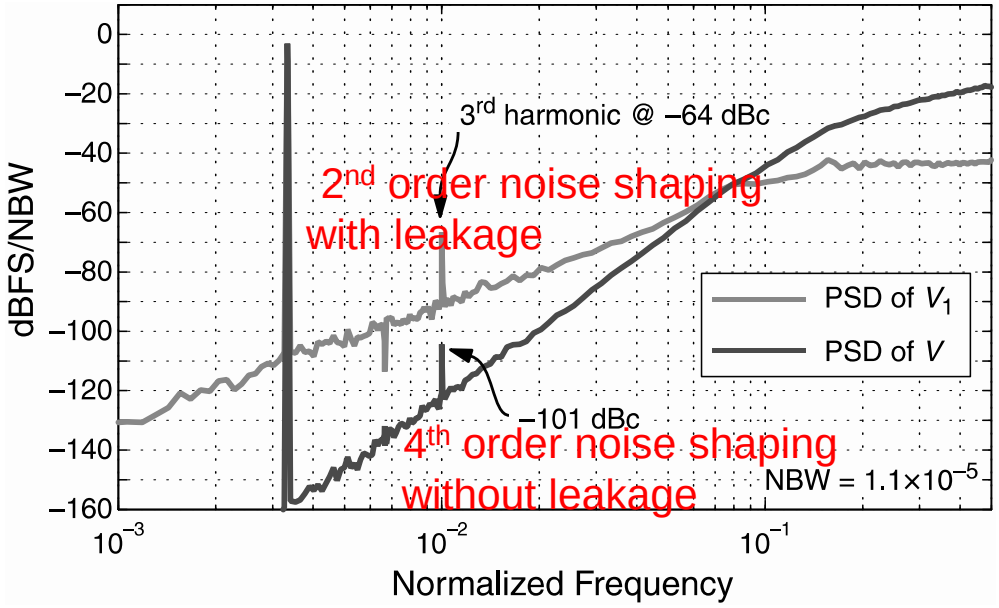
→ $H_1(z) = \mathrm{STF}_2(z)$
and $H_2(z) = \mathrm{NTF}_2(z)$

→ $V(z) = \mathrm{STF}_1(z)\;\mathrm{STF}_2(z) - \mathrm{NTF}_1(z)\,\mathrm{NTF}_2(z)$

→ Higher order noise shaping

Quantization Noise Leakage

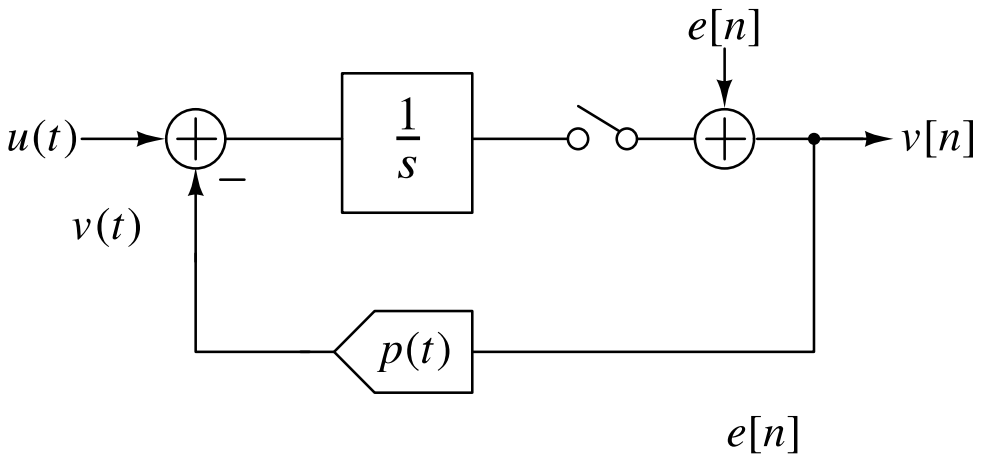
- If actual analog STF and NTF do not match digital H:
- $\mathrm{STF}_{2a}(z) \neq \mathrm{STF}_2(z) = H_1(z)$
  $NTF_{1a} \neq \mathrm{NTF}_1(z) = H_2(z)$
- Result: $H_{l1}(z) = H_1(z)\,STF_{2a}(z) - H_2(z)\,NTF_{1a}(z)$
  → First stage quantization error leakage: $H_{l1}(z)\,E_1(z)$



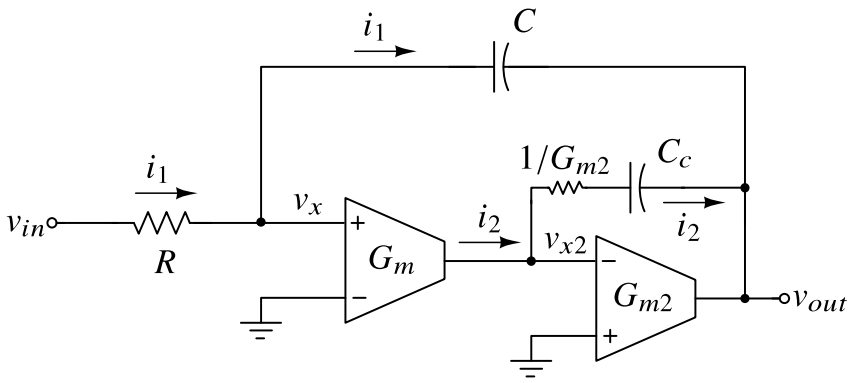
2-2 MASH ΣΔ ADC

Continuous-Time ΔΣ ADCs

- Continuous-time integrators instead of discrete-time



OTA-RC Integrator using Miller OTA

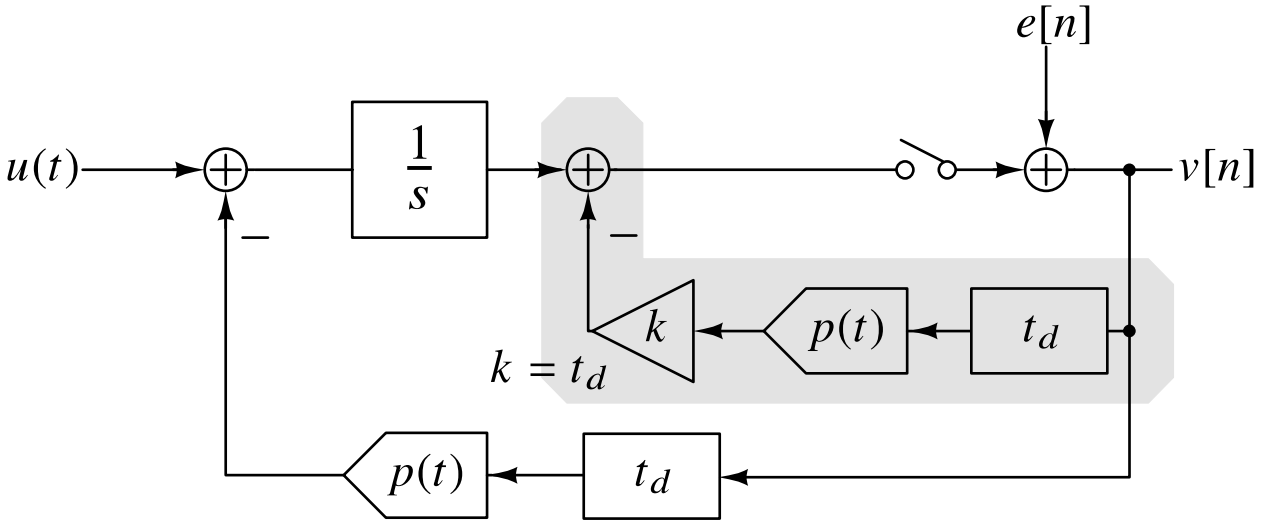


- Design using impulse invariant transform CT ←→ DT

- CT typically lower power compared to DT

Continuous-Time ΔΣ ADC Non-Idealities

- Excess loop delay from quantizer to feedback DAC
  - Comparator needs to time to resolve input
  - Requires loop modifications



- RC time-constant variations → ΣΔ loop variations
- Clock jitter sensitivity

Multi-Bit ΣΔ ADCs/DACs

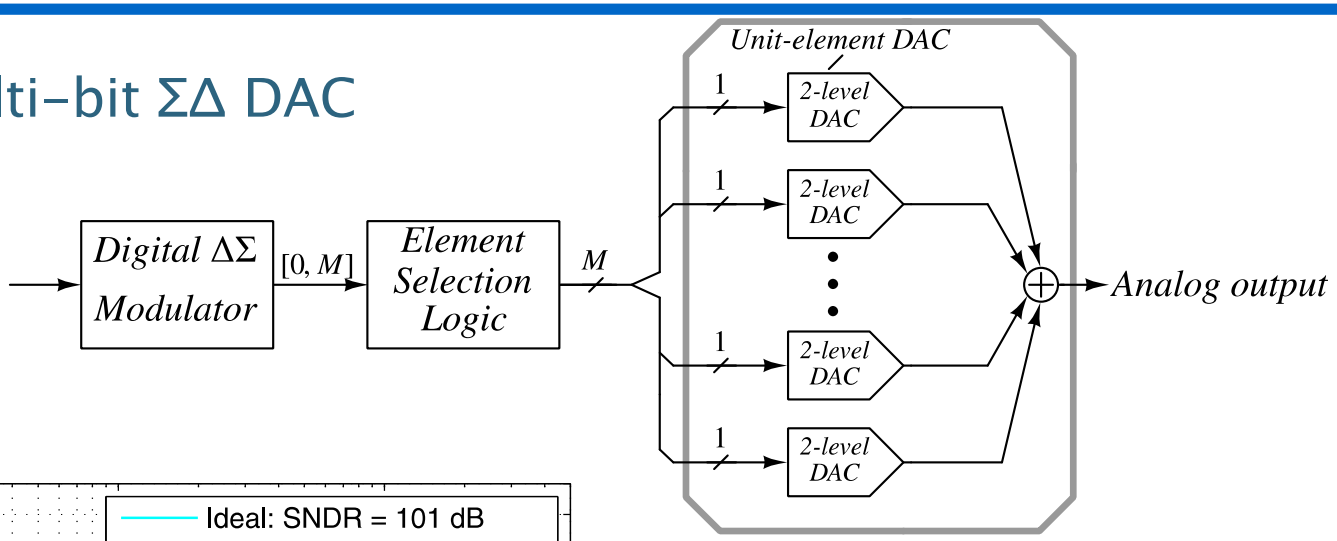
- Multi-bit quantizer & multi-bit feedback DAC
  - Lower quantization with same loop filter & OSR
  - Lower jitter sensitivity in CT loops
    - Smaller feedback steps

- 3-level DAC requires 0.01% matching for -90dB distortion

- Solution
  - Calibration (but aging, drift, package shifts, …)
  - Digital correction (but aging, drift, package shifts, …)
  - Mismatch shaping

Mismatch-Shaping for Multi-Bit ΣΔ ADCs/DACs (1/3)

- Example: multi-bit ΣΔ DAC (M = 16)



A ΔΣ DAC system.

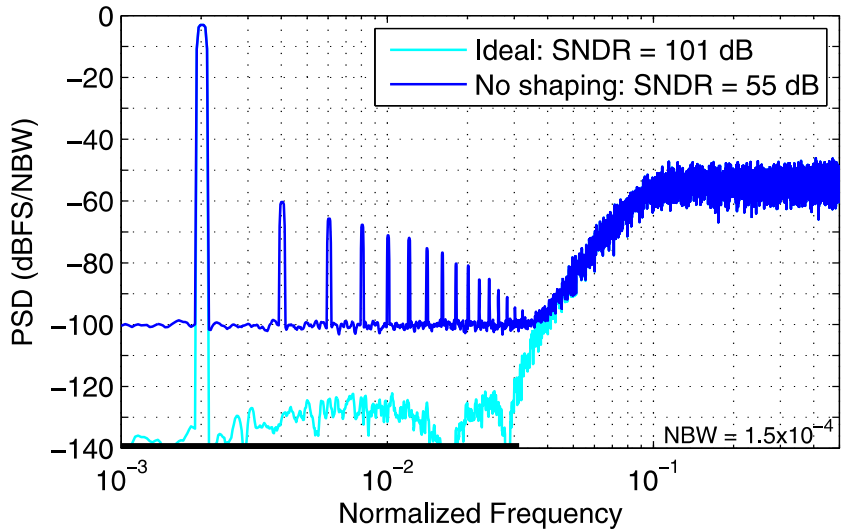


Figure 6.4 Average PSD for a 16-element DAC with 1% element mismatch – no shaping.

Mismatch-Shaping for Multi-Bit ΣΔ ADCs/DACs (2/3)

- Random element selection
  → removes tones, but does not lower noise floor

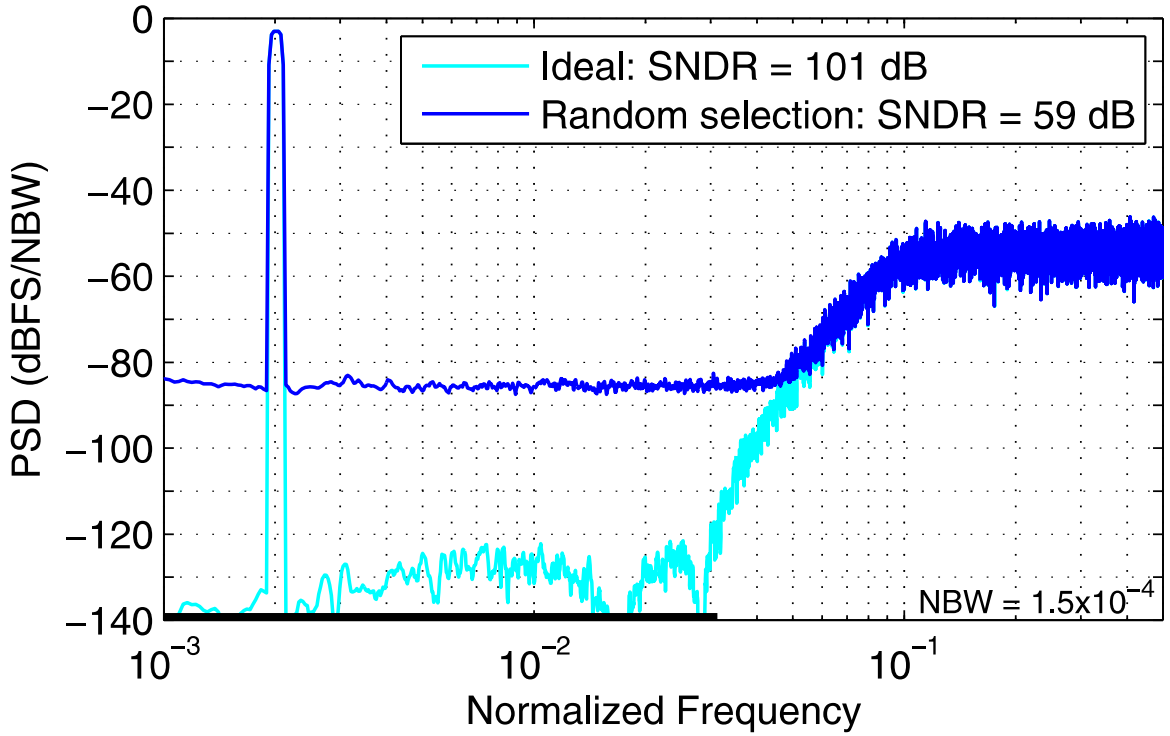
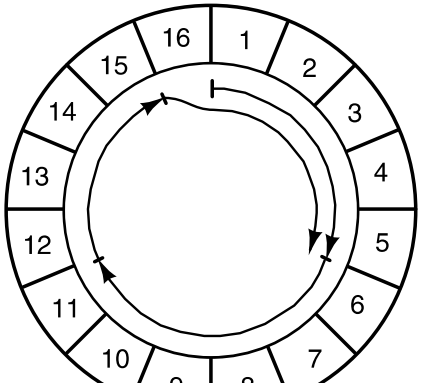
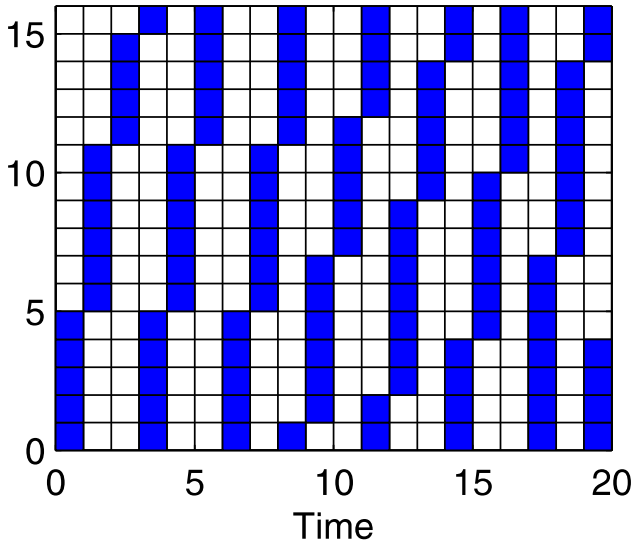


Figure 6.5 Average PSD for a 16-element DAC with 1% element mismatch– random selection.

Mismatch-Shaping for Multi-Bit ΣΔ ADCs/DACs (3/3)

- Element rotation
  - Data-weighted averaging
  - Shapes mismatch-induced noise floor





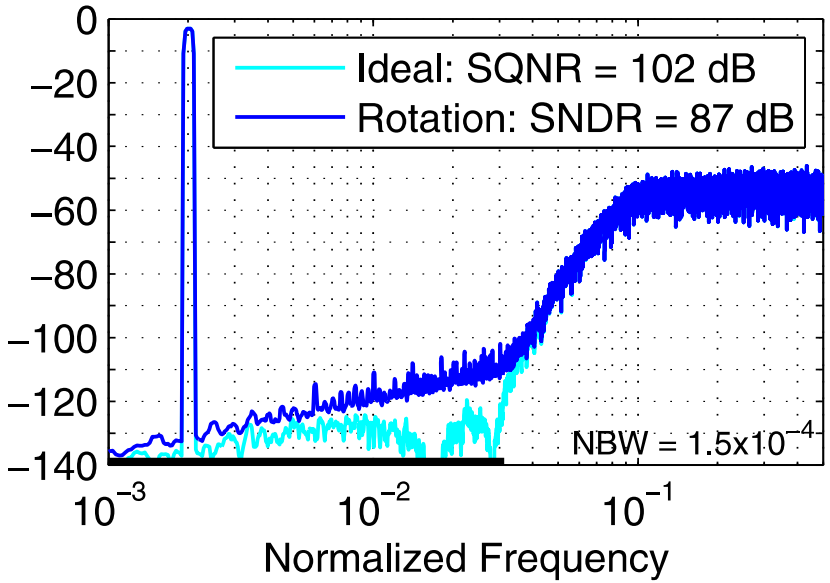


Figure 6.7 Example usage pattern and spectrum for rotation.

Bandpass ΔΣ ADCs

- Band-stop NTF instead of high-pass NTF
- Applications: wireless communications; resonant sensors

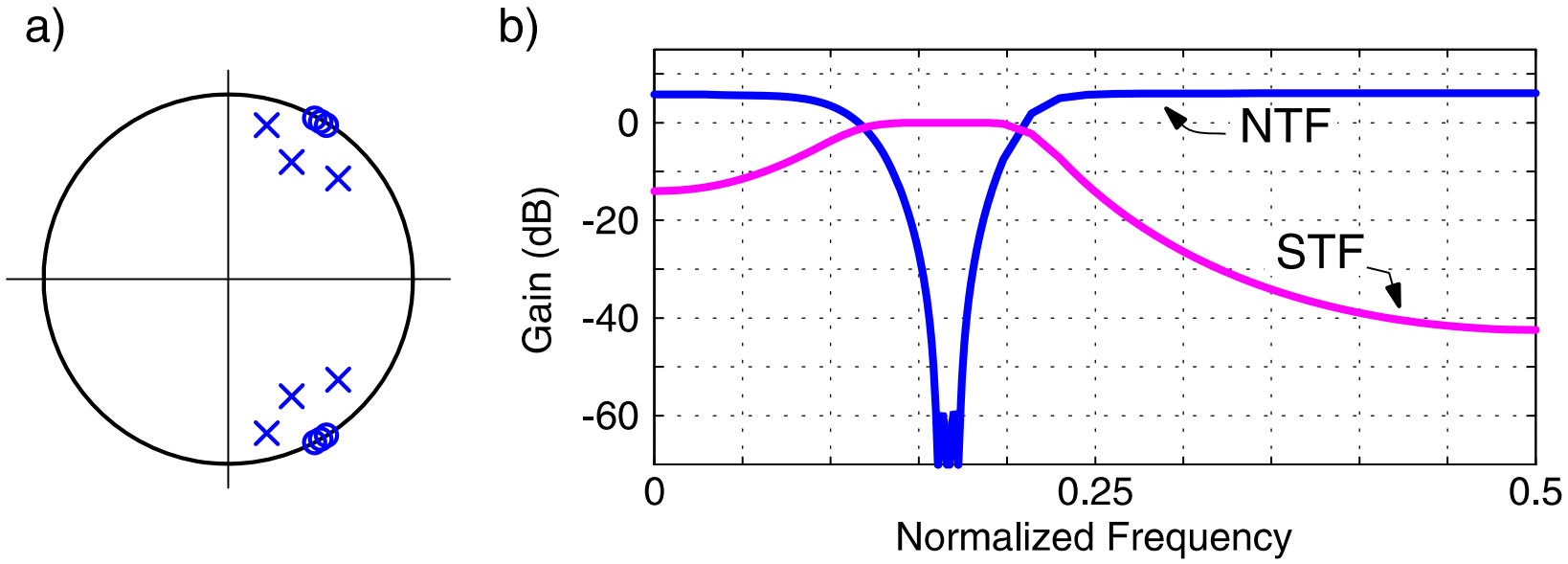
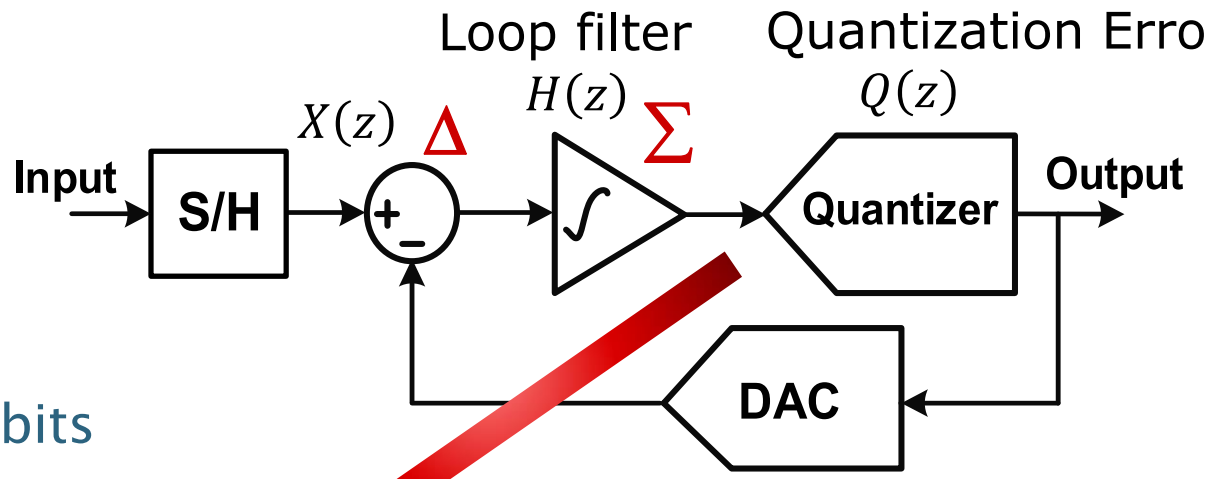
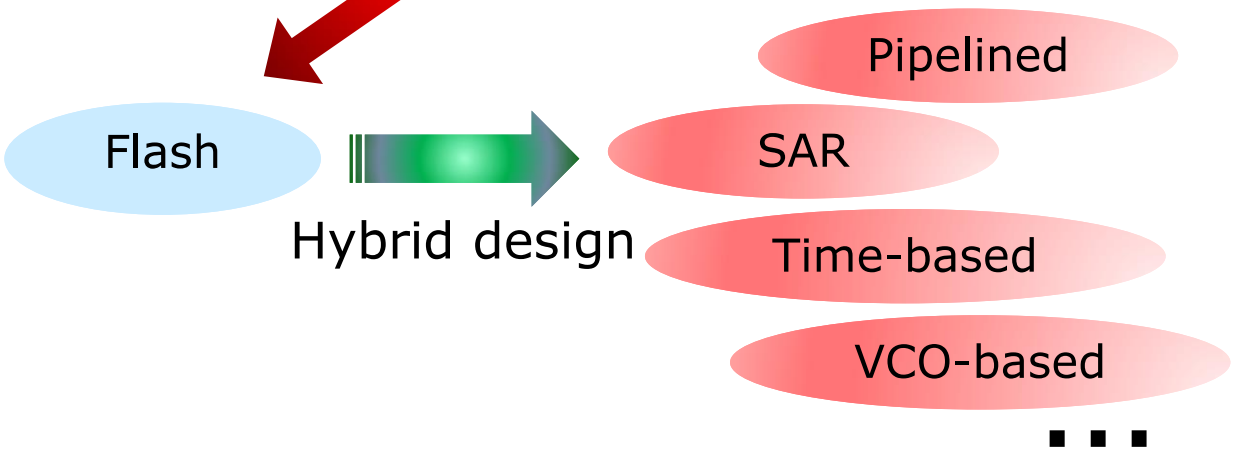


Figure 11.5 (a) Pole-zero and (b) NTF/STF magnitude plots for an $f_s/6$ bandpass modulator.

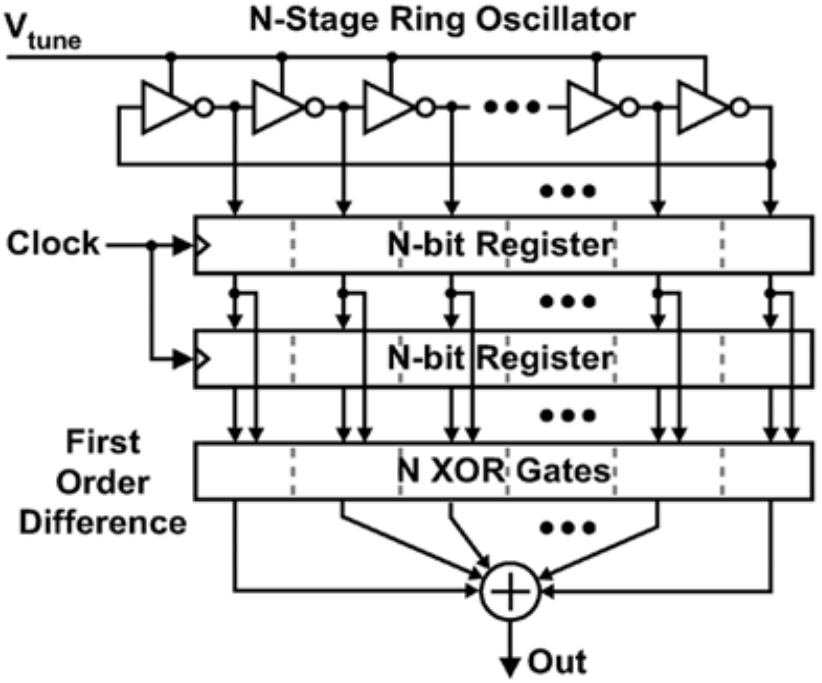
Hybrid Oversampling ADCs

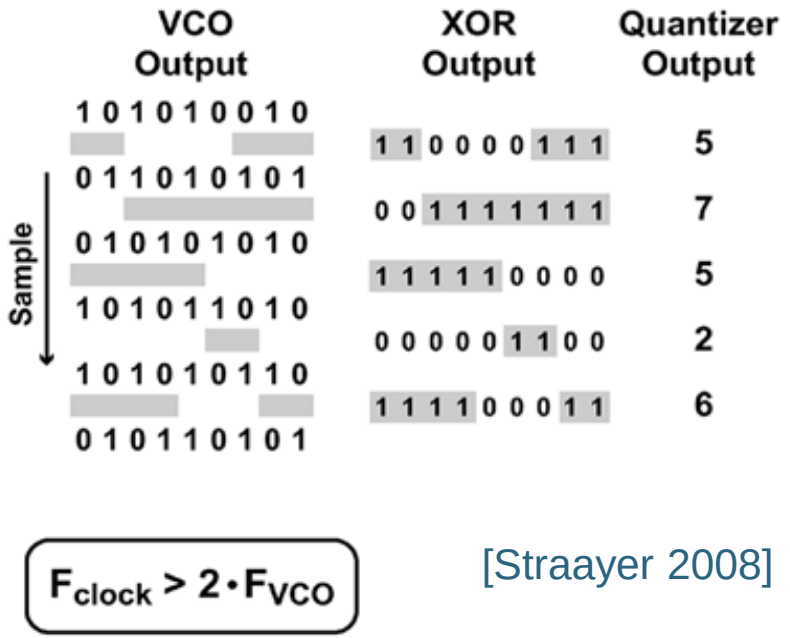
- Increased quantizer resolution with limited OSR
- Flash quantizer not efficient for higher number of bits





VCO-based Quantizer





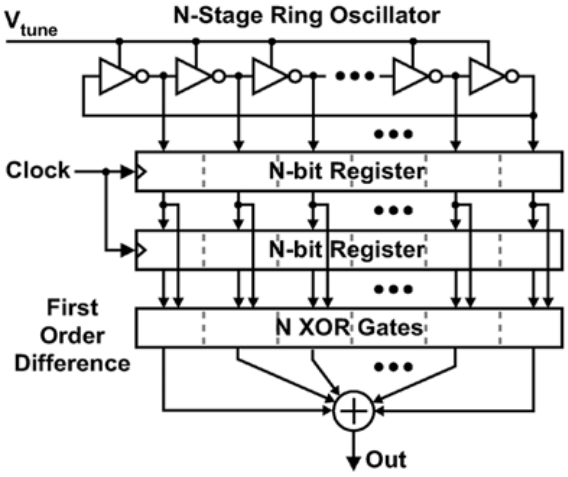
$F_{clock} > 2 \cdot F_{VCO}$

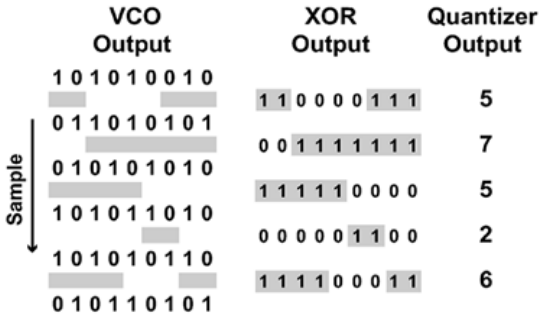
[Straayer 2008]

- Free running VCO:
  quantized value = number of VCO stages changing over T_{clk}
  - Calculated using registers and XOR gates
- K_{VCO} limits linearity
- Thermometer code at output of XOR gates rotates → DEM

VCO-based Quantizer: Noise Shaping

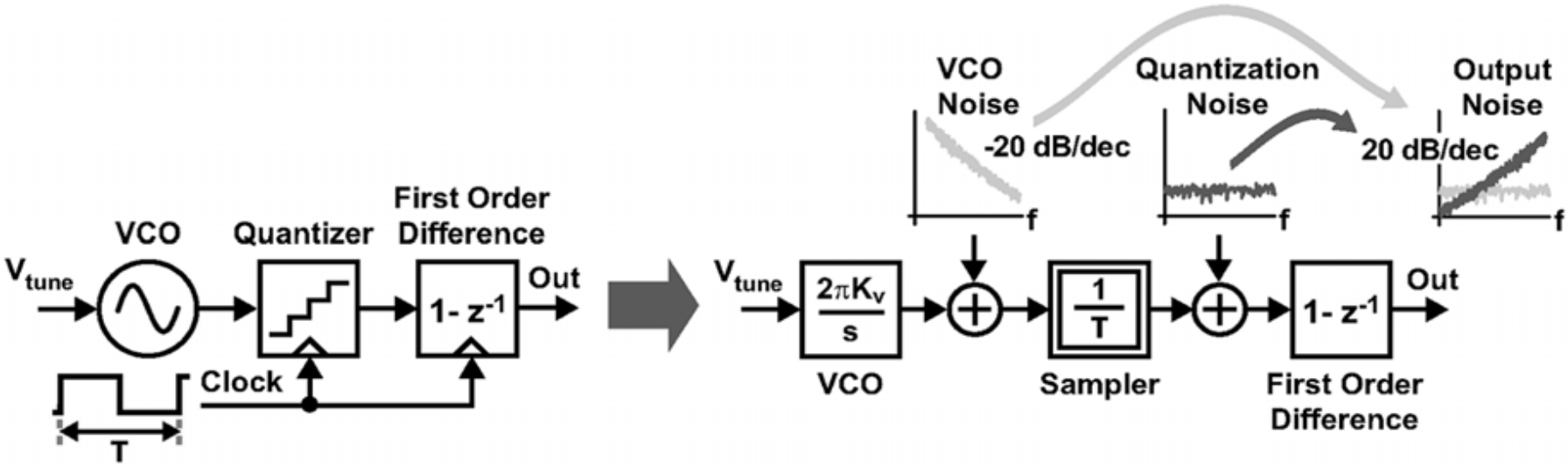
- Quantization noise is shaped → additional order of noise shaping





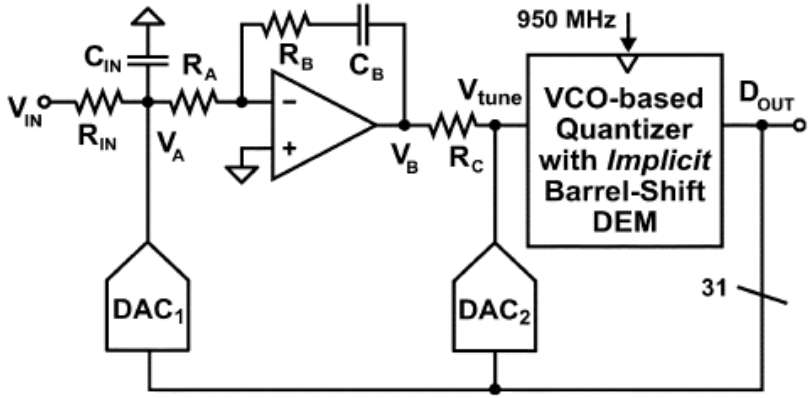
$F_{clock} > 2 \cdot F_{VCO}$

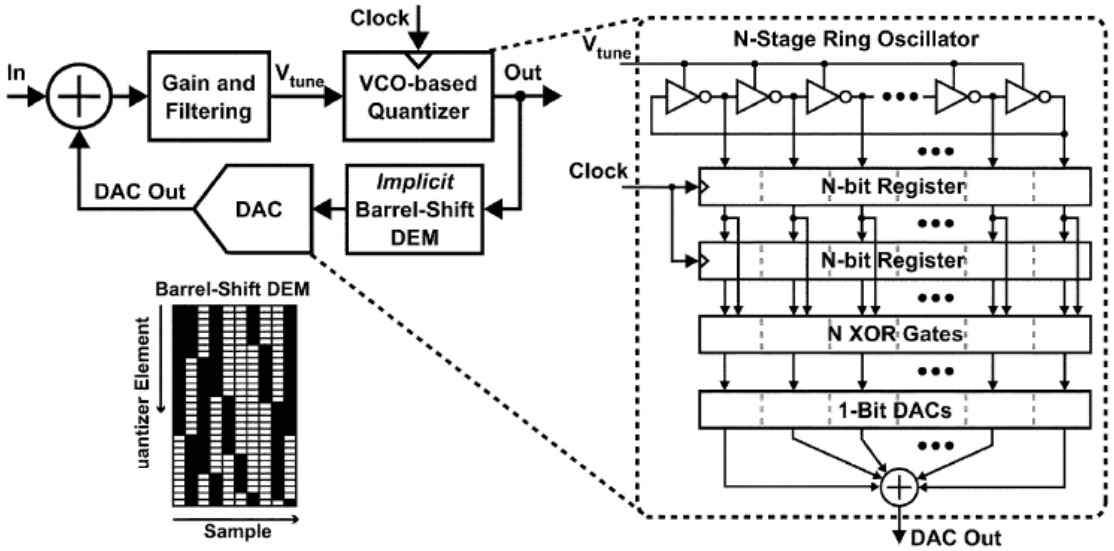
[Straayer 2008]



VCO-based Quantizer: Implicit DEM

- Thermometer code at output of XOR gates rotates → DEM



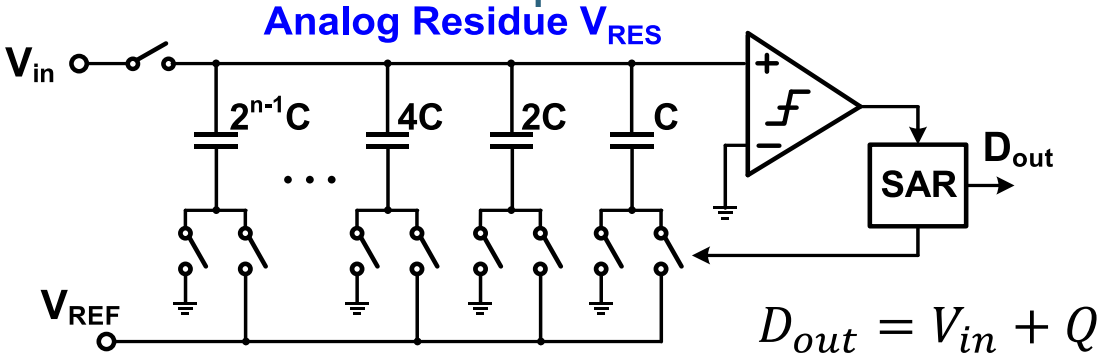


[Straayer 2008]

12b 86dB SNDR
10 MHz BW, 950 MS/s, 40 mW

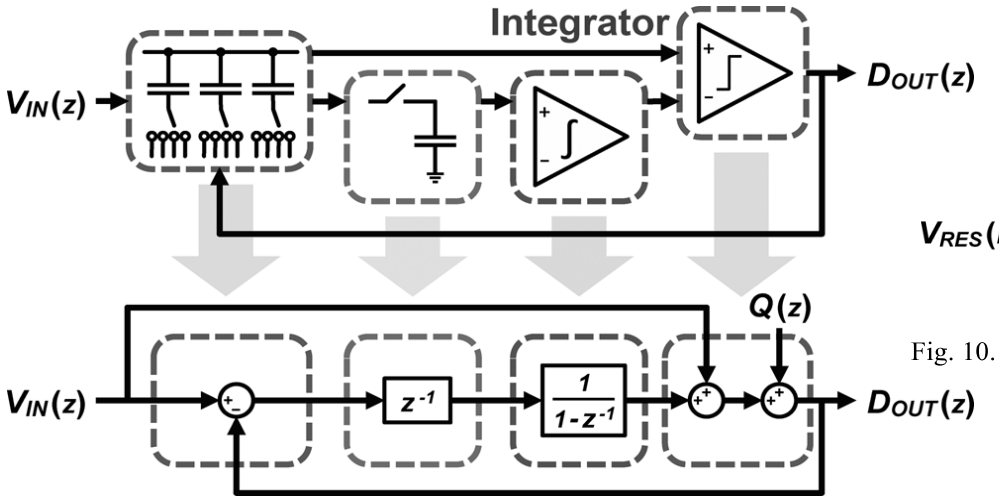
Noise Shaping SAR

- Use SAR residue as quantization error



$$D_{out} = V_{in} + Q$$

[Fredenburg 2012]



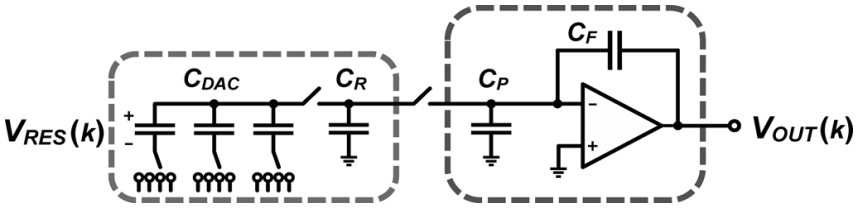


Fig. 10. Simplified depiction of improved noise-shaping SAR ADC.

Incremental ADCs

- Incremental ADC = resettable ΣΔ ADC (& resettable decimation)
  - Multiplexed operation
  - Duty-cycled operation

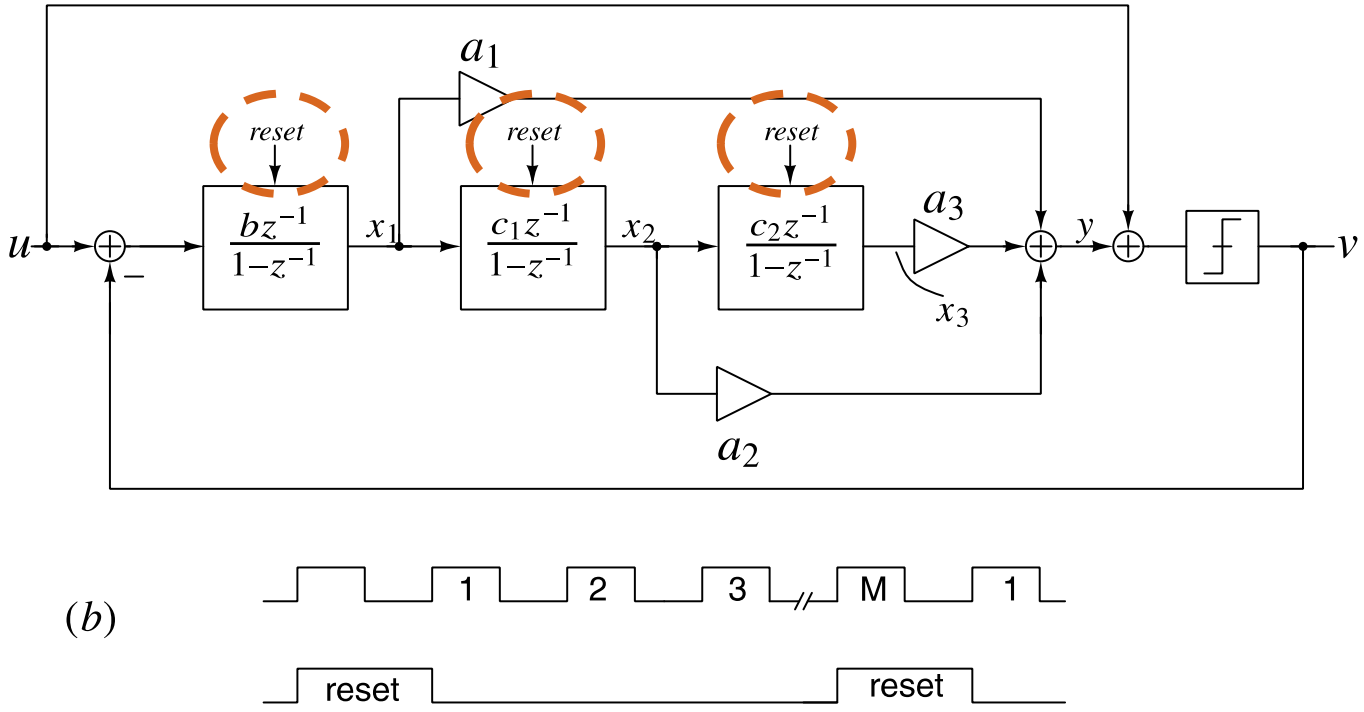


Figure 12.3 Third-order IADC.

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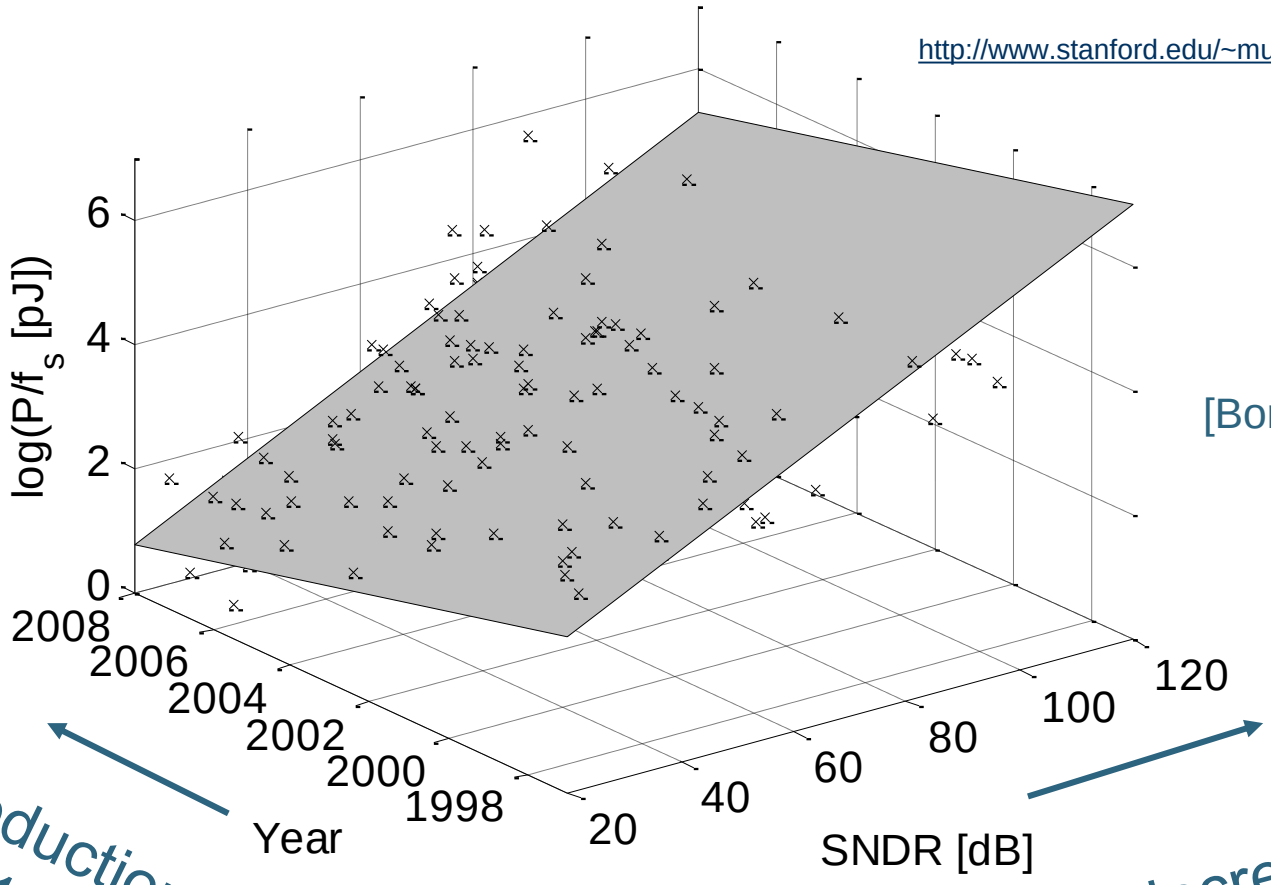
Limits on ADC Power Dissipation

Power Dissipation Trend

http://www.stanford.edu/~murmann/adcsurvey.html



[Boris Murmann]

2x reduction every 2.1 years (!)

1.87x power increase per 6dB

Predicting the Trend

- Figures of Merit
- Fundamental Limits
- Practical Limits

ADC Figures of Merit (1)

- Objective
  - Compare performance of different ADCs
- Can use FOM to combine several performance metrics into one single number
- What are reasonable FOMs for ADCs?
- What's the impact of technology scaling?
- Trends and limits?

- Reference: B. Murmann, "Limits on ADC Power Dissipation," in *Analog Circuit Design,* by M. Steyaert, A.H.M Roermund, J.H. van Huijsing (eds.), Springer, 2006.

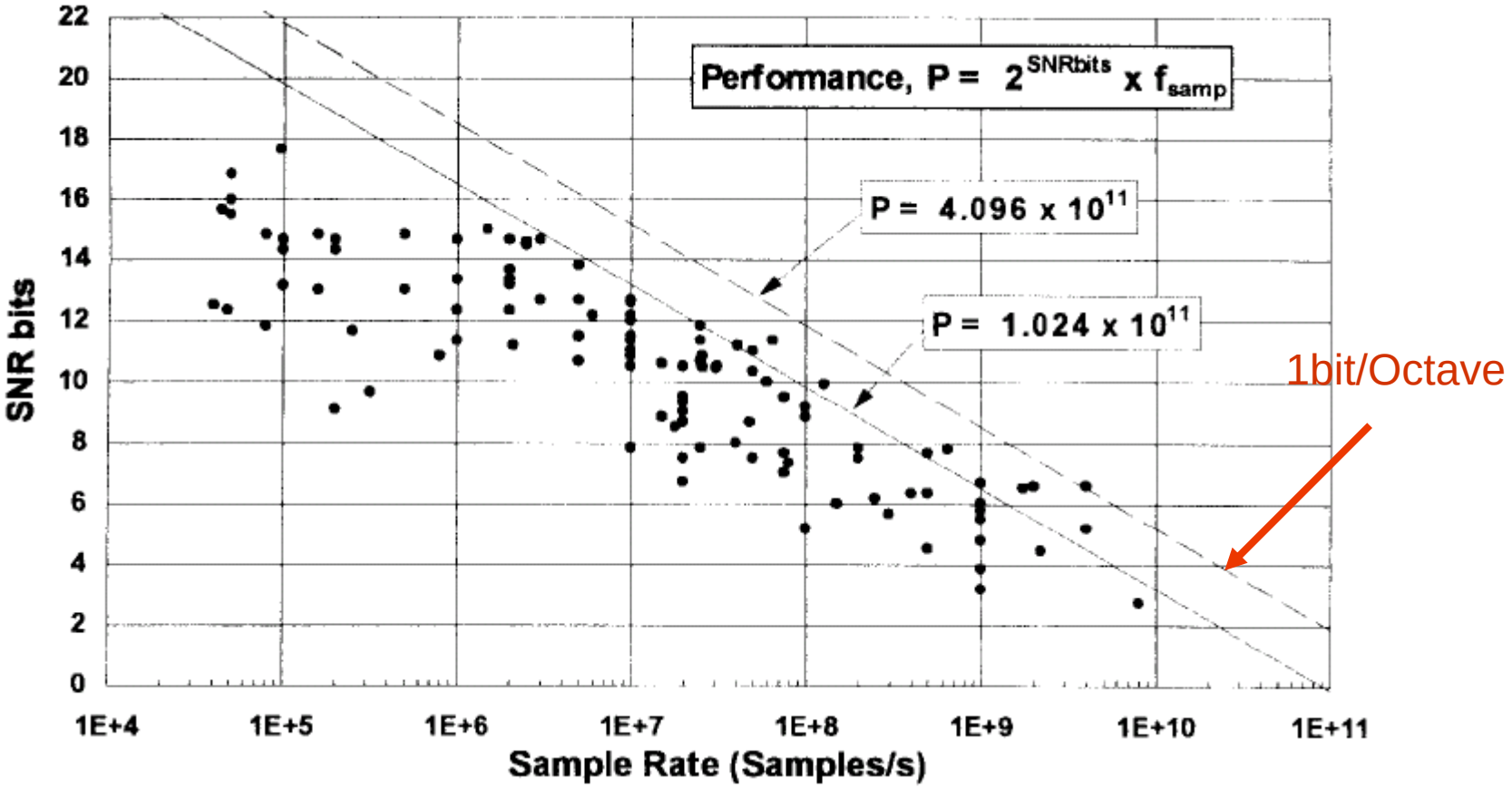
ADC Figures of Merit (2)

$$\text{FOM}_1 = f_s \cdot 2^{\text{ENOB}}$$

[R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, April 1999]

- This FOM suggests that adding a bit to an ADC is just as hard as doubling its bandwidth
- Is this a good assumption?

Survey Data



[Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Selected Areas Comm.*, April 1999]

ADC Figures of Merit (3)

$$\text{FOM}_\text{W} = \frac{\text{Power}}{f_s \cdot 2^{\text{ENOB}}}$$

[R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, April 1999]

- Walden Figure of Merit
- Most widely used FOM
- In typical circuits power ~ speed
  - FOM_W captures this tradeoff correctly
- Power vs. ENOB
  - One additional bit = 2x in power?

ADC Figures of Merit (4)

- In a circuit that is limited by thermal noise, each additional bit in resolution means...
  - 6dB SNR, 4x less noise power, 4x bigger C
  - Power ~ G_m ~ C increases 4x
- Even worse: Flash ADC
  - Extra bit means 2x number of comparators
  - Each of them needs double precision
  - Transistor area 4x, Current 4x to maintain current density
  - Net result: Power increases 8x
- "Tends to work" because not all power in an ADC is noise limited
  - E.g. Digital power, biasing circuits, etc.

ADC Figures of Merit (5)

$$\text{FOM}_3 = \frac{\text{Power}}{2 \cdot \text{Conversion Bandwidth}} = \text{"Energy / Nyquist Sample"} = [\text{J/conv.}]$$

- Compare only power of ADCs with approximately same SNR or SNDR (ENOB)
- Useful numbers (~state-of-the-art):
  - 10b (~9 ENOB) ADCs: 0.25 ... 1 mW/MHz
  - 12b (~11 ENOB) ADCs: 2 ... 6 mW/MHz

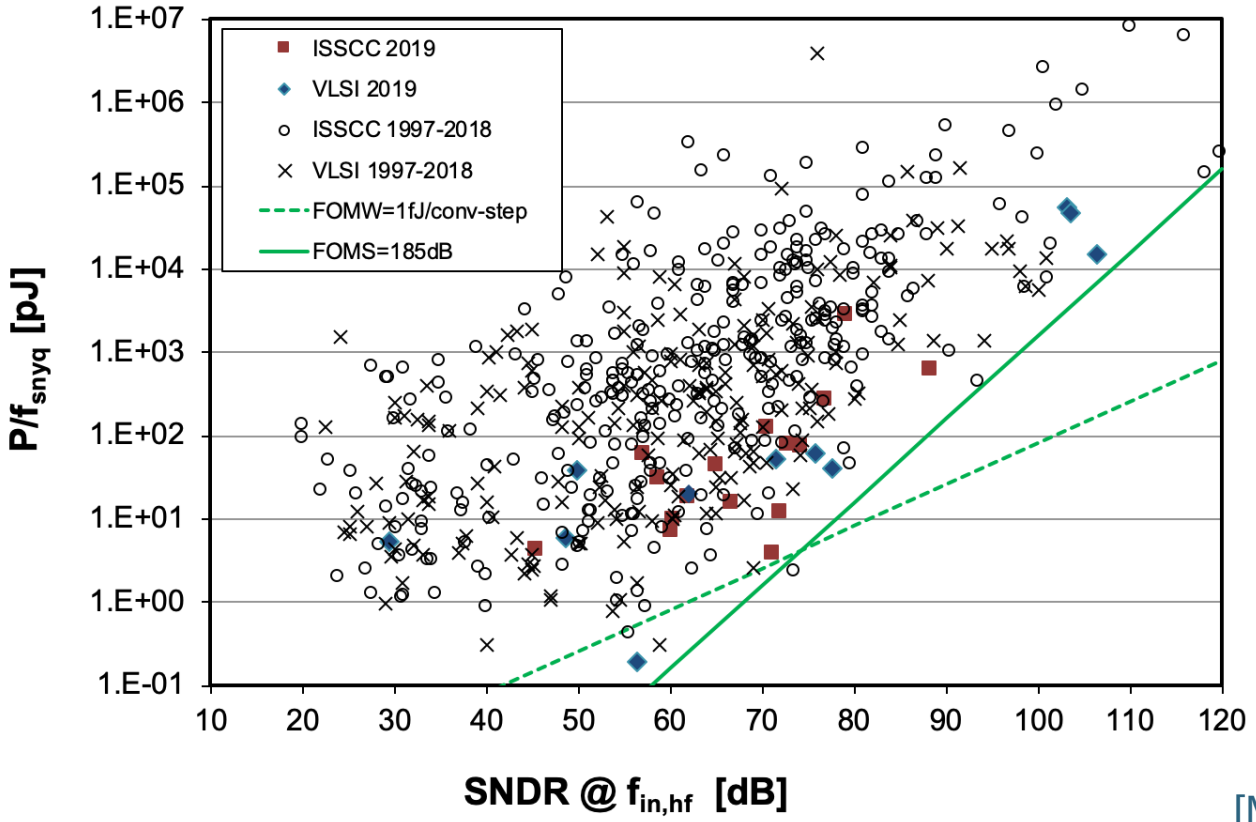
ADC Figures of Merit (6)

$$\mathrm{FOM_S} = \mathrm{DR}(dB) + 10\log_{10}\left(\frac{\mathrm{BW}}{\mathrm{Power}}\right)$$

- Schreier Figure of Merit
- Power vs. ENOB
  - One additional bit = 4x in power
  - Thermal noise limited ADCs
- HF Schreier FoM:
  - SNDR instead of DR: includes distortion

$$\mathrm{FOM_{S,HF}} = \mathrm{SNDR}(dB) + 10\log_{10}\left(\frac{\mathrm{BW}}{\mathrm{Power}}\right)$$

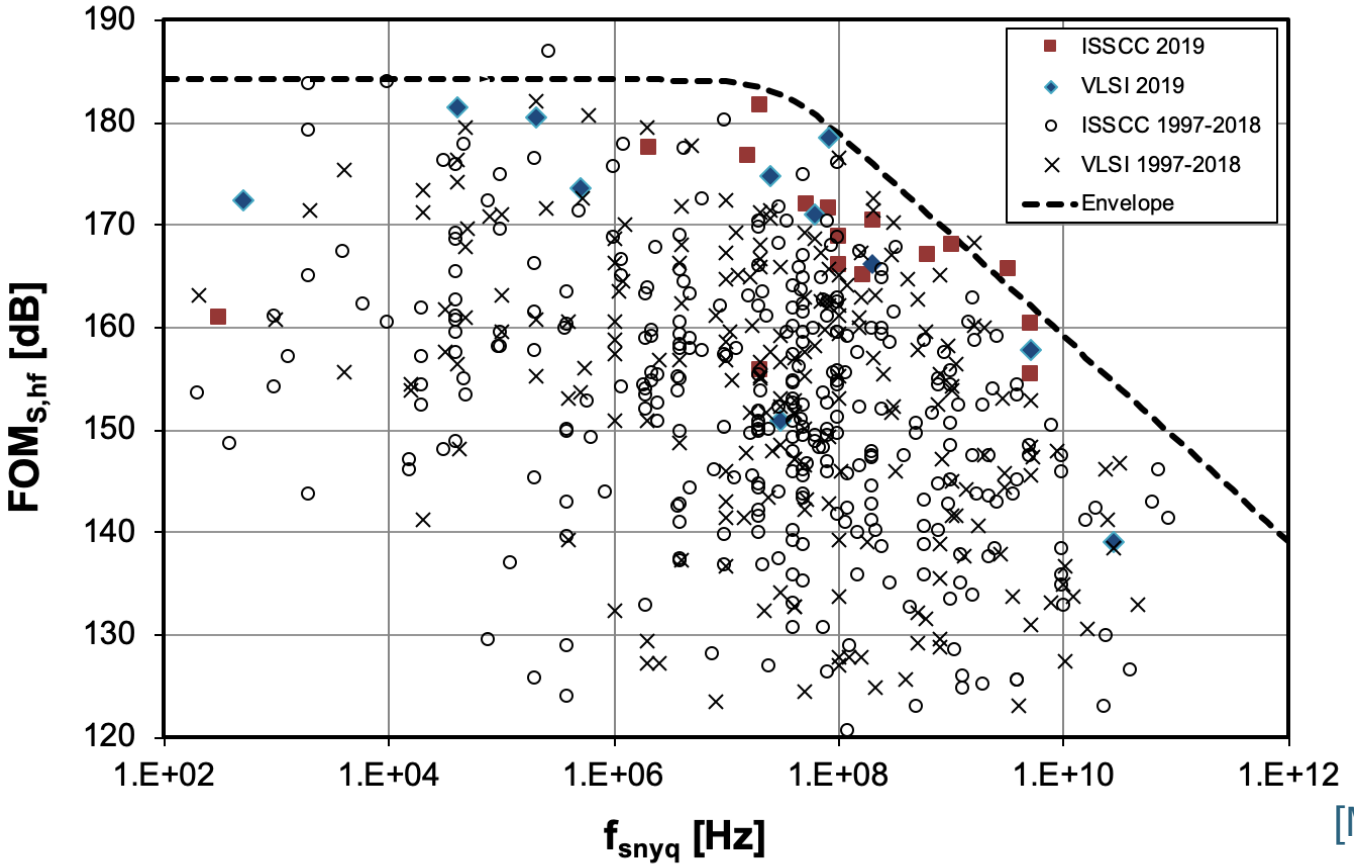
FOM (ISSCC & VLSI 1998 – 2018)



[Murmann]

- Technology-limited at lower SNDR: 100 fJ = 1V 100 fF / conv
- Noise-limited at higher SNDR

FOM (ISSCC & VLSI 1998 – 2018)



[Murmann]

- Some improvement over time at low f_{snyq} (1 dB / year)
- Progress at high f_{snyq} driven by technology scaling (2x / 1.6yr)

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Fundamental Limits

Fundamental Limits

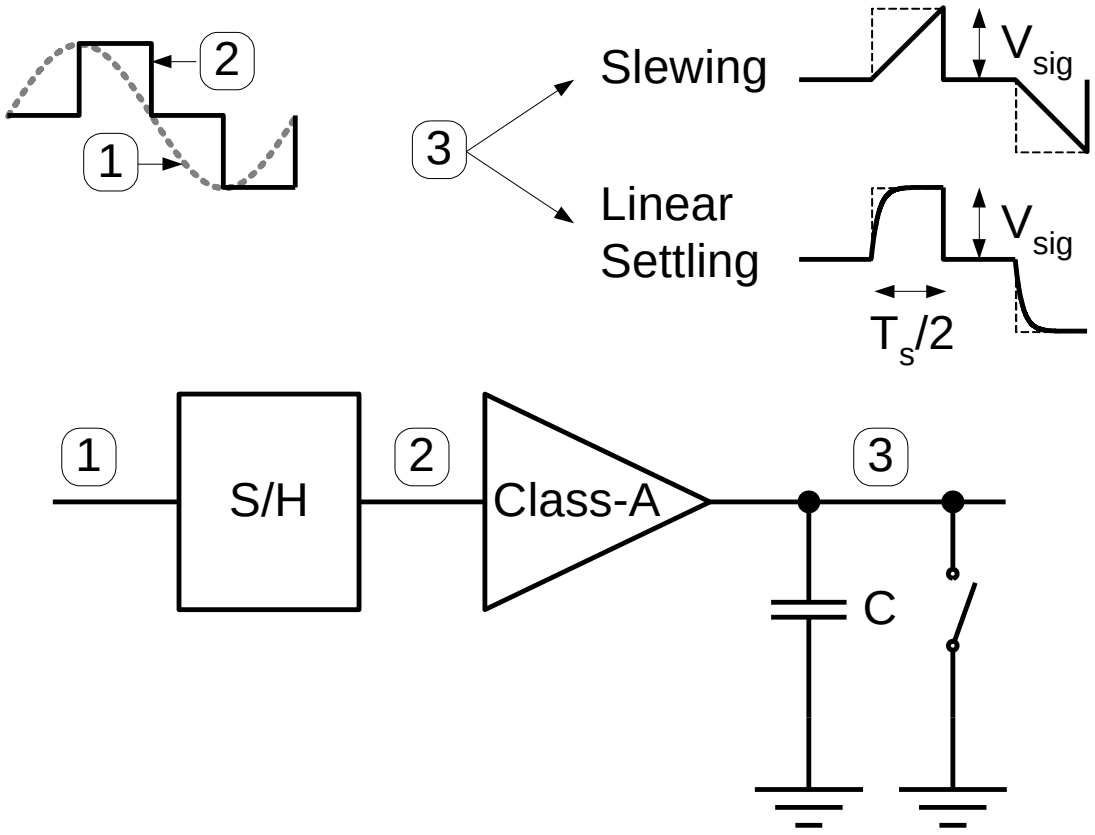
- Fundamental power limit for a class-B amplifier driving a single capacitor [Vittoz, ISCAS 1990]

$$P = 8 \cdot f_{sig} \cdot CV_{sig}{}^2 \qquad V_n^2 = \frac{k_B T}{C} \qquad SNR = \frac{0.5 \times V_{sig}^2}{V_n^2}$$

$$\therefore P = 8 k_B T \cdot SNR \cdot f_{sig}$$

- Class-A power limit is π times higher
- At $f_{sig} = f_s/2 \rightarrow FOM_S = 195$ dB

Switched Capacitor Circuits



Case 1: 100% Slewing

$$I_{bias} = C \cdot \frac{dV}{dt} = C \cdot \frac{V_{sig}}{T_s / 2} = 4 \cdot C \cdot V_{sig} \cdot f_{sig}$$

$$P = 2 \cdot V_{sig} \cdot I_{bias} \qquad SNR = \frac{0.5 \times V_{sig}^2}{k_B T / C}$$

$$\therefore P = 16 k_B T \cdot SNR \cdot f_{sig}$$

Case 2: 100% Linear Settling

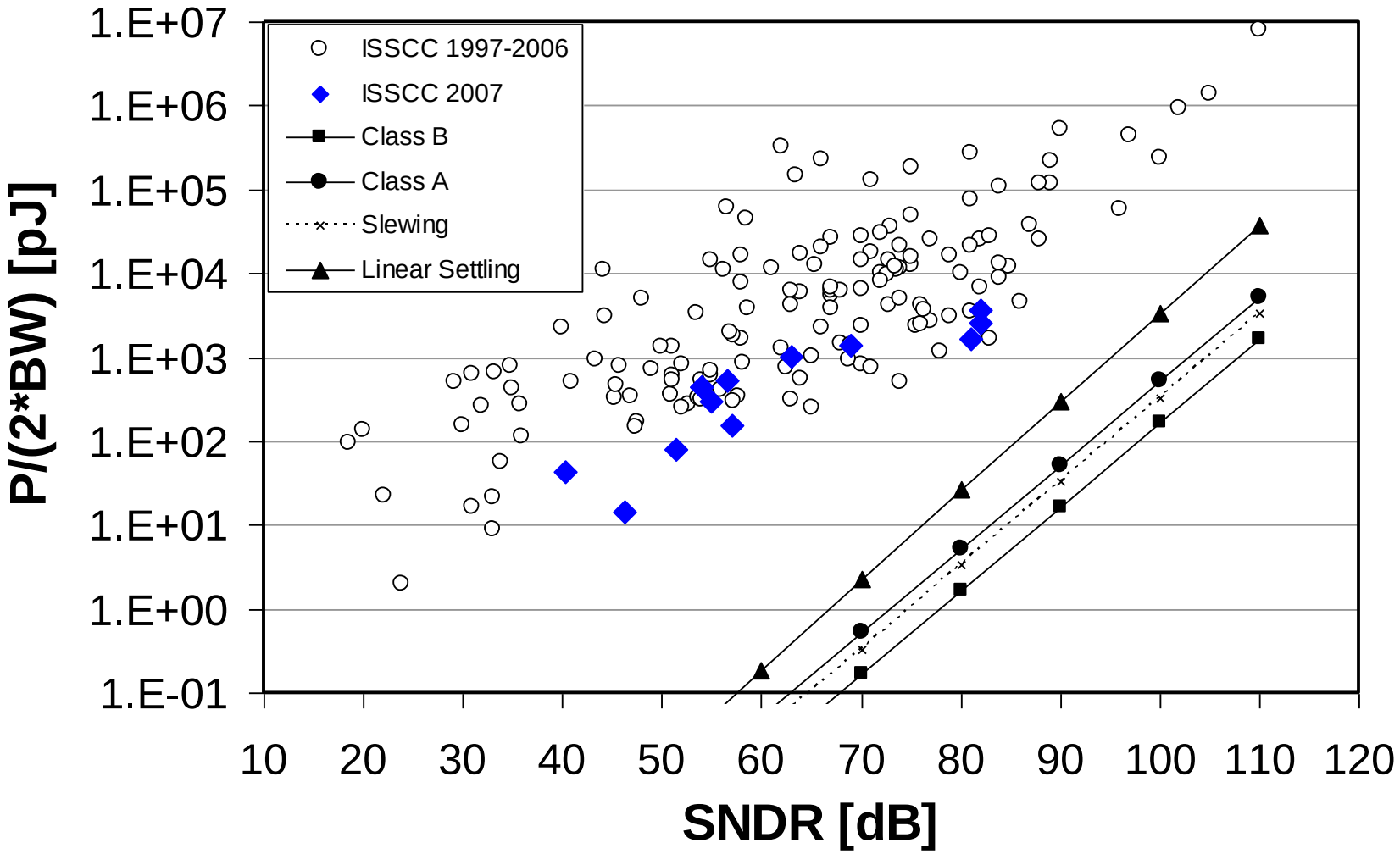
$$I_{bias} = C \cdot \left.\frac{dV}{dt}\right|_{max} = C \cdot \left.\frac{d}{dt}\right|_{max} \left[V_{sig} \left(1 - e^{-t/\tau} \right) \right] = C \cdot \frac{V_{sig}}{\tau}$$

Number of settling time constants: $N = \dfrac{T_s / 2}{\tau}$

$$\therefore P = 16 \cdot N \cdot k_B T \cdot SNR \cdot f_{sig}$$

- Much worse
  - E.g. N=6.9 for settling to 0.1% precision

Limit Lines


ISSCC 1997-2006
ISSCC 2007
Class B
Class A
Slewing
Linear Settling
P/(2*BW) [pJ]
1.E+07
1.E+06
1.E+05
1.E+04
1.E+03
1.E+02
1.E+01
1.E+00
1.E-01
10
20
30
40
50
60
70
80
90
100
110
120
SNDR [dB]

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Practical Limits

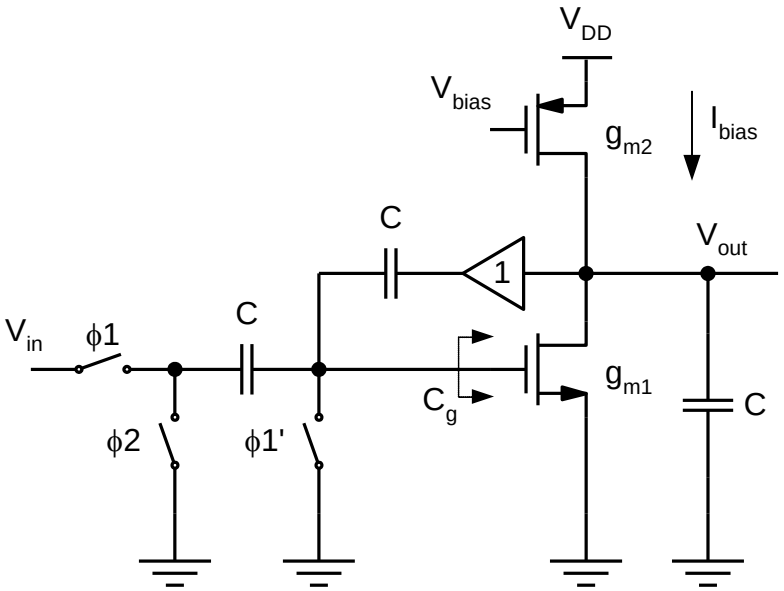
Discussion

- Orders of magnitude away from limits
- Slope of limit lines is much steeper than fit to experimental data
- What contributes to these large gaps?
  - Must keep in mind that ADCs are not just single capacitor circuits …
- The following analysis factors in practical considerations
  - Not fundamental, but somewhat unavoidable in today's implementations

Design Space Partitioning

- High SNR
  - Complexity ~1 (e.g. first integrator in sigma-delta ADC)
  - Limited by thermal noise
- Moderate SNR
  - Complexity ~Bits (e.g. pipelined ADC)
  - Partly limited by thermal noise
- Low SNR
  - Complexity ~2^{Bits} (e.g. flash ADC)
  - Limited by matching, quantization noise

High SNR SC-Stage (1)



- Considerations
  - Noise is multiple of k_BT/C (n_f)
  - Swing is only a fraction of V_{DD} (α)
  - Feedback factor (β)
  - g_m/I_D is upper bounded (especially if slewing must be avoided)

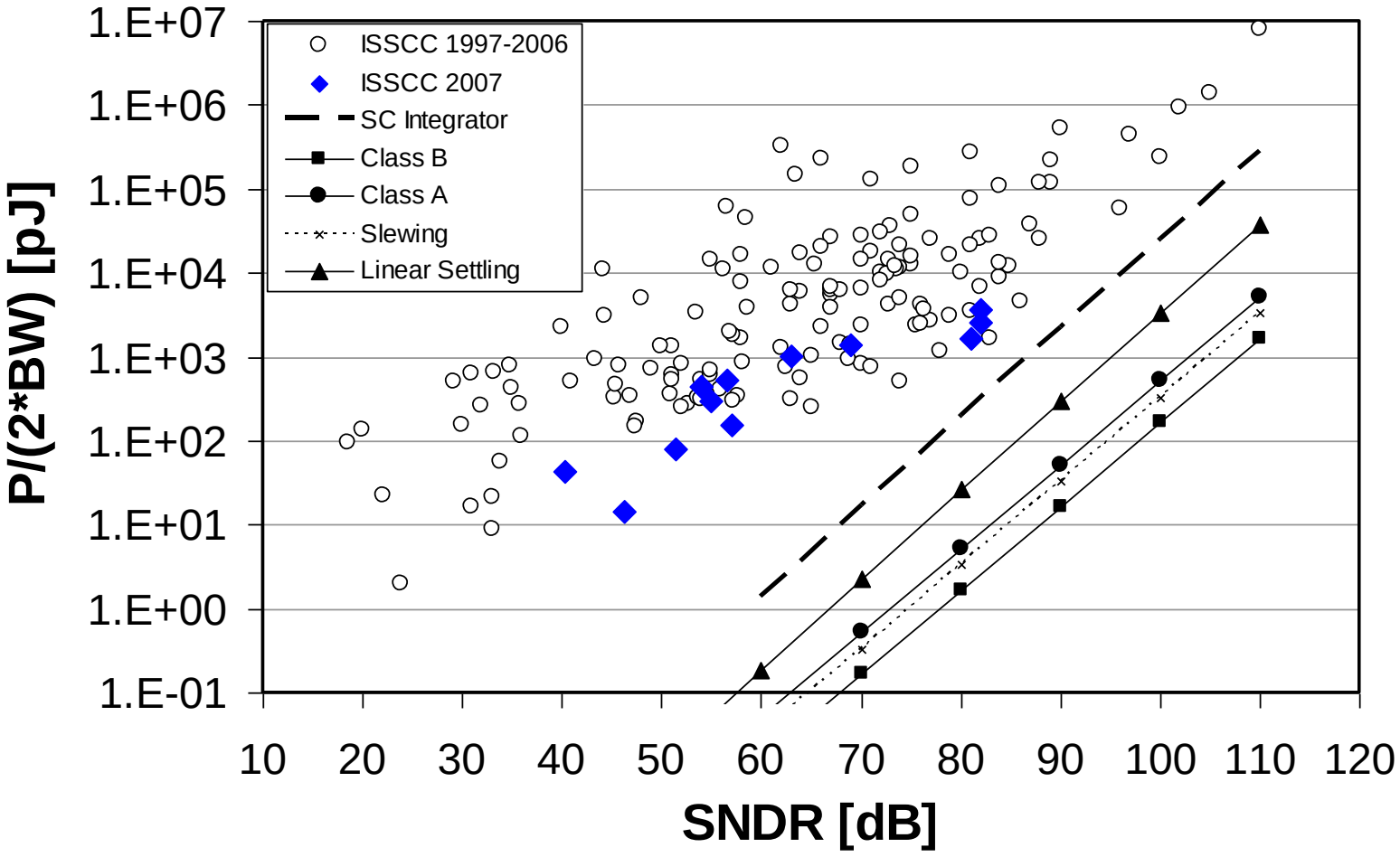
High SNR SC-Stage (2)

To avoid slewing: $\frac{g_{m1}}{I_{bias}} \leq \frac{1}{\beta \cdot V_{sig}}$

$$\therefore P = 16 \cdot N \cdot n_f \cdot \frac{1}{\alpha} \cdot k_B T \cdot SNR \cdot f_{sig} \cdot max\left(1, \frac{1}{\frac{g_{m1}}{I_{bias}} \cdot \beta \cdot V_{sig}}\right)$$

- Graph on following slide shows result assuming
  - n_f=5, α=2/3, β=0.5, onset of slewing

High SNR SC-Stage (3)

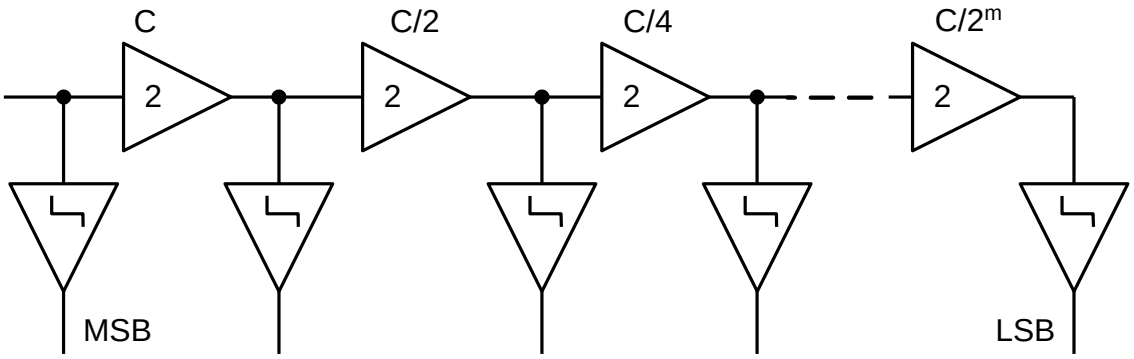


- Close to experimental data at high SNDR!

Medium SNR

- Consider two cases
- Pipeline ADC using SC stages
  - Partially limited by thermal noise
- Continuous time G_m–C integrator
  - Limited by distortion

Pipeline ADC



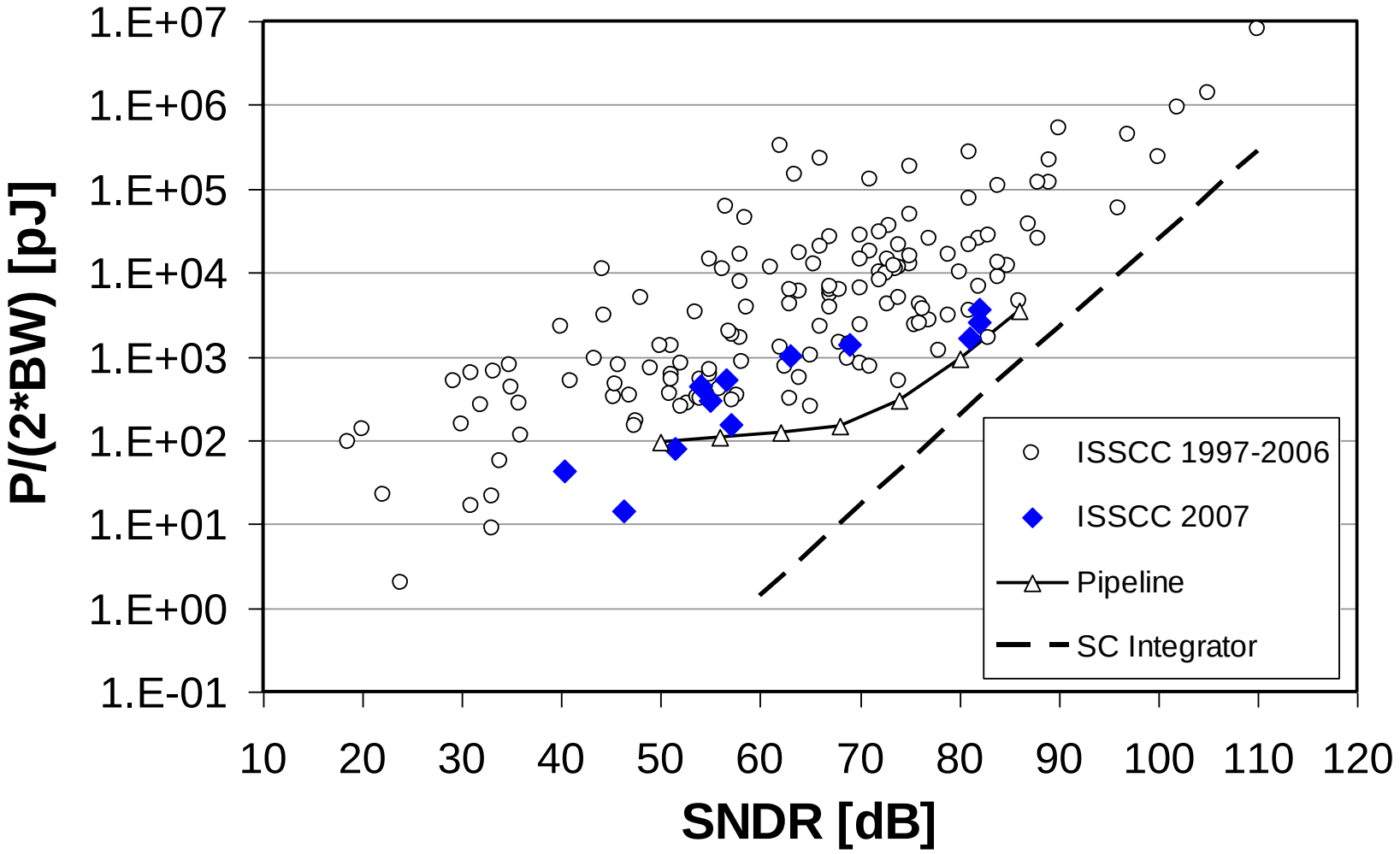
- Theoretical near optimum power scaling
  - Scale capacitance by gain of preceding stage
  - Stage 1 consumes half of total power
  - Adding one bit means power goes up 4x
- Caveat
  - Usually impractical to scale capacitors down to $C/2^m$

Stage Scaling Example

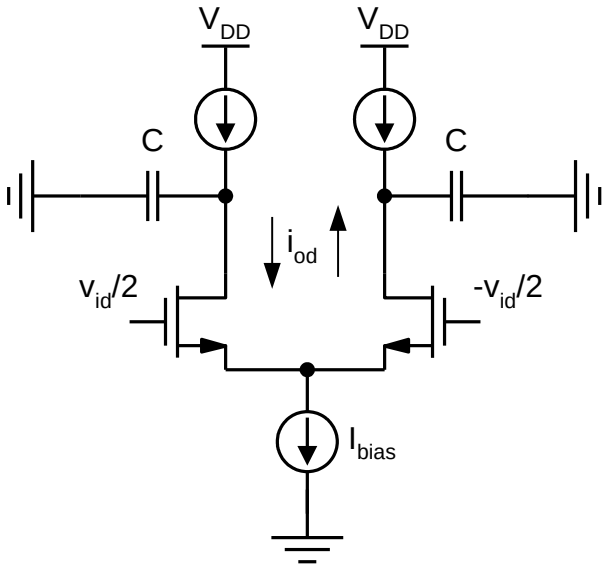
Number of Amplifiers	13	12	11	10
Stage Capacitances	1	1/4	1/16	1/64
	1/2	1/8	1/32	1/128
	1/4	1/16	1/64	*1/128*
	1/8	1/32	1/128	*1/128*
	1/16	1/64	*1/128*	*1/128*
	1/32	1/128	*1/128*	*1/128*
	1/64	*1/128*	*1/128*	*1/128*
	1/128	*1/128*	*1/128*	
	1/128	*1/128*		
	1/128			
ΣC	2.03	0.54	0.17	0.086
C_{single}	1/2	1/8	1/32	1/128
Relative Power Pipeline/Single SC Stage ($\Sigma C/C_{single}$)	4.06	4.32	5.44	11.01

- Example is simplistic, but in line with state-of-the art
  - 10bits ~0.5mW/MSample/s, 12bits ~2mW/MSample/s

Pipeline ADC Limit Line



G_m-C Integrator



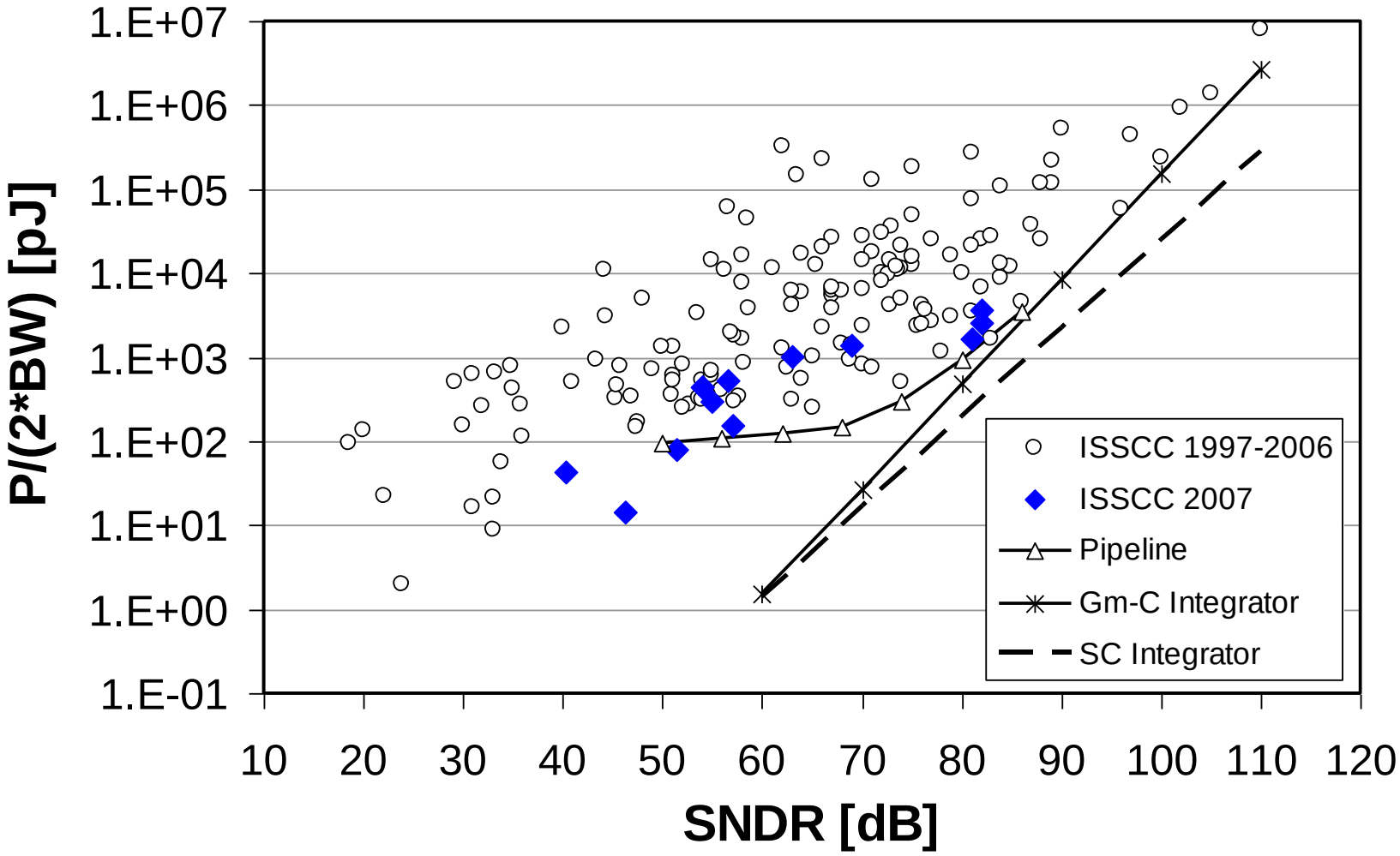
$$IM_3 \cong \frac{3}{32}\left(\frac{v_{id,max}}{V_{ov}}\right)^2$$

$$\eta_{cur} = \frac{i_{od,max}}{I_{bias}}$$

$$\eta_{cur} \cong \frac{v_{id,max}}{V_{ov}} = \sqrt{\frac{32}{3} IM_3}$$

- Only a small fraction of bias current can be steered into load
  - E.g. IM_3=60dB, η_{cur}=10%

Gm-C Limit Line



Low SNR

- Power of matching limited class-B circuit [Kinget, CICC 1996]

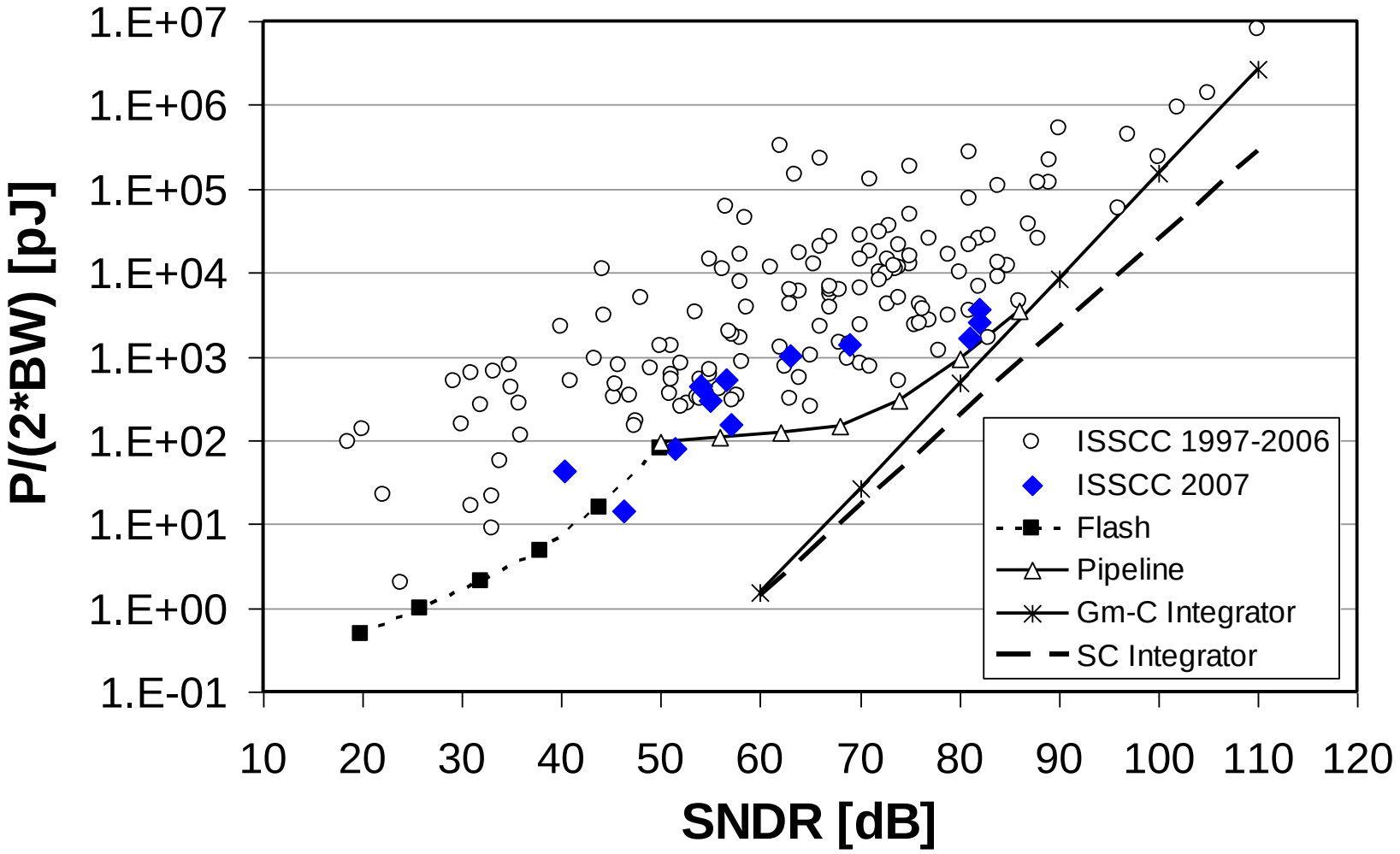
$$P = 24 \cdot C_{ox} \cdot A_{VT}^2 \cdot f_{sig} \cdot \left(\frac{V_{sig,rms}}{3 \cdot \sigma_{Vos}} \right)^2$$

- Refined result for flash ADC, assuming
  - Class-A, 1/2 LSB matching with 3σ-confidence, 2^B components, additional E_{dyn} per clock cycle, partial supply usage (α)

$$P = \left(12\pi \cdot \frac{1}{\alpha} \cdot C_{ox} \cdot A_{VT}^2 \cdot 2^{3B} + 2 \cdot E_{dyn} \cdot 2^B \right) \cdot f_{sig}$$

- Example: α=2/3, C_{ox}=15fF/μm^2, A_{Vt}=3mV$\cdot\mu$m, E_{dyn}=60fJ (~10gates in 0.13μm CMOS)

End Result


1.E+07
1.E+06
1.E+05
1.E+04
1.E+03
1.E+02
1.E+01
1.E+00
1.E-01
P/(2*BW) [pJ]
10
20
30
40
50
60
70
80
90
100
110
120
SNDR [dB]
ISSCC 1997-2006
ISSCC 2007
Flash
Pipeline
Gm-C Integrator
SC Integrator

Discussion

- Shown results include only minor assumptions about technology
- Scaling brings some good, some bad news offsetting each other
  - – Lower V_{DD}, lower V_{swing}/V_{DD}, …
  - + Lower E_{dyn}, higher f_t enables moderate/weak inversion operation with high g_m/I_D,…
- Limit lines won't move much, unless someone hands us a new disruptive technology

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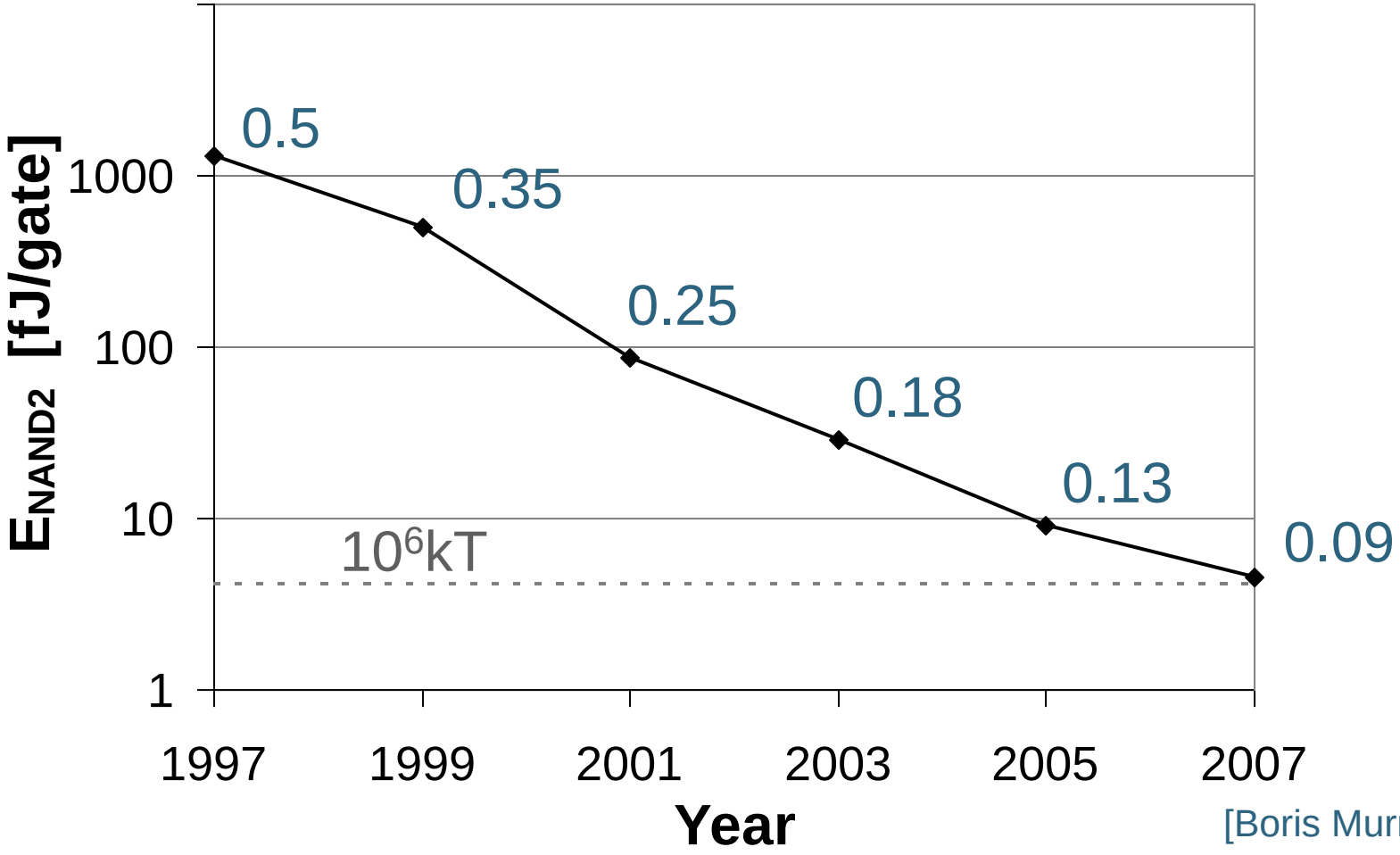
Digitally Assisted Analog Circuits

Future Opportunities

- More intelligent ADCs
  - Improved average power dissipation by adapting to instantaneous speed/resolution requirements
- "Minimalistic" ADCs using significantly simpler circuits
  - Analog front-end:
    - Meet noise specification
    - Relax systematic error specs, e.g. distortion
  - Digital compensation of resulting non-idealities
  - Digital post-processing is (within limits) "free" in terms of area and energy

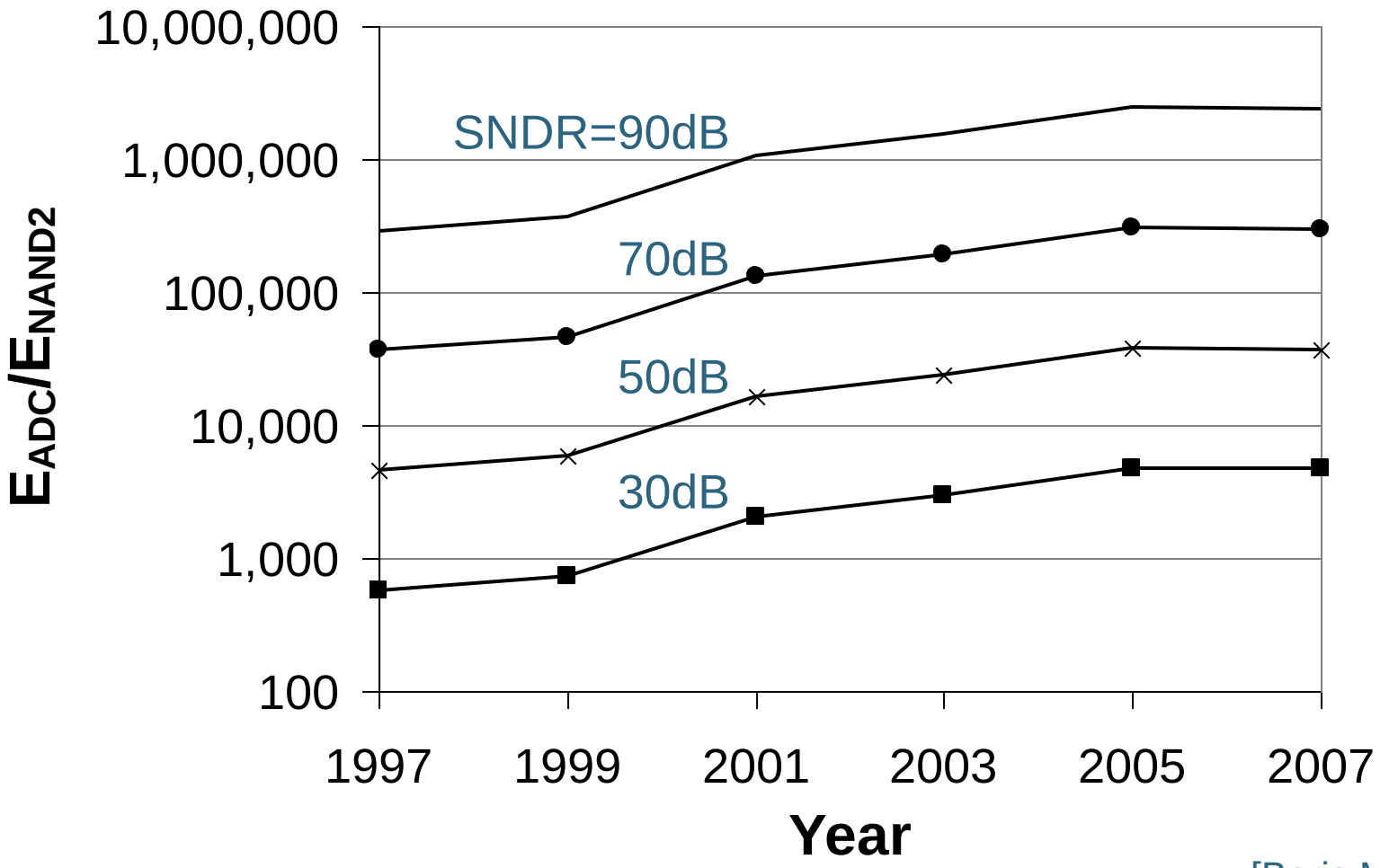
Digital Logic Energy Trend

Mainstream ADC technologies, standard logic library data



[Boris Murmann]

ADC/Digital Logic Energy Ratio



[Boris Murmann]

Energy Ratio in 2007

- Interpretation for digitally enhanced ADCs (energy centric)

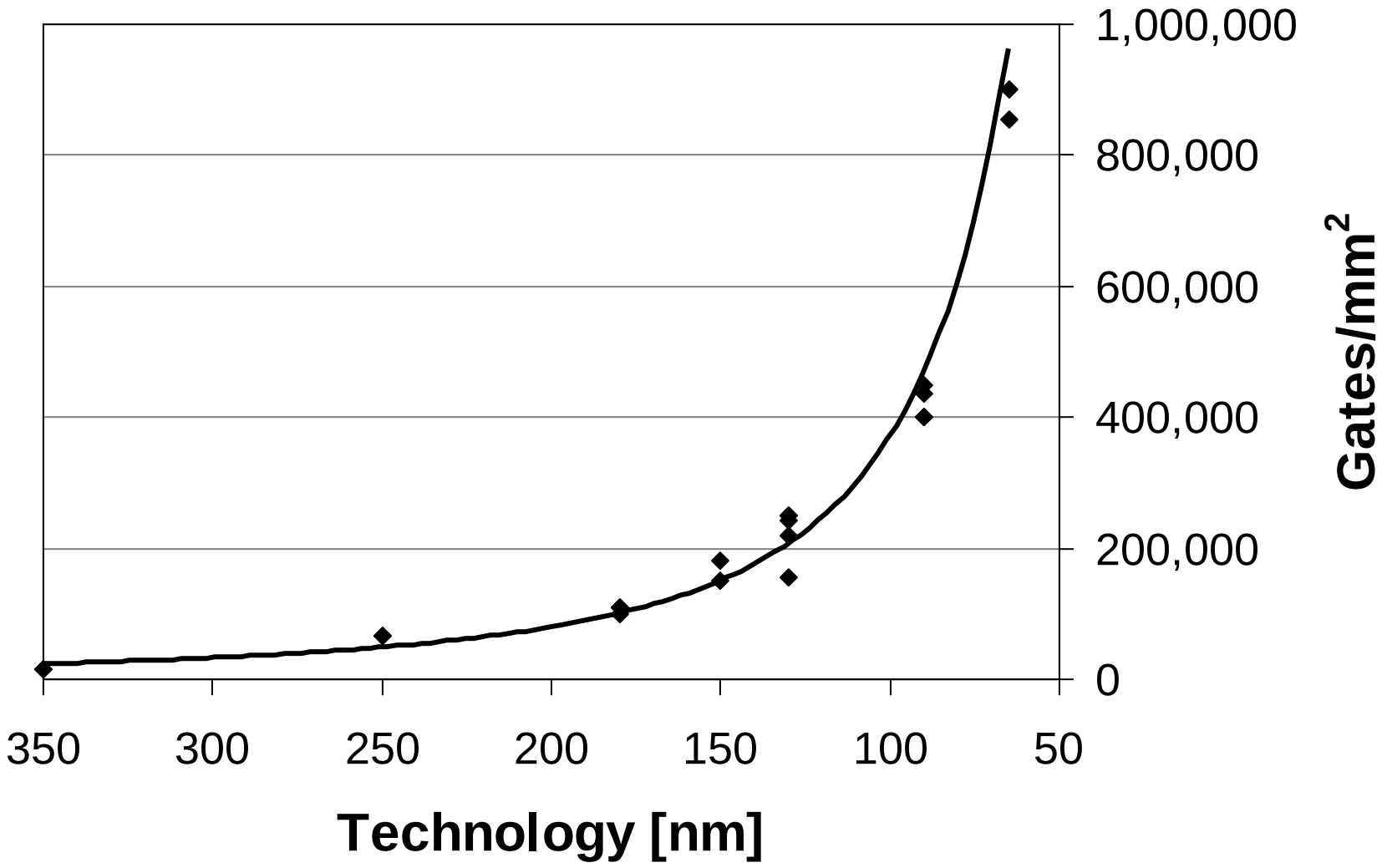
SNDR	E_{ADC}/E_{NAND2}
30	4,679
50	37,432
70	299,479
90	2,396,045

⇨ Additional digital processing is costly!

⇨ Several tens of thousand gates are "free"

⇨ Use as many gates as you can fit…

Digital Logic Gate Density Trend



EE 240C
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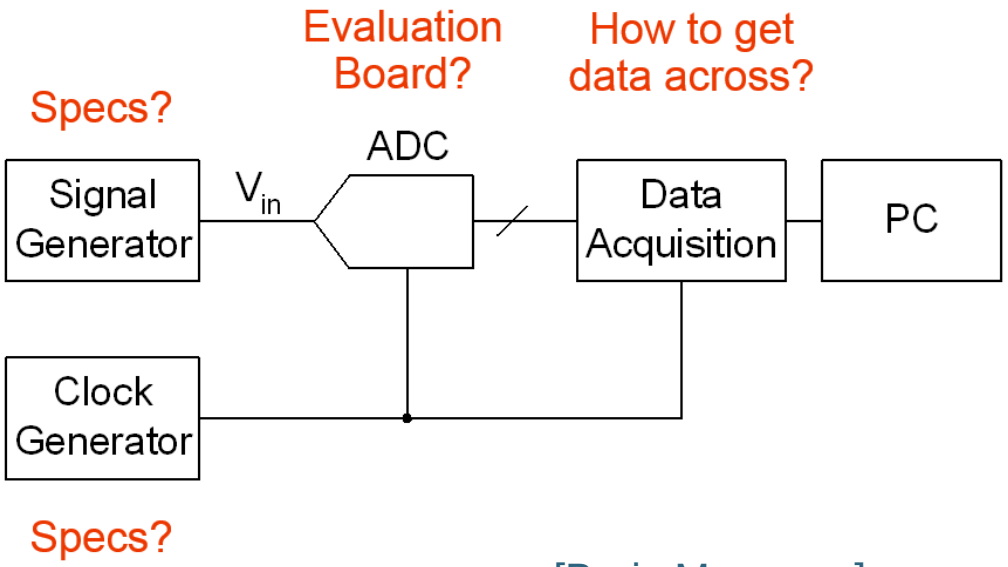
ADC Testing

Testing ADCs

- Test equipment
  - Signal source
  - Clock generator
  - Supplies
- Test fixture
- Data acquisition



[Boris Murmann]

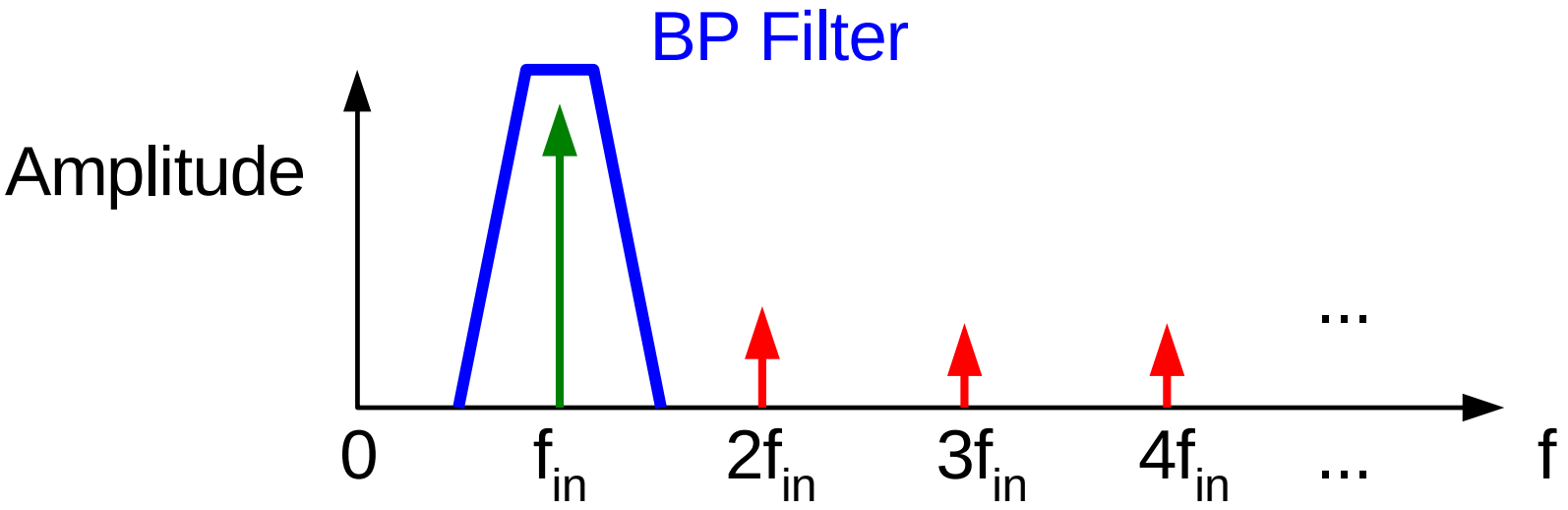
Signal Source

- Want: SFDR>85dB @ $f_{in}=f_s/2=37.5MHz$

- Harmonic distortion (f>1MHz): -35dBc
- Need something better...

- ~ $40k
- f=100kHz...3GHz
- Harmonic distortion (f>1MHz): -30dBc !

Filtering Out Harmonics



- Given HD=-30dBc, we need a stopband rejection > 60dB to get SFDR>90dB

Available Filters

Elliptical Function Bandpass Filters 1kHz to 20MHz

www.tte.com, or
www.allenavionics.com

Stopband to Passband Bandwidth Ratios

Series Number	BWR	*Stopband Attenuation
Q34	4.0:1	-40dBc
Q40	4.0:1	-40dBc
Q36	10.0:1	-60dBc
Q54	2.5:1	-40dBc
Q70	3.5:1	-60dBc
Q56	3.5:1	-60dBc

- Want to test at many frequencies
  → Need to have many different filters!

Tunable Filter

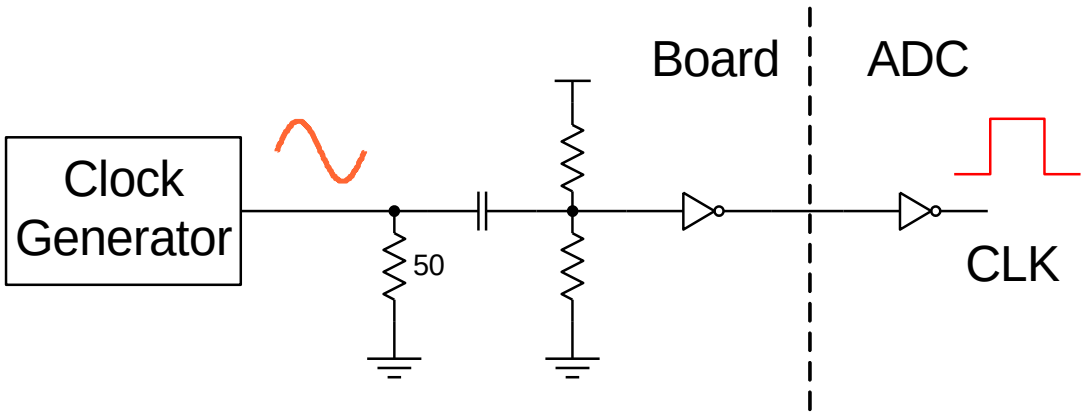
www.klmicrowave.com

K&L Model	Frequency Range (MHz)	Passband Insertion Loss	Length Inch/mm	Width Inch/mm	Height Inch/mm
5BT-30/76-5-N/N	30-76	1.3 dB Max	9.80/249	5.38/137	2.75/50
5BT-63/125-5-N/N	63-125	1.3 dB Max	9.80/249	5.38/137	2.75/50
5BT-125/250-5-N/N	125-250	1.3 dB Max	9.80/249	5.38/137	2.75/50
5BT-250/500-5-N/N	250-500	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-375/750-5-N/N	375-750	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-500/1000-5-N/N	500-1000	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-750/1500-5-N/N	750-1500	1.0 dB Max	9.80/249	5.38/137	2.75/50
5BT-1000/2000-5-N/N	1000-2000	1.0 dB Max	7.38/187	2.88/73	2.75/50
5BT-1200/2600-5-N/N	1200-2600	1.0 dB Max	7.38/187	2.88/73	2.75/50

Beware: The filters themselves also introduce distortion

Clock Generator

- The clock signal controls sampling instants – which we assumed to be precisely equidistant in time (period T)
  - See earlier lecture for a discussion of aperture uncertainty
- Typically use sine wave and "square up" with inverter chain



Jitter Supression

- Once we have a good enough generator, other circuit and test setup related issues may determine jitter
- Usually, clock jitter in the single-digit picosecond range can be prevented by appropriate design techniques
  - Separate supplies
  - Separate analog and digital clocks
  - Short inverter chains between clock source and destination
- Few, if any, other analog-to-digital conversion non-idealities have the same symptoms as sampling jitter
  - RMS noise proportional to input frequency
  - RMS noise proportional to input amplitude
- So, if sampling clock jitter is limiting your dynamic range, it's easy to tell, but may be difficult to fix ...

Evaluation Board

- Planning begins with converter pin-out
  - Uhps, my clock pin is right next to a digital output …
- Not "black magic", but requires extreme care
- Key aspects
  - Supply/ground routing
  - Bypass capacitors
  - Coupling between signals
- Good idea to look at ADC vendor datasheets for example layouts/schematics/application notes
  - E.g. Analog Devices AD9235 Data Sheet

One Thing to Remember…

- A converter does not just have one "input"
  - Clock
  - Power supply, ground
  - Reference voltage
- For good practices on how to avoid issues see e.g.
  - Analog Devices Application Note 345:
    "Grounding for Low-and-High-Frequency Circuits"
  - Maxim Application Note 729:
    "Dynamic Testing of High-Speed ADCs, Part 2"

How to Get the Bits Off Chip?

- "Full swing" CMOS signaling works well for $f_{CLK} < 100MHz$
- But we want to build faster ADCs …
- Alternative to CMOS: LVDS – Low Voltage Differential Signaling
- LVDS vs. CMOS:
  - Higher speed, also more power efficient at high speed
  - Two pins/bit!

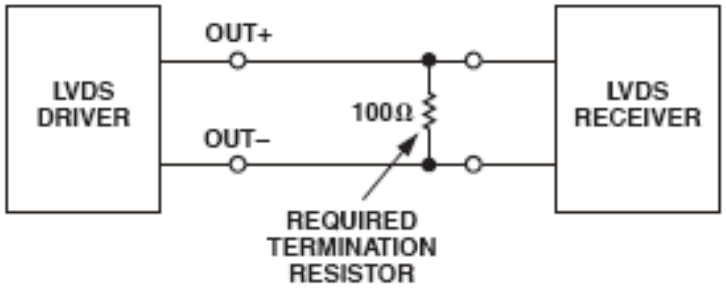
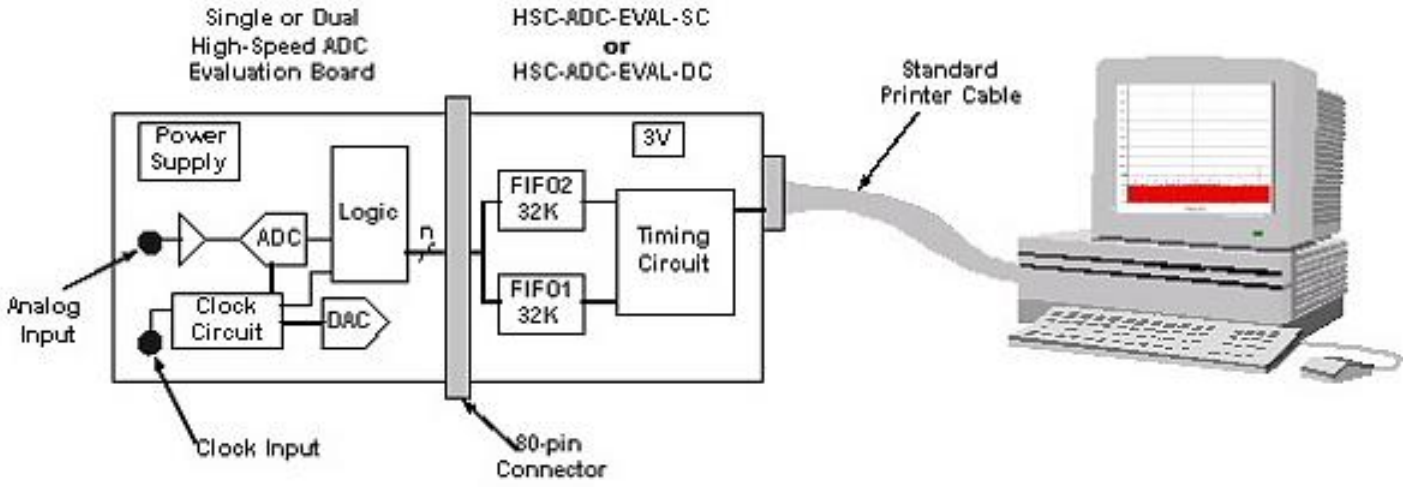


Figure 1. LVDS Output Levels

Analog Devices Application Note 586: "LVDS Data Outputs for High Speed ADCs"

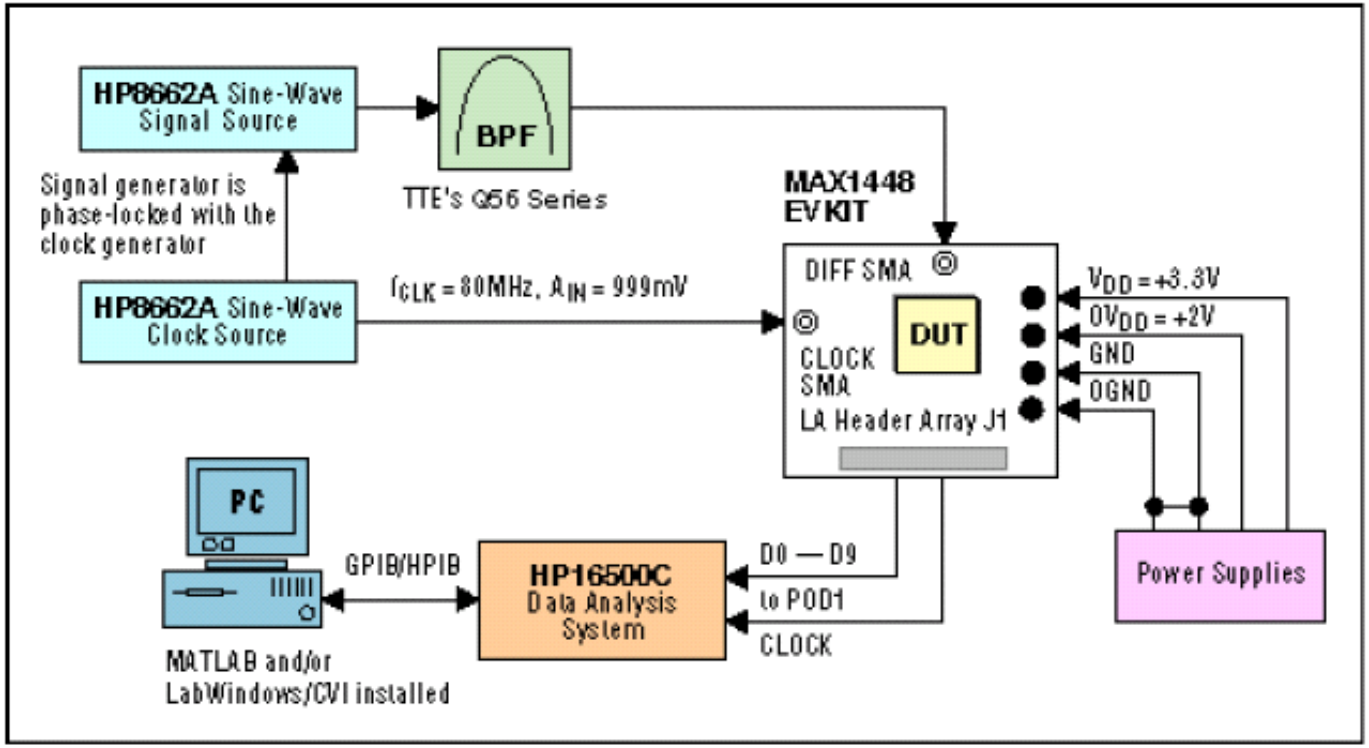
Data Acquisition

- Several options:
  - Logic analyzer with PC interface
  - FIFO board, interface to PC DAQ card
  - Vendor kit, simple interface to printer port:



[Analog Devices, High-Speed ADC FIFO Evaluation Kit]

Complete Setup



[Maxim Application Note 729: "Dynamic Testing of High-Speed ADCs, Part 2]