

EE 240C

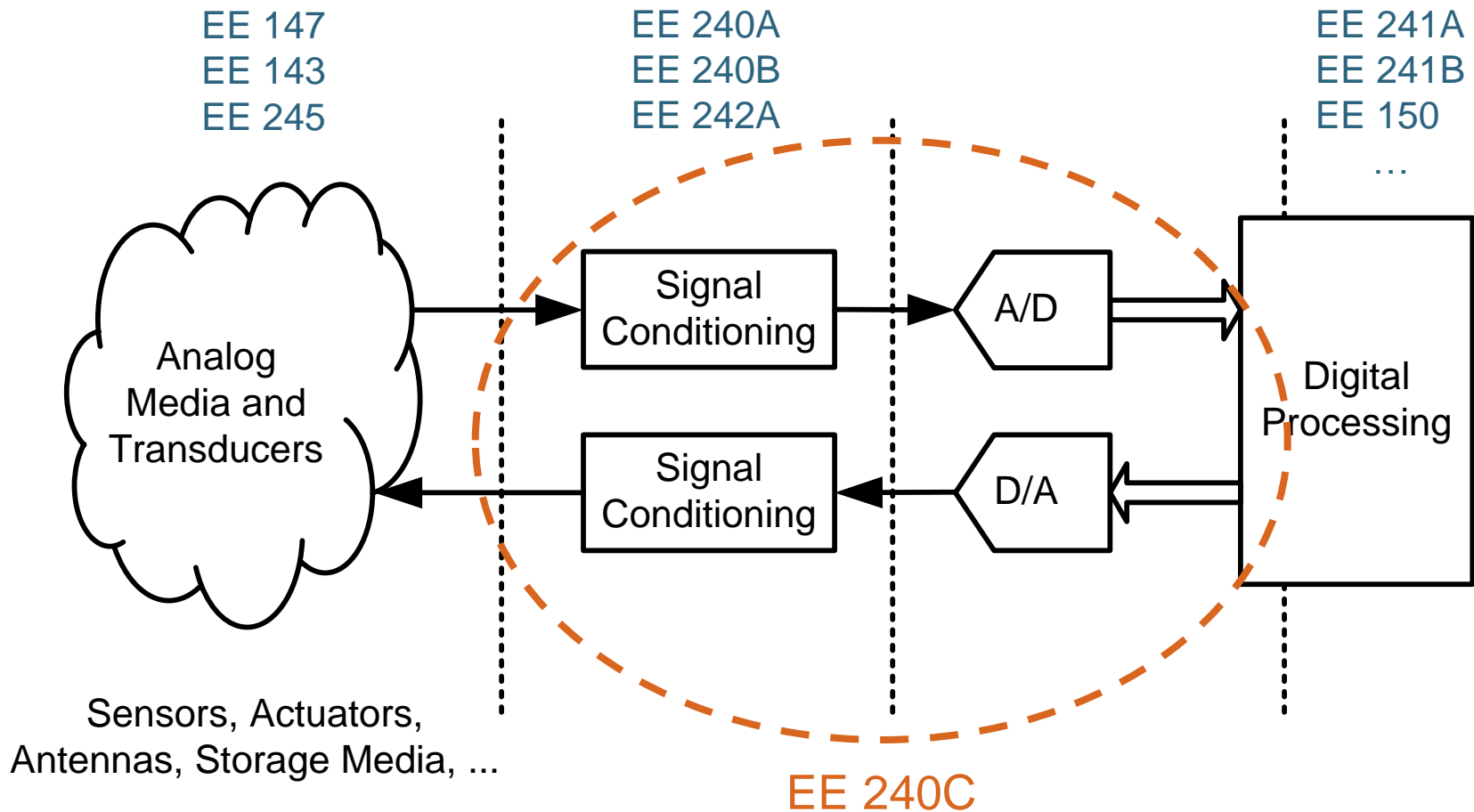
Analog-Digital Interface Integrated Circuits

Topics and Motivation

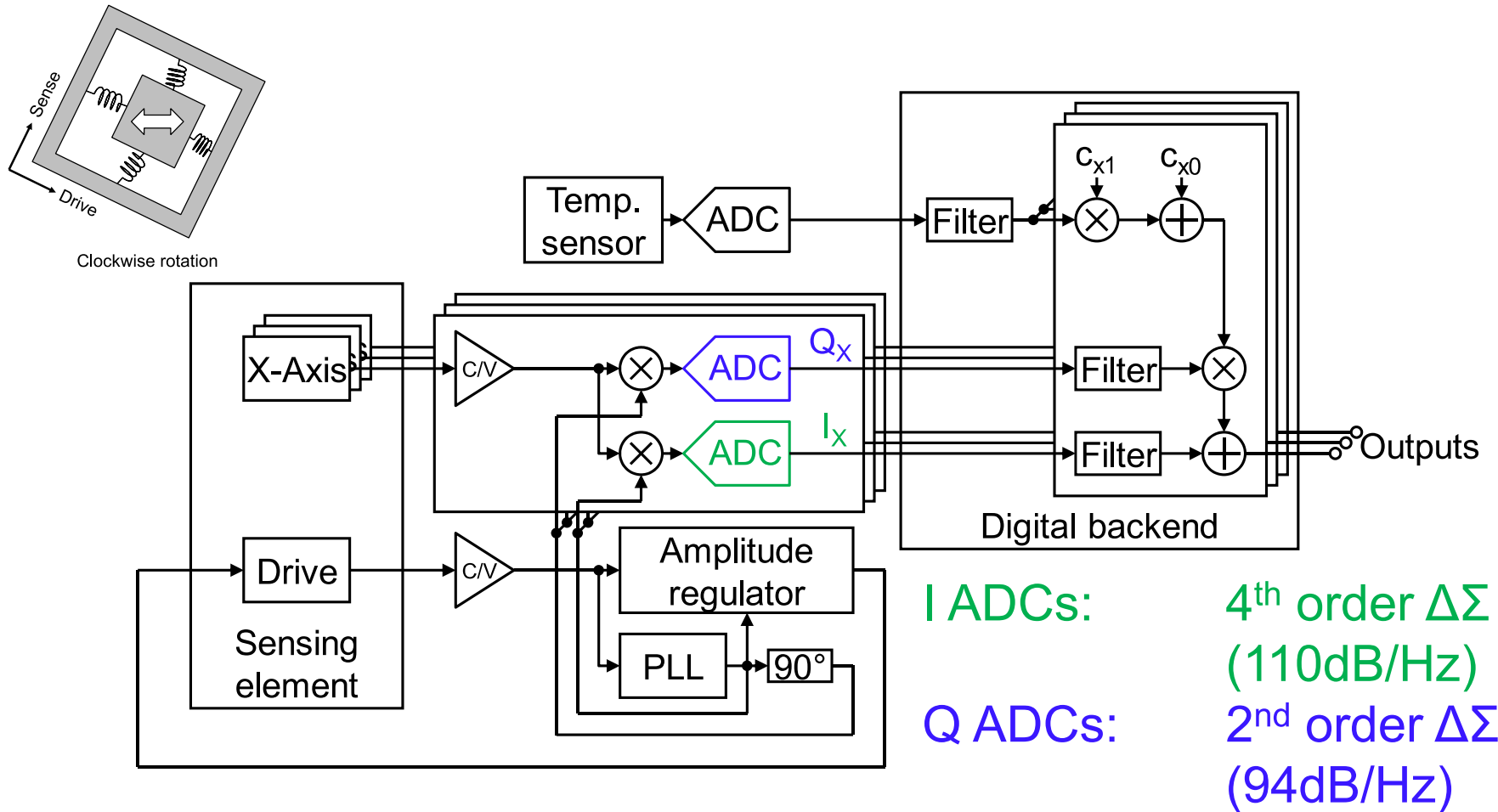
Johan Vanderhaegen
jpv@berkeley.edu

(Based on slides by Bernhard Boser)

Mixed Signal System

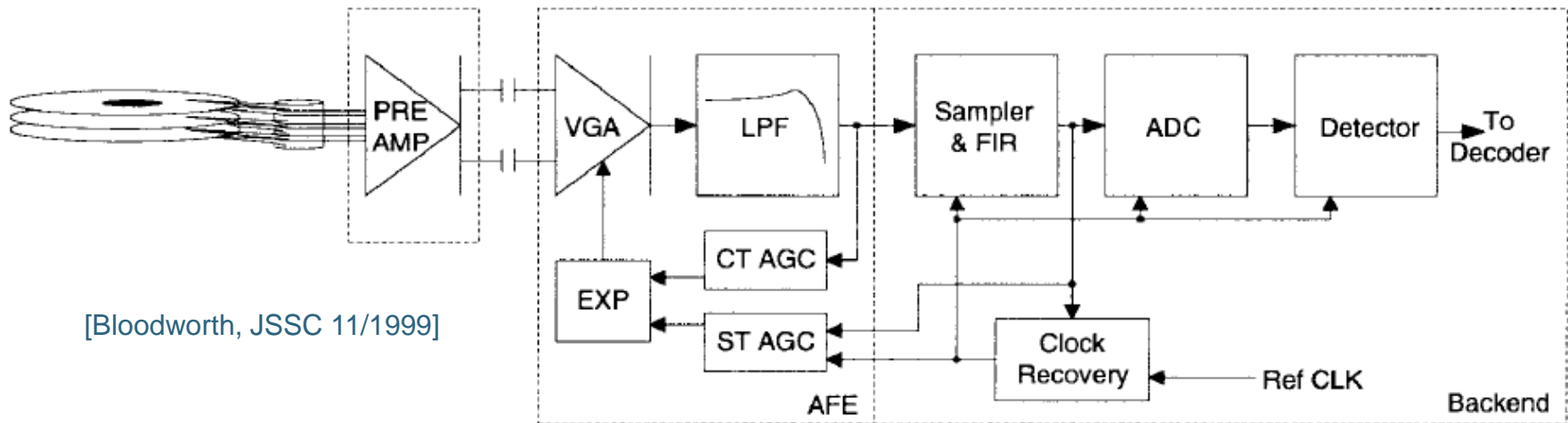


Example: Gyroscope Front-End



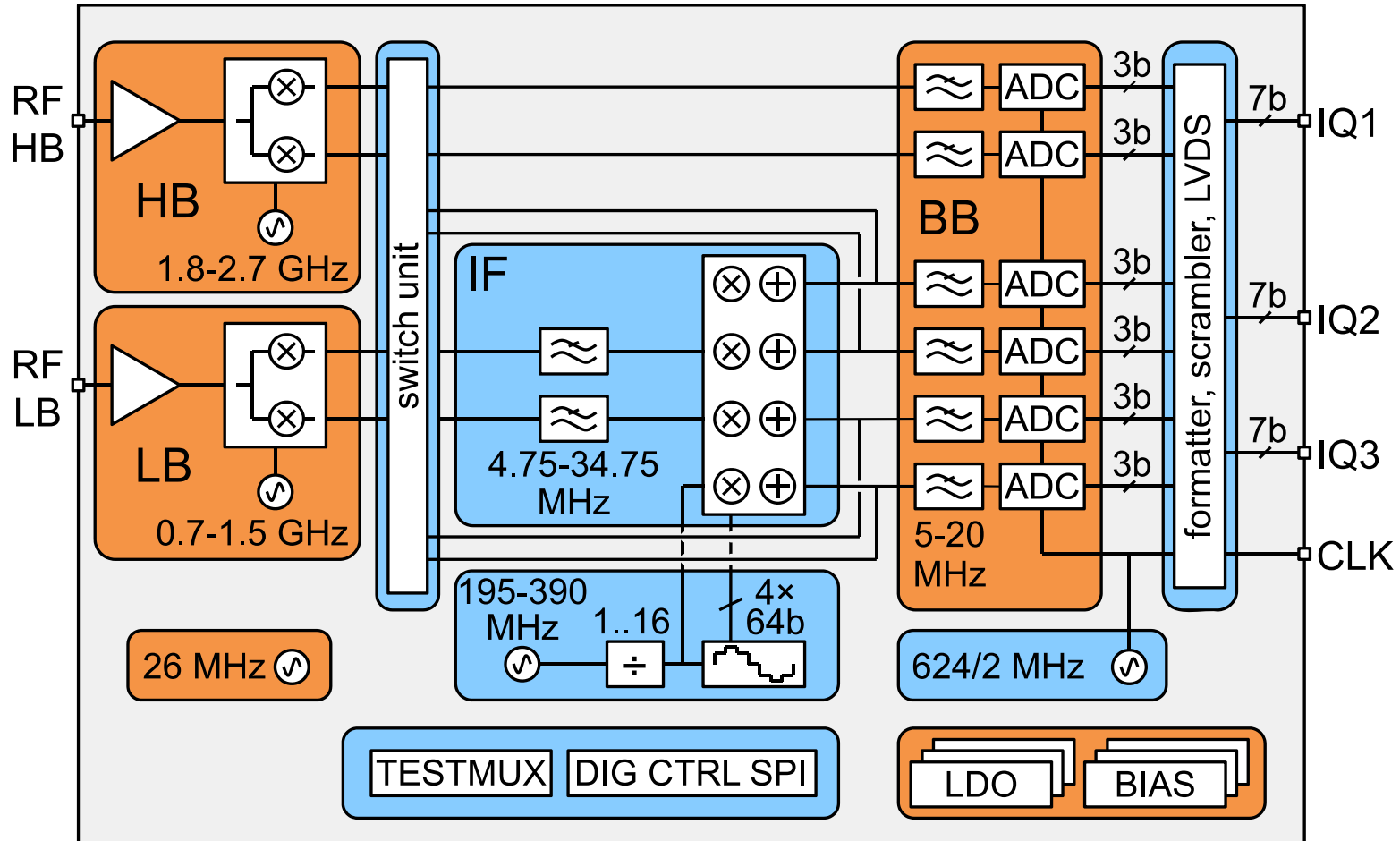
Ezekwe, Chinwuba D., Wolfram Geiger, and Torsten Ohms. "27.3 A 3-axis open-loop gyroscope with demodulation phase error correction." Solid-State Circuits Conference-(ISSCC), 2015 IEEE International. IEEE, 2015.

Example : Hard Disk Drive



AGC Specifications		LPF Specifications	
Input Signal Range	$45 \text{ mVppd} < V_{IN} < 500 \text{ mVppd}$	LPF Bandwidth	$20 \text{ MHz} \leq f_c \leq 120 \text{ MHz}$
Output Target	1.400 Vppd	Cutoff Variation	$< \pm 2.5 \%$
PGA Gain Settings	-3 dB, 3 dB, 9 dB	Group Delay Variation ($0.30f_c$ to f_c)	$< 5 \%$
VGA Gain Range	$-24 \text{ dB} \leq A_V \leq 0 \text{ dB}$	Group Delay Variation (f_c to $1.75f_c$)	$< 8 \%$
w/Extended Range	$-30 \text{ dB} \leq A_V \leq 6 \text{ dB}$	Group Delay Adjustment	$\pm 30 \%$
AFE THD	$< 1.0 \%$	Boost	0 dB to 15 dB at f_c
AFE SNR	$> 35 \text{ dB}$	CT Acquisition Time	$< 10 \text{ bytes}$
AFE Output Offset	$< 5.0 \text{ mV}$	Power Dissipation	$< 250 \text{ mW}$

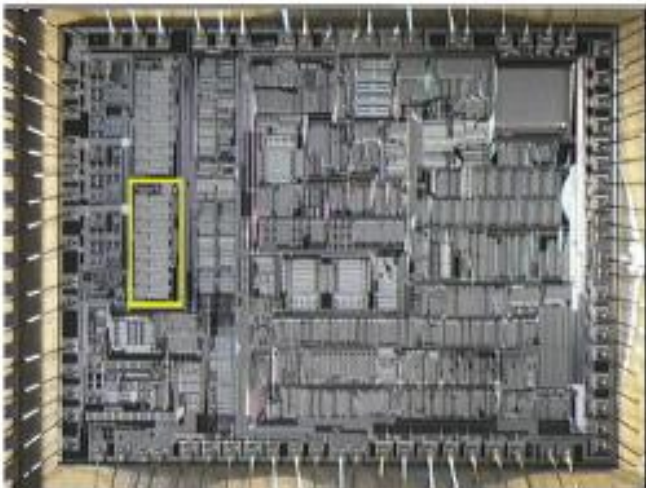
Example: Cellular LTE Front-End



Sundström, Lars, et al. "A receiver for LTE Rel-11 and beyond supporting non-contiguous carrier aggregation." *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*. IEEE, 2013.

Why Digital Processing?

- Digital circuitry:
 - Cost/function decreases by 29% each year
→ 30X in 10 years
- Analog circuitry:
 - Cost/function is constant
 - Dropping supply voltages threaten feasibility



Digital Television IC:
1 μ m (1995) vs 0.35 μ m (2002)

- Digital: 10x smaller
- Analog: approximately same size

[M. Pelgrom, *Analog-to-Digital Conversion*, 2nd Ed., Springer, 2013]

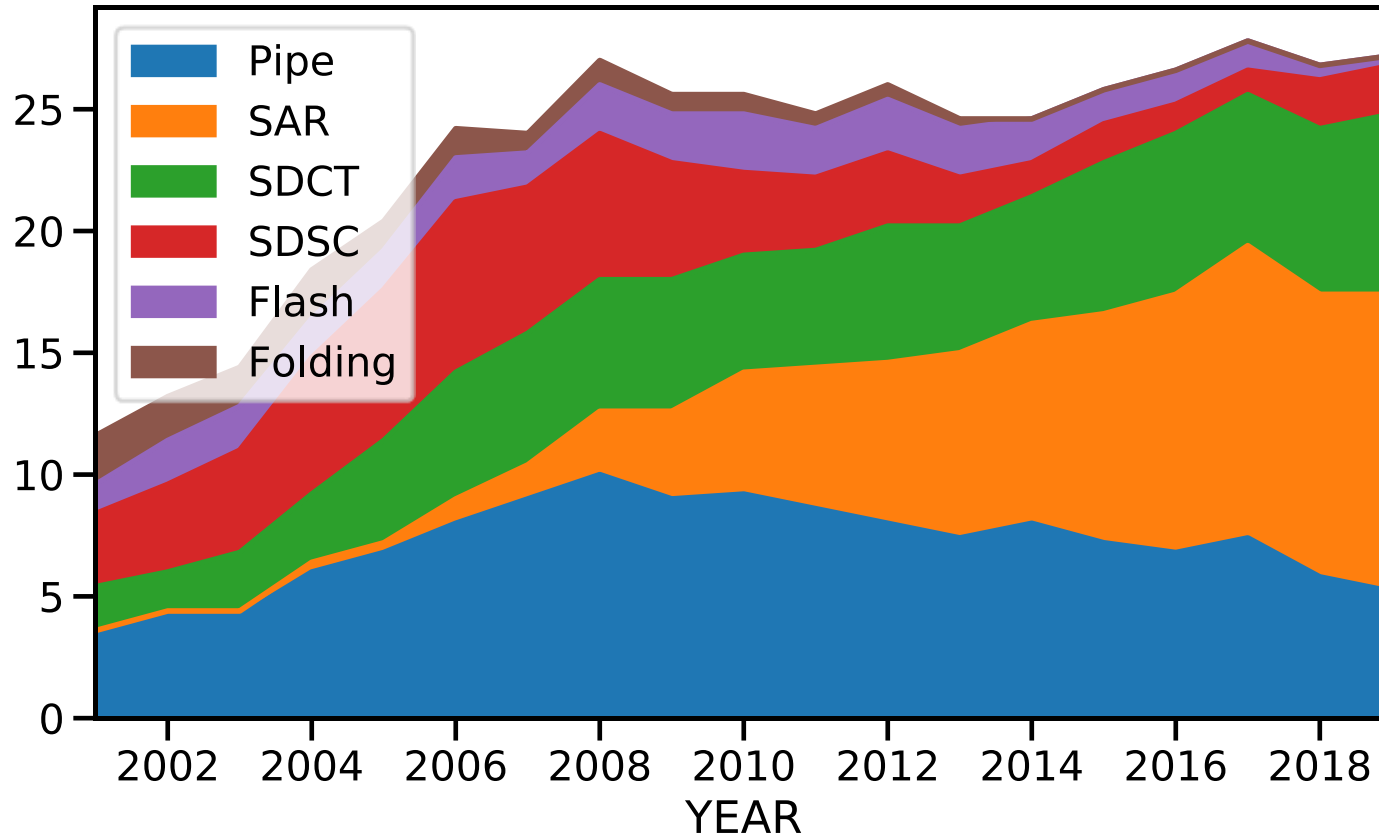
Why Analog Processing?

- The “real” or “physical” world is analog
- Examples:
 - Digital Audio
 - RF receiver
 - Wireline communications

Course Topics

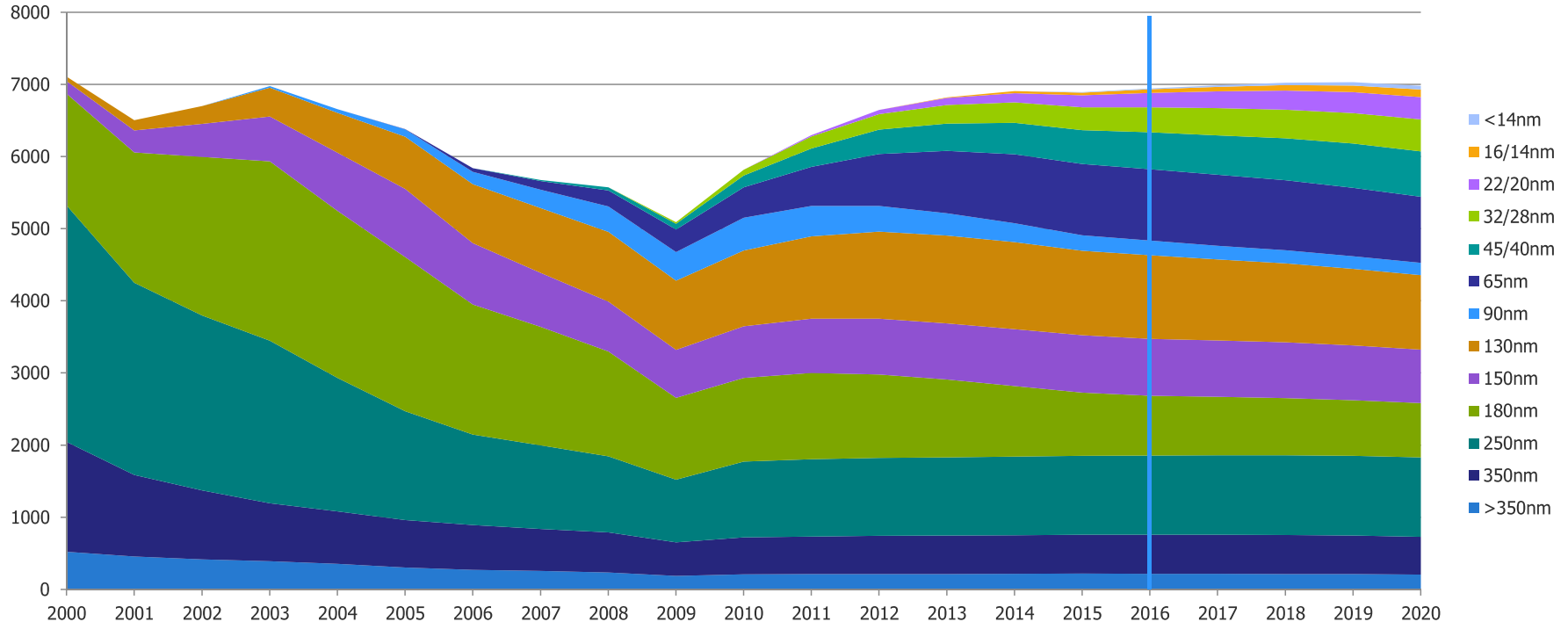
- Analog-Digital Interfaces
 - A/D Converters & D/A Converters
 - Sampling, Quantization
 - Performance Metrics & Limits
 - Architecture Tradeoffs
- Filters
 - Types of filters
 - Synthesis
 - Implementations:
 - Biquads versus Ladders
 - Continuous Time versus Switched Capacitor

Architectures of Published ADCs (ISSCC and VLSI)



- Evolution due to ADC improvements, technology shift, and focus on low power
- Source data: B. Murmann, "ADC Performance Survey 1997-2019," [Online]. Available: <http://web.stanford.edu/~murmman/adcsurvey.html>
- TI arch. combined with core arch. (e.g. SAR and TI SAR); other arch, (10-15%) not incl.

IC Design Start per Technology Node



Source: International Business Strategies, Inc. 2015

R. Subramanian- Semicon West 2016

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www.mentor.com

Complexity in IC Design

- Model hierarchy
 - Behavioral
MATLAB, Simulink, CppSim, System-Verilog, Verilog-A(MS)
 - Structural
(wo/ and w/ non-idealities)
MATLAB, Simulink, CppSim, System-Verilog, Verilog-A(MS)
 - Circuits
SPICE, Spectre
 - Silicon
- Development practices
 - Version control
 - Unit tests

EE 240C

Analog-Digital Interface Integrated Circuits

Organization

Johan Vanderhaegen
jpv@berkeley.edu

Instructor

Johan Vanderhaegen

- IC Design Lead,
Google / Verily Life Sciences,
2015 – Present
- IC Designer (ADC, sensor, and
sensor signal path topics)
Robert Bosch Research and
Technology Center, 2005 – 2015
- Graduate Student,
UC Berkeley
- jpv@berkeley.edu
- Lectures:
Wed 9am–12pm 299 Cory
- Office Hours:
Wed 8am – 9am 299 Cory
Mon 3:30pm – 4:30pm
<https://meet.google.com/ffa-uvqk-ayy>

Course Website

- bcourses (slides)
- <http://inst.eecs.berkeley.edu/~ee240c>

References

- Books (not required)
 - *Converters*
 - M. Pelgrom, *Analog-to-Digital Conversion*, Springer, 3rd Ed., 2017
 - F. Maloberti, *Data Converters*, Springer, 2007
 - M. Gustavsson, J. Wikner, N. Tan, *CMOS Data Converters for Communications*, Kluwer, 2002
 - R. v. d. Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, 2nd Ed., Kluwer, 2003
 - *Oversampling Converters*
 - S. Pavan, R. Schreier, G. Temes, *Understanding Delta-Sigma Data Converters*, 2nd Ed., Wiley-IEEE Press, 2017
 - S. Norsworthy, R. Schreier, G. Temes, *Delta-Sigma Data Converters*, Wiley-IEEE Press, 1996

References

- Books
 - *Filters*
 - K. Su, *Analog Filters*, 2nd Ed., Kluwer, 2002
 - R. Schaumann, H. Xiao, M. Van Valkenburg, *Design of Analog Filters*, 2nd Ed., Oxford University Press, 2009
 - A. Zverev, *Handbook of Filter Synthesis*, Wiley-Interscience, 1963
- Journals and Conferences, <http://ieeexplore.ieee.org>
 - IEEE Journal of Solid-State Circuits (JSSC)
 - IEEE International Solid-State Circuits Conference (ISSCC)
 - ...

Prerequisites

- Transistor-level circuit design course
 - Device physics and models
 - Transistor level analog circuits, elementary gain stages
 - Frequency response, feedback, noise
 - E.g. EE 140 or 240A, 240 B
 - Gray, Hurst, Lewis, Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Ed, Wiley, 2011
 - Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd Ed. McGraw-Hill.
- Familiarity with Spectre, Matlab, Simulink, Verilog-A
- Basic signals and systems
 - Laplace and z-transforms
 - Noise power spectral density

Assignments

- Homework: (20%)
 - Lowest HW score is dropped in final grade calculation
- Project: (30%)
 - Design of a high performance interface
 - Class project
 - Project report in the format of an IEEE journal paper
- Midterm & Final Exam (50%)
 - Midterm: Oct 16th (in class)
 - Final: Thu Dec 19th

Acknowledgements

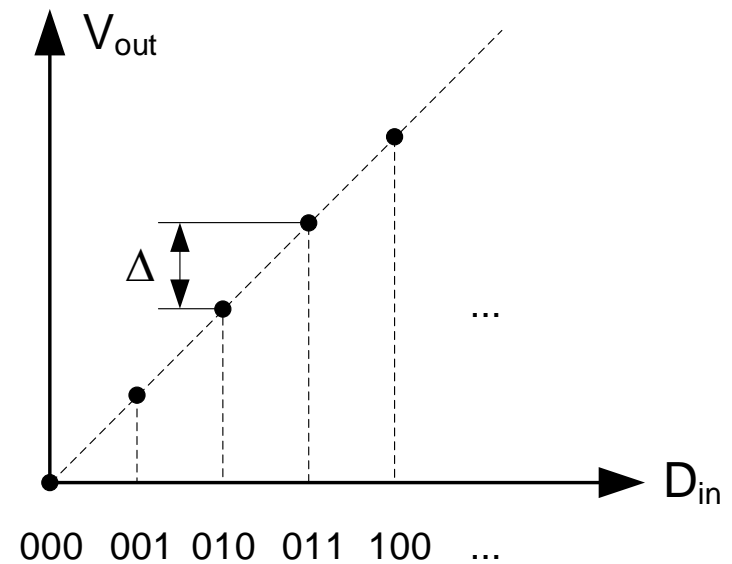
- Bernhard Boser, UC Berkeley
- Paul Gray, UC, Berkeley
- Boris Murmann, Stanford University
- Eric Swanson, Crystal Semiconductor
- Haideh Khorramabadi
- Aaron Buchwald, Mobius Semiconductor
- Countless books and articles

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Analog-Digital Interface Integrated Circuits

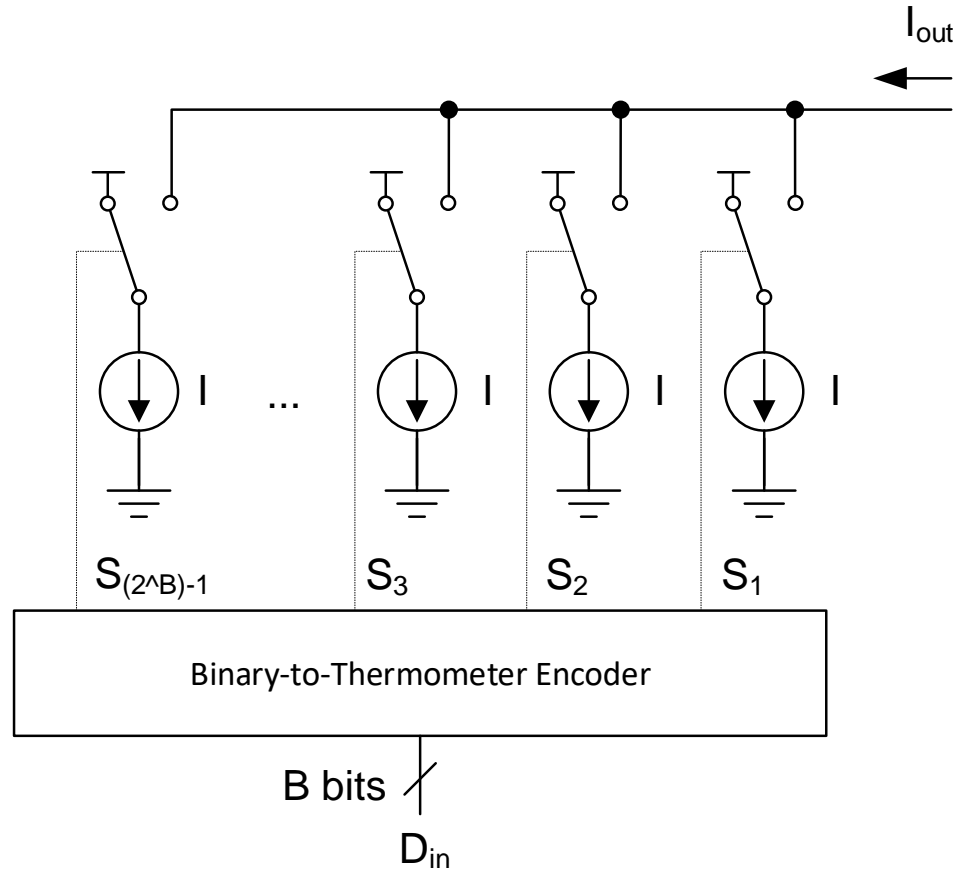
Digital-to-Analog Converter

Digital-to-Analog Converter

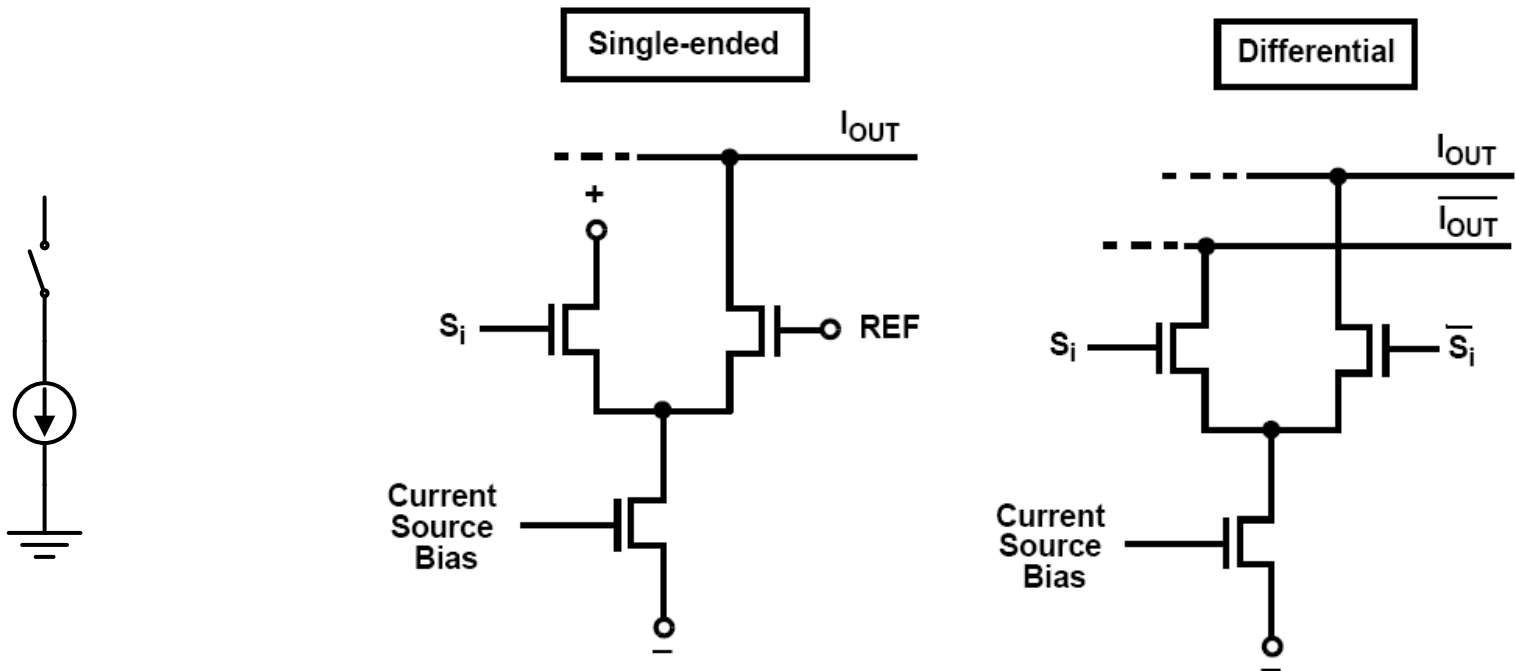


Realization?

Current DAC (“M-DAC”)



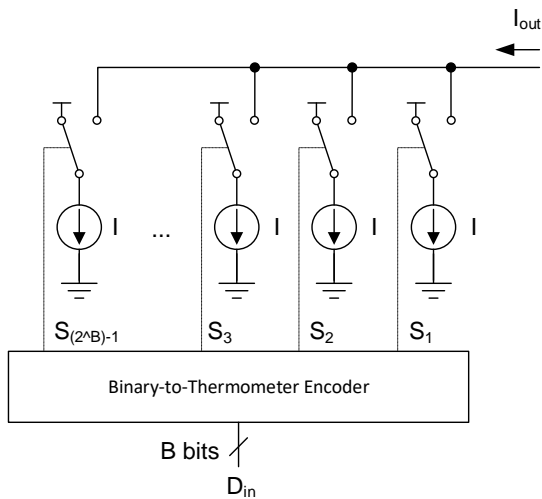
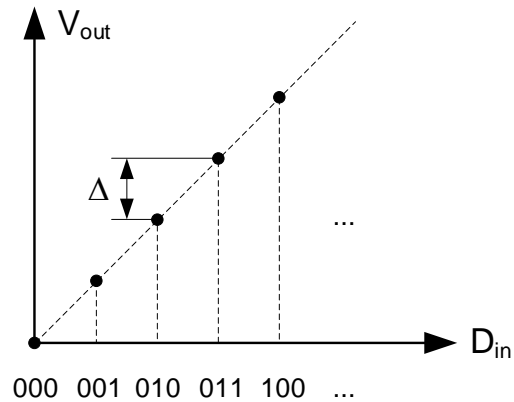
Circuit Realization



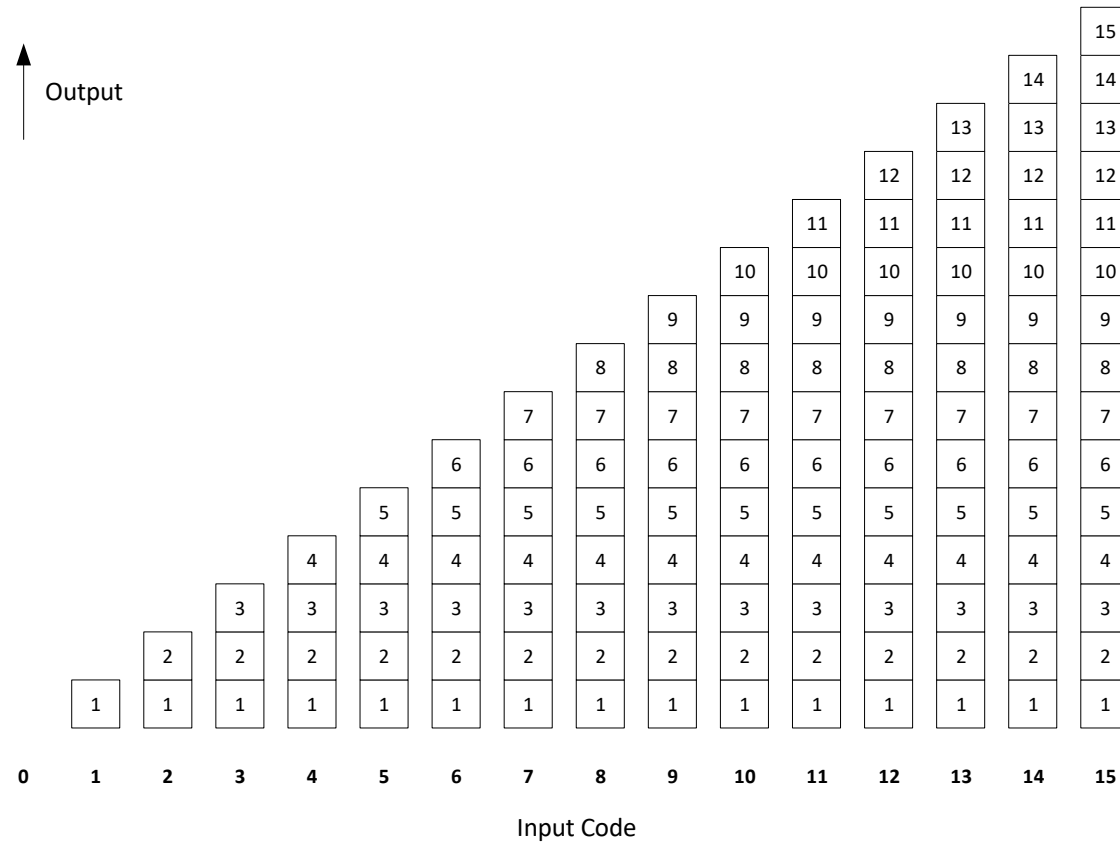
Other DAC implementations:

- Resistor string DAC
- Charge redistribution DAC

How Many Current Sources?



Thermometer DAC Operation



[Boris Murmann]

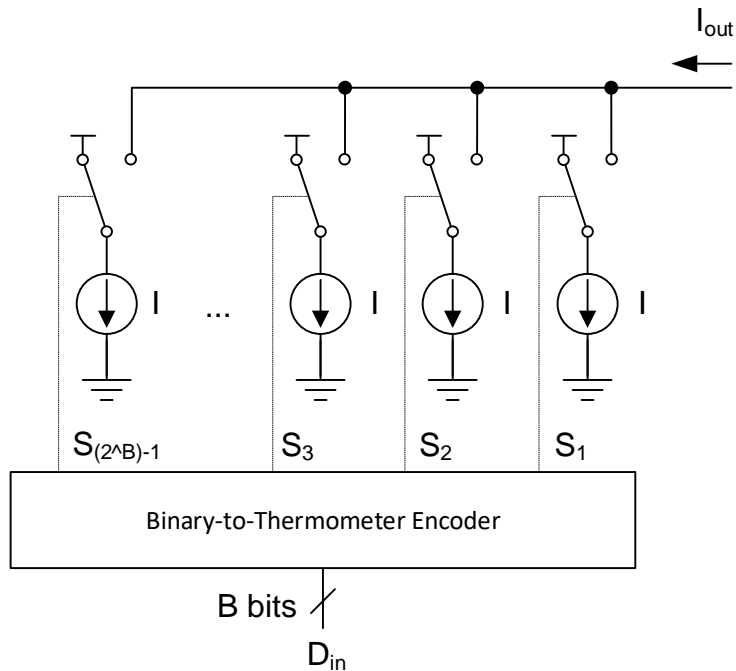
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Digital-to-Analog Converter

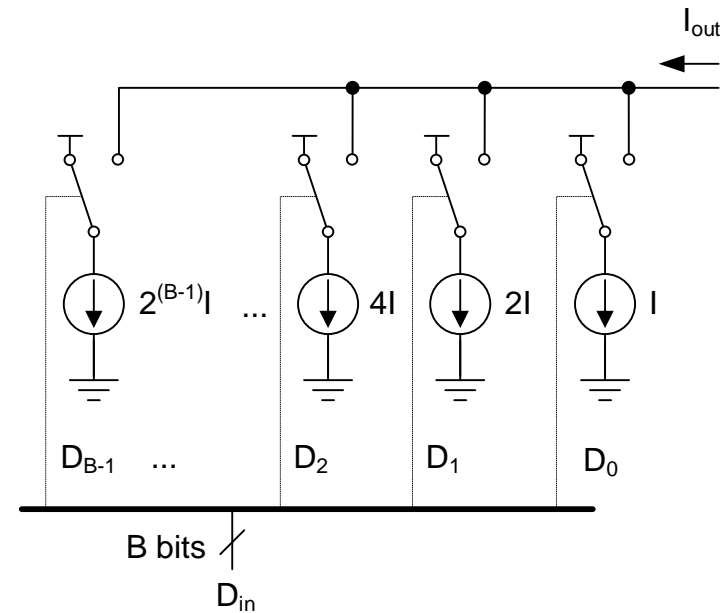
Current DAC (“M-DAC”)

Unit Element



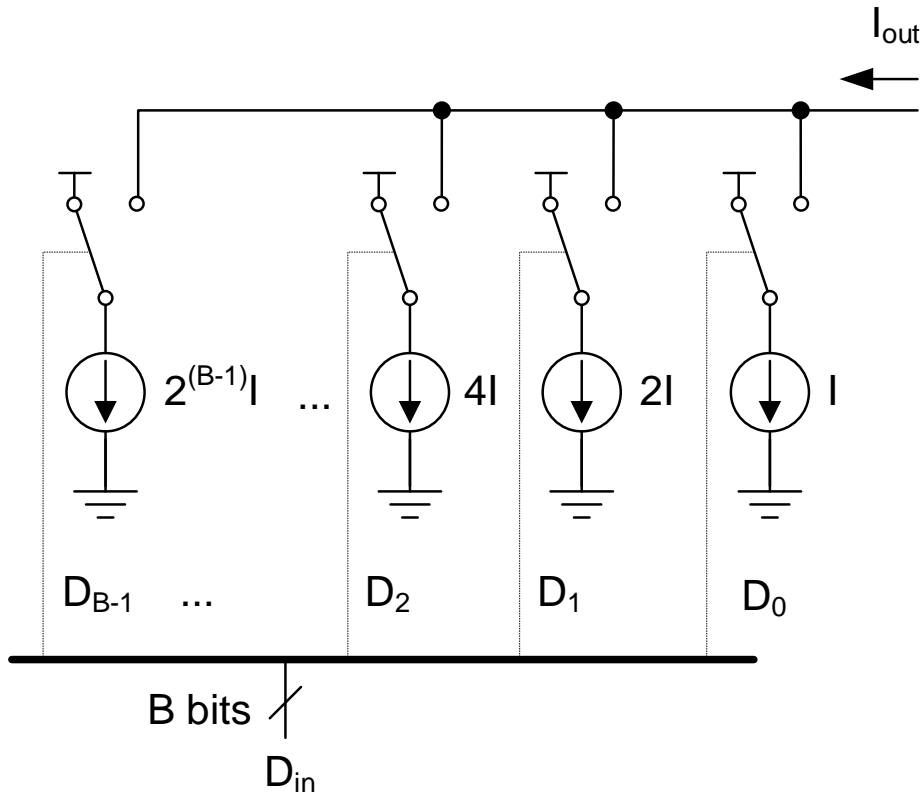
2^B-1 switches

Binary Weighted



B switches

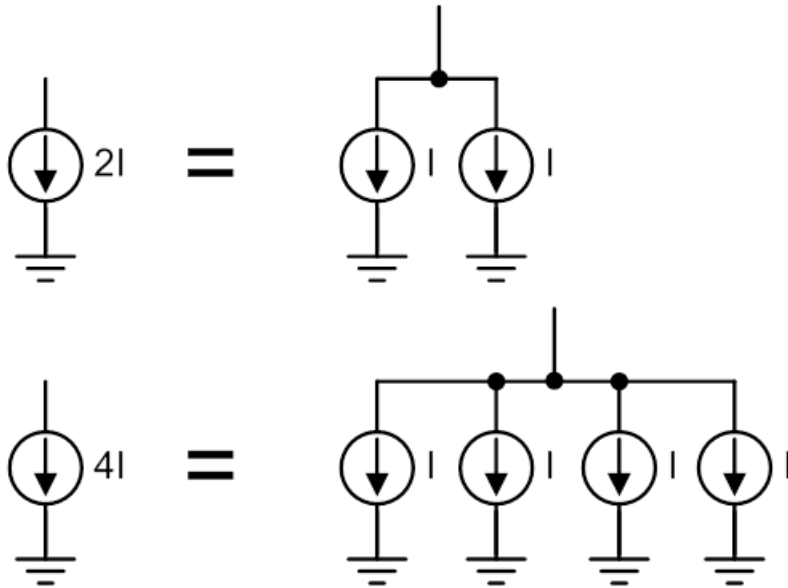
Binary Weighted DAC



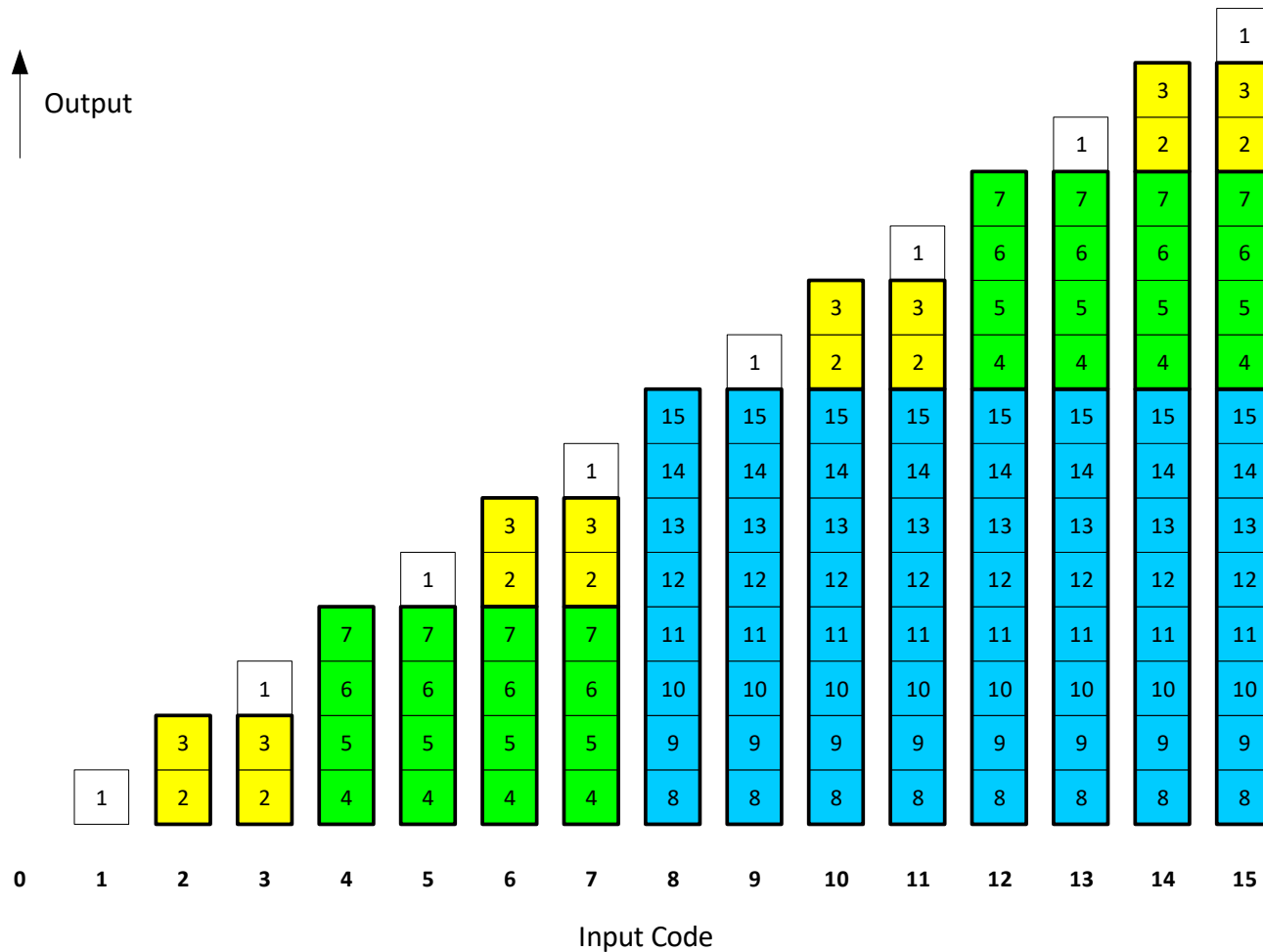
- No encoder needed
- B switches
- How many current sources?

Implementation of Weighted Sources

Transistor-level design:



Weighted DAC Operation



[Boris Murmann]

DAC Comparison

Thermometer

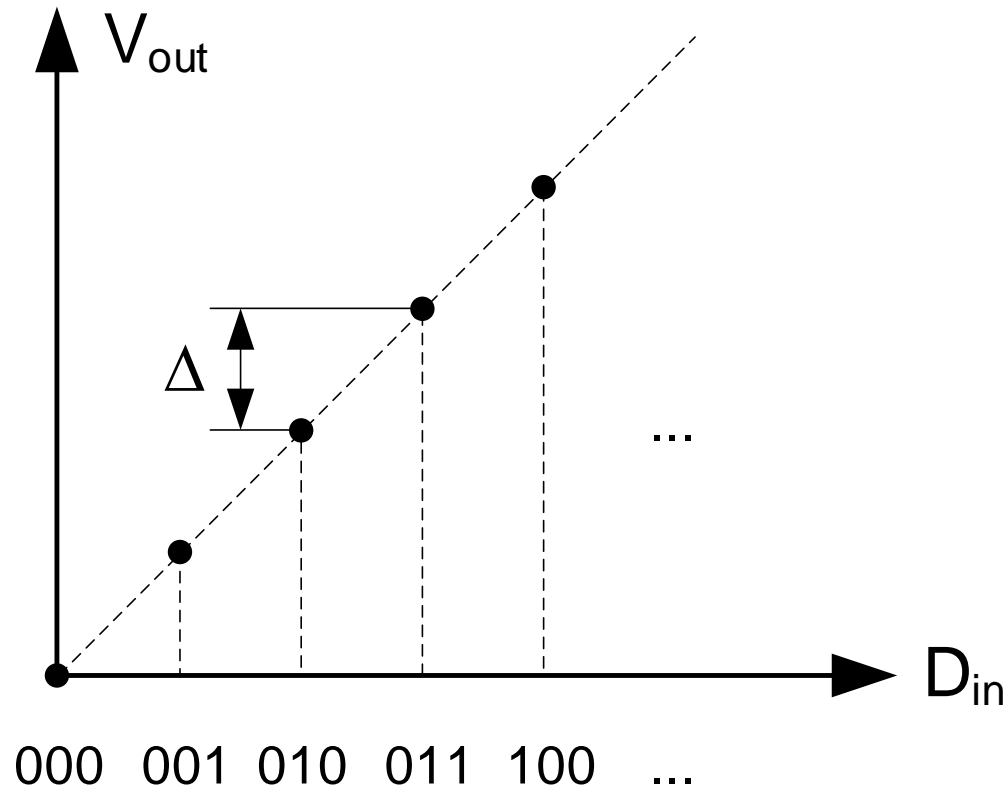
- $2^B - 1$ switches
- Encoder

Binary Weighted

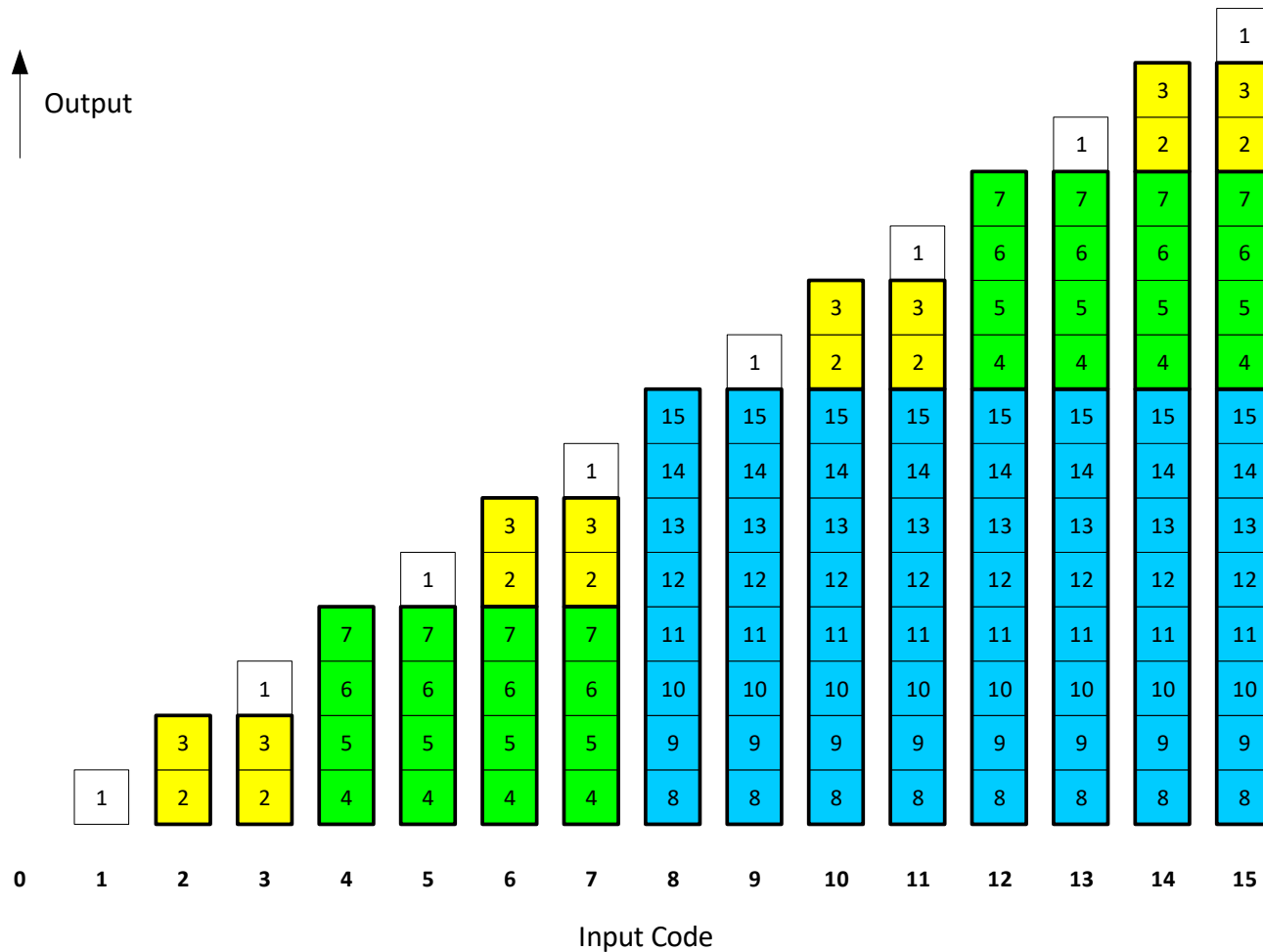
- B switches
- No encoder

Which one is “better”?

Monotonicity



Non-Monotonic Weighted DAC



[Boris Murmann]

Questions

- What is causing imperfections such as non-monotonicity?
- What metrics can we use to quantify the errors?

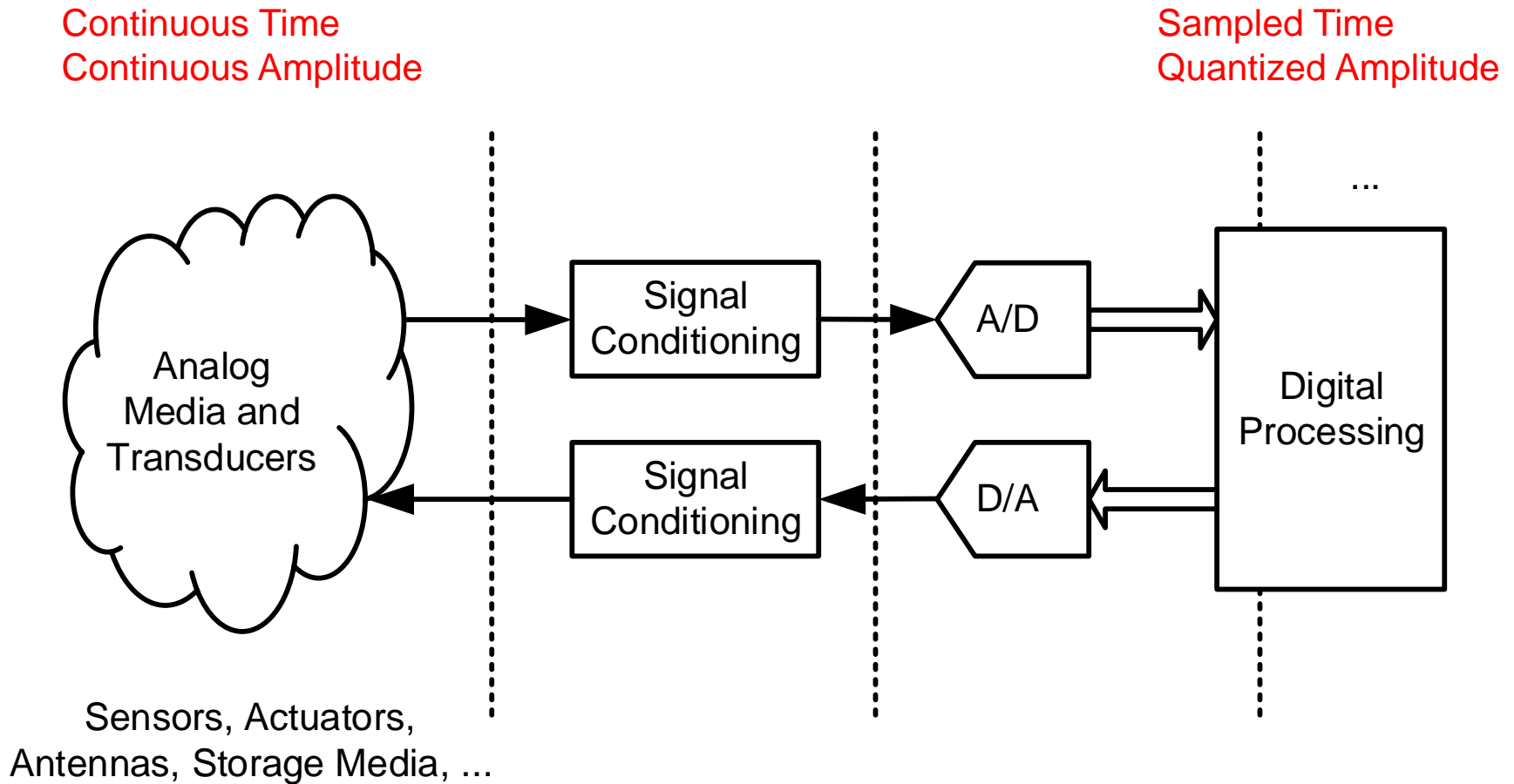
- Let's look at these questions in detail.
- This will take several lectures!

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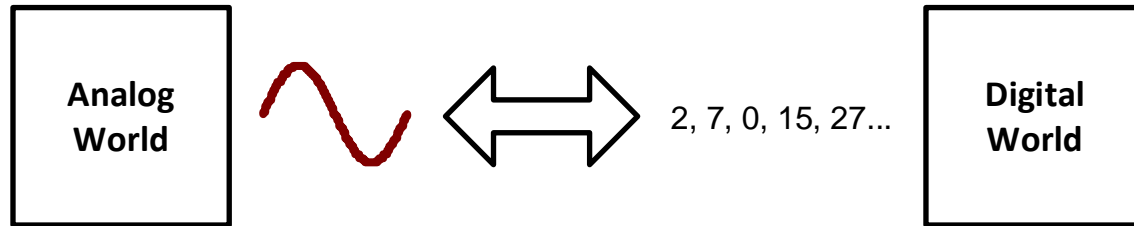
Analog-Digital Interface Integrated Circuits

Sampling and Quantization

Mixed Signal System

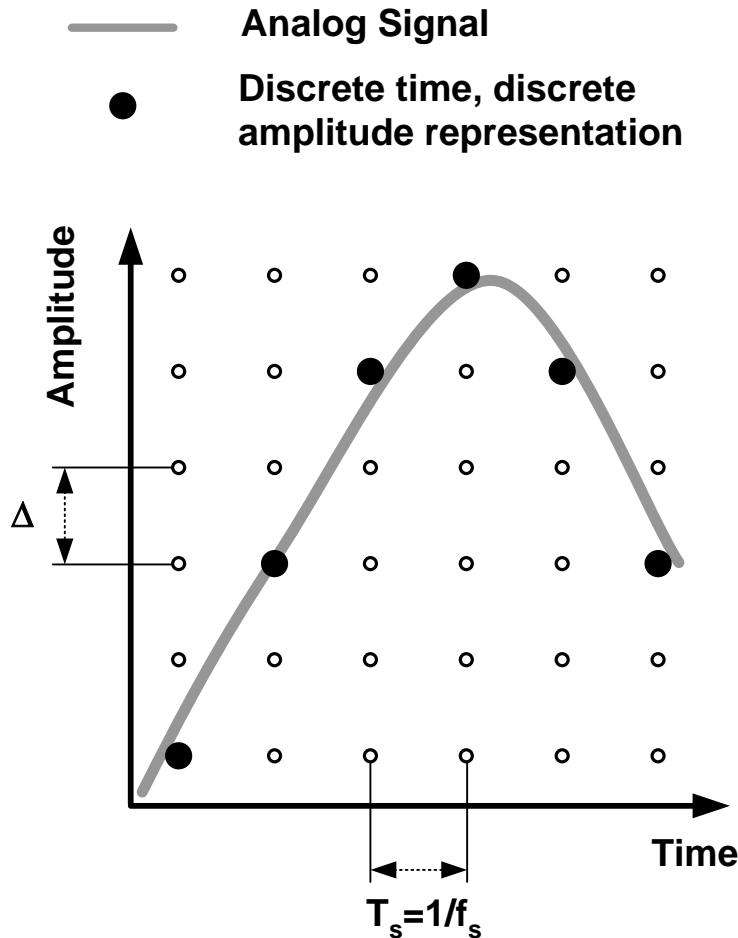


Quantized Signals



- Real world signals
 - Continuous time, continuous amplitude
- Digital abstraction
 - Discrete time, discrete amplitude
- Two problems – how to discretize / "undescretize"
 - in time (sampling / reconstruction)
 - in amplitude (quantization / ...)
- Often performed in conjunction
 - A/D conversion: discretize in time and amplitude
 - D/A conversion: "undescretize" in time and amplitude
 - Other valid combinations, especially discrete time & continuous amplitude
 - Examples?

Uniform Sampling and Quantization



Most common way of performing A/D conversion

- Sample signal uniformly in time
- Quantize signal uniformly in amplitude

Questions

- How fast do we need to sample ?
- How fine do we need to quantize ?

Questions

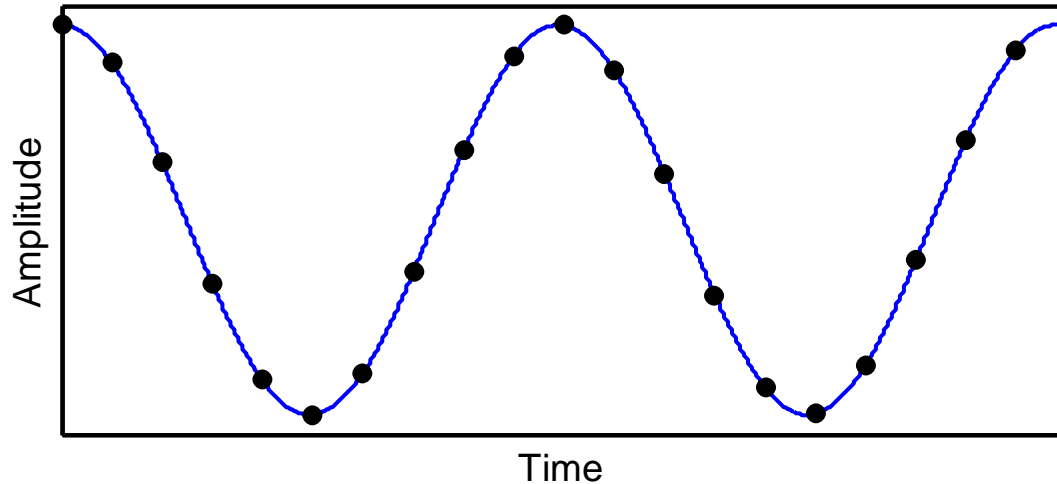
1. How fast do we need to sample an audio signal?
2. What is the criterion?
3. How about an RF signal modulated at a 1GHz carrier frequency with 1MHz bandwidth?
4. How do we prevent “other RF channels” from corrupting the signal?
5. How do we determine the “number of bits” of an A/D converter?
6. How do errors in the quantizer thresholds affect signal quality?
7. Is there a formal procedure for answering these and similar questions?
8. Your question?

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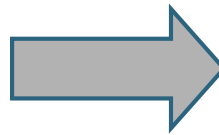
Sampling

Sampling Case (1)



$$f_s = \frac{1}{T_s} = 1000 \text{ kHz}$$
$$f_{sig} = 101 \text{ kHz}$$

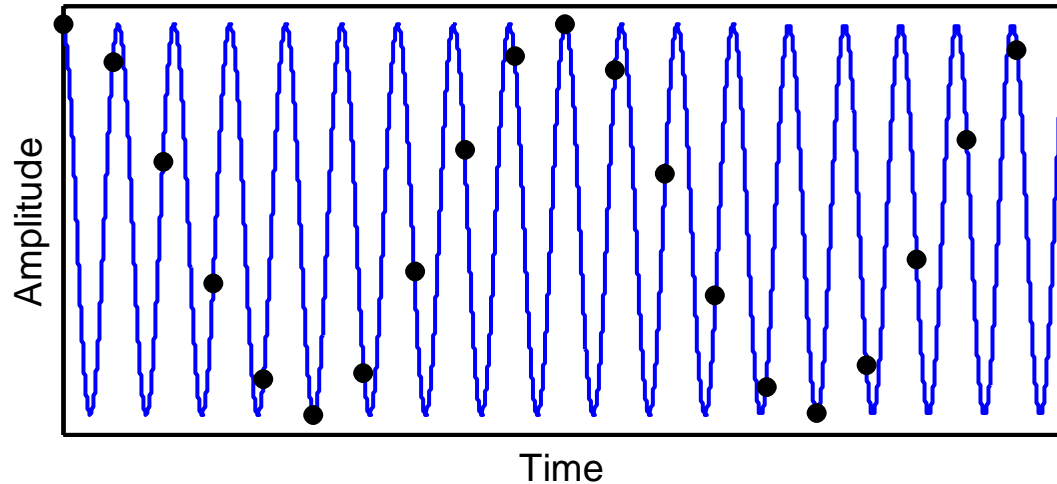
$$v_{sig}(t) = \cos(2\pi \cdot f_{in} \cdot t)$$



$$t \rightarrow n \cdot T_s = \frac{n}{f_s}$$

$$v_{sig}(n) = \cos\left(2\pi \cdot \frac{f_{in}}{f_s} \cdot n\right)$$
$$= \cos\left(2\pi \cdot \frac{101}{1000} \cdot n\right)$$

Sampling Case (2)

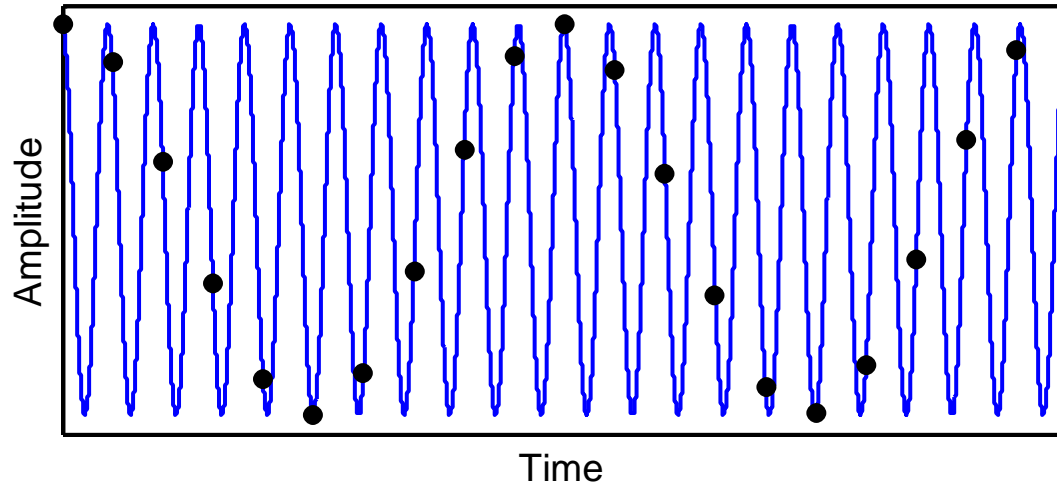


$$f_s = \frac{1}{T_s} = 1000 \text{ kHz}$$
$$f_{sig} = 899 \text{ kHz}$$

$$v_{sig}(n) = \cos\left(2\pi \cdot \frac{899}{1000} \cdot n\right) = \cos\left(2\pi \cdot \left[\frac{899}{1000} - 1\right] \cdot n\right) = \cos\left(2\pi \cdot \frac{101}{1000} \cdot n\right)$$

Sampled signal indistinguishable from Case 1 (101 kHz)

Sampling Case (3)

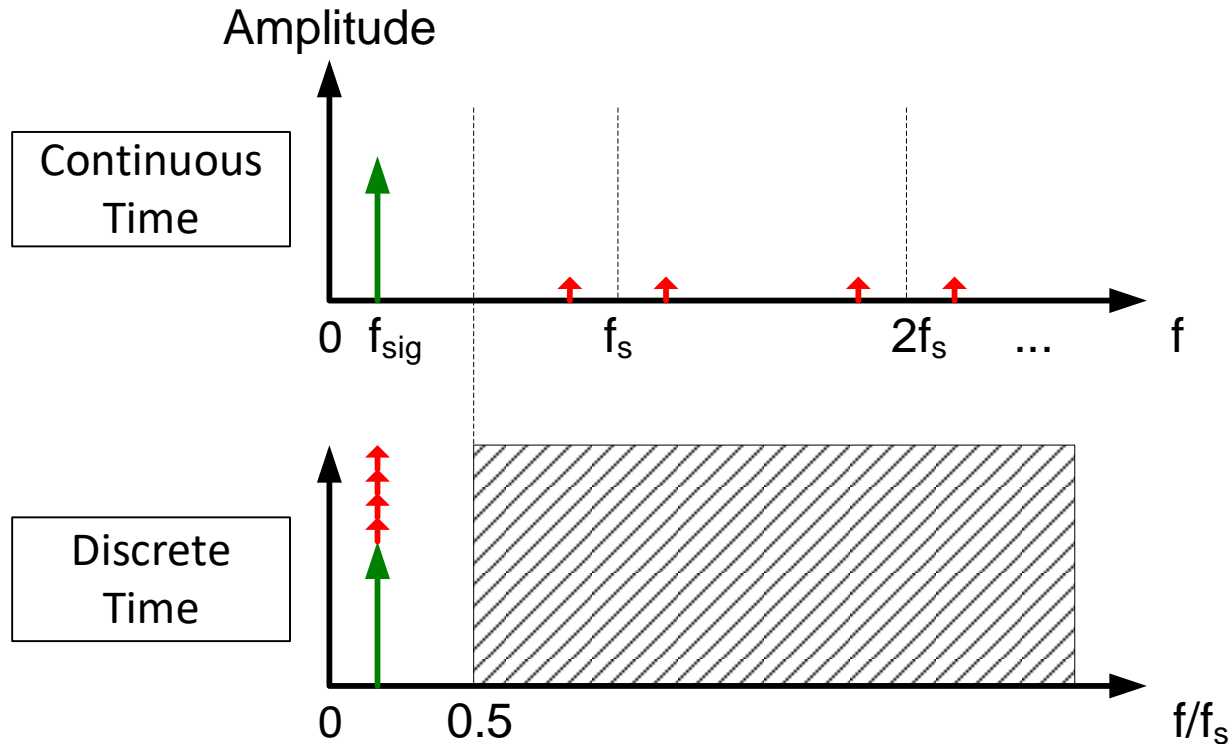


$$f_s = \frac{1}{T_s} = 1000 \text{ kHz}$$
$$f_{sig} = 1101 \text{ kHz}$$

$$v_{sig}(n) = \cos\left(2\pi \cdot \frac{1101}{1000} \cdot n\right) = \cos\left(2\pi \cdot \left[\frac{1101}{1000} - 1\right] \cdot n\right) = \cos\left(2\pi \cdot \frac{101}{1000} \cdot n\right)$$

Sinusoids with frequencies 101, 899, 1101 kHz etc
sampled at 1000 kHz are indistinguishable

Spectrum



- The frequencies f_{sig} and $N \cdot f_s \pm f_{\text{sig}}$ (N integer), are indistinguishable in the discrete time domain

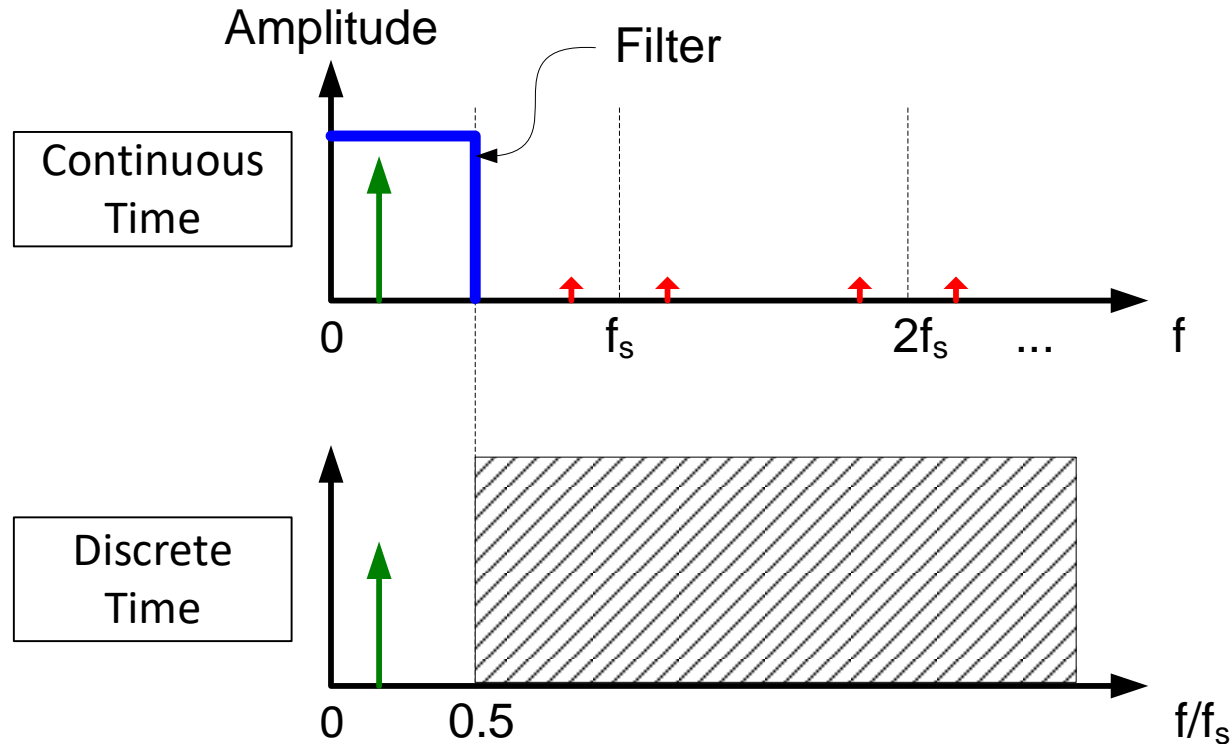
Sampling Theorem

- In order to prevent aliasing, we need

$$B_{sig} < \frac{f_s}{2}$$

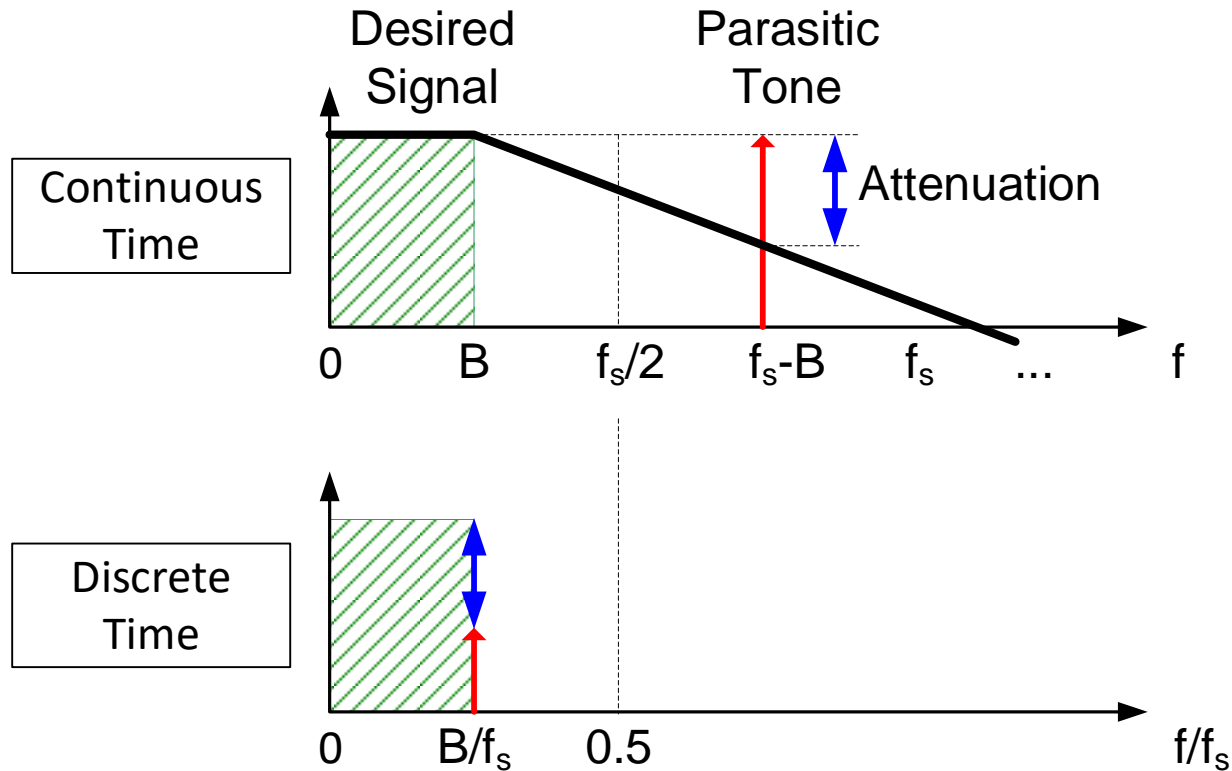
- B_{sig} is the signal bandwidth
 - For “baseband signals”, B_{sig} equals the “highest” signal frequency $f_{sig,max}$
- The sampling rate $f_s = 2 \cdot B_{sig}$ is called the Nyquist rate
- Two options:
 - Sample fast enough to cover all spectral components, including “parasitic” ones outside band of interest
 - Limit B_{sig} through filtering

Brick Wall Anti-Alias Filter



Most ideal contraptions cannot be realized in practice. Brick-Wall filters are no exception ...

Practical Anti-Alias Filter



- Need to sample faster than Nyquist rate to get good attenuation
 - "Oversampling"

How much Oversampling?



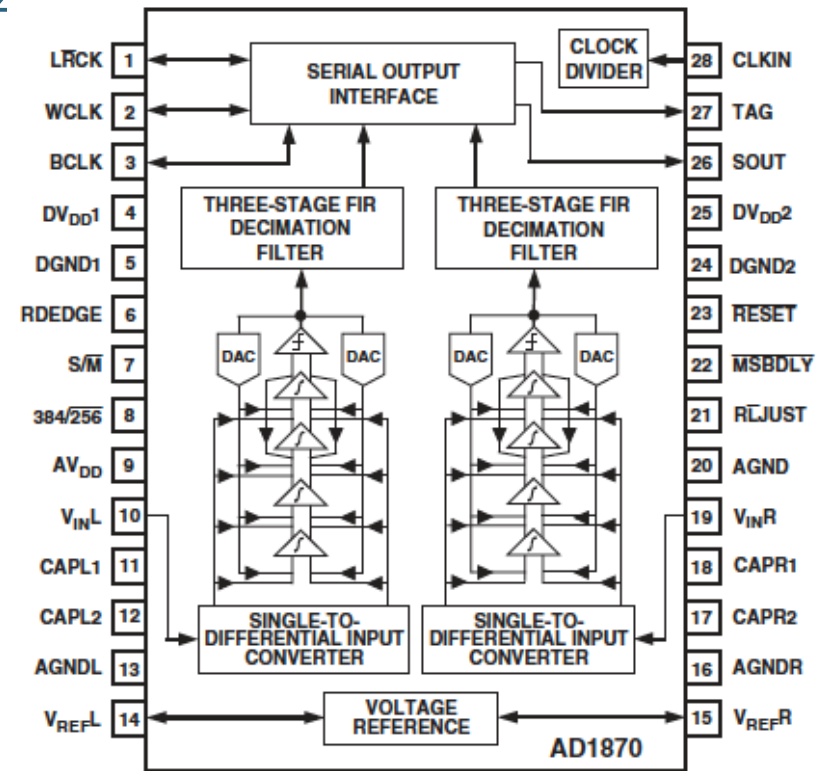
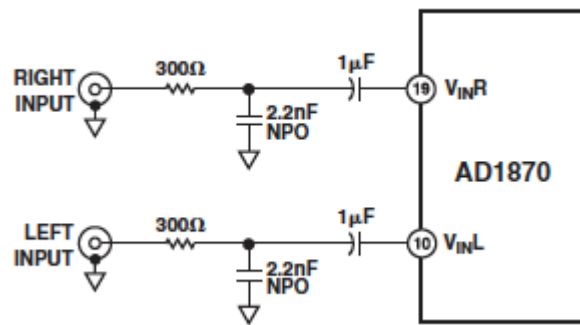
- Tradeoff sampling rate versus filter order
- In high speed converters, $f_s/f_{\text{sig,max}} > 10$ is usually impossible or too costly → need fairly high order filters
- Question: how much alias rejection is required? Give an example!

Types of Sampling

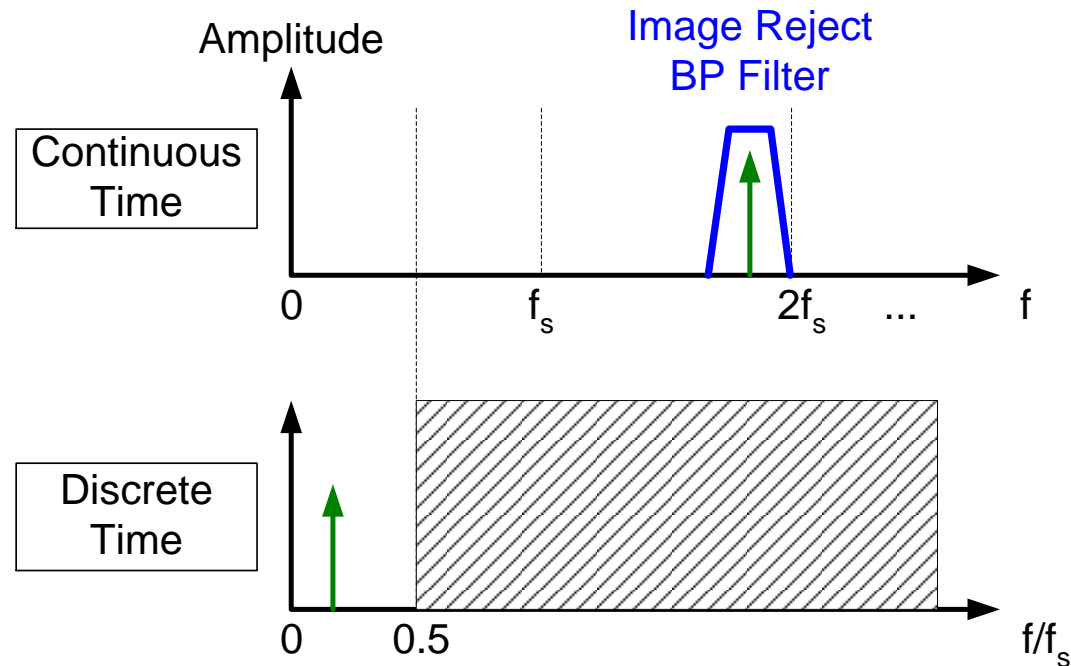
1. Nyquist-rate sampling ($f_s > 2 \cdot f_{\text{sig,max}}$)
 - Nyquist data converters
 - In practice always slightly oversampled
2. Oversampling ($f_s \gg 2 \cdot f_{\text{sig,max}}$)
 - Slowly varying signals (e.g. temperature)
 - Oversampled data converters
 - Anti-alias filtering is often trivial or not needed
 - Explain “trivial”
3. Undersampling, subsampling ($f_s < 2 \cdot f_{\text{sig,max}}$)
 - Exploit aliasing to mix RF/IF signals down to baseband
 - See e.g. Pekau & Haslett, JSSC 11/2005

Oversampling Anti-Aliasing Filter

- CD Audio Signals: $B = 20 \text{ KHz}$ and $f_s = 44.1 \text{ KHz}$
- Example: AD1870 Single-Supply 16-bit $\Sigma\Delta$ Stereo ADC
ADC $f_s = 64 \times 44.1 \text{ KHz} = 2.8 \text{ MHz}$
 - First-order passive analog anti-alias filter with 22dB rejection at 3 MHz
 - Digital filter with 90dB stopband rejection



Subsampling



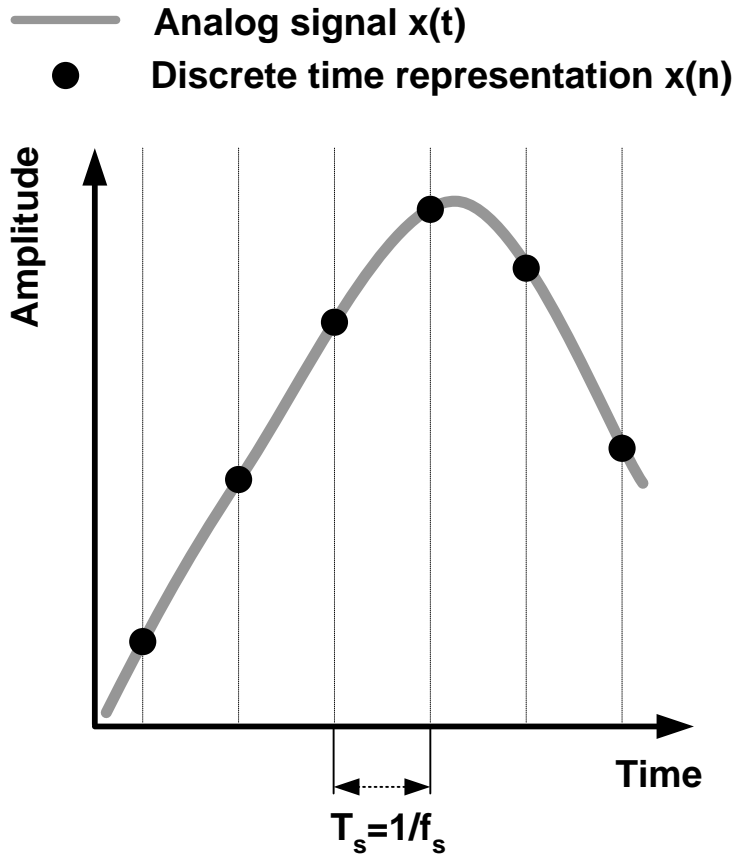
- Aliasing is "non-destructive" if signal is band limited around some carrier frequency
- Downfolding of noise is a severe issue in practical subsampling mixers
 - Typically achieve noise figure no better than 20 dB (!)

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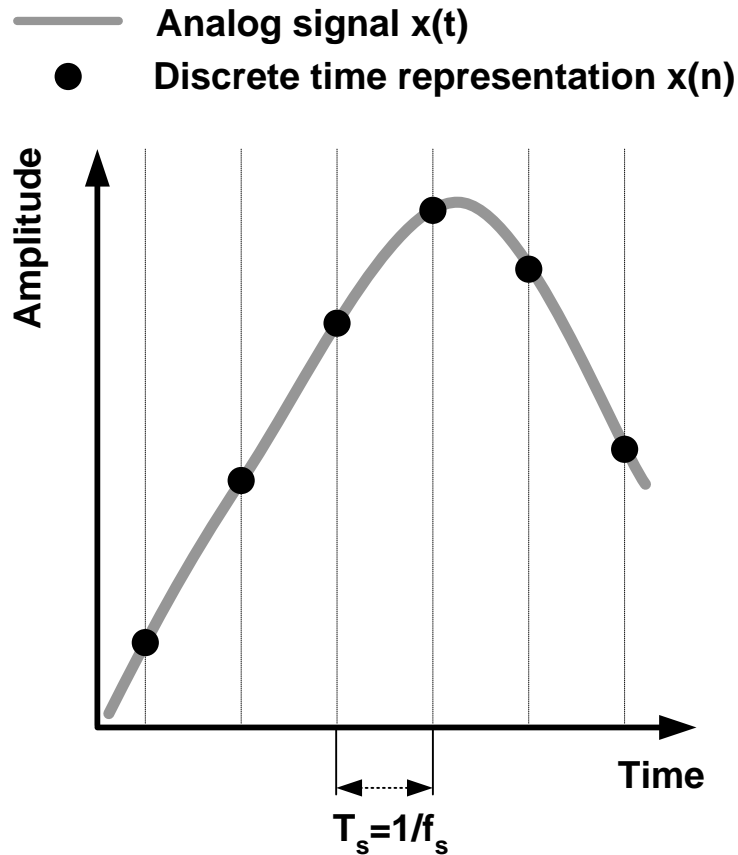
Reconstruction

Reconstruction Problem



- Known: discrete time samples $x(n)$
- Objective: recover $x(t)$
- Sampling theorem: signal spectrum preserved provided that $f_s > 2 \cdot B$
- Should be possible to perfectly recover original analog signal $x(t)$
- How?

Ideal Reconstruction



- Ideal interpolation

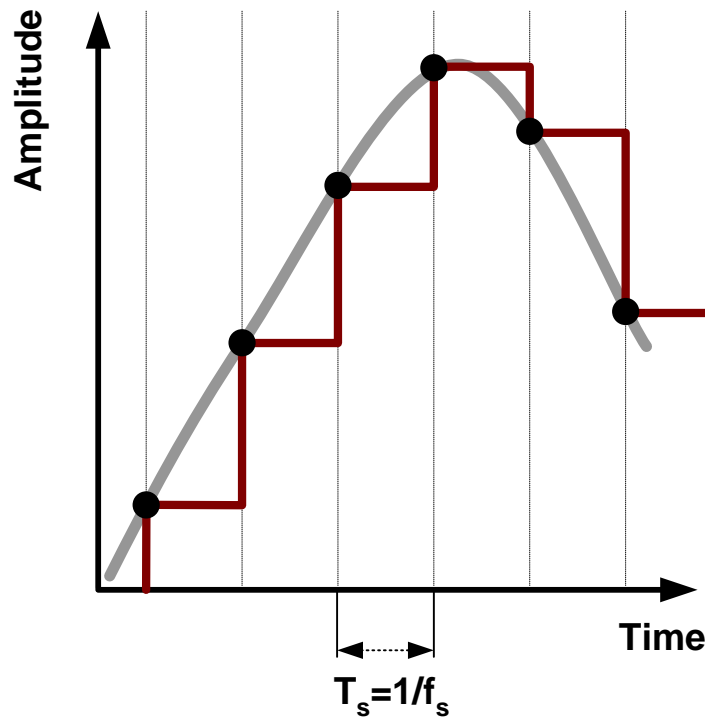
$$x(t) = \sum_{n=-\infty}^{\infty} x(n) \cdot g(t - nT_s)$$

$$g(t) = \frac{\sin(\pi f_s t)}{\pi f_s t}$$

- Not practical
- Question:
 - What happens if each sampling point is replaced with an ideal Dirac impulse?
 - (not very practical, either)

Zero-Order Hold (ZOH) Reconstruction

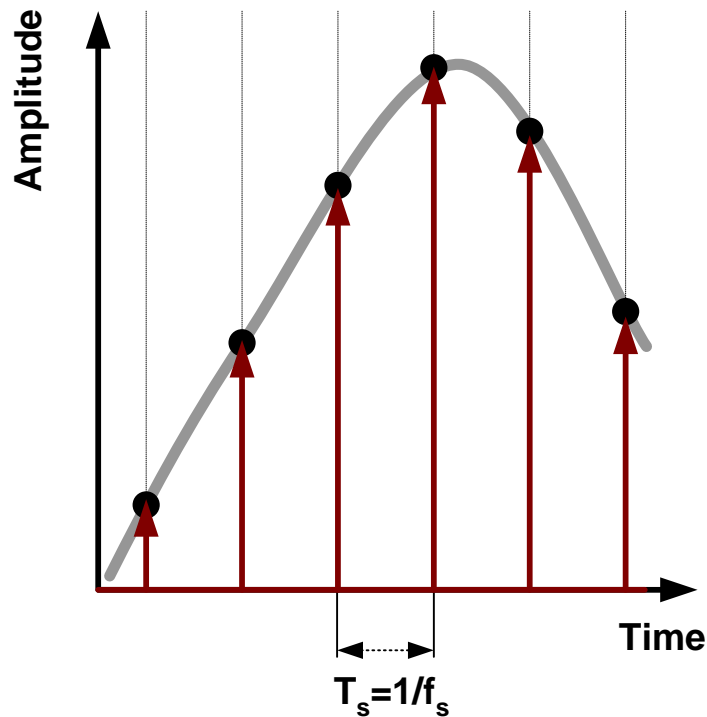
- Analog signal $x(t)$
- Discrete time representation $x(n)$
- Zero order hold approximation



- The most practical way of reconstructing the continuous time signal is to simply "hold" the discrete time values
 - Either for full period T_s or a fraction thereof
 - Other schemes exist, e.g. first- or partial-order hold [Jha, TCAS II, 11/2008]
- What does this do to the signal spectrum?
- Analyze in two steps
 - First look at infinitely narrow reconstruction pulses

Dirac Pulses

- Analog signal $x(t)$
- Discrete time representation $x(n)$
- Dirac pulse signal $x_d(t)$



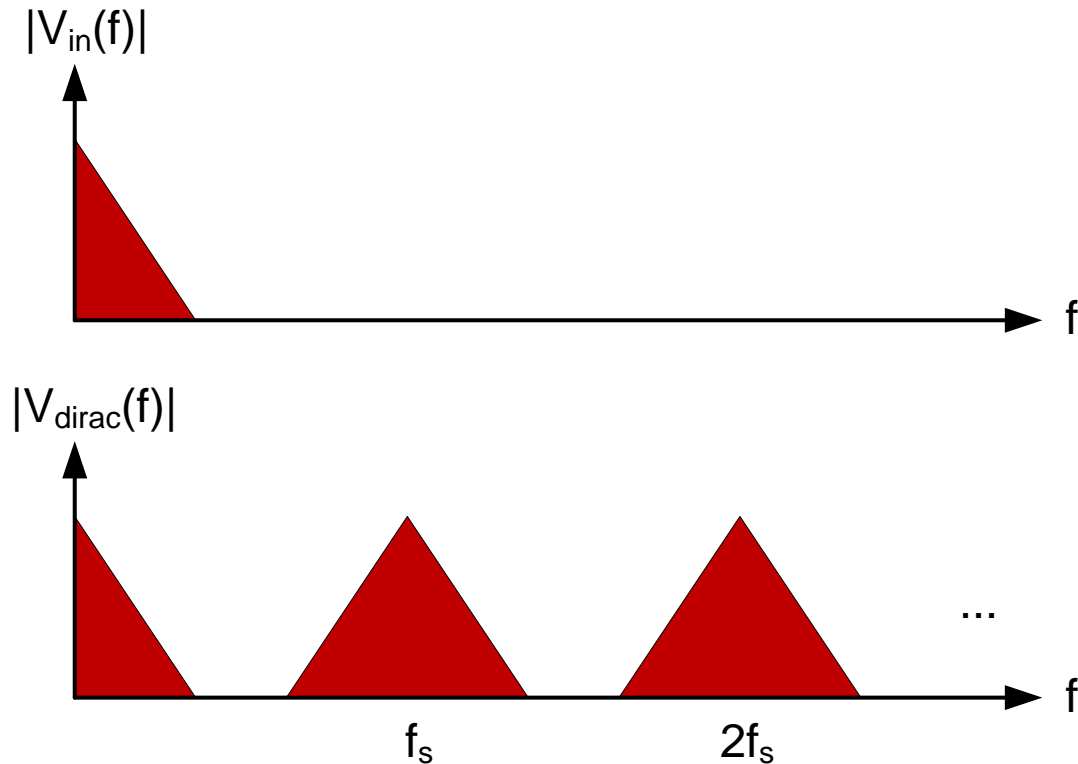
- $x_d(t)$ is zero between pulses
 - Note that $x(n)$ does not exist at these times

$$x_d(t) = x(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT_s)$$

- Multiplication in time means convolution in frequency
 - Resulting spectrum

$$X_d(f) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} X\left(f - \frac{n}{T_s}\right)$$

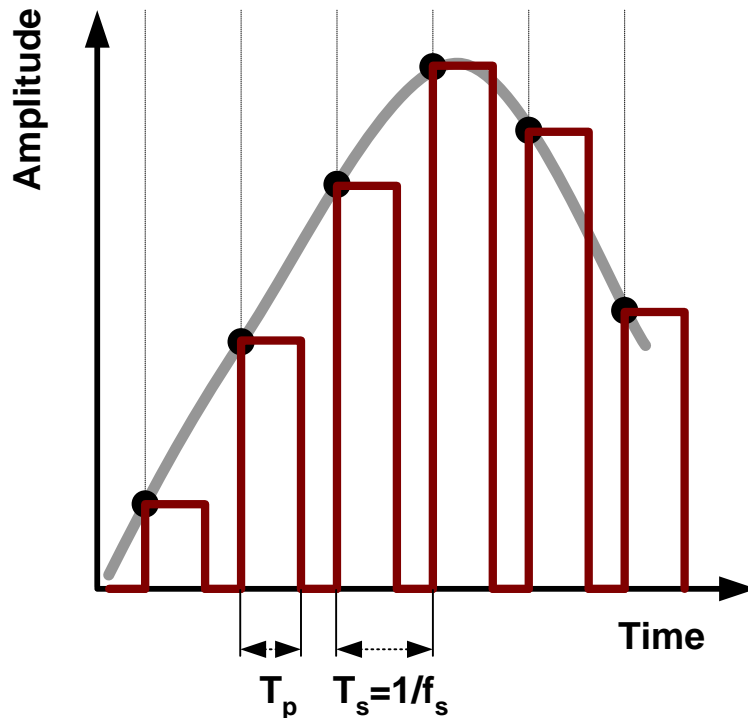
Spectrum for “Dirac Interpolation”



Spectrum of Dirac signal includes replicas of $V_{in}(f)$ at integer multiples of the sampling frequency

Finite Hold Duration

- Analog signal $x(t)$
- Discrete time representation $x(n)$
- Zero order hold approximation



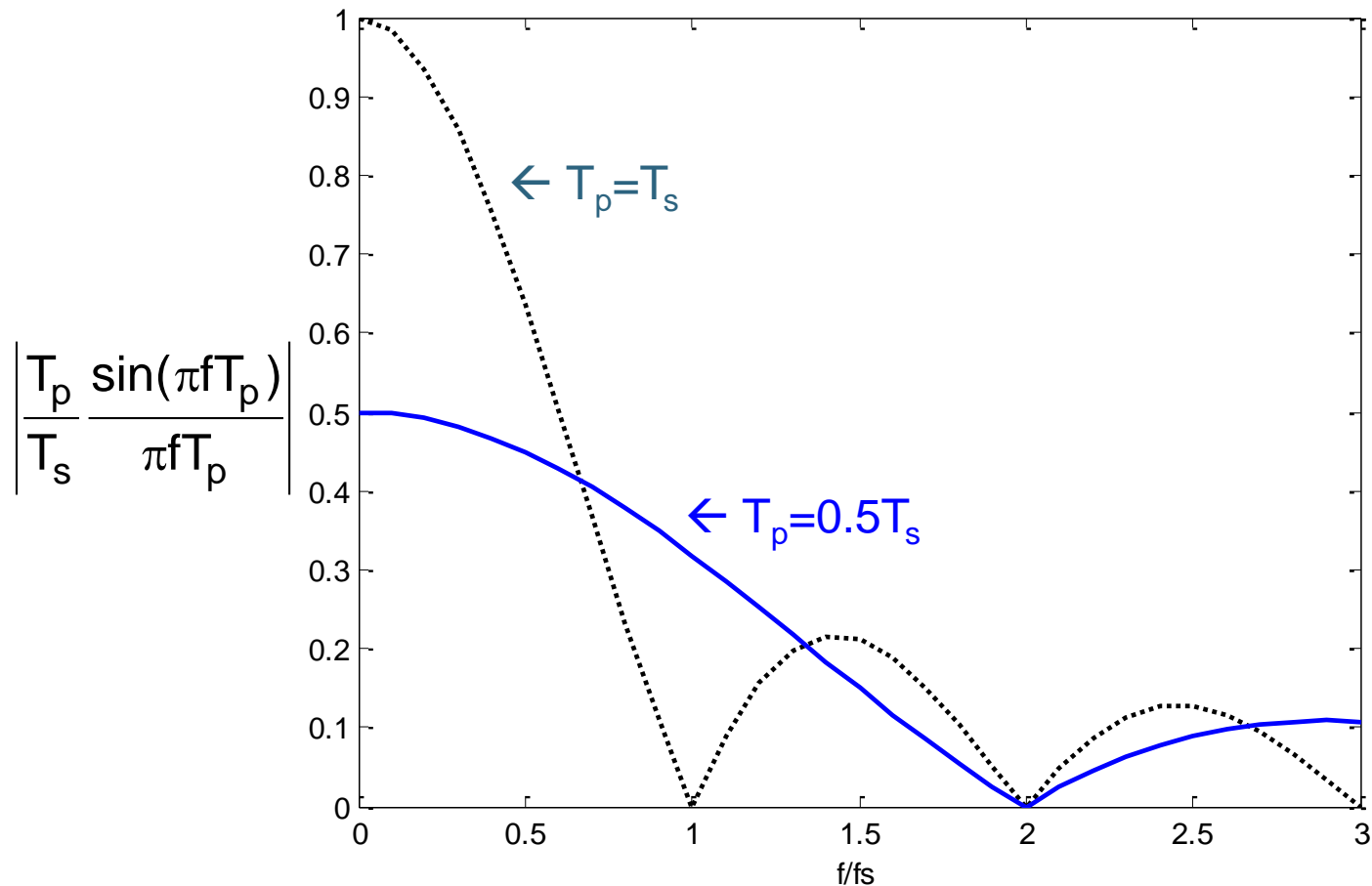
- General case $0 < T_p \leq T_s$
- The time domain signal on the left results from convolving the Dirac sequence with a rectangular unit pulse
- Spectrum: multiplication with Fourier transform of the pulse

$$H_p(s) = \frac{1 - e^{-sT_p}}{s} \quad H_p(f) = T_p \frac{\sin(\pi f T_p)}{\pi f T_p} \cdot e^{-j\pi f T_p}$$

“sinc” filter

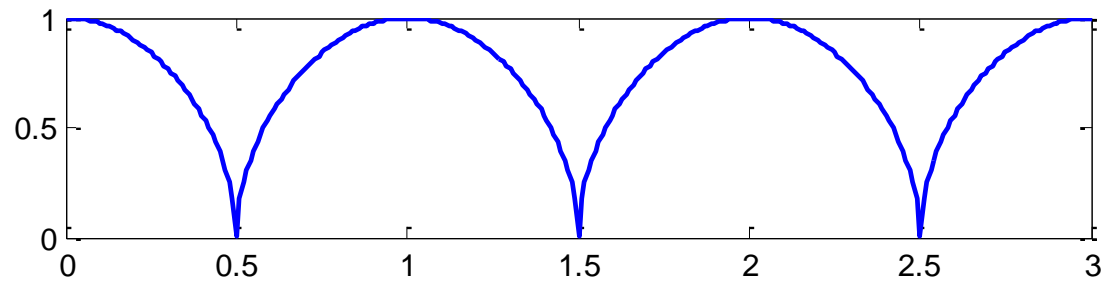
$$X_p(f) = \underbrace{\frac{T_p}{T_s} \frac{\sin(\pi f T_p)}{\pi f T_p}}_{\text{amplitude envelope}} \cdot e^{-j\pi f T_p} \sum_{n=-\infty}^{\infty} X\left(f - \frac{n}{T_s}\right)$$

Spectra for $T_p=T_s$ and $T_p=0.5\cdot T_s$

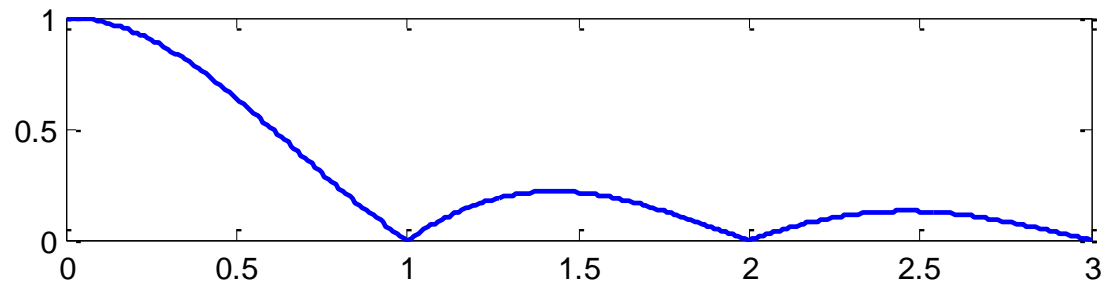


Example

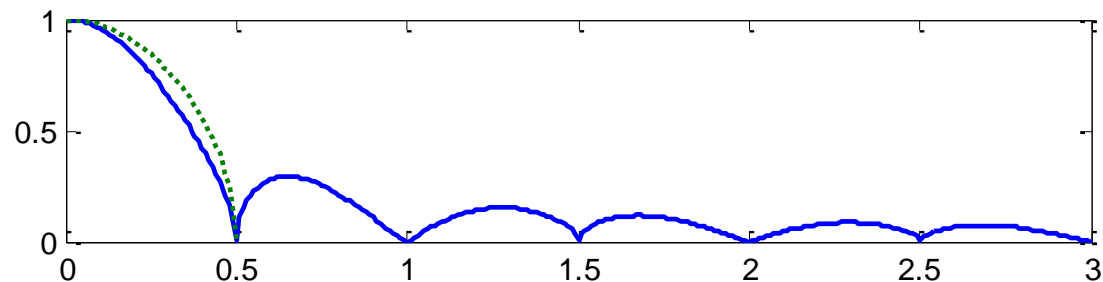
**Spectrum of
Continuous Time
Dirac Pulse Train
(Arbitrary Example)**



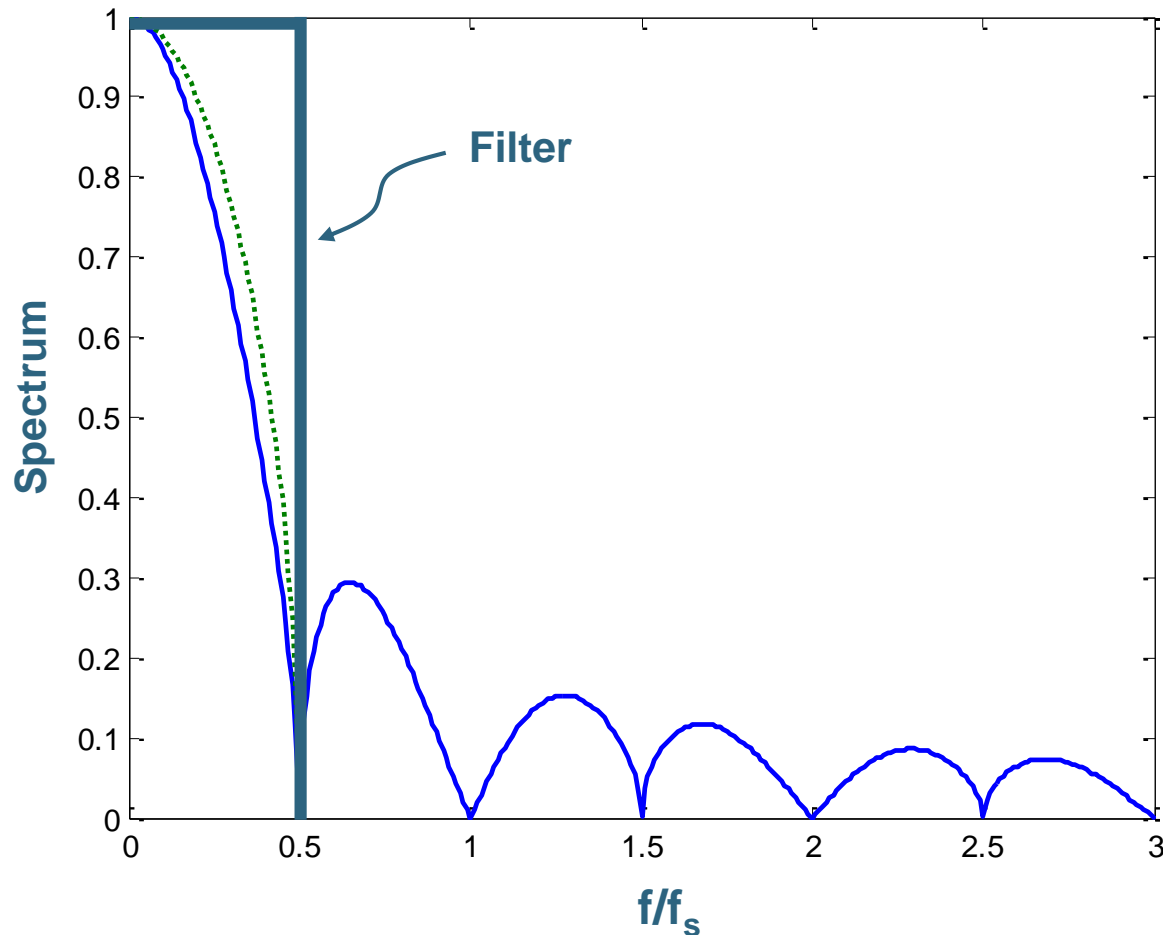
**ZOH Transfer
Function
(sinc “Distortion”)
 $T_p = T_s$**



**ZOH output,
Spectrum of
Staircase
Approximation
(image rejection &
in-band attenuation)**



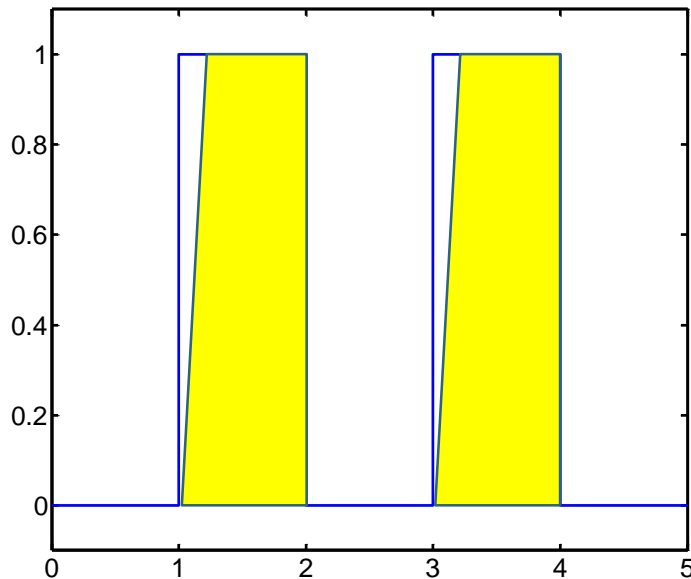
Reconstruction Filter



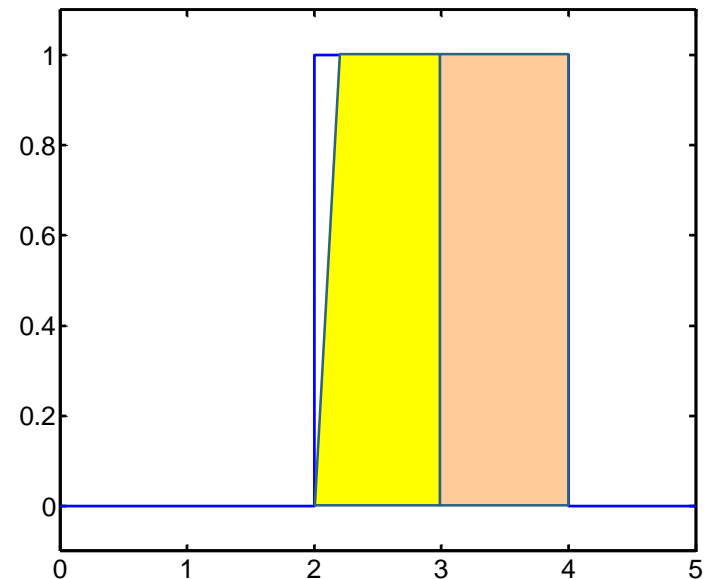
- Also called smoothing filter
 - Same situation as with anti-alias filter
 - A brick wall filter with post-emphasis for sinc attenuation would be ideal ...
 - What is post-emphasis?
 - Oversampling helps reduce filter order.
- How?

NRZ versus RZ DAC

1-Bit Example (non return to zero, NRZ):



Area: $1-\Delta$ $1-\Delta$
Total: $2-2\Delta$



$1-\Delta$ 1
 $2-\Delta$

Areas are different for the two cases. RZ coding avoids this.