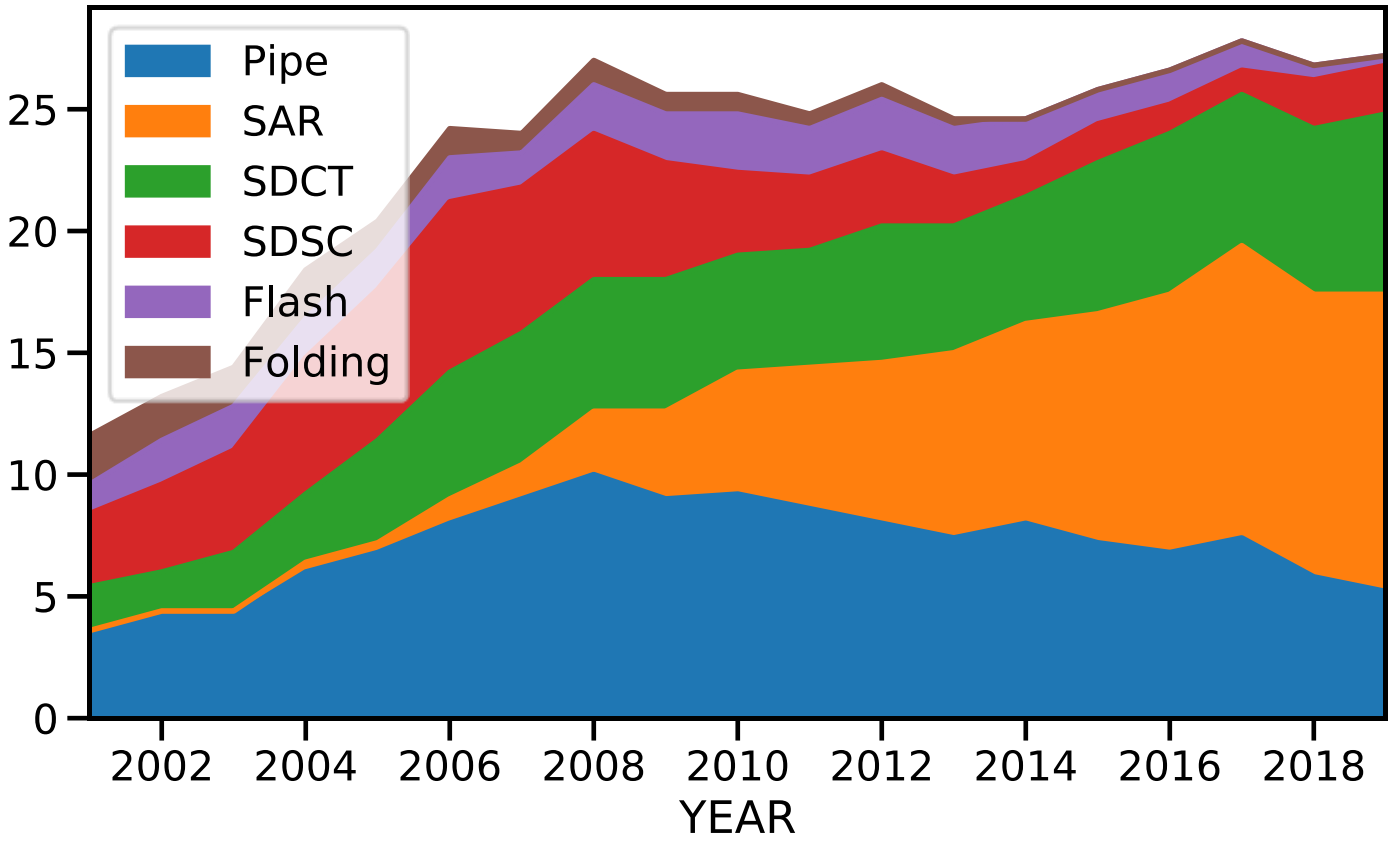
EE 240C
Analog-Digital Interface Integrated Circuits

ADC Architectures

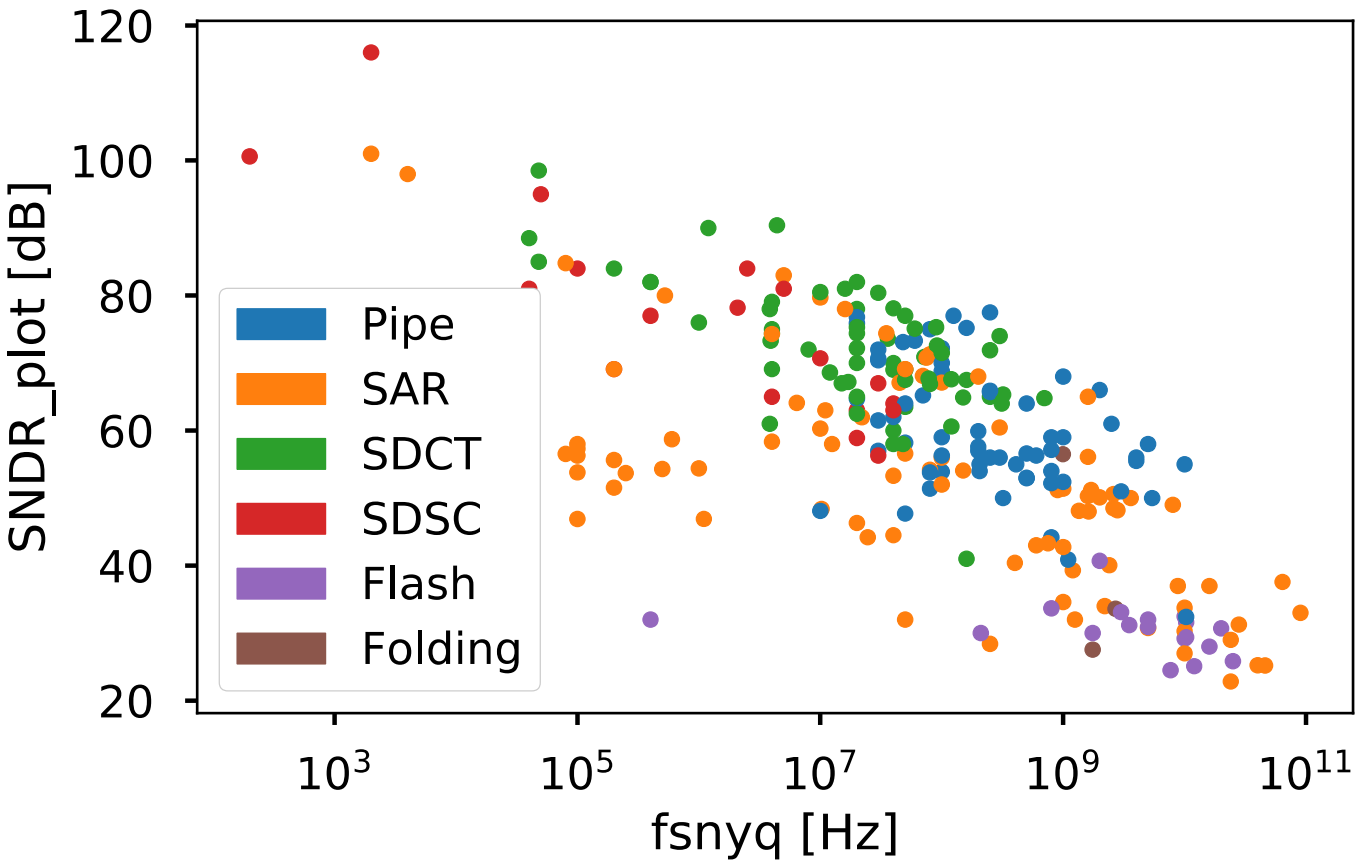
Architectures of Published ADCs (ISSCC and VLSI)



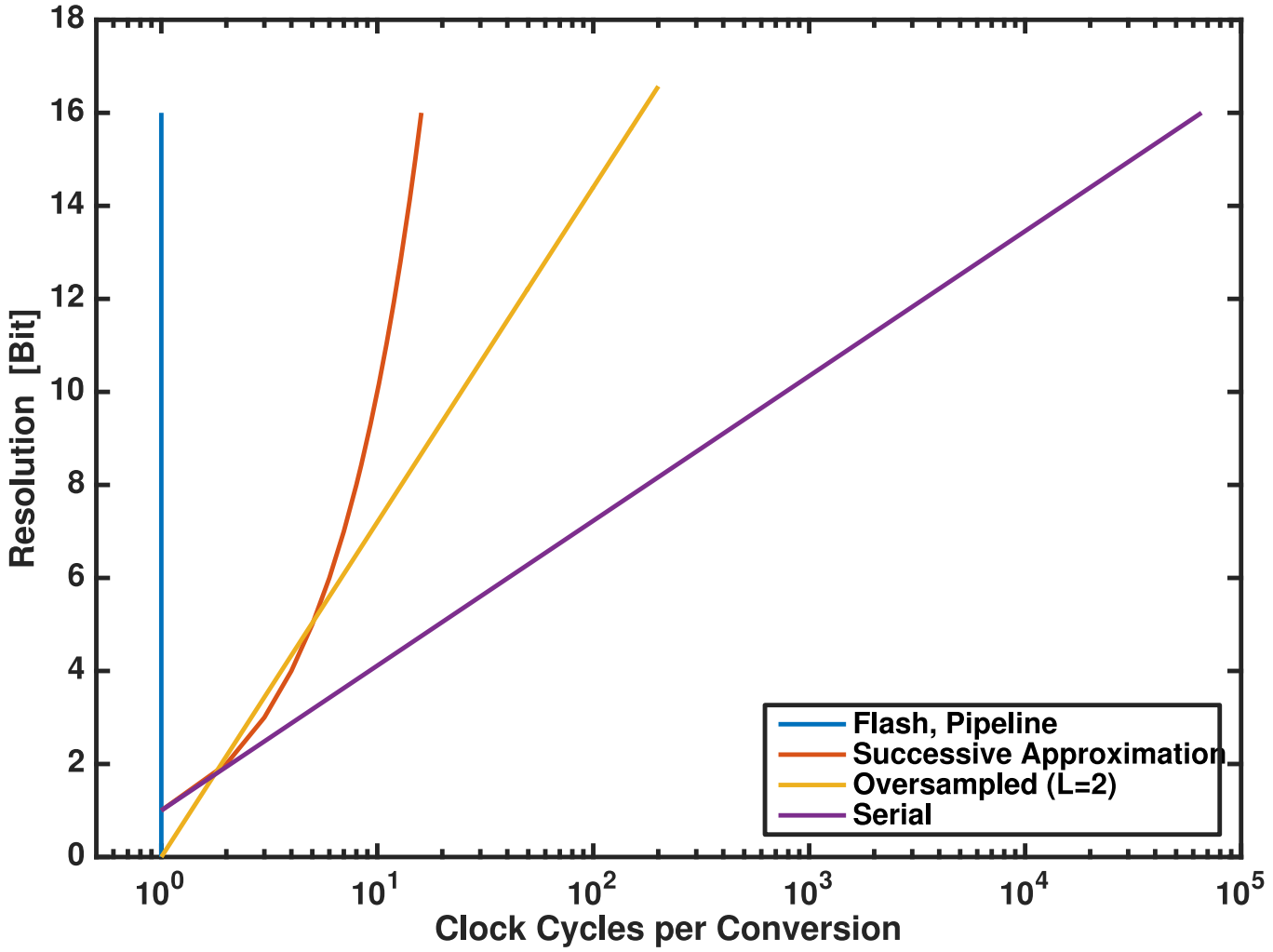
- Evolution due to ADC improvements, technology shift, and focus on low power
- Source data: B. Murmann, "ADC Performance Survey 1997-2019," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html
- TI arch. combined with core arch. (e.g. SAR and TI SAR); other arch, (10-15%) not incl.

ADC Performance Survey (ISSCC & VLSI 2007-2017)

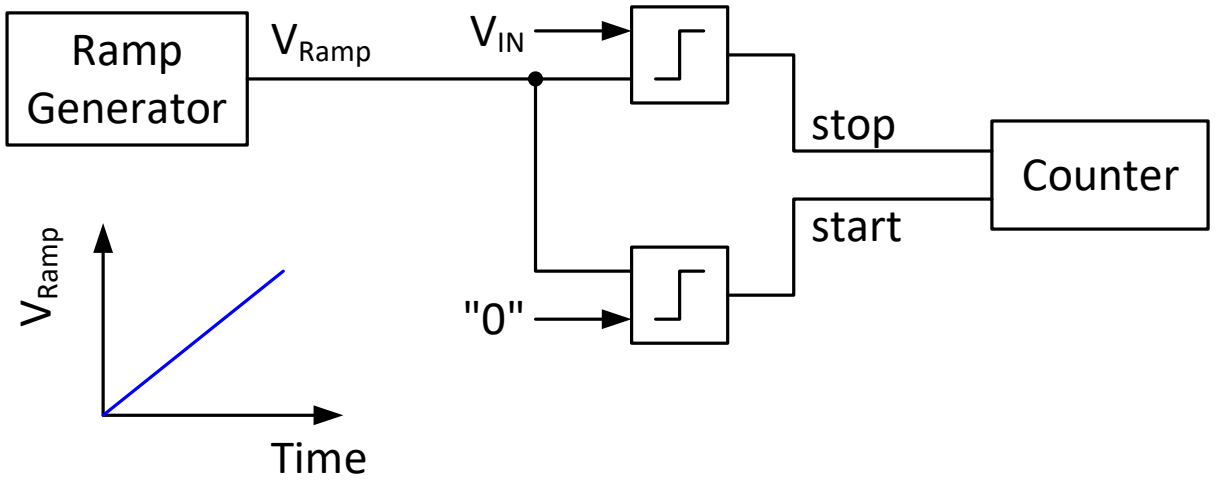
Data: http://www.stanford.edu/~murmann/adcsurvey.html



Speed Comparison

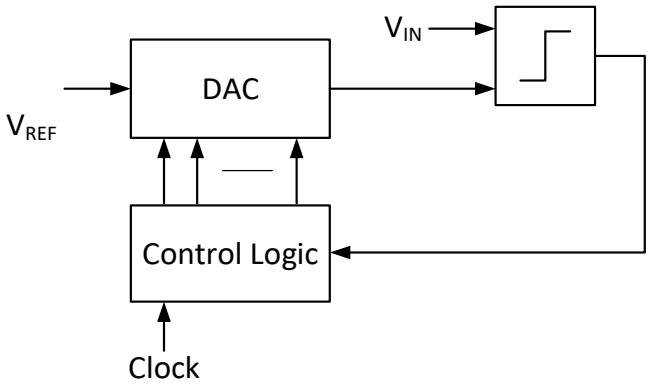


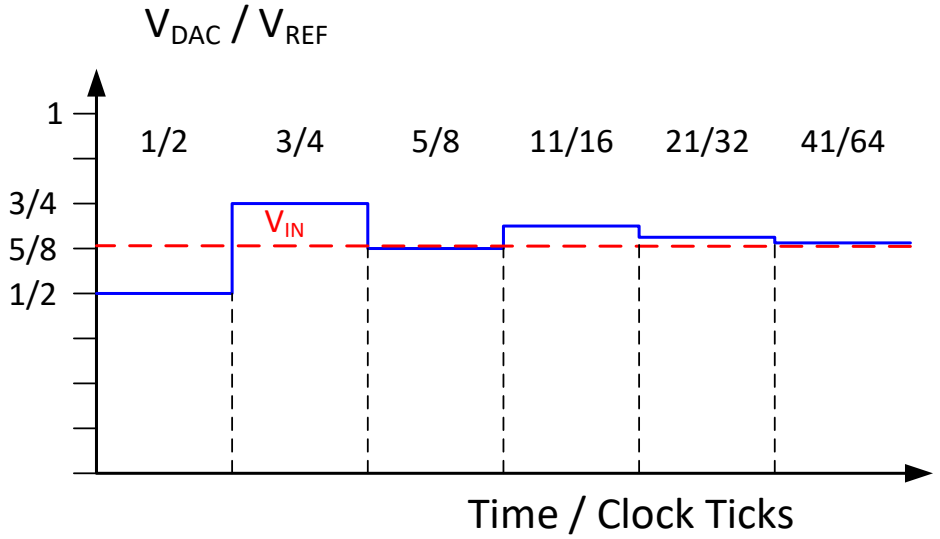
Serial ADC



- Low complexity
- Very high accuracy achievable (digital volt-meter)
- Slow: conversion time proportional 2^B

Successive Approximation

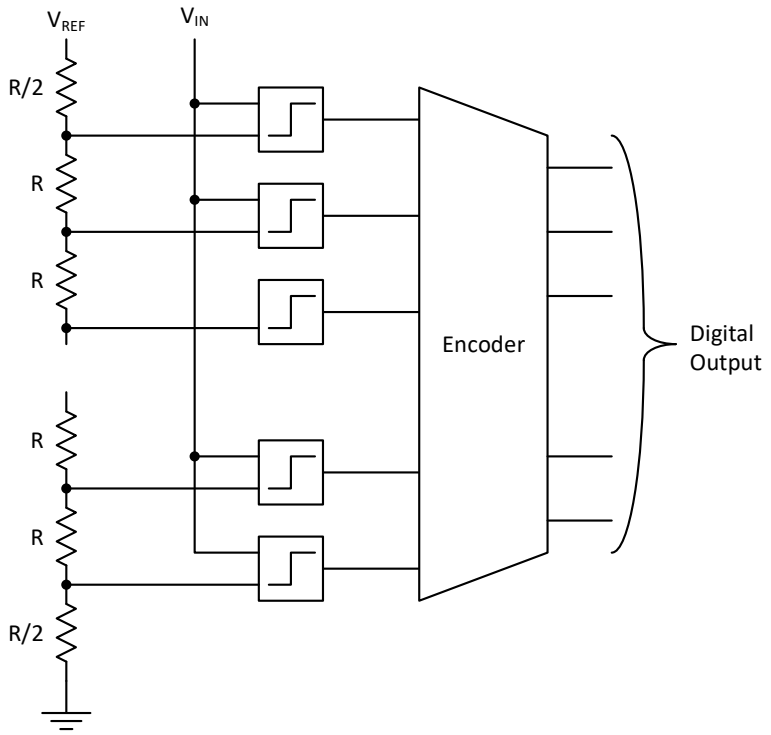




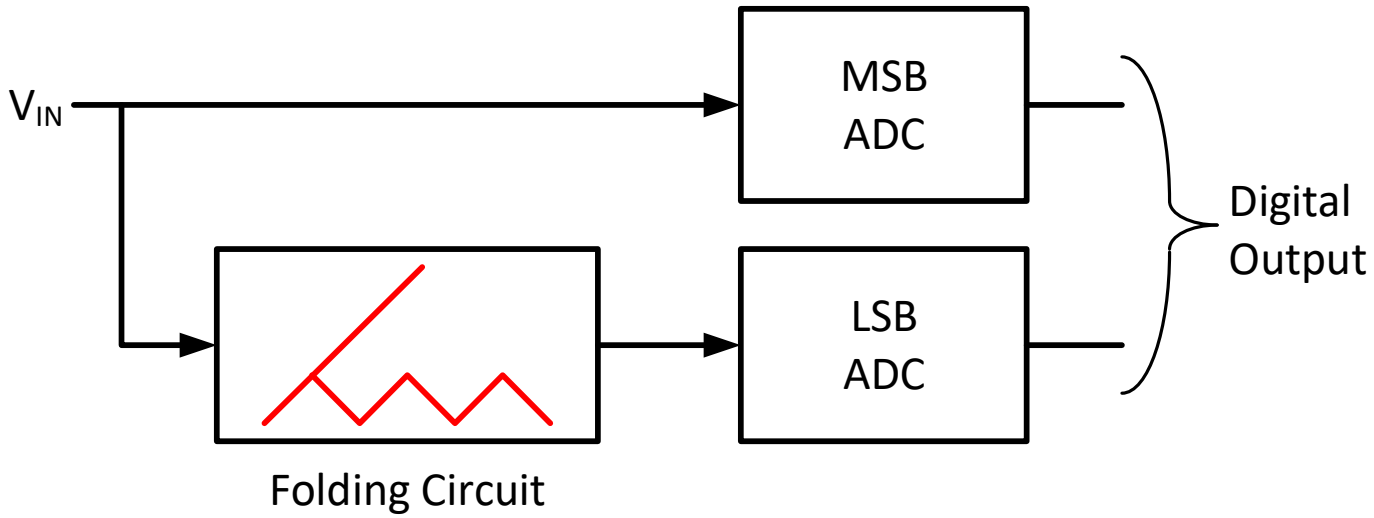
- Binary search over DAC output
- High accuracy achievable (16+ Bits)
- Moderate speed proportional to B (1+ MHz)

Flash Converter

- Very fast: only 1 clock cycle per conversion
- High complexity: 2^B-1 comparators
- High input capacitance



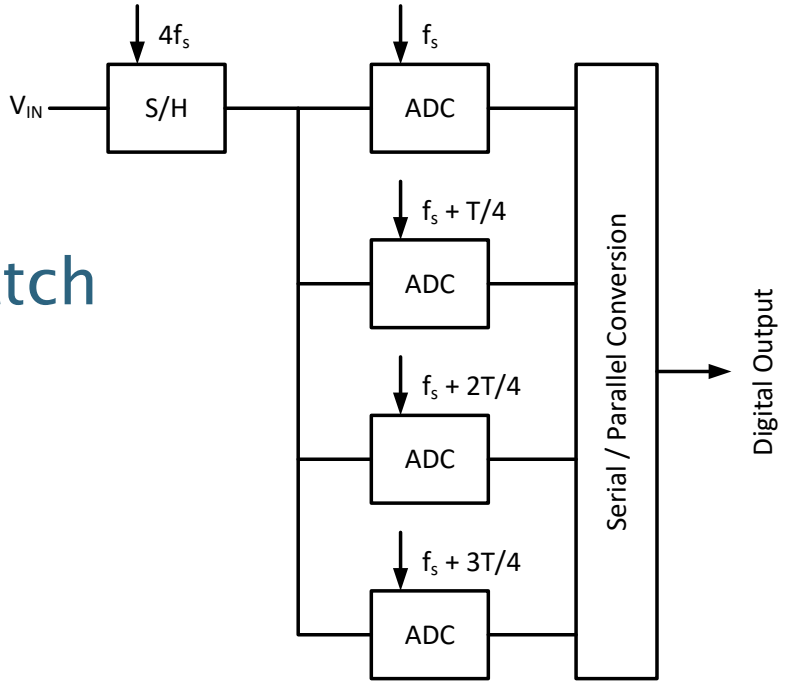
Folding Converter



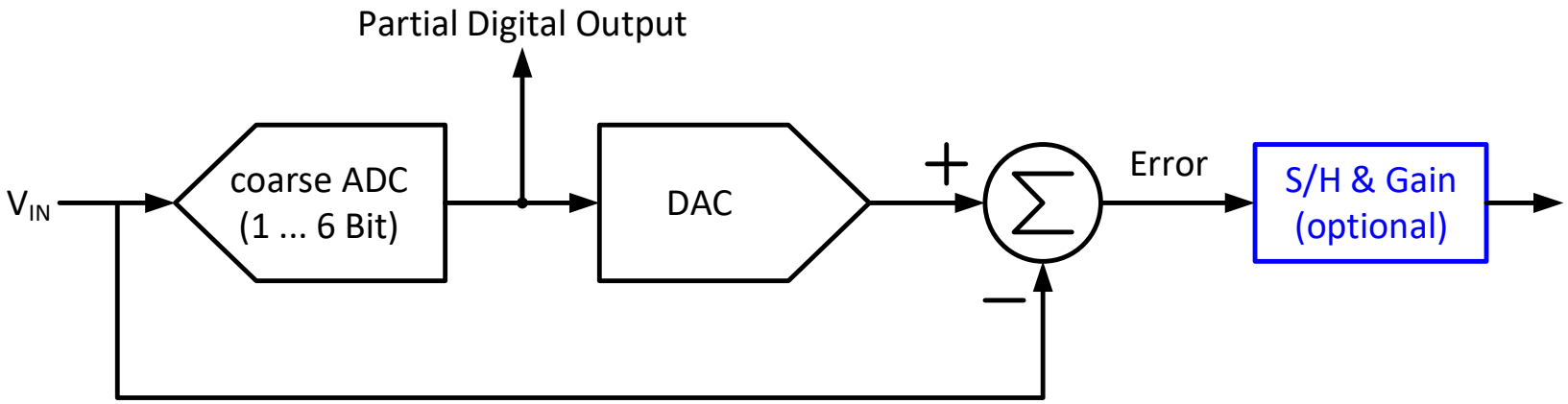
- Significantly fewer comparators than flash ~$2^{B/2+1}$
- Fast
- Nonidealities in folder limit resolution to ~10Bits

Time Interleaved Converter

- Extremely fast:
  Limited by speed of S/H
- Accuracy limited by mismatch
  in individual ADCs
  (timing, offset, gain, …)

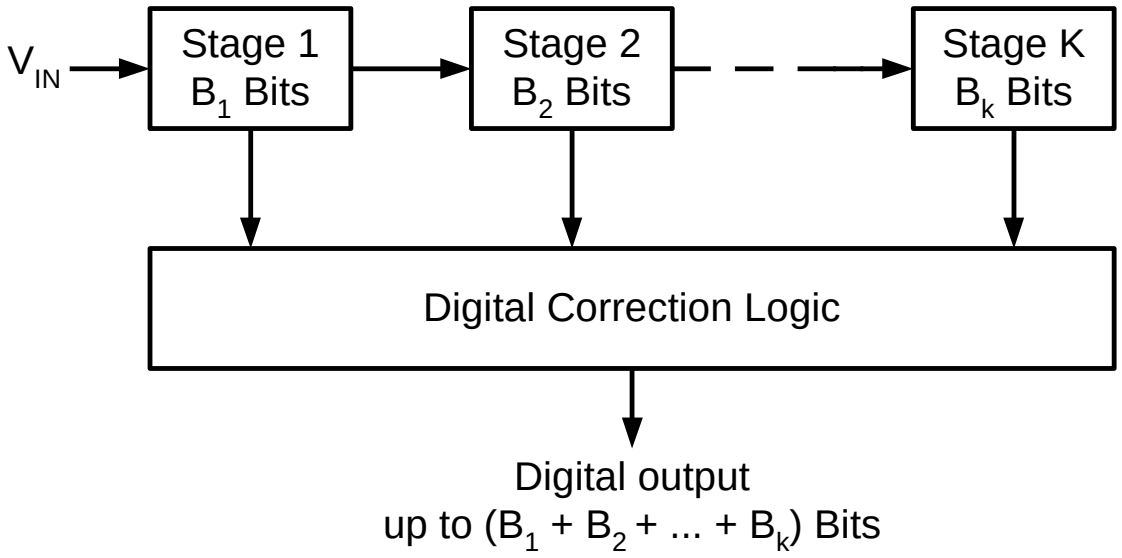


Residue Type ADC



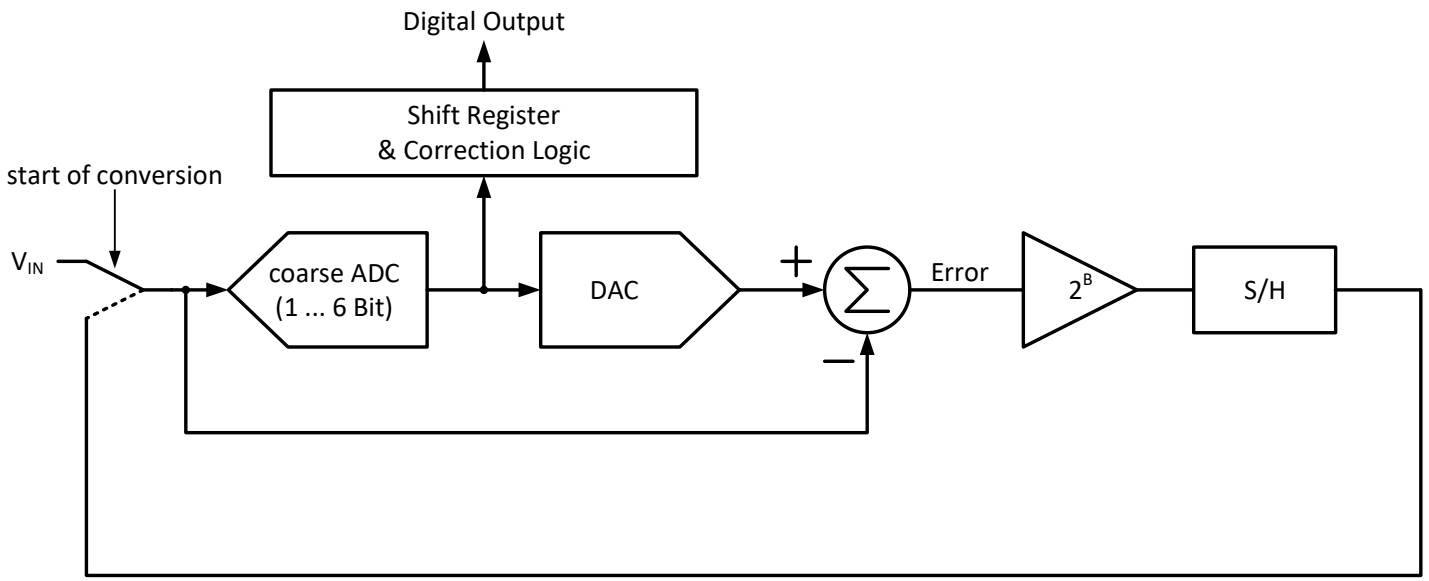
- Quantization error output (“residuum”) enables cascading for higher resolution
- Flexibility for stages: flash, oversampling ADC, …
- Optional S/H enables parallelism (pipelining)
- Fast: one clock per conversion (with S/H), latency

Pipelined ADC



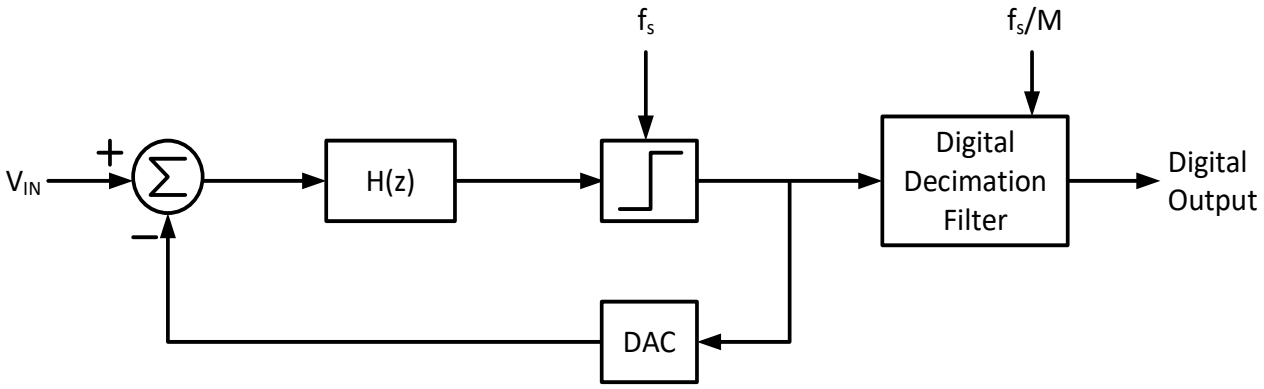
- Approaches speed of flash, but lower complexity
- One clock per conversion, but K clocks latency
- Efficient digital calibration possible
- Versatile: from 16Bits/1MS/s to 14Bits/100MS/s

Algorithmic ADC



- Essentially same as pipeline, but a single stage is used for all partial conversions
- K clocks per conversion

Oversampled ADC



- Hard to comprehend … "easy" to build
- Input is oversampled (M times output rate)
- Reduces Anti-Aliasing filter requirements and capacitor size
- Accuracy independent of component matching
- Very high resolution achievable (> 20 Bits)

Nyquist ADC Architectures

- Nyquist rate
  - Word-at-a-time
    - Flash ADC
    - Instantaneous comparison with 2^B-1 reference levels
  - Multi-step
    - E.g. pipeline ADCs
    - Coarse conversion, followed by fine conversion of residuum
  - Bit-at-a-time
    - E.g. successive approximation ADCs
    - Conversion via a binary search algorithm
  - Level-at-a-time
    - E.g. single or dual slope ADCs
    - Input is converted by measuring the time it takes to charge/discharge a capacitor from/to input voltage

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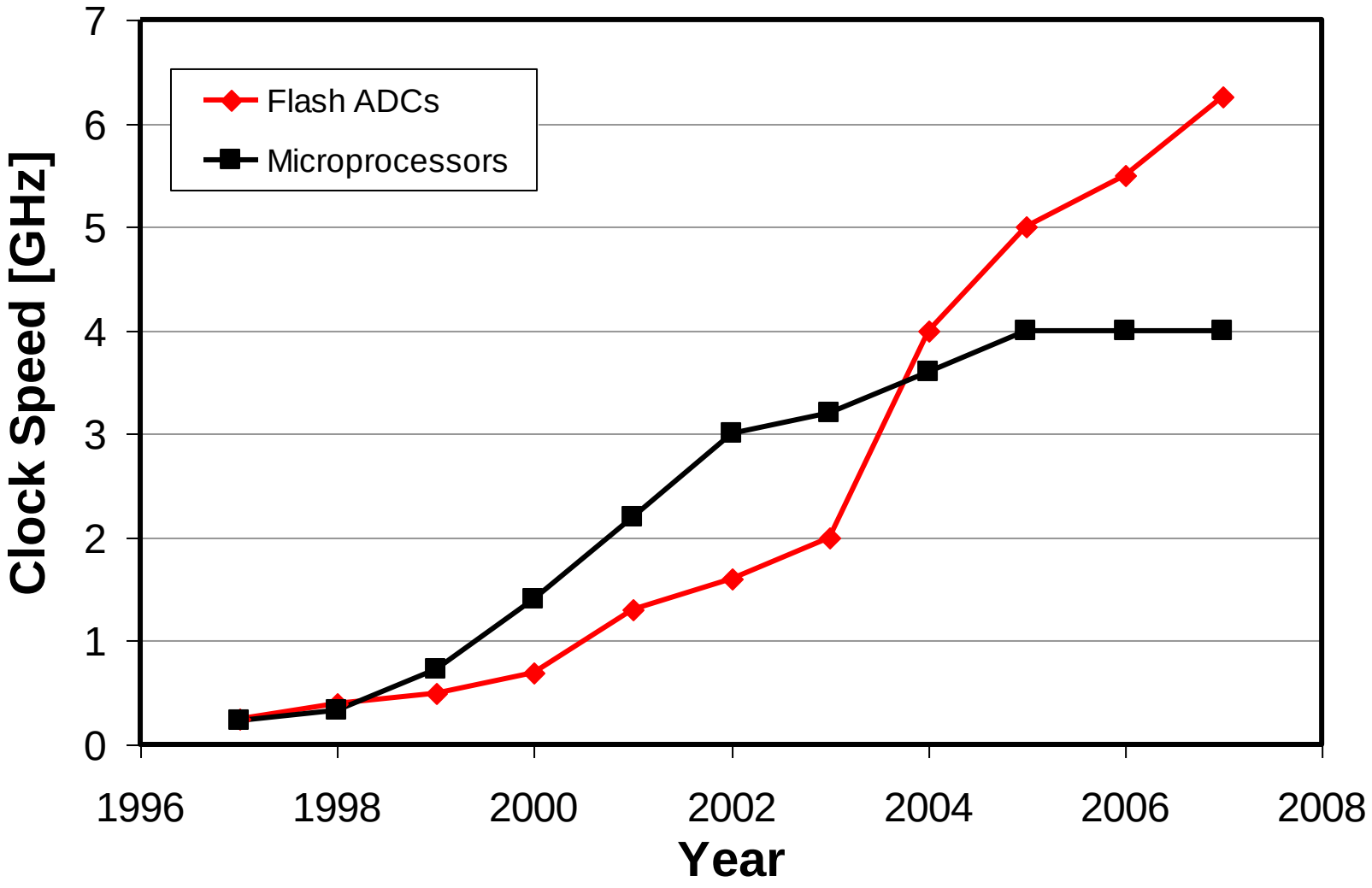
Flash Converters

High-Speed A/D Converter

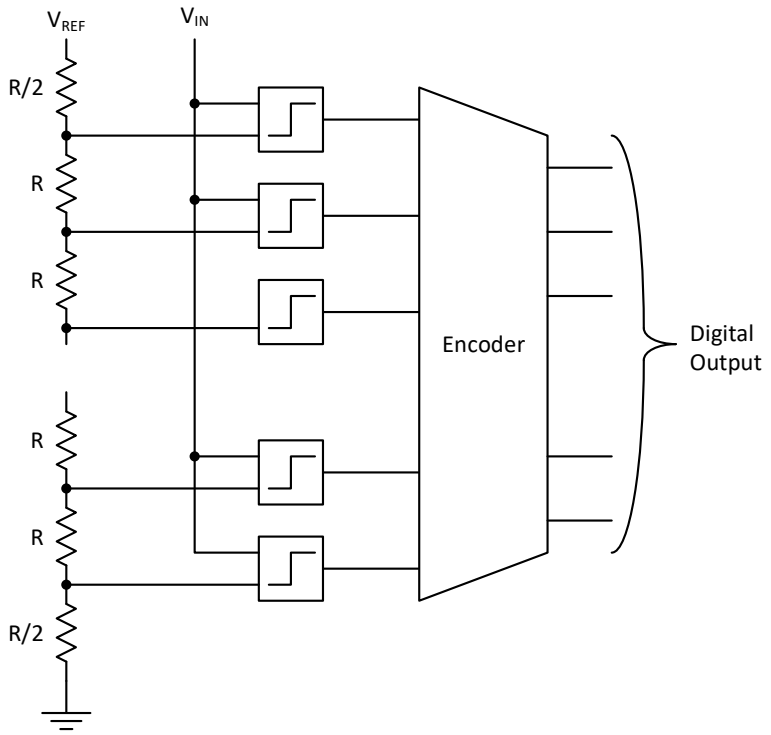
- Flash Converter
  - Comparator
  - Binary Encoder
- Interpolation
- Folding

Flash ADC Speed

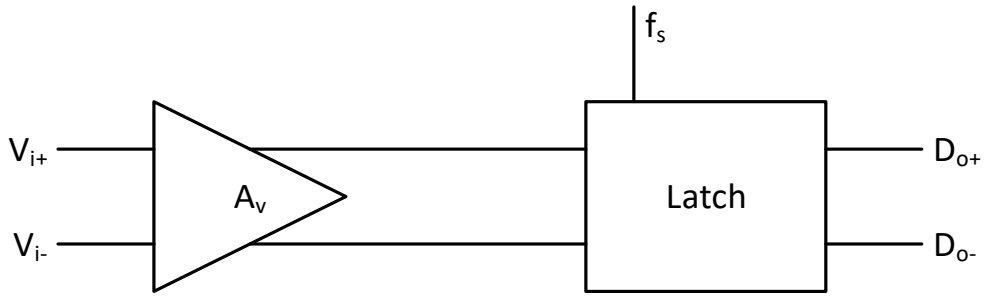


Flash Converter

- Very fast: only 1 clock cycle per conversion
- High complexity: 2^B-1 comparators for 2^B levels
- R/2 at ends → end points ½ LSB beyond end transition
- High input capacitance

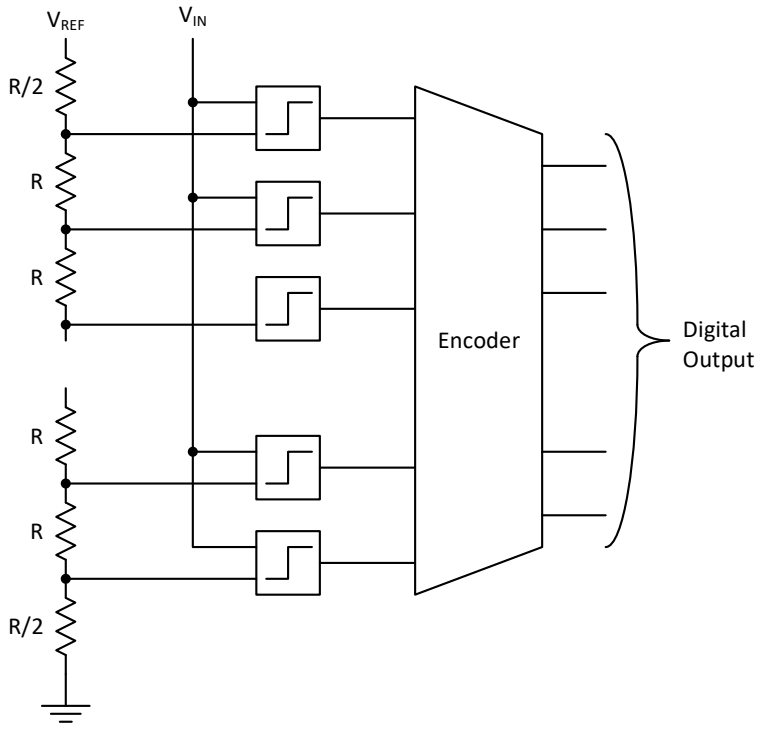


Comparator



- Clock rate f_s
- Resolution
- Overload Recovery
- Input capacitance (and linearity!)
- Power dissipation
- Common-mode rejection
- Kickback noise
- …

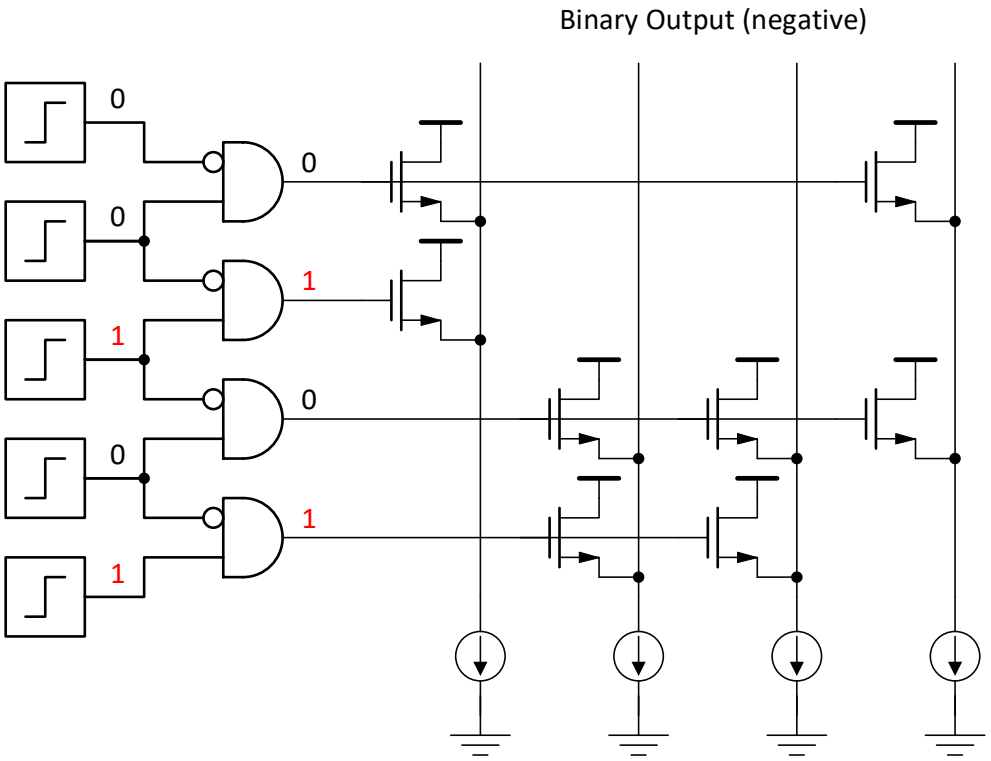
Flash Converter Errors



- Comparator input:
  - Offset
  - Nonlinear input capacitance
  - Kickback noise (disturbs reference)
  - Signal dependent sampling time
- Comparator output:
  - Sparkle codes (…111101000…)
  - Metastability

Ref: Analog Devices application note: "Find Those Elusive ADC Sparkle Codes and Metastable States"
http://www.analog.com/en/content/0,2886,760%255F788%255F91218,00.html

Sparkle Codes



Correct Output:

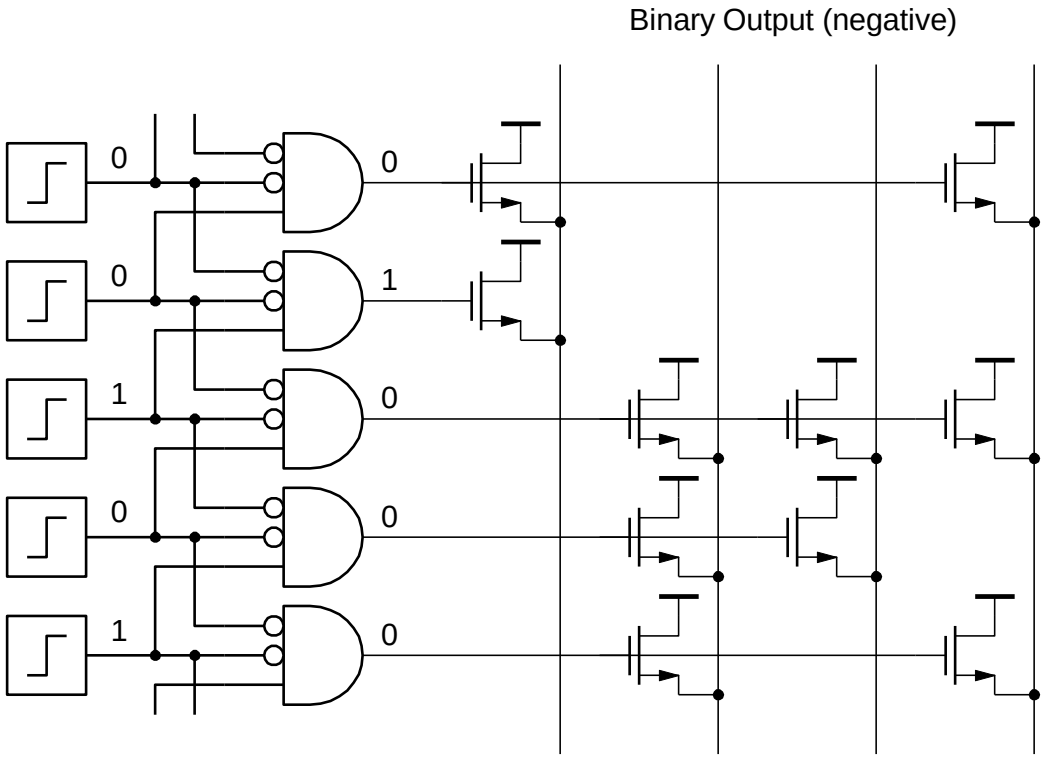
0110 …

1000

Actual Output:

1110

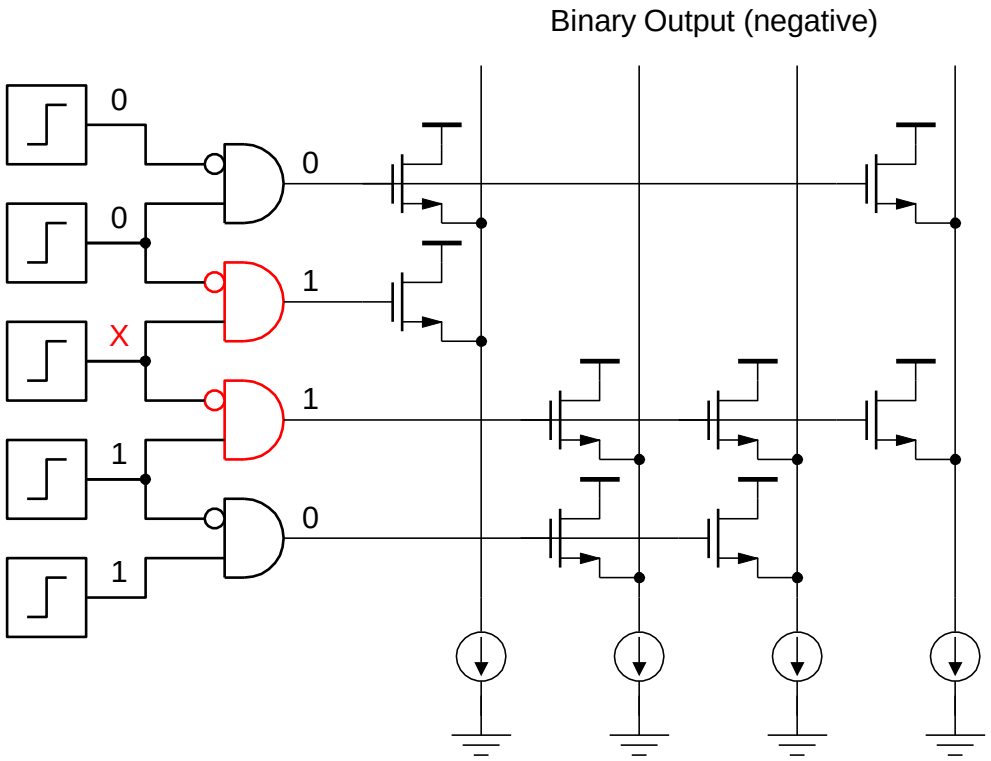
Sparkle Tolerant Encoder



Protects against a *single* sparkle.

Ref: C. Mangelsdorf et al, "A 400-MHz Flash Converter with Error Correction," JSSC February 1990, pp. 997-1002.

Meta Stability



Different gates interpret metastable output X differently

Correct Output:0111 or 1000

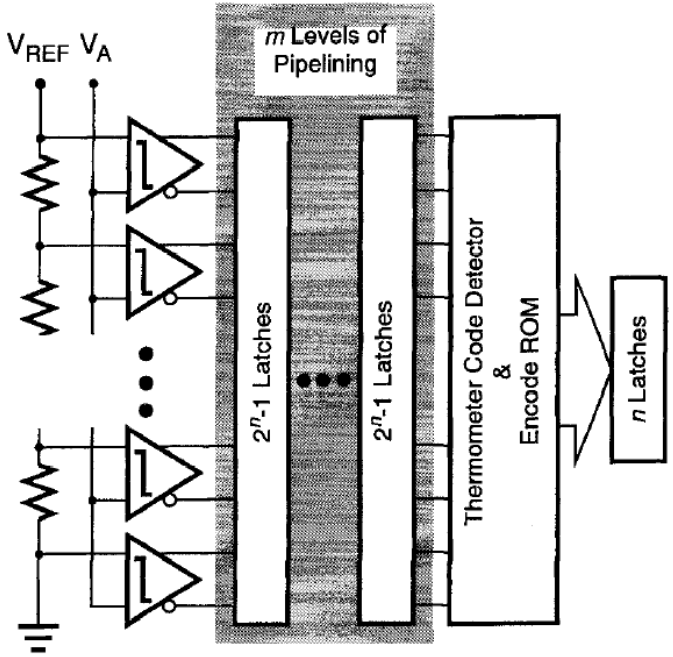
Actual Output: 1111

Solutions:

- Latches (high power)
- Gray encoding
- Adder

Ref: C. Portmann and T. Meng, "Power-Efficient Metastability Error Reduction in CMOS Flash A/D Converters," JSSC August 1996, pp. 1132-40.

Solution 1: Latch Pipelining



- Use additional latches to create extra gain before generating decoder signals
- High power and area inefficient

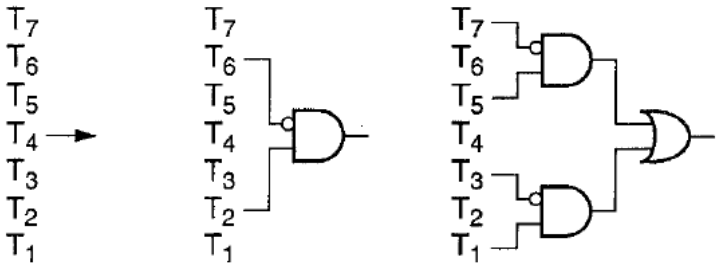
Solution 2: Gray Encoding

Thermometer Code							Gray			Binary		
T_1	T_2	T_3	T_4	T_5	T_6	T_7	G_3	G_2	G_1	B_3	B_2	B_1
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	0	0	1	1	0	1	0
1	1	1	0	0	0	0	0	1	0	0	1	1
1	1	1	1	0	0	0	1	1	0	1	0	0
1	1	1	1	1	0	0	1	1	1	1	0	1
1	1	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1	0	0	1	1	1

$$G_1 = T_1\overline{T_3} + T_5\overline{T_7}$$

$$G_2 = T_2\overline{T_6}$$

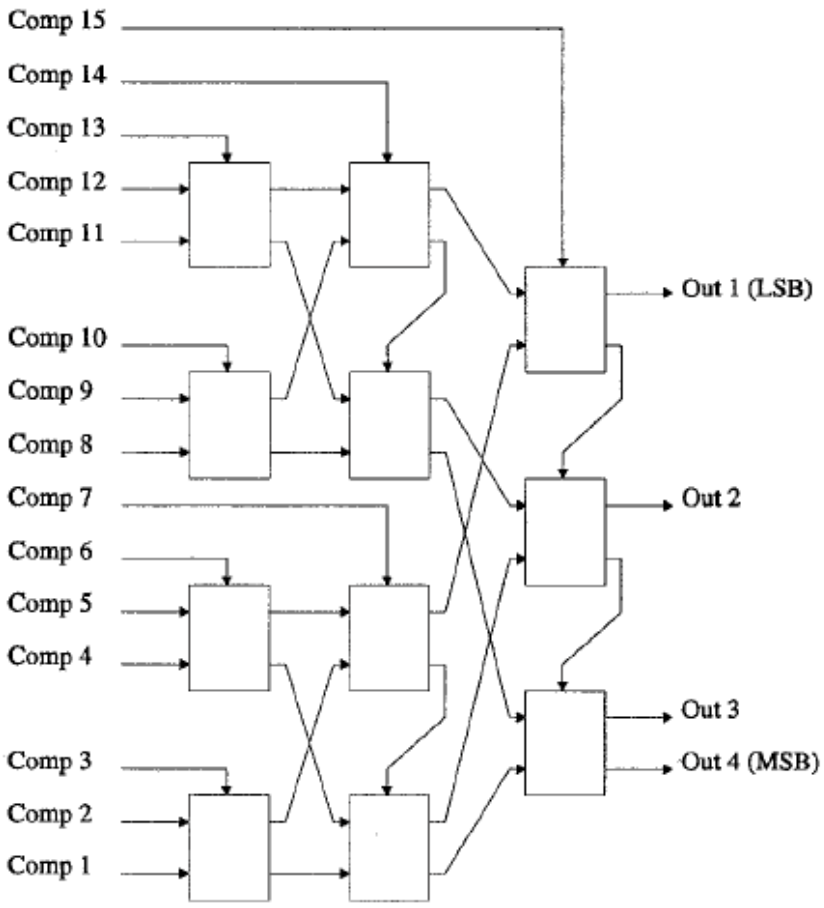
$$G_3 = T_4$$



- Each T_i affects only one G_i
  → Avoids disagreement of interpretation by multiple gates
- Protects also against sparkles
- Follow Gray encoder by (latch and) binary encoder

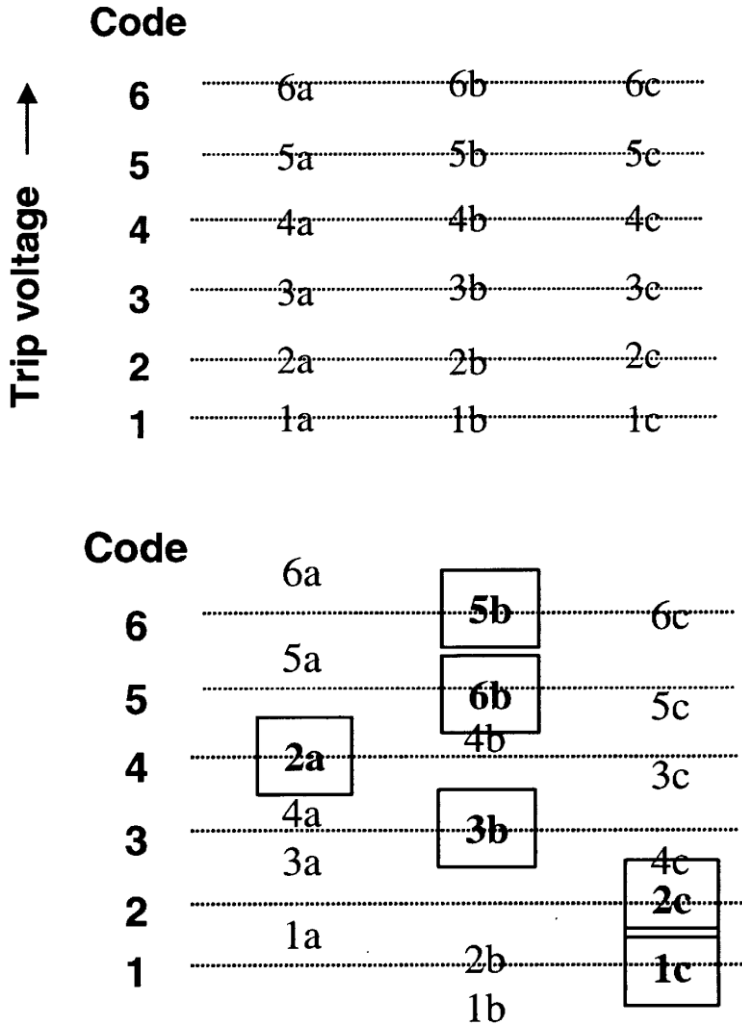
Solution 3: Adder

- Wallace-tree adder
- F. Kaess et al., "New encoding scheme for high-speed flash ADC's," in Proceedings of 1997 IEEE International Symposium on Circuits and Systems, 1997. ISCAS '97., vol. 1, pp. 5-8 vol.1, June 1997

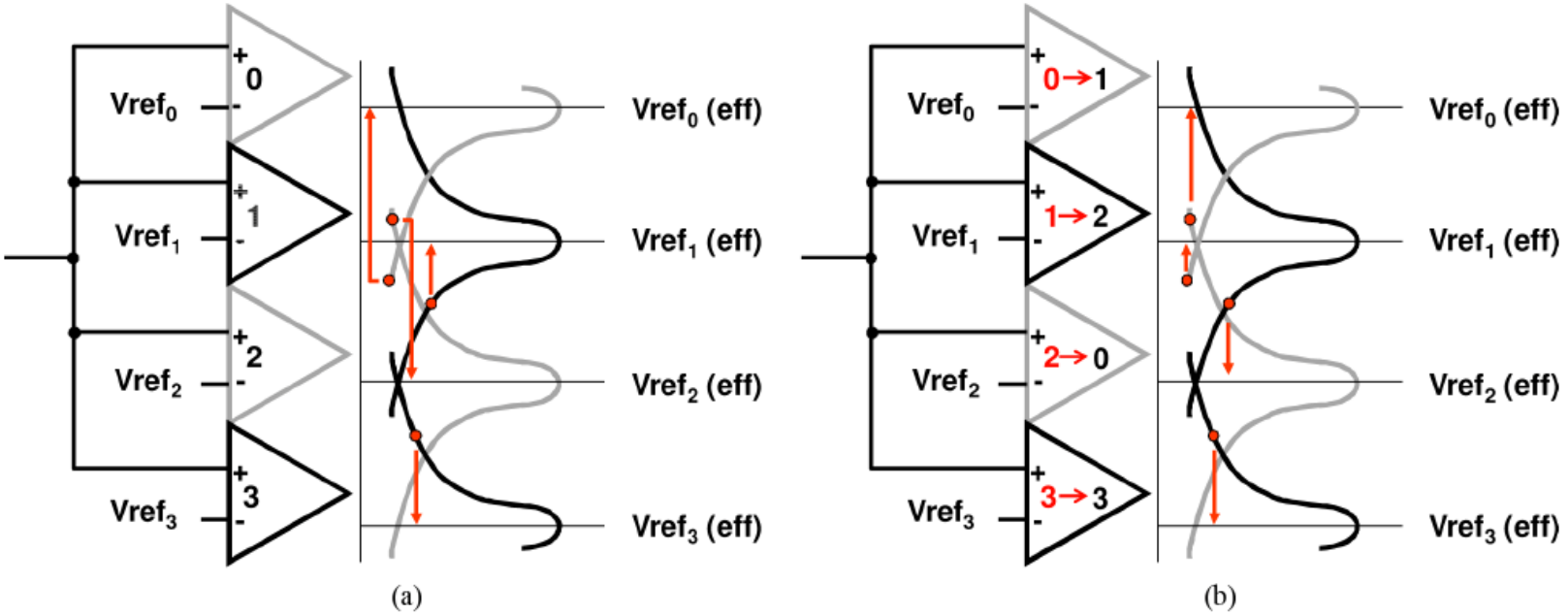


Redundant Comparators

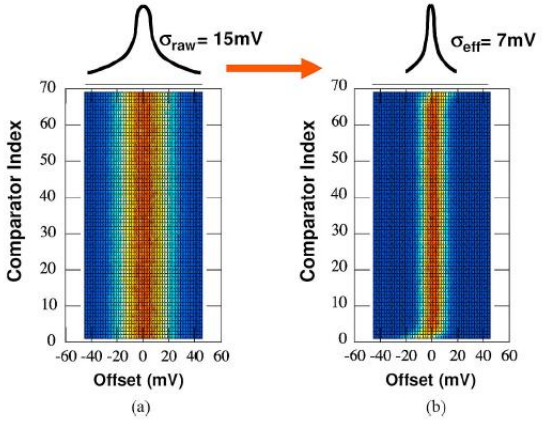
- Redundant comparators
  [M. P. Flynn, C. Donovan, and L. Sattler, "Digital calibration incorporating redundancy of flash ADCs," *IEEE J. Solid-State Circuits*, vol. 50, pp. 205–213, May 2003]
- Choose comparators at power-on
- Implementation: select input diff pairs of comparator



Reorder comparators



- [A. Varzaghani et al., "A 10.3-GS/s, 6-Bit flash ADC for 10g ethernet applications," *IEEE J. Solid-State Circu* vol. 48, pp. 3038-3048, Dec. 2013]
- Automatically reorder comparators using adder (therm → binary)
- Monte Carlo simulations



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Interpolation

Offset

- Typically want offset of each comparator < ¼ LSB
  - If we budget half of the input referred offset for the latch, the other half for the pre-amp, this means pre-amp offset must be < ¼ LSB / sqrt(2)

$$3\sigma_{VOS} = 3\frac{A_{VT}}{\sqrt{WL}} < \frac{1}{4\sqrt{2}}\frac{\text{FSR}}{2^B}$$

- E.g. 6-bit flash ADC, FSR=1V:

$$3\frac{A_{VT}}{\sqrt{WL}} < \frac{1}{4\sqrt{2}}\frac{1V}{2^6} = 2.8mV$$

$$WL > \left(\frac{3A_{VT}}{2.8mV}\right)^2 = \left(\frac{3 \cdot 4mV\mu m}{2.8mV}\right)^2 = 18.4\mu m^2 \Rightarrow W > \frac{18.4\mu m^2}{0.18\mu m} = 102\mu m$$

Huge!

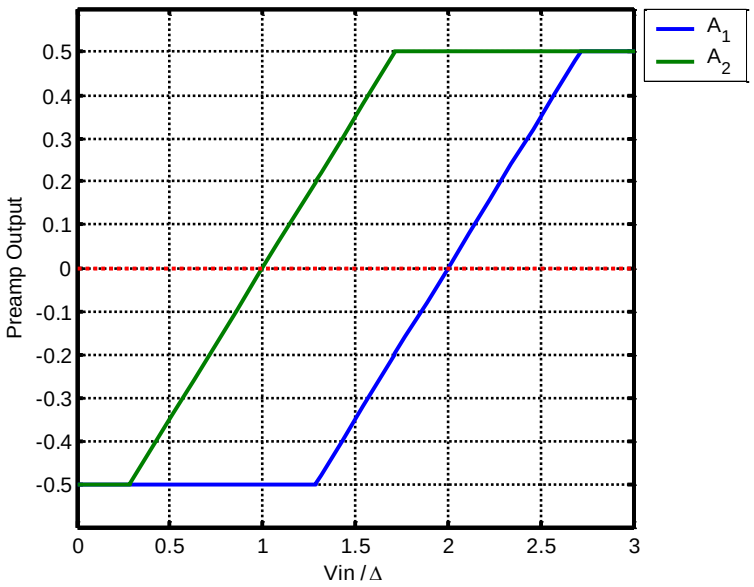
Options

- Simply use large devices
  - For each extra bit, need to increase width by 4x, also need to double number of comparators
  - Assuming constant current density, this means each additional bit costs 8x in power!
- Offset cancellation
  - Tends to cost speed
- Offset averaging
- Calibration and/or postprocessing techniques

Interpolation

- Idea
  - Interpolation between preamp outputs
- Reduces number of preamps
  - Reduced input capacitance
  - Reduced area, power dissipation
- Same number of latches
- Important “side-benefit”
  - Decreased sensitivity to preamp offset
  - → improved DNL

Preamp Output

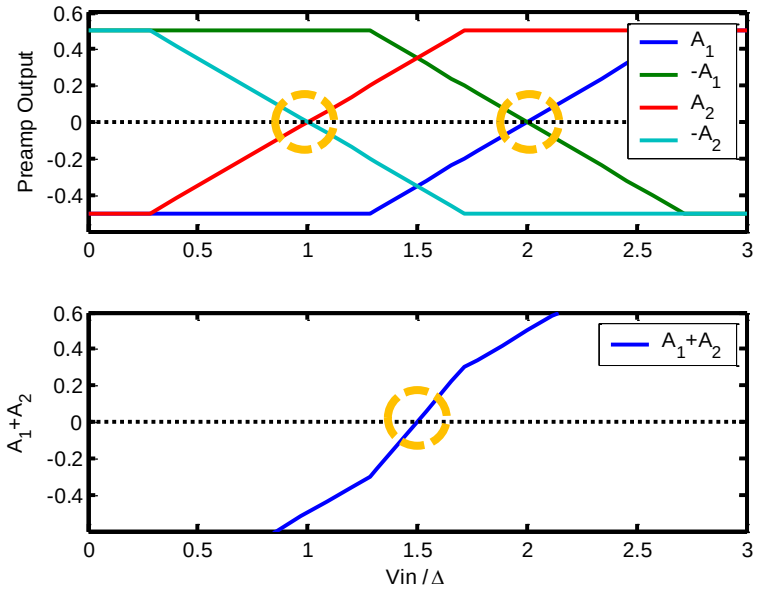


Zero crossings (to be detected by latches) at V_{in} =

$V_{ref1} = 1\ \Delta$

$V_{ref2} = 2\ \Delta$

Differential Preamp Output



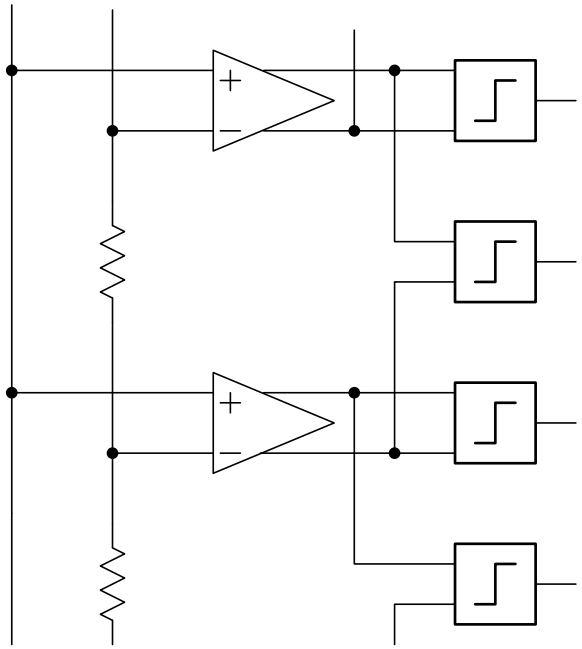
Zero crossings at V_{in} =

$V_{ref1} = 1\ \Delta$

$V_{ref12} = 0.5*(1+2)\ \Delta$

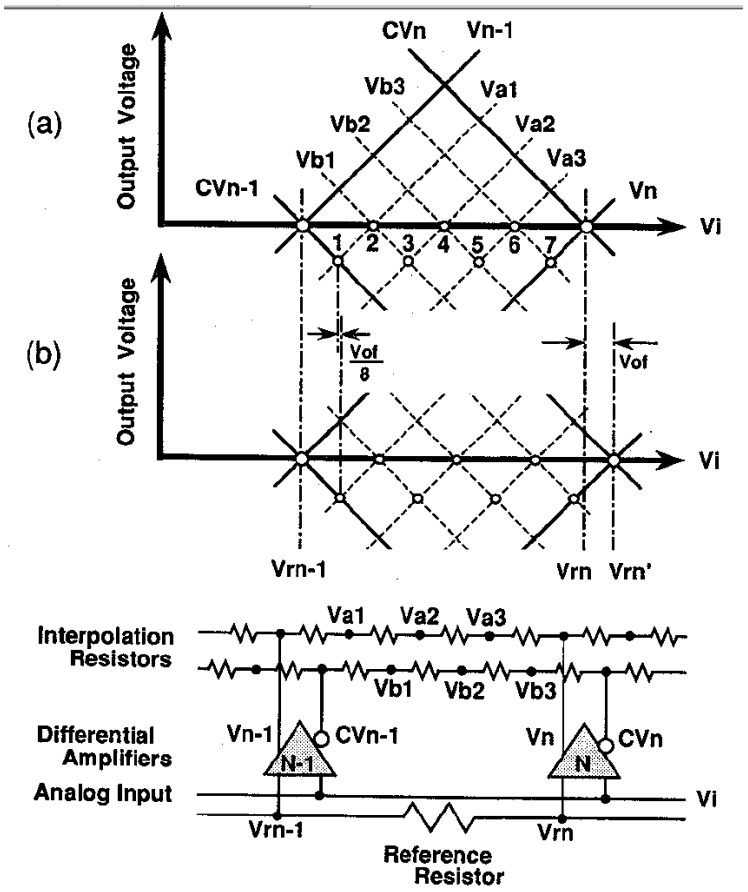
$V_{ref2} = 2\ \Delta$

Interpolation in Flash ADC



Half as many reference voltages and preamps

Resistive Interpolation



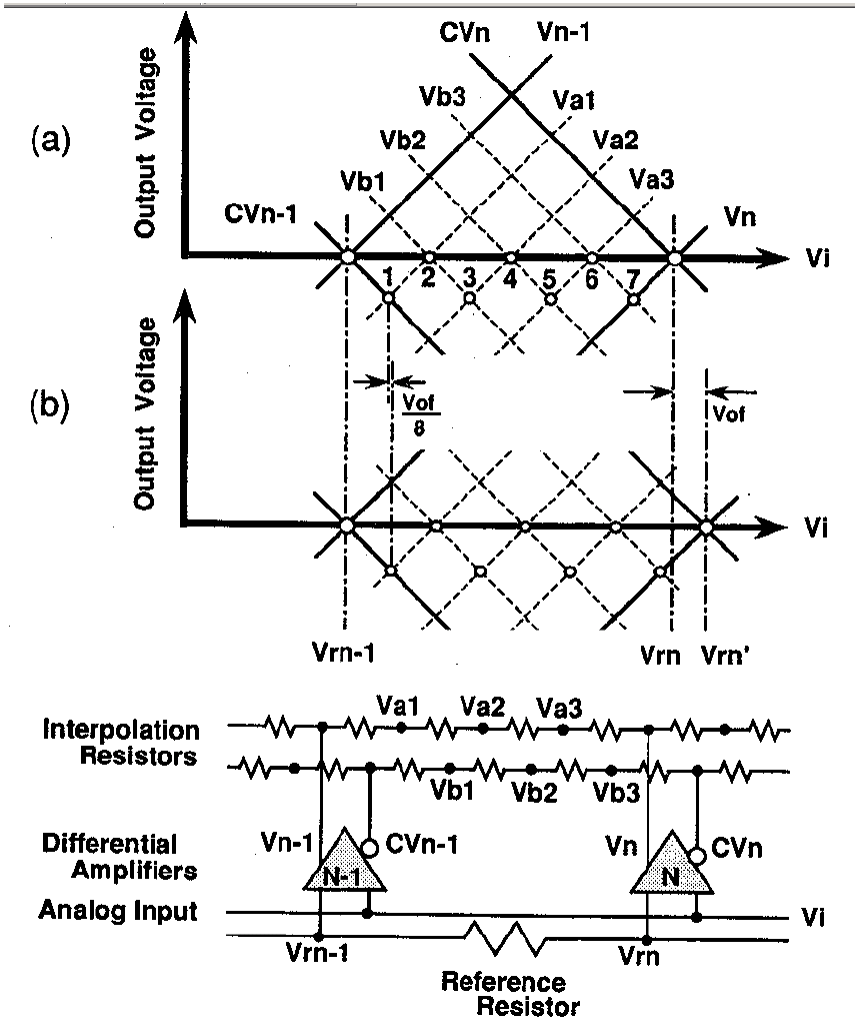
Resistive Interpolation

- Resistors produce additional levels
- Interpolation factor
  = ratio of latches / preamps
- With 4 resistors, the "interpolation factor" M=8

Preamp offset distributed over M resistively interpolated voltages:
→ impact on DNL divided by M

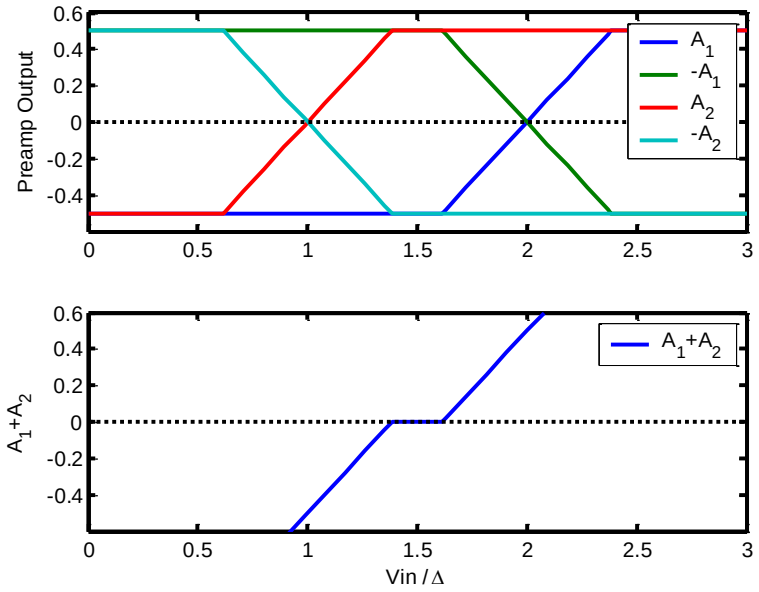
Ref: H. Kimura et al, "A 10-b 300-MHz Interpolated-Parallel A/D Converter," JSSC April 1993, pp. 438-446.

DNL Improvement



- Preamp offset distributed over M resistively interpolated voltages:
  → impact on DNL divided by M
- Latch offset divided by gain of preamp
  → use "large" preamp gain …
  → but …

Preamp Input Range



Linear preamp input ranges must overlap

i.e. range > Δ

Sets upper bound on gain << V_{DD} / Δ

Example

Resolution		10 b
Maximum conversion frequency		300 MHz
Integral non-linearity		±1.0 LSB
Differential non-linearity		±0.4 LSB
SNR/THD	10MHz input	56/-59 dB
	50MHz input	48/-47 dB
Input capacitance		8 pF
Input range		2 V
Power supply		-5.2V
Power dissipation		4.0W
Chip size		9.0 × 4.2 mm^2
Element count		36,000
Technology		1.0 μm bipolar:ft=25GHz

Ref: H. Kimura et al, "A 10-b 300-MHz Interpolated-Parallel A/D Convterter," JSSC April 1993, pp. 438-446.

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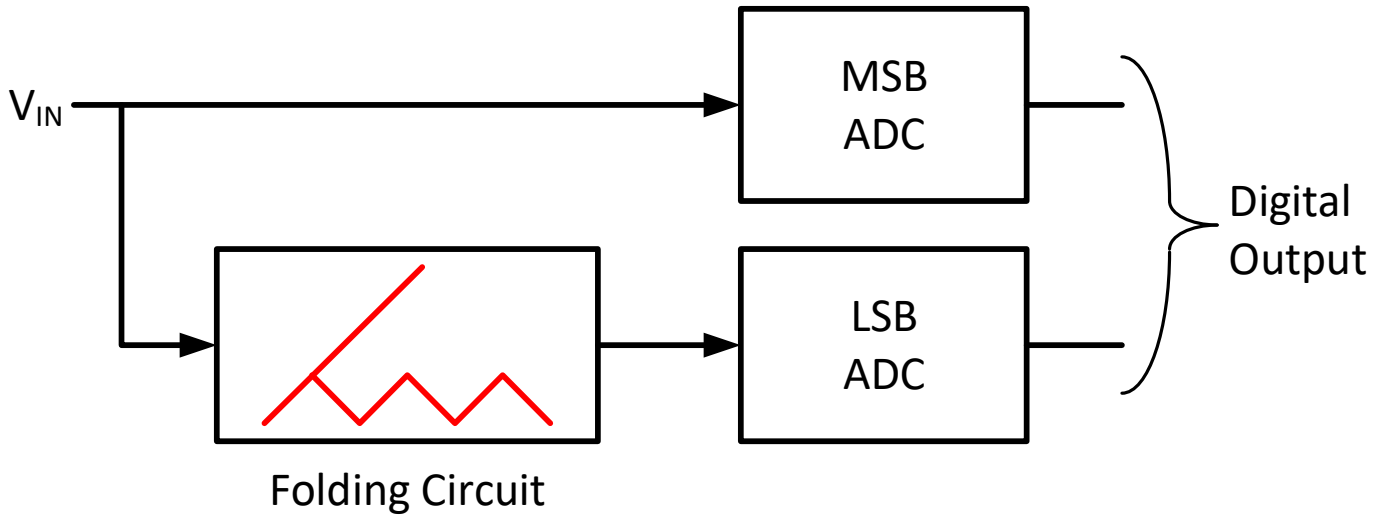
Folding ADCs
Folding & Interpolating ADCs

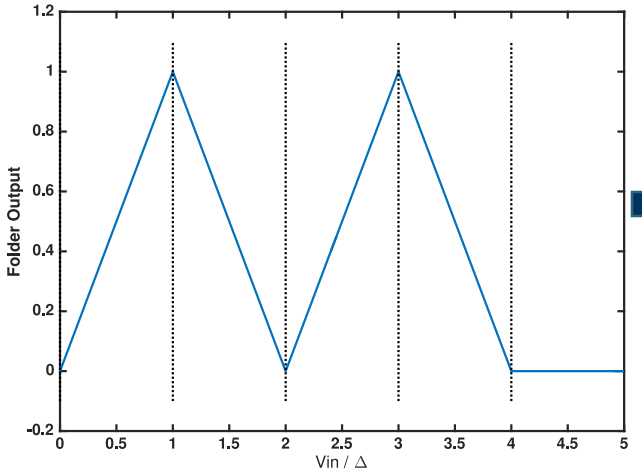
Folding Converter



- Significantly fewer comparators than flash $\sim 2^{B/2+1}$
- Reduced input capacitance
- Nonidealities in folder limit resolution to ~10Bits

Folding

- Folder maps input to smaller range
- MSB ADC determines which fold input is in
- LSB ADC determines position within fold
- Logic circuit combines LSB and MSB results

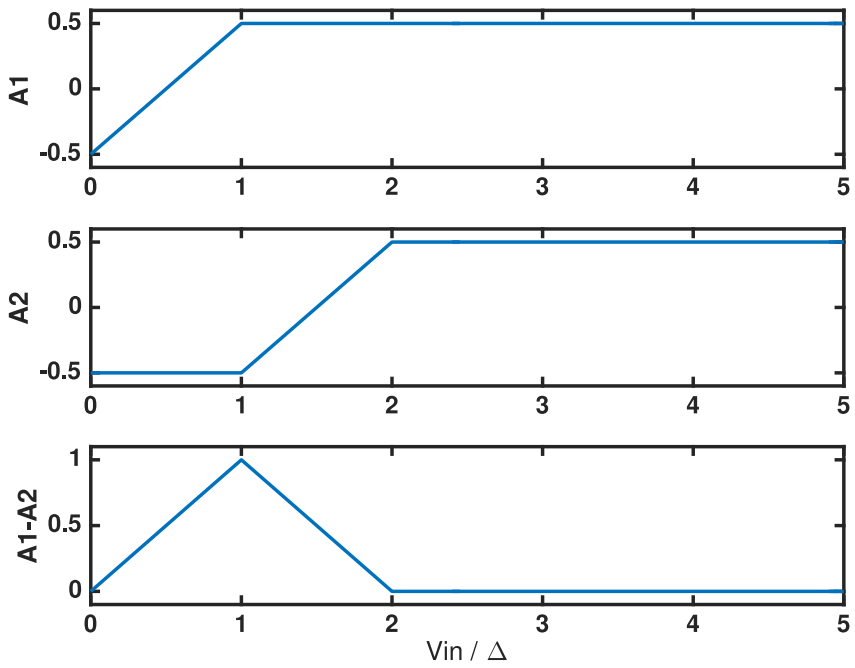


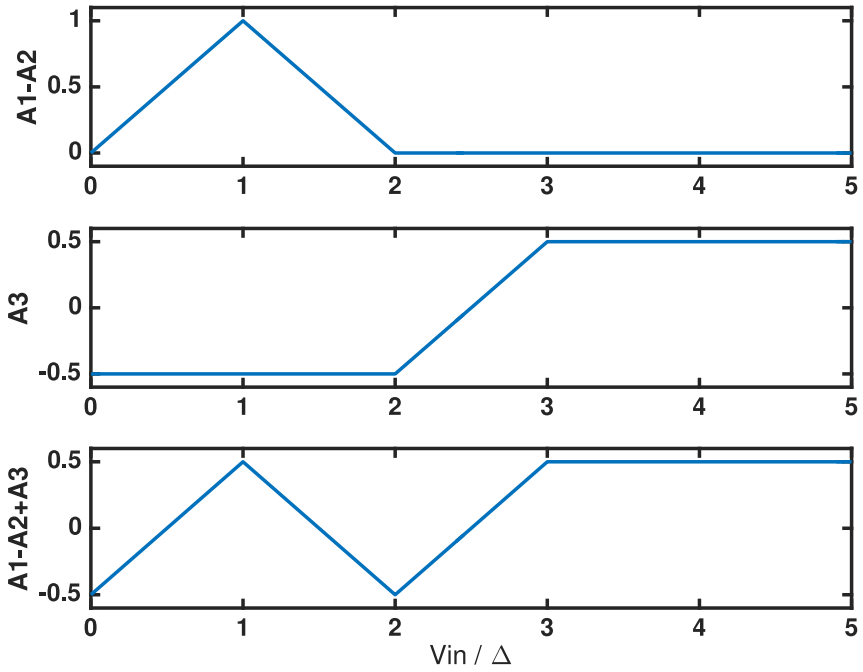
LSB ADC

MSB ADC
Low resolution
(determine fold)

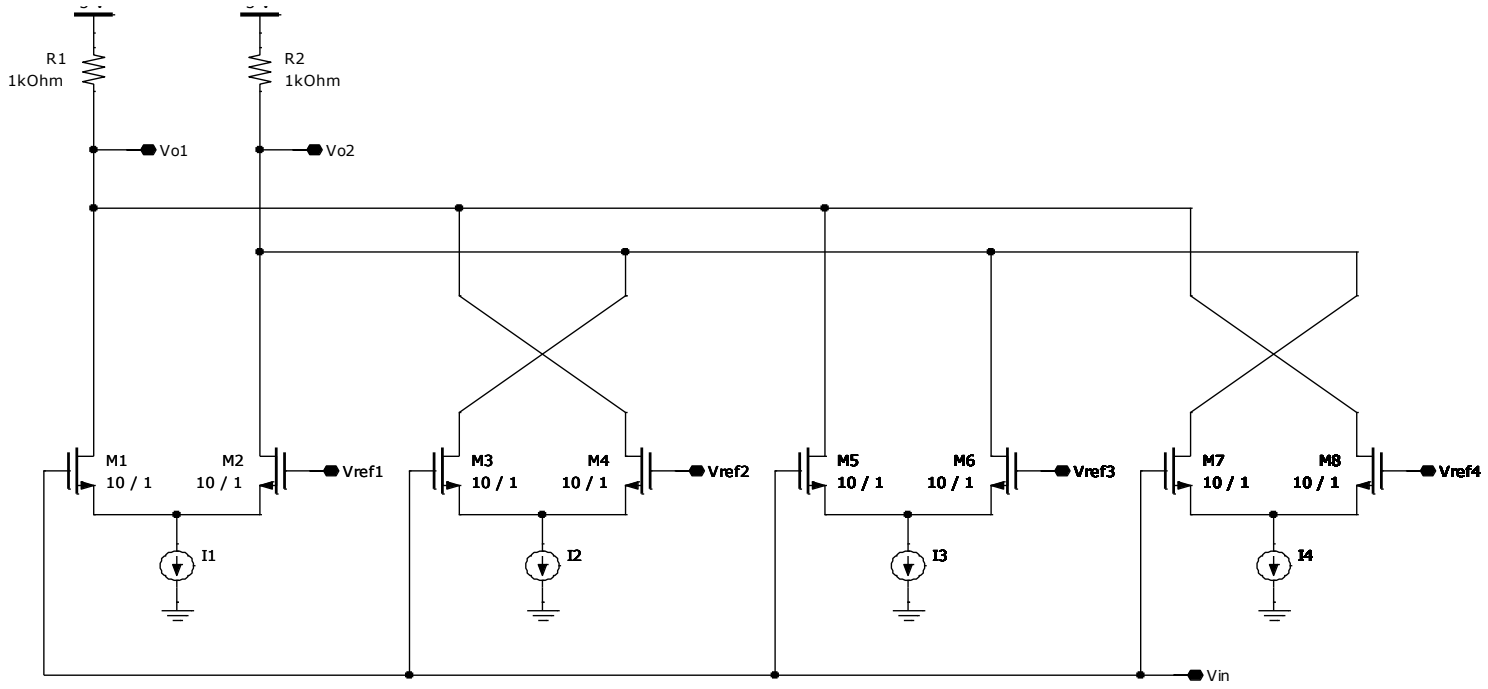
Analog Input

Generating Folds

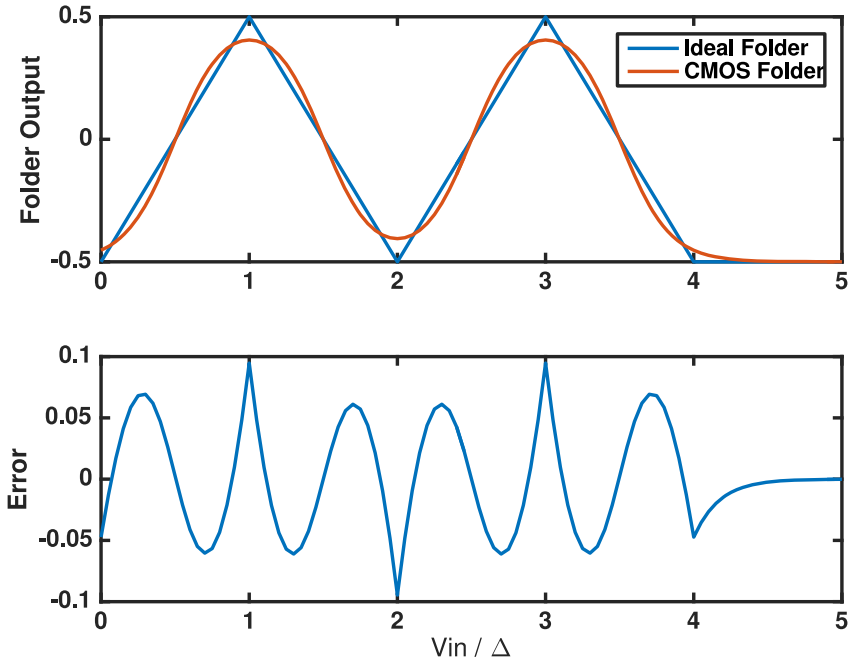




Folding Circuit

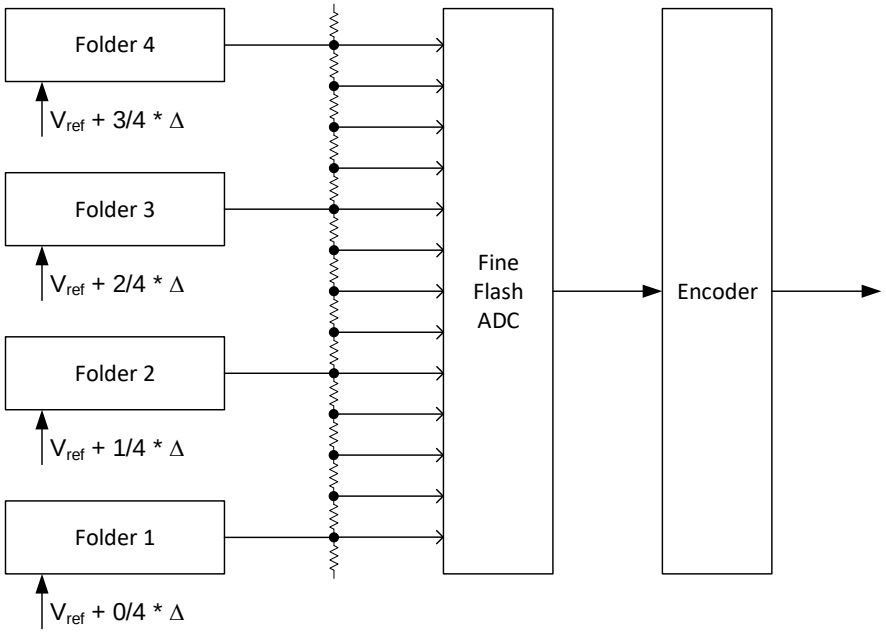


CMOS Folder Output



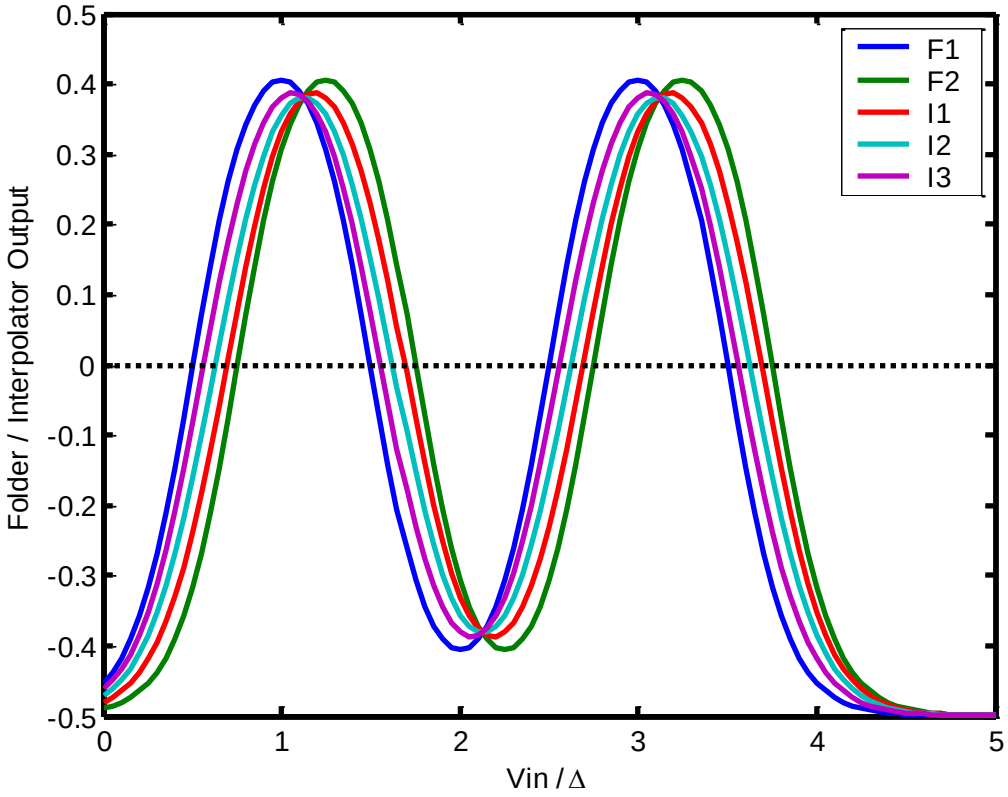
- Accurate only at zero-crossings
- Most folding ADCs do not actually use the folds, but only the zero-crossings!

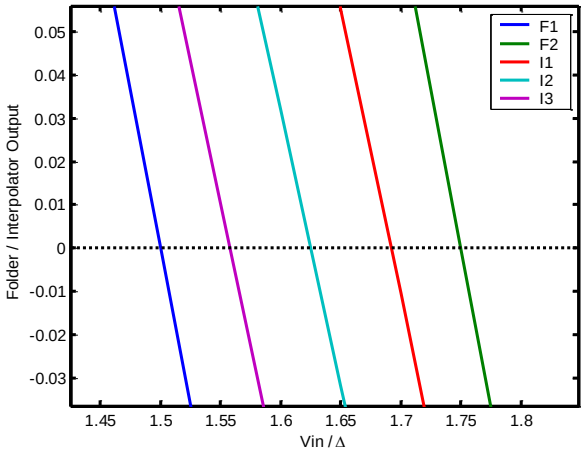
Folding & Interpolation



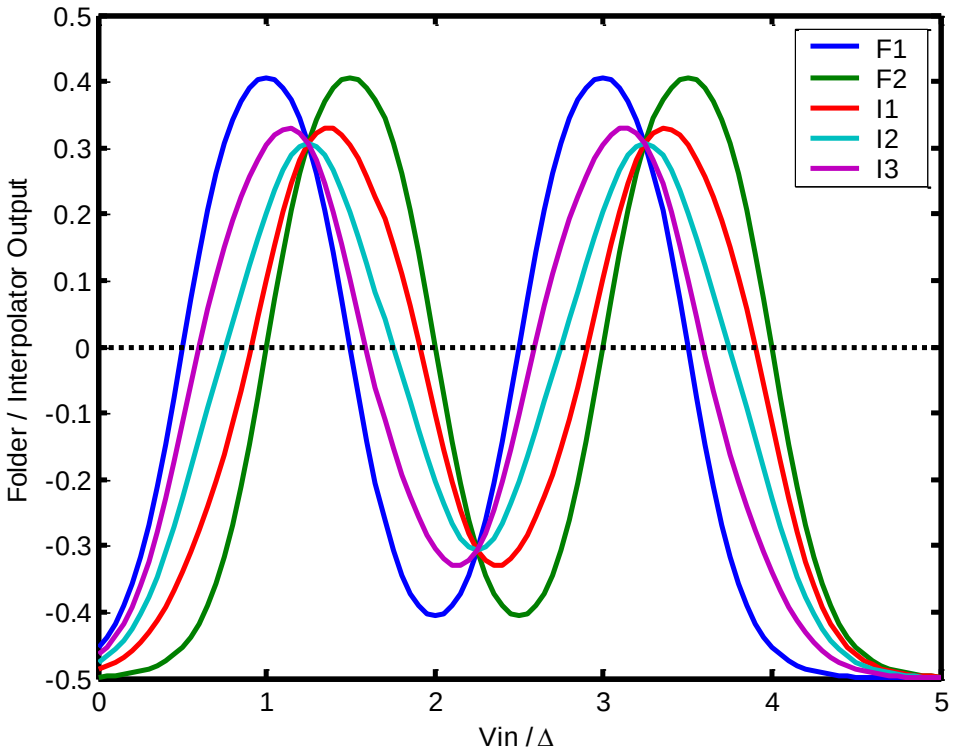
- Parallel folders
- Interpolate folder outputs

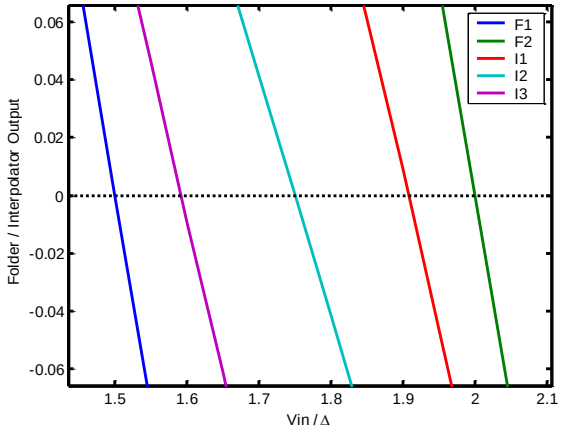
Folder / Interpolator Output





Folder / Interpolator Output

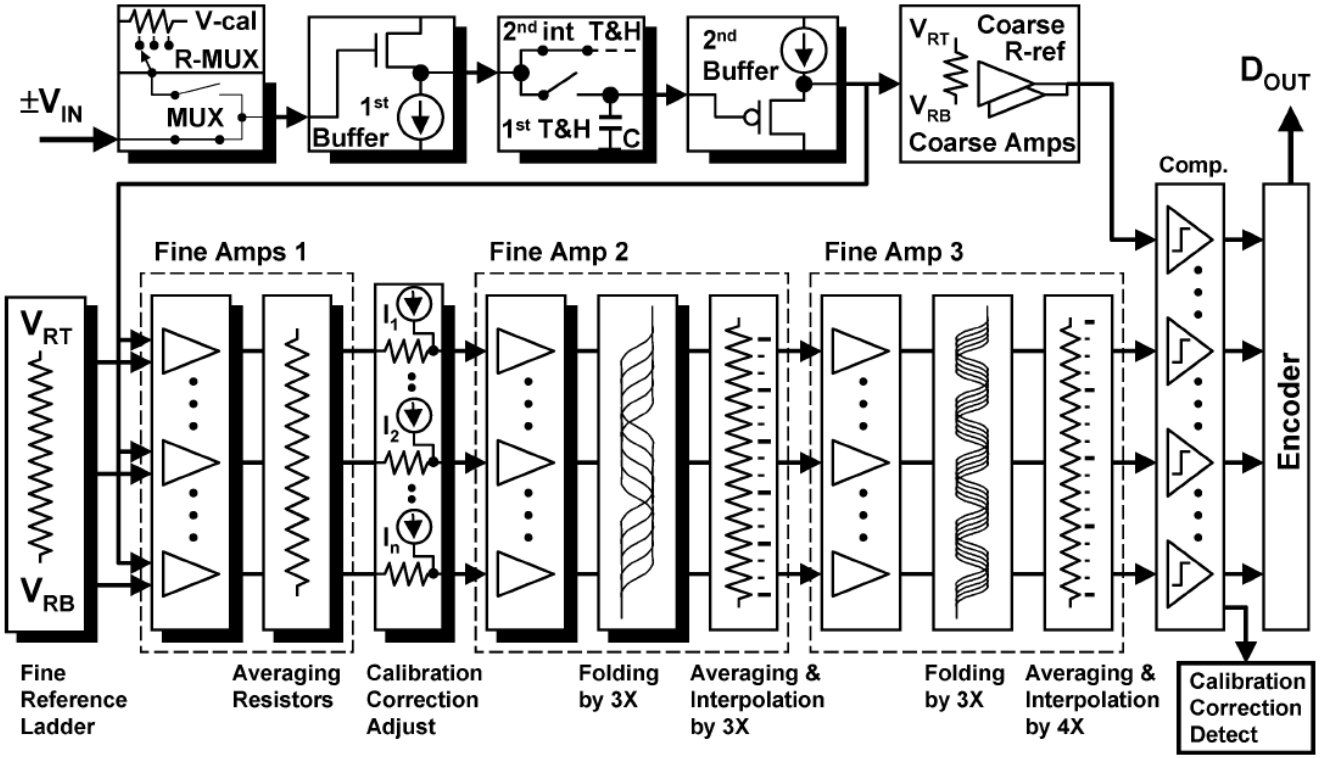




Interpolate only between closely spaced folds to avoid nonlinear distortion

Folding and Interpolationg ADC Example

R. C. Taft et al., "A 1.8-V 1.6-GSample/s 8-b self-calibrating folding ADC with 7.26 ENOB at Nyquist frequency," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2107–2115, Dec. 2004



Each folding stage:
- 9 x 3 diff pairs
- 3x folding
- 9 outputs

9x overall folding

9x reduction # comp

Folding and Interpolationg ADC Example

TABLE I
PERFORMANCE SUMMARY AT 1.6 GS/S FOR A SINGLE ADC

	F_{IN} = 97.77 MHz	F_{IN} = 797.77 MHz (Nyquist)
Sample Rate, F_S	1.6 GS/s	
Resolution	8 bits	
Max DNL	±0.15 LSB	
Max INL	±0.35 LSB	
SNR	48 dB	46 dB
SFDR	61 dB	56 dB
THD	- 57 dB	- 57 dB
ENOBs	7.60	7.26
Interleave aperture offset	< 0.35 ps @ F_S = 1 GS/s & F_{IN} = 1.5 GHz	
Input (–3 dB) Bandwidth	> 1.75 GHz	
Resolution (-0.5 ENOB) Bandwidth	1.0 GHz	
Input Range	±400 mV differential	
Input Capacitance	1.8 pF (to gnd, w/o package)	
Input Termination	50 Ω (100 Ω differential)	
Single Supply	1.8 V	
Analog (DC) Current	245 mA	
Switching (AC) Current	185 mA	
LVDS Output Drivers	90 mA	
ADC Core Power (w/o outputs)	774 mW	
ADC core area	3.6 mm^2	
ADC die area	16 mm^2 (for dual ADC, pad limited)	
Package	128-pin EPQFP	
Technology	0.18 μm CMOS (1-poly, 5-metal) No capacitor module nor dual-gate process	

R. C. Taft et al., "A 1.8-V 1.6-GSample/s 8-b self-calibrating folding ADC with 7.26 ENOB at Nyquist frequency," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2107–2115, Dec. 2004

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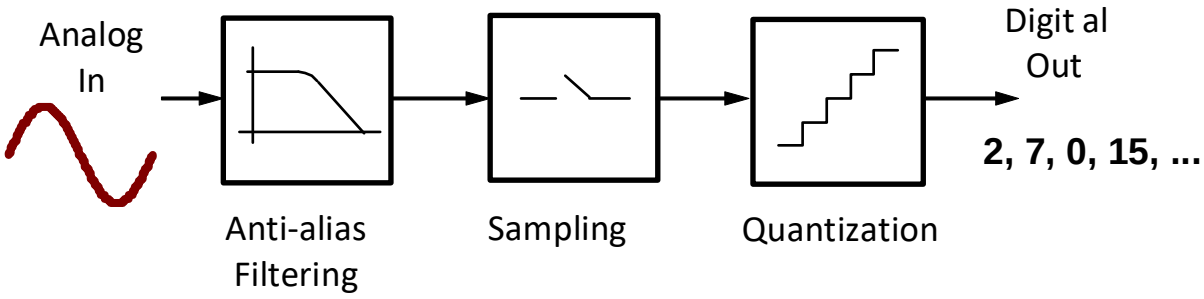
Track & Hold Amplifier

Recap

A/D Conversion

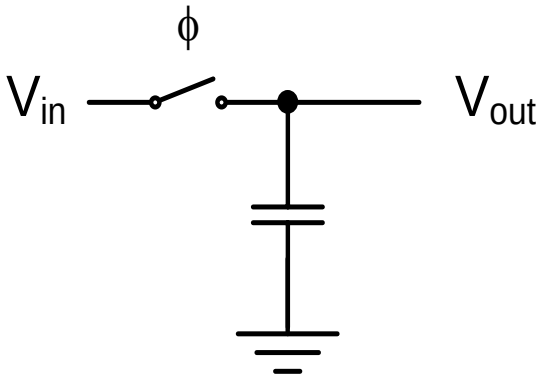


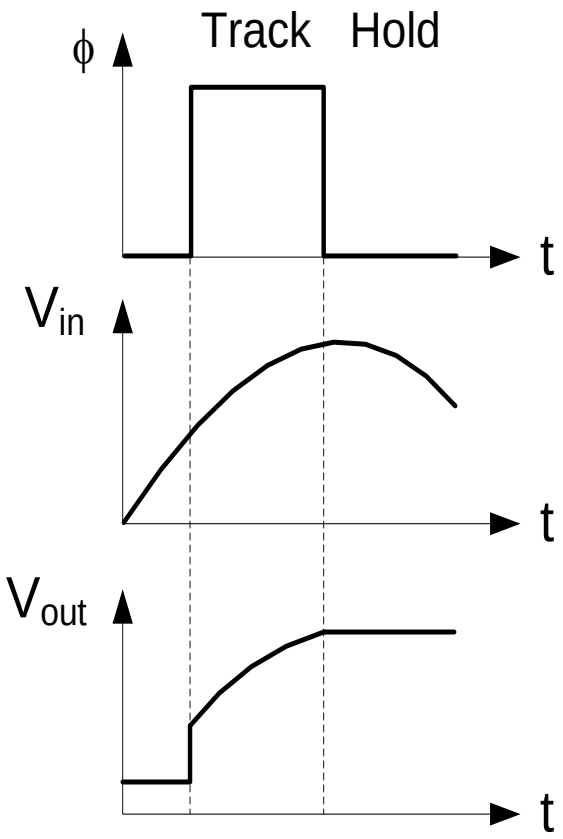
- How to build circuits that "sample"?
- Ideal Dirac sampling is impractical
  - Need a switch that opens, closes and acquires signal within an infinitely small time
- Practical solution
  - "Track & hold“
  - Customary to liberally use the term “SHA” = Sample & Hold, although the function is different

Outline

- Elementary track-and-hold circuit and its nonidealities
- First order improvements to elementary track-and-hold
- Advanced techniques
  - Clock bootstrapping
  - Bottom plate sampling
- Settling and noise analysis in charge-redistribution track-and-hold circuit
- Noise simulation example

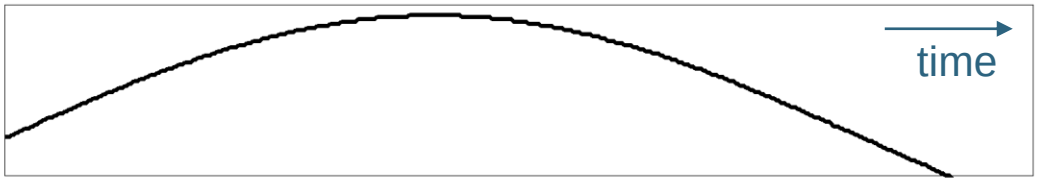
Ideal Track-and-Hold Circuit





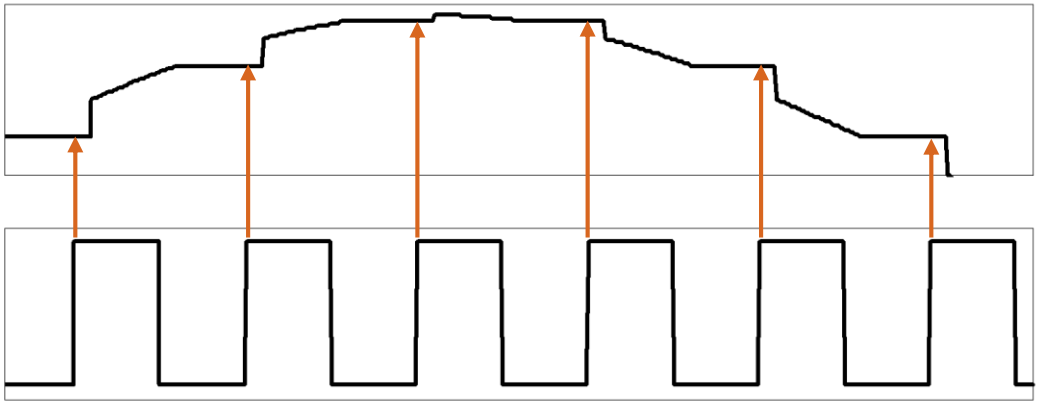
Signal Nomenclature

Continuous Time Signal

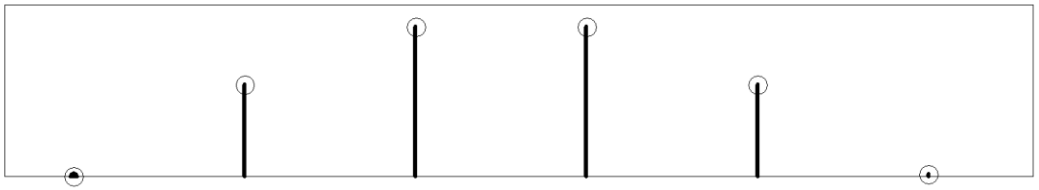


T/H Signal
("Sampled Data Signal")

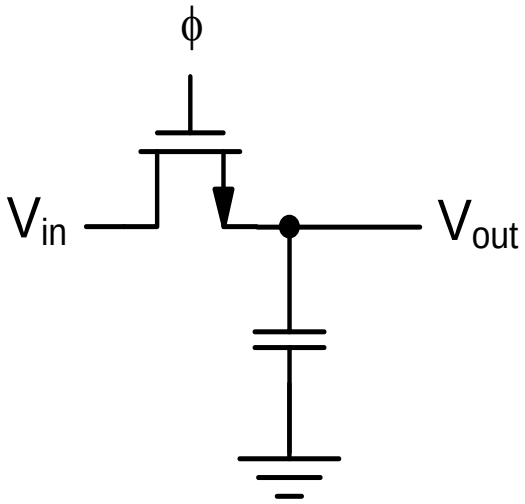
Clock

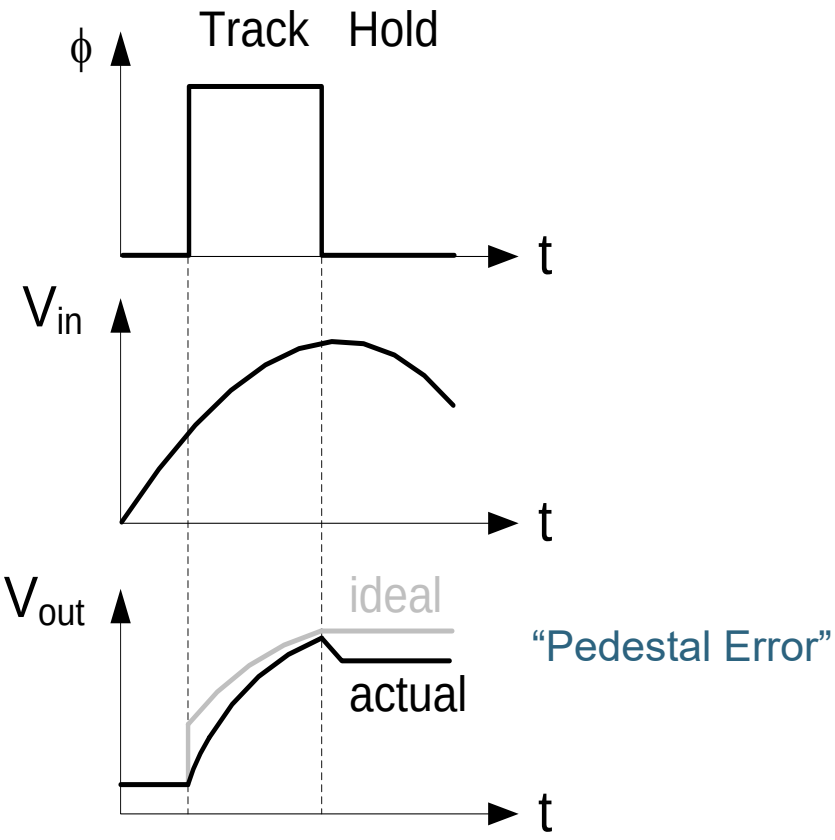


Discrete Time Signal



Circuit with MOS Switch





"Pedestal Error"

Nonidealities

- Finite acquisition time
- Thermal noise
- Clock jitter
- Signal dependent hold instant
- Tracking nonlinearity
- Hold mode feedthrough and leakage
- Charge injection and clock feedthrough

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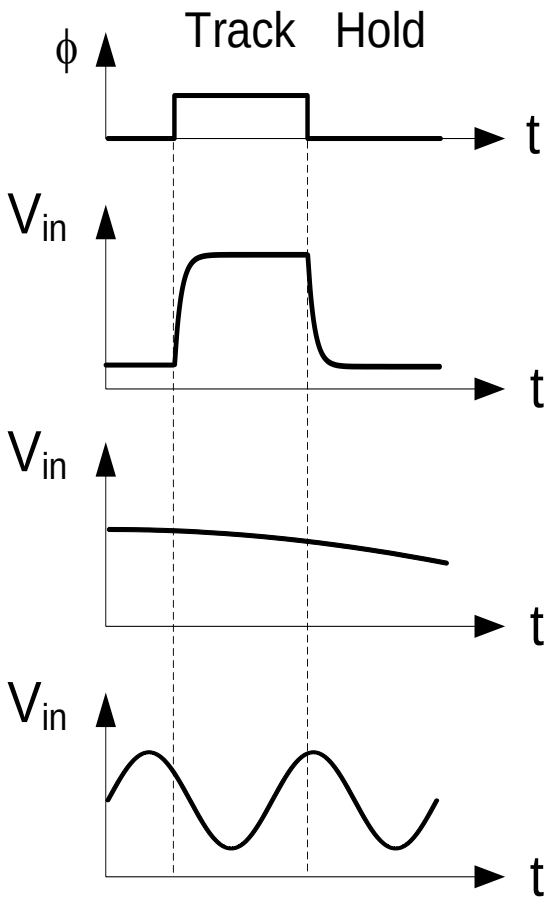
Track & Hold Amplifier
Acquisition Time

Finite Acquisition Time

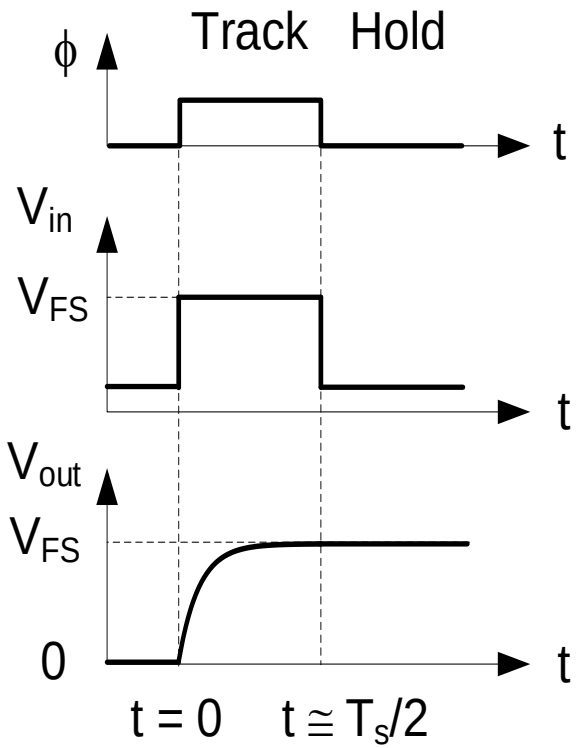


- Consider various input signal scenarios

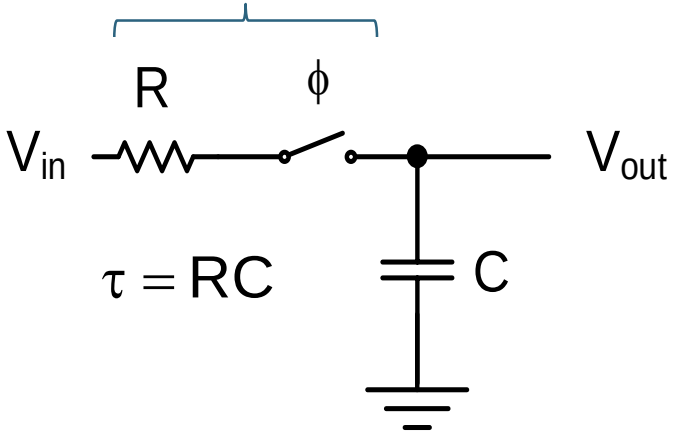
1. Input is a sampled data signal, i.e. the output of another switched capacitor stage
2. Input is a slowly varying continuous time signal, e.g. the input of an oversampling ADC
3. Input is a rapidly varying continuous time signal, e.g. the input of a Nyquist or sub-sampling ADC

Finite Acquisition Time – Case 1

- For simplicity, neglect finite rise time of the input signal
- Consider worst case – the output is required to settle from 0 to the full-scale voltage of the system (V_{FS})



First order MOS switch model



$$\Rightarrow V_{\text{out}}(t) = V_{\text{FS}}\left(1 - e^{-t/\tau}\right)$$

Finite Acquisition Time – Case 1

$$V_{\text{out,err}}\left(\frac{T_s}{2}\right) = -V_{\text{FS}}e^{-\frac{T_s}{2}/\tau} = -V_{\text{FS}}e^{-N}$$

- Typically think about settling error in terms of the number of settling time constants (N) required for ½ LSB settling in a B-bit system

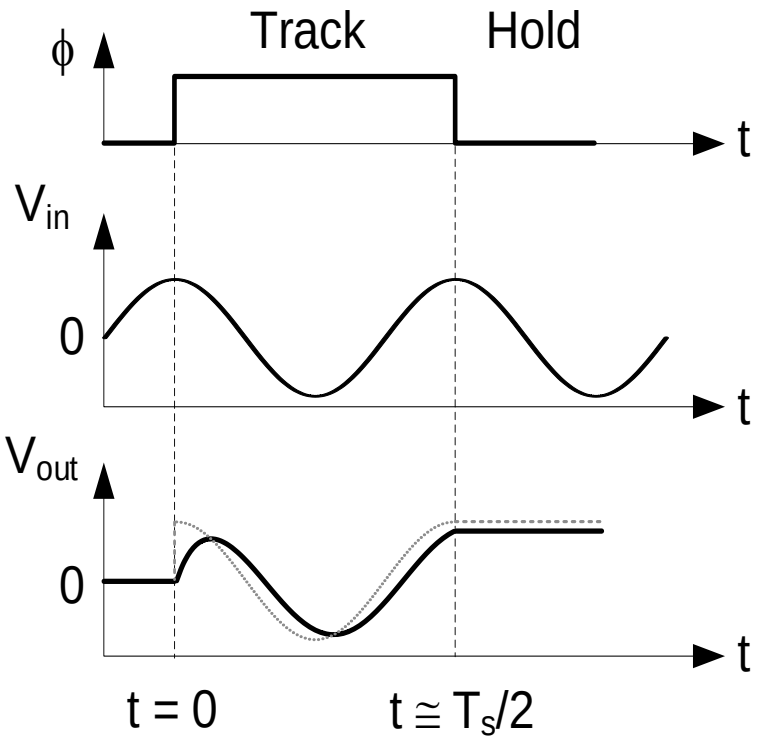
$$\left|-V_{\text{FS}}e^{-N}\right| \leq \frac{1}{2}\frac{V_{\text{FS}}}{2^B}$$

$$N = \frac{T_s/2}{\tau} \geq \ln\left(2 \cdot 2^B\right)$$

B	N
6	>4.9
10	>7.6
14	>10.4
18	>13.2

Finite Acquisition Time – Case 2 & 3

- Consider a sinusoidal input around "0", and "0" also as the initial condition for V_{out} (for notational simplicity)



$$V_{\text{in}}(t) = A\cos(\omega t + \phi)$$

$$V_{\text{out}}(t) = \underbrace{-\frac{A\cos(\phi - \theta)}{\sqrt{1+\omega^2\tau^2}}e^{-\frac{t}{\tau}}}_{\text{initial transient}} + \underbrace{\frac{A\cos(\omega t + \phi - \theta)}{\sqrt{1+\omega^2\tau^2}}}_{\text{steady-state response}}$$

$$\theta = \text{atan}(\omega\tau)$$

Finite Acquisition Time – Case 2 & 3

- At $t=T_s/2$, the error in the held signal consists of two parts
- Residual error due to initial exponentially decaying initial transient term
  - In order to minimize this error, we need to chose N appropriately, as calculated for the step input scenario
- Error due to magnitude attenuation and phase shift in the steady state term
  - This error depends only on the RC time constant and the input frequency; it cannot be reduced by extending the length of the track phase
  - How significant is the error due to the steady-state term?

Finite Acquisition Time – Case 2 & 3

- As an example, let's compute the percent amplitude error for the N values derived previously (½ LSB, B-bit settling to a step)

$$A_{\text{err}} = \left| \frac{\frac{A}{\sqrt{1+(\omega\tau)^2}} - A}{A} \right| = 1 - \frac{1}{\sqrt{1+(\omega\tau)^2}} = 1 - \frac{1}{\sqrt{1+\left(2\pi f_{\text{in}} \frac{T_s/2}{N}\right)^2}} = 1 - \frac{1}{\sqrt{1+\left(\frac{\pi}{N}\frac{f_{\text{in}}}{f_s}\right)^2}}$$

B	N	A_{err} ($f_{\text{in}} = f_s/20$)	A_{err} ($f_{\text{in}} = f_s/2$)
6	4.9	0.052%	4.9%
10	7.6	0.021%	2.1%
14	10.4	0.011%	1.1%
18	13.2	0.007%	0.7%

Summary – Finite Acquisition Time

- Precise settling to an input step is accomplished within 5…13 RC time constants (depending on precision)
- Precise tracking of a high-frequency continuous time input signal tends to impose more stringent requirements
  - Number to remember: ~1% attenuation error at Nyquist ($f_{in}=f_s/2$) for N ~10
- In applications where attenuation is tolerable, the RC time constant requirements then tend to follow from the distortion specs
  - The larger the attenuation, the larger the instantaneous voltage drop across the (weakly nonlinear) MOSFET → undesired harmonics

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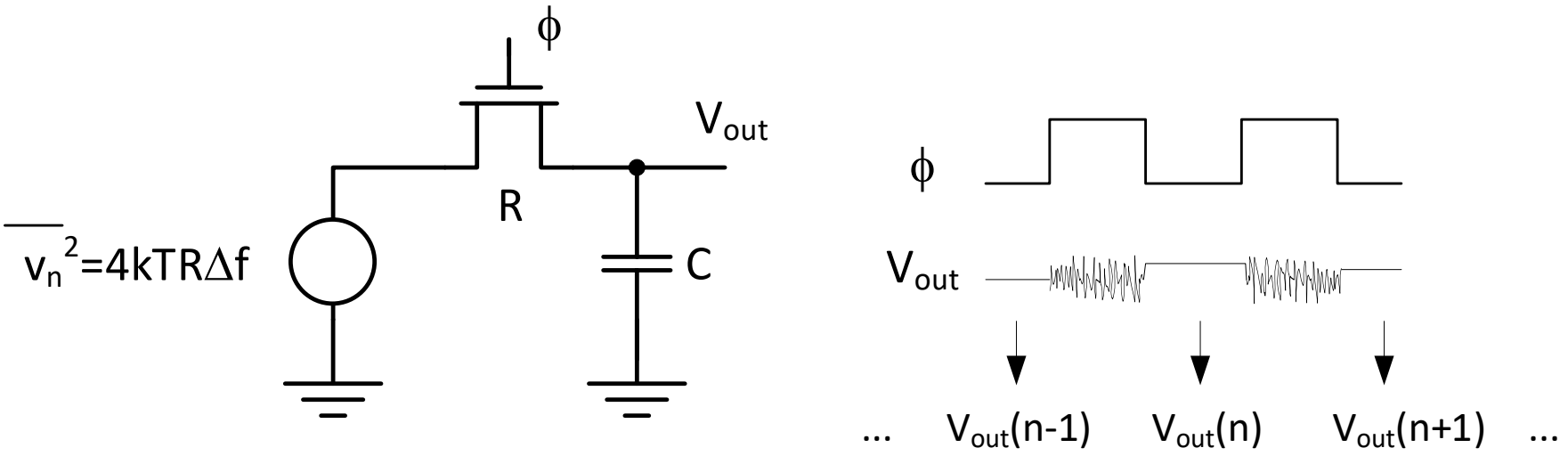
Track & Hold Amplifier – Noise

Thermal Noise (1)



- Questions
  - What is the noise variance of the Vout samples in hold mode?
  - What is the spectrum of the discrete time sequence representing these samples?
    - Nearly white, provided that the number of settling time constants (N) is large

Thermal Noise (2)

- Sample values Vout(n) correspond to instantaneous values of the track mode noise process
- From Parseval's theorem, we know that the time domain power (or variance) of this process is equal to its power spectral density integrated over all frequencies
  - Further, given that the process is ergodic, this number must also be equal to the "ensemble" variance, i.e. the variance of a sample taken at a particular time

$$\frac{\overline{v_{out}^2}}{\Delta f} = 4kTR \cdot \left| \frac{1}{1+sRC} \right|^2$$

$$\text{var}[V_{\text{out}}(n)] = \overline{v_{\text{out,tot}}^2} = \int_0^\infty 4kTR \cdot \left| \frac{1}{1+j2\pi f \cdot RC} \right|^2 df = \frac{kT}{C}$$

Alternative Derivation

- The equipartition theorem says that each “degree of freedom" (typically a quadratic energy variable) of a system in thermal equilibrium holds an average energy of kT/2
- In our system, the degree of freedom is the energy stored on the capacitor

$$\overline{\frac{1}{2}Cv_{\text{out}}{}^2} = \frac{1}{2}kT$$

$$\overline{v_{\text{out}}{}^2} = \frac{kT}{C}$$

Implications of kT/C Noise

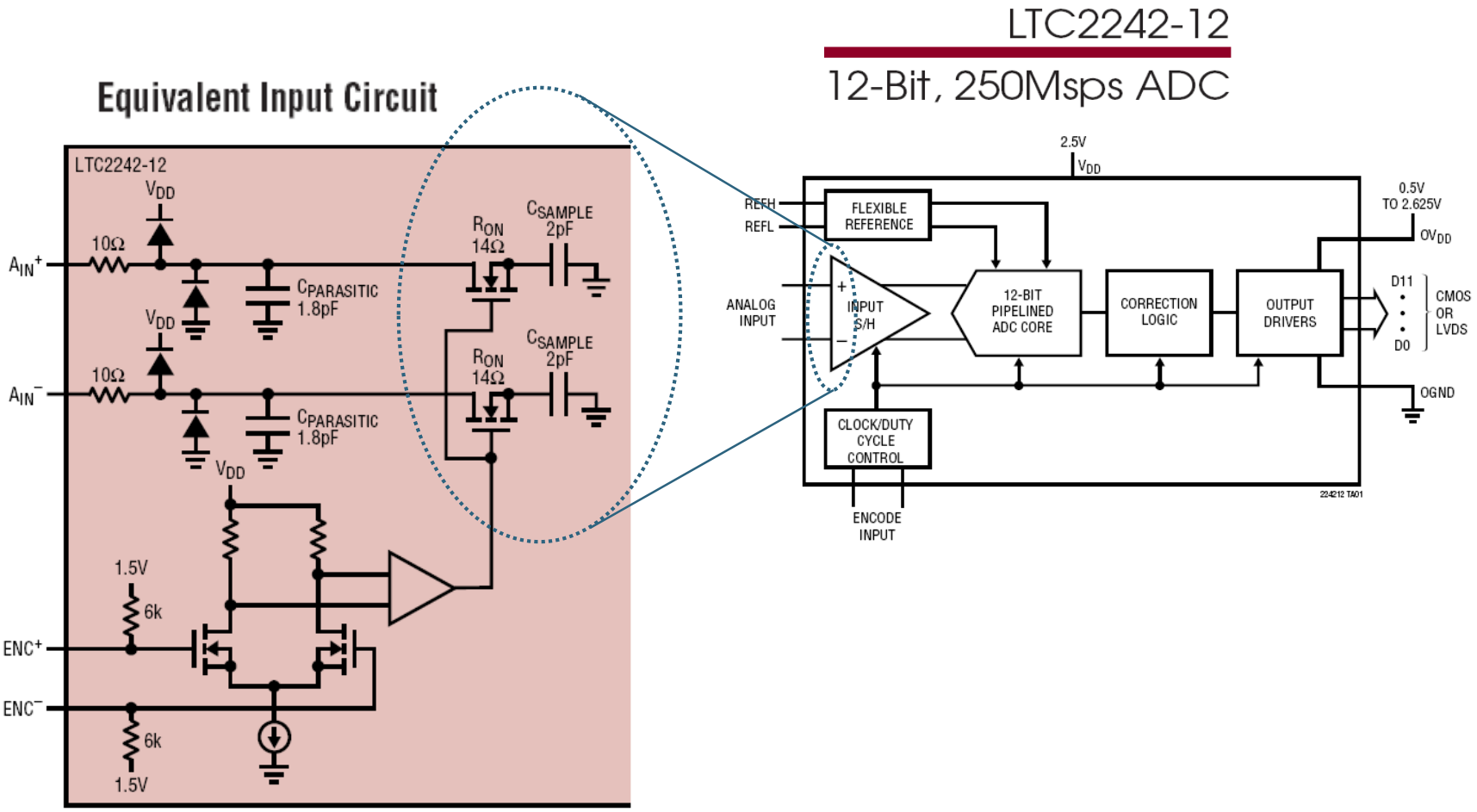
- Example: suppose we make the kT/C noise equal to the quantization noise of a B-bit ADC

$$\frac{kT}{C} = \frac{\Delta^2}{12}, \quad \Delta = \frac{V_{\text{FS}}}{2^B} \Rightarrow \quad C = 12kT\left(\frac{2^B}{V_{\text{FS}}}\right)^2$$

- For a given B, both C and R (via N on slide 19) are fully determined
- Example numbers for V_{FS}=1V and f_s=100MHz:

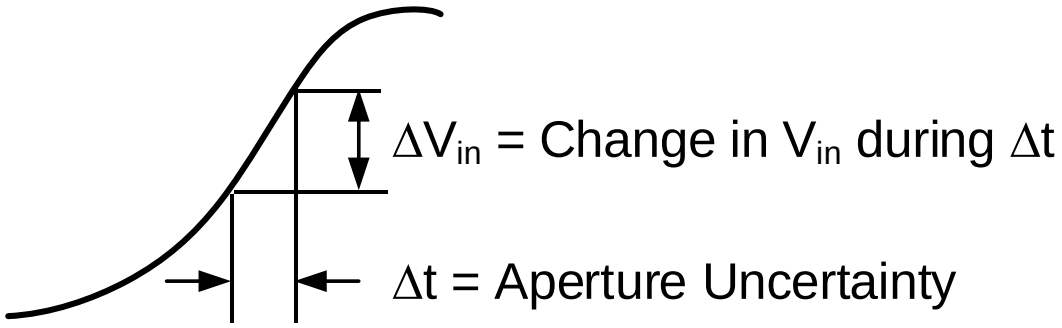
B	C [pF]	R [Ω]
8	0.003	246,057
10	0.052	12,582
12	0.834	665
14	13.3	36
16	213	1.99
18	3,416	0.11

Commercial Example



Aperture Uncertainty

- In any sampling circuit, electronic noise causes random timing variations in the actual sampling clock edge
  - Adds "noise" to samples, especially if dVin/dt is large



$$\Delta V_{\text{in}} \cong \frac{dV_{\text{in}}}{dt} \cdot \Delta t$$

- Analysis
  - Consider sine wave input signal
  - Assume Δt is random with zero mean and standard deviation σ_t

Analysis

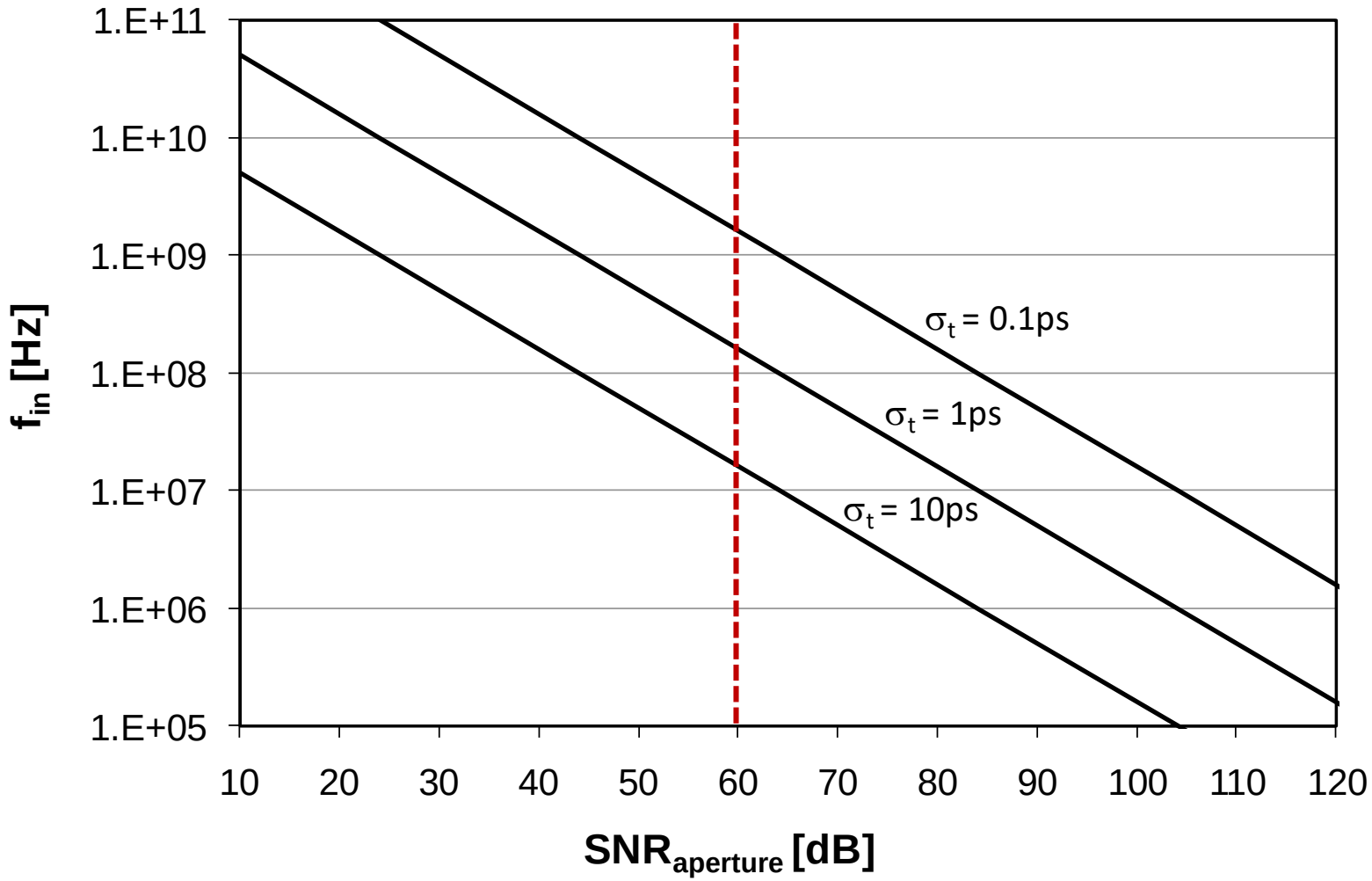
$$E\{\Delta V_{\text{in}}^2\} \cong E\left\{\left(\frac{dV_{\text{in}}}{dt}\right)^2 \cdot \Delta t^2\right\} = E\left\{\left(\frac{dV_{\text{in}}}{dt}\right)^2\right\} \cdot E\{\Delta t^2\}$$

$$\cong E\left\{\left(\frac{d}{dt} A\cos[2\pi \cdot f_{\text{in}} \cdot t]\right)^2\right\} \cdot \sigma_t^2 \cong \frac{1}{2}(2\pi \cdot A \cdot f_{\text{in}})^2 \cdot \sigma_t^2$$

$$SNR_{\text{aperture}}[dB] \cong 10 \cdot \log\left[\frac{\frac{1}{2}A^2}{\frac{1}{2}(2\pi \cdot A \cdot f_{\text{in}} \cdot \sigma_t)^2}\right] = 20 \cdot \log\left[\frac{1}{2\pi \cdot f_{\text{in}} \cdot \sigma_t}\right]$$

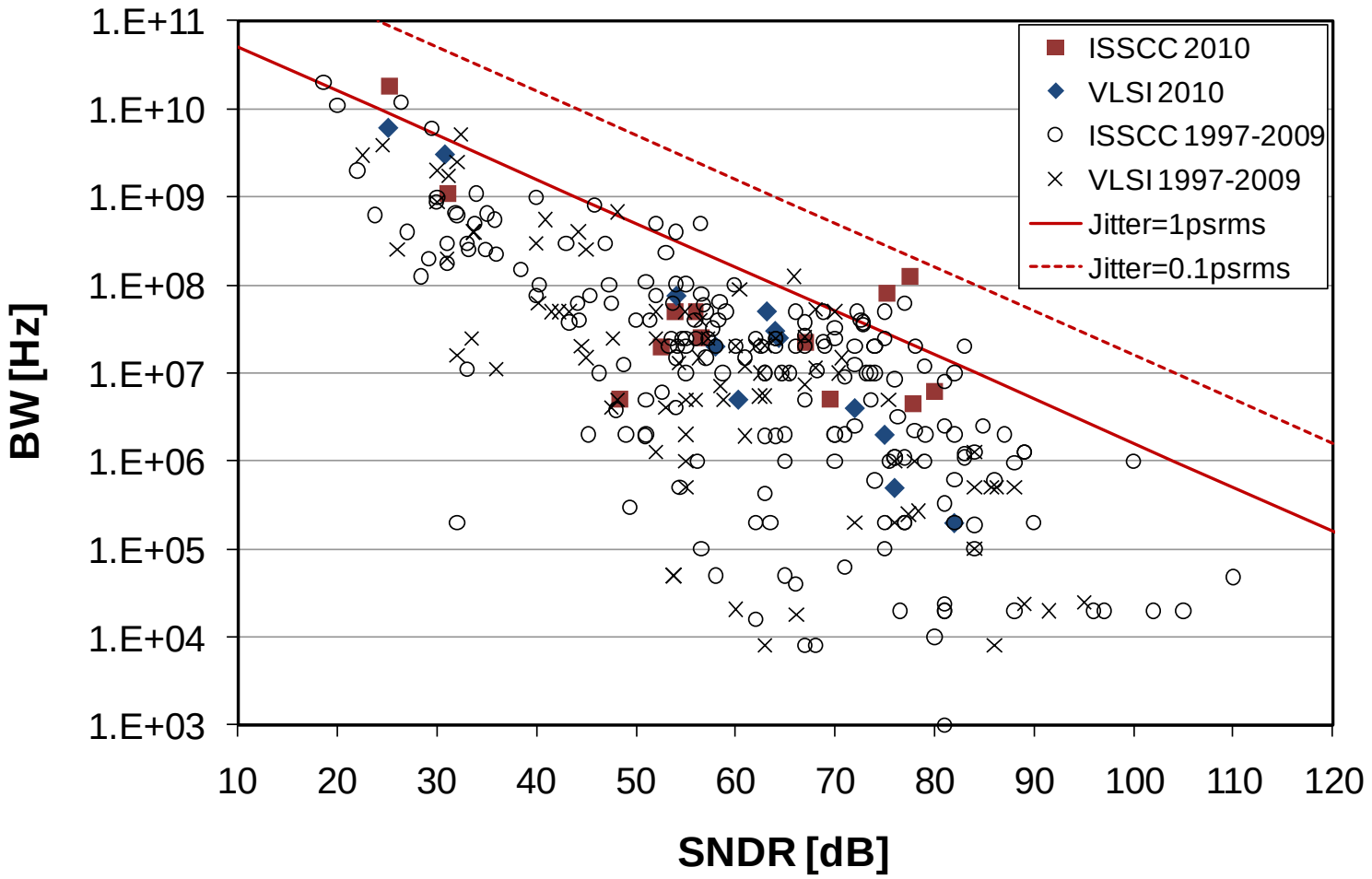
- For an input signal whose power is evenly distributed between 0…fs/2, the above result improves by 4.8 dB
  - See e.g. [Da Dalt, TCAS1, 9/2002]

Result


1.E+11
1.E+10
1.E+09
1.E+08
1.E+07
1.E+06
1.E+05
f_{in} [Hz]
σ_t = 0.1ps
σ_t = 1ps
σ_t = 10ps
10
20
30
40
50
60
70
80
90
100
110
120
$SNR_{aperture}$ [dB]

ADC Performance Survey (ISSCC & VLSI 97-10)

Data: http://www.stanford.edu/~murmann/adcsurvey.html



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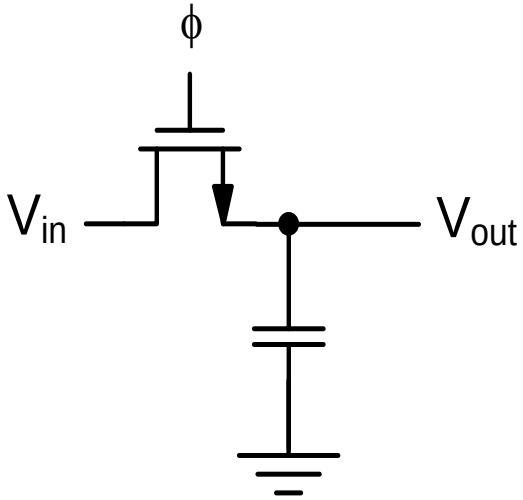
Track & Hold Amplifier – Linearity

Voltage Dependence of Switch

$$I_{D(\text{triode})} = \mu C_{ox} \frac{W}{L}\left(V_{GS} - V_t - \frac{V_{DS}}{2}\right)V_{DS}$$

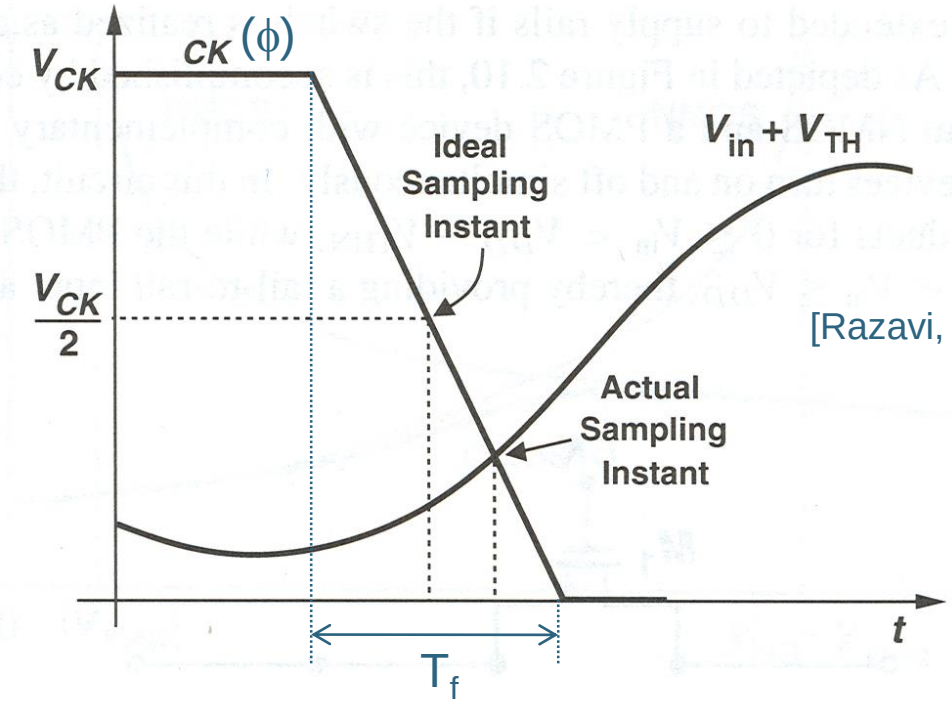
$$R_{ON} \cong \left[\left.\frac{dI_{D(\text{triode})}}{dV_{DS}}\right|_{V_{DS}\to 0}\right]^{-1}$$

$$R_{ON} = \frac{1}{\mu C_{ox}\frac{W}{L}(\phi - V_{\text{in}} - V_t)}$$



- Two problems
  - Transistor turn off is signal dependent, occurs when $\phi = V_{in} + V_t$
  - R_{ON} is modulated by Vin (assuming e.g. f=VDD=const.)

Signal Dependent Sampling Instant (1)



[Razavi, Data Conversion System Design, p.17]

- Must make fall time of sampling clock (T_f) much faster than maximum dV_{in}/dt

Signal Dependent Sampling Instant (2)

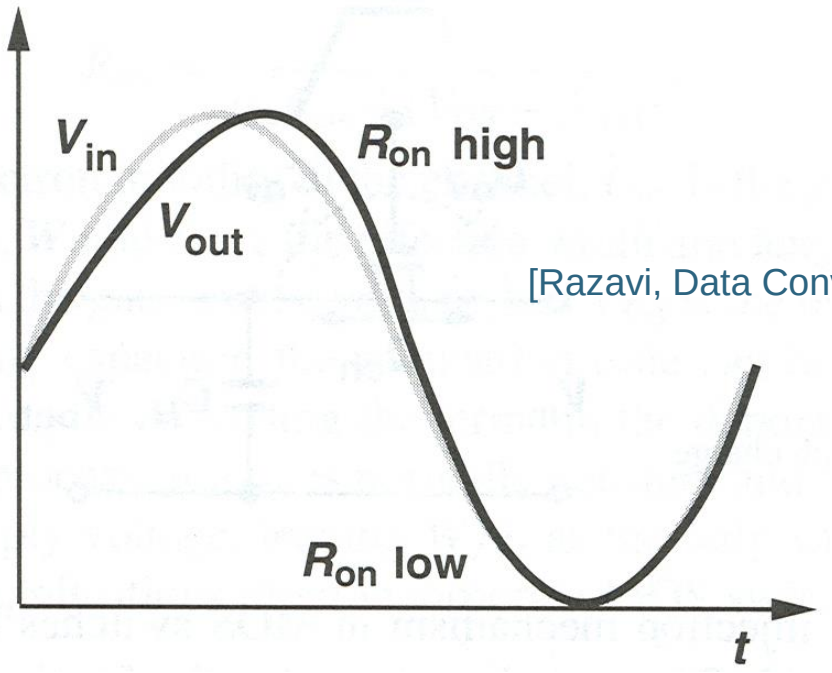
- Distortion analysis result (see Yu, TCAS II, 2/1999]

$$HD_3 = \frac{\text{Amplitude of third harmonic}}{\text{Amplitude of fundamental}} \cong \frac{3}{8}\left(\frac{A}{V_{CK}}\omega T_f\right)^2$$

- Example:
  V_{CK} = 1.8V, A = 0.5V, T_f = 100ps, ω = 2π 100MHz

$$HD_3 \cong \frac{3}{8}\left(\frac{0.5}{1.8}\cdot 2\pi 100\cdot 10^6\cdot 100\cdot 10^{-12}\right)^2 = -79dB$$

Track Mode Nonlinearity



[Razavi, Data Conversion System Design, p.16]

- Output tracks well when input voltage is low
  - Gets distorted when voltage is high due to increase in R_{ON}

Analysis

$$I_D \cong K(V_{GS} - V_t)V_{DS} - \frac{K}{2}V_{DS}^2$$

$$C\frac{dV_{\text{out}}}{dt} = K(\phi - V_{\text{out}} - V_t)(V_{\text{in}} - V_{\text{out}}) - \frac{K}{2}(V_{\text{in}} - V_{\text{out}})^2$$

- "All" we need to do is solve the above differential equation…
- Can use Volterra Series analysis
  - General method that allows us to calculate the frequency domain response of nonlinear circuits with memory
  - See e.g. EE 242B
- Luckily someone has already done this for us
  - See [Yu, TCAS II, 2/1999]

Result

$$HD_3 = \frac{\text{Amplitude of third harmonic}}{\text{Amplitude of fundamental}}$$
$$\cong \frac{1}{4}\left(\frac{A}{V_{GS}-V_t}\right)^2 \cdot \omega\tau = \frac{1}{4}\left(\frac{A}{V_{GS}-V_t}\right)^2 \frac{f_{\text{in}}}{f_s} \cdot \frac{\pi}{N}$$

- V_{GS} is the "quiescent point" value of the gate-source voltage; i.e. in the zero crossing of the sine input
- For low distortion
  - Make amplitude smaller than $V_{GS}-V_t$
    - Low swing → bad for SNR
  - Make $1/\tau$ much larger than ω (input frequency)
    - Big switch → may cost lots of power to drive, comes with large parasitic capacitances

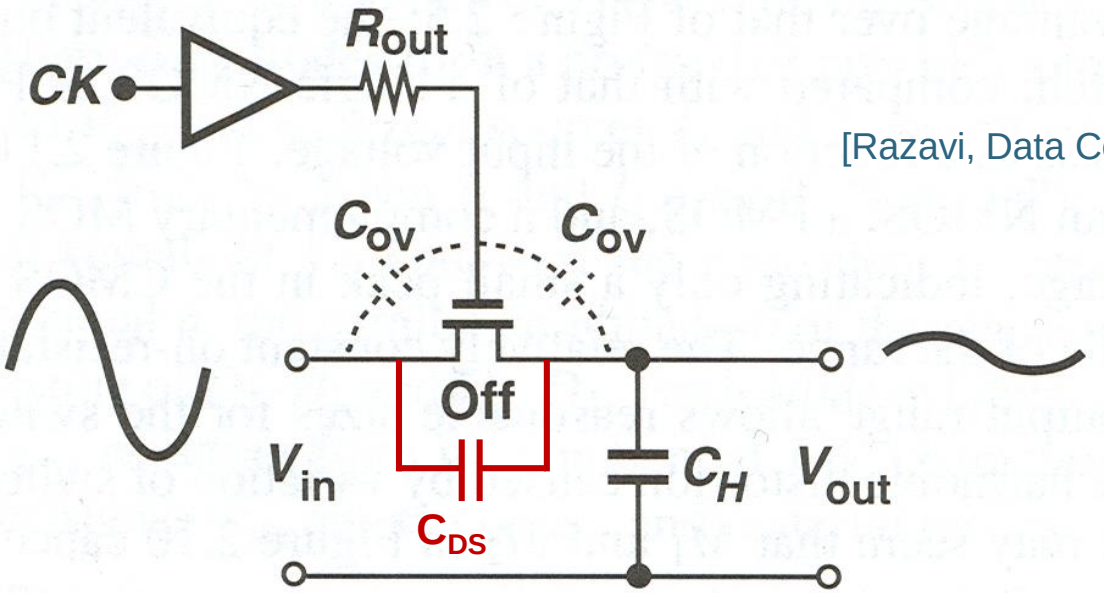
Numerical Example

- Parameters
  - $V_{DD} = V_{CK} = 1.8V$
  - Signal is centered about $V_{DD}/2 = 0.9V$
  - $V_{GS}-V_t = 1.8V-0.9V-0.45V = 0.45V$
  - $A = 0.2V$
  - $N = 0.5T_s/\tau = 10$
  - $f_{in} = f_s/2$

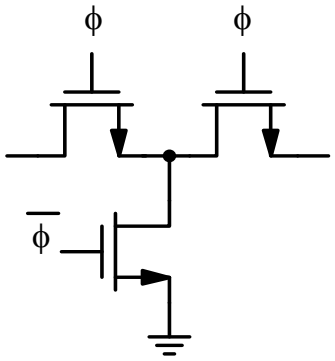
$$HD_3 \cong \frac{1}{4}\left(\frac{0.2}{0.45}\right)^2 \frac{1}{2} \cdot \frac{\pi}{10} = -42dB$$

- Not all that great…

Hold Mode Feedthrough



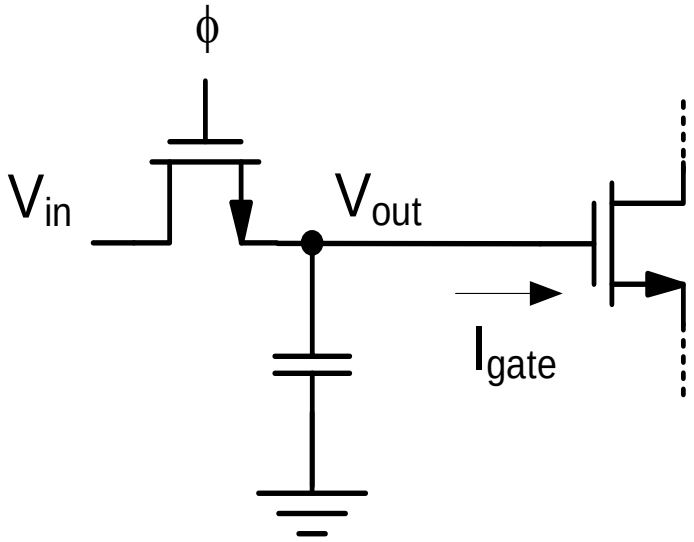
[Razavi, Data Conversion System Design, p.17]

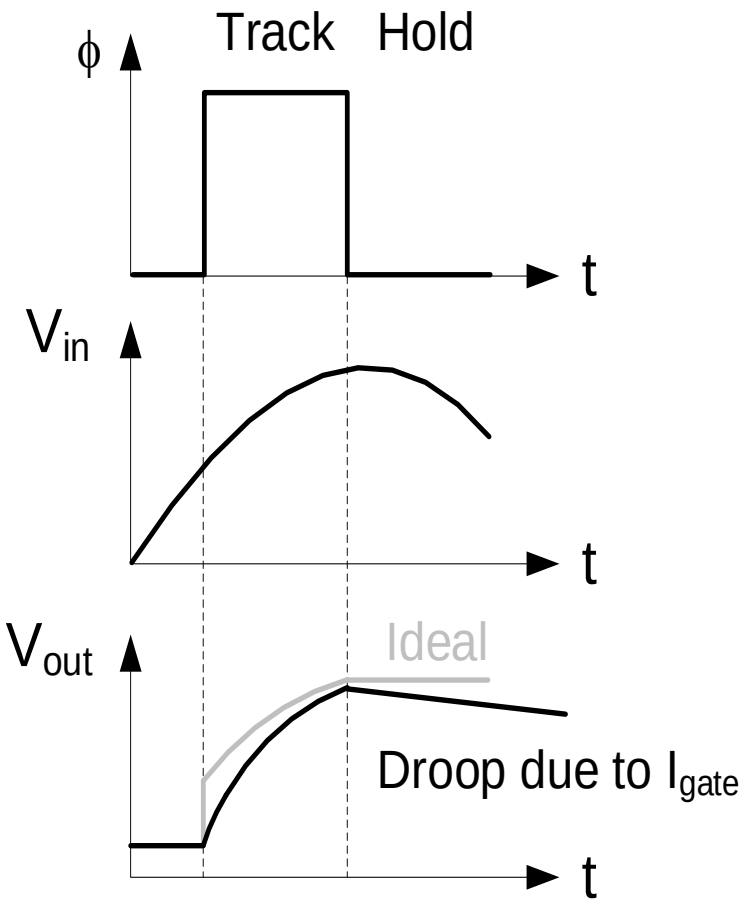


- Want to make R_{out} as small as possible
- Consider using a "T-switch" when hold-mode feedthrough is a problem

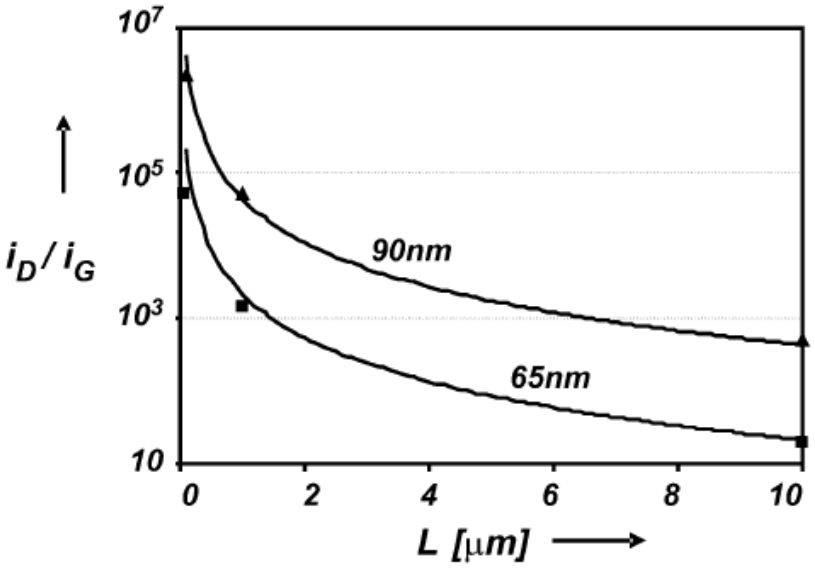
Hold Mode Leakage

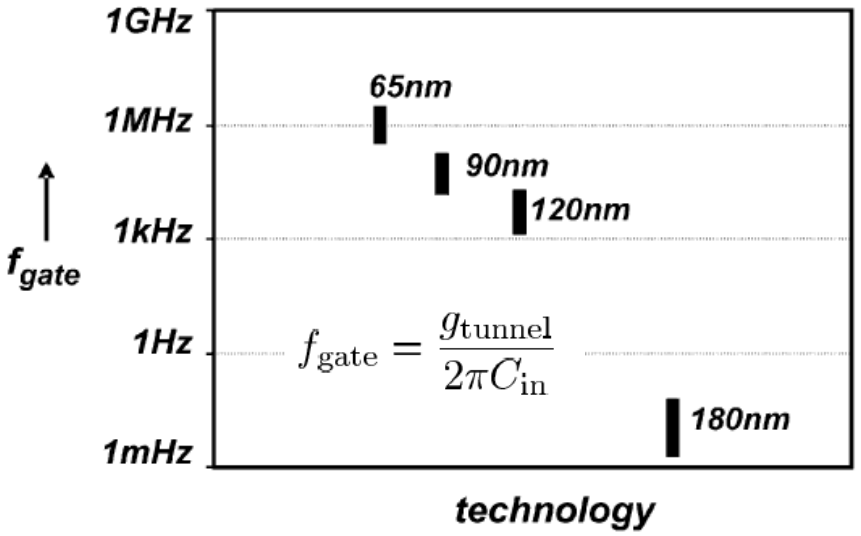
- Example:





Gate Leakage Data





A. Annema, et al., "Analog circuits in ultra-deep-submicron CMOS," *IEEE J. Solid-State Circuits,* pp. 132-143, Jan. 2005.

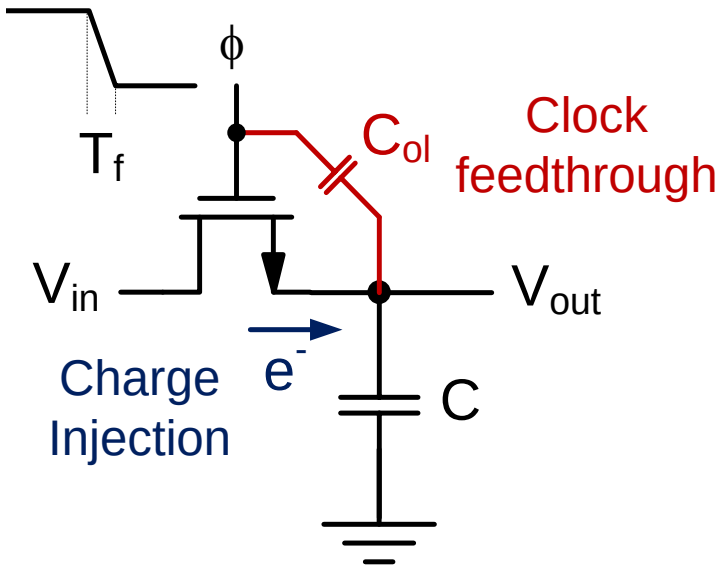
$$\frac{dv_C}{dt} \approx -\gamma_{dv\,dt} \cdot f_{\text{gate}} \left[\frac{V}{s}\right] \quad \text{with } \gamma_{dv\,dt} \approx 1\text{ V}.$$

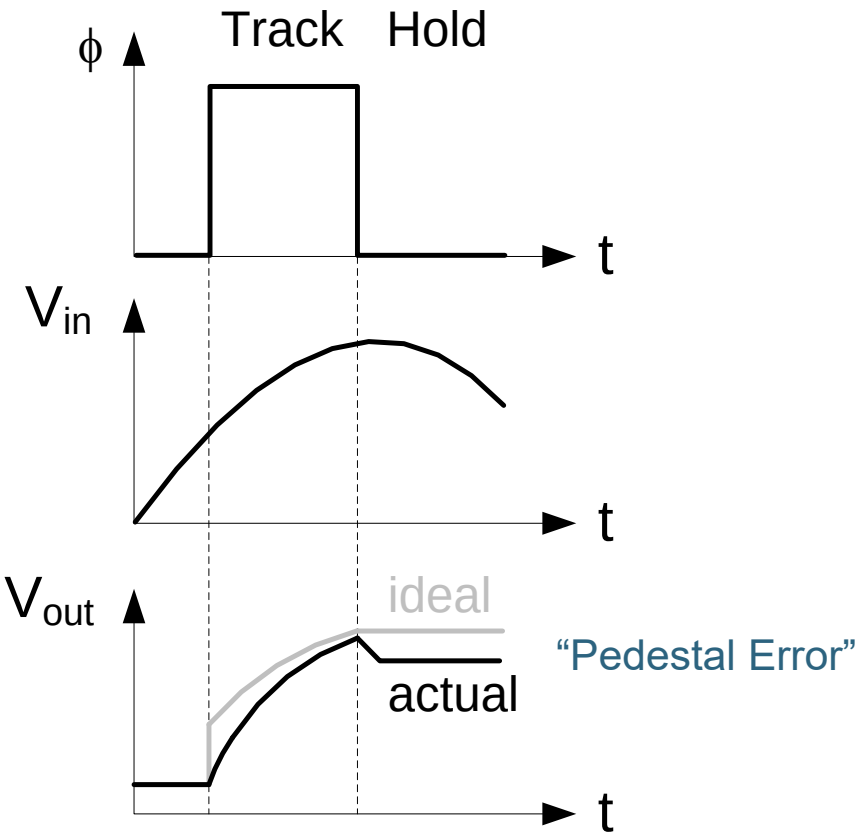
- In 65nm CMOS, gate capacitance droop rate is ~1V/ms (!)
- Issue is solved with high-k dielectrics in post-65nm technologies

EE 240C
Analog-Digital Interface Integrated Circuits

Track & Hold Amplifier
Switch Charge Injection

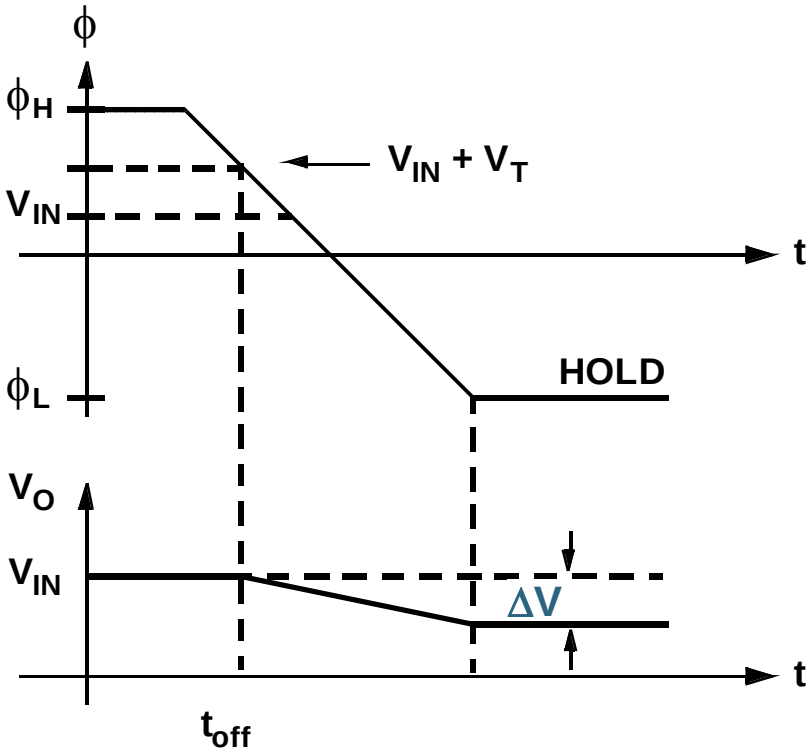
Charge Injection and Clock Feedthrough





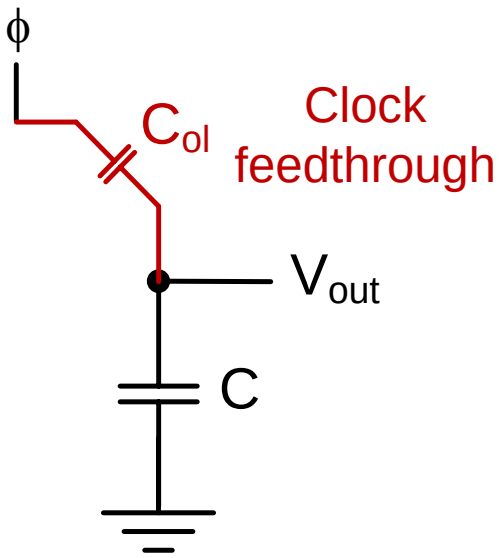
- Analyze two extreme cases
  - Very large T_f ("slow gating")
  - Very small T_f ("fast gating")

Slow Gating



- All channel charge has disappeared by t_{off} without introducing error; it is absorbed by the input source

Slow Gating Model for $t > t_{off}$



$$V_{out} = V_{in} - \Delta V_{out}$$

$$V_{out} = V_{in} - \frac{C_{ol}}{C_{ol} + C}\left(V_{in} + V_t - \phi_L\right) = V_{in}\left(1+\varepsilon\right) + V_{os}$$

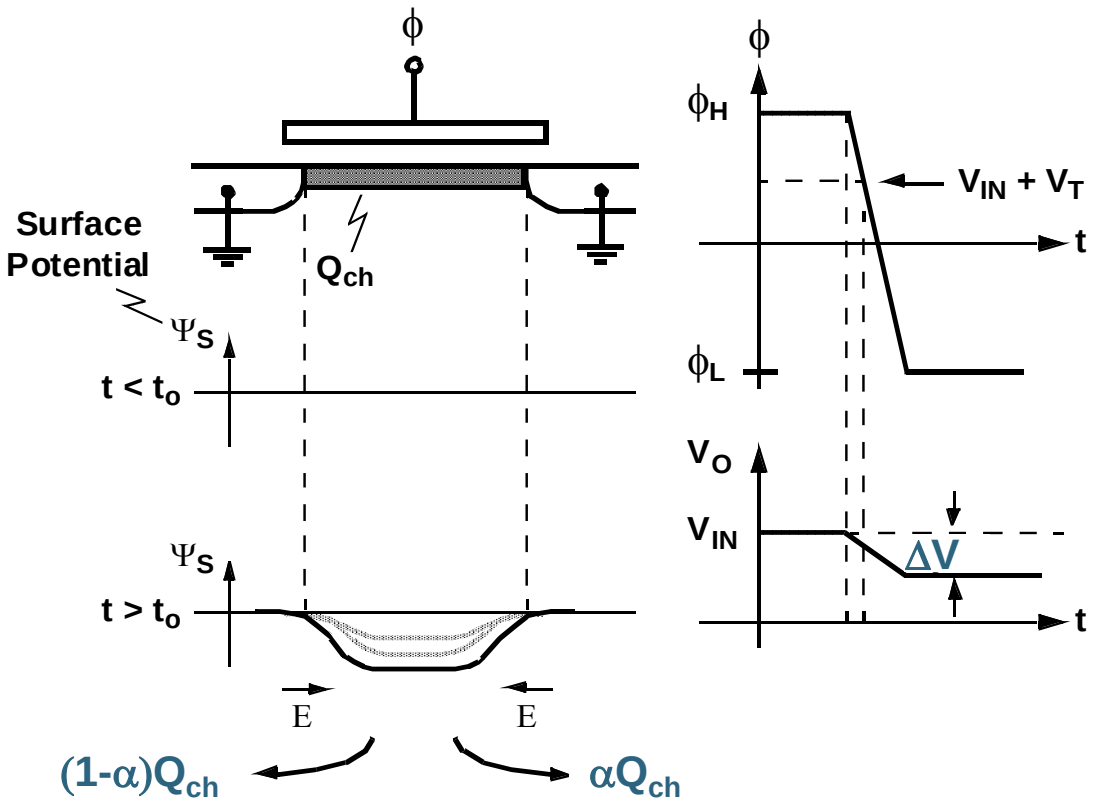
$$\varepsilon = -\frac{C_{ol}}{C_{ol} + C} \qquad V_{os} = -\frac{C_{ol}}{C_{ol} + C}\left(V_t - \phi_L\right)$$

Gain Error Offset Error

- Example: C=1pF, ϕ_L=0V, V_t=0.45V, W=20μm, C_{ol}'=0.1fF/μm, C_{ol}=2fF

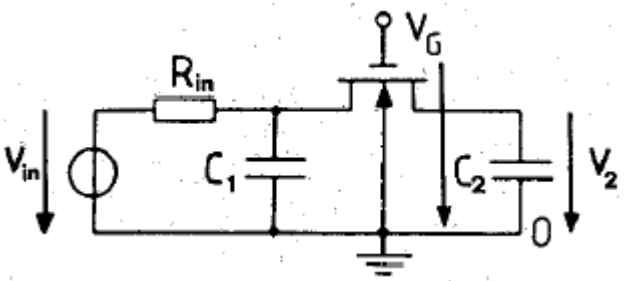
$$\varepsilon = -0.2\% \qquad V_{os} = -0.9\text{mV}$$

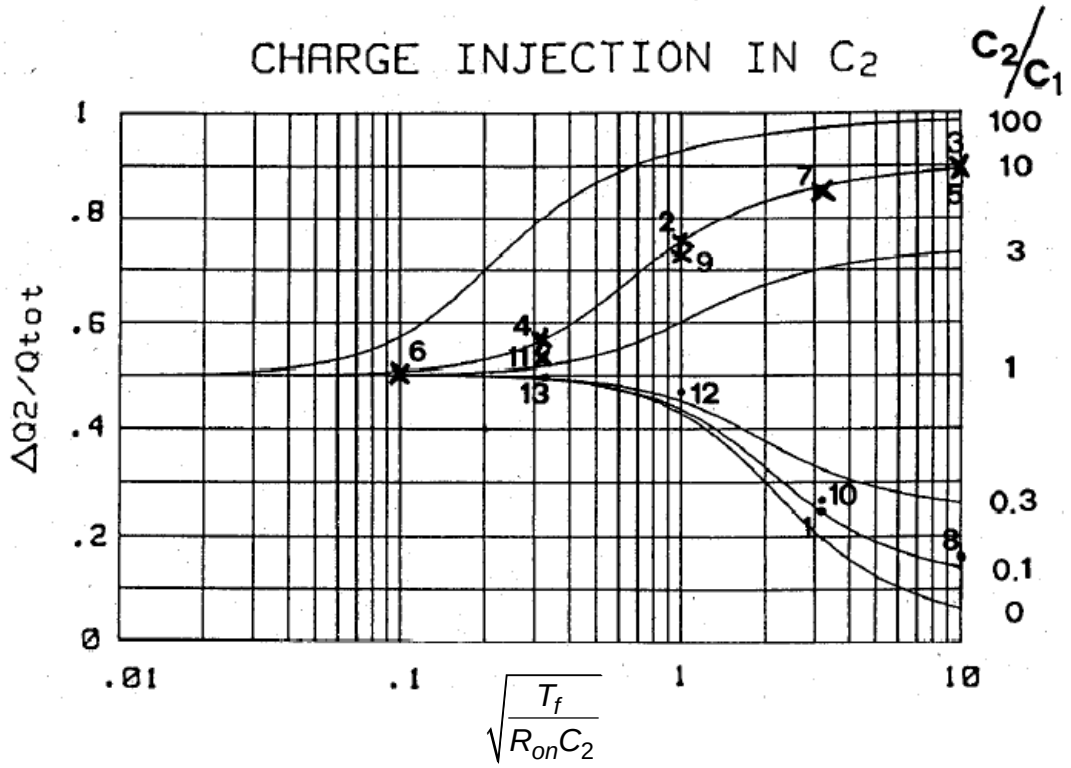
Fast Gating



- Channel charge cannot change instantaneously
- Resulting surface potential decays via charge flow to source and drain
- Charge divides between source and drain depending on impedances loading these nodes

Charge Split Ratio Data





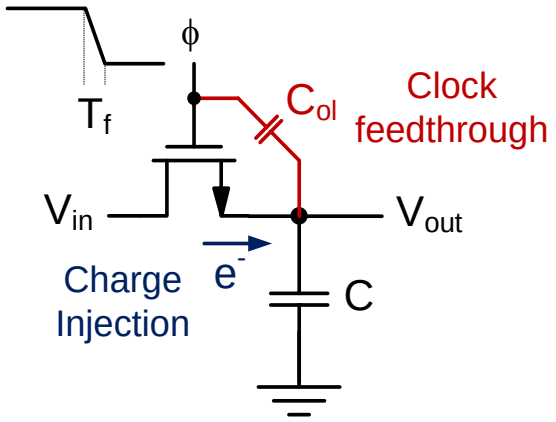
G. Wegmann et al., "Charge injection in analog MOS switches," IEEE J. Solid-State Circuits, pp. 1091-1097, June 1987.

Y. Ding and R. Harjani, "A universal analytic charge injection model," Proc. ISCAS, pp. 144-147, May 2000.

Interpretation

- $R_{on}C_2$ and T_f are usually comparable, or at least not more than an order of magnitude apart
  - This brings us into the range of 0.1…1 on the chart by Wegmann
- This means that the charge split will in practice have some dependence on the impedances seen on the two sides of the transistor
- Remember: Slightly more charge will go to the side with lower impedance

Fast Gating Model for $t > t_{off}$



$$V_{out} = V_{in} - \Delta V_{out} = V_{in}(1+\varepsilon) + V_{os}$$

$$V_{out} = V_{in} - \frac{C_{ol}}{C_{ol}+C}(\phi_H - \phi_L) + \frac{1}{2}\frac{Q_{ch}}{C}$$

Assuming 50/50 charge split

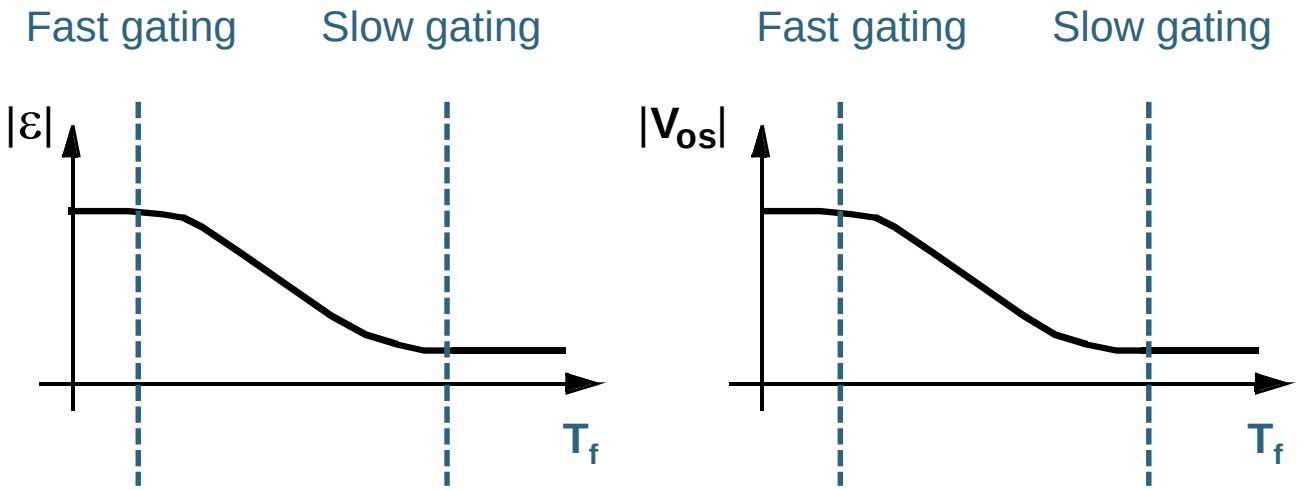
$$Q_{ch} = -WLC_{ox}[\phi_H - V_{in} - V_t]$$

$$\varepsilon = \frac{1}{2}\frac{WLC_{ox}}{C} \qquad V_{os} = -\frac{C_{ol}}{C_{ol}+C}(\phi_H - \phi_L) - \frac{1}{2}\frac{WLC_{ox}}{C}(\phi_H - V_t)$$

- Example: C=1pF, ϕ_H-ϕ_L=1.8V, V_t=0.45V, W=20μm, LC_{ox}=2fF/μm C_{ol}'=0.1fF/μm, C_{ol}=2fF

$$\varepsilon = +2\% \qquad V_{os} = -30.6mV$$

Transition Fast/Slow Gating



- $|\varepsilon|$ and $|V_{os}|$ decrease as the fall time of ϕ (T_f) increases and approach the limit case of slow gating
- Unfortunately, high-speed switched capacitor circuits tend to operate in fast gating regime

Impact of Technology Scaling

$$\Delta V \cong \frac{1}{2}\frac{Q_{ch}}{C} \qquad \frac{1}{2f_s} = \frac{T_s}{2} = N \cdot RC$$

$$R \cong \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_t)} = \frac{L^2}{\mu Q_{ch}}$$

$$\frac{\Delta V}{f_s} \cong N\frac{L^2}{\mu}$$

- Charge injection error to speed ratio benefits from shorter channels and increases in mobility (e.g. due to strain)