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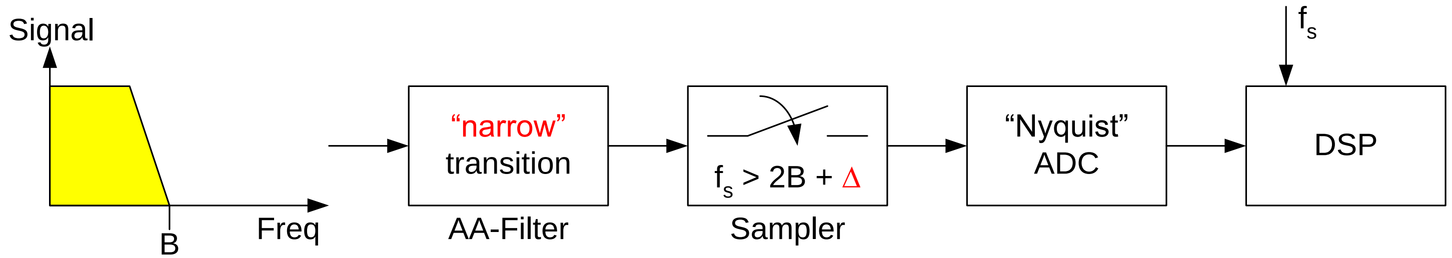
Analog-Digital Interface Integrated Circuits

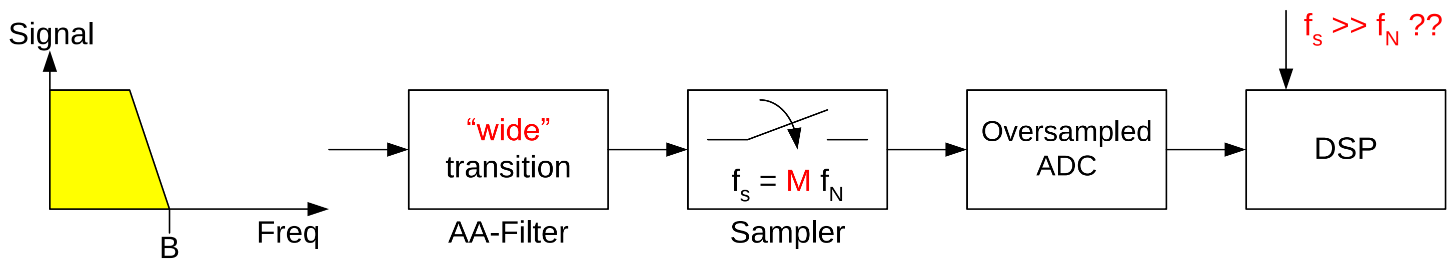
Oversampled ADCs

The Case for Oversampling

Nyquist sampling:

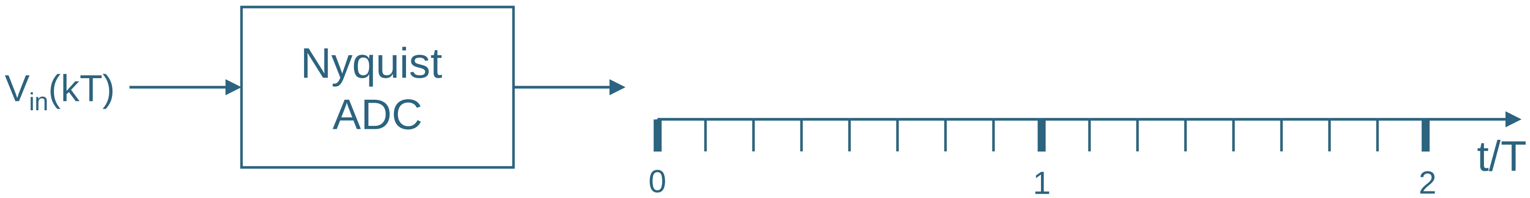


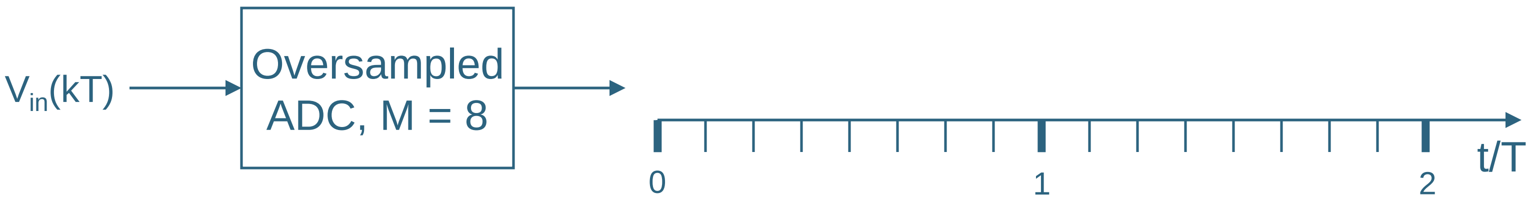
Oversampling:



- Nyquist rate $f_N = 2B$
- Oversampling rate $M = f_s/f_N > 1$

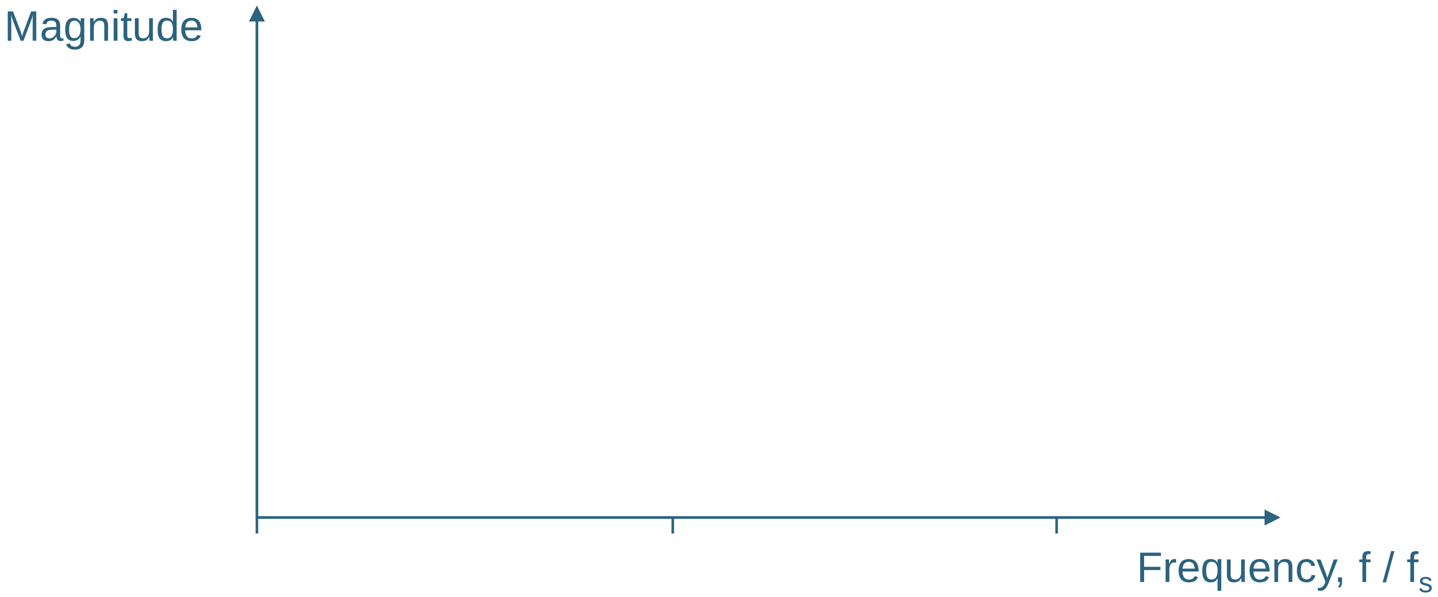
Pulse-Count Modulation





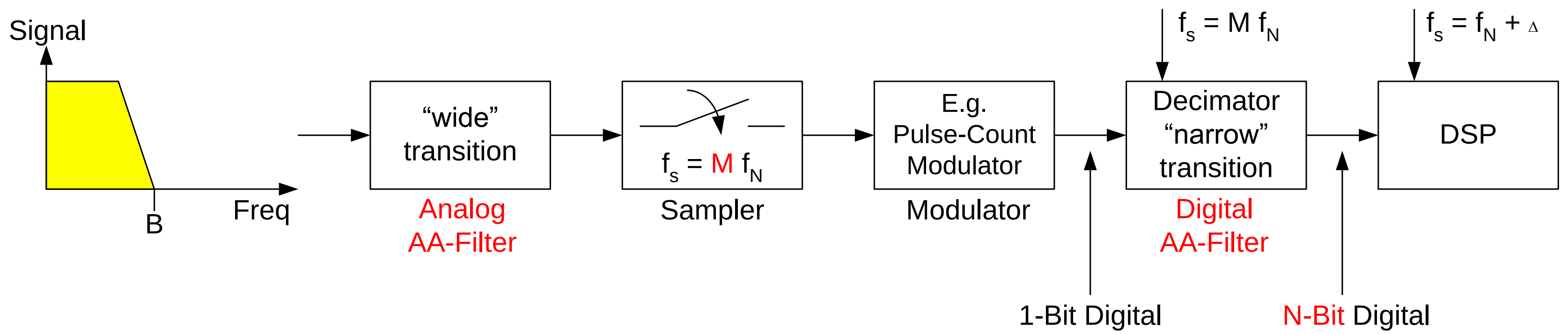
Mean of pulse-count signal approximates analog input!

Pulse-Count Spectrum



- Signal: low frequencies, $f < B << f_s$
- Quantization error: high frequency, $B \ldots f_s / 2$
- Separate with low-pass filter!

Oversampled ADC



Decimator:
- Digital (low-pass) filter
- Removes quantization error for f > B
- Provides most anti-alias filtering
- Narrow transition band, high-order
- 1-Bit input, N-Bit output (essentially computes "average")

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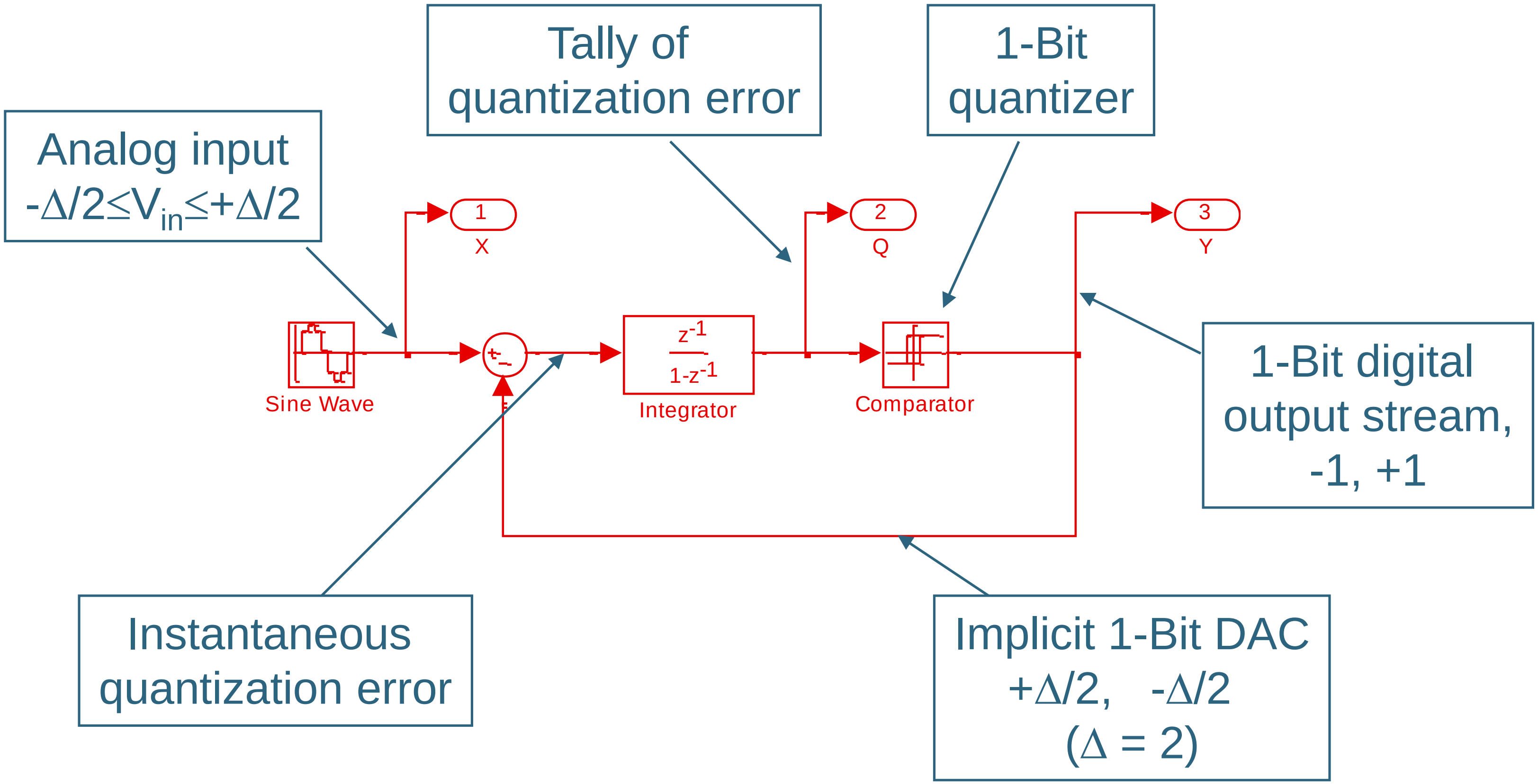
Modulator

Modulator

- Objectives:
  - Convert analog input to 1-Bit pulse density stream
  - Move quantization error to high frequencies f >>B
  - Operates at high frequency $f_s >> f_N$
    - M = 4 … 256 (typical)
    - Better be "simple"

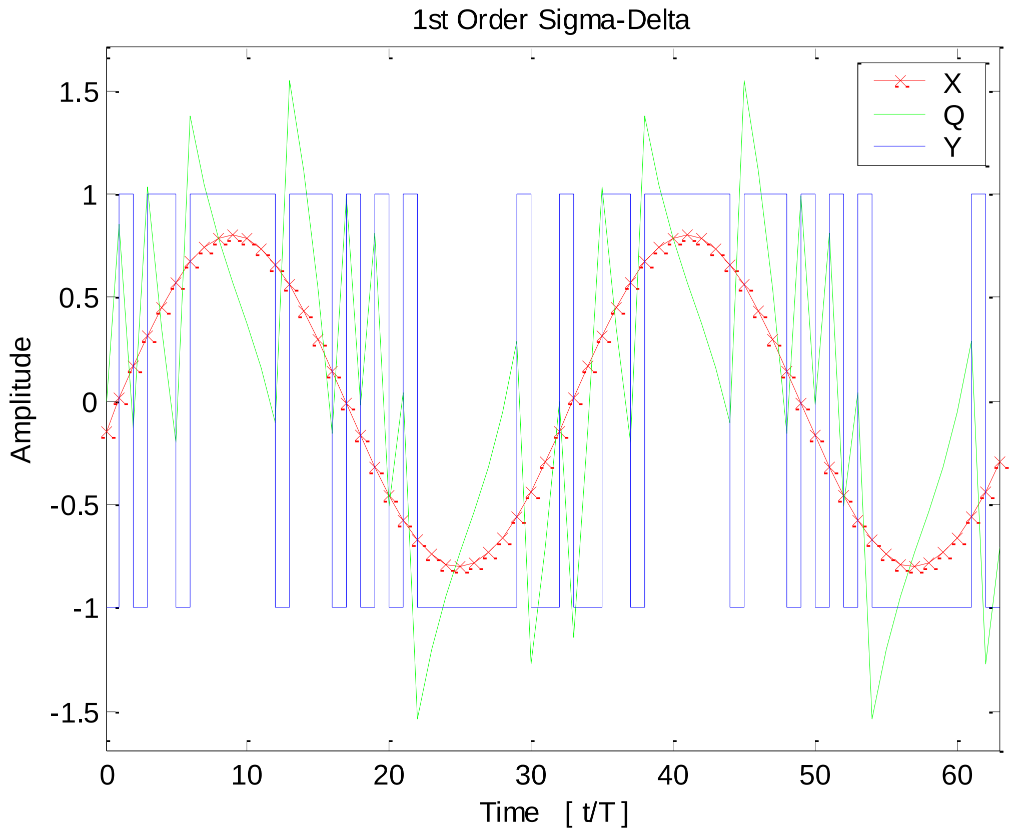
- → $\Sigma\Delta = \Delta\Sigma$ Modulator

1st Order ΣΔ Modulator



sigma_delta_L1.mdl

1^{st} Order Modulator Signals



sigma_delta_L1.m

X analog input
Q tally of q-error
Y digital/DAC output

Mean of Y approximates X

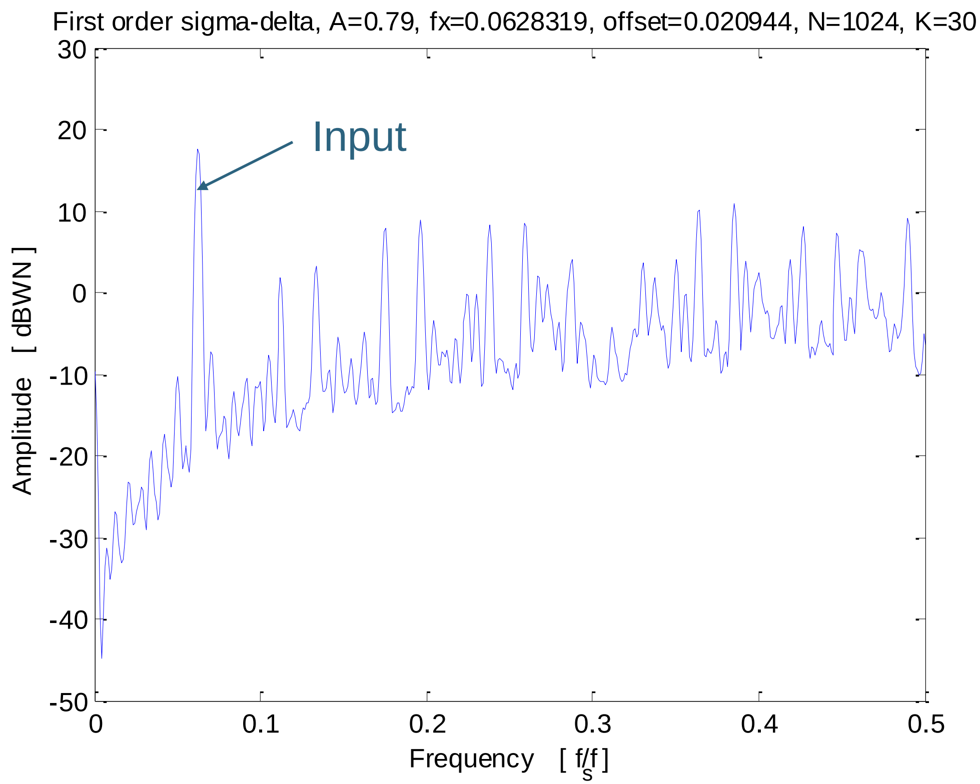
$T = 1/f_s = 1/(M f_N)$

ΣΔ Modulator Characteristics

- Quantization error independent of component matching
- Very high SQNR achievable (> 20 Bits!)
- Inherently linear for 1-Bit DAC
- Limited to "moderate" speed
  (try to build a 10GS/s, 8-Bit oversampled ADC)

- What about the quantization noise spectrum?

Output Spectrum



sigma_delta_L1_sin.m

- Definitely not white!
- Skewed towards higher frequencies
- Tones
- dBWN (dB White Noise) scale sets the 0dB line at the noise per bin of a random -1, +1 sequence

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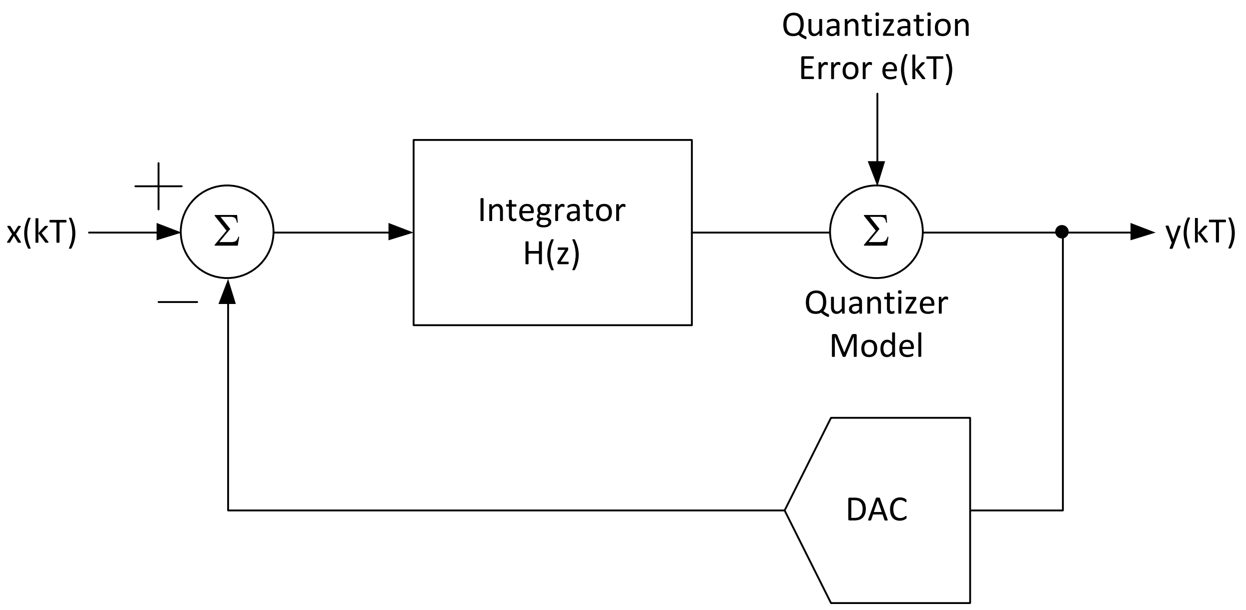
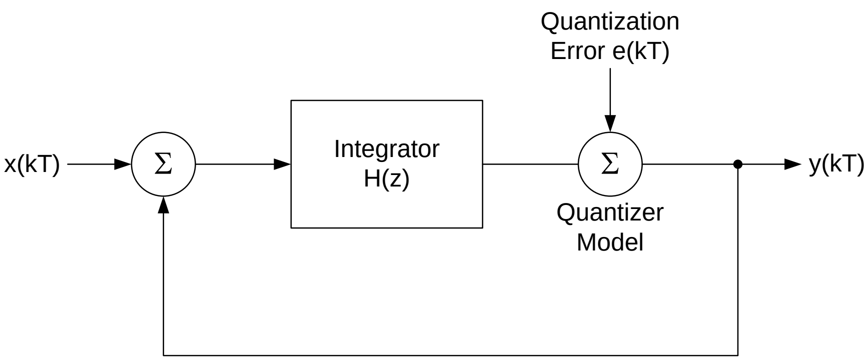
Quantization Noise Analysis

Quantization Noise Analysis



- Sigma-Delta modulators are nonlinear systems with memory → very difficult to analyze
- Representing the quantizer as an additive noise source linearizes the system

STF and NTF



$$\mathrm{H}(z) = \frac{z^{-1}}{1 - z^{-1}}$$

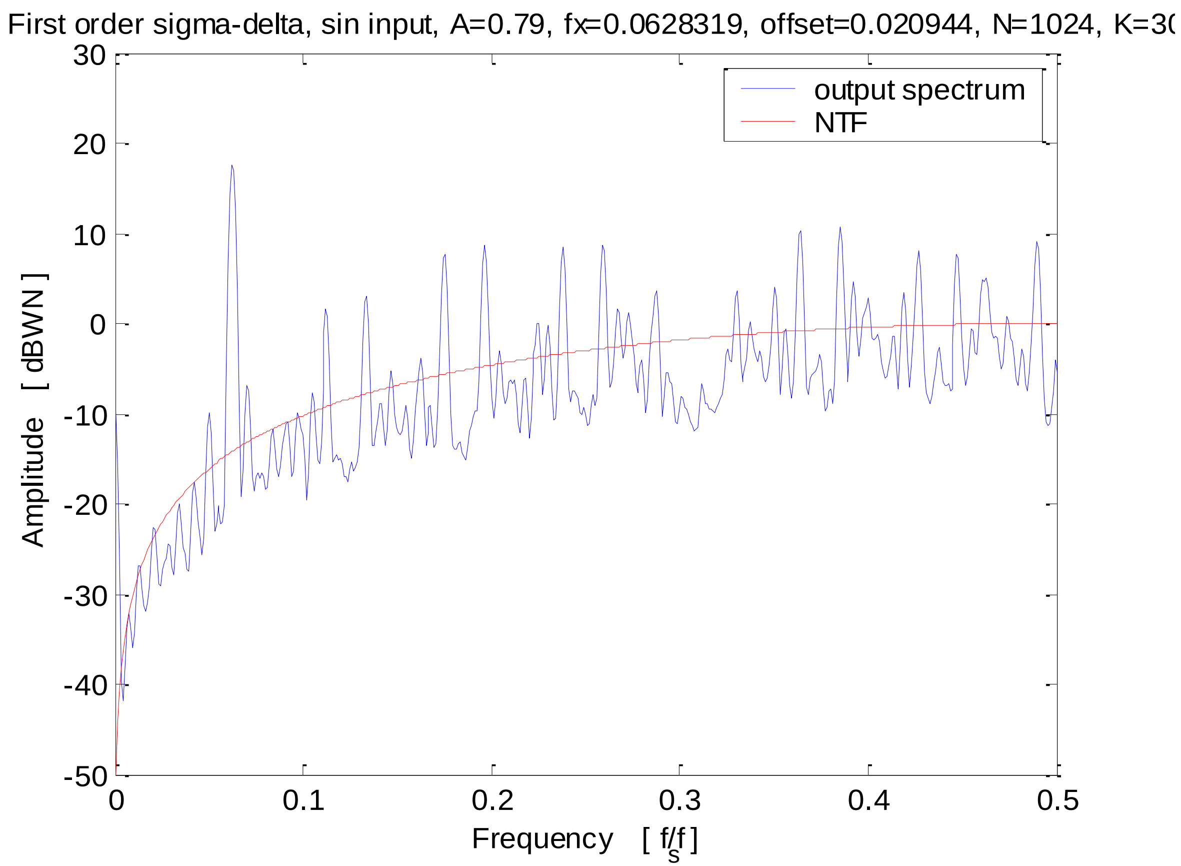
Signal transfer function:

$$\mathrm{STF} = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} = z^{-1} \quad \Rightarrow \quad \text{Delay}$$

Noise transfer function:

$$\mathrm{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} = 1 - z^{-1} \quad \Rightarrow \quad \text{Differentiator}$$

Noise Transfer Function, NTF



sigma_delta_L1_ntf.m

Quantizer Error

- For quantizer with many bits

$$\overline{e^2(kT)} = \frac{\Delta^2}{12}$$

- Let's use the same expression for the 1-Bit case
- And assume the spectrum of the quantization error is white
- Simulation will tell if the result is useful

Experience: often sufficiently accurate to be useful,
with enough exceptions to be careful

In-Band Quantization Noise

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

$$G = 1$$

$$NTF(z) = 1 - z^{-1}$$

$$\begin{aligned}
\left|NTF(z)\right|^2 &= NTF(z)\,NTF\left(z^{-1}\right) \\
&= \left(1 - z^{-1}\right)\left(1 - z\right) \\
&= 1 - z^{-1} - z + 1 \\
&= 2 - 2\cos\omega T \\
&= \left(2\sin\pi f T\right)^2 \\
&\approx \left(2\pi f T\right)^2 \qquad \text{for} \quad M >> 1
\end{aligned}$$

$$\begin{aligned}
\overline{S_Y} &= \int_{-B}^{B} S_Q(f)\left|NTF(z)\right|^2_{z=e^{2\pi j f T}} df \\
&\cong \int_{-f_s/2M}^{f_s/2M} \frac{1}{f_s}\frac{\Delta^2}{12}\left(2\sin\pi f T\right)^2 df \\
&\approx \frac{\pi^2}{3}\frac{1}{M^3}\frac{\Delta^2}{12}
\end{aligned}$$

Dynamic Range (Quantization Error)

$$DR = \frac{\text{peak signal power}}{\text{peak noise power}} = \frac{\overline{S_X}}{\overline{S_Y}}$$

$$\overline{S_X} = \frac{1}{2}\left(\frac{\Delta}{2}\right)^2$$

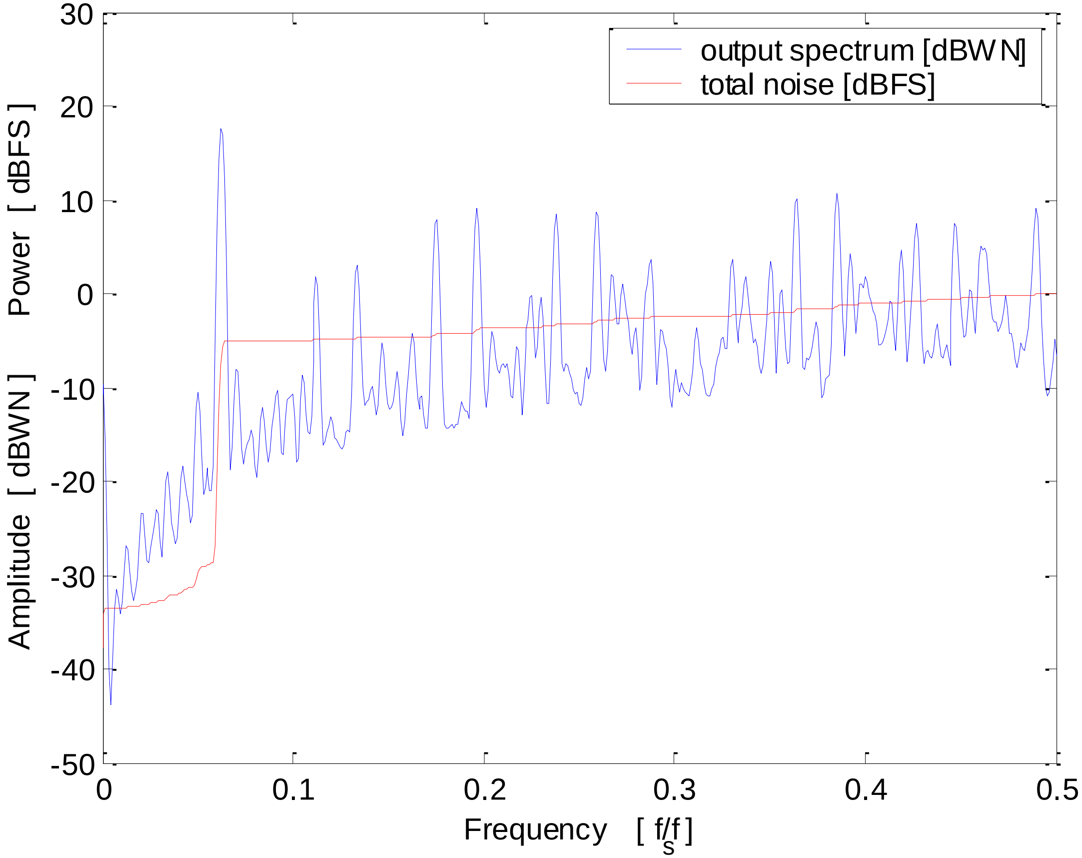
sinusoidal input, $STF = 1$

$$\overline{S_Y} = \frac{\pi^2}{3}\frac{1}{M^3}\frac{\Delta^2}{12}$$

$$\boxed{DR = \frac{9}{2\pi^2}M^3}$$

M	DR
16	33 dB
32	42 dB
1024	87 dB

Integrated Noise



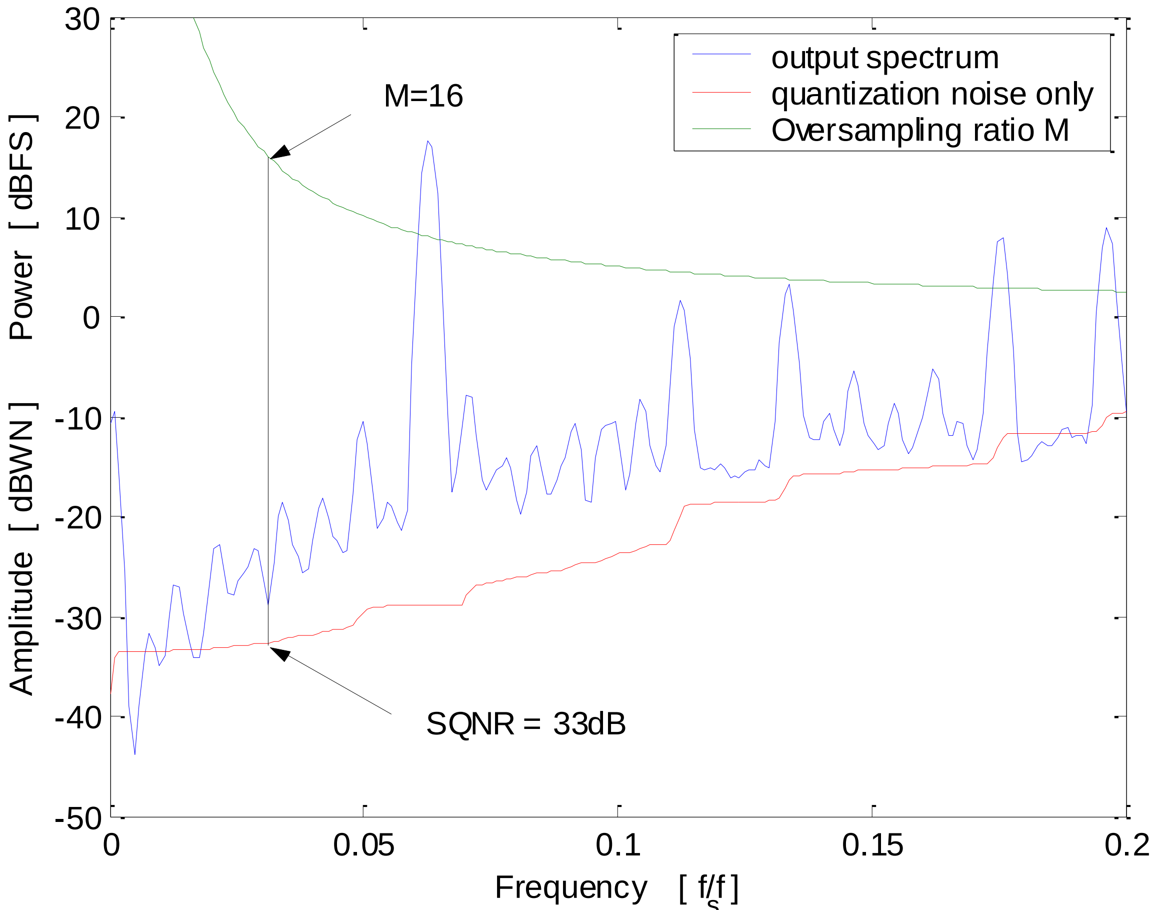
sigma_delta_L1_total_noise.m

The signal+noise at the modulator output sums to 1 (0dB)

→ This is consistent with a binary ±1 signal

[Eric Swanson]

SQNR



sigma_delta_L1_total_noise.m

Remarkably good agreement between simulation and analysis, despite violated assumptions about ADC quantization error.

<u>Detail</u>: actually simulation is 3dB short of analysis, since dBFS scale assumes full-scale DC input, not sinusoid

Matlab Source Code

```
K  = 30;                    % number of averaged simulations
N  = 2^10;                  % number of output samples
fs = 1;                     % sampling frequency
fx = pi/53;                 % signal freq
A  = 0.79;                  % signal amplitude (full-scale=1)
offset = pi/150;            % signal offset

Y = zeros(N, K);            % result vector
for i=1:K                   % average K results
    [t,x,y] = sim('sigma_delta_L1_sim', T*(N-1));
    Y(:, i) = y(:, 3);
end
[f, p, pint, pintfx] = avg_spectrum(Y, fx/fs);

plot(f, 10*log10(p), f, 10*log10(pintfx));
```

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Quantization Noise Characterisitcs

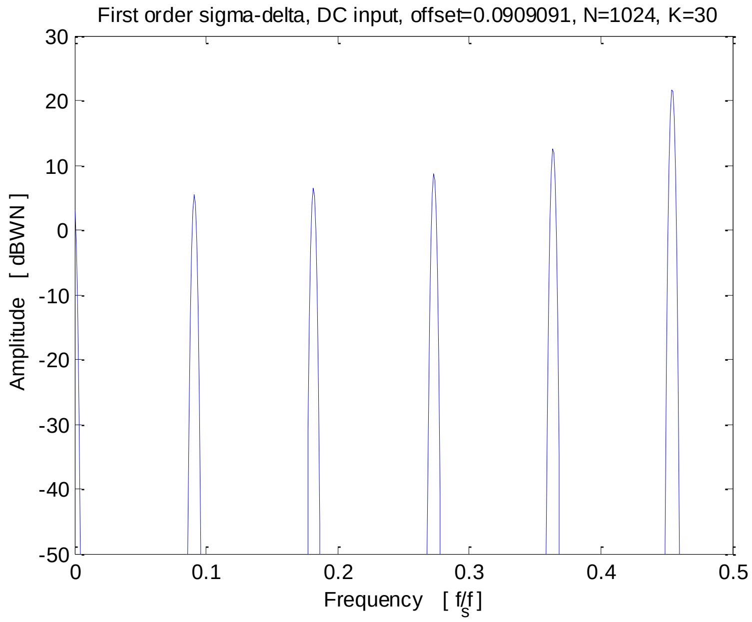
Oversampling and Noise Shaping

- ΣΔ modulators have interesting characteristics
  - Unity gain for the the input signal V_{IN}
  - Large attenuation of quantization noise injected at q
  - Much better than 1-Bit noise performance is possible if we're only interested in frequencies << f_s

- Oversampling ($M = f_s/f_N > 1$) improves SQNR considerably
  - 1^{st}-Order SD: DR increases 9dB for each doubling of M or 30 dB per decade
  - L^{th}-Order SD: DR increases (3 + 6L) dB for each doubling of M or (10 + 20L) dB per decade
  - SQNR independent of circuit complexity and accuracy

- Analysis assumes that the quantizer noise is "white"
  - Not true in practice, especially for low-order modulators
  - Practical modulators suffer from other noise sources also (e.g. thermal noise)

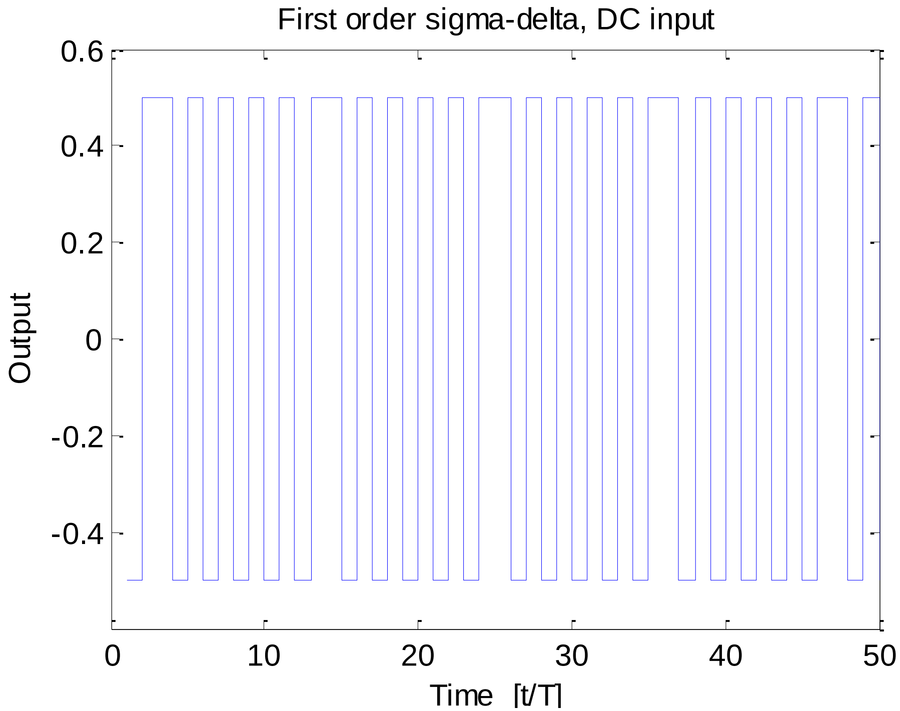
DC Input



sigma_delta_L1_sin.m

- DC input A = 1/11
- Doesn't look like spectrum of DC at all
- The ADC "sings" ???
- → Quantization "noise" is periodic

Limit Cycle



sigma_delta_L1_dc.m

DC input 1/11 →
Periodic sequence:

1	+1
2	+1
3	-1
4	+1
5	-1
6	+1
7	-1
8	+1
9	-1
10	+1
11	-1

Summary

- Oversampled ADCs decouple SQNR from circuit complexity and accuracy
- If a 1-Bit DAC is used, the converter is inherently linear—independent of component matching
- Higher order loop filters consisting of several integrators provide much better noise shaping than 1st order realizations and are less prone to limit cycles
- References

S. Pavan, R. Schreier, G. C. Temes, *Understanding Sigma Delta Converters*, IEEE Press, 2017

J. C. Candy and G. C. Temes, "Oversampling Methods for A/D and D/A Conversion", Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation, 1992, pp. 1-25.

S. R. Norsworthy, R. Schreier, and G. C. Temes, "Delta-Sigma Data Converters, Theory, Design, and Simulation," IEEE Press, 1997.

+ many others (see course website)

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5^{th} Order Modulator
(Example)

Overview

- Building and evaluating behavioral models
  - Focus on functionality first
  - Add nonidealities later
  - Beware: changes get more expensive later in the process …

- A 5th-order, 1-Bit $\Sigma\Delta$ modulator example
  - Noise shaping
  - Complex loop filters
  - Stability
  - Voltage scaling

SD Modulator Filter Design

- Procedure
  - Establish requirements
  - Design noise-transfer function, NTF
  - Determine loop-filter, H
  - Synthesize filter
  - Evaluate performance, stability

- References:

  - R. W. Adams and R. Schreier, "Stability Theory for DS Modulators," in Delta-Sigma Data Converters, S. Norsworthy et al. (eds), IEEE Press, 1997, pp. 141-164.
  - S. Pavan, R. Schreier, and G. C. Temes, Understanding Delta-Sigma Data Converters. Wiley-IEEE Press, 2017. Chapter 4.

Modulator Specification

- Example: Audio ADC

– Dynamic range	DR	16 Bits
– Signal bandwidth	B	20 kHz
– Nyquist frequency	fN	44.1 kHz
– Modulator order	L	5
– Oversampling ratio	M = fs/fN	64
– Sampling frequency	fs	2.822 MHz

- The order L and oversampling ratio M are chosen based on
  - SQNR > 120dB (20dB below thermal noise)
  - Experience (e.g. Figure 4.14 in Adams & Schreier or Figure 4.18, 4.19, 4.20 in Understand Delta-Sigma Data Converters)

Modulator Specification

- SQNR
  - Modulator Order (N in graphs below)
  - Oversampling Ratio (OSR)
  - Number of levels / bits in quantizer

[S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, 2017. Chapter 4.]

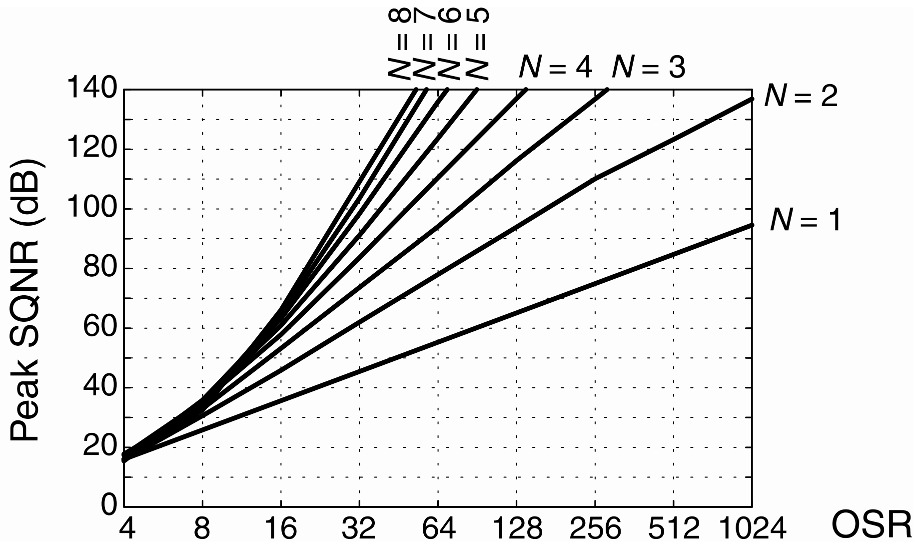


Figure 4.18 Empirical SQNR limit for 1-bit modulators of order N.

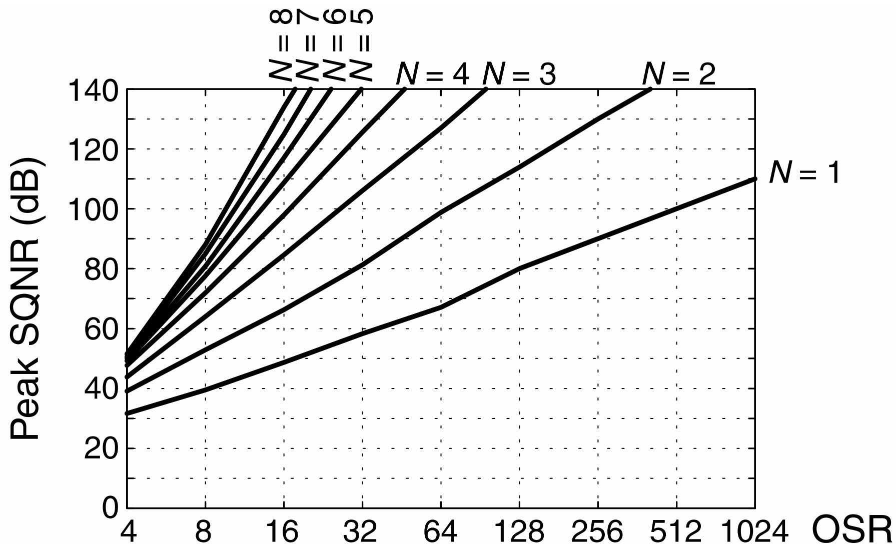
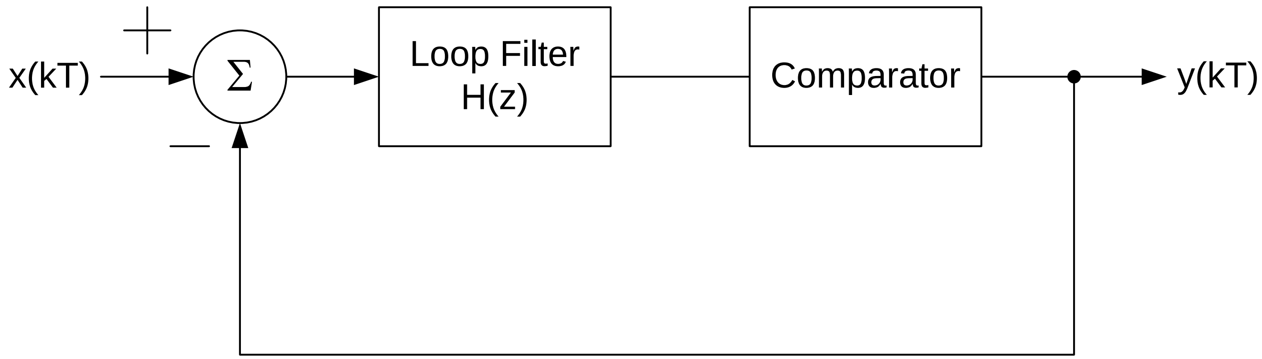


Figure 4.20 Empirical SQNR limit for modulators with 3-bit quantizers of order N.

Modulator Block Diagram



$$\mathrm{STF} = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)}$$

$$\mathrm{NTF} = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)}$$

Approach:
Design NTF and solve for H(z)

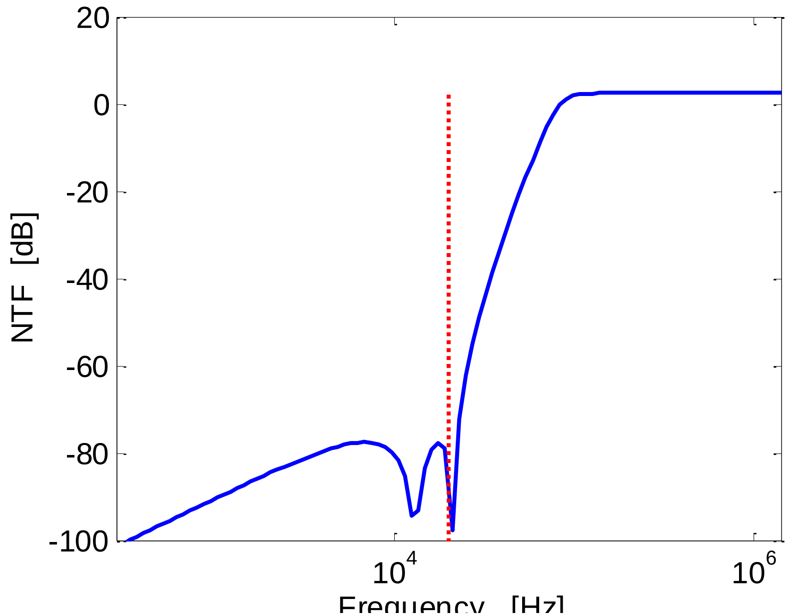
Noise Transfer Function, NTF(z)

```
% stop-band attenuation Rstop ...
% reduce if design is not stable

Rstop = 80;
[b,a] = cheby2(L, Rstop, 1/M, 'high');

% normalize (for causality)
b = b/b(1);
NTF = filt(b, a, 1/fs);

% check stability (mag < 1.5)
[mag] = bode(NTF, pi*fs)
```



>> mag = 1.32

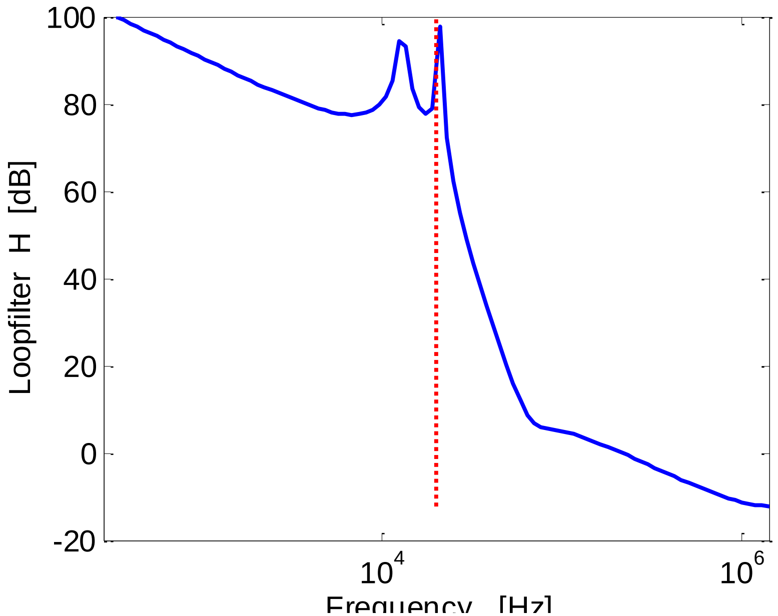
sigma_delta_L5_design.m

Loop-Filter, H(z)

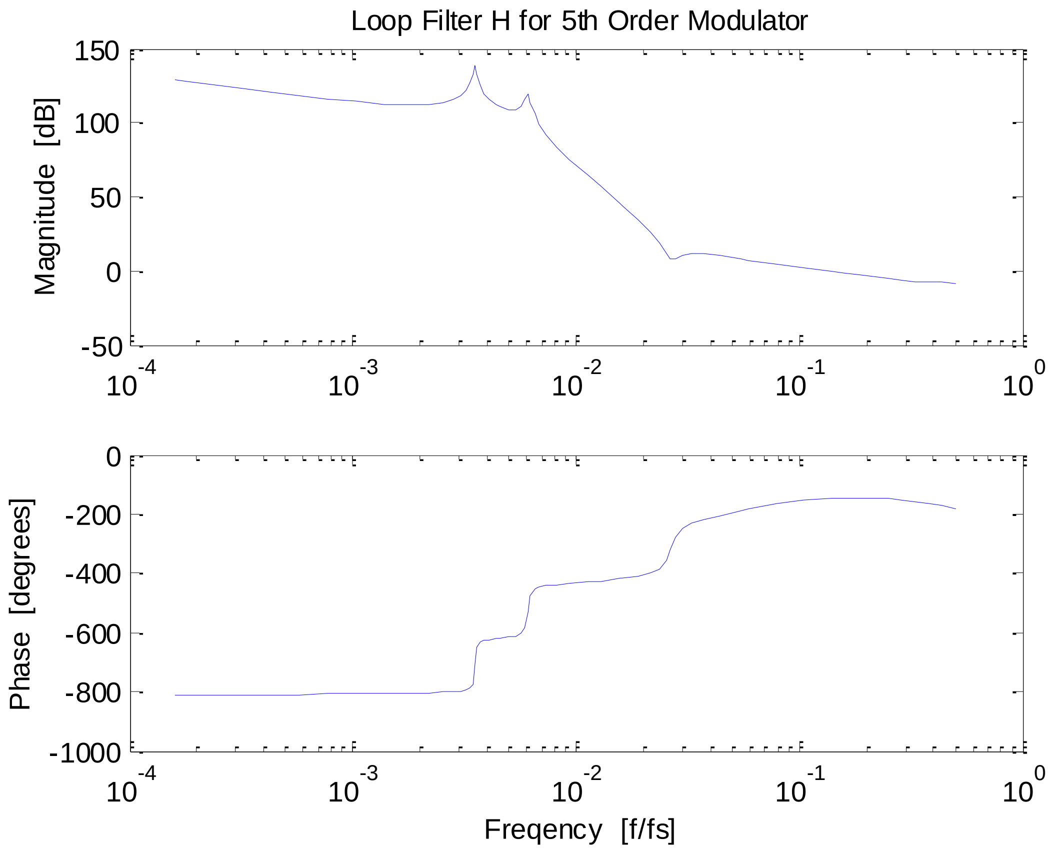
```
H = inv(NTF) - filt(1, 1, 1/fs);

% check causality … y(1) should be 0
y = impulse(H);
y = y(1)
```

>> y = 0



5^{th} Order Loop Filter



sigma_delta_L5_H.m

- Lot's of gain in the pass-band
- Remember that NTF ~ 1/H
- H ~ 0dB in stop-band gives quantization noise a place to show up

Modulator Topologies

- CIFB: Cascade of Integrators with Feedback
  - State at the output of the integrators
    → larger unscaled signals at output of integrators
  - Multiple DACs

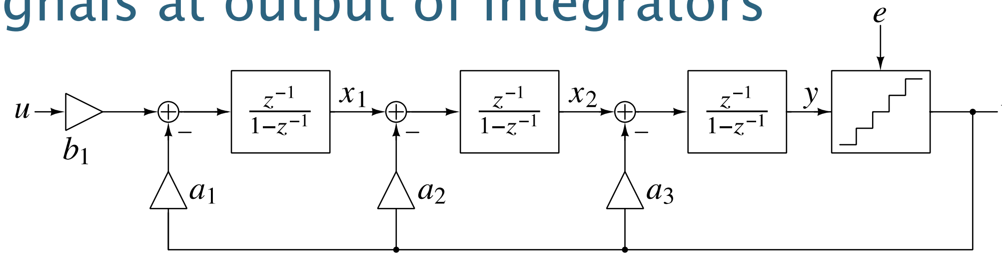


Figure 4.21 A third-order NTF realized as a cascade of integrators with feedback (CIFB) structure. All NTF zeros are at $z = 1$.

- CIFF: Cascade of Integrators with Feed-forward
  - Only quantization noise in integrators

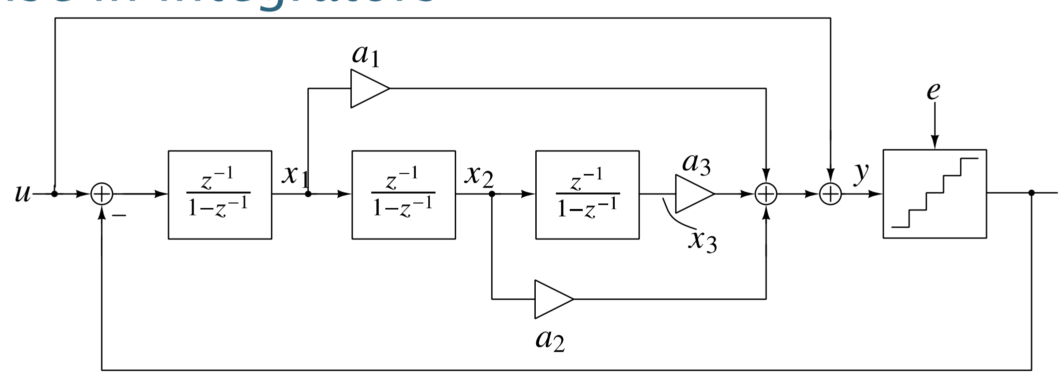
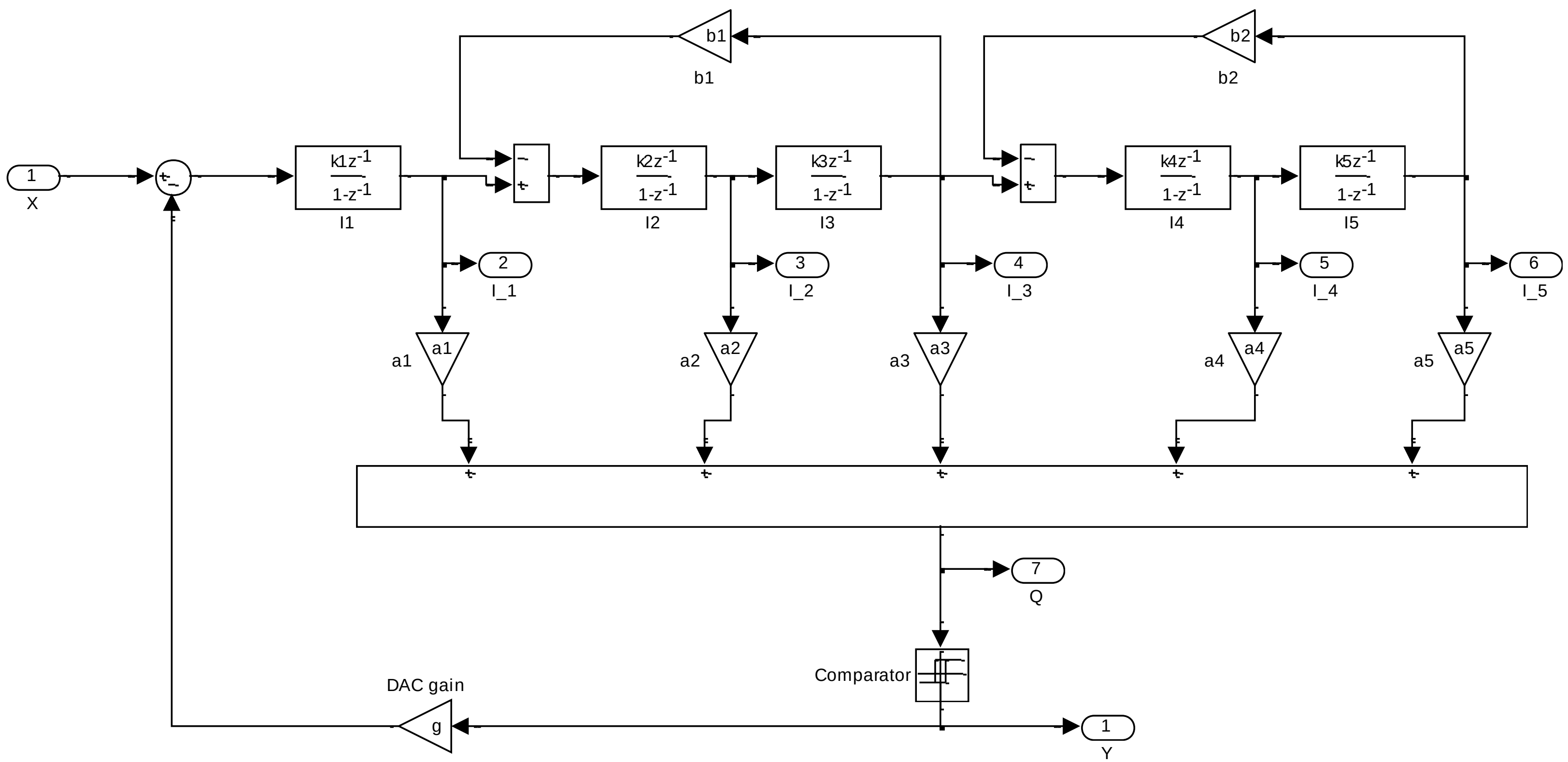


Figure 4.29 A low distortion CIFF structure, accomplished using input feedforward.

[S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, 2017. Chapter 4.]

Modulator Topology



sigma_delta_L5_sim.mdl

Rounded Filter Coefficients

```
a1=1;       k1=1;       b1=1/1024;
a2=1/2;     k2=1;       b2=1/16-1/64;
a3=1/4;     k3=1/2;
a4=1/8;     k4=1/4;     g =1;
a5=1/8;     k5=1/8;
```

Ref: Nav Sooch, Don Kerth, Eric Swanson, and Tetsuro Sugimoto, “Phase Equalization System for a Digital-to-Analog Converter Using Separate Digital and Analog Sections”, U.S. Patent 5061925, 1990, figure 3 and table 1.

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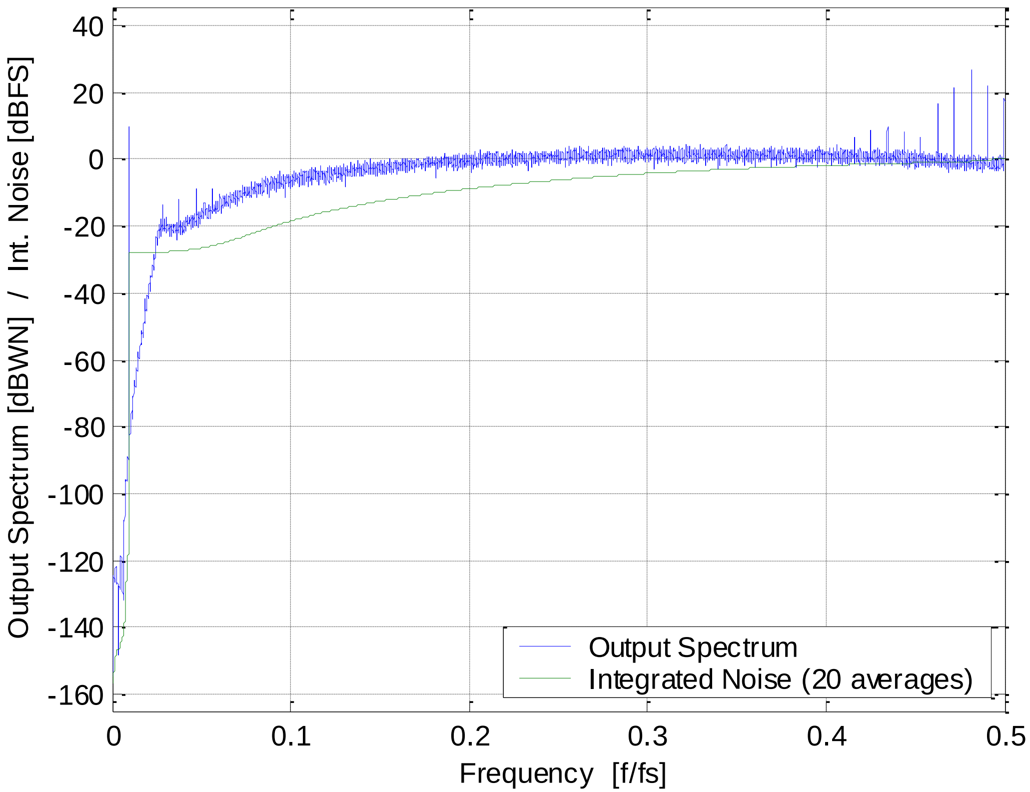
Noise Shaping

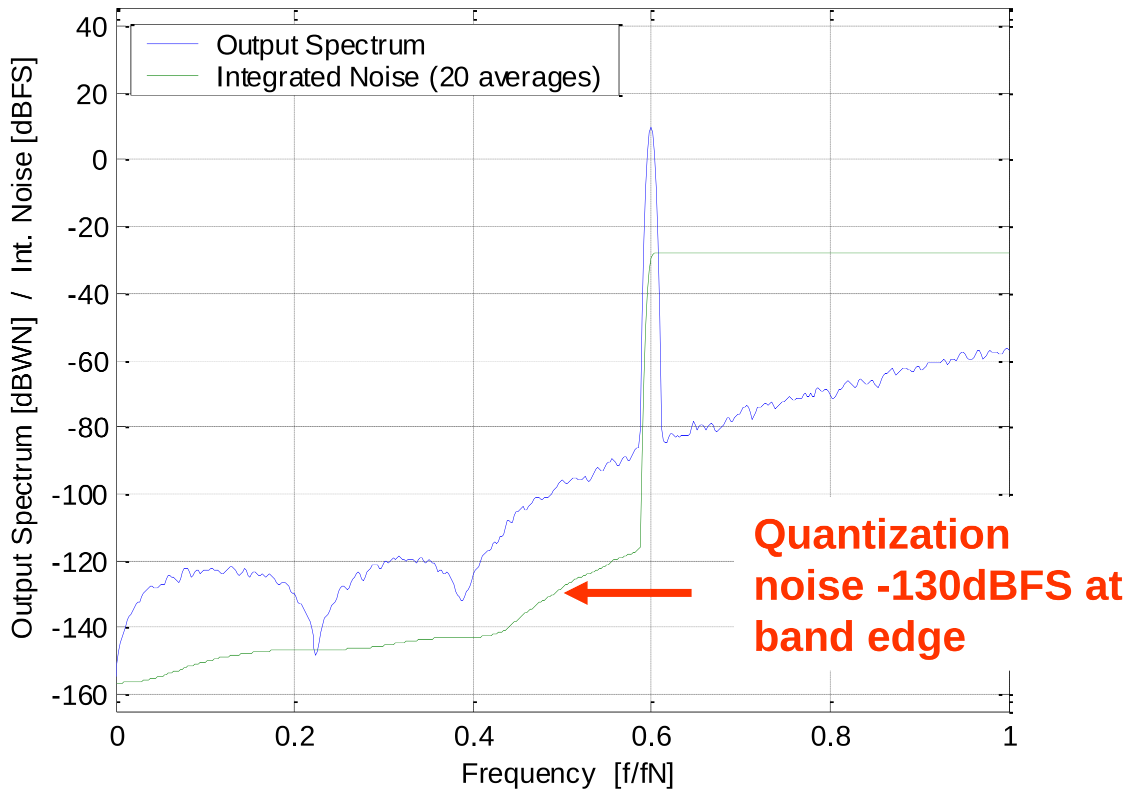
5^{th} Order Noise Shaping



- Mostly quantization noise, except at low frequencies
- Let's zoom …

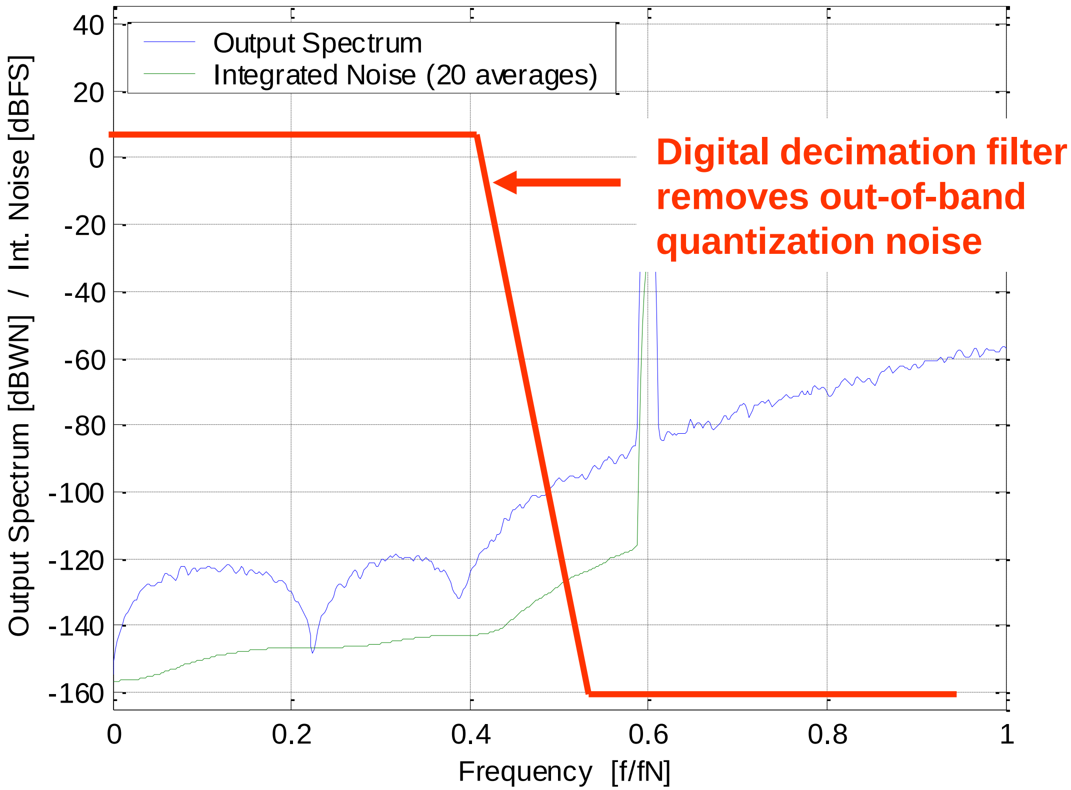
sigma_delta_L5.m

5th Order Noise Shaping



sigma_delta_L5.m

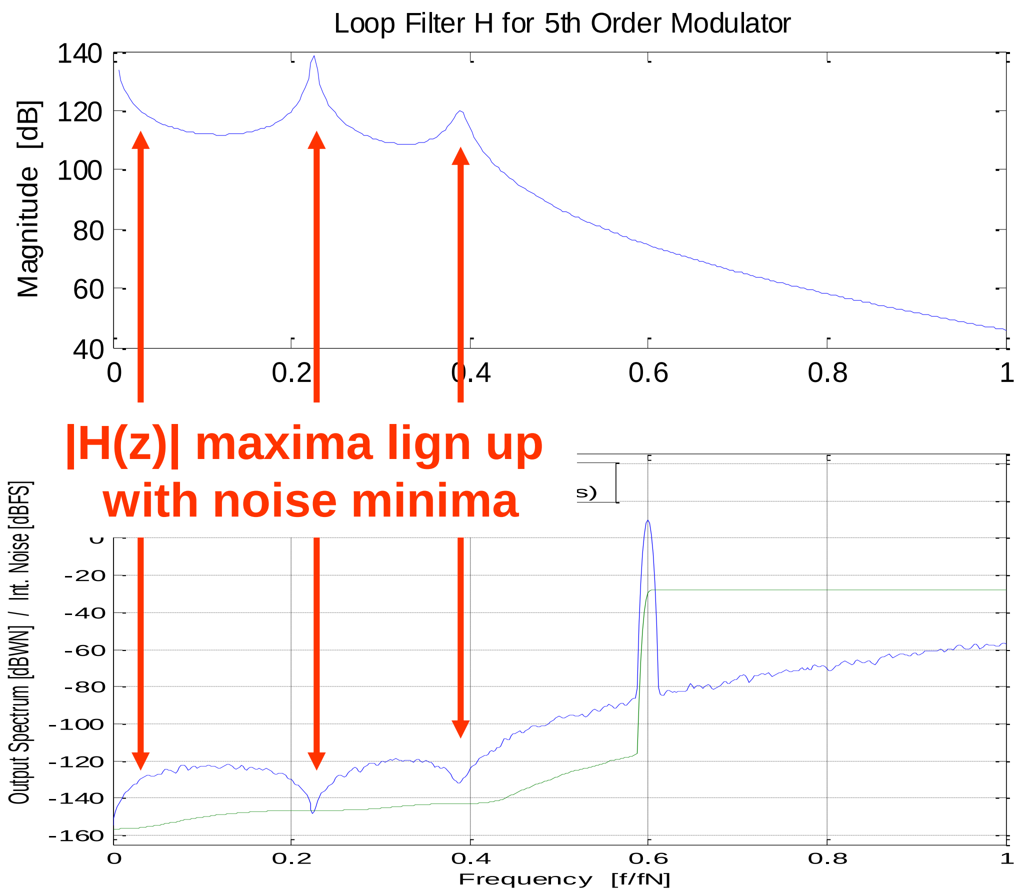
5^{th} Order Noise Shaping



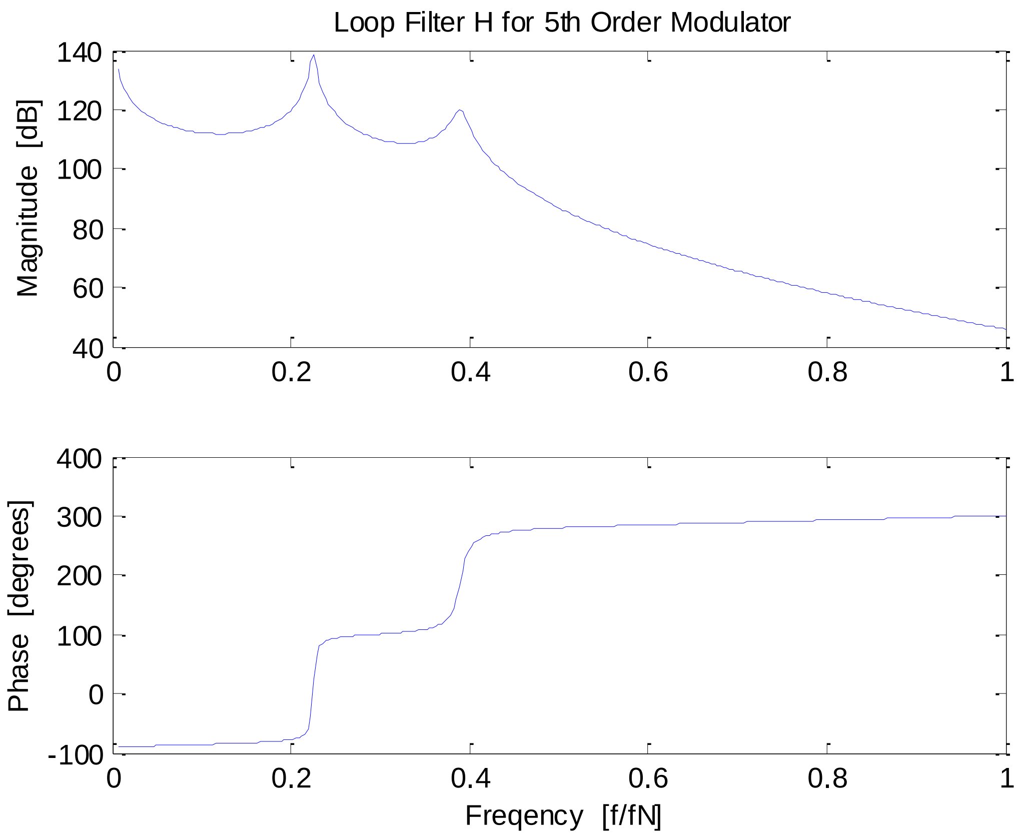
sigma_delta_L5.m

- SQNR > 120dB
- Sigma-delta modulators are usually designed for negligible quantization noise
- Other error sources dominate, e.g. thermal noise

In-Band Noise Shaping



In-Band Noise Shaping



- Positive phase jumps indicates poles of H(z) slightly outside unit circle
- Is the modulator stable?
- Let's analyze …

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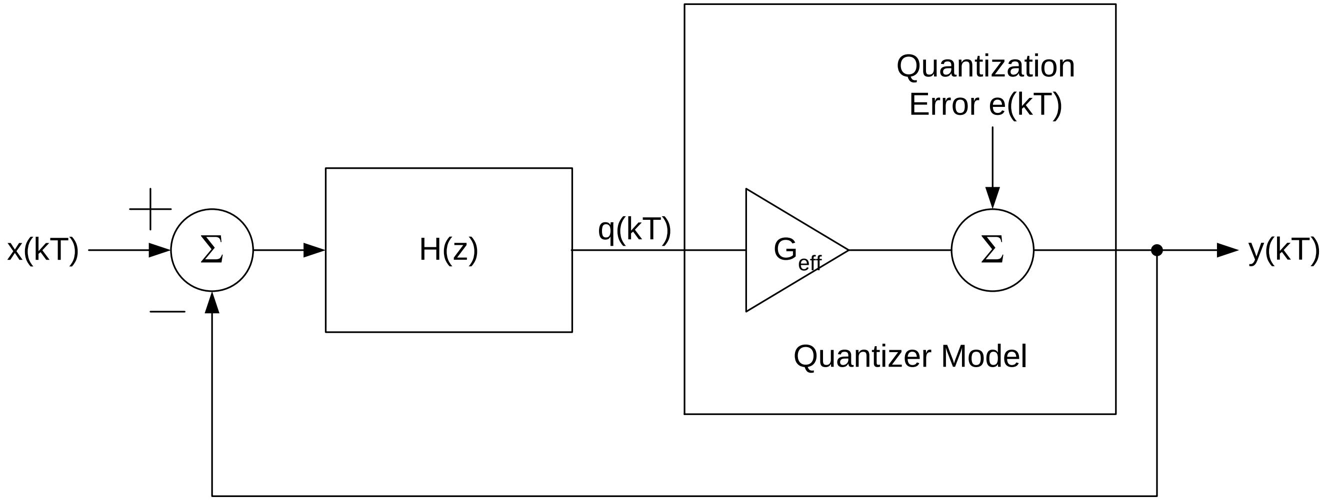
Stability and Voltage Scaling

Stability Analysis

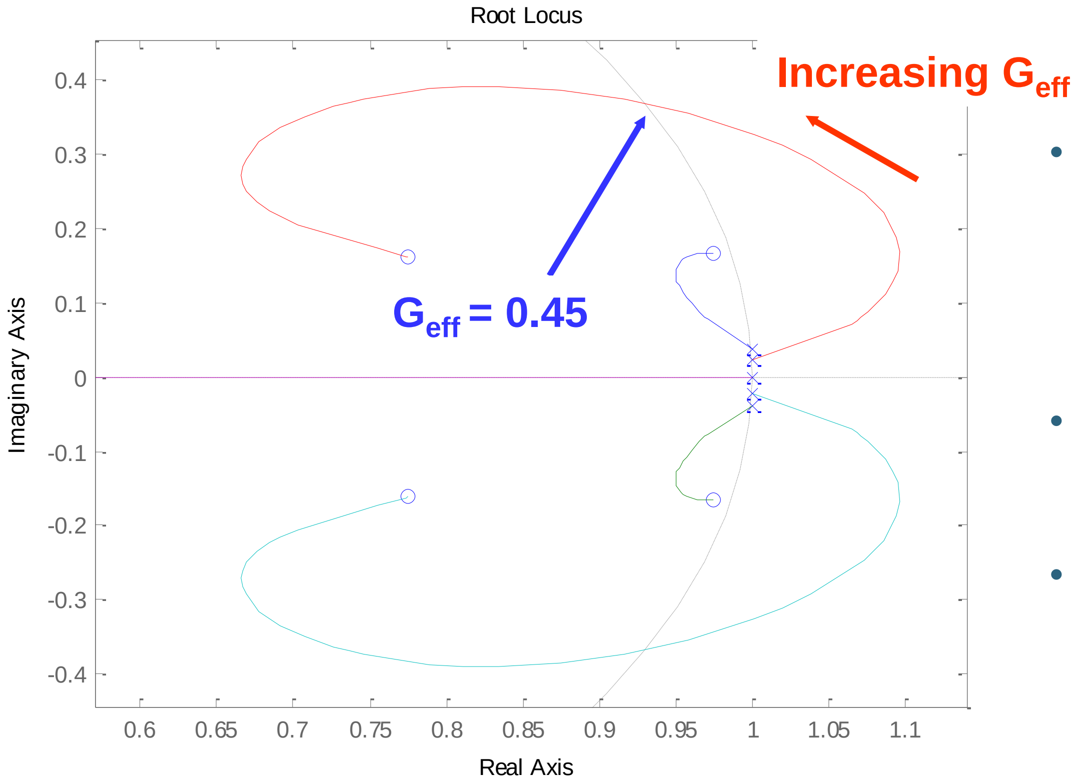


- Approach: linearize quantizer and use linear system theory!
- Effective quantizer gain

$$G_{eff}^2 = \overline{y^2} \Big/ \overline{q^2}$$

- Obtain G_{eff} from simulation

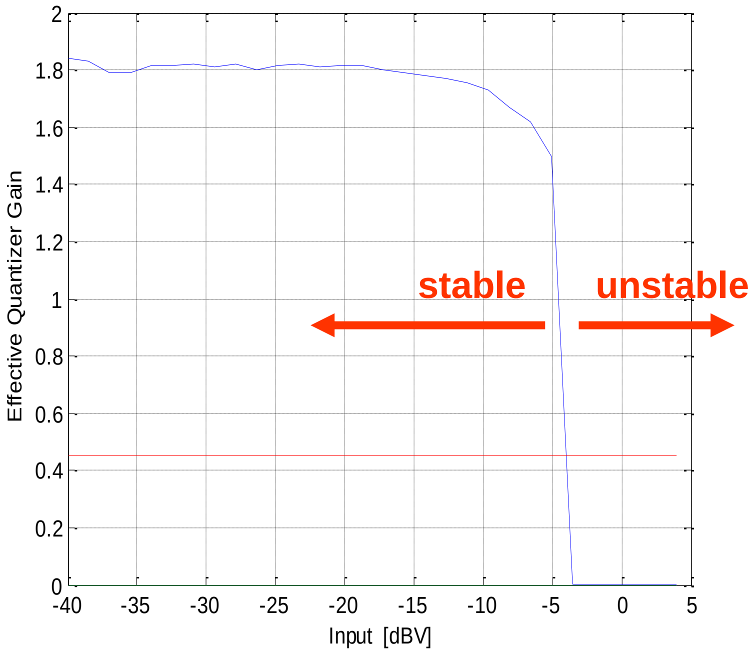
Modulator Root-Locus



- As G_{eff} increases, poles of STF move from
  - poles of H(z) (G_{eff} = 0) to
  - zeros of H(z) (G_{eff} = ∞)
- Pole-locations inside unit-circle correspond to stable modulator
- G_{eff} > 0.45 for stability

sigma_delta_L5_H.m

Effective Quantizer Gain, G_{eff}

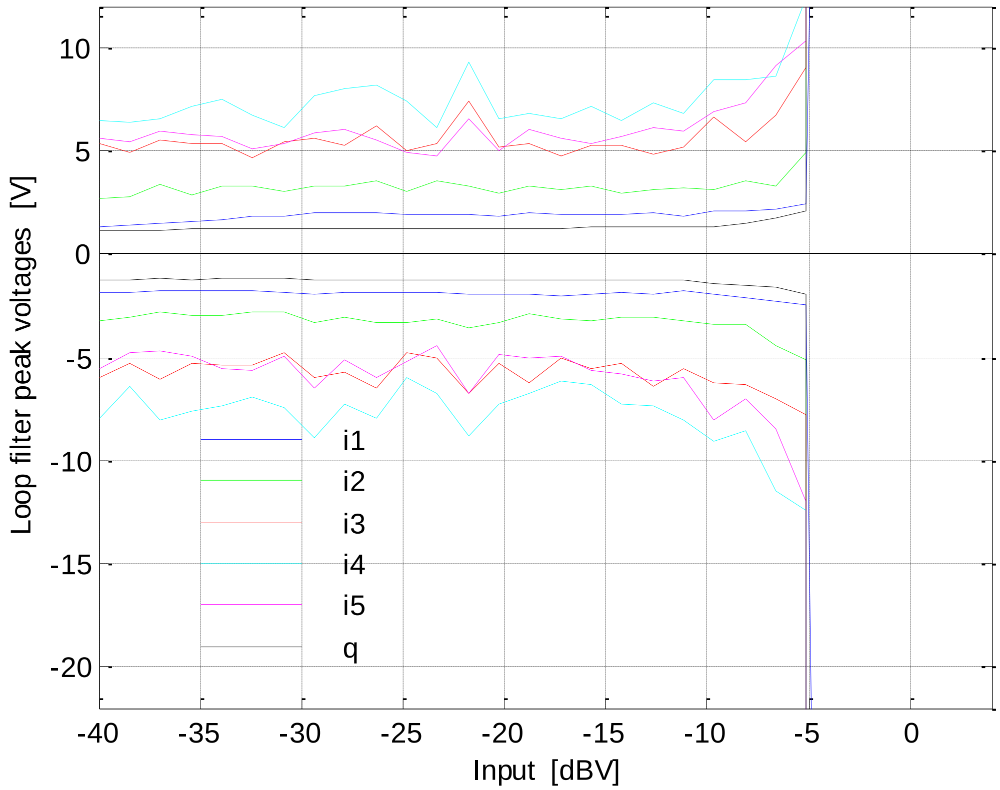


sigma_delta_L5_peaks.m

- Large inputs → comparator input grows
- Output is fixed (±1)
- → G_{eff} drops
- → modulator unstable for large inputs

- <u>Solution</u>:
  - Limit input amplitude
  - Detect instability (long sequence of +1 or -1) and reset integrators
  - Note: signals grow slowly for nearly stable systems → use long simulations

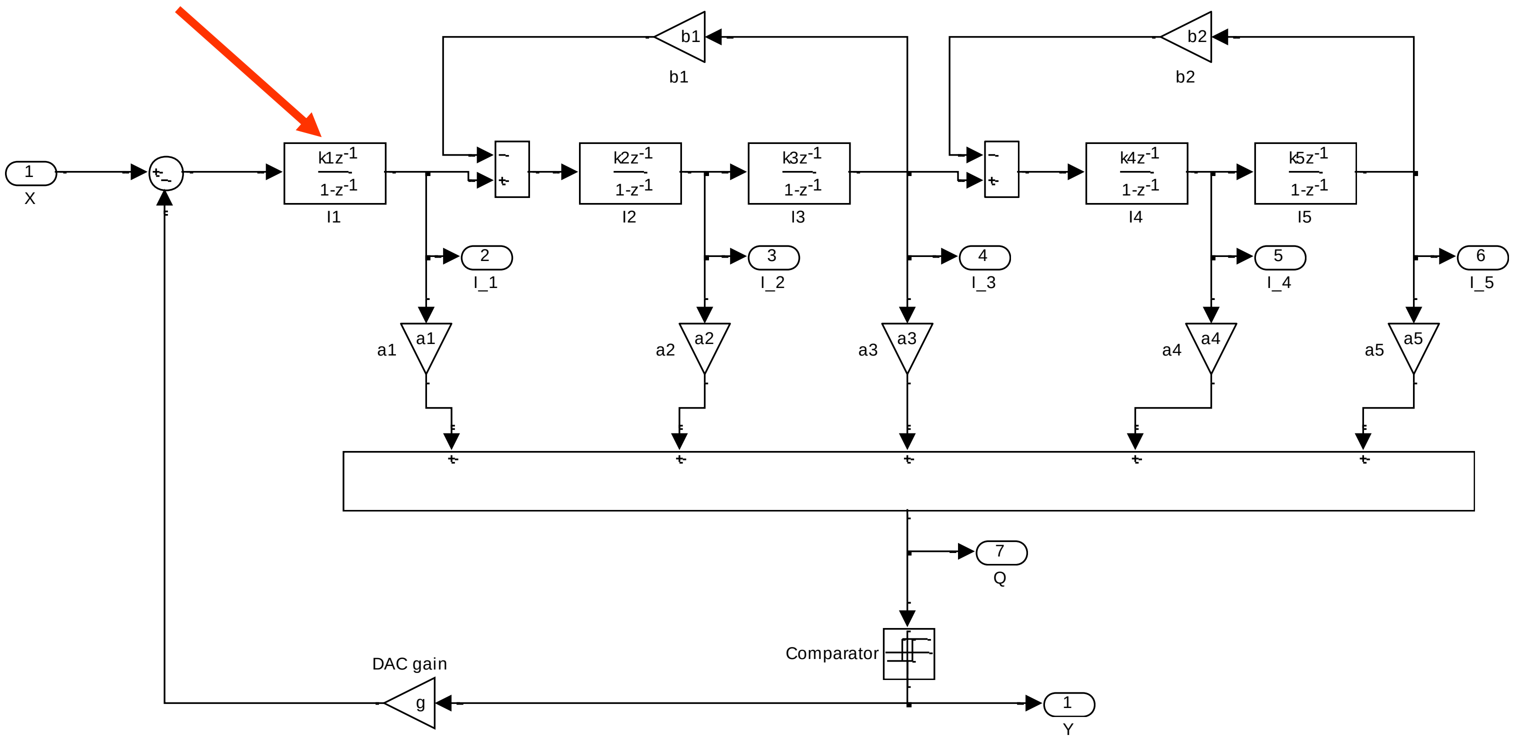
Loop Voltages



- Internal signal amplitudes are week function of input level (except near overload)
- Exceed supply voltage
- Solutions:
  - Reduce V_{ref} ??
  - Scaling

5^{th} Order Modulator – Scaling

Only the sign of Q matters: choose k_1 without changing the 1-Bit data at all

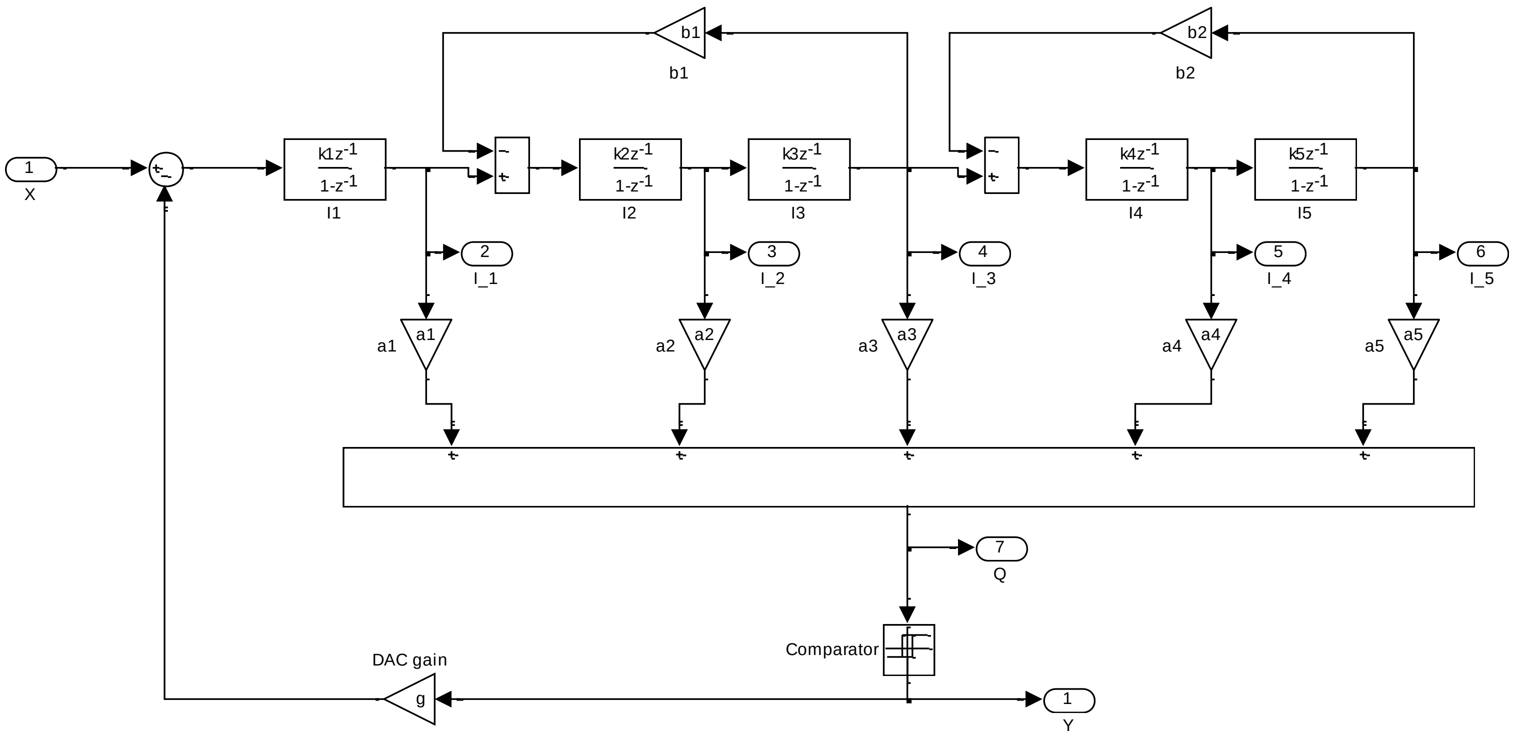


sigma_delta_L5_sim.mdl

Scaling Example

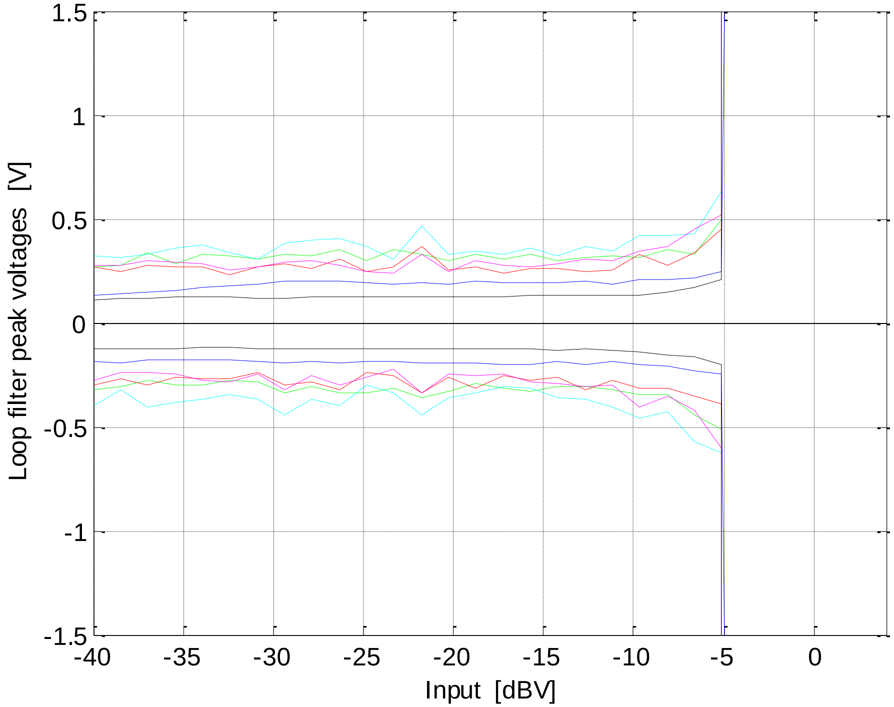
Integrator 3 Output times S:

K3 * S, b1 /S, a3 / S, K4 / S, b2 * S



sigma_delta_L5_sim.mdl

Voltage Scaling



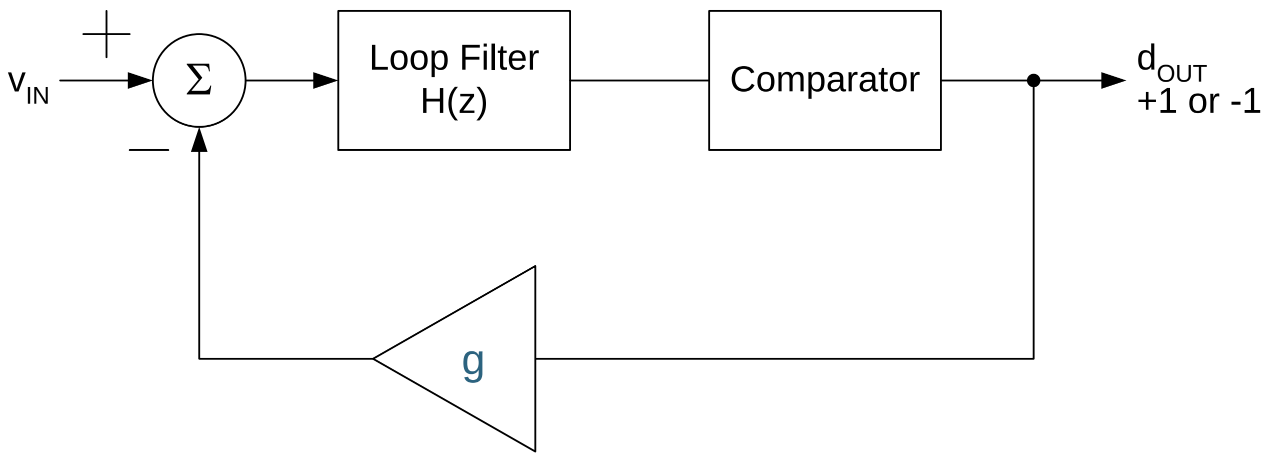
k1=1/10;
k2=1;
k3=1/4;
k4=1/4;
k5=1/8;
a1= 1;
a2=1/2;
a3=1/2;
a4=1/4;
a5=1/4;
b1=1/512;
b2=1/16-1/64;
g =1;

- Integrator output range is fine now
- But: maximum input signal limited to -5dB (-7dB with safety) – fix?

Input Range Scaling

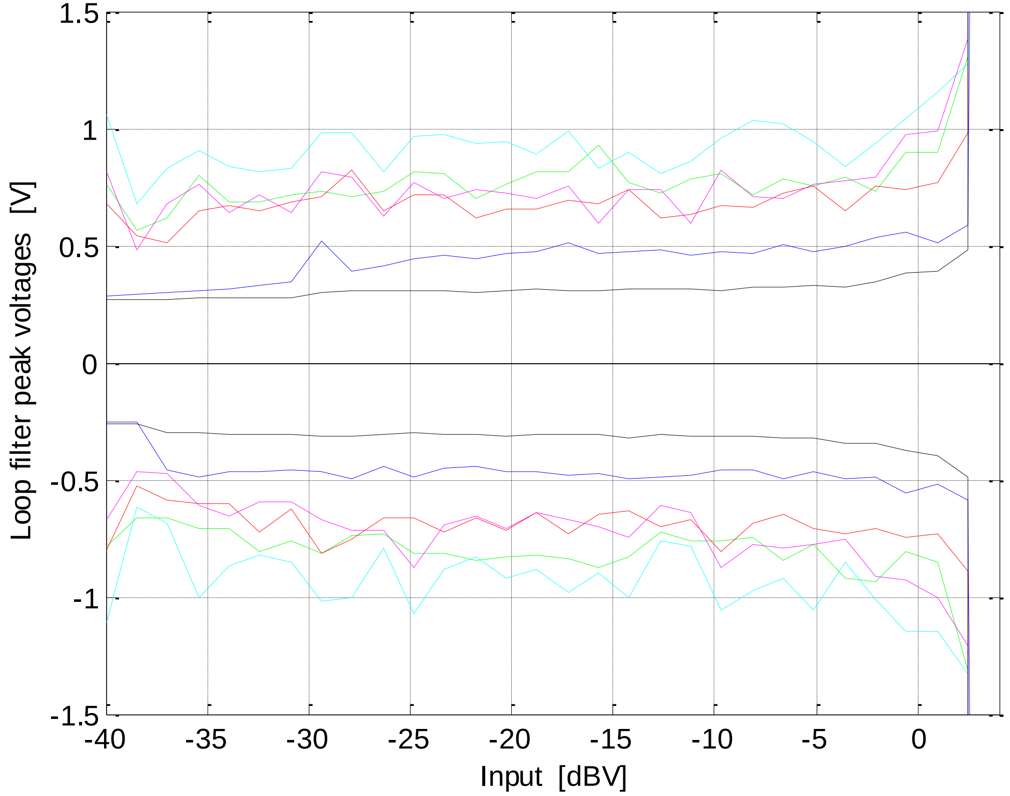
Increasing the DAC levels by g reduces the analog to digital conversion gain:

$$\frac{D_{OUT}(z)}{V_{IN}(z)} = \frac{H(z)}{1+gH(z)} \cong \frac{1}{g}$$



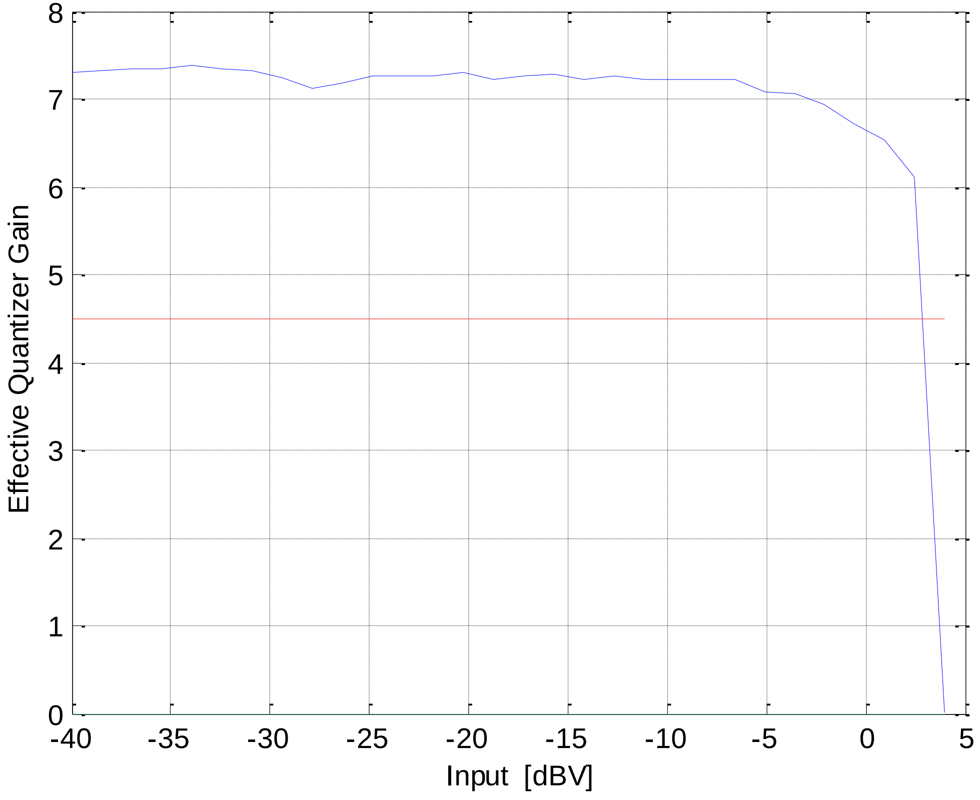
Increasing v_{IN} & DAC level (g) by the same factor leaves 1-Bit data unchanged

Scaled Modulator Model



g = 2.5;

Scaled Model Overload



2dB safety margin for stability