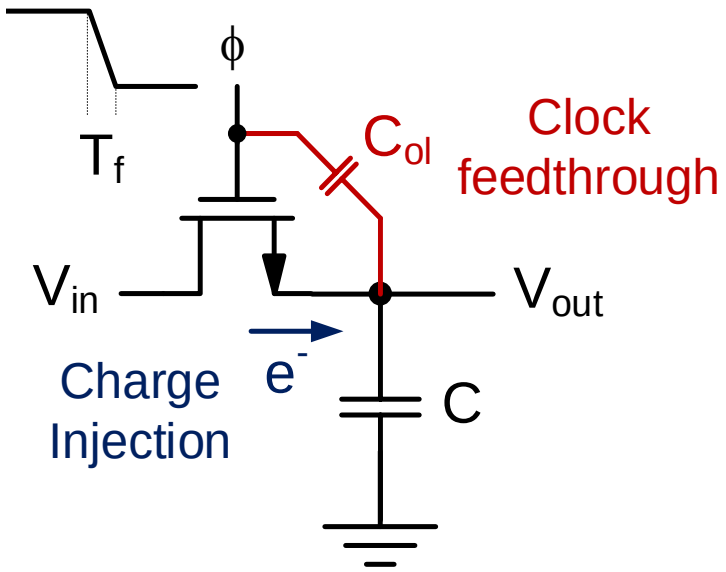
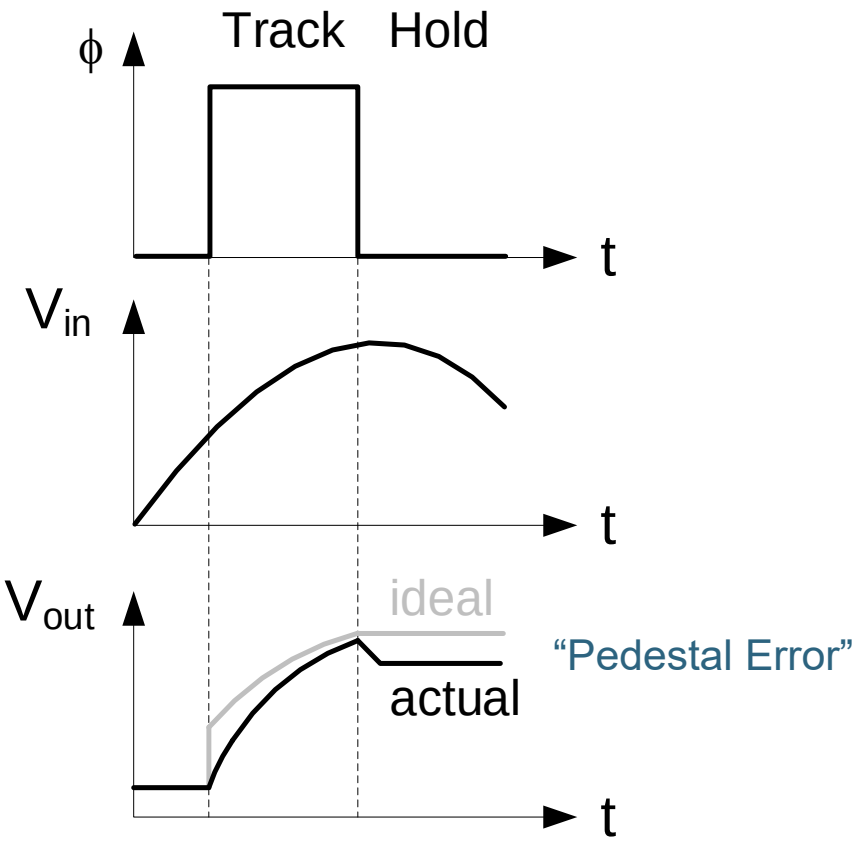
EE 240C
Analog-Digital Interface Integrated Circuits

Track & Hold Amplifier
Switch Charge Injection

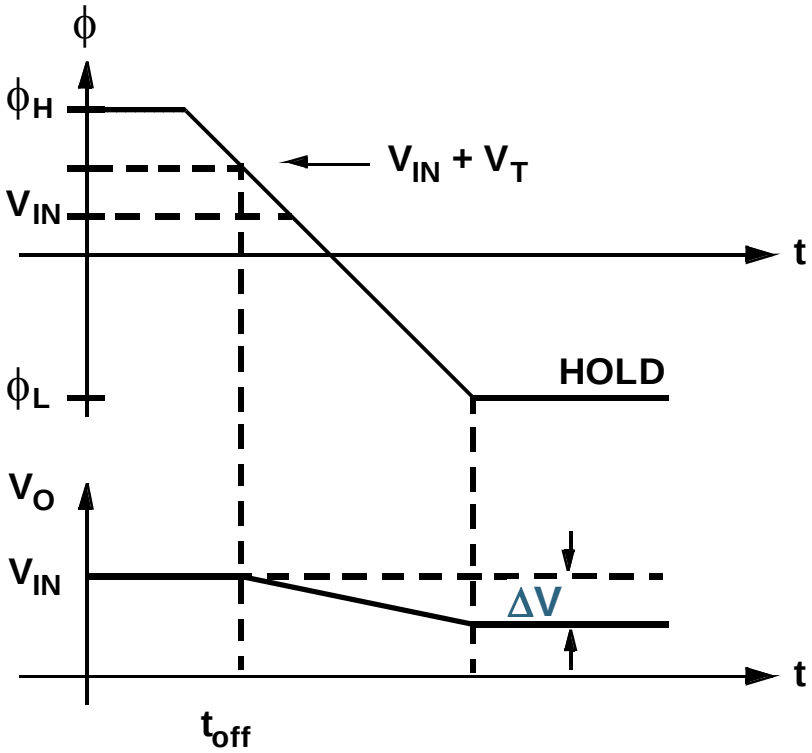
Charge Injection and Clock Feedthrough





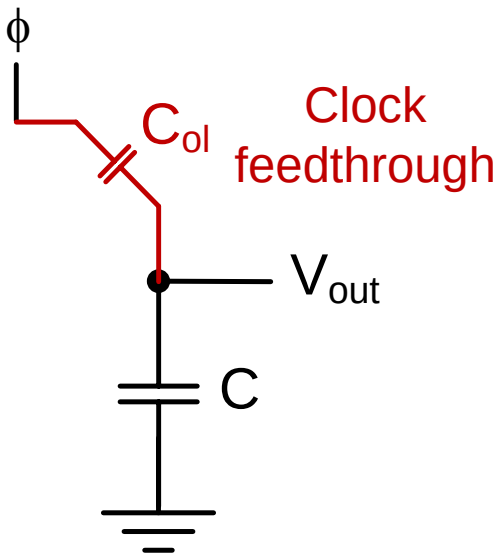
- Analyze two extreme cases
  - Very large T_f ("slow gating")
  - Very small T_f ("fast gating")

Slow Gating



- All channel charge has disappeared by t_{off} without introducing error; it is absorbed by the input source

Slow Gating Model for t > t_{off}



$$V_{\text{out}} = V_{\text{in}} - \Delta V_{\text{out}}$$

$$V_{\text{out}} = V_{in} - \frac{C_{ol}}{C_{ol}+C}(V_{\text{in}} + V_t - \phi_L) = V_{\text{in}}(1+\varepsilon) + V_{\text{os}}$$

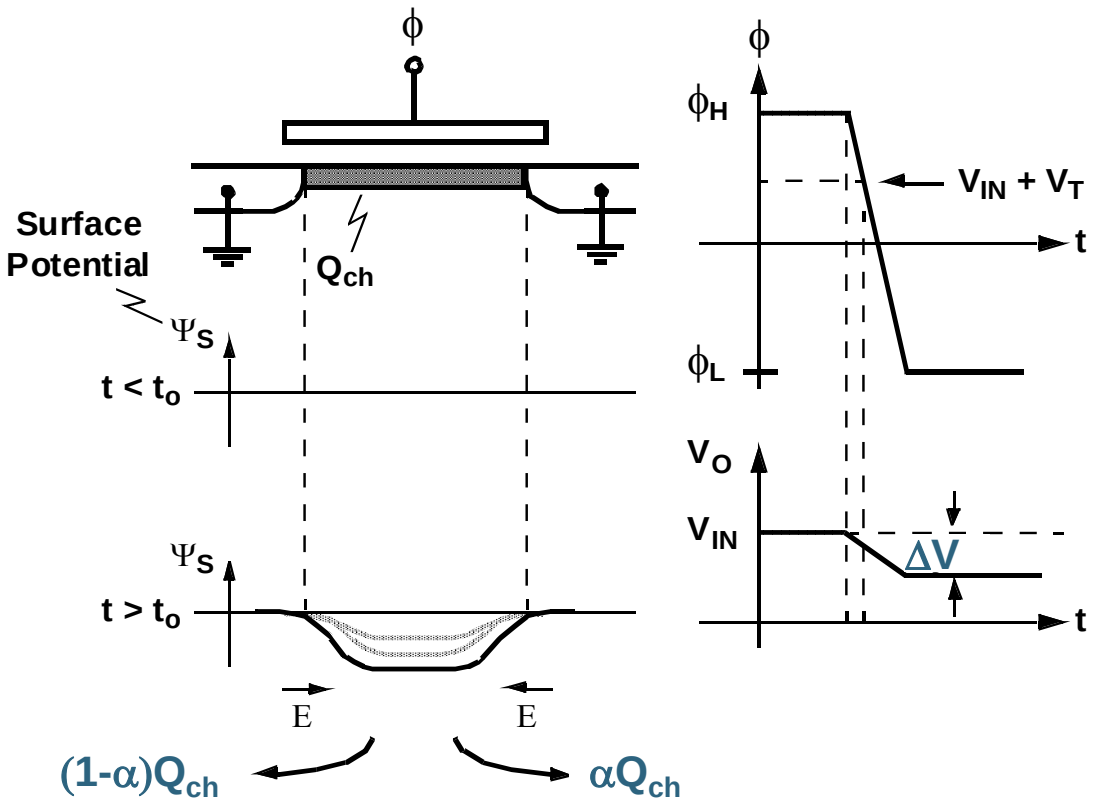
$$\varepsilon = -\frac{C_{ol}}{C_{ol}+C} \qquad V_{\text{os}} = -\frac{C_{ol}}{C_{ol}+C}(V_t - \phi_L)$$

Gain Error Offset Error

- Example: C=1pF, ϕ_L=0V, V_t=0.45V, W=20μm, C_{ol}'=0.1fF/μm, C_{ol}=2fF

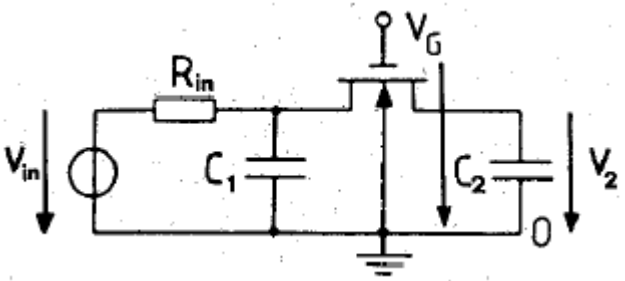
$$\varepsilon = -0.2\% \qquad V_{\text{os}} = -0.9mV$$

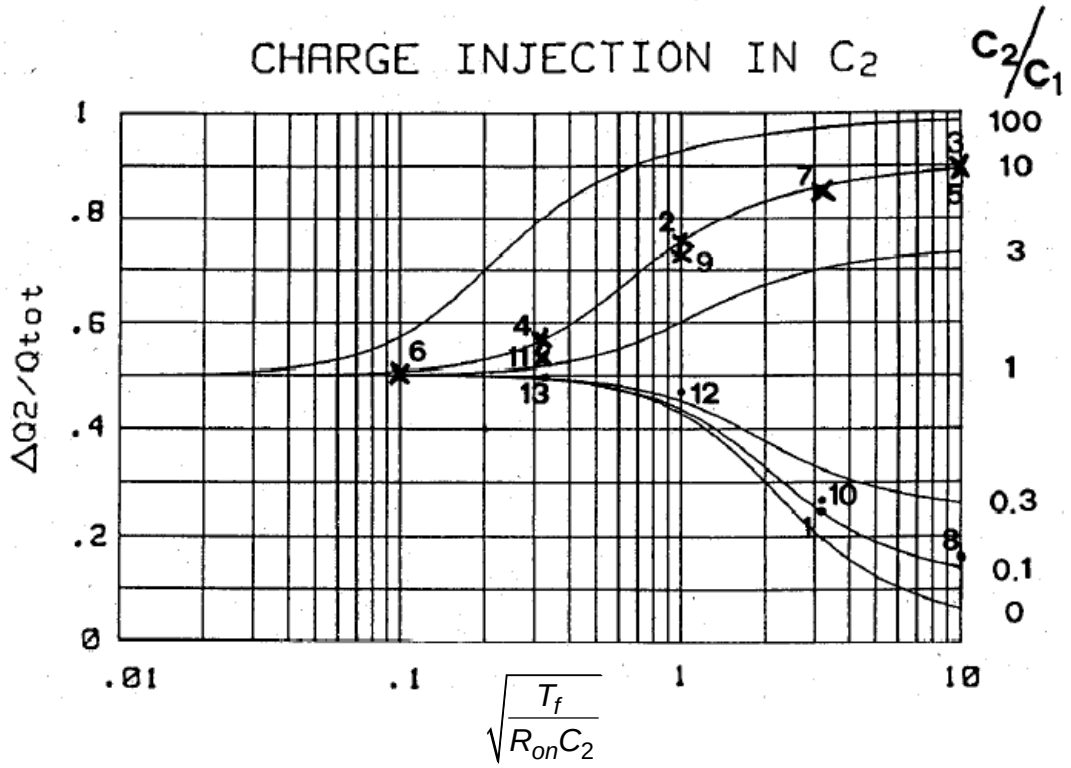
Fast Gating



- Channel charge cannot change instantaneously
- Resulting surface potential decays via charge flow to source and drain
- Charge divides between source and drain depending on impedances loading these nodes

Charge Split Ratio Data



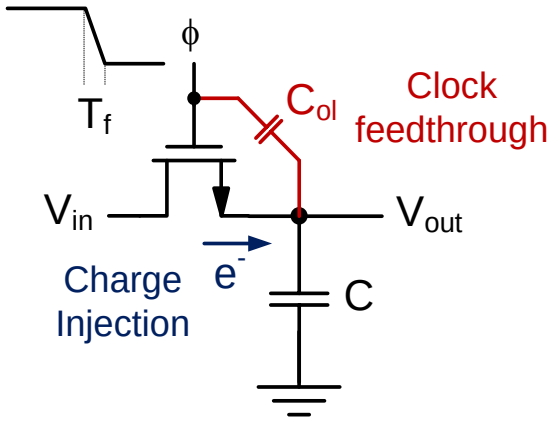


- G. Wegmann et al., "Charge injection in analog MOS switches," IEEE J. Solid-State Circuits, pp. 1091–1097, June 1987.
- Y. Ding and R. Harjani, "A universal analytic charge injection model," Proc. ISCAS, pp. 144–147, May 2000.

Interpretation

- $R_{on}C_2$ and T_f are usually comparable, or at least not more than an order of magnitude apart
  - This brings us into the range of 0.1…1 on the chart by Wegmann
- This means that the charge split will in practice have some dependence on the impedances seen on the two sides of the transistor
- Remember: Slightly more charge will go to the side with lower impedance

Fast Gating Model for t > t_{off}



$$V_{\text{out}} = V_{\text{in}} - \Delta V_{\text{out}} = V_{\text{in}}(1+\varepsilon) + V_{\text{os}}$$

$$V_{\text{out}} = V_{\text{in}} - \frac{C_{ol}}{C_{ol}+C}(\phi_H - \phi_L) + \frac{1}{2}\frac{Q_{ch}}{C}$$

Assuming 50/50 charge split

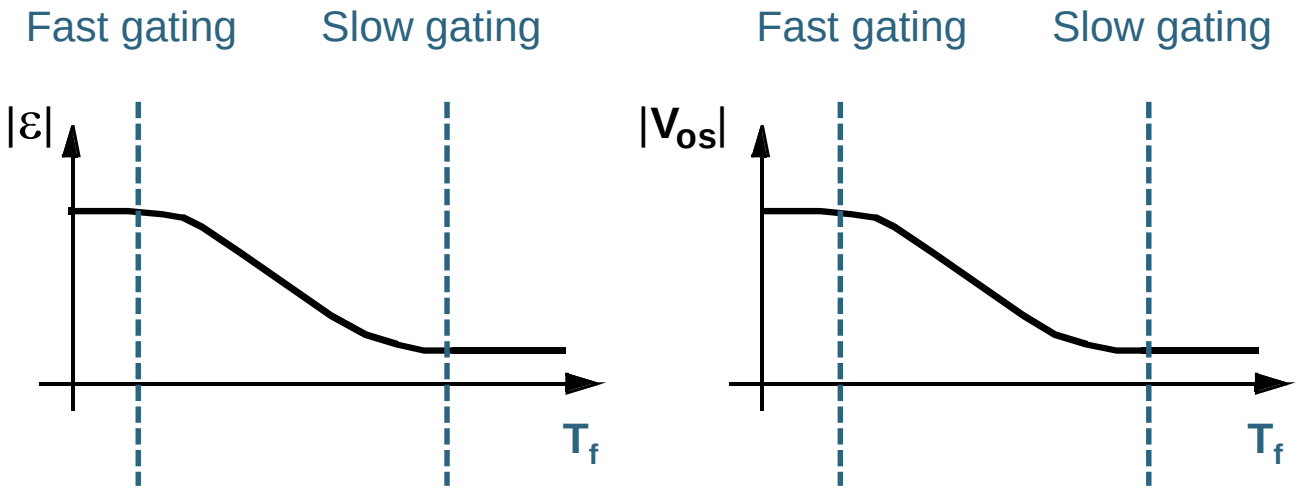
$$Q_{ch} = -WLC_{ox}[\phi_H - V_{\text{in}} - V_t]$$

$$\varepsilon = \frac{1}{2}\frac{WLC_{ox}}{C} \qquad V_{\text{os}} = -\frac{C_{ol}}{C_{ol}+C}(\phi_H - \phi_L) - \frac{1}{2}\frac{WLC_{ox}}{C}(\phi_H - V_t)$$

- Example: C=1pF, ϕ_H-ϕ_L=1.8V, V_t=0.45V, W=20μm, LC_{ox}=2fF/μm C_{ol}'=0.1fF/μm, C_{ol}=2fF

$$\varepsilon = +2\% \qquad V_{\text{os}} = -30.6mV$$

Transition Fast/Slow Gating



- $|\varepsilon|$ and $|V_{os}|$ decrease as the fall time of ϕ (T_f) increases and approach the limit case of slow gating
- Unfortunately, high-speed switched capacitor circuits tend to operate in fast gating regime

Impact of Technology Scaling

$$\Delta V \cong \frac{1}{2}\frac{Q_{ch}}{C} \qquad \frac{1}{2f_s} = \frac{T_s}{2} = N \cdot RC$$

$$R \cong \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_t)} = \frac{L^2}{\mu Q_{ch}}$$

$$\frac{\Delta V}{f_s} \cong N\frac{L^2}{\mu}$$

- Charge injection error to speed ratio benefits from shorter channels and increases in mobility (e.g. due to strain)

EE 240C
Analog-Digital Interface Integrated Circuits

Track & Hold Amplifier – Improvements

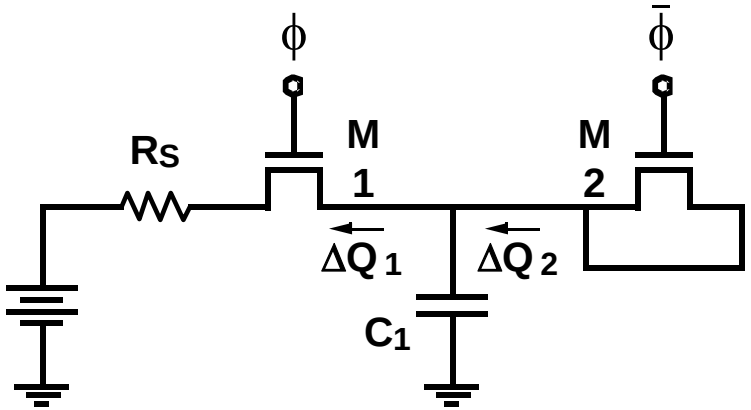
Outline

- Elementary track-and-hold circuit and its nonidealities
- First order improvements to elementary track-and-hold
- Advanced techniques
  - Clock bootstrapping
  - Bottom plate sampling
- Settling and noise analysis in charge-redistribution track-and-hold circuit
- Noise simulation example

Improvements

- Charge cancelation
  - Try to cancel channel charge by injecting a charge packet with opposite sign
- Differential sampling
  - Use a differential circuit to suppress offset
- CMOS switch
  - Try to balance the nonidealities of NMOS device with a parallel PMOS

Charge Cancellation



$L_2=L_1$
$W_2=0.5W_1$

$$\Delta Q_1 = 0.5Q_{ch1} + Q_{ol1}$$

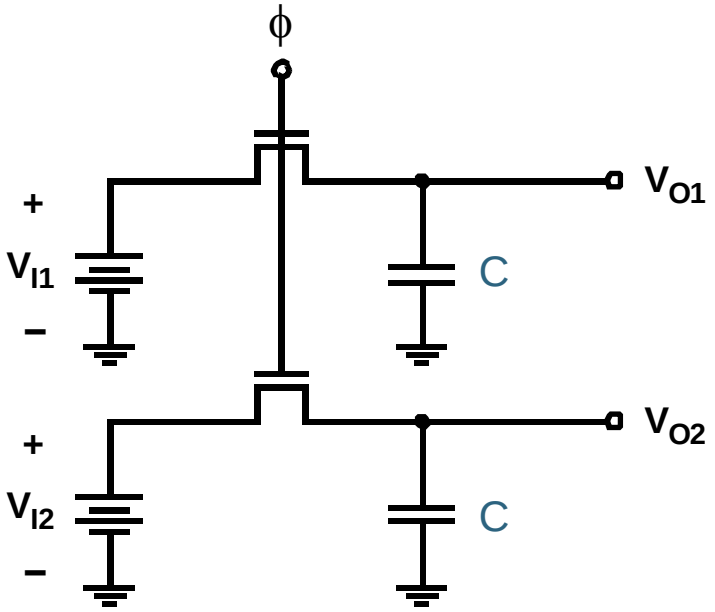
$$\Delta Q_2 \cong Q_{ch2} + 2Q_{ol2} \cong 0.5Q_{ch1} + Q_{ol1}$$

$$\Delta Q_1 - \Delta Q_2 \cong 0$$

[C. Eichenberger and W. Guggenbuhl, "Dummy transistor compensation of analog MOS switches," *IEEE J. Solid-State Circuits*, vol. 24, no. 4, pp. 1143-1146, Aug. 1989.]

- Cancellation is never perfect, since channel charge of M1 will not exactly split 50/50
  - E.g. if R_s is very small, most of M1's channel charge will flow toward the input voltage source
- Not a precision technique, just an attempt to do a partial clean-up

Differential Sampling (1)



$$V_{ID} = V_{I1} - V_{I2} \qquad V_{OD} = V_{O1} - V_{O2}$$

$$V_{IC} = \frac{V_{I1} + V_{I2}}{2} \qquad V_{OC} = \frac{V_{O1} + V_{O2}}{2}$$

$$V_{O1} = (1 + \varepsilon_1)V_{I1} + V_{OS1}$$

$$V_{O2} = (1 + \varepsilon_2)V_{I2} + V_{OS2}$$

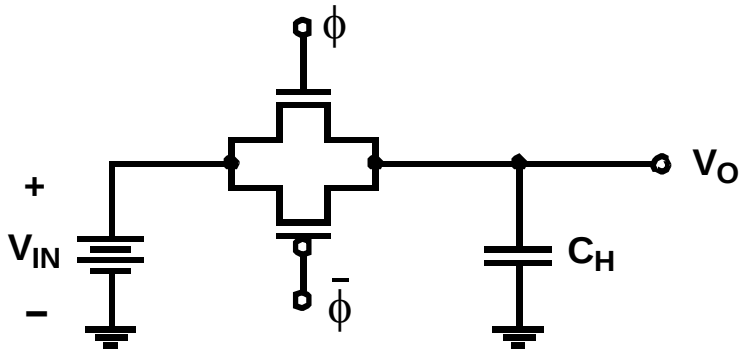
$$V_{OD} = \left(1 + \frac{\varepsilon_1 + \varepsilon_2}{2}\right)V_{ID} + (\varepsilon_1 - \varepsilon_2)V_{IC} + (V_{OS1} - V_{OS2}) \cong \left(1 + \frac{\varepsilon_1 + \varepsilon_2}{2}\right)V_{ID}$$

$$V_{OC} = \left(\frac{\varepsilon_1 - \varepsilon_2}{4}\right)V_{ID} + \left(1 + \frac{\varepsilon_1 + \varepsilon_2}{2}\right)V_{IC} + \left(\frac{V_{OS1} + V_{OS2}}{2}\right) \cong \left(1 + \frac{\varepsilon_1 + \varepsilon_2}{2}\right)V_{IC} + \left(\frac{V_{OS1} + V_{OS2}}{2}\right)$$

Differential Sampling (2)

- Assuming good matching between the two half circuits, we have
  - Small residual offset in V_{OD}
  - Good rejection of coupling noise, supply noise, …
  - Small common-mode to differential-mode gain
- Unfortunately, V_{OD} has essentially same gain error as the basic single ended half circuit
- This also means that there will be nonlinear terms
  - Our simplistic analysis assumed that the channel charge is linearly related to V_{in}
  - This is true only to first order (consider e.g. backgate effect)
    - Expect to see nonlinear distortion along with gain error

CMOS Switch



$$Q_{chn} \cong -W_n L_n C_{ox}(\phi_H - V_{\mathrm{IN}} - V_{tn})$$

$$Q_{chp} \cong W_p L_p C_{ox}\left(V_{\mathrm{IN}} - \phi_L - |V_{tp}|\right)$$

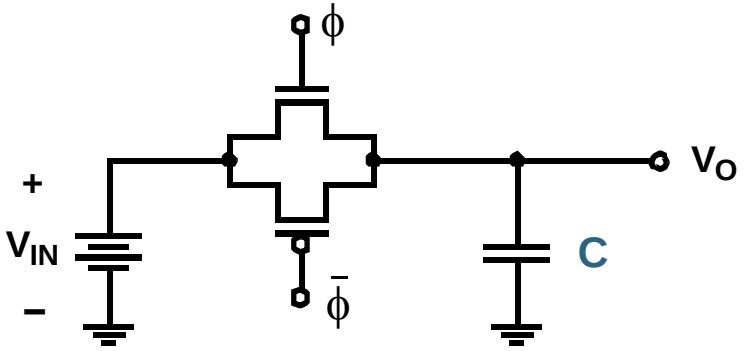
- Assuming fast gating, 50/50 charge split and $W_nL_n = W_pL_p$

$$\Delta V_o \cong \frac{\frac{1}{2}Q_{chn} + \frac{1}{2}Q_{chp}}{C} = \frac{C_{ox}}{C}\left(V_{\mathrm{IN}} - \frac{\phi_H - \phi_L}{2} + \frac{V_{tn} - |V_{tp}|}{2}\right)$$

- Charges fully cancel e.g. for $V_{IN} = (\phi_H - \phi_L)/2 = V_{DD}/2$, and $V_{tn} = |V_{tp}|$, but there is still signal dependent residual injection

On Resistance of CMOS Switch

- At least in principle, adding a PMOS can also help with the problem of signal dependent R_{on} in track mode
  - For increasing V_{IN}, NMOS resistance goes up, PMOS resistance goes down



$$R \cong \frac{1}{\mu_n C_{ox}\left[\frac{W}{L}\right]_n (V_{GSn} - V_{tn})} \Bigg\| \frac{1}{\mu_p C_{ox}\left[\frac{W}{L}\right]_p \left(|V_{GSp}| - |V_{tp}|\right)}$$

Analysis

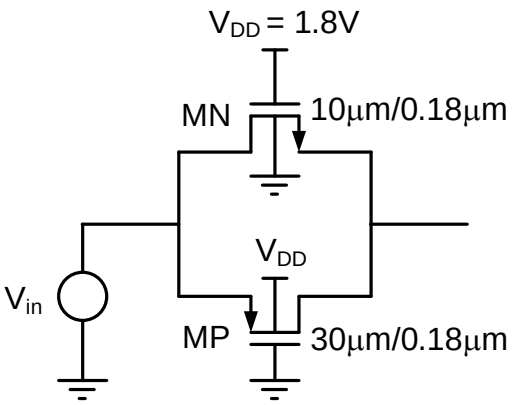
$$R \cong \frac{1}{\mu_n C_{ox}\left[\frac{W}{L}\right]_n (V_{GSn} - V_{tn})} \Bigg\| \frac{1}{\mu_p C_{ox}\left[\frac{W}{L}\right]_p (|V_{GSp}| - |V_{tp}|)}$$

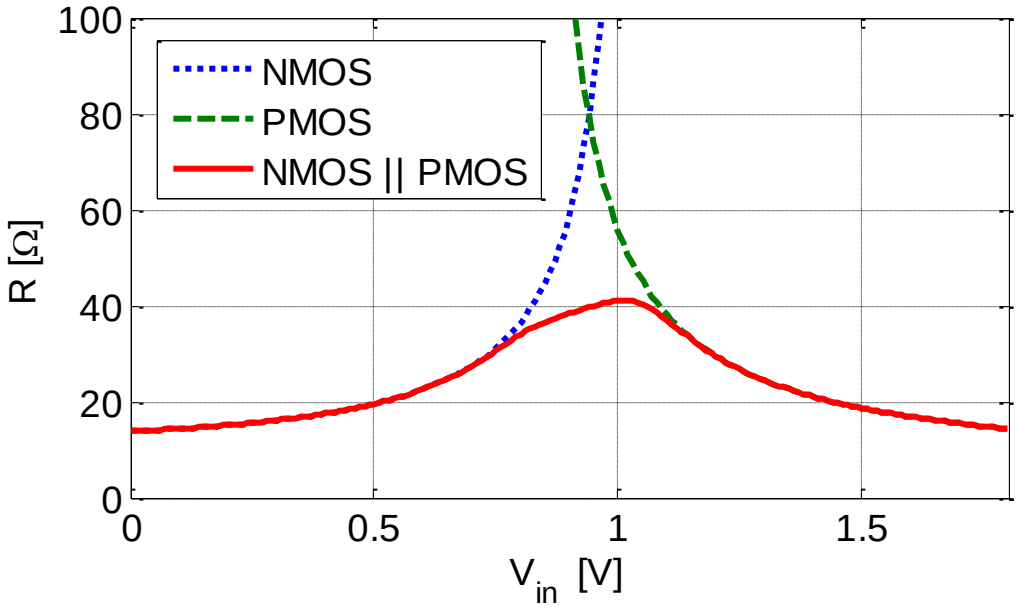
$$R \cong \frac{1}{\mu_n C_{ox}\left[\frac{W}{L}\right]_n (V_{DD} - V_{tn}) - \left(\mu_n C_{ox}\left[\frac{W}{L}\right]_n - \mu_p C_{ox}\left[\frac{W}{L}\right]_p\right) v_{in} - \mu_p C_{ox}\left[\frac{W}{L}\right]_p |V_{tp}|}$$

$$R \cong \frac{1}{\mu_n C_{ox}\left[\frac{W}{L}\right]_n (V_{DD} - V_{tn} - |V_{tp}|)} \quad if \quad \mu_n \left[\frac{W}{L}\right]_n = \mu_p \left[\frac{W}{L}\right]_p$$

- Independent of V_{in} → too good to be true!
- Missing factors:
  - Backgate effect
  - Short channel effects

Real CMOS Switch





- Design
  - Size P/N ratio to minimize change in R over input range
  - Size P and N simultaneously to meet distortion specs
- PMOS brings limited benefit unless the input signal range is large or centered near $V_{DD}/2$

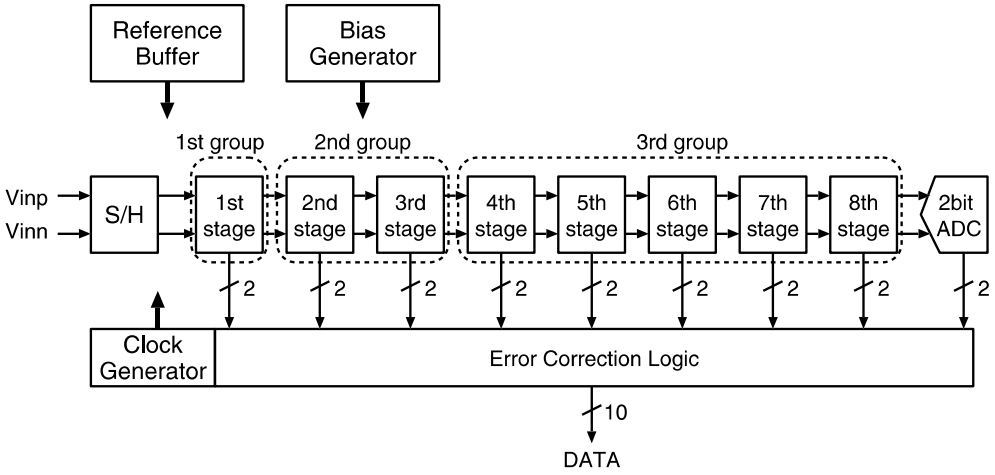
EE 240C
Analog-Digital Interface Integrated Circuits

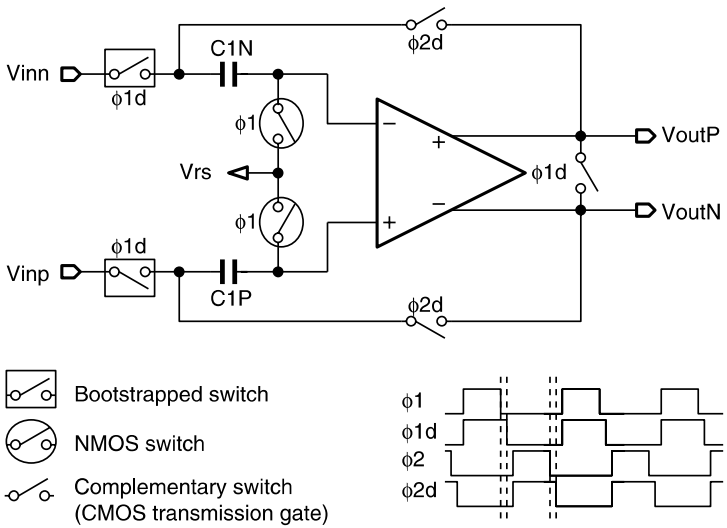
Track & Hold Amplifier – Bootstrapping

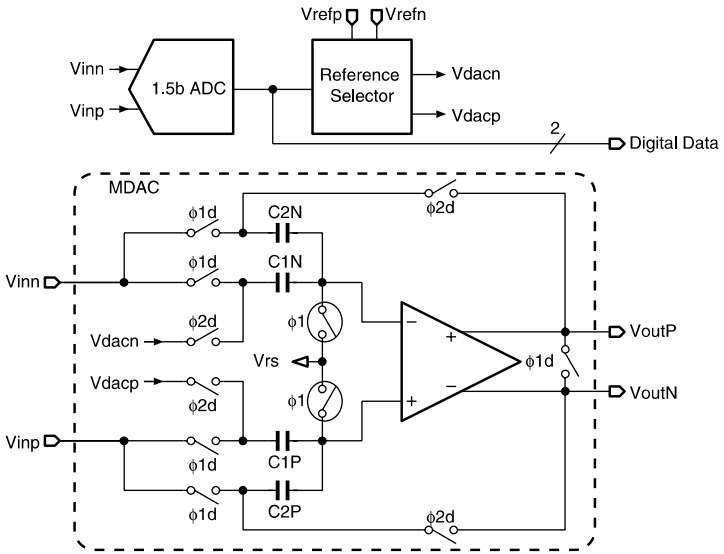
Outline

- Elementary track-and-hold circuit and its nonidealities
- First order improvements to elementary track-and-hold
- Advanced techniques
  - Clock bootstrapping
  - Bottom plate sampling
- Settling and noise analysis in charge-redistribution track-and-hold circuit
- Noise simulation example

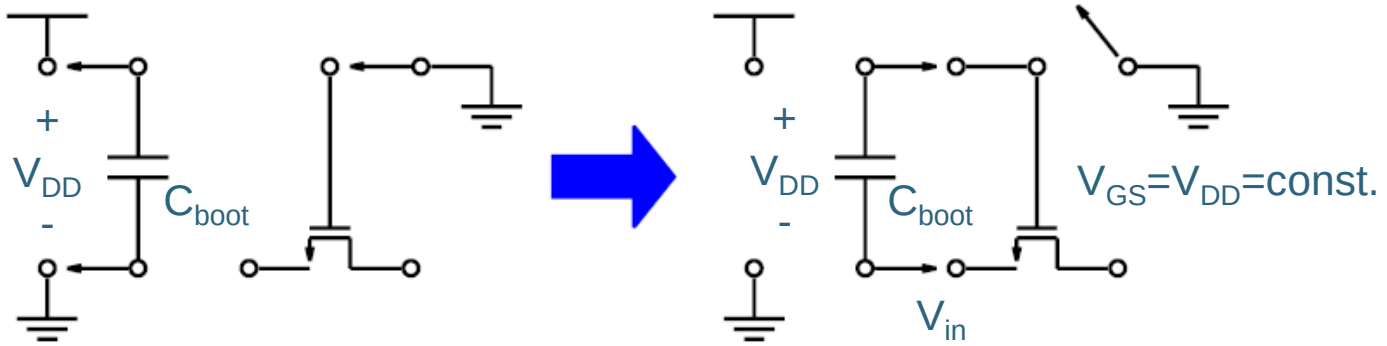
SHA / Pipelined Stage Example







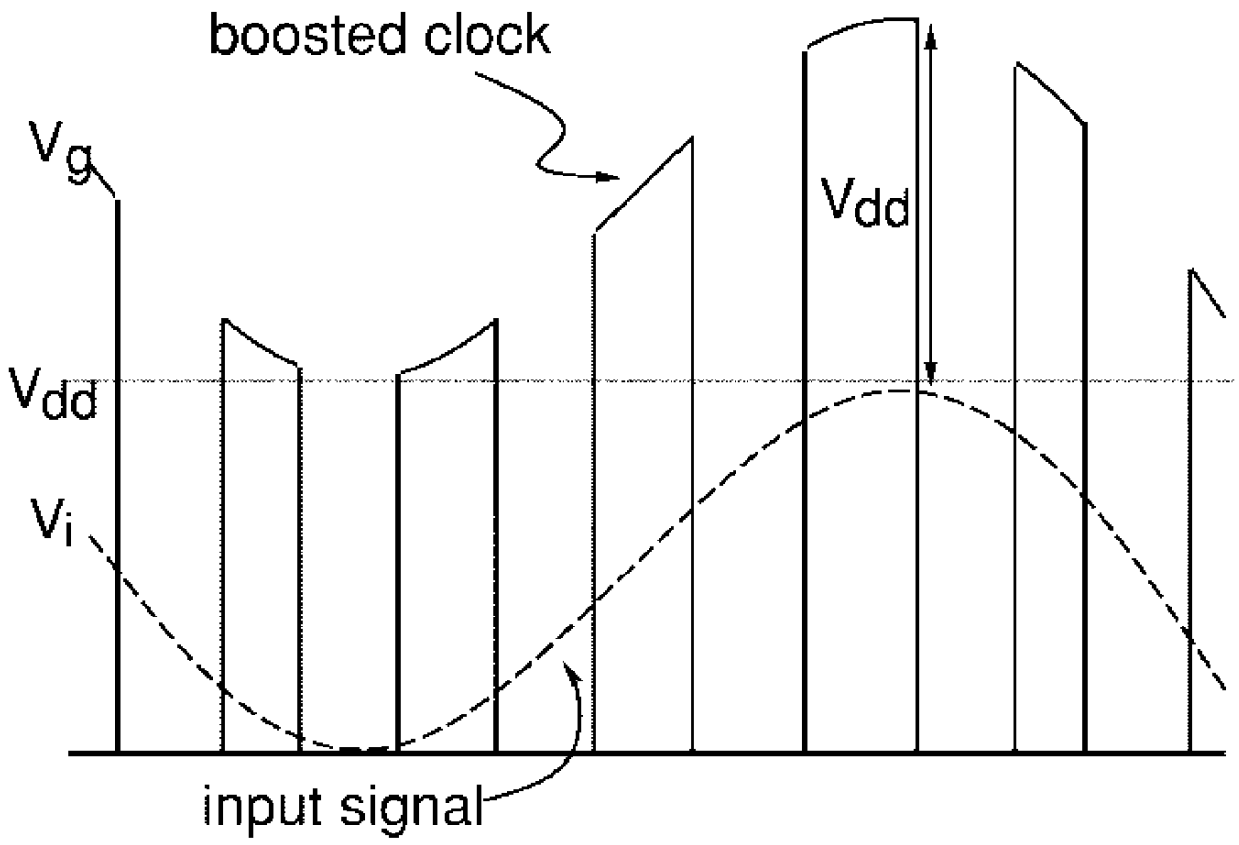
Clock Bootstrapping

- 

A. Abo, "Design for Reliability of Low-voltage, Switched-capacitor Circuits," PhD Thesis, UC Berkeley, 1999.

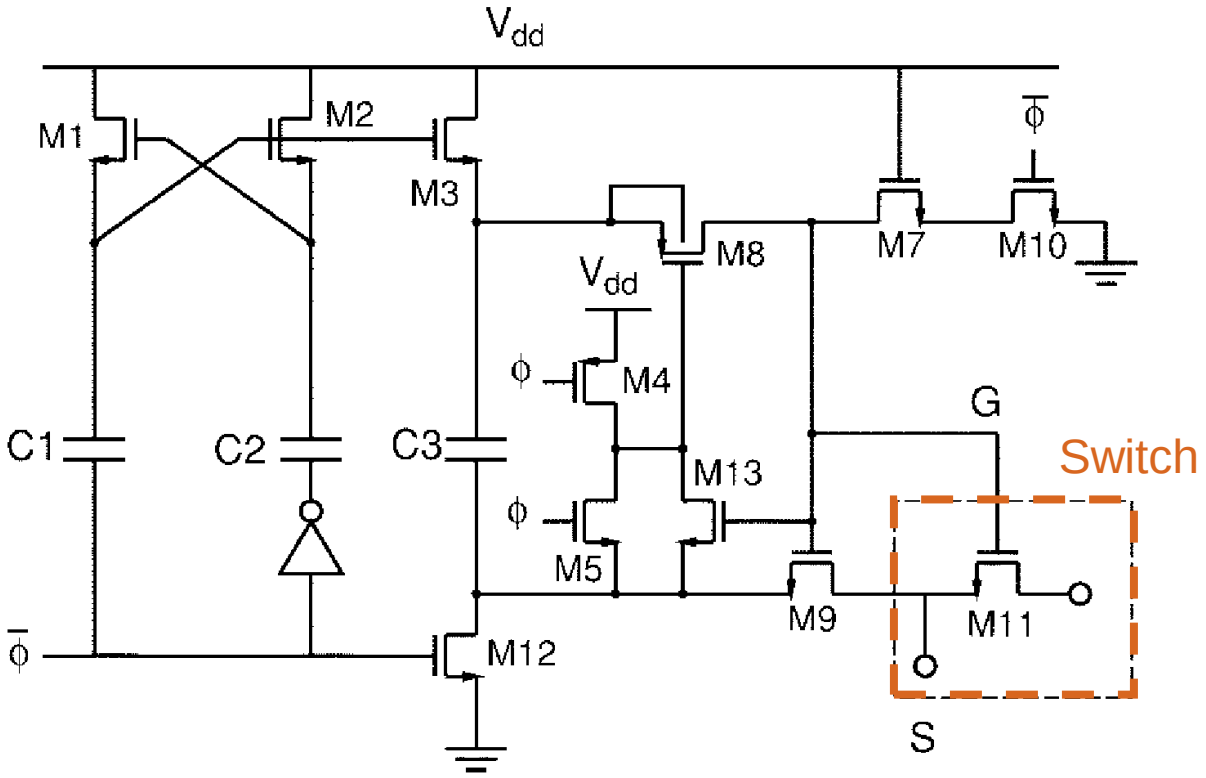
- Phase 1
  - C_{boot} is precharged to V_{DD}
  - Sampling switch is off
- Phase 2
  - Sampling switch is on with $V_{GS}=V_{DD}$=const.
  - To first order, both R_{on} and channel charge are signal independent

Waveforms



A. Abo, "Design for Reliability of Low-voltage, Switched-capacitor Circuits," PhD Thesis, UC Berkeley, 1999.

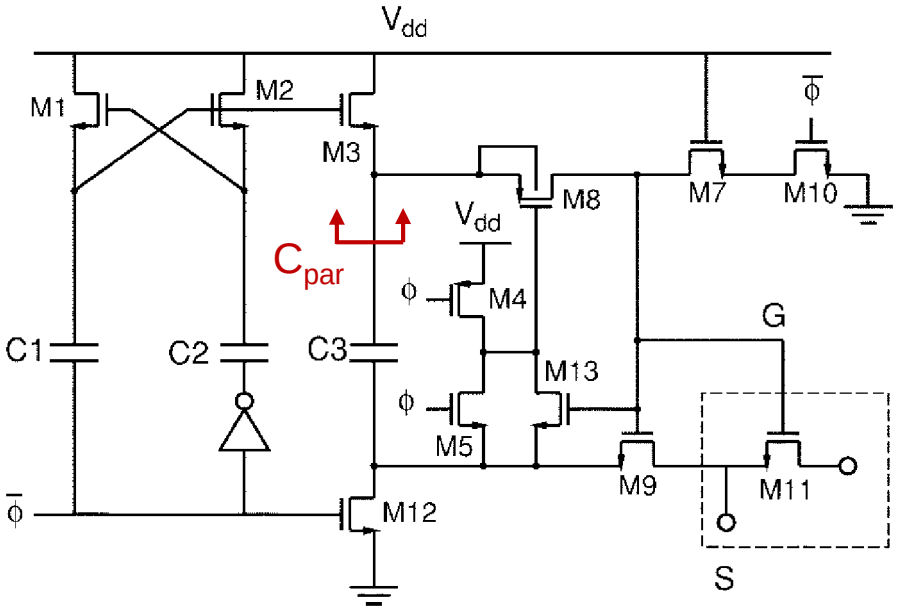
Circuit Implementation



A. Abo et al., "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," IEEE J. Solid-State Circuits, pp. 599, May 1999

Limitations

- Efficacy of bootstrap circuit is reduced by
  - Backgate effect
  - Parasitic capacitance C_{par} at top plate of C_3=C_{boot}
- Charge conservation:
  $C_{boot}\ V_{DD}$
  $= C_{boot}\ V_{GS,switch}$
  $+ C_{par}\ (V_{GS,switch} + V_{in})$



$$R \cong \frac{1}{\mu_n C_{ox}\left[\frac{W}{L}\right]_n\left(\frac{C_{\text{boot}}}{C_{\text{boot}}+C_{\text{par}}}V_{DD} - \frac{C_{\text{par}}}{C_{\text{boot}}+C_{\text{par}}}V_{\text{in}} - \underbrace{V_{tn}[V_{\text{in}}]}_{\text{Backgate effect}}\right)}$$

Alternative Implementation

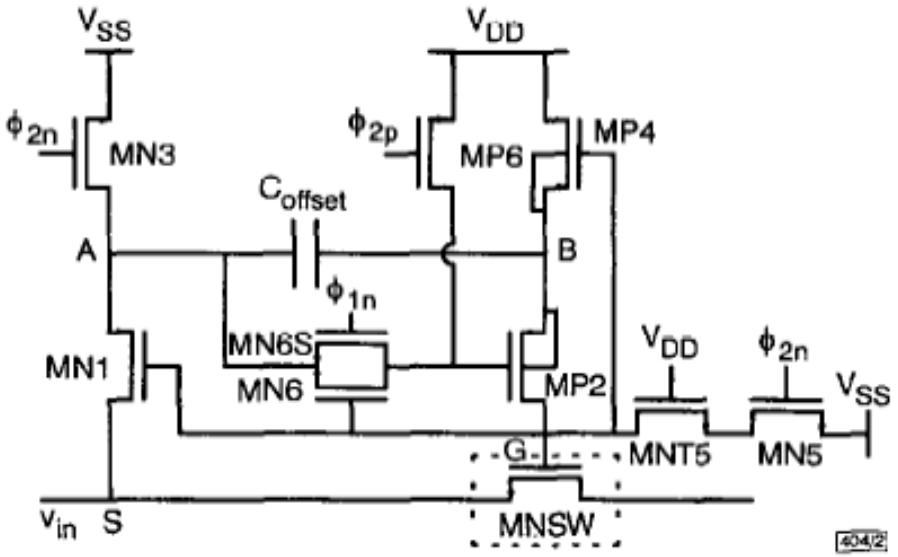


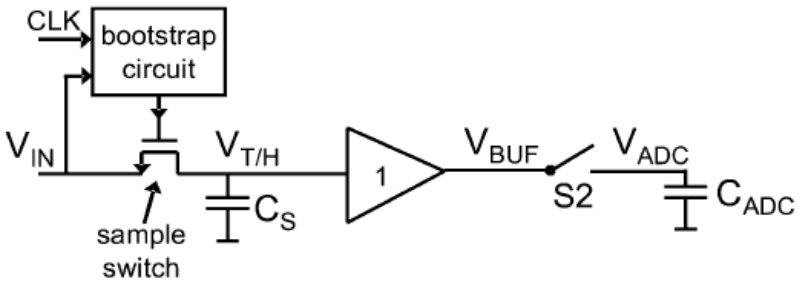
Fig. 2 *Proposed implementation*

Dessouky and Kaiser, "Input switch configuration suitable for rail-to-rail operation of switched opamp circuits," Electronics Letters, Jan. 1999.

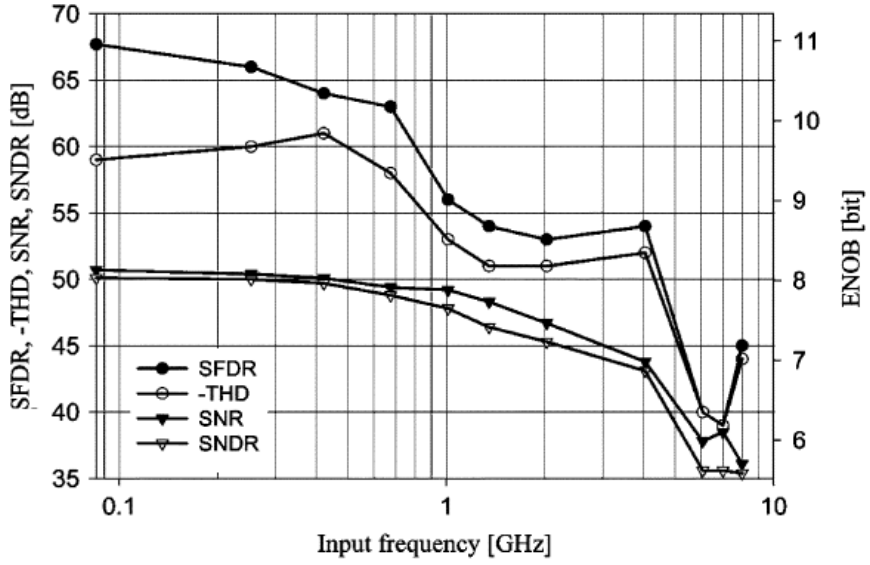
- Less complex, but C_{par} tends to be larger due to two parasitic well capacitances

Performance of Bootstrapped Samplers

- Bootstrapped "top plate" sampling works well up to ~10bit resolution
- Use "bottom plate sampling" for higher resolution (see later)
- Example



[Louwsma, JSSC 4/2008]



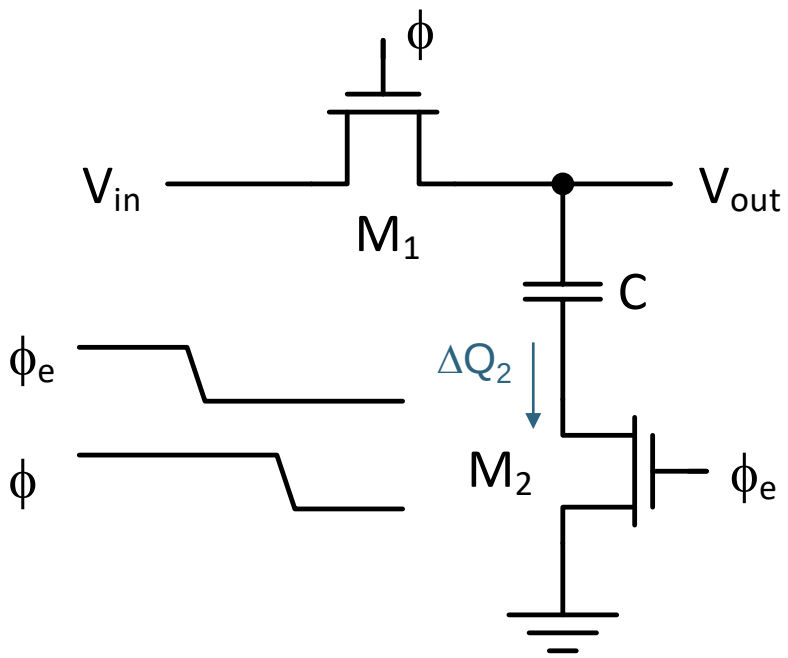
EE 240C
Analog-Digital Interface Integrated Circuits

Track & Hold Amp – Bottom Plate Sampling

Bottom Plate Sampling

- What if we want to do much better, e.g. 16 bits?
- Basic idea
  - Make "switched" voltage (V_{in}?) constant …
  - How? Sample signal at the "grounded" side of the capacitor to achieve signal independent sampling
- References
  - D. J. Allstot and W. C. Black, Jr., "Technological Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems," Proc. IEEE, pp. 967-986, Aug. 1983.
  - K.-L. Lee and R. G. Meyer, "Low-Distortion Switched-Capacitor Filter Design Techniques," IEEE J. Solid-State Circuits, pp. 1103-1113, Dec. 1985.
- First look at single ended half circuit for simplicity

Bottom Plate Sampling Analysis (1)



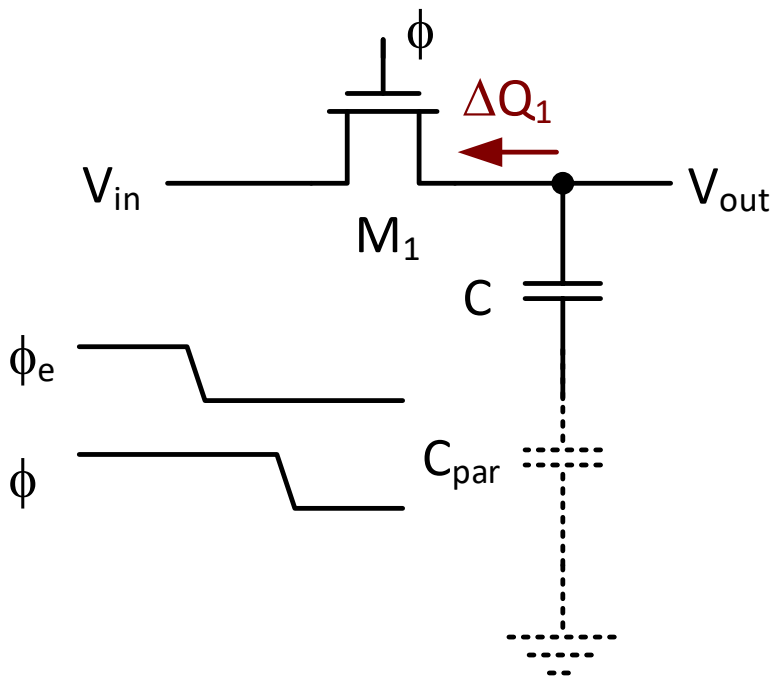
- Turn M_2 off "slightly" before M_1
  - Typically few hundred ps delay between falling edges of ϕ_e and ϕ
- During turn off, M_2 injects charge

$$\Delta Q_2 \cong \frac{1}{2} WLC_{ox}(\phi_H - V_{tn})$$

- To first order, the charge injected by M_2 is signal independent
- Voltage across C

$$V_C = V_{\text{in}} + \frac{\Delta Q_2}{C}$$

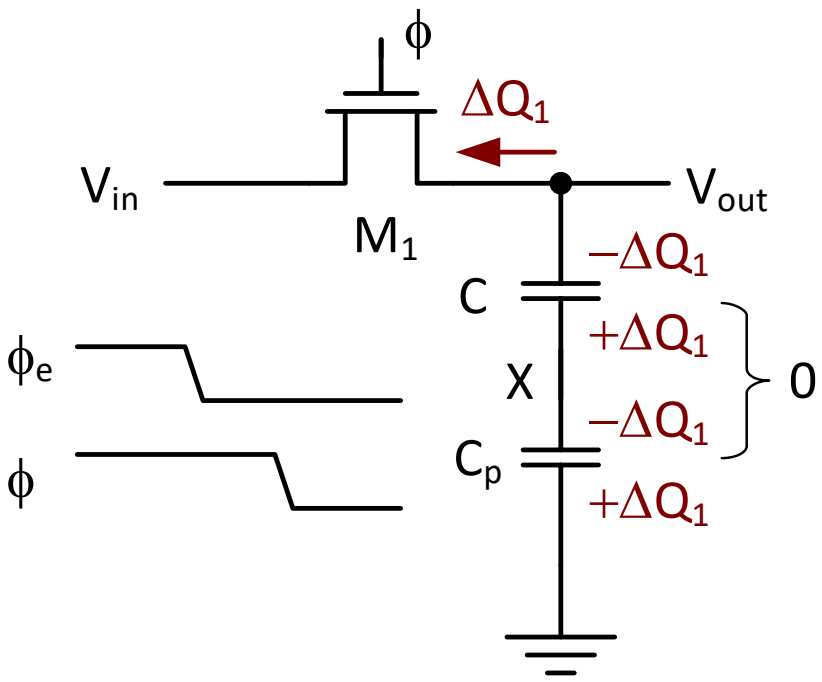
Bottom Plate Sampling Analysis (2)



$$\Delta Q_1 \cong \frac{1}{2} WLC_{ox}(\phi_H - V_{\text{in}} - V_{tn})$$

- Next, turn off M1
- M1 will inject signal dependent charge onto the series combination of C and the parasitic capacitance at its bottom plate (C_{par})
- Looks like, this is not much different from the conventional top-plate sampling?
  - But wait…

Bottom Plate Sampling Analysis (3)

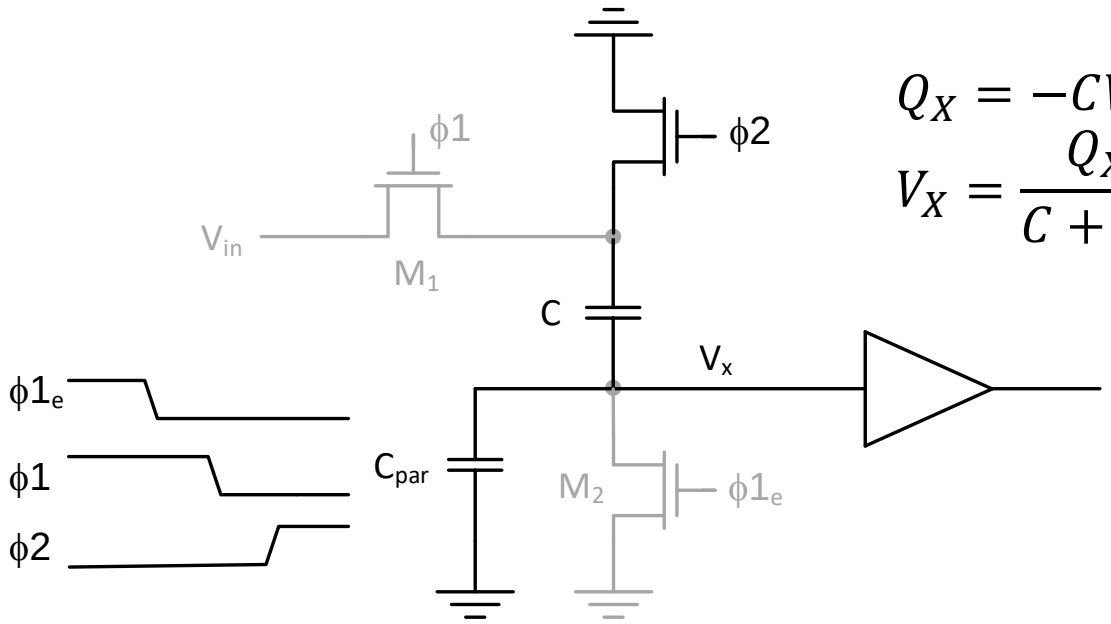


$$Q_X = -CV_{\text{in}} - \Delta Q_2$$

Charge injected by M2
(Signal independent)

- Interesting observation
  - Even though M1 injects some charge, the total charge at node X cannot change!
- Idea
  - Process total charge at node X instead of voltage across C
- The charge can be processed in two ways
  - Open-loop
  - Closed-loop (charge redistribution)

Open-Loop Charge Processing



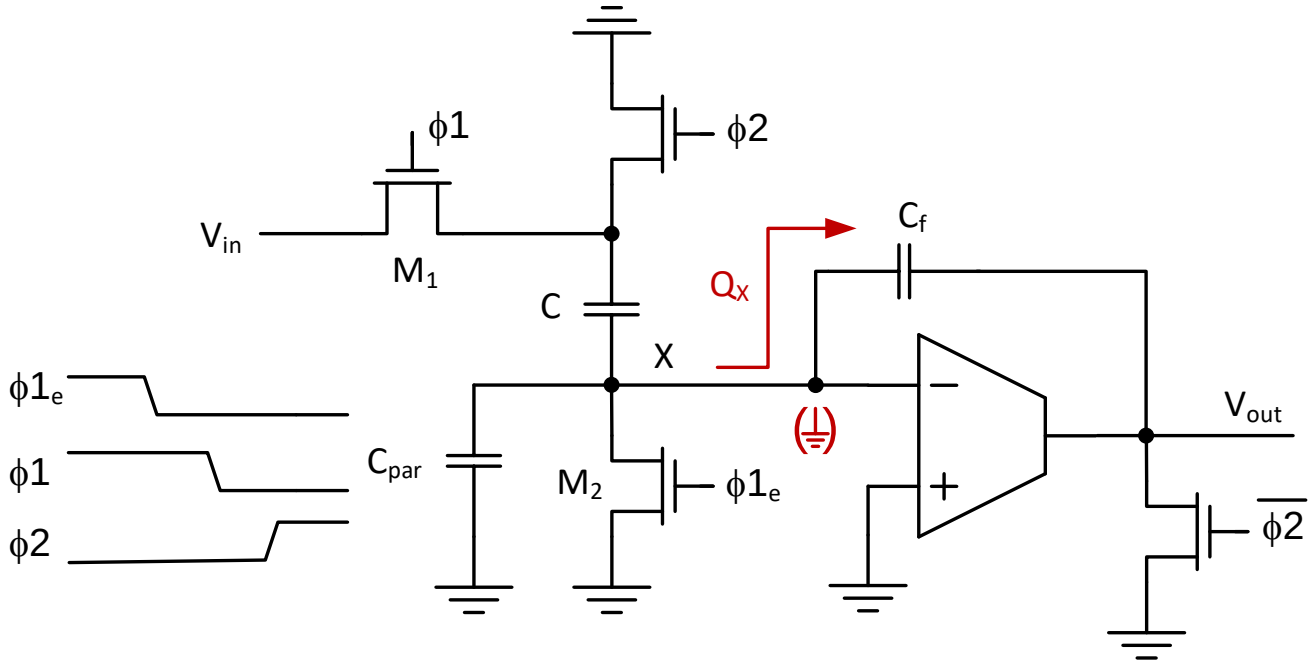
$$Q_X = -CV_{in} - \Delta Q_2$$

$$V_X = \frac{Q_X}{C + C_p} = -V_{in}\frac{C}{C + C_p} - \frac{\Delta Q_2}{C + C_p}$$

(no term due to signal dependent charge!)

- Remaining drawback
  - C_{par} (and buffer input capacitance) is usually weakly nonlinear and will introduce some harmonic distortion

Closed-Loop Charge Processing



- Amplifier forces voltage at node X to "zero"
  - Means that charge at node X must redistribute onto feedback capacitor C_f

Charge Conservation Analysis

Charge at node X during $\phi 1$: $Q_{X1} = -CV_{\text{in}} - \Delta Q_2 + 0 \cdot C_f$

Charge at node X during $\phi 2$: $Q_{X2} = -C_f V_{\text{out}}$

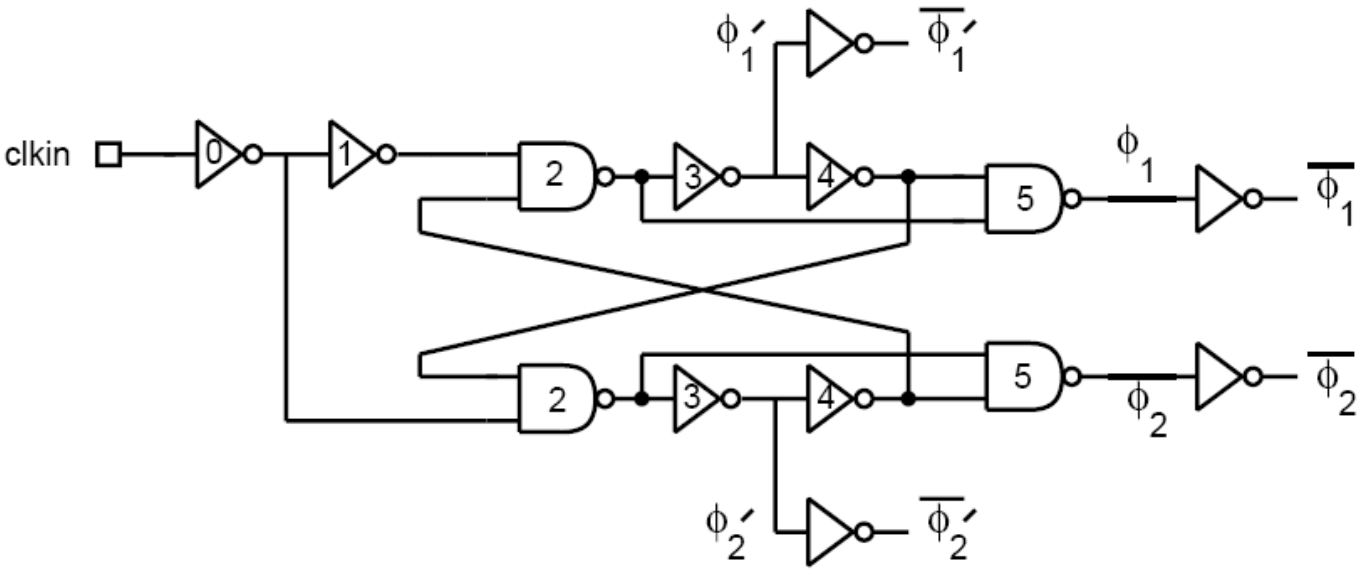
Charge Conservation:

$$Q_{X1} = Q_{X2}$$
$$-CV_{\text{in}} - \Delta Q_2 = -C_f V_{\text{out}}$$

$$\therefore V_{\text{out}} = \frac{C}{C_f} V_{\text{in}} + \frac{\Delta Q_2}{C_f}$$

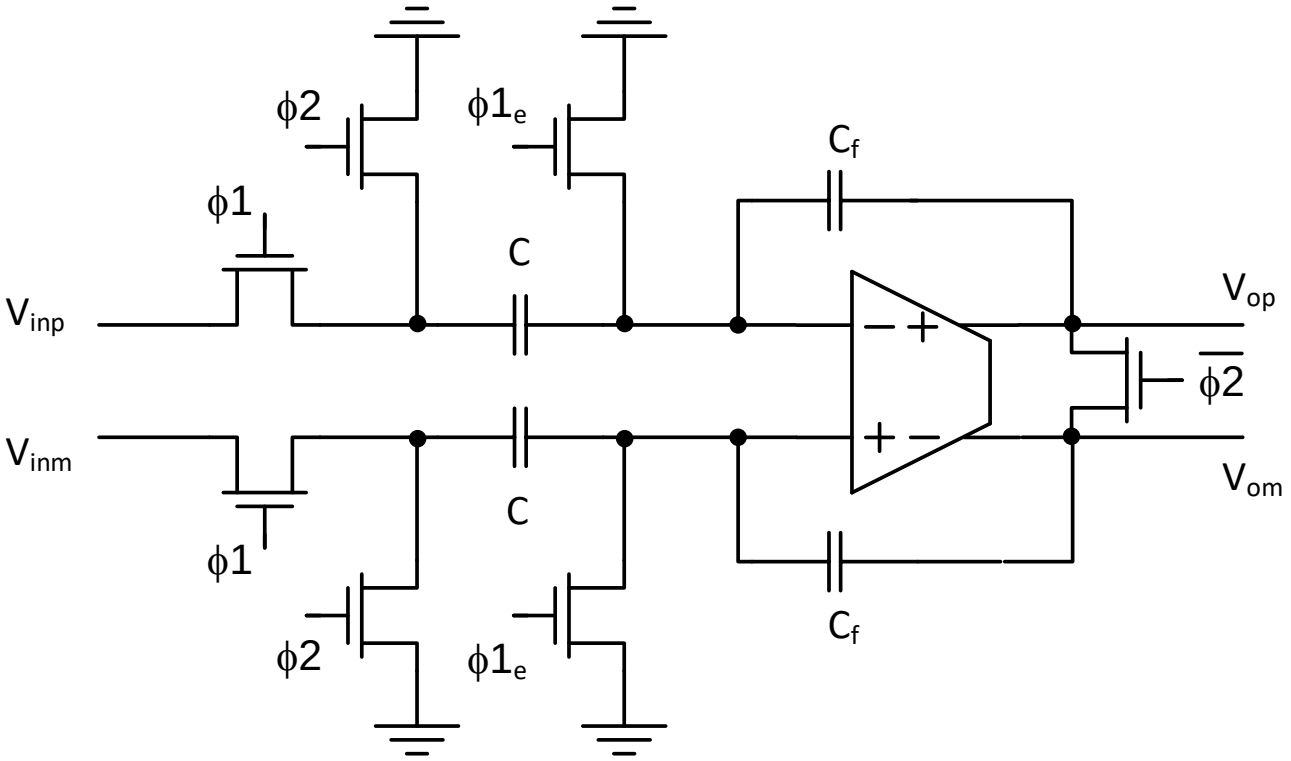
- No gain error
- Offset term due to signal independent injection from M2 can be easily removed using a differential architecture

Clock Generation



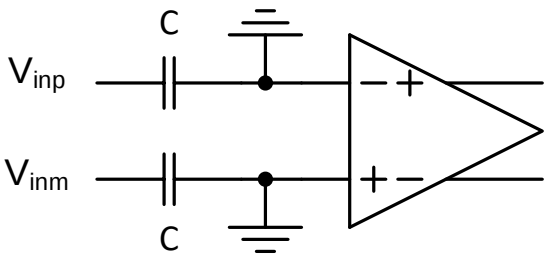
[A. Abo, "Design for Reliability of Low-voltage, Switched-capacitor Circuits," PhD Thesis, UC Berkeley, 1999]

Fully Differential Circuit

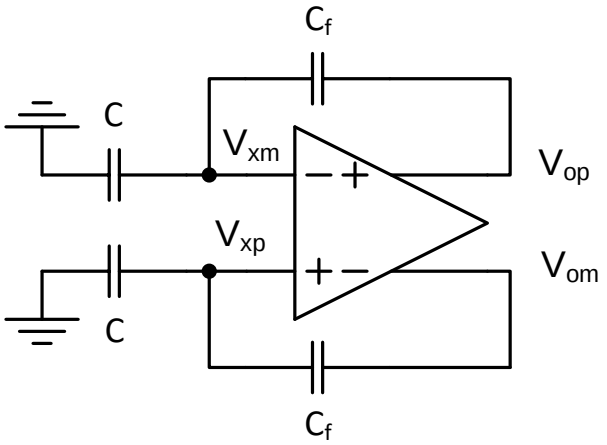


Analysis (1)

During $\phi 1$



During $\phi 2$



$$Q_{1m} = -CV_{inp} + \Delta Q$$

$$Q_{1p} = -CV_{inm} + \Delta Q$$

$$Q_{2m} = CV_{xm} - C_f\left(V_{op} - V_{xm}\right)$$

$$Q_{2p} = CV_{xp} - C_f\left(V_{om} - V_{xp}\right)$$

1) $Q_{1m} = Q_{2m}$ $\quad V_{xm} = V_{xp}$ $\quad \dfrac{V_{op} + V_{om}}{2} = V_{oc}$

2) $Q_{1p} = Q_{2p}$

Analysis (2)

- Subtracting 1) and 2) yields

$$V_{op} - V_{om} = \frac{C}{C_f}\left(V_{inp} - V_{inm}\right)$$

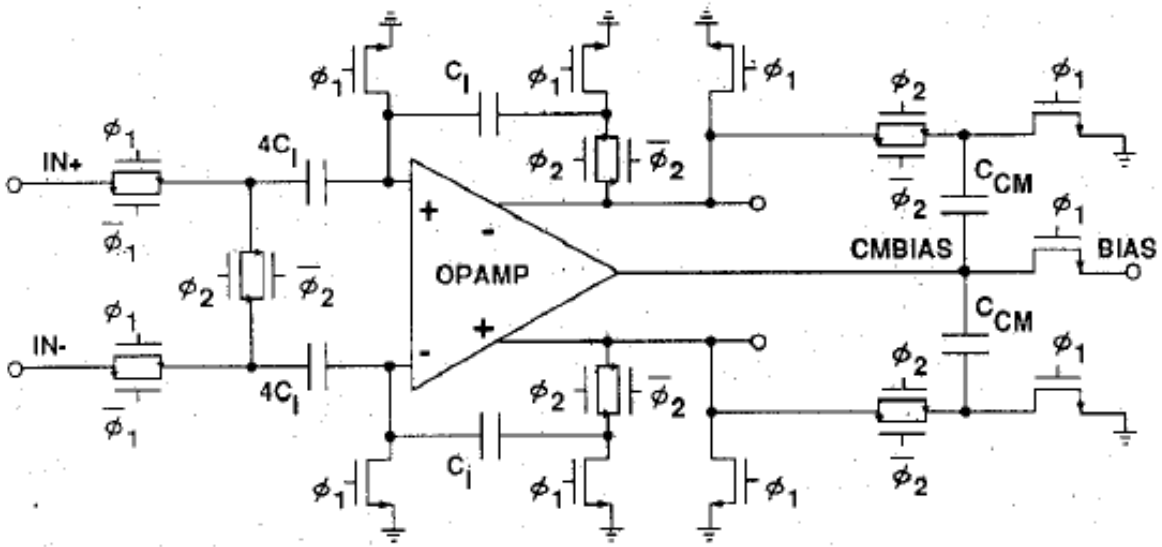
- Adding 1) and 2) yields

$$-C\left(V_{inp} + V_{inm}\right) + 2\Delta Q = \left(C + C_f\right)\left(V_{xp} + V_{xm}\right) - C_f\left(V_{op} + V_{op}\right)$$

$$V_{xc} = \frac{\Delta Q}{C + C_f} + \frac{C_f}{C + C_f} V_{oc} - \frac{C}{C + C_f} V_{ic}$$

- Variations in V_{ic} show up as common mode variations at the amplifier input
  - Need amplifier with good CMRR

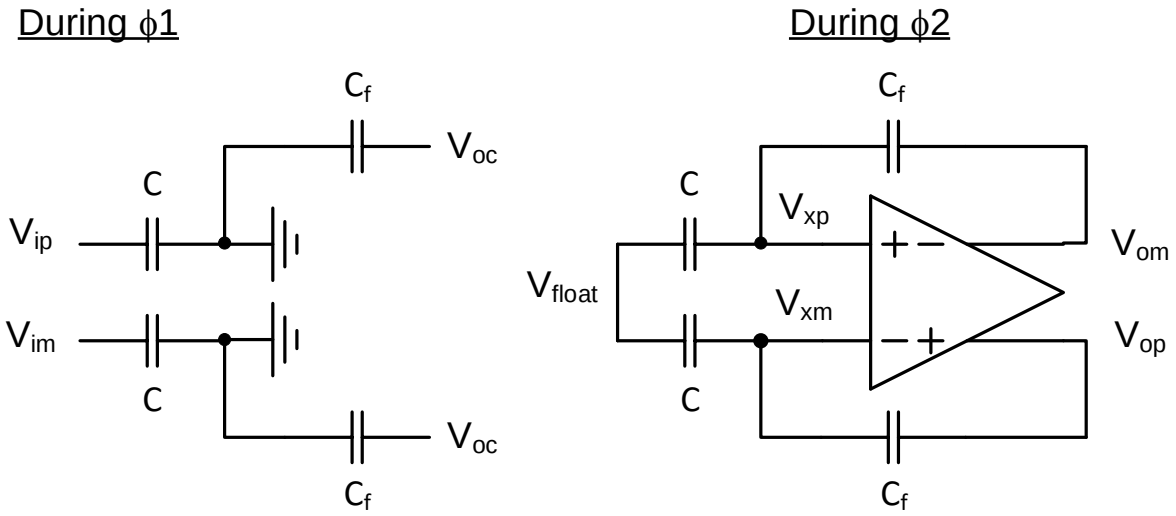
T/H with Common Mode Cancellation



S.H. Lewis & P.R. Gray, "A Pipelined 5 MSample/s 9-bit Analog-to-Digital Converter", IEEE J. Solid-State Circuits, pp. 954-961, Dec. 1987

- Shorting switch allows to re-distribute only differential charge on sampling capacitors
- Common mode at OPAMP input becomes independent of common mode at circuit input terminals (IN+/IN-)
- Original idea: Yen & Gray, JSSC 12/1982

Analysis (1)



- Charge conservation at Vip,Vim and Vfloat

$$(V_{ip} + V_{im}) \cdot C = (V_{float} - V_{xp}) \cdot C + (V_{float} - V_{xm}) \cdot C$$

$$V_{ic} = V_{float} - V_{xc}$$

$$V_{float} = V_{ic} + V_{xc}$$

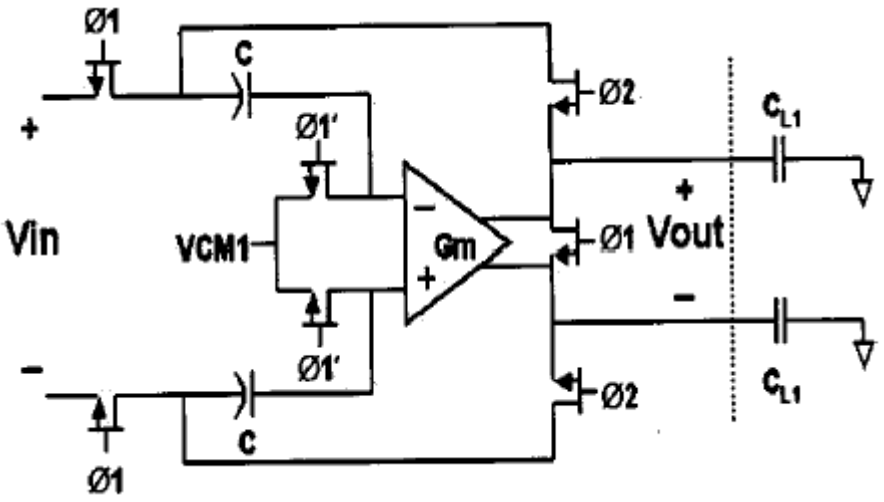
Analysis (2)

- Common mode charge conservation at amplifier inputs

$$-V_{ic} \cdot C - V_{oc} \cdot C_f = -\left(V_{float} - V_{xc}\right) \cdot C - (V_{oc} - V_{xc}) \cdot C_f$$
$$-V_{ic} \cdot C = -([V_{ic} + V_{xc}] - V_{xc}) \cdot C + V_{xc} \cdot C_f$$
$$0 = V_{xc}$$

- Amplifier input common mode (V_{xc}) is independent of
  - Input common mode (V_{ic})
  - Output common mode (V_{oc})

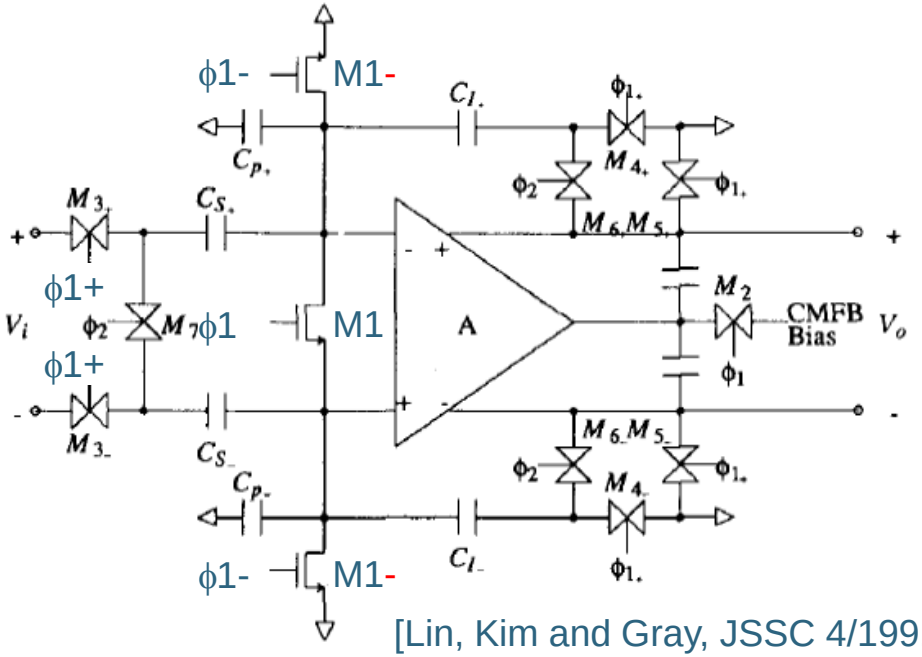
Flip-Around T/H



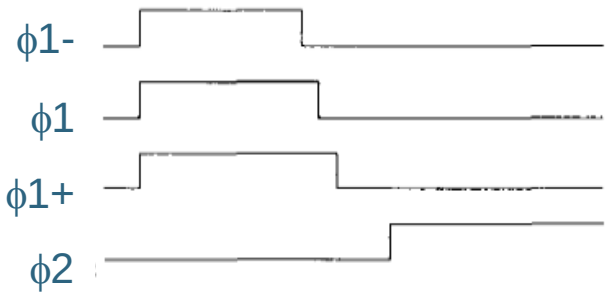
[W. Yang et al., "A 3-V 340-mW 14-b 75-MSample/s CMOS ADC With 85-dB SFDR at Nyquist Input", IEEE J. Solid-State Circuits, pp. 1931-1936, Dec. 2001]

- Sampling caps are "flipped around" OTA and used as feedback capacitors during ϕ_2
- Main advantage: improved feedback factor (lower noise, higher speed)
- Main disadvantage: OTA input common mode variations

Sampling Network Design Considerations

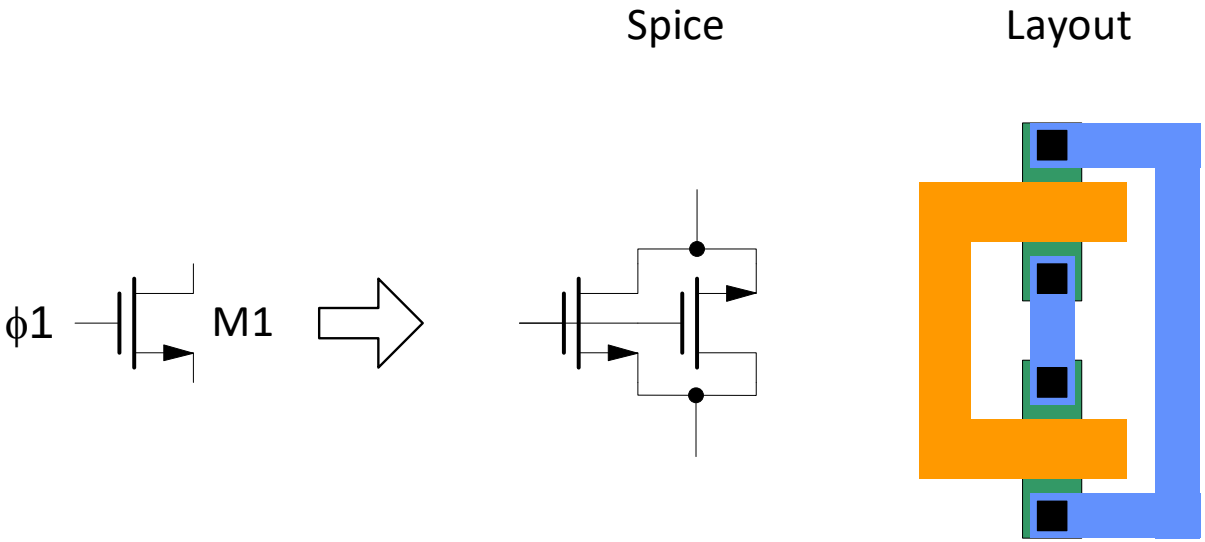


[Lin, Kim and Gray, JSSC 4/1991]



- M1– switches only needed to set common mode; M1 is actual sampling switch
  - Make M1 larger than M1–
- Ideally turn off M1– before M1
  - In practice, usually OK to turn off simultaneously
- In track mode, the total path resistance is R(M3) plus bottom plate switch resistance
  - Since R(M3) is signal dependent, make its resistance small compared to that of bottom plate network

Schematic Entry and Layout of M1



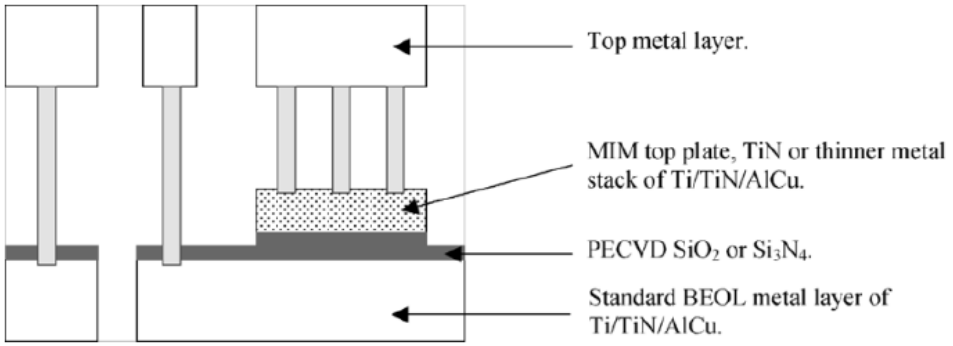
- Use antiparallel devices to implement M1
  - Needed in simulation to guarantee circuit symmetry
    - E.g. BSIM model is not necessarily perfectly symmetric with respect to drain/source!
  - Needed in layout to ensure symmetry in presence of drain/source asymmetry due to processing artifacts

What Ultimately Limits Linearity?

- Track mode nonlinearity due to R=f(Vin)
  - Mitigate using clock bootstrapping and proper partitioning of total path resistance
  - Eventually, bootstrapping falls apart at high frequencies, due to parasitic capacitances inside the bootstrap circuit
- Mismatch in half-circuit charge injection due to R=f(Vin)
  - Bottom plate switches in the two half circuits see input dependent impedance; this creates input dependent charge injection mismatch
  - Bootstrapping helps; ultimately limited by backgate effect
  - This effect is often fairly independent of frequency (somewhat dependent on realization of top plate switch)
- In high performance designs, can achieve ~80-100dB linearity up to a few hundreds of MHz

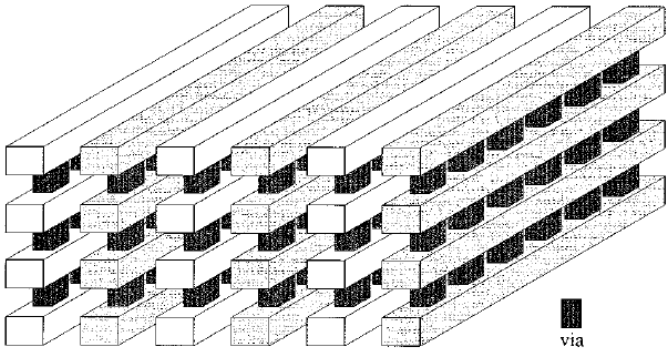
Capacitors

Metal-Insulator-Metal (MIM)



[Ng, Trans. Electron Dev., 7/2005]

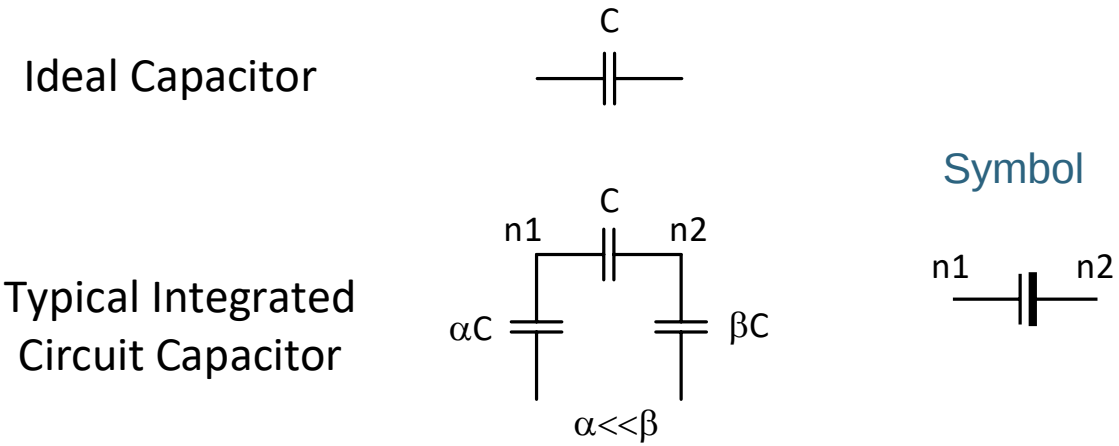
Vertical Parallel Plate (VPP)



[Aparicio, JSSC 3/2002]

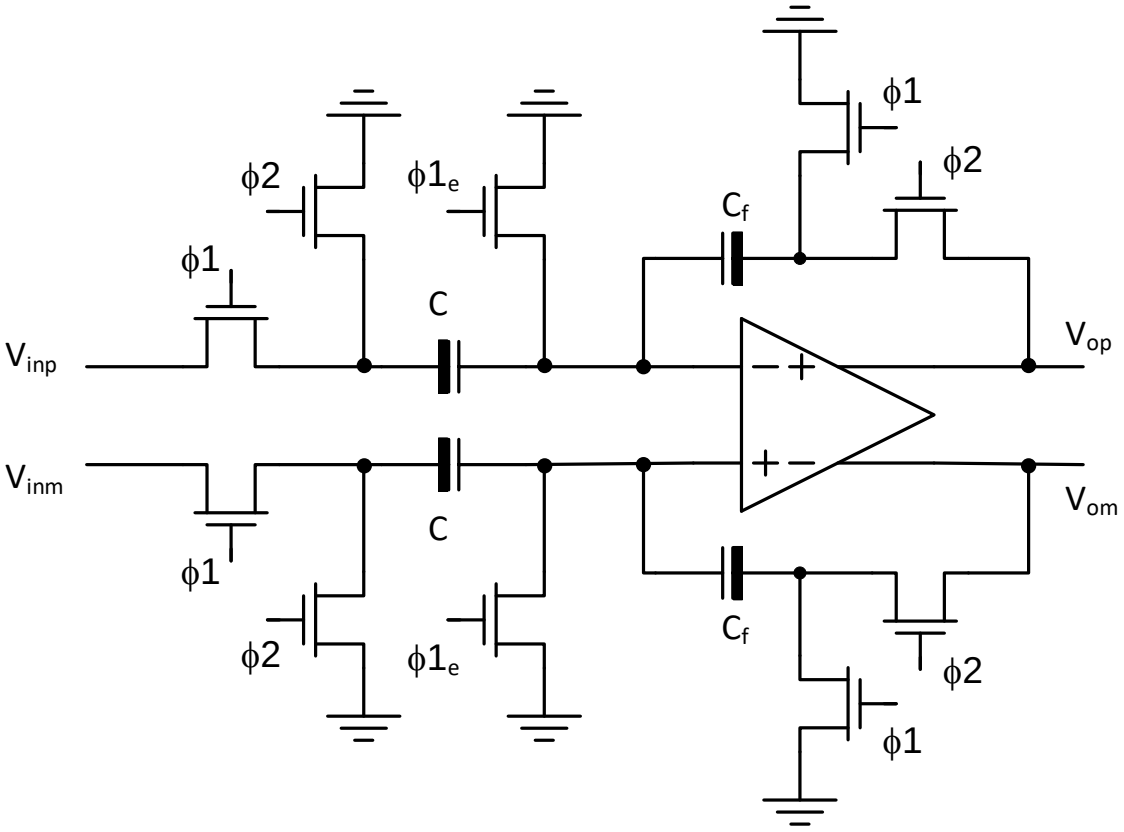
- Typically 1-2 fF/mm2 (10-20 fF/mm2 for advanced structures)
  - For 1 fF/mm2, a 10 pF capacitor occupies ~100mm x 100mm
- Both MIM and VPP capacitors have good electrical properties
  - Mostly worry about parasitic caps
  - Series and parallel resistances are often not a concern

Plate Parasitics



- Node n1 is usually the "physical" top plate of the capacitor
  - Makes nomenclature very confusing, since this plate is typically used as the "electrical" bottom plate in a sampling circuit (in the context of "bottom plate sampling")
- Typical values for a MIM capacitor
  - a=1%, b=10%

Proper Connection of Capacitors



- "Fat plate" is oriented away from virtual ground nodes to avoid reduction of feedback factor and reduce noise gain and interference

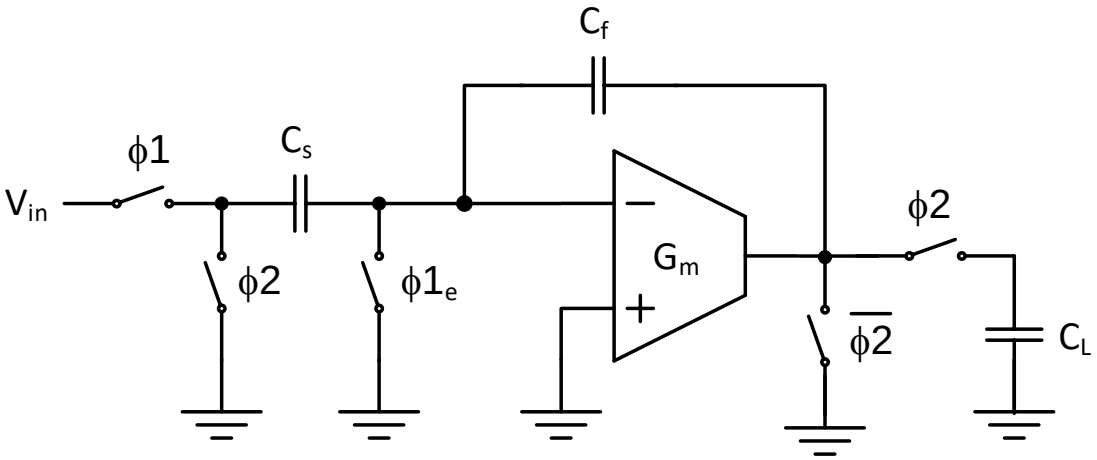
EE 240C
Analog-Digital Interface Integrated Circuits

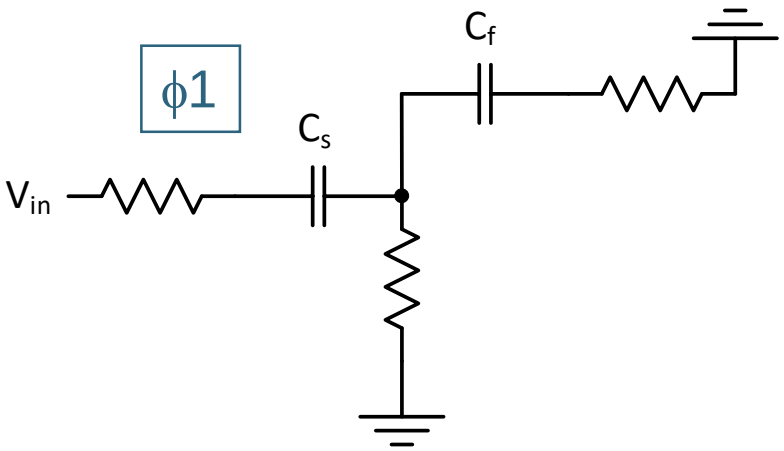
Track & Hold Amp – Settling

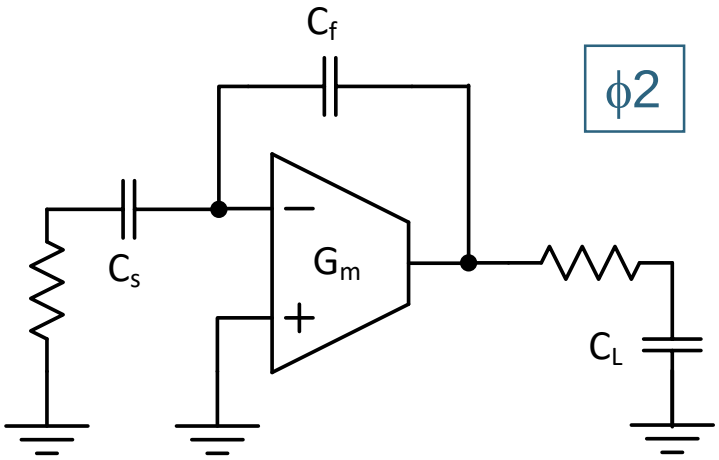
Outline

- Elementary track-and-hold circuit and its nonidealities
- First order improvements to elementary track-and-hold
- Advanced techniques
  - Clock bootstrapping
  - Bottom plate sampling
- Settling and noise analysis in charge-redistribution track-and-hold circuit
- Noise simulation example

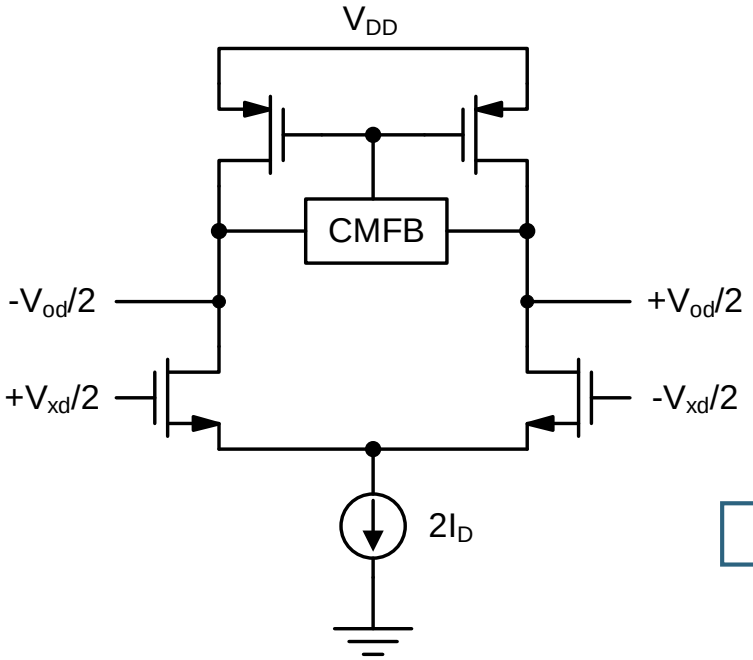
Settling and Noise Analysis

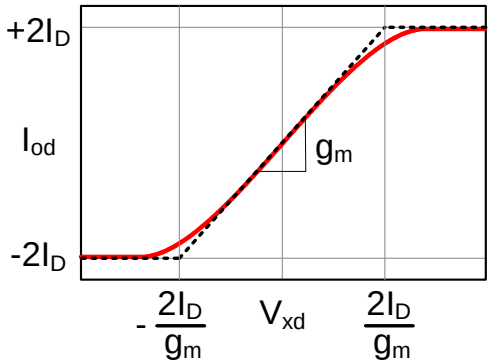




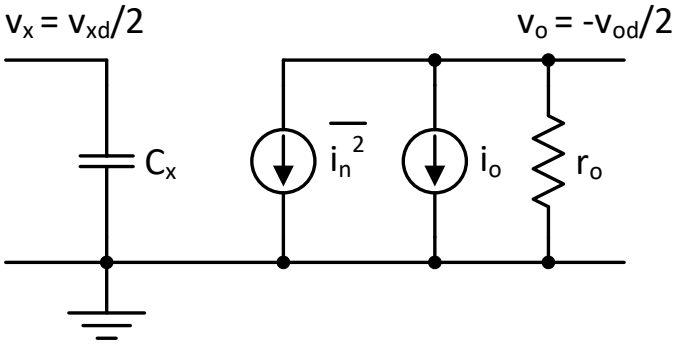


First Order Amplifier Model



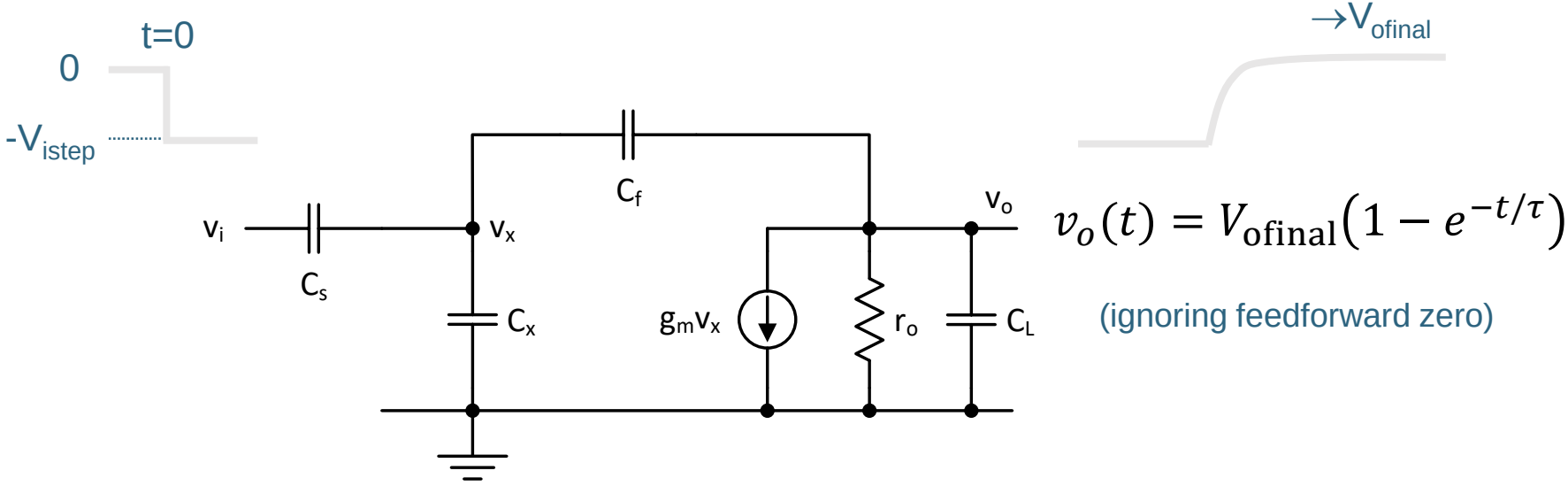


Piecewise linear half-circuit



$$i_o = \begin{cases} g_m v_x & \text{for} \quad |g_m v_x| < I_D \\ I_D \cdot \text{sign}(v_x) & \text{else} \end{cases}$$

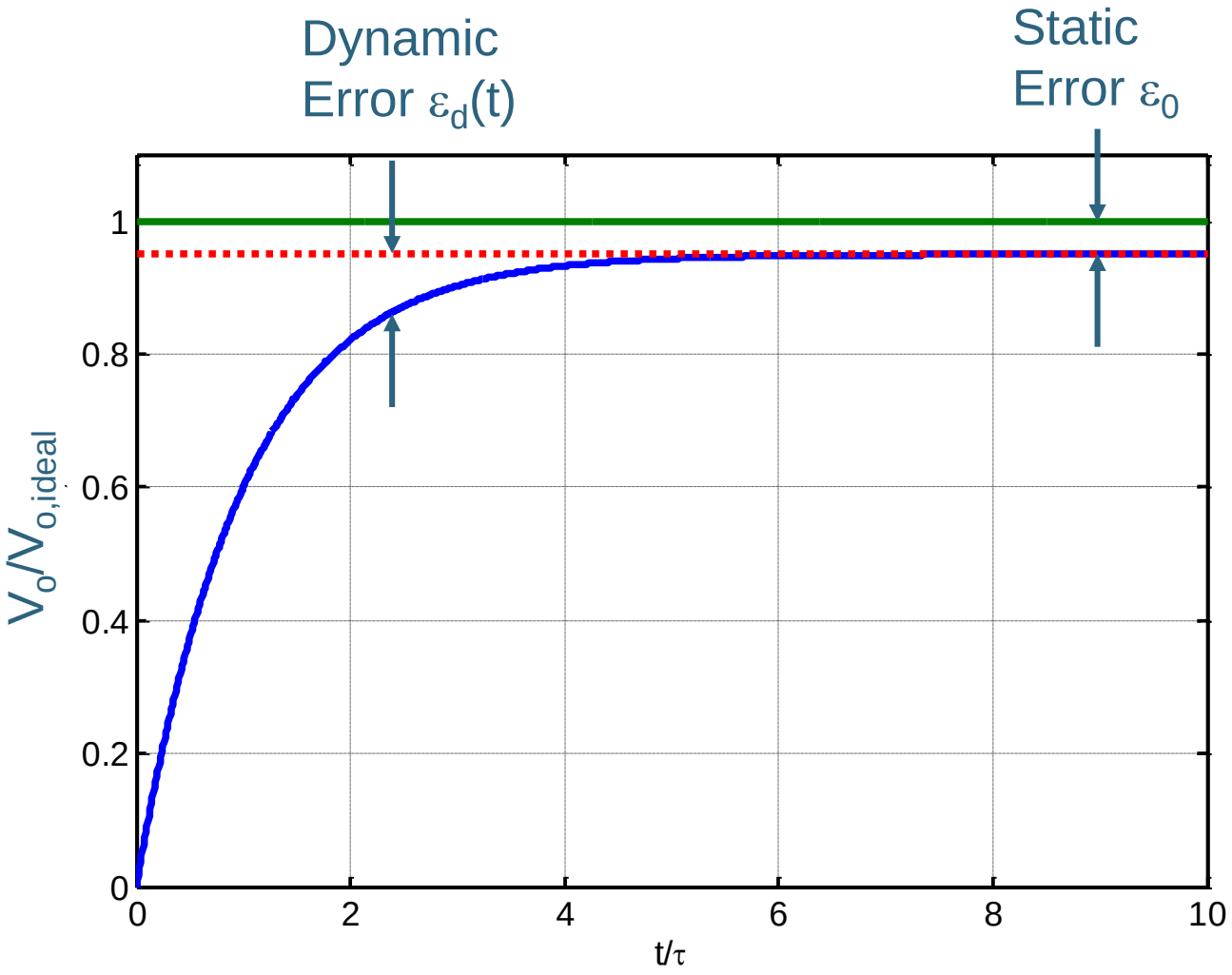
Linear Settling (Small Input Step)



- Important parameter: Return factor or "feedback factor" β

$$\beta = \frac{C_f}{C_f + C_s + C_x}$$

Waveform Detail



Static Settling Error

- Ideal output voltage for t→∞ $$V_{\text{ofinal,ideal}} = V_{\text{istep}} \cdot \frac{C_s}{C_f}$$

- Actual output voltage (from detailed analysis)

$$V_{\text{ofinal}} = V_{\text{istep}} \cdot \frac{C_s}{C_f} \cdot \frac{T_0}{1+T_0} \qquad T_0 = \beta \cdot g_m r_o = \beta \cdot a_{vo}$$

- Define static settling error

$$\varepsilon_0 = \frac{V_{\text{ofinal}} - V_{\text{ofinal,ideal}}}{V_{\text{ofinal,ideal}}} = \frac{\frac{T_0}{1+T_0} - 1}{1} = -\frac{1}{1+T_0} \cong -\frac{1}{T_0}$$

- Example: T_0=1000 → 0.1% static settling error

Dynamic Settling Error

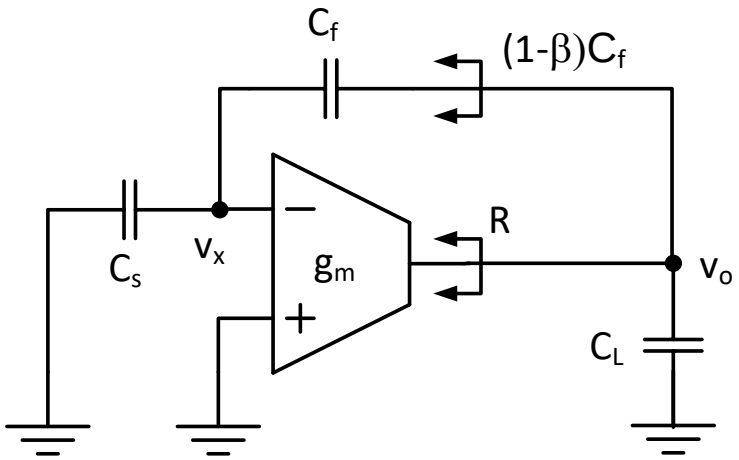
$$\varepsilon_{\text{dynamic}}(t) = \frac{v_{\text{o}}(t) - V_{\text{ofinal}}}{V_{ofinal}} = \frac{V_{\text{ofinal}}\left(1 - e^{-t/\tau}\right) - V_{\text{ofinal}}}{V_{\text{ofinal}}} = -e^{-t/\tau}$$

$$N = \frac{t_s}{\tau} = -\ln(\varepsilon_{\text{d}})$$

$\varepsilon_{\text{dynamic}}$	N
1%	4.6
0.1%	6.9
0.01%	9.2

Time Constant

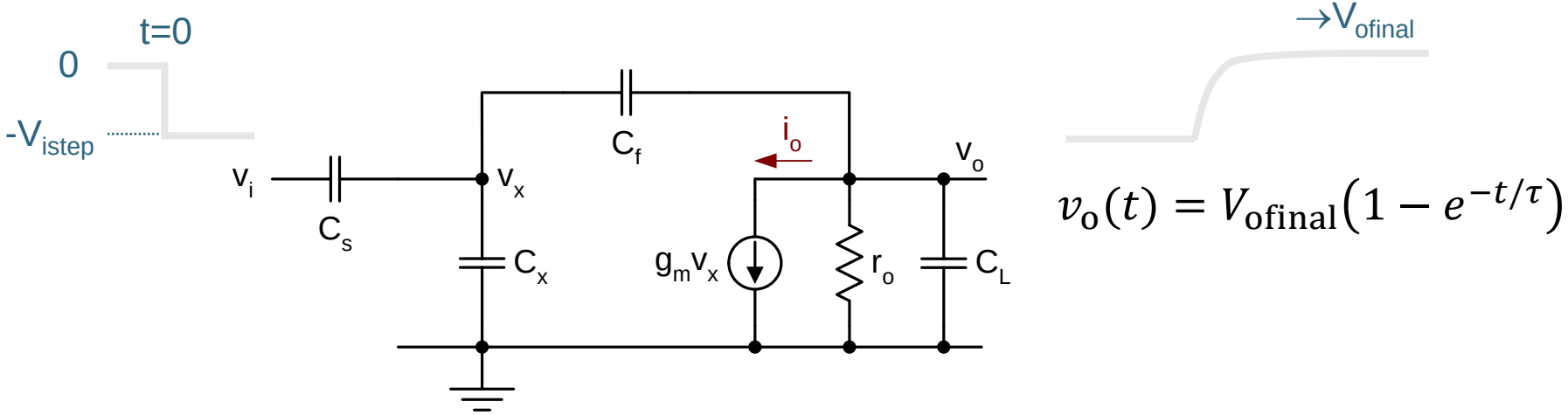
$$\beta = \frac{C_f}{C_f + C_s + C_x}$$



$$R = \frac{1}{\beta g_m} \qquad C_{\text{Ltot}} = C_L + (1-\beta)C_f$$

$$\tau = \frac{1}{\beta} \cdot \frac{C_{\text{Ltot}}}{g_m}$$

Transconductor Current



$$v_o(t) = V_{ofinal}\left(1 - e^{-t/\tau}\right)$$

- During linear settling, the current delivered by the transconductor is

$$i_o \cong -C_{Ltot}\frac{dv_o(t)}{dt} = -C_{Ltot}\frac{V_{ofinal}}{\tau}e^{-t/\tau}$$

- Peak current occurs at t=0

$$|i_o|_{max} = C_{Ltot}\frac{V_{ofinal}}{\tau}$$

Slewing

- The amplifier can deliver a maximum current of I_D
  - If $|i_o|_{max} > I_D$, slewing occurs

$$|i_o|_{max} = C_{Ltot}\frac{V_{ofinal}}{\tau} > I_D$$

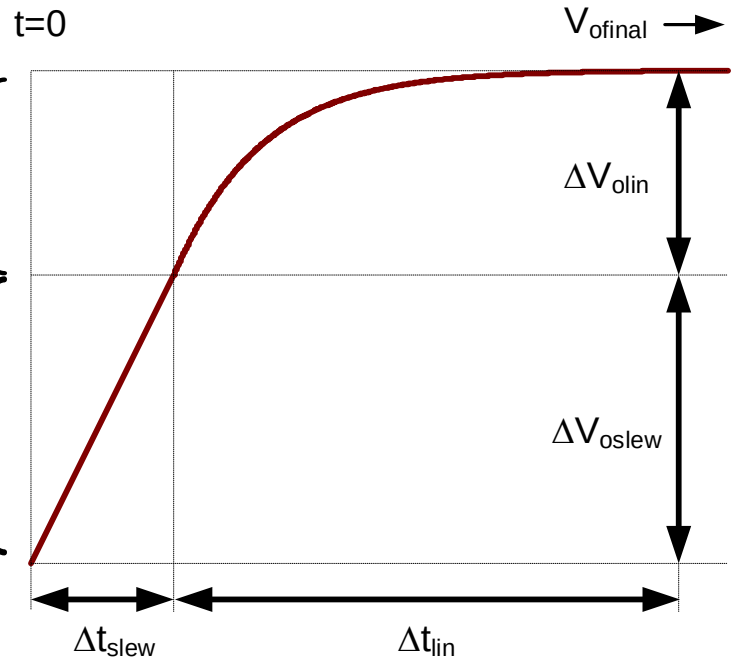
$$C_{Leff}\frac{V_{ofinal}}{\frac{1}{\beta}\cdot\frac{C_{Ltot}}{g_m}} > I_D \quad \Rightarrow \quad \frac{g_m}{I_D} > \frac{1}{\beta V_{ofinal}} \quad \text{or} \quad V^* < 2\beta V_{ofinal}$$

- Example: β=0.5, V_{ofinal}=0.5V → g_m/I_D > 4 S/A (V*<500mV) will result in slewing
- Challenging to avoid slewing, unless
  - Bias at very low g_m/I_D (power inefficient & large headroom)
  - Feedback factor is small (large closed-loop gain, C_S/C_f)
  - Output voltage swing is small

Output Waveform with Initial Slewing

$$v_o(t) = \Delta V_{oslew} + \Delta V_{olin}\left(1 - e^{-(t-\Delta t_{slew})/\tau}\right)$$

$$v_o(t) = \frac{I_D}{C_{Ltot}} t = SR \cdot t$$



- Continuous derivative in the transition slewing→linear requires

$$\frac{I_D}{C_{\mathrm{Ltot}}} = \frac{\Delta V_{\mathrm{olin}}}{\tau} \qquad \Delta V_{olin} = \frac{\tau \cdot I_D}{C_{Ltot}}$$

Dynamic Error with Slewing

$$\Delta V_{oslew} = V_{ofinal} - \Delta V_{olin} \qquad \Delta t_{slew} = (V_{ofinal} - \Delta V_{olin}) \cdot \frac{C_{Ltot}}{I_D}$$

- Using the above result, we can now calculate the dynamic error during the final linear settling portion

$$\text{For } t > \Delta t_{slew}: \qquad v_o(t) = \Delta V_{oslew} + \Delta V_{olin}\left(1 - e^{-(t-\Delta t_{slew})/\tau}\right)$$

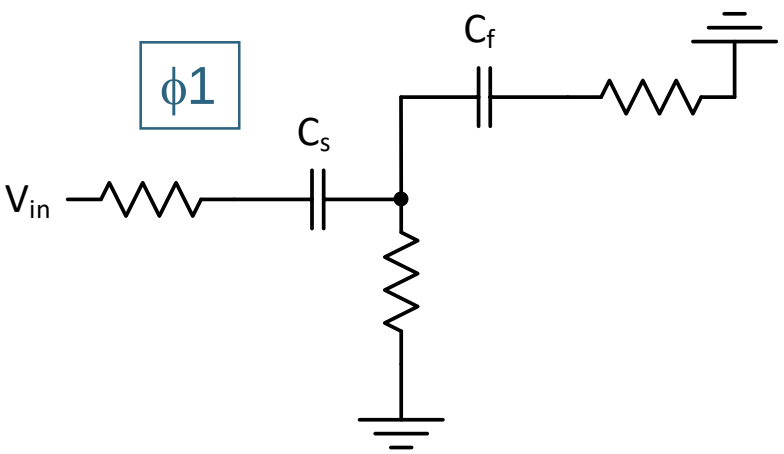
$$\varepsilon_d(t) = \frac{v_o(t) - V_{final}}{V_{final}} = \frac{\Delta V_{oslew} + \Delta V_{olin}\left(1 - e^{-(t-\Delta t_{slew})/\tau}\right) - V_{ofinal}}{V_{ofinal}}$$

$$\varepsilon_d(t) = -\frac{\Delta V_{olin}}{V_{ofinal}} e^{-(t-\Delta t_{slew})/\tau}$$

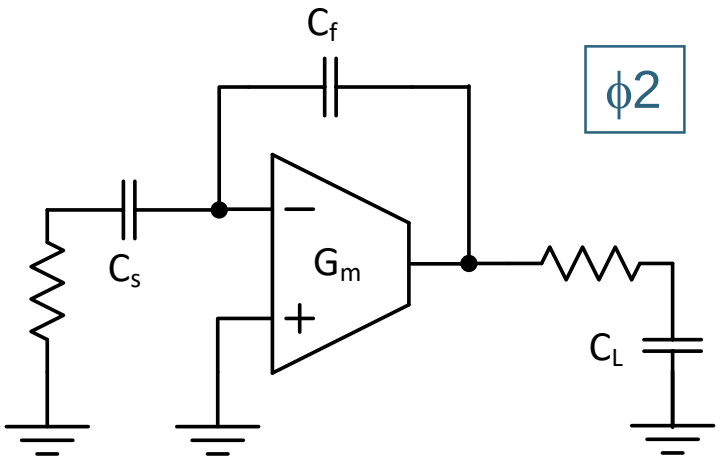
EE 240C
Analog-Digital Interface Integrated Circuits

Track & Hold Amp – Noise

Noise Analysis

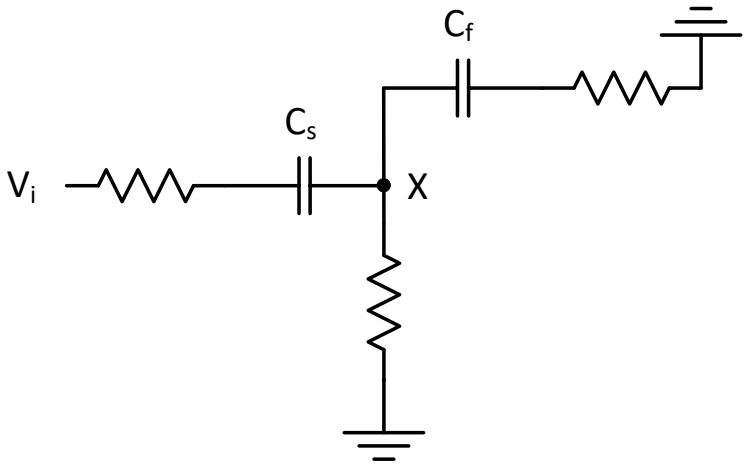


Noise due to switches



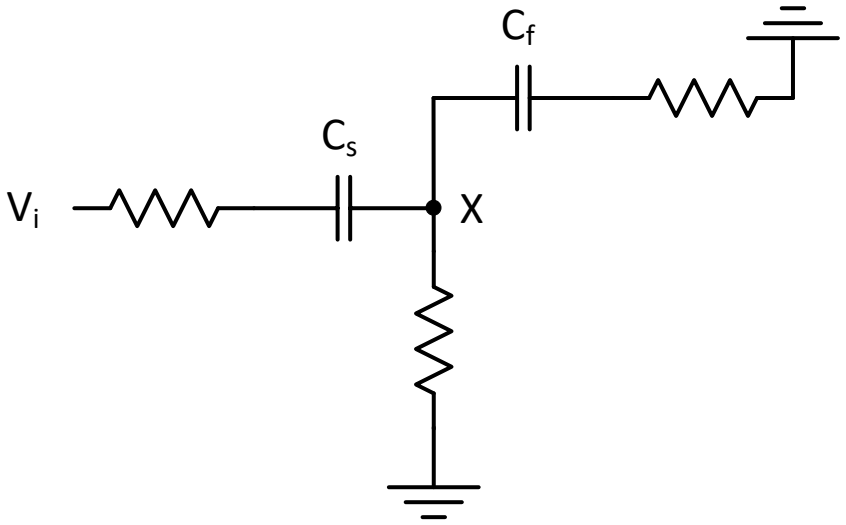
Noise due to amplifier and switches

Tracking Phase ($\phi 1$)



- Variable of interest is total integrated "noise charge" at node X, q_x^2
- Cumbersome to compute using standard analysis
  - Find transfer function from each noise source (3 resistors) to q_x
  - Integrate magnitude squared expressions from zero to infinity and add
- Much easier
  - Use equipartition theorem

Tracking Phase Noise Charge



- Energy stored at node X is

$$\frac{1}{2}\frac{q_x^2}{C_{\text{eff}}} = \frac{1}{2}\frac{q_x^2}{C_s + C_f}$$

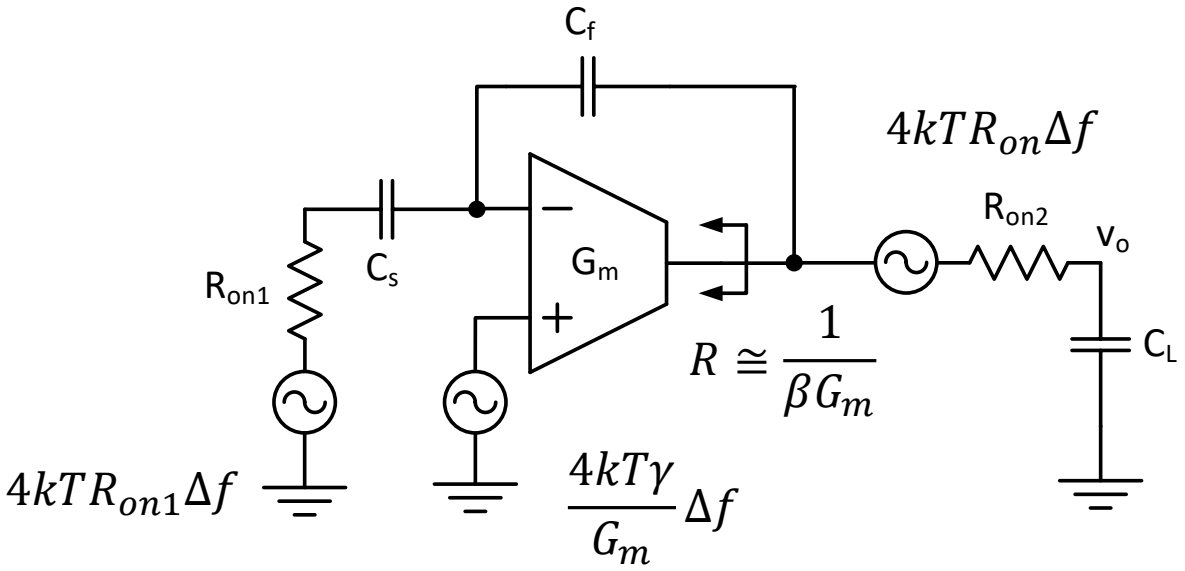
- Apply equipartition theorem

$$\overline{\frac{1}{2}\frac{q_x^2}{C_s + C_f}} = \frac{1}{2}kT$$

$$\overline{q_x^2} = kT\left(C_s + C_f\right)$$

- Note that any additional parasitic capacitance at node X will increase the sampled noise charge!

Redistribution Phase Noise



(γ includes excess noise from load, n_f)

- In a proper design, R_{on1} and R_{on2} will be much smaller than $1/\beta G_m$, else the switches would significantly affect the dynamics, which would be very wasteful
  - Switches with low on-resistance consume much less power than amplifiers with large G_m

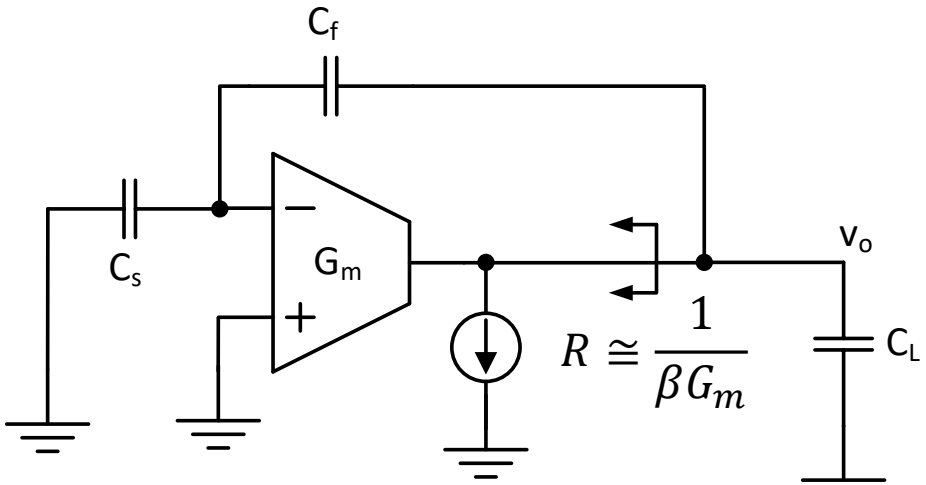
Output Referred Noise Comparison

- R_{on1} noise referred to v_o $$N_1 = 4kTR_{on1}\Delta f \cdot \left(\frac{C_s}{C_f}\right)^2 \cdot |H(j\omega)|^2$$
- R_{on2} noise referred to v_o $$N_2 = 4kTR_{on2}\Delta f \cdot |H(j\omega)|^2$$
- Amplifier noise referred to v_o $$N_a = \frac{4kT\gamma}{G_m}\Delta f \cdot \left(1+\frac{C_s}{C_f}\right)^2 \cdot |H(j\omega)|^2$$

$$\frac{N_a}{N_1} = \frac{\gamma}{G_m R_{on1}} \frac{\left(1+\frac{C_s}{C_f}\right)^2}{\left(\frac{C_s}{C_f}\right)^2} >> 1 \qquad \frac{N_a}{N_2} = \frac{\gamma}{G_m R_{on2}} \left(1+\frac{C_s}{C_f}\right)^2 >> 1$$

- Amplifier noise dominates over noise due to R_{on1}, R_{on2}

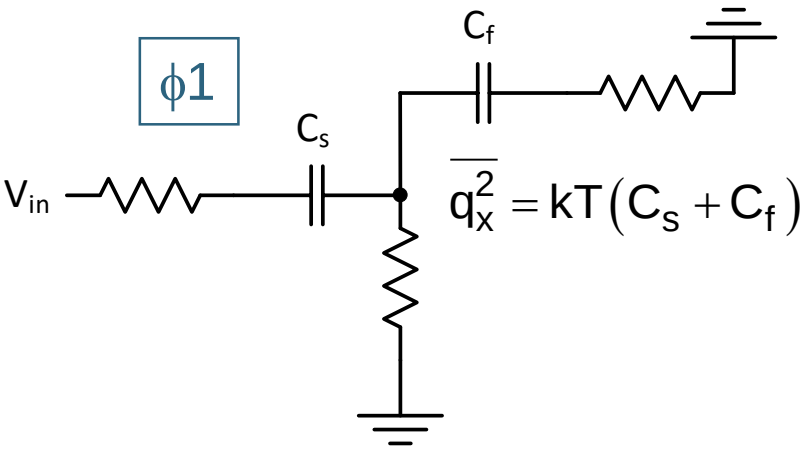
Total Integrated Amplifier Noise

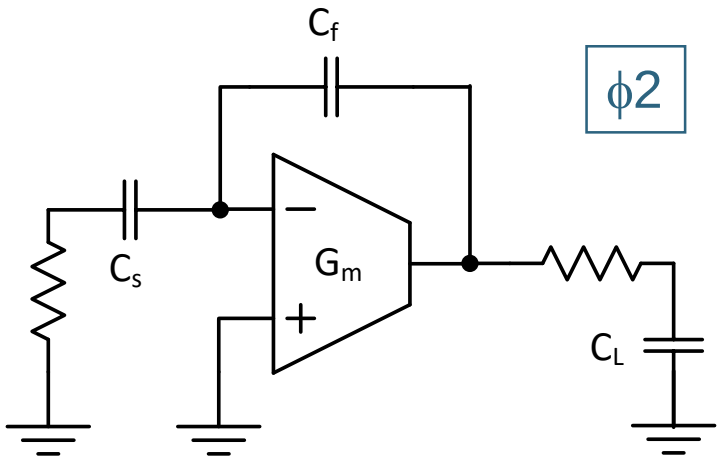


$$\frac{\overline{v_o^2}}{\Delta f} = 4kT\gamma \frac{1}{\beta R} \cdot \left| R \| \frac{1}{j\omega C_{L\text{tot}}} \right|^2$$

$$\overline{v_o^2} = \int_0^\infty 4kT\gamma \frac{1}{\beta R} \cdot \Delta f \cdot \left| \frac{R}{1 + j\omega R C_{L\text{tot}}} \right|^2 df = \gamma \frac{1}{\beta} \frac{kT}{C_{L\text{tot}}}$$

Adding up the Noise Contributions





$$\overline{v_{o,1}^2} = \frac{\overline{q_x^2}}{C_f^2} = kT\left(\frac{C_s + C_f}{C_f^2}\right) = \frac{kT}{C_f}\left(1 + \frac{C_s}{C_f}\right)$$

$$\overline{v_{o,2}^2} \cong \gamma \frac{1}{\beta}\frac{kT}{C_{Ltot}}$$

$$\boxed{\overline{v_{o,tot}^2} = \frac{kT}{C_f}\left(1 + \frac{C_s}{C_f}\right) + \gamma \frac{1}{\beta}\frac{kT}{C_{Ltot}}}$$

Noise in Differential Circuits

- In differential circuits, the noise power is doubled (because there are two half circuits contributing to the noise)
- But, the signal power increases by 4x
  - Looks like a 3dB win?

$$DR_{\text{single}} \propto \frac{\hat{V}_o^2}{\frac{kT}{C}} \qquad DR_{\text{diff}} \propto \frac{\left(2\hat{V}_o\right)^2}{2\frac{kT}{C}} = 2\frac{\hat{V}_o^2}{\frac{kT}{C}}$$

- Yes, there's a 3dB win in DR, but it comes at twice the power dissipation (due to two half circuits)
- Can get the same DR/power in a single ended circuit by doubling all cap sizes and g_m
- But: beware of differential amplifiers with one input grounded!

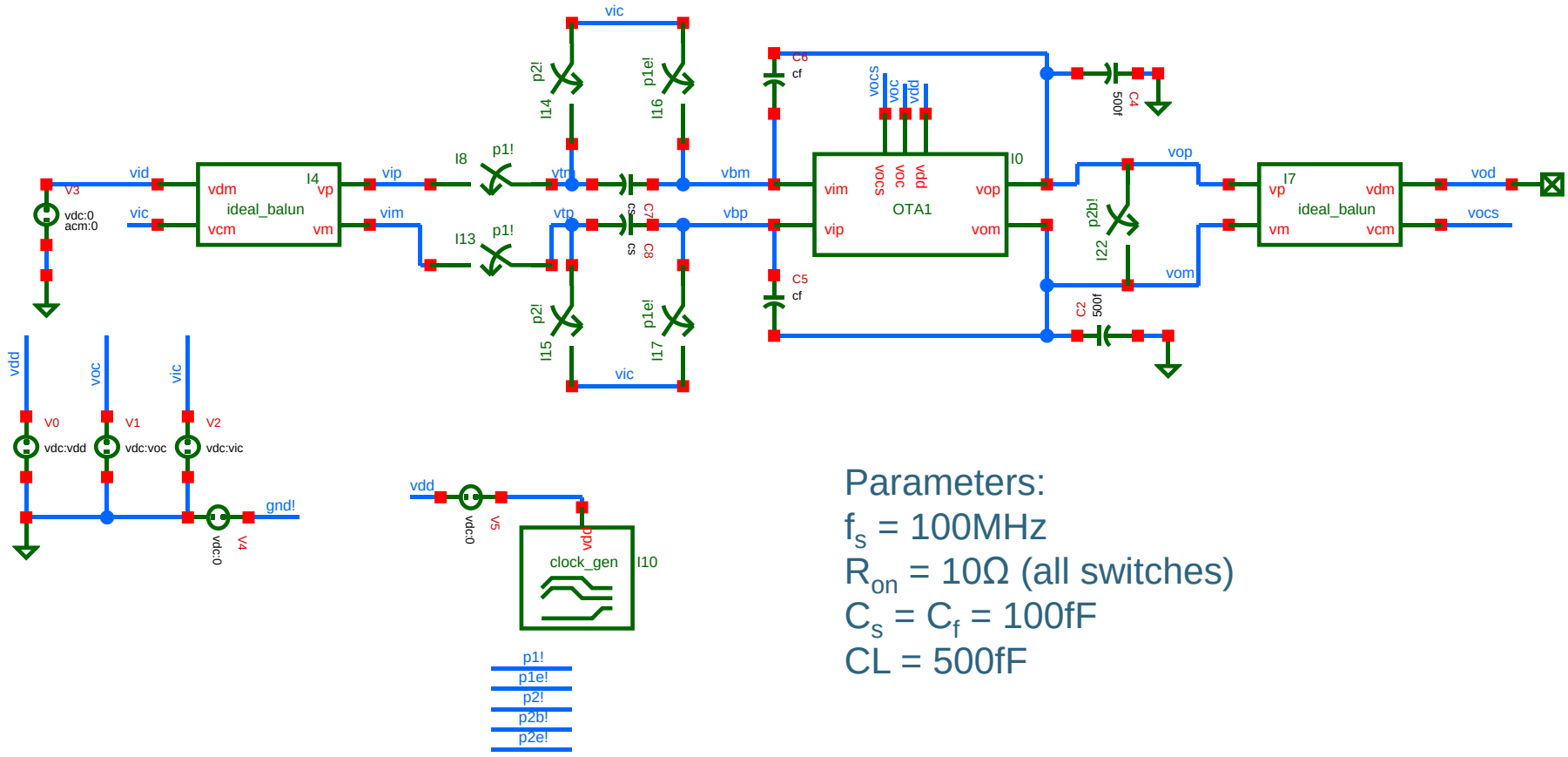
EE 240C
Analog-Digital Interface Integrated Circuits

Track & Hold Amp – Noise Simulation

Noise Simulation Example

- Three ways to simulate noise in switched capacitor circuits
- Basic .ac/.noise Spice simulations
  - Must simulate noise in each clock phase separately
    - Activate $\phi 1$ switches, run .noise and integrate noise charge at relevant node over all frequencies and refer to output
    - Activate $\phi 2$ switches, run .noise and integrate noise at output
- Periodic Steady State Simulation
  - E.g. SpectreRF or BDA, "periodic noise analysis“ (PNOISE)
  - For linear time-variant circuits → periodic clocked SC circuits
    - Noise from all phases is automatically added, all correlation taken care of
- Transient Noise
  - Simple setup
  - Computation intensive

Example Track and Hold Schematic



Parameters:

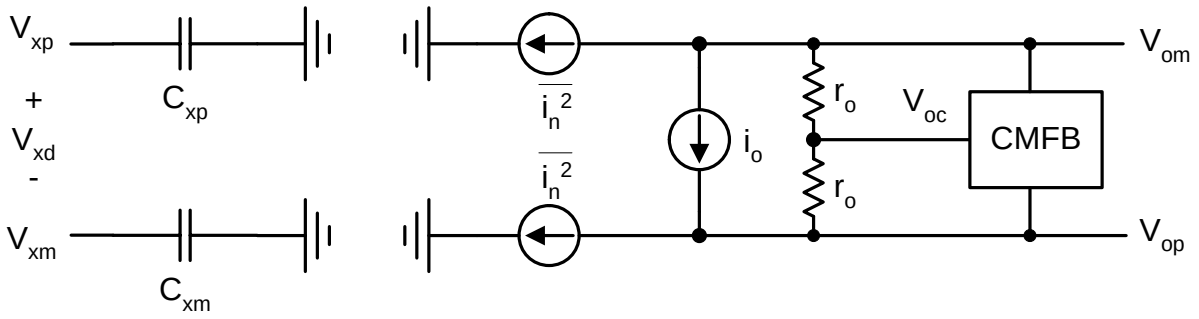
f_s = 100MHz

R_{on} = 10Ω (all switches)

$C_s = C_f$ = 100fF

CL = 500fF

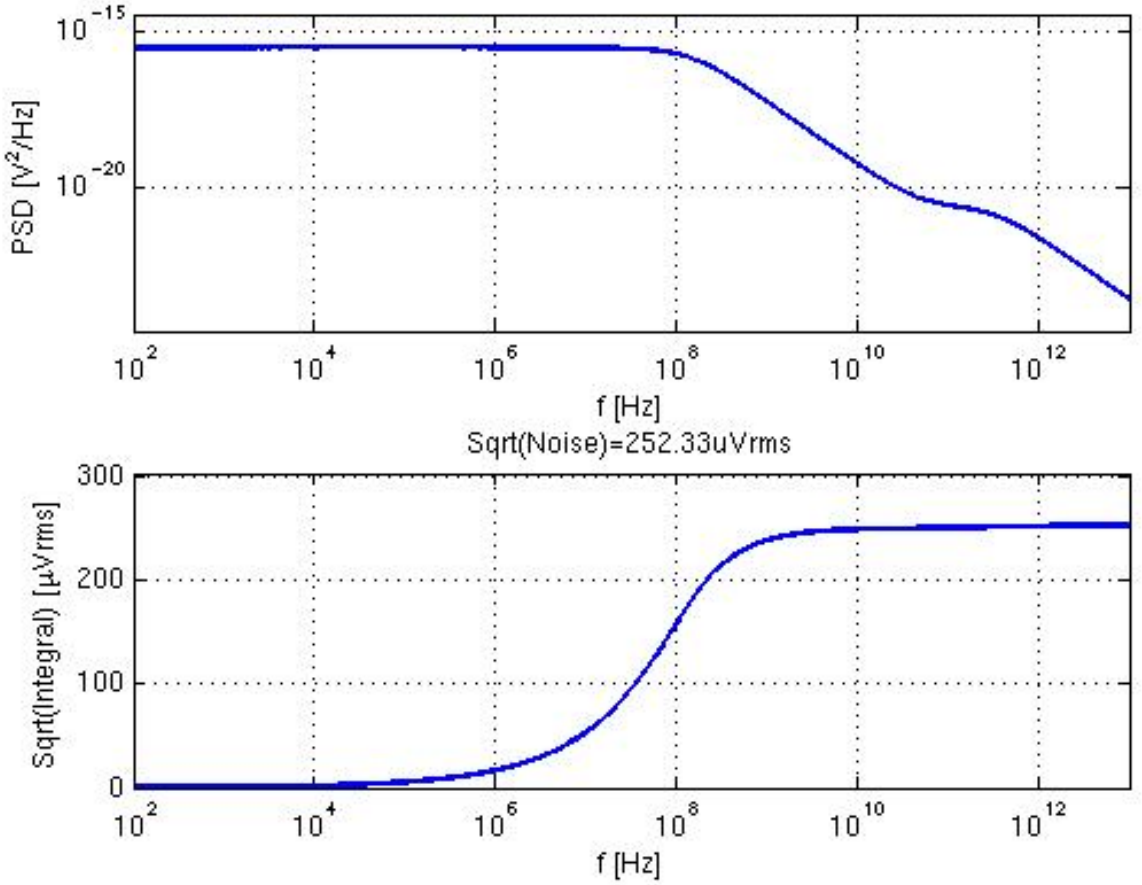
OTA Simulation Model



$$C_{xp,m} = \frac{g_m}{2\pi f_T} \qquad \frac{\overline{i_n^2}}{\Delta f} = \alpha \cdot kTg_m \qquad r_o = \frac{a_{vo}}{g_m} \qquad I_D = \frac{g_m}{(g_m / I_D)}$$

Parameters: g_m=1mS, a_{vo}=1000, α=2, g_m/I_D=10S/A , f_T=20GHz

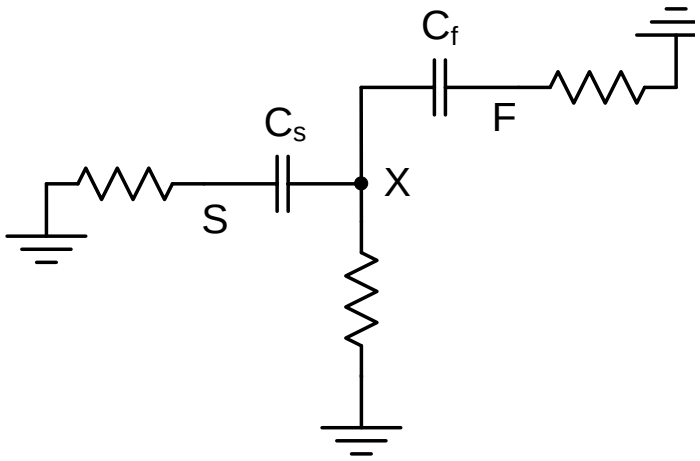
Hold Mode Noise Simulation (.noise)



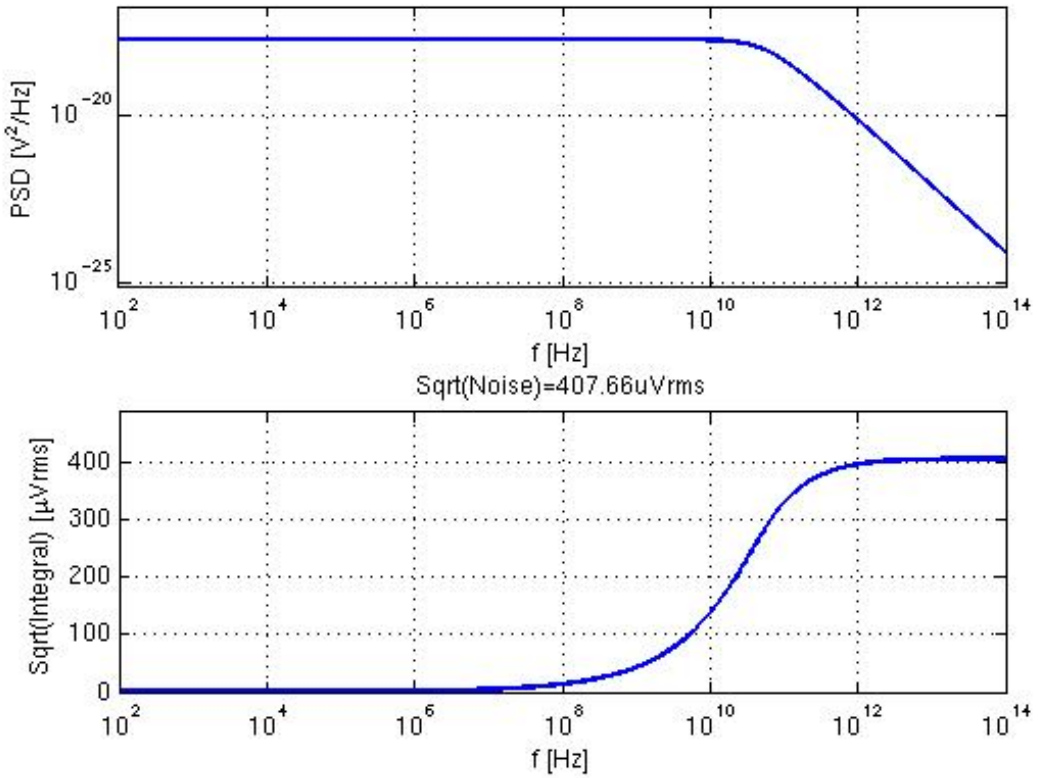
Calculated value: 248uVrms

Track Mode Noise Simulation (.noise)

```
*** Compute noise charge and refer charge referred to output via Cf
en vno 0  vcvs vol= '( cs*v(x,s) + cf*v(x,f) )/cf'
.ac dec 100 100 100Gig
.noise v(vno) vdummy
```

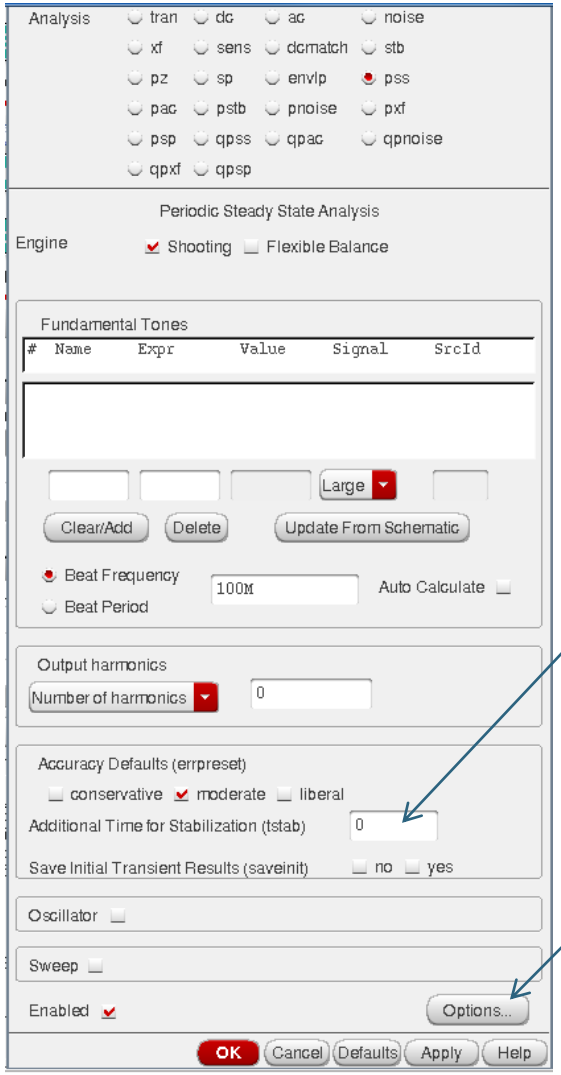


(shown single ended for simplicity)



Calculated value: 413uVrms

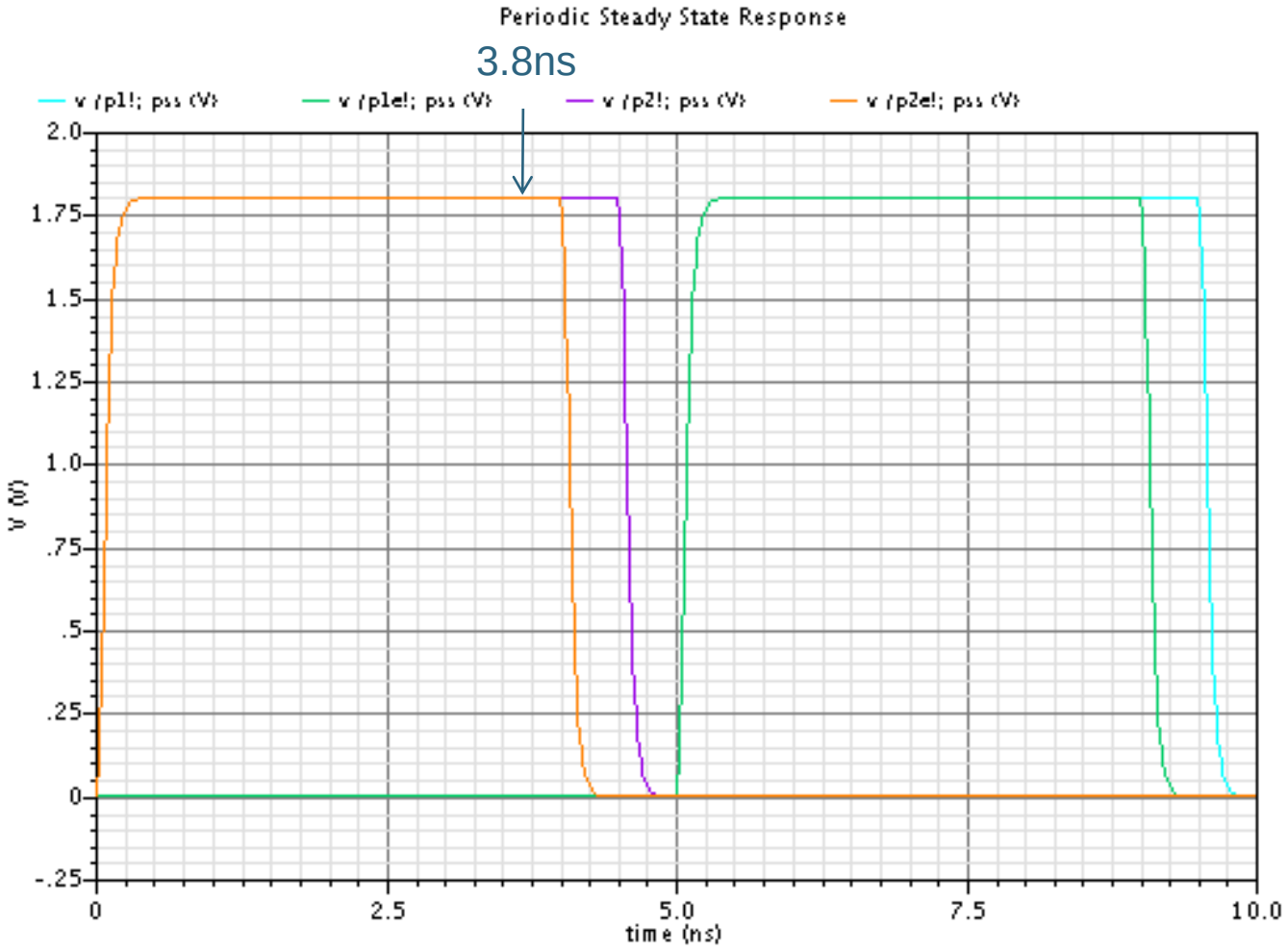
PSS Setup



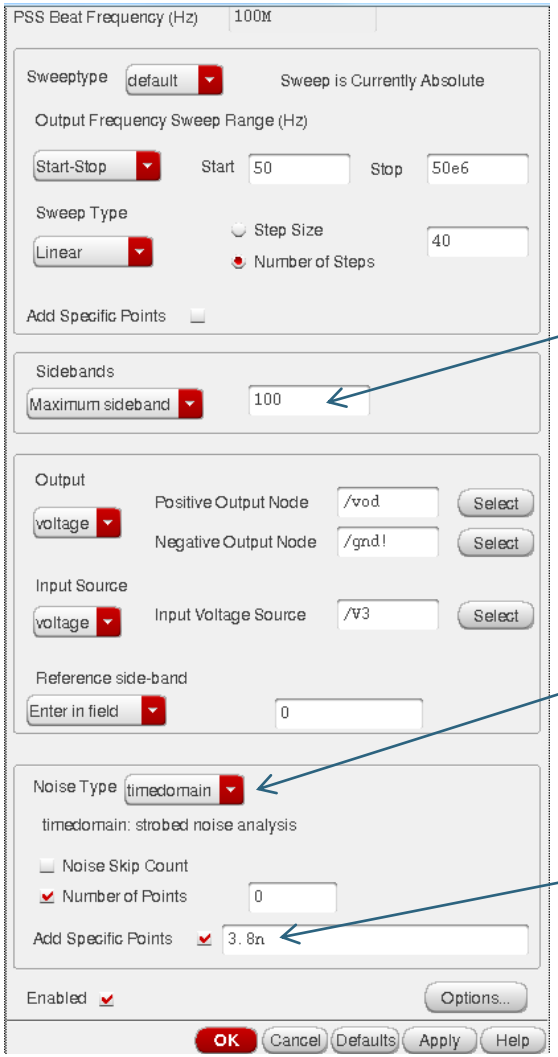
Use “tstab” if your circuit needs time to get into steady state (e.g. clock bootstrap circuits)

Important: set “maxacfreq” to the highest frequency at which you expect noise to be significant (10GHz in this example; see “Hold Mode Noise Simulation”)

PSS Waveforms (Clocks)



PNOISE Setup



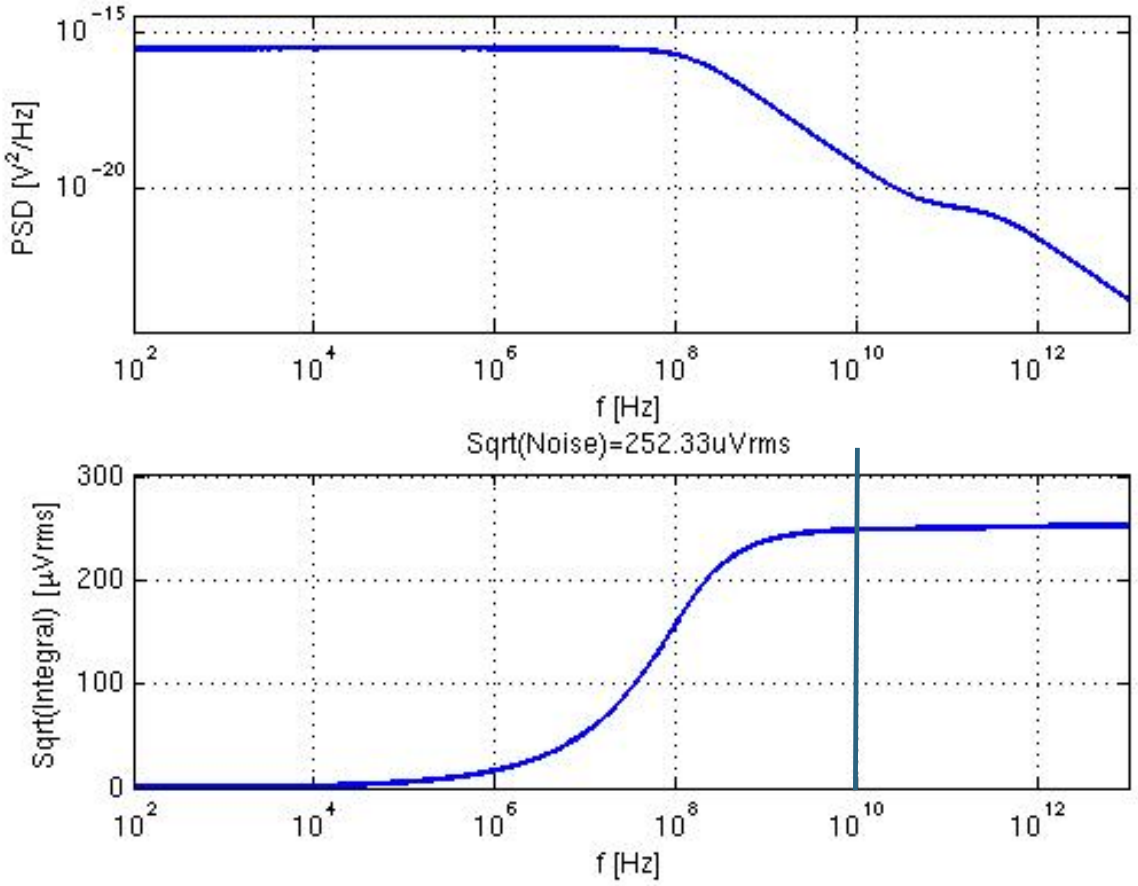
"Number of sidebands" – typically ~20…200 to handle noise folding properly. Fast switches → more sidebands needed. Again, Be sure to set "maxacfrequency" in the PSS analysis options to a correspondingly large value. Note: This is not a problem in some simulators such as BDA, which cover an "infinite" number of sidebands

"timedomain" means simulator computes spectrum of discrete time noise samples

Sampling instant (3.8ns in this example)

How Many Sidebands are Needed? (1)

Hold mode noise integral (.noise)



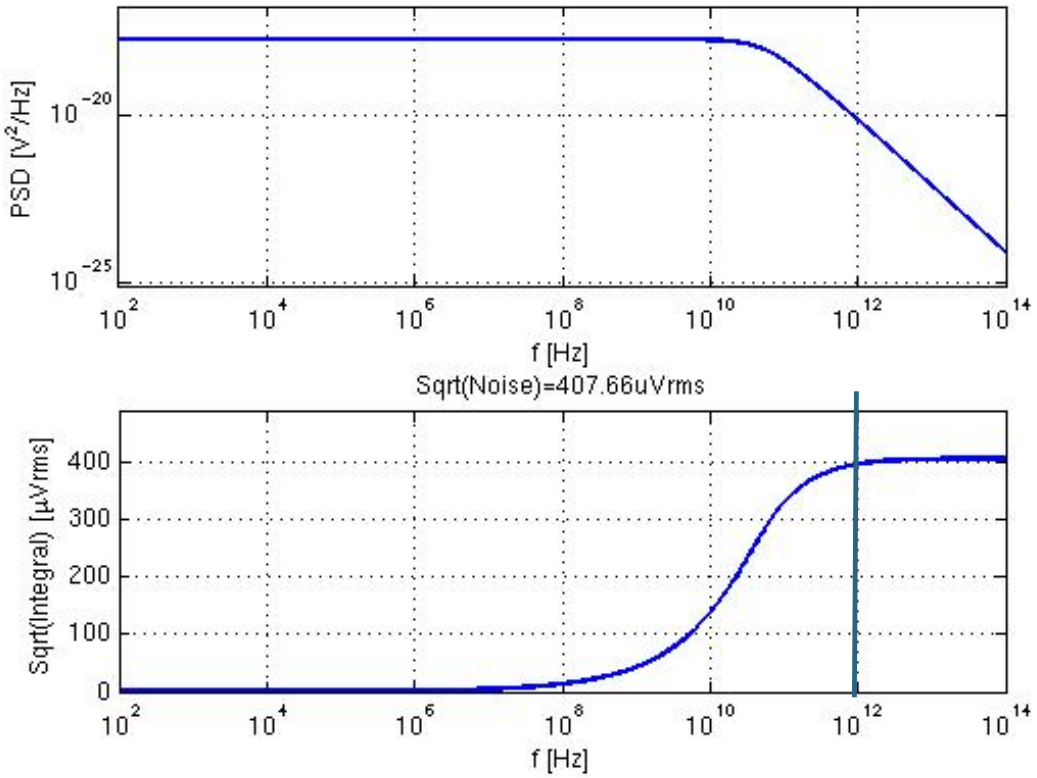
Noise up to 10GHz must be considered !

→ numsidebands =100

→ maxacfreq = 10GHz,

How Many Sidebands are Needed? (2)

Track mode noise integral, (.noise, R_{on} = 10 Ohms)



Noise up to 1 THz must be considered !

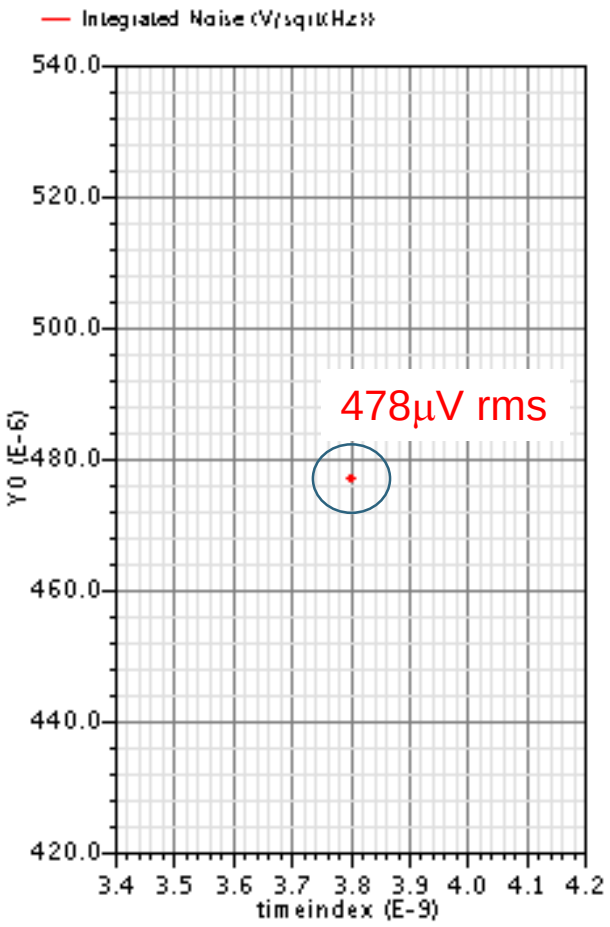
→ numsidebands =10,000?

No! Increase R_{on} to maintain reasonable simulation time.

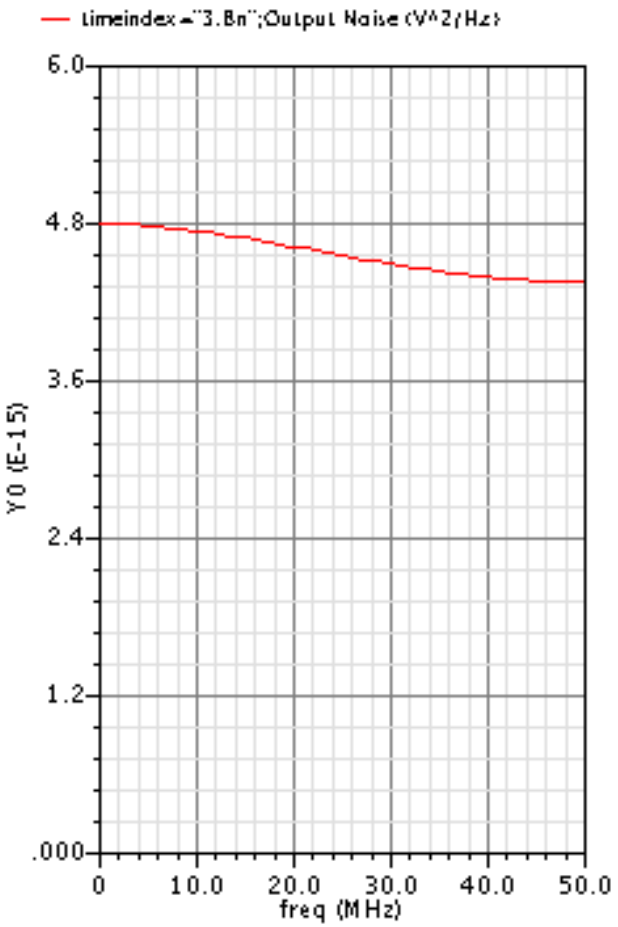
Keep $R_{on}C$ ~ 10x faster than amplifier.

PNOISE Result

Sampled Noise



Noise PSD



Comparison

Calculated:	$\overline{v_{o,1}^2} = (413\mu Vrms)^2$	$\overline{v_{o,2}^2} = (248\mu Vrms)^2$	$\overline{v_{o,tot}^2} = (482\mu Vrms)^2$
Simulated: (.noise)	$\overline{v_{o,1}^2} = (415\mu Vrms)^2$	$\overline{v_{o,2}^2} = (252\mu Vrms)^2$	$\overline{v_{o,tot}^2} = (485\mu Vrms)^2$
Simulated: (PNOISE)		$\overline{v_{o,tot}^2} = (478\mu Vrms)^2$	

- Very good agreement between calculation and both simulation approaches

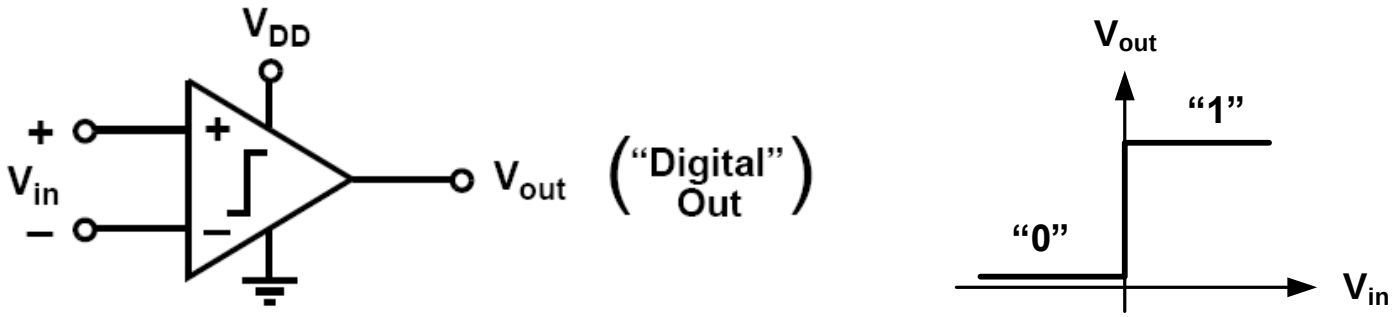
Summary – Sampling Circuits

- Implementation styles
  - Purely passive
  - Charge redistribution or flip-around architecture
    - Input common-mode rejection & gain>1 vs increased feedback factor
- In a properly designed circuit only the most fundamental issues are significant
  - Jitter, kT/C noise
- Charge injection is not a problem if properly handled
  - E.g. through bottom plate sampling

EE 240C
Analog-Digital Interface Integrated Circuits

Comparators

Ideal Voltage Comparator

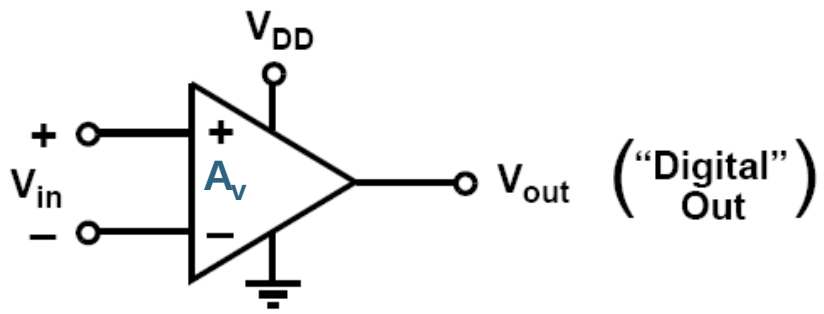


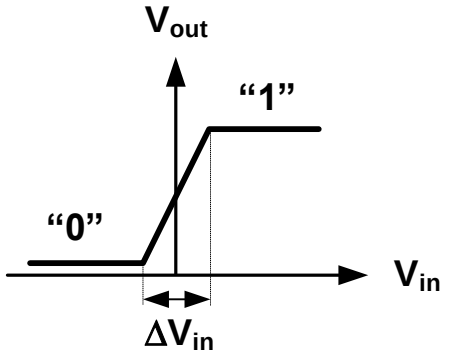
- Function
  - Compare the instantaneous values of two analog voltages (e.g. an input signal and a reference voltage) and generate a digital 1 or 0 indicating the polarity of that difference

Design Considerations

- Accuracy
  - Gain (resolution)
  - Offset
- Speed
  - Small-signal bandwidth
  - Settling time or delay time, slew rate
  - Overdrive recovery
- Power dissipation
- Input properties
  - Sampled data versus continuous time
  - Common-mode rejection
  - Input capacitance and linearity of input capacitance
  - Kickback noise

Gain Requirements



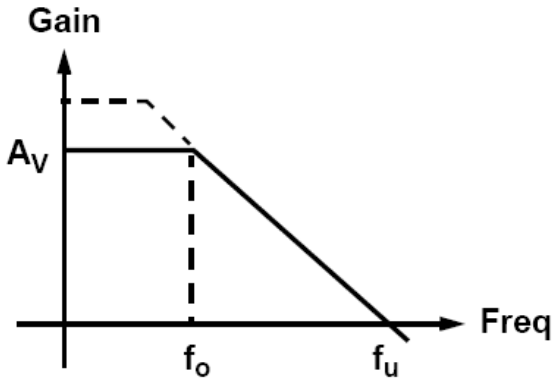


$$\Delta V_{\text{in}} = \frac{V_{\text{DD}}}{A_{vo}}$$

- E.g. 12-bit ADC, V_{DD}=1.8V, FSR=0.9V $\Rightarrow$ LSB=0.9V/4096
- For 1/2 LSB precision, we need

$$A_v = \frac{1.8V}{0.5 \cdot 0.9V/4096} \cong 16{,}000 = 84dB$$

How about Using an OpAmp or OTA?



f_u = unity gain frequency, f_o = – 3dB frequency

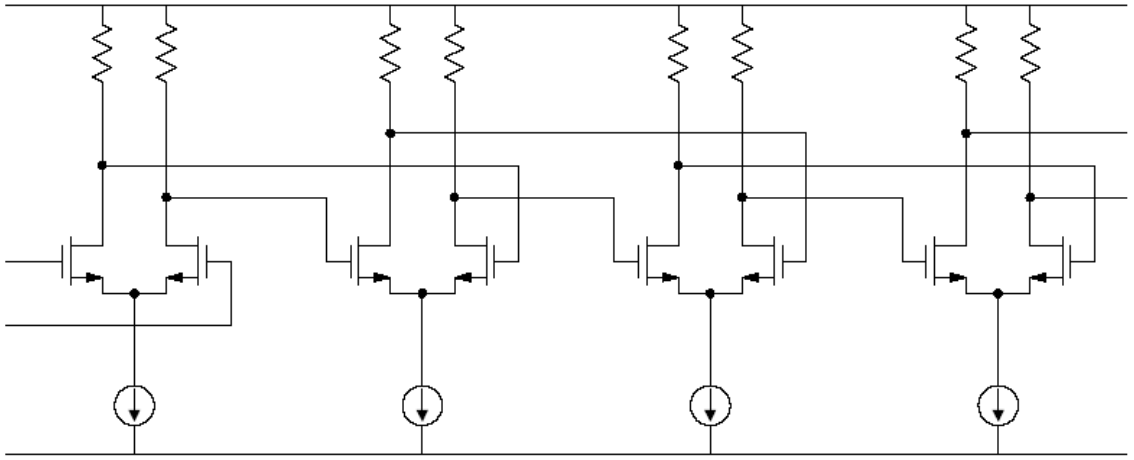
How to Implement High Gain?

- Considerations
  - Amplification need not be linear
  - Amplification need not be continuous in time, if comparator is used in a sampled data system
    - Clock signal will tell comparator when to make a decision
- Implementation options
  - Single stage amplification
    - E.g. OTA or OpAmp in open loop configuration
  - Multi-stage amplification
    - E.g. cascade of resistively loaded differential pairs
  - Regenerative latch using positive feedback
    - E.g. cross coupled inverters

EE 240C
Analog-Digital Interface Integrated Circuits

Comparators – Cascade of Amplifiers

Cascade of Open-Loop Amplifiers



In each stage: $\omega_u = \frac{g_m}{C_{gs}} \cong \text{const.}$ $A_0 = g_m R = \frac{\omega_u}{\omega_0}$ $\omega_0 = \frac{1}{RC} = \frac{\omega_u}{A_0}$

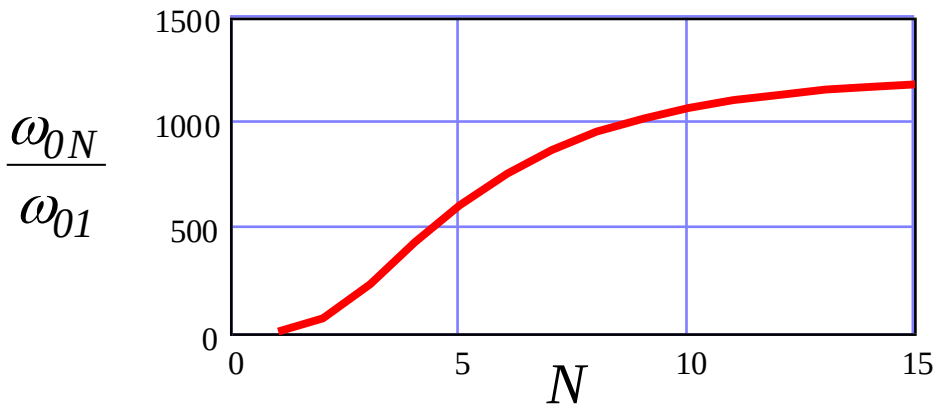
- Possible choices for a given, constant overall gain objective
  - Lots of stages with low gain
  - Only a few stages with moderate gain

Bandwidth Perspective

- If we only care about small signal bandwidth, it follows that we should cascade many low gain stages
  - Makes intuitive sense, because each individual stage will have a very large bandwidth
- Detailed analysis shows (for fixed ω_u)

$$\frac{\omega_{0N}}{\omega_{01}} = A_v^{\left(\frac{N-1}{N}\right)}\sqrt{2^{\frac{1}{N}}-1}$$

A_v Total gain requirement
ω_{01} Bandwidth of single stage realization
ω_{0N} Bandwidth of N stage realization



(A_v=10,000)

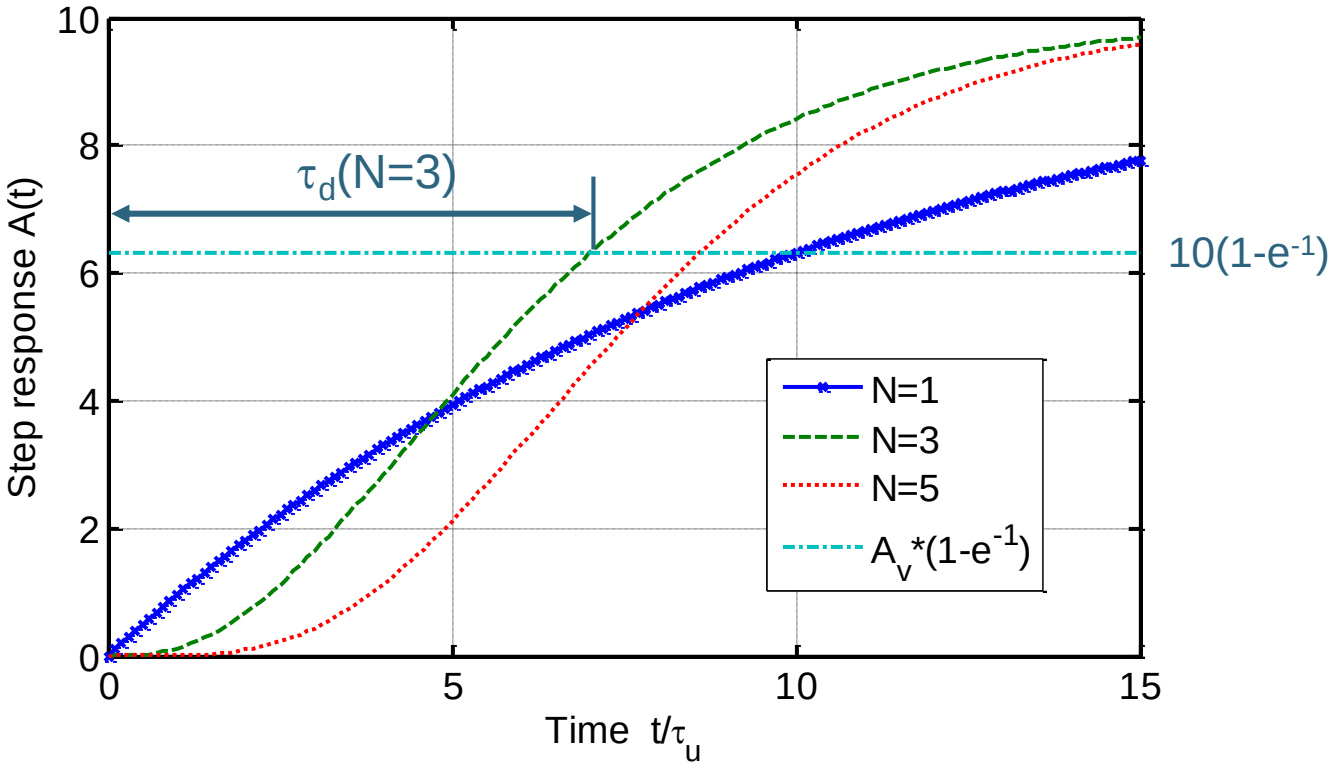
Step Response (1)

- When the input is a sampled data signal, it is more important to minimize the delay in response to an input step

$$V_{\text{out}}(s) = V_{\text{in}}(s)A(s) = \frac{V_{\text{istep}}}{s}\frac{A_v}{\left(1 + s \cdot \tau_u {A_v}^{1/N}\right)^N} \qquad \tau_u = \frac{1}{\omega_u} \qquad A_v = A_0^N$$

$$V_{\text{out}}(t) = V_{\text{istep}} A_v \underbrace{\left(1 - e^{-\frac{t}{\tau_u \cdot {A_v}^{1/N}}} \sum_{i=0}^{N-1} \frac{\left(\frac{t}{\tau_u \cdot {A_v}^{1/N}}\right)^i}{i!}\right)}_{A(t)}$$

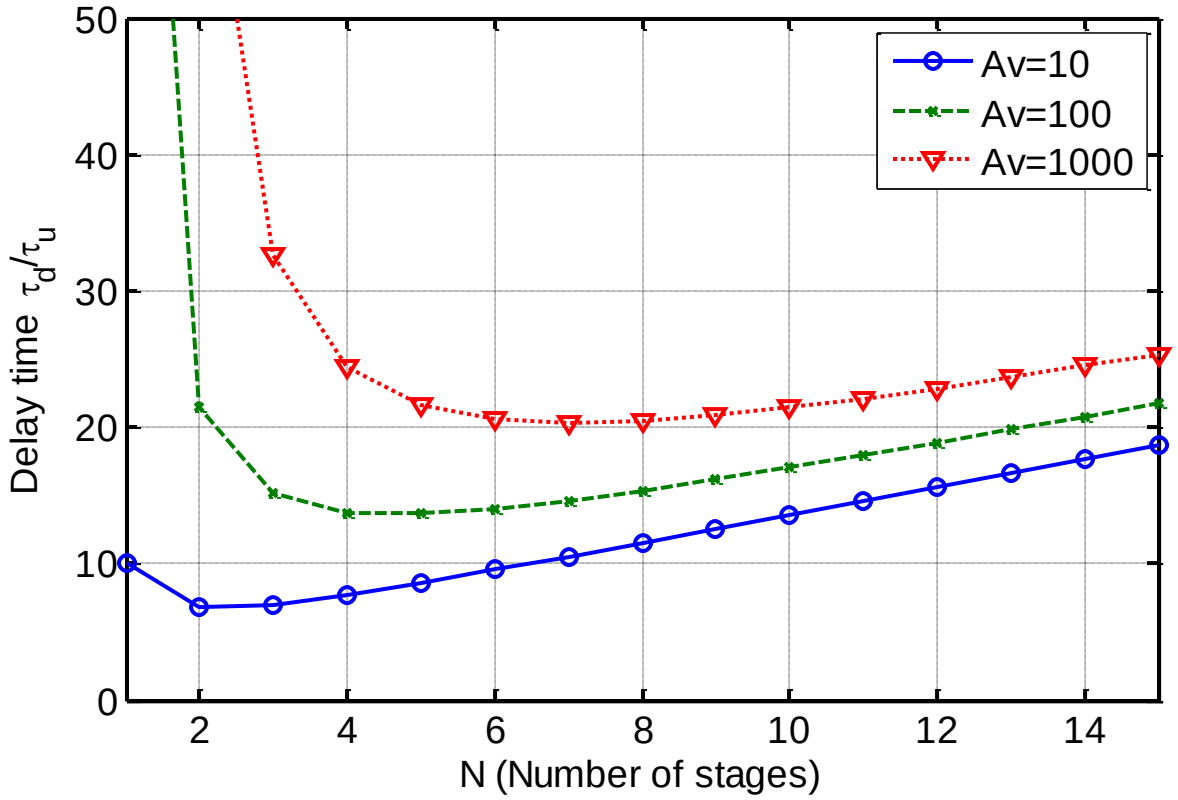
Step Response (2)



- Three stage amplifier wins! (for A_v=10)

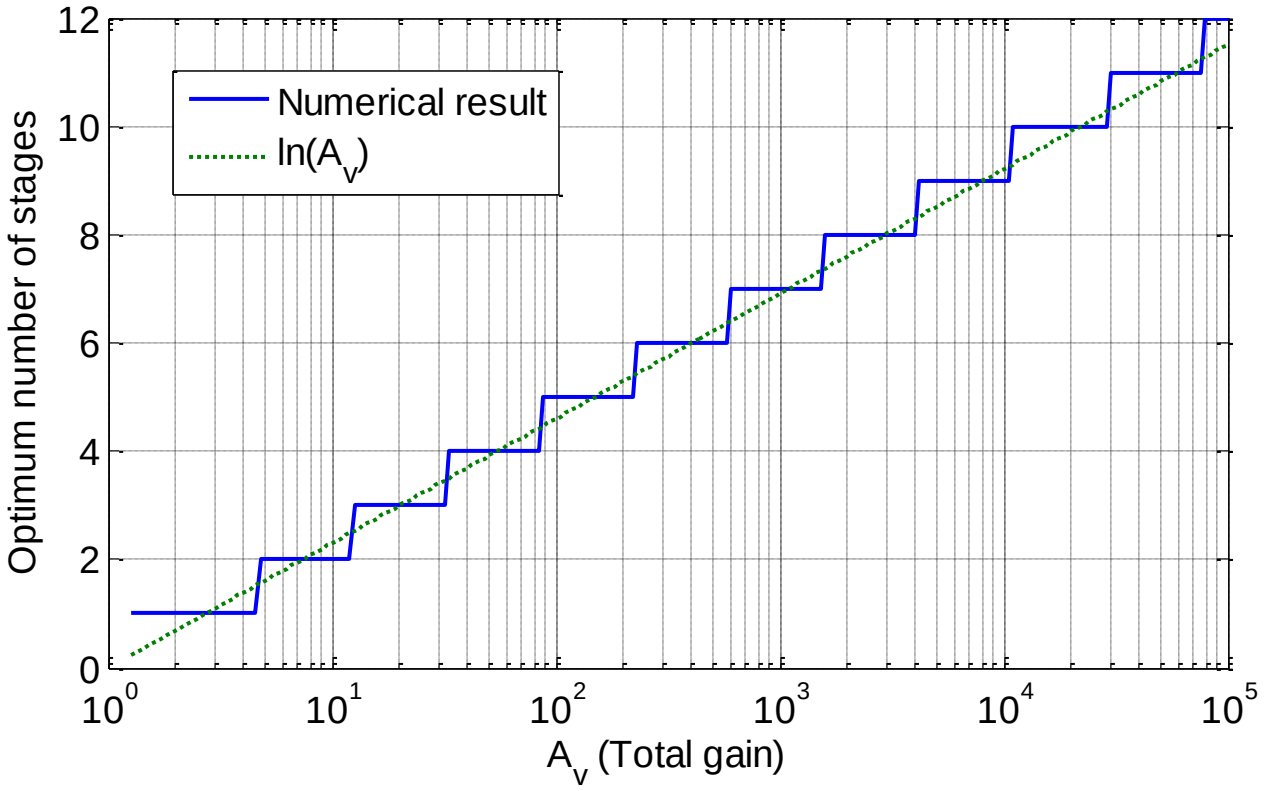
Delay versus Number of Stages

$$A(\tau_d) = A_v(1 - e^{-1}) \quad \Rightarrow \quad \tau_d \quad \text{(numerically)}$$



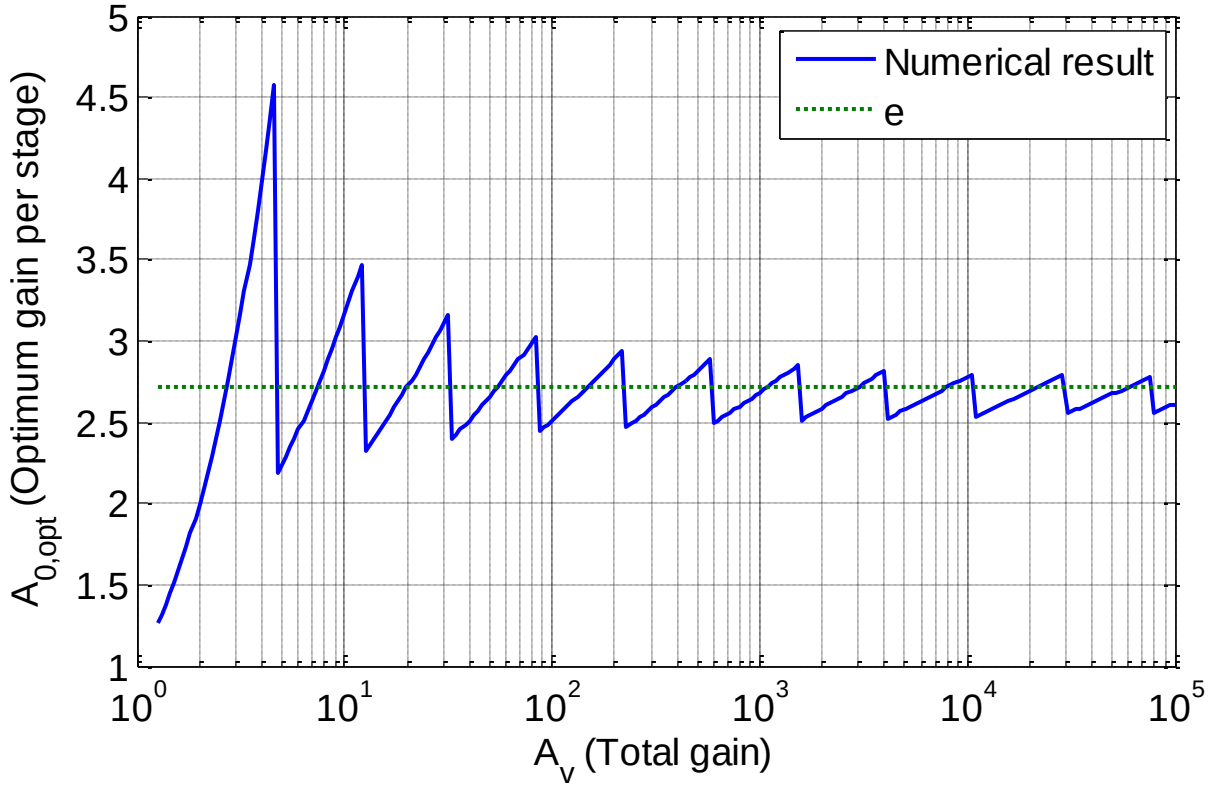
- Shallow minima!

Optimum Number of Stages



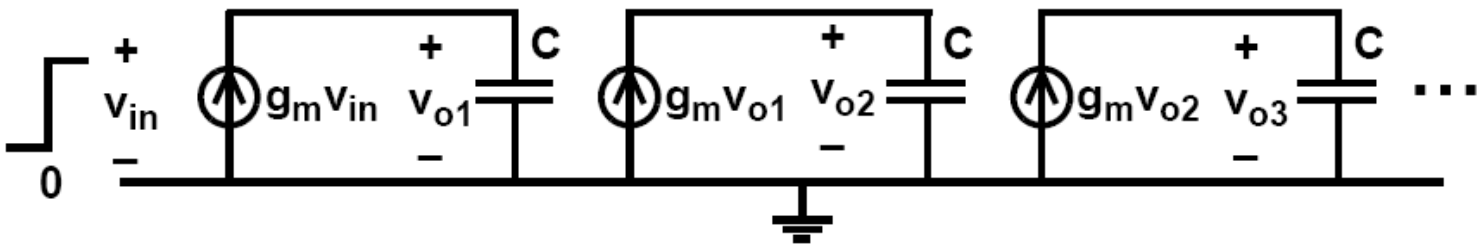
$$N_{\text{opt}} \cong \ln(A_v)$$

Optimum Gain per Stage



$$N_{\text{opt}} \cong \ln(A_v) \qquad e^{N_{\text{opt}}} \cong A_v = {A_{0,\text{opt}}}^{N_{\text{opt}}} \quad \Rightarrow \quad A_{0,\text{opt}} \cong e$$

Cascade of "Integrators" (1)

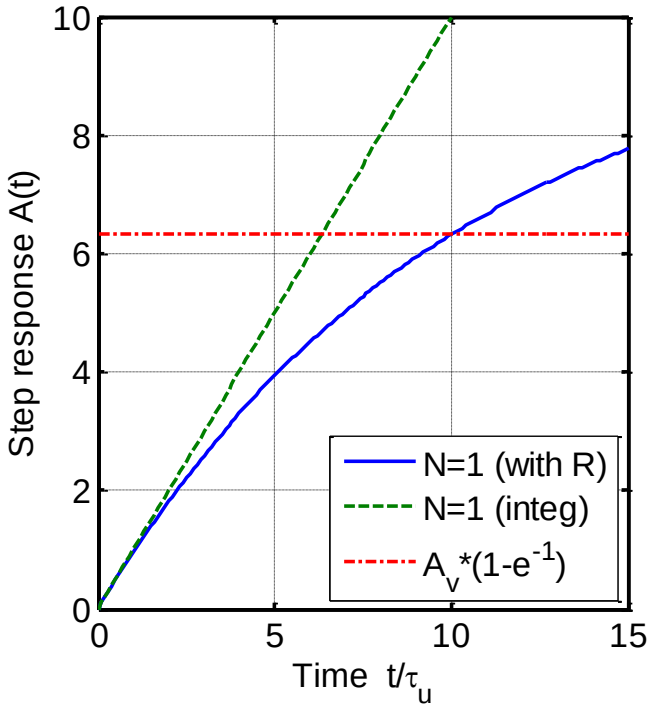


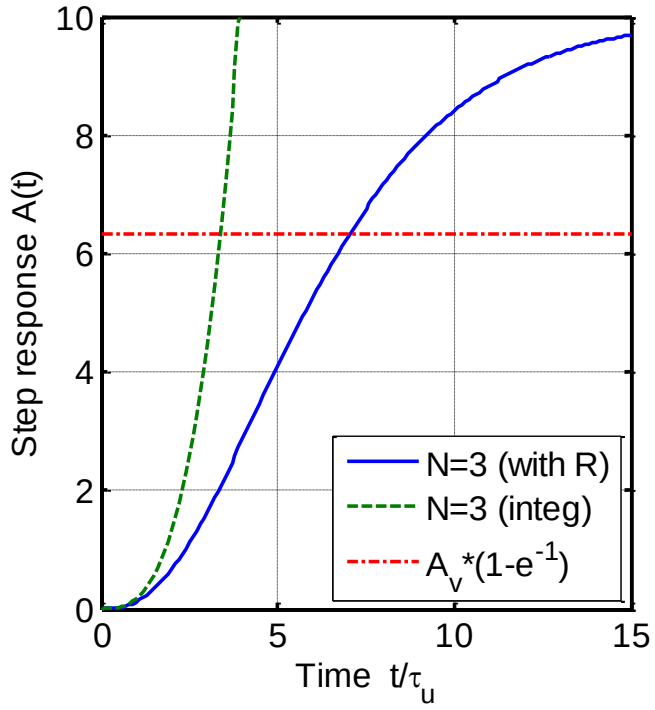
- Intuition
  - Load resistors (in cascade of open loop amplifiers) shunt current away from load capacitance; this slows down amplification
  - Drop assumption $A_v=A_0^N$ to see what happens…
- Analysis

$$v_{o1} = \frac{g_m}{sC} v_{in} = \frac{\omega_u}{s} v_{in} \qquad v_{oN} = \frac{\omega_u^N}{s^N} v_{in}$$

Cascade of "Integrators" (2)

$$V_{\text{out}}(s) = \frac{V_{\text{istep}}}{s}\frac{\omega_u^N}{s^N} \qquad V_{out}(t) = V_{\text{istep}} \cdot \omega_u^N \frac{t^N}{N!}$$





Cascade of "Integrators" (3)

- Cascade of integrators achieves faster amplification than cascade of resistively loaded stages
- Delay time

$$\tau_d = \tau_u[(N! \cdot A(\tau_d))]^{1/N} \qquad A(\tau_d) = \frac{V_{\text{out}}(\tau_d)}{V_{\text{instep}}}$$

- Optimum number of stages approximately given by

$$N_{\text{opt}} = 1.1 \ln[A(\tau_d)] + 0.79$$ [Wu, JSSC 12/1988)

- Effective gain per stage is still relatively close to e=2.7183…