

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

B. E. BOSER

Midterm Exam

EECS 240C

Name: _____

SID: _____

Score: **/100**

- **One (1) 8 ½” by 11” sheet of handwritten notes (no copies)**
- **Closed books**
- **Mark all results with a box around.**
- Write solutions on the exam sheets. Add extra pages where needed.
- Simplify algebraic results as much as possible.
- Bring into standard form where applicable.
- Show derivations.

Useful Expressions:

$$\cos^2 x = \frac{1}{2} + \frac{1}{2} \cos 2x$$

$$\cos^3 x = \frac{3}{4} \cos x + \frac{1}{4} \cos 3x$$

$$\cos^4 x = \frac{3}{8} + \frac{1}{2} \cos 2x + \frac{1}{8} \cos 4x$$

1. (20 points) Find the maximum pulse duration at the output of a DAC that results in no more than 1dB attenuation for inputs at half the sampling frequency f_s . Express your result as a function of f_s .

2. (20 points) Compute the spurious-free dynamic range in dB of an A/D converter sampling at 10MHz with a 1V peak-to-peak sinusoidal input at 3MHz. The converter has negligible quantization noise but distorts its input as follows:

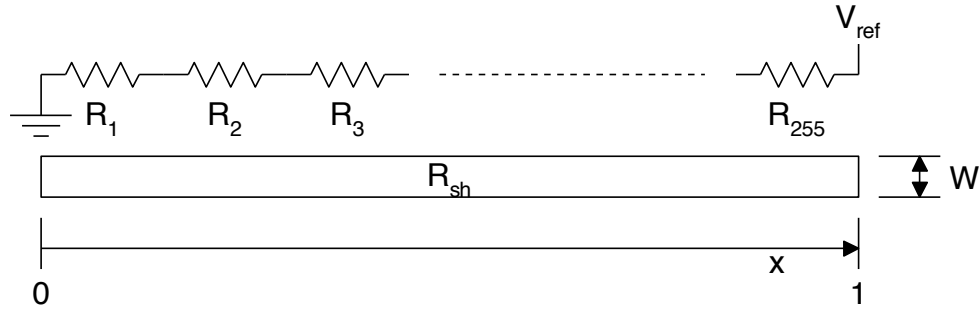
$$V_{in} + \alpha V_{in}^2 + \beta V_{in}^3$$

with $\alpha=0\text{V}^{-1}$, $\beta=0.05\text{V}^{-2}$.

3. (20 points) The layout of the reference ladder of an 8-bit DAC is shown conceptually below. Due to a process gradient, the sheet resistance R_{sh} of the resistor material is position dependent according to the following equation:

$$R_{sh}(x) = R_o(1 + \alpha x)$$

with $R_o = 1.5 \Omega/\square$ and $\alpha = 0.08$. Compute the maximum INL error of the converter in LSBs.



4. (20 points) A segmented DAC consists of a unit-element MSB DAC with B_1 bits. The standard deviation of the elements from their nominal value is σ_1 . The number of bits in the binary weighted LSB DAC is B_2 and the standard deviation of the elements is σ_2 . Derive an expression for the standard deviation of the maximum DNL, σ_{DNL} .

5. (20 points) A pipeline ADC consists of (a very large number of) 1-bit stages with inter-stage gain 1.8. Calculate the maximum comparator offset that can be tolerated without performance degradation. Ignore all other error sources.