EE240C: Analog-Digital Interface ICs **2019**

Term Project

(Due 2019/12/13)

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1 Objective

The goal of the project is to deepen and demonstrate your understanding of the topics covered in EE 240C. The objective is to design and implement a behavioral-level design of an analog-to-digital converter meeting the specifications listed below. Multiple ADC architecture could fulfill the specifications.

The behavioral-level design should implement the relevant non-idealities for the selected architecture. Some circuit simulations might be needed to get reasonable values as input to the behavioral model.

For process-related parameters, any CMOS process up to 90 nm with a supply up to 1.2 V is acceptable; generic 45 nm and 90 nm processes are available on the instructional Unix machines.

2 Specifications

Parameter	Description	Value
BW	Bandwidth	$\geq$ 12.5 MHz
DR	Dynamic Range	$\geq$ 70 dB
SNDR	Signal to Noise and Distortion Ratio (at $f_{in} = f_s/2$; optional, extra credit)	$\geq$ 65 dB
P	Power consumption	minimize

3 Teamwork

You may either work alone or in a group of two and submit a joint report. Discussion with others is encouraged, but submit a genuine design.

No exchange of computer code or design files.

4 Deliverables

You are to submit a concise project report that documents your design procedure and obtained results. Your report should be formatted as indicated below (additional pages will not be considered):

1. (2 pages max): Choice of architecture. Survey different options (e.g. using the data at `https://web.stanford.edu/~murmann/adcsurvey.html`) and discuss their advantages and disadvantages with respect to meeting the objectives.

2. (2 pages max): Hand calculations and analysis that the design is based on. Indicate how the power consumption is calculated and minimized.

3. (2 pages max): Functional design and verification in a high-level simulator (e.g. MATLAB and/or Verilog-AMS). The functional design needs to incorporate relevant non-idealities like transistor or capacitor mismatch, noise, etc, …

4. (3 pages max): Testbenches: Devise and evaluate a comprehensive set of simulations (incl. circuit simulation) to verify all design requirements.

5. (1 page max): Summarize the achieved performance in a table and write a short critique of your design.

5 Submission

Submit your report as a PDF document to jpv@berkeley.edu.