EE240C: Analog-Digital Interface ICs **2019**

Midterm Exam

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Name: Solution

SID: _____

Score:

1	2	3	4	5	

- One (1) 8 ½" by 11" sheet of notes (no copies)
- Closed books
- Mark all results with a box around.
- Clearly cross out incorrect results.
- Write solutions on the exam sheets. Add extra pages where needed.
- Simplify algebraic results as much as possible.
- Bring into standard form where applicable.
- Show derivations.

Problem 1. True/False Questions (10 points)

Answer with "T" for a true statement, and with "F" for a false statement; no explanation necessary. (correct: +1; incorrect: -1; unanswered: 0; minimum overall score: 0).

Question	T/F
a) The effective number of bits of an ADC is always an integer.	F
b) Increasing the number of samples used to create an FFT plot helps lower the spectrum's noise floor.	T
c) A thermometer encoded DAC typically exhibits its worst DNL at codes near the center of the transfer characteristic.	F
d) DNL measurements are not affected by noise, only INL measurements are.	F
e) An imbalance in the capacitive loading of a regenerative comparator can lead to input-referred offset.	T
f) Transient dynamic errors, such as sparkles, cannot be detected by a histogram test.	T
g) Bottom-plate sampling improves k T / C noise.	F
h) SNR can be lower than SNDR.	F
i) ADC gain and offset errors do not affect non-linearity measures such as INL and DNL.	T
j) A dynamic comparator does not introduce noise.	F

Problem 2. ADC SNR and BW (10 points)

The dynamic range of an ADC is dominated by thermal noise from the sampler. Technical constraints limit the sampling capacitance to 1 pF.

1. Determine the minimum sampling rate f_s to achieve a SNR of 90 dB for sinusoidal inputs with frequency 0...1 MHz and **zero-to-peak** amplitude of 1 V. Note that the assumption is that the ADC is followed by an ideal digital low pass filter.
2. By what factor does the f_s have to increase to improve the SNR by 1 bit.

1. signal power $S = 1V^2/2$

noise power $N = \underbrace{\frac{4T}{C} \cdot \frac{2}{f_s}}_{\text{PSD after sampling}} \cdot 1\,\text{MHz}$

$$\frac{S}{N} = \frac{1V^2/2}{\frac{4T}{C} \cdot \frac{2}{f_s} \cdot 1\text{MHz}} \geq 10^9$$

$$\Rightarrow f_s \geq 1\,\text{MHz} \cdot \frac{4T}{C} \cdot \frac{4 \cdot 10^9}{1V^2} \approx 16.5\,\text{MHz}$$

2. 1 bit SNR improvement is 6dB

$\Rightarrow$ f_s has to increase by a factor of 4

Problem 3. Sampling (10 points)

What is the result of sampling v(t) at sampling times kT, with $T = 1\,\mu s$?

$$v(t) = 0.5\sin(2\pi \cdot 217\,\text{kHz} \cdot t) + 0.5\sin(2\pi \cdot 783\,\text{kHz} \cdot t)$$

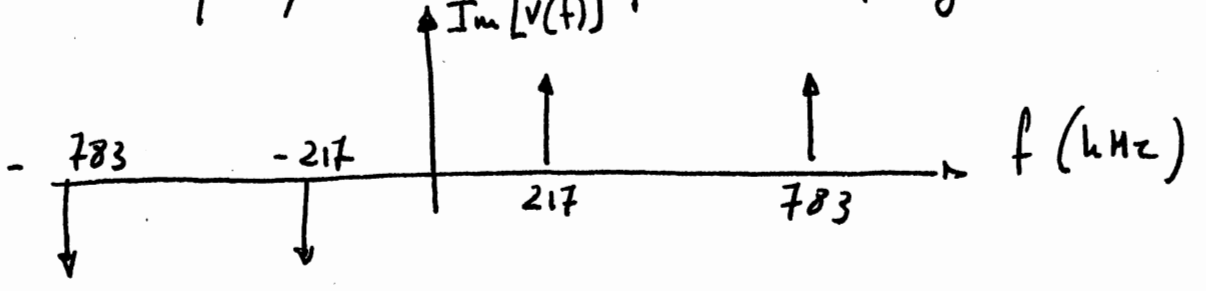
$$= 0.5 \sin(2\pi \cdot 0.217 \cdot k) + 0.5 \sin(2\pi \cdot 0.783 \cdot k)$$

$$= 0.5 \sin(2\pi \cdot 0.217k) + 0.5 \sin(2\pi \cdot 0.783 \cdot k - 2\pi \cdot k)$$

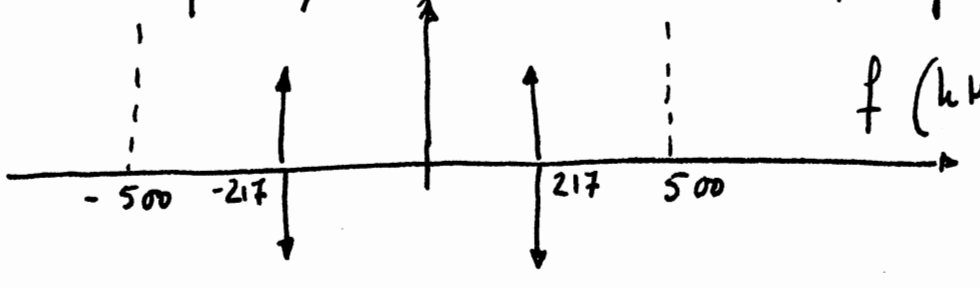
$$= 0.5 \sin(2\pi \cdot 0.217\,k) + 0.5 \sin(-2\pi \cdot 0.217\,k)$$

$$= 0$$

Frequency domain before sampling:



Frequency domain after sampling:



Problem 4. SAR ADC (10 points)

Consider a single-ended SAR ADC switching scheme: the single-ended input is sampled on the top-plate of the capacitors and the bottom-plate of the capacitors is used for feedback, as shown in figure 1. The DAC is a binary-weighted capacitive DAC: $C_1 = 2C_0$, $C_2 = 2C_1$, ... The node OUT is connected to one of the inputs of a comparator.

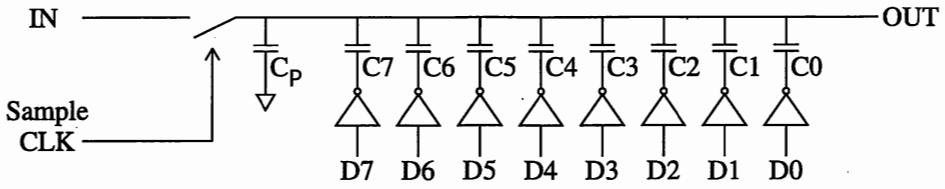


Figure 1: SAR ADC DAC array

1. Using charge conservation, write the voltage on node OUT as a function of the input voltage during the sampling phase, the DAC feedback during the sampling, and the DAC feedback during the SAR algorithm phase. The DAC feedback D7-D0 can be represented as a single voltage V_{DAC} (which would need to be defined).

2. How does a parasitic capacitor C_p influence the input-output characteristic of this SAR ADC?

1. $C_{DAC}(V_{IN} - V_{DAC}^0) + C_p V_{IN}$

$= C_{DAC}(V_{OUT} - V_{DAC}) + C_p V_{OUT}$

$\Rightarrow V_{OUT} = V_{IN} + \frac{C_{DAC}}{C_{DAC} + C_p}(V_{DAC} - V_{DAC}^0)$

$C_{DAC} = C_7 + C_6 + \ldots + C_0 = 255\, C_0$

$V_{DAC} = \frac{\sum C_k D_k V_{ref}}{\sum C_k}$

$= V_{ref} \sum_{k=0}^{7} \frac{C_k}{C_{DAC}} D_k \quad \text{with } D_k \in \{0,1\}$

2. After convergence of the SAR algorithm:

$$V_{OUT} \approx V_{ref}^{comparator}$$

$$\Rightarrow V_{IN} = -\frac{C_{DAC}}{C_{DAC}+C_P}\left(V_{DAC} - V_{DAC}^{0}\right) + V_{ref}^{comp}$$

$$V_{DAC} = V_{ref}\frac{\sum C_k D_k}{C_{DAC}}$$

$$= \frac{C_{DAC}+C_P}{C_{DAC}}\left(V_{IN} - V_{ref}^{comp}\right) - V_{DAC}^{0}$$

C_P leads to a gain error of C_P/C_{DAC} (and potentially an offset error depending on the choice of V_{DAC}^{0} & $V_{ref}^{comparator}$)

Problem 5. Regenerative latch (10 points)

1. A regenerative latch with two cross-coupled transistors each having a transconductance g_m and each having a capacitive load C_L has a regeneration time constant equal to C_L/g_m.

   If the regenerative latch additionally has a coupling capacitor C_c between the two sides, as shown in figure 2, what is the regeneration time constant ?

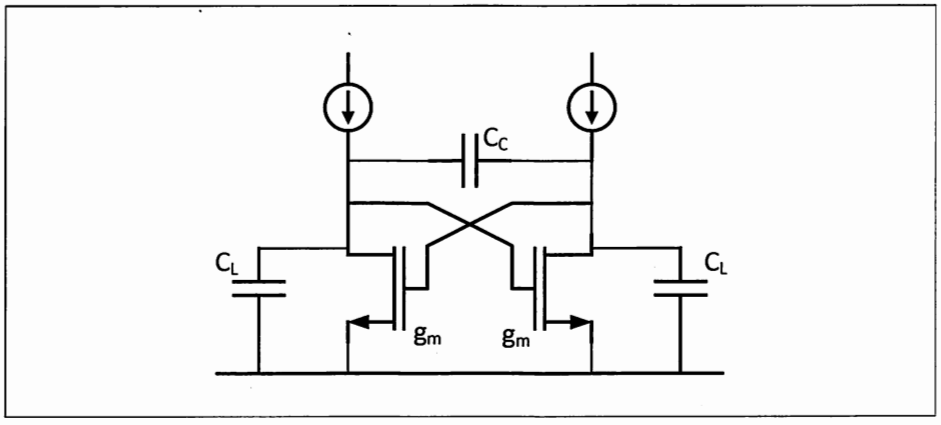


Figure 2: Comparator

2. A regenerative comparator with a latch time-constant of 20 ps is used in a 6-bit flash converter. If the comparator pre-amplifier has a gain of 5, and $V_{FS} = V_{DD}$, what is the maximum ADC clock speed for a metastability error probability lower than 10^{-12} ?

1. Differential equations:

$$\begin{cases} C_L \frac{dV_1}{dt} + C_C \frac{d(V_1 - V_2)}{dt} + g_m V_2 = 0 \\ C_L \frac{dV_2}{dt} + C_C \frac{d(V_2 - V_1)}{dt} + g_m V_1 = 0 \end{cases}$$

$$C_L \frac{d(V_1 - V_2)}{dt} + 2C_C \frac{d(V_1 - V_2)}{dt} = -g_m (V_1 - V_2) = 0$$

$$\tau = \frac{C_L + 2C_C}{g_m}$$

(this result can also be derived from the differential half-circuit by inspection)

2. $$P_E = \frac{1}{A_V} \frac{V_{DD}}{\frac{1}{2}\frac{V_{FS}}{2^B}} e^{-T/2\tau}$$

$$\Rightarrow f_S \leq \frac{1}{2\tau} \frac{1}{\log \frac{1}{P_E} \frac{1}{A_V} \frac{V_{DD}}{\frac{1}{2}\frac{V_{FS}}{2^B}}}$$

$$= \frac{1}{40ps} \frac{1}{\log \frac{10^{12}}{5} 2^7}$$

$$\approx 810 \text{ MHz}$$