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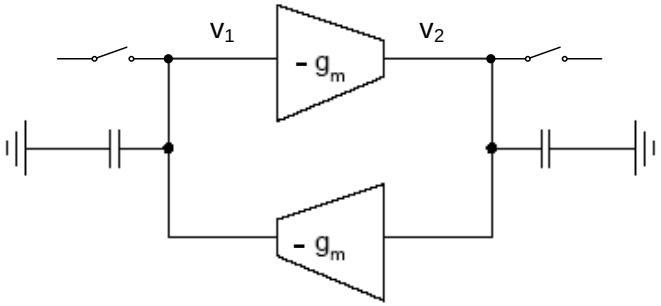
Analog-Digital Interface Integrated Circuits

Comparators – Latch

Regenerative Sense Amplifier (Latch)

$t < 0$ setup initial condition $v_{10} - v_{20} = v_{d0}$

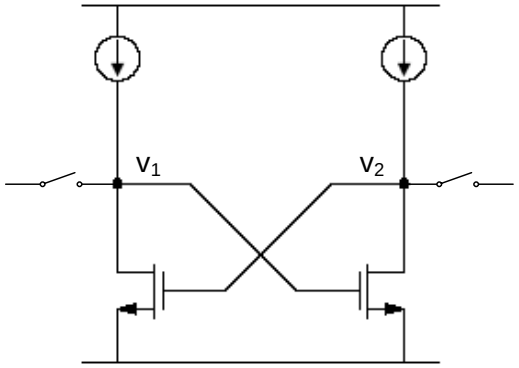
$t \geq 0$ enable positive feedback



$$\frac{dv_1}{dt} = \frac{i_1(t)}{C} = \frac{-g_m v_2(t)}{C}$$

$$\frac{dv_2}{dt} = \frac{i_2(t)}{C} = \frac{-g_m v_1(t)}{C}$$

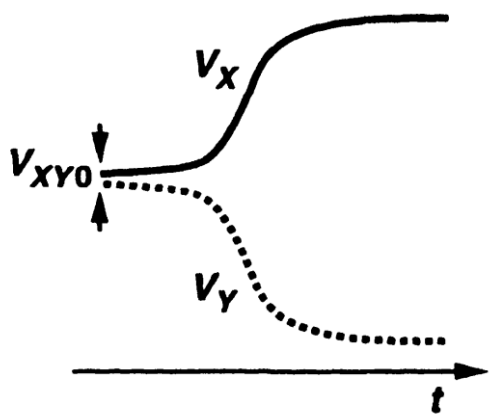
$$\tau_u = \frac{C}{g_m}$$

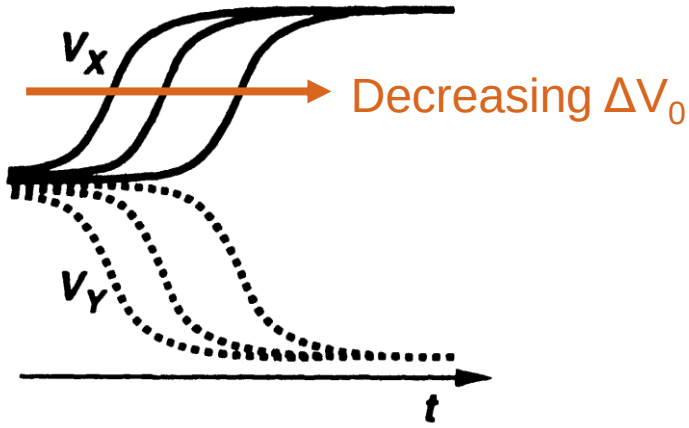


$$\Rightarrow v_1(t) - v_2(t) = v_d(t) = v_{d0} \cdot e^{t/\tau_u}$$

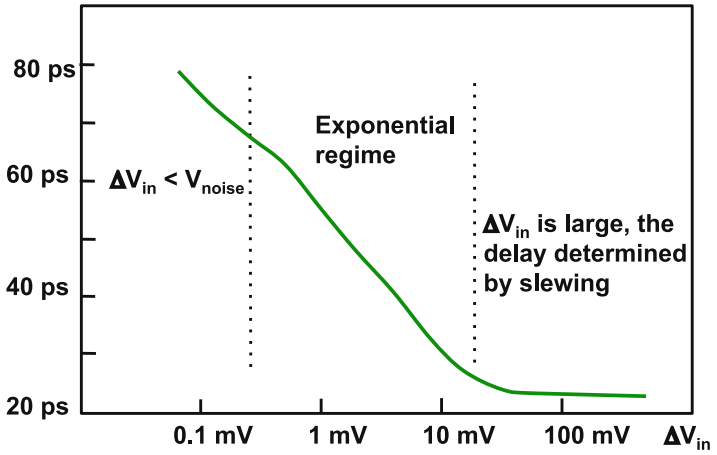
$$\Rightarrow A(t) = \frac{v_d(t)}{v_{d0}} = e^{t/\tau_u}$$

Regenerative Sense Amplifier (Latch)



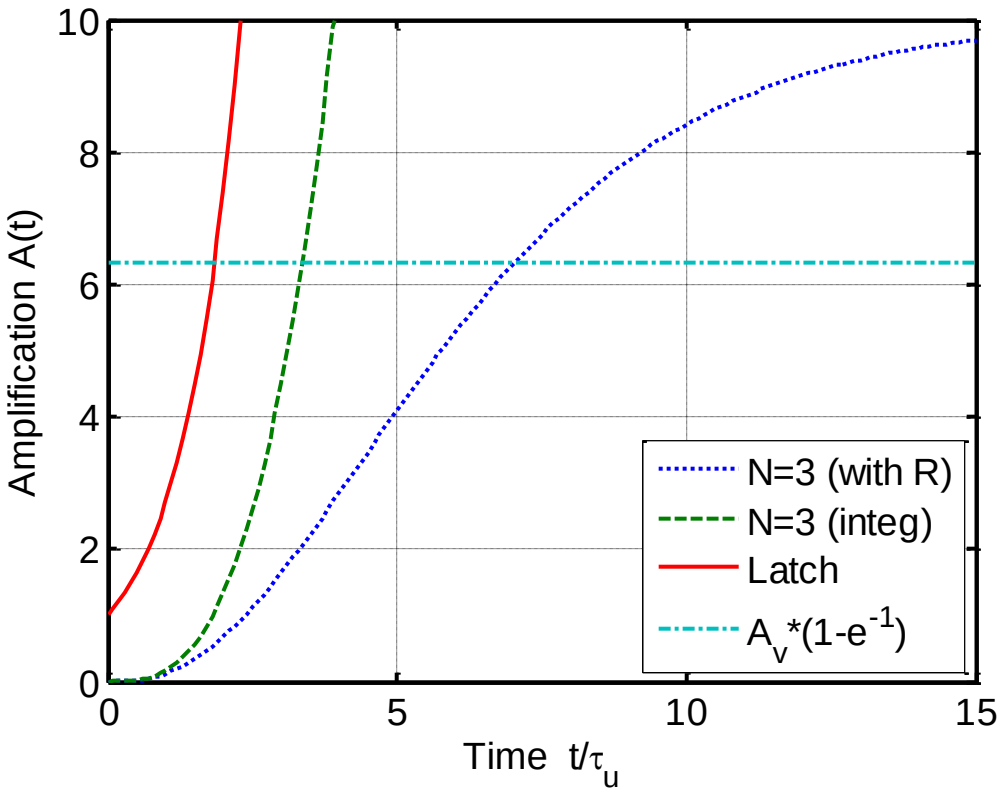


[Razavi, "Principles of Data Conversion System Design"]



[Pelgrom, "Analog to Digital Conversion", 3rd Ed]

Comparison



- Latch is much faster than cascade of amplifiers/integrators

Latch "Gain"

$A(\tau_d)$	τ_d/τ_u
10	2.3
100	4.6
1,000	6.9
10,000	9.2

Metastability (1)

- References
  - H. J. Veendrick, "The behaviour of flip-flops used as synchronizers and prediction of their failure rate," *JSSC*, Apr. 1980
  - P. M. Figueiredo, "Comparator metastability in the presence of noise," *TCAS-I*, May 2013.
- Consider minimum initial latch input voltage needed to regenerate to V_{DD} within maximum available time T_{max}

$$V_{d0\min} = \frac{V_{DD}}{e^{T_{max}/\tau_u}}$$

- Minimum required pre-amplifier input:

$$V_{id0\min} = \frac{1}{A_v}\frac{V_{DD}}{e^{T_{max}/\tau_u}}$$

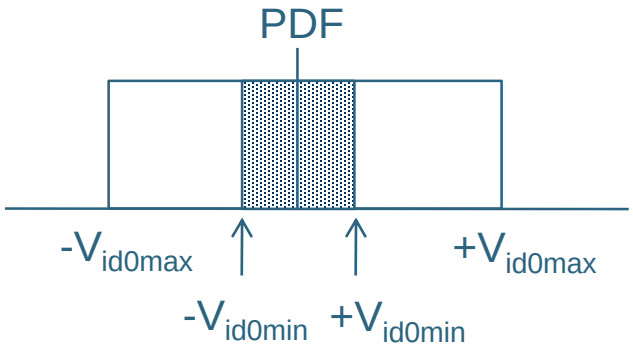
- Probability of seeing a metastable output:

$$P(\text{Error}) = P(|V_{id0}| < V_{id0\min})$$

Metastability (2)

- Assuming a uniform input signal distribution over some range, we have

$$P(\text{Error}) = \frac{V_{id0min}}{V_{id0max}}$$



- In a *flash ADC*, only one out of all comparators can be metastable. The effective input range V_{id0max} over which the signal is distributed is therefore ½ LSB ($\Delta/2$)

$$\therefore P(\text{Error}) = \frac{V_{id0min}}{V_{id0max}} = \frac{\frac{1}{A_v}\frac{V_{DD}}{e^{T_{max}/\tau_u}}}{\frac{\Delta}{2}} = \frac{\frac{1}{A_v}\frac{V_{DD}}{e^{T_{max}/\tau_u}}}{\frac{V_{FS}}{2\cdot 2^B}} = \frac{2^{B+1}}{A_v}\frac{V_{DD}}{V_{FS}}e^{-T_{max}/\tau_u}$$

Metastability (3)

- Example: 6-bit, 500MHz Flash ADC, $T_{max}=T_s/2=1ns$, $\tau_u=1/(2\pi\cdot 5GHz)=32ps$, $A_v=3$, $V_{FS}=0.5V_{DD}$

$$P(\text{Error}) = \frac{2^{6+1}}{3} \cdot 2 \cdot e^{-1000/32} \cong 2 \cdot 10^{-12}$$

- Mean time to failure (MTF)

$$MTF = \frac{1}{P(\text{Error}) \cdot f_s} = \frac{1}{2 \cdot 10^{-12} \cdot 0.5 \cdot 10^9} s = 1000s \cong 16 \text{ minutes}$$

- Ideally design for MTF > 1…10 years (not always possible)
- Can improve MTF by
  - Reducing speed (larger T_{max}/τ_u)
    - Exponential dependence
  - Adding pre-amplifier gain
    - Linear dependence

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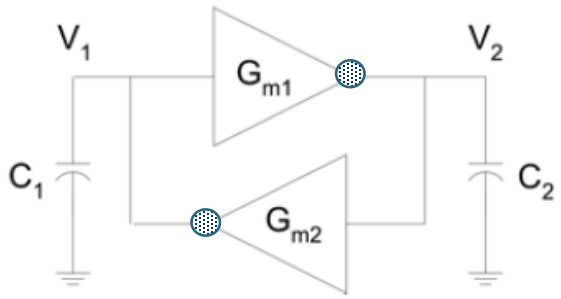
Comparators – Offset

Dynamic Offset



$$\Delta C = C_1 - C_2$$

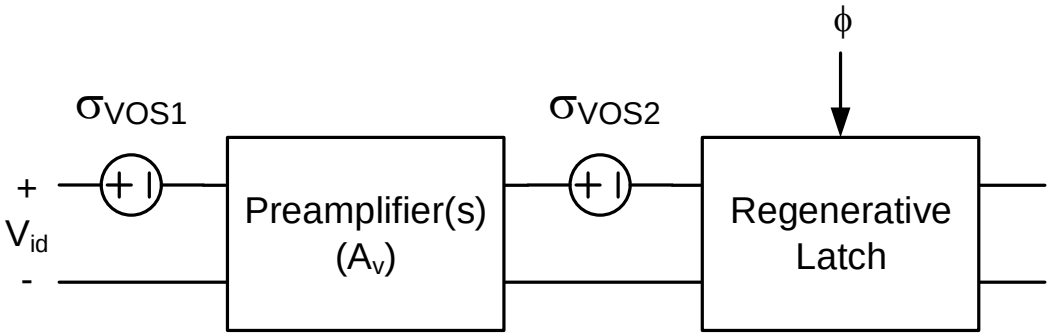
- $C_1 \neq C_2$ causes dynamic offset:
- Can show $V_{os} \cong 0.5 \cdot \Delta C/C \cdot (V_{(t=0)} - V_S)$;
  V_S = inverter switching voltage
  - Nikoozadeh & Murmann, IEEE TCAS II, Dec. 2006.
- Example
  - 0.5·10fF/100fF·(1V–0.5V)= 25mV (!)
    → symmetrical layout (incl. routing !)

Dynamic Offset

- Dynamic offset can be caused by signal-dependent capacitive loading of the comparator
  → capacitive load depends on previous decision
  → comparator hysteresis

- Example: logic gates being driven by comparator

Input Referred Offset



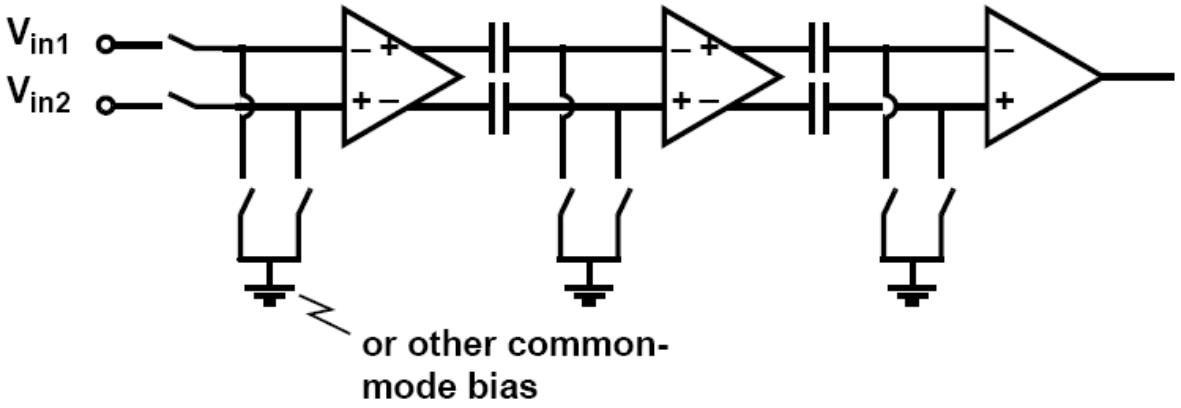
$$\sigma_{VOS}^2 = \sigma_{VOS1}^2 + \frac{1}{A_v^2}\sigma_{VOS2}^2$$

- Example: σ_{VOS1}=3mV, σ_{VOS2}=30mV, A_v=10

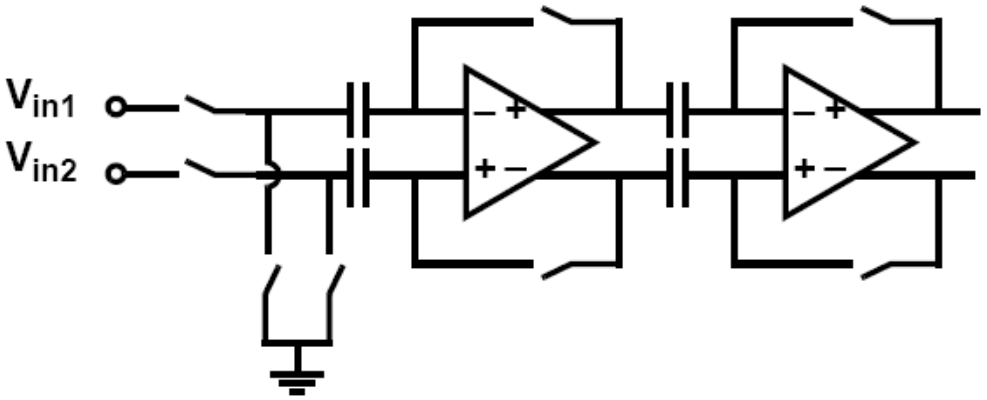
$$\sigma_{VOS} = \sqrt{(3mV)^2 + \frac{1}{10^2}(30mV)^2} = 4.2mV$$

Offset Cancellation

OUTPUT SERIES CANCELLATION

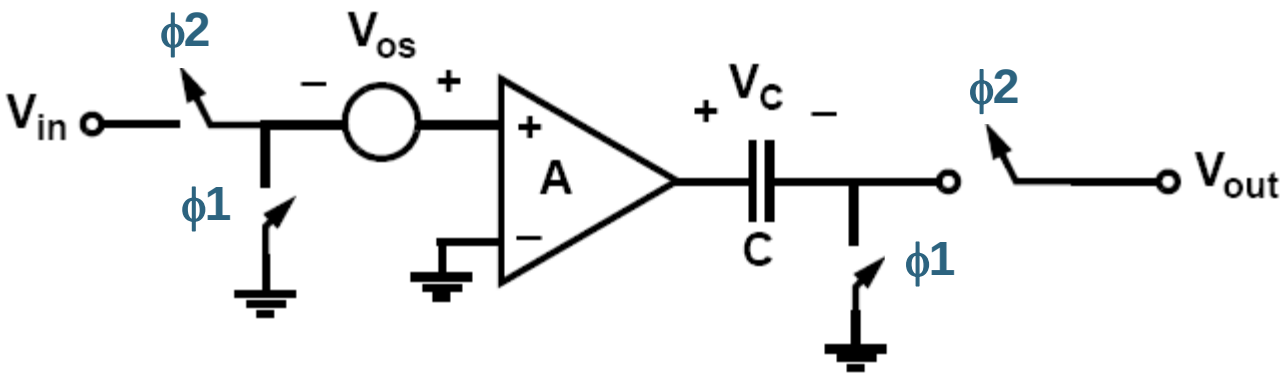


INPUT SERIES CANCELLATION



Output Series Cancellation

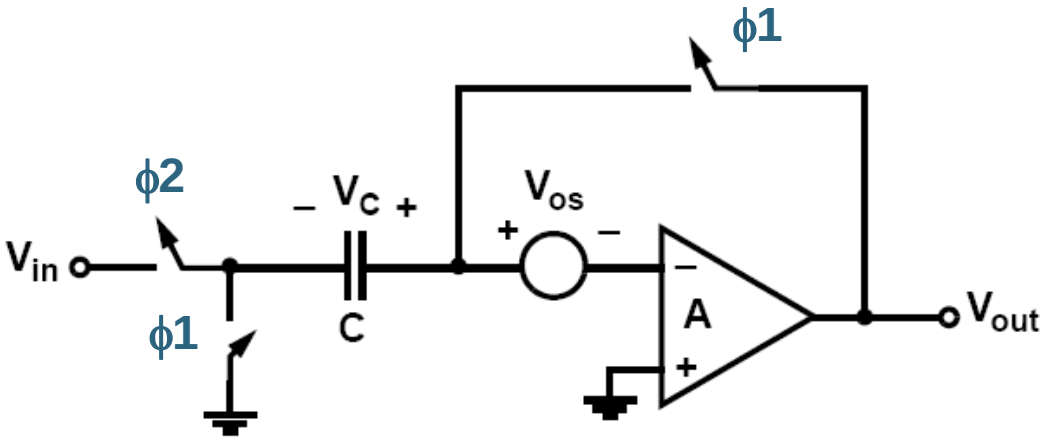
Ref: Poujois, et al., JSSC 8/78



- Phase 1: Offset storage, phase 2: Amplify
- Design considerations
  - Must ensure that amplifier does not saturate during phase 1
  - Must make C sufficiently large to avoid attenuation and mitigate charge injection error

Input Series Cancellation

Refs: McCreary & Gray
Yee, et al.



- Phase 1: Offset storage, phase 2: Amplify
- In phase 2, input referred offset is ≈Vos/(A+1)
  - 4x reduction if A=3

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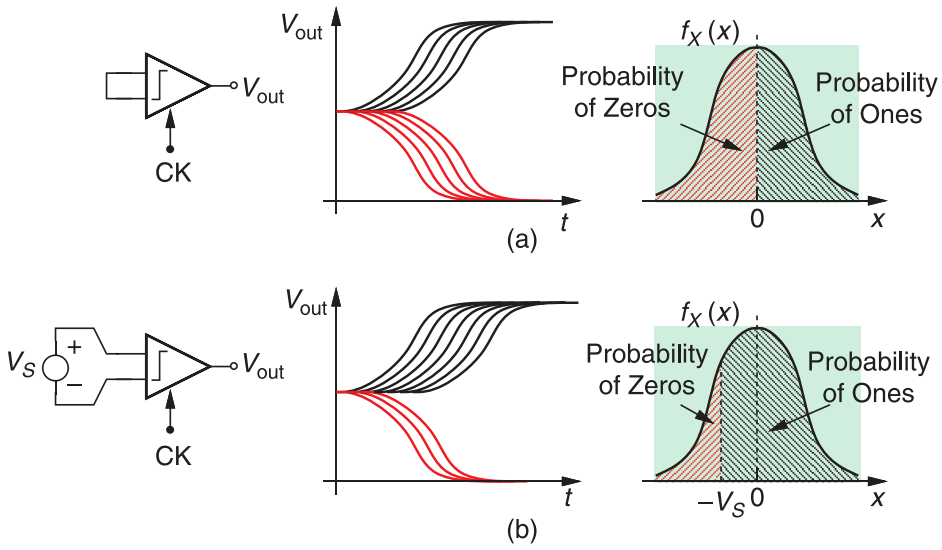
Comparators - Noise

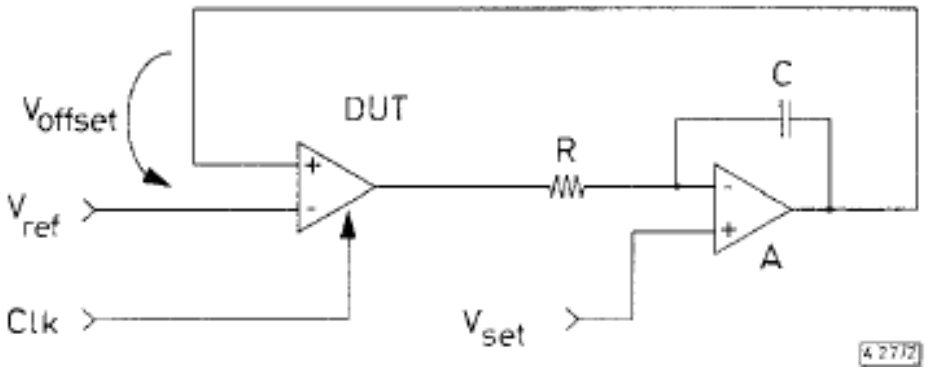
Noise in Comparators

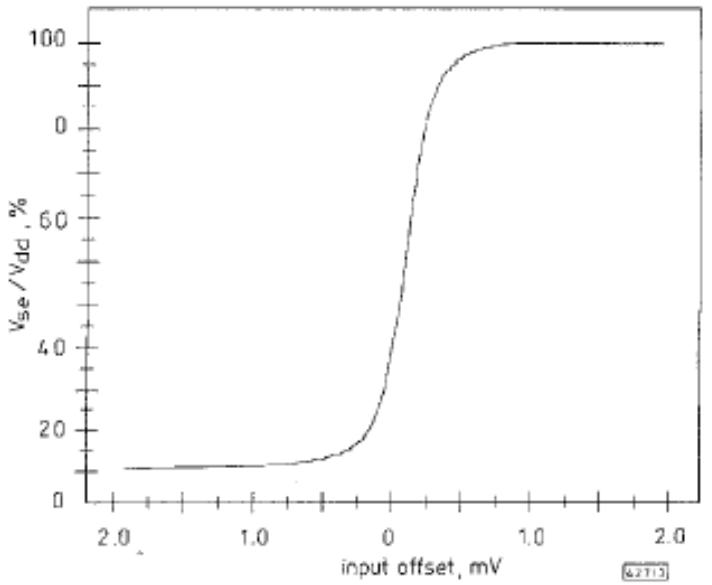
- Comparator noise randomizes decisions around transition point
  - At transition point: $P_0 = P_1 = 0.5$
  - $P_0 = 1 - P_1$ increases below transition point; $P_1 = 1 - P_0$ increases above transition point
- P_0, P_1 as a function of (cumulative) distribution function of comparator noise



$$P_0 = P(V_{in} + v_n \le 0) = P(v_n \le -V_{in}) = F_{v_n}(-V_{in})$$

$$P_1 = P(V_{in} + v_n \le 0) = P(v_n \le -V_{in}) = 1 - F_{v_n}(-V_{in})$$





[I. Opris, "Noise estimation in strobed comparators," Electronics Letters, vol. 33, no. 15, pp. 1273–1274, Jul. 1997]

- Comparator has a noisy transition region between 0 and 1
- Usually dominated by noise of pre-amplifier

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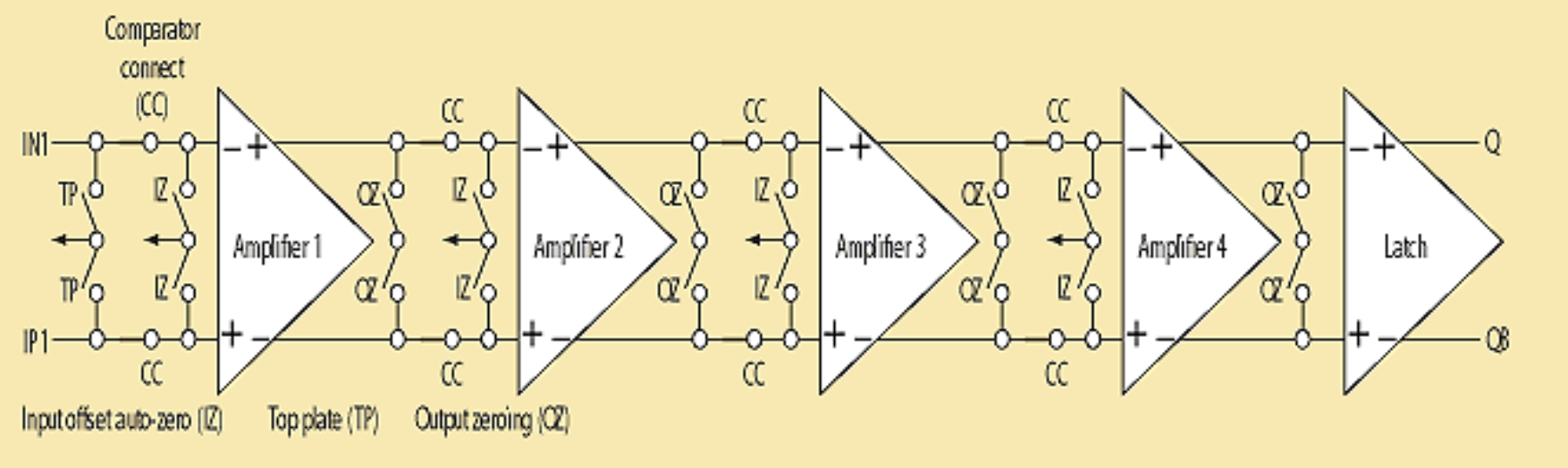
Comparators - Examples

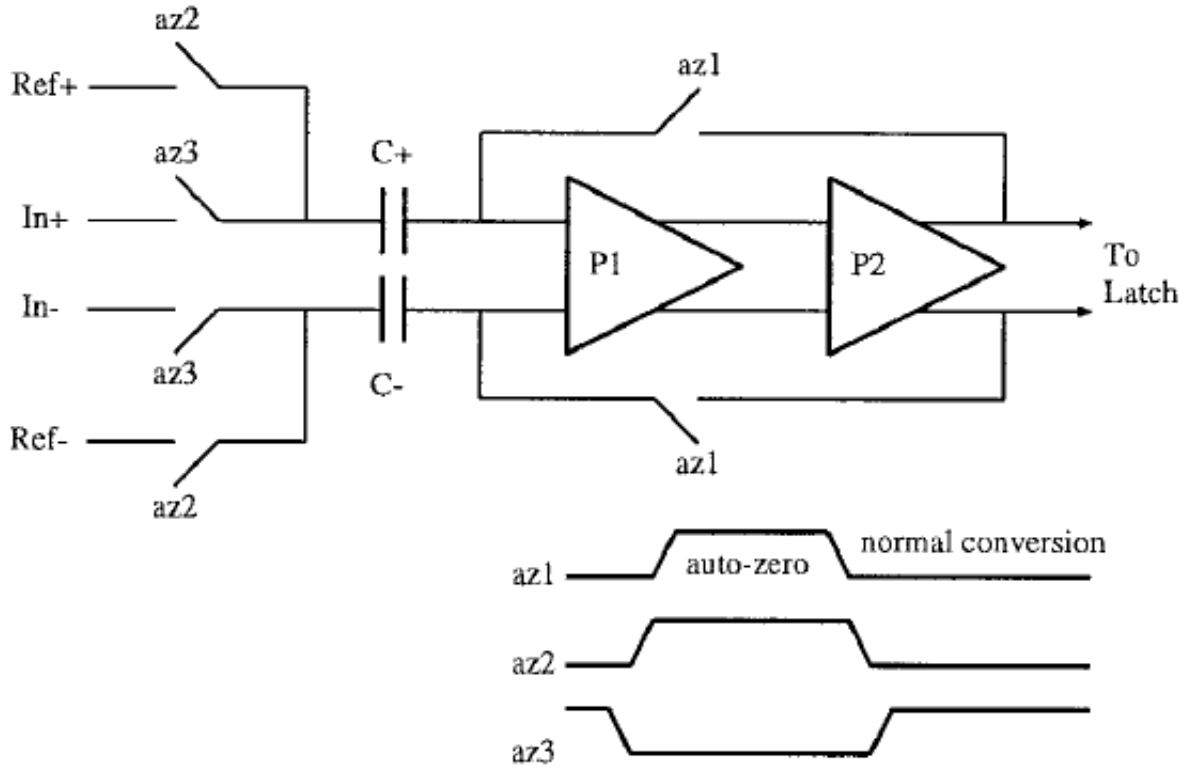
Commercial Example: AD7671



- Used in 16-bit, 1 MS/s successive approximation ADC, 0.6 μm CMOS technology
- Uses cascaded output series offset cancellation
- Offset <3 mV (over process, temperature)

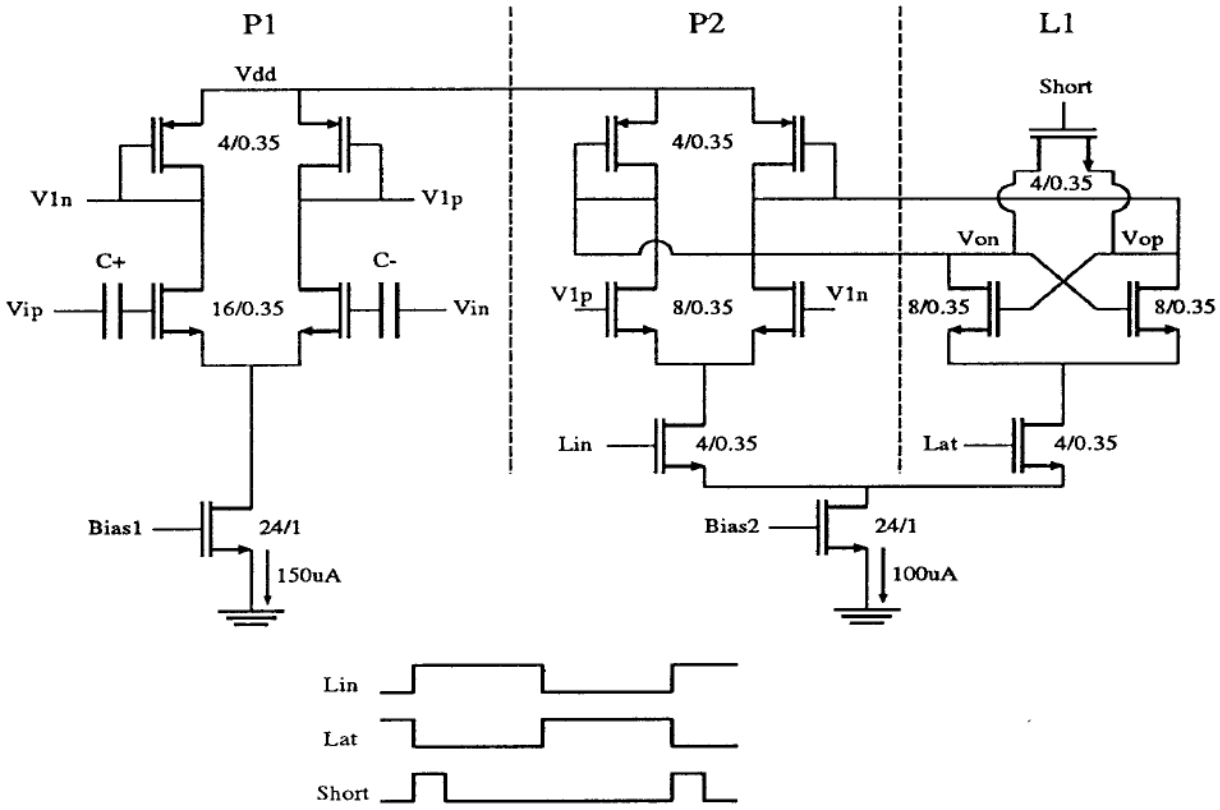
Comparator Examples (1a)

- Mehr & Dalton, JSSC 7/1999



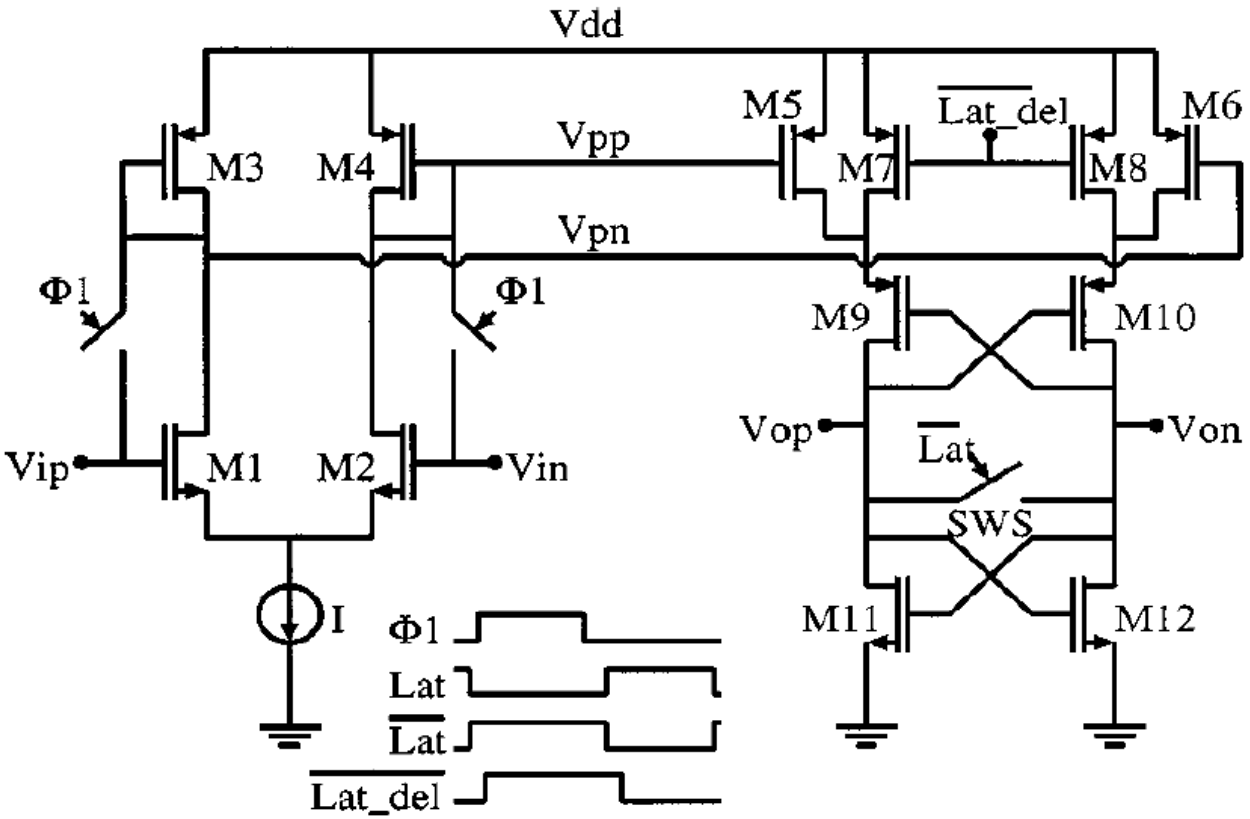
Comparator Examples (1b)

- Mehr & Dalton, JSSC 7/1999



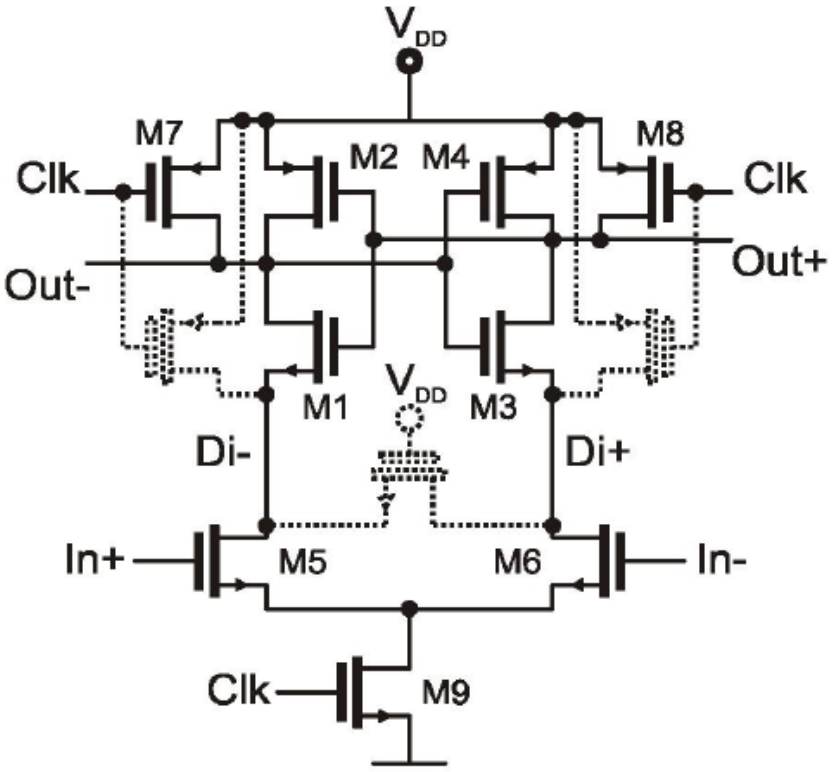
Comparator Examples (2)

- Mehr & Singer, JSSC 3/2000



Comparator Examples (3a)

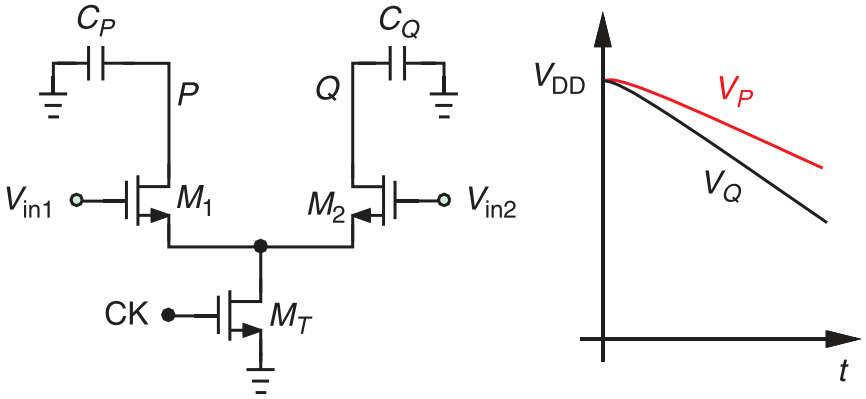
- Purely dynamic "sense amplifier"
  - No DC current
  - Headroom problems with low V_{DD}
  - Sensitive to V_{icm}
  - Offset–speed tradeoff:
    - Narrow M9 for low offset
    - Wide M9 for high speed



[B. Razavi, "The StrongARM latch", IEEE Solid- State Circuits Mag., vol. 7, no. 2, pp. 12–17, Spring 2015]

StrongARM Latch

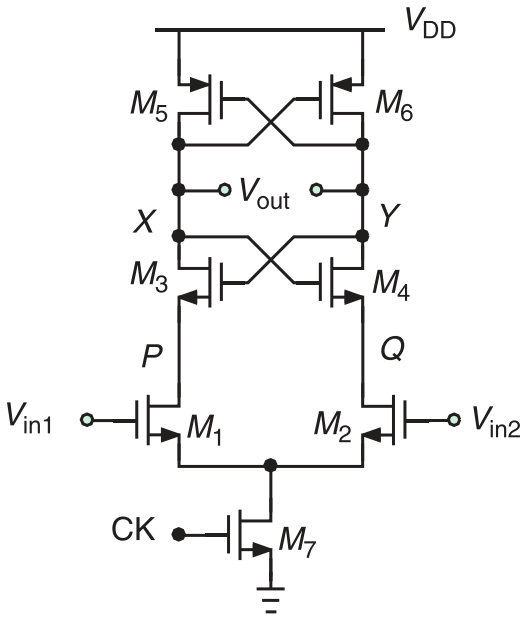
- Phase 0: Reset → internal latch nodes reset to V_{DD}
- Phase 1: Dynamic amplification

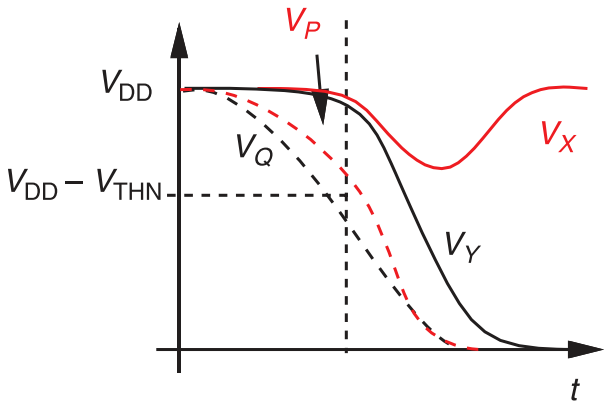


  - $\Delta T_1 = \frac{C_P V_{thn}}{I_{tail}/2}$
  - Dynamic amplification: $A_v = \frac{g_{m1,2}}{C_P} \Delta T_1 = \frac{g_{m1,2} V_{thn}}{I_{tail}/2}$
  - Dynamic input-referred offset: $V_{offset} \approx \Delta C_P \frac{V_{thn}}{g_{m1,2} \Delta T_1} = \frac{\Delta C_P}{C_P} \frac{I_{tail}/2}{g_{m1,2}}$
  - Input-referred noise: $v_n^2 \approx (2 \frac{k T}{C_P} + 2 \frac{4kT\gamma g_{m1,2}}{C_P^2} \Delta T_1)/A_v^2$

StrongARM Latch

- Phase 3: Regeneration
  - Phase 3a: cross-coupled NMOS only
  - Phase 3b: cross-coupled NMOS & PMOS

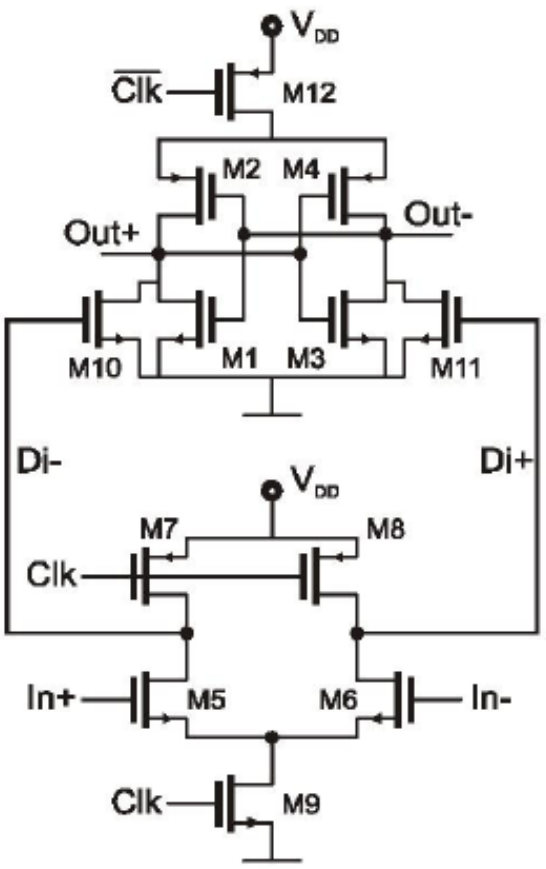




- Power consumption: $P \approx f_{\text{clock}}(2C_{\text{P}} + C_{\text{L}})V_{DD}^2$

Comparator Examples (3b)

- Schinkel, ISSCC 2007: "Double tail sense amplifier"



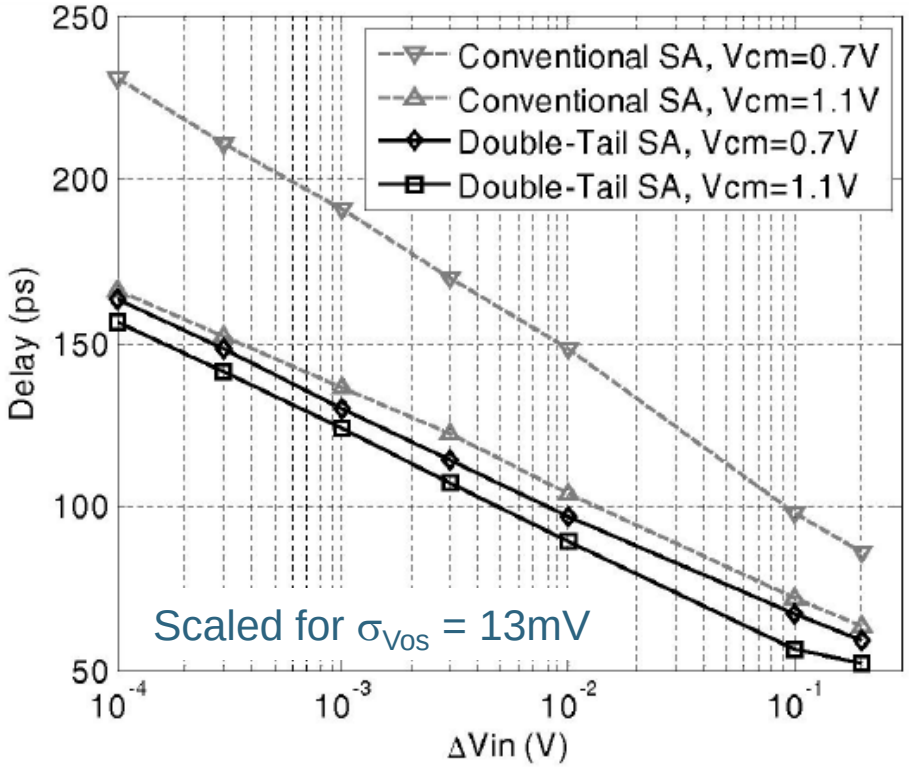


Figure 17.7.3: Simulated sense amplifier delays versus differential input voltage. The delay is the time between the clock edge and the instant when ΔOut crosses 1/2 V_{DD}.

Narrow M9 (low offset) and wide M12 (fast)

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1. R. Poujois and J. Borel, "A Low Drift Fully Integrated MOSFET Operational Amplifier," *IEEE J. of Solid-State Circuits*, pp. 499-503, Aug. 1978.
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4. Y. S. Yee, L. M. Terman and L. G. Heller, "A 1mV MOS Comparator," *IEEE J. of Solid-State Circuits*, vol. SC-13, pp. 294-297, June 1978.
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6. B. J. McCarroll, C. G. Sodini, and H.-S. Lee, "A High-Speed CMOS Comparator for Use in an ADC," *IEEE J. of Solid-State Circuits*, vol. 23, pp. 159-165, Feb. 1988.
7. J.-T. Wu and B. A. Wooley, "A 100-MHz Pipelined CMOS Comparator," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1379-1385, Dec. 1988.
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Selected References (2)

9. M. Choi and A. A. Abidi, "A 6-b 1.3-GSample/s A/D converter in 0.35-μm CMOS," *IEEE J. Solid-State Circuits,* pp. 1847-1858, Dec. 2001.
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16. D. Schinkel et al., "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," ISSCC Dig. Techn. Papers, pp. 314-315, 2007.
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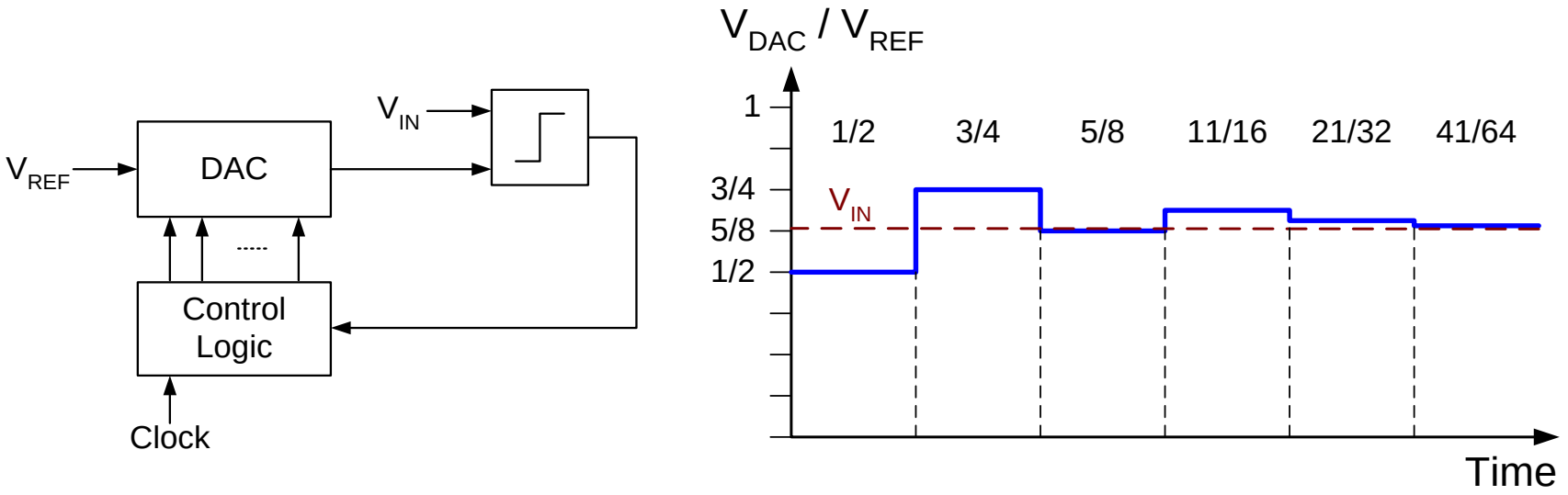
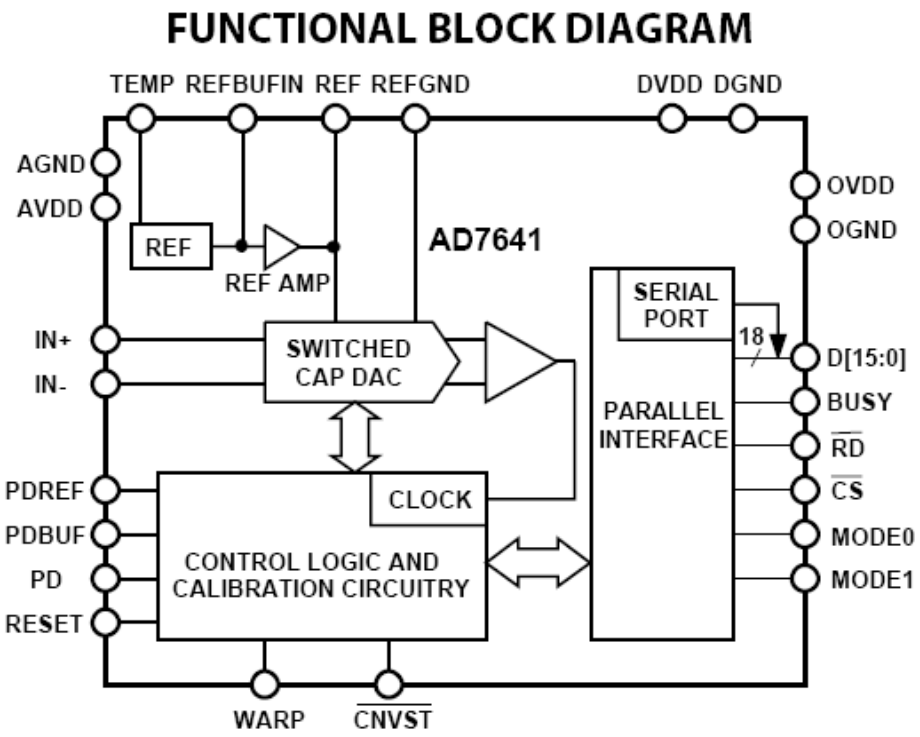
Successive Approximation ADC

Successive Approximation Register ADC



- Binary search over DAC output
- High accuracy achievable (16+ Bits)
  - Relies on highly accurate comparator
  - No amplifier
- Moderate speed (1++ MHz)

High Performance Example

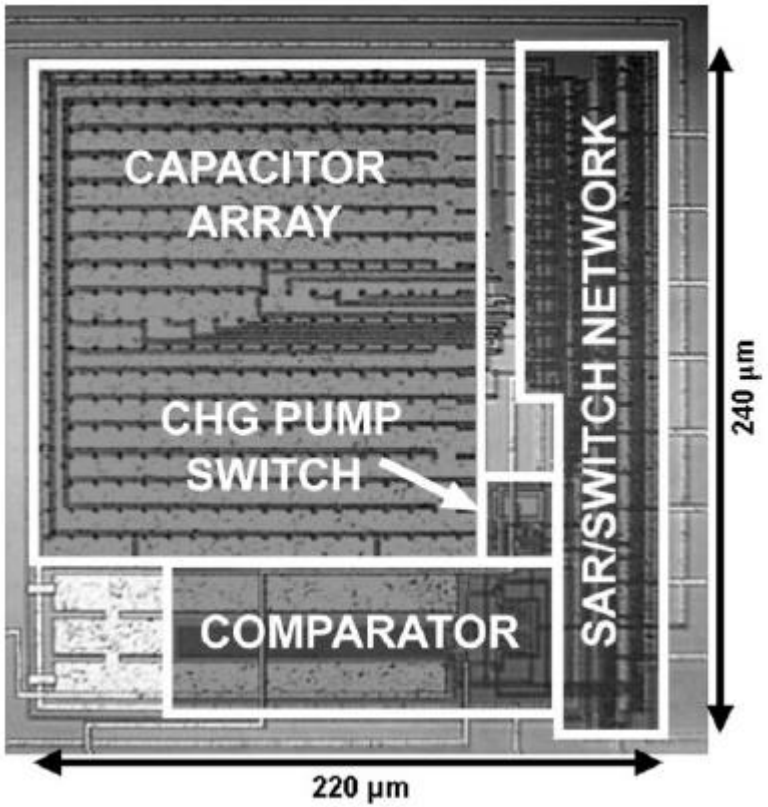


FEATURES

Throughput:
- 2 MSPS (Warp mode)
- 1.5 MSPS (Normal mode)

18-bit resolution with no missing codes
2.048V internal low drift refernce
INL: ±2 LSB typical
S/(N+D): 93 dB typical @ 20 kHz
THD: –115 dB typical @ 20 kHz
Differential input range: ±V_{REF} (V_{REF} up to 2.5 V)
No pipeline delay (SAR architecture)
Parallel (18-, 16-, or 8-bit bus)
Serial 5 V/3.3 V/2.5 V interface
SPI®/QSPI™/MICROWIRE™/DSP compatible
Single 2.5 V supply operation
Power dissipation: 65 mW typical @ 2 MSPS

Low Power Example



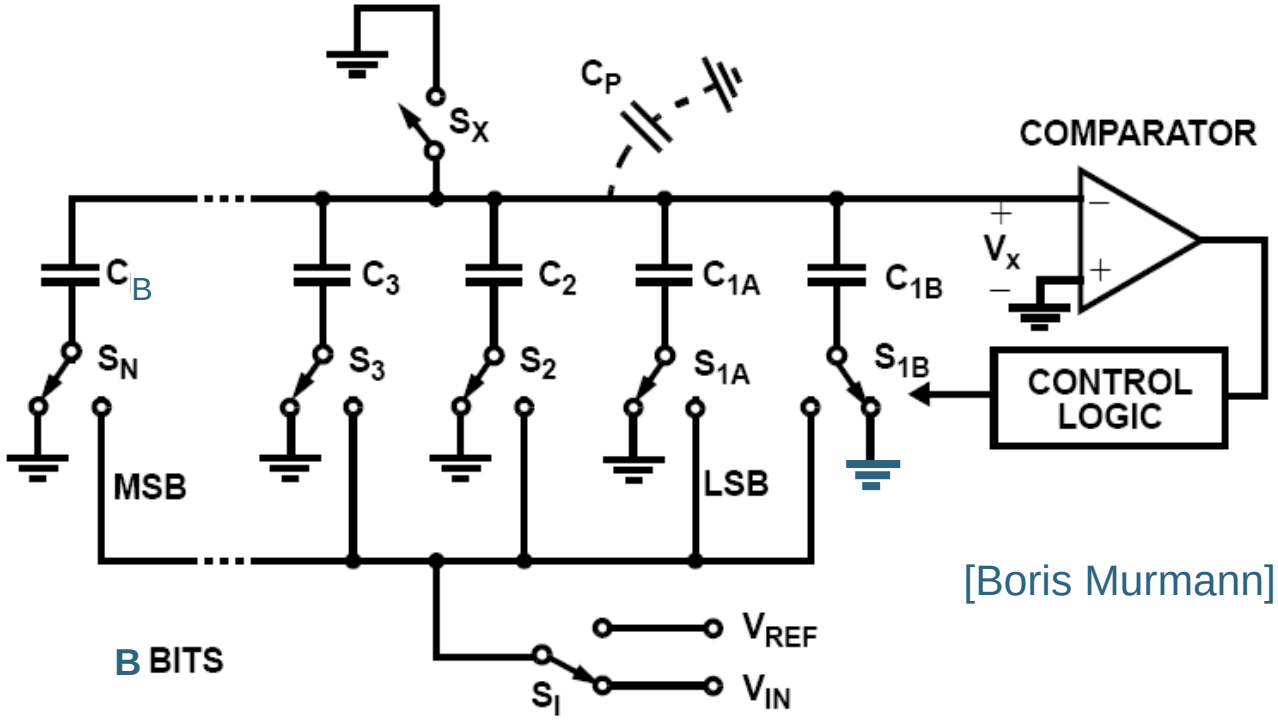
SUMMARY OF ADC PERFORMANCE

Performance Metric	Value
Voltage supply	1 V (nominal)
Input range	Rail-to rail
Sampling rate	100 kHz
Unit capacitance	12 fF
DNL	< ± 0.5 LSB typical
INL	< ± 0.5 LSB typical
ENOB (1V)	7.9 (DC), 7.0 (4.61 kHz)
Power dissipation (1V)	3.1 µW
Energy per sample (1V)	31 pJ
Standby power (1V)	70 pW
Die area (active)	0.053 mm^2
Process	0.25 µm CMOS (2P5M)

M.D. Scott, B.E. Boser, K.S.J. Pister, "An ultralow-energy ADC for Smart Dust," IEEE J. Solid-State Circuits, pp. 1123 -1129, July 2003.

Implementation

- See e.g. [McCreary, JSSC 12/1975]

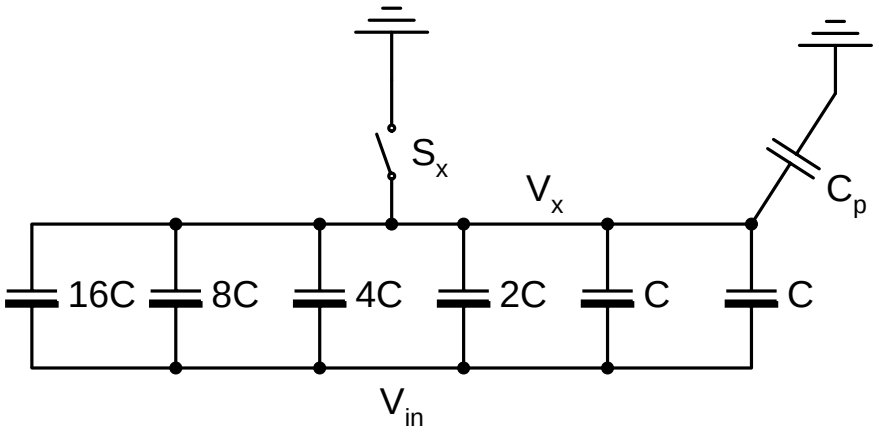


[Boris Murmann]

$$C_{1A} = C_{1B} = C \qquad C_2 = 2C \qquad C_3 = 4C \qquad C_B = 2^{B-1}C$$

$$C_{TOTAL} = 2^B C$$

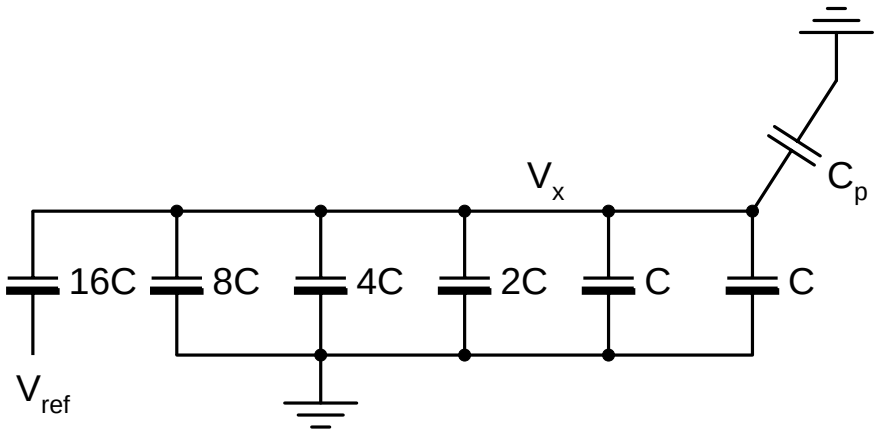
Sampling Phase (5-bit Example)



- Total charge at node V_x after opening S_x

$$Q = -V_{in} \cdot 32C = -V_{in} \cdot C_{total}$$

Bit5 Test (MSB)

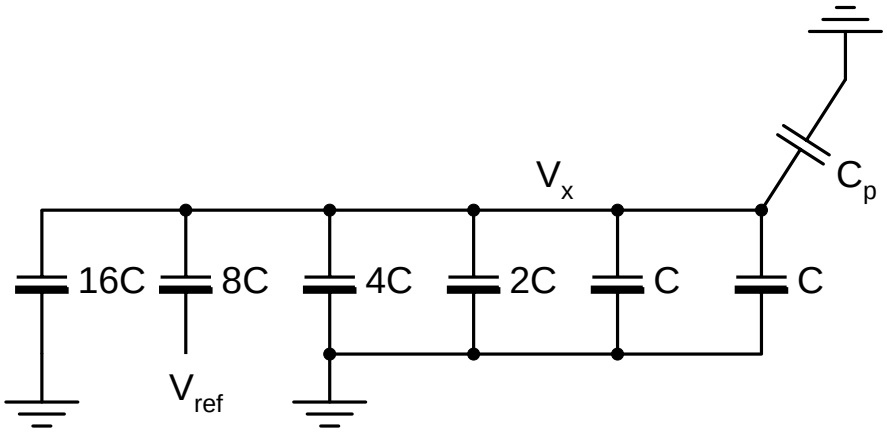


$$Q = -V_{in} \cdot C_{total} = (V_x - V_{ref}) \cdot 16C + V_x \cdot (16C + C_p)$$

$$\therefore V_x = \left(\frac{1}{2}V_{ref} - V_{in}\right) \cdot \frac{C_{total}}{C_{total} + C_p}$$

- $V_x<0 \Rightarrow V_{in}>0.5V_{ref} \Rightarrow$ Bit5=1
- $V_x>0 \Rightarrow V_{in}<0.5V_{ref} \Rightarrow$ Bit5=0

Bit4 Test (Assuming bit5=0)

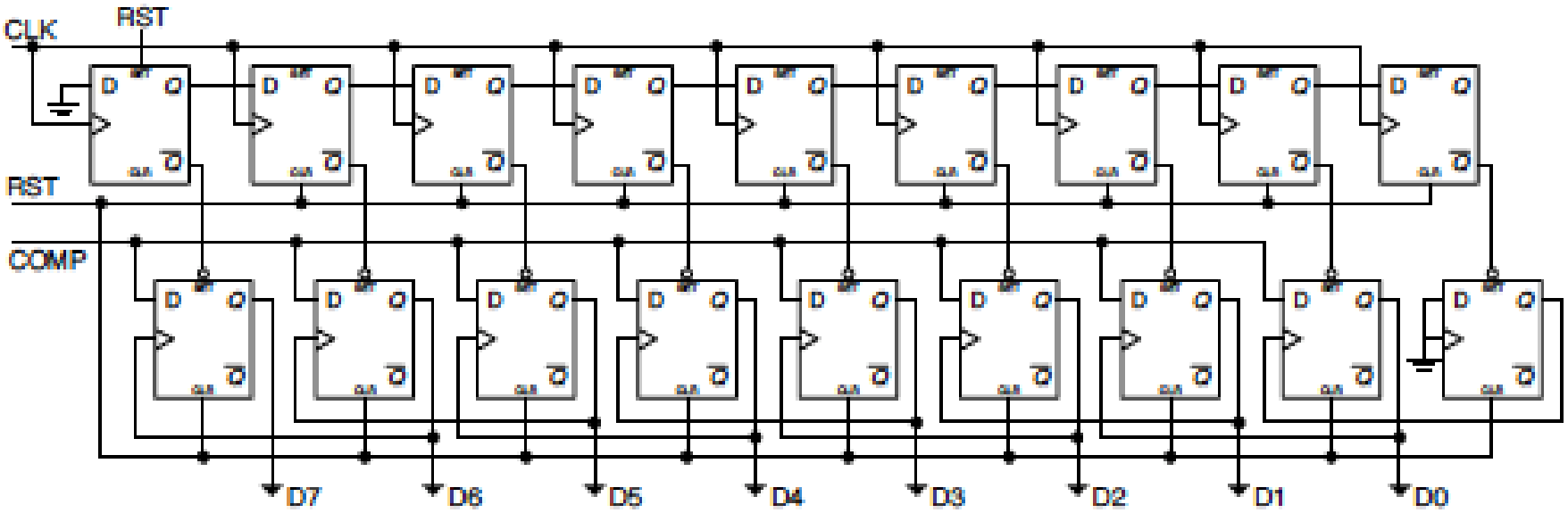


$$Q = -V_{in} \cdot C_{total} = (V_x - V_{ref}) \cdot 8C + V_x \cdot (24C + C_p)$$

$$\therefore V_x = \left(\frac{1}{4}V_{ref} - V_{in}\right) \cdot \frac{C_{total}}{C_{total} + C_p}$$

- $V_x<0 \Rightarrow V_{in}>0.25V_{ref} \Rightarrow$ Bit4=1
- $V_x>0 \Rightarrow V_{in}<0.25V_{ref} \Rightarrow$ Bit4=0

Digital Control



[M.D. Scott, B.E. Boser, K.S.J. Pister, "An ultralow-energy ADC for Smart Dust," IEEE J. Solid-State Circuits, pp. 1123 -1129, July 2003.]

- One register to store “1” for bit tests
- One register to store comparator results

Limitations

- Conversion rate typically limited by finite bandwidth of RC network during sampling and bit-tests
- For high resolution, the binary weighted capacitor array can become quite large
  - E.g. 16-bit resolution, C_{total}~100pF for reasonable kT/C noise contribution
- If matching is an issue, an even larger value may be needed
  - E.g. if matching dictates C_{min}=10fF, then $2^{16}C_{min}$=655pF
- Commonly used techniques
  - Implement "two-stage" or "multi-stage" capacitor network to reduce array size [Yee, JSSC 8/79]
  - Calibrate capacitor array to obtain precision beyond raw technology matching [Lee, JSSC 12/84]

SAR Techniques

- Small custom unit capacitors for low- to mid-resolution SAR ADC
- DAC schemes and switching schemes for low power or lower area
- Self-timed comparator or asynchronous SAR
  - At most 2 critical comparator decisions
  - Optimize time needed for comparator
- Redundant SAR
  - Make SAR robust against DAC settling errors and comparator noise
- SAR DAC Calibration
  - DAC non-linearity
  - Digital overhead

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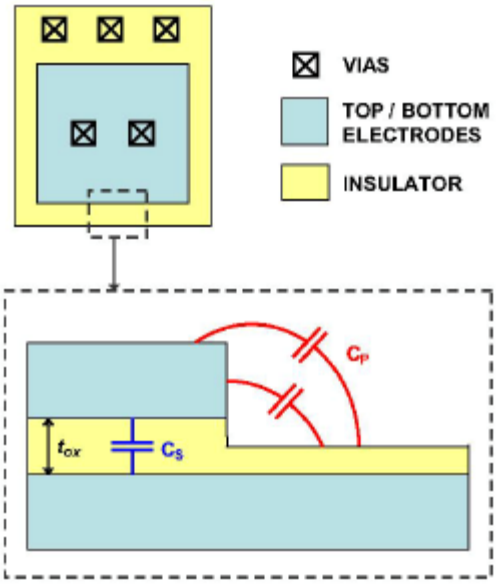
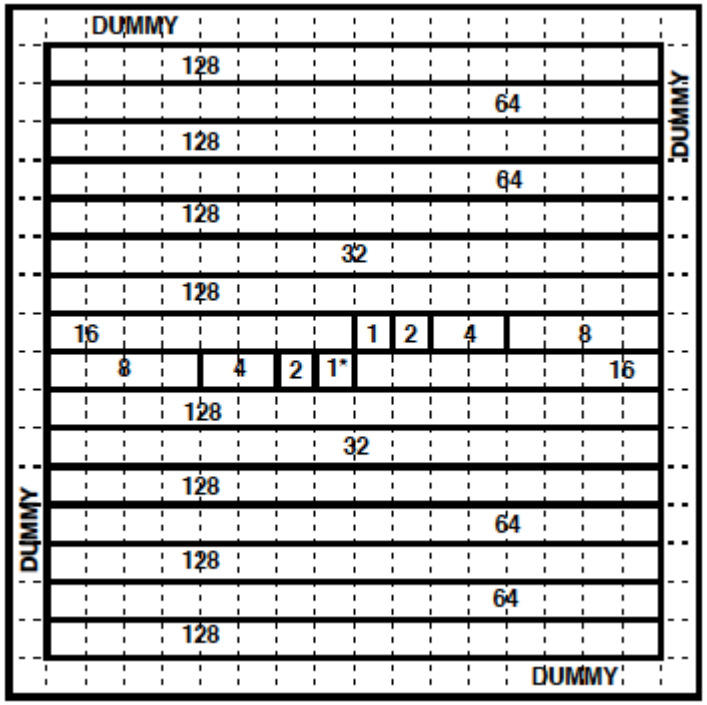
Capacitors

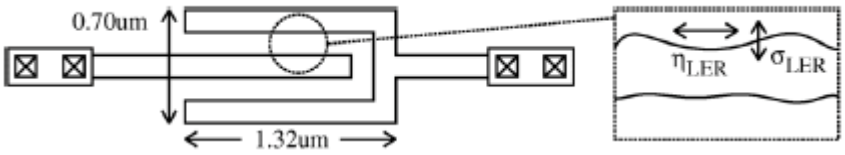
DAC Capacitors: MIMCap

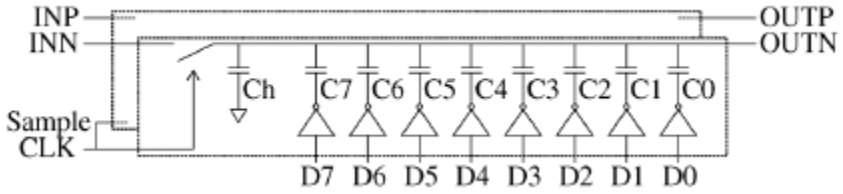


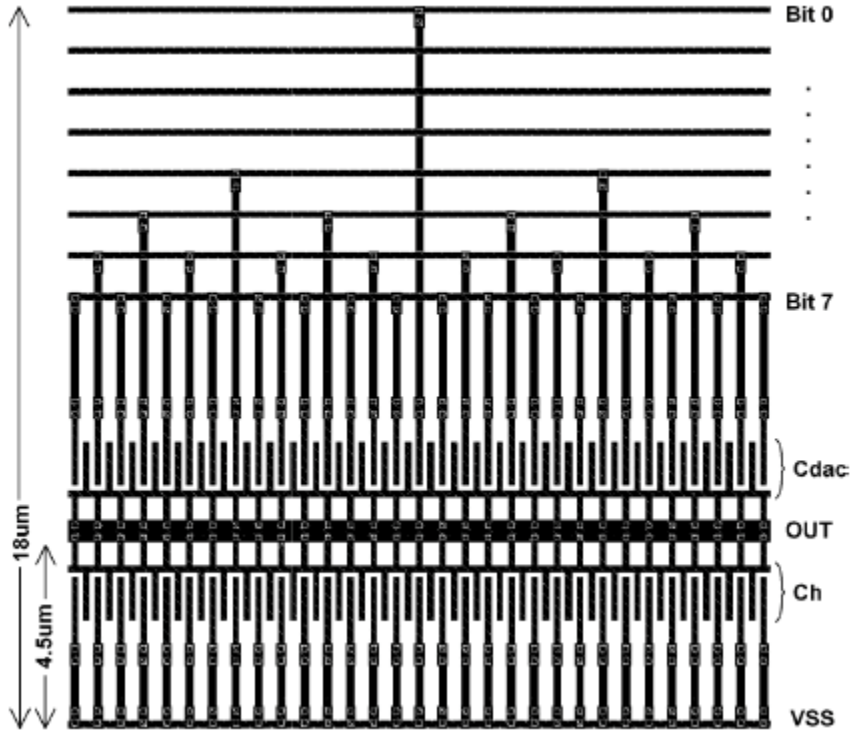


- Minimum capacitor value (10s of fF)
- Area overhead
- Routing parasitics (difficult to separate top and bottom plate) → grounded shield with one hole per unit capacitor for bottom-plate

DAC Capacitors: MOMCap







[P. J. A. Harpe et al., "A 26 w 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," IEEE J. Solid-State Circuits, vol. 46, no. 7, pp. 1585–1595, Jul. 2011]

- Custom structure with low minimum capacitor size (< 1fF)
- Custom mismatch model (typ. 0.2 % for 0.25fF unit cap in 90nm)

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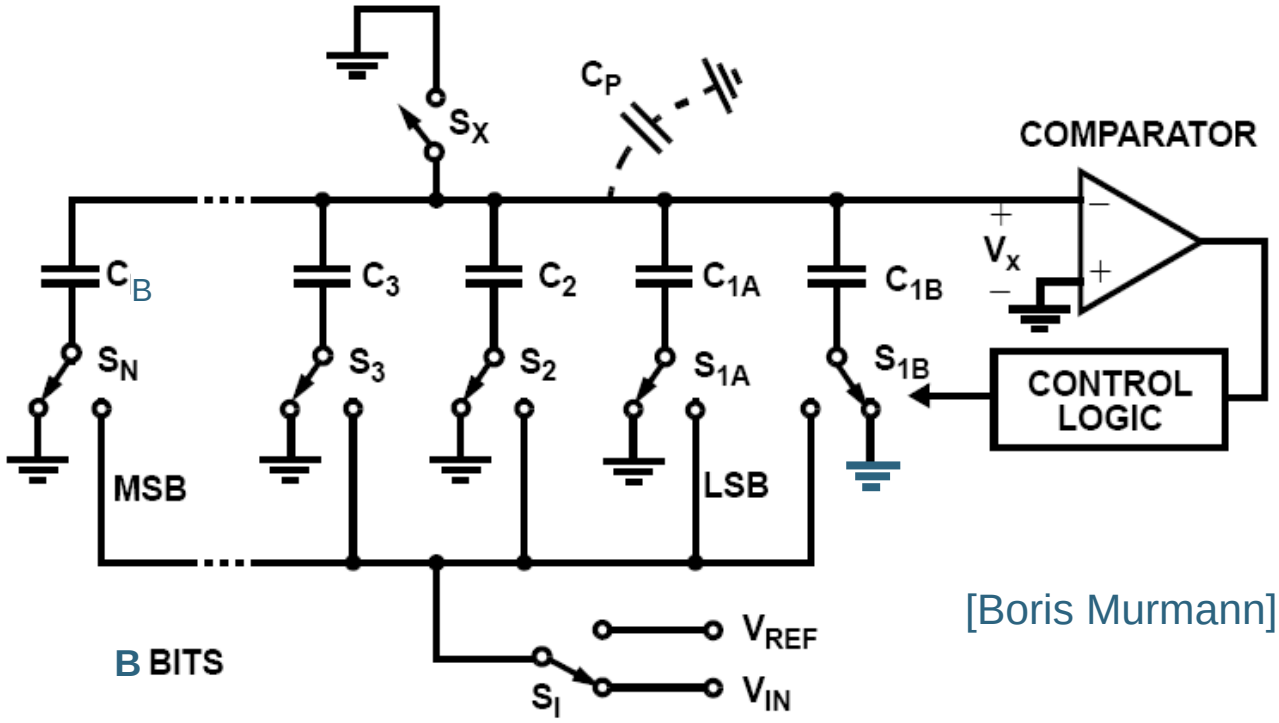
SAR ADC Capacitor and Switching Schemes

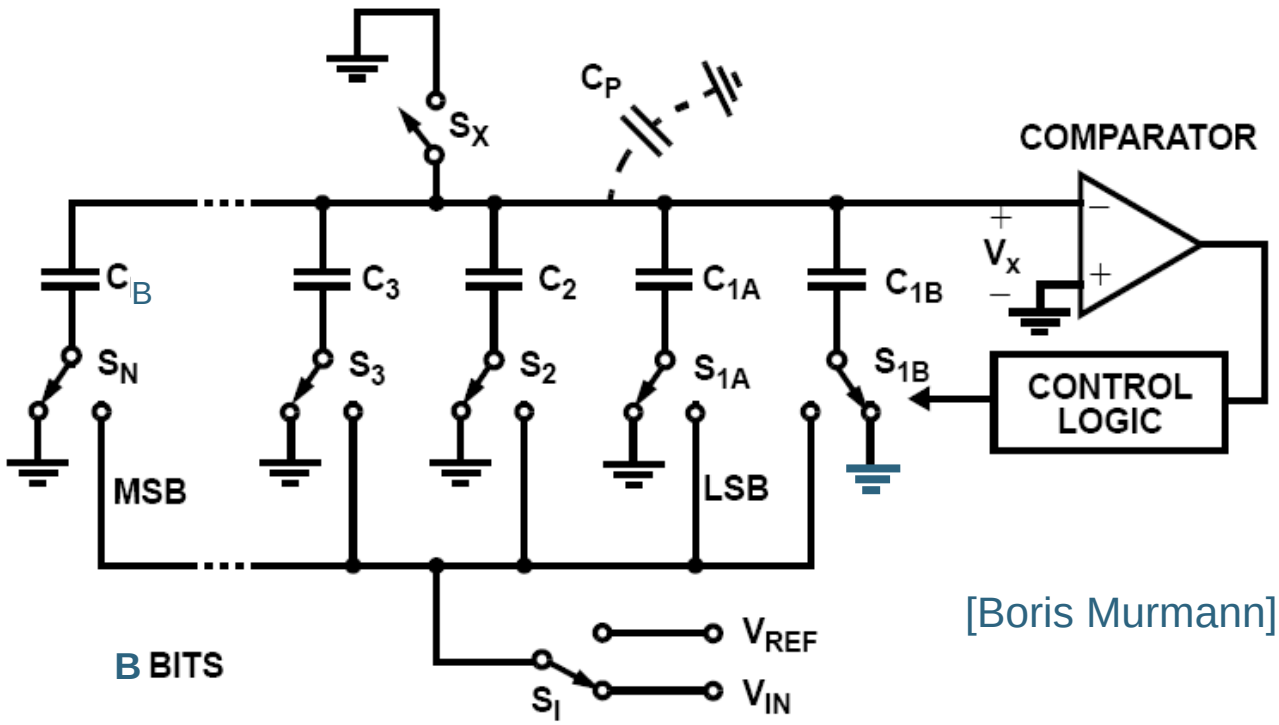
Conventional Switching Scheme



[Boris Murmann]

- Fully differential variants
- Unsuccessful bit trials lead to reference power loss
- Comparator input node swing

Conventional Switching Scheme

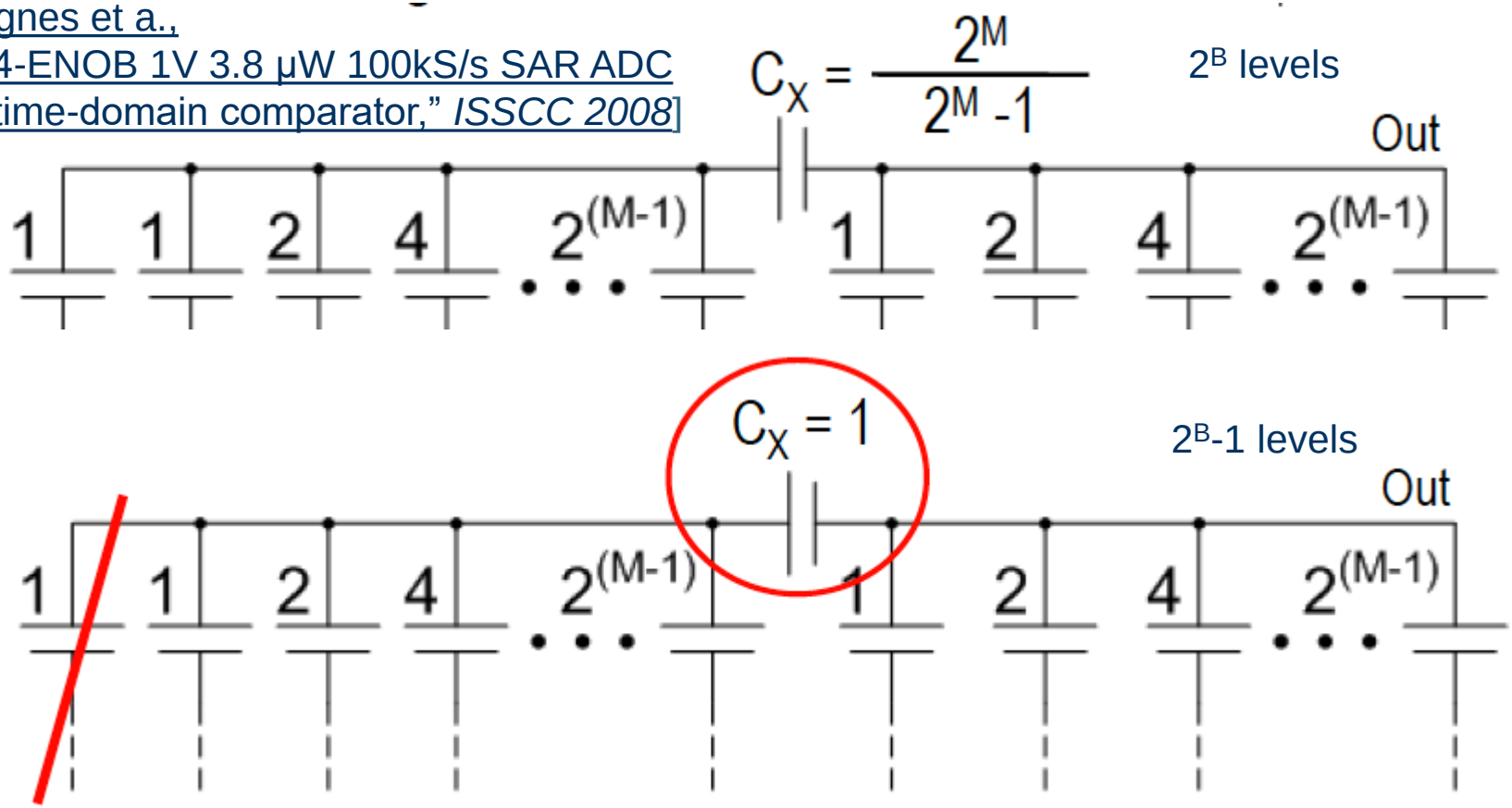


[Boris Murmann]

- Parasitic capacitor C_p only causes smaller comparator signal
  - Capacitive divider between switched capacitor and parasitic capacitor

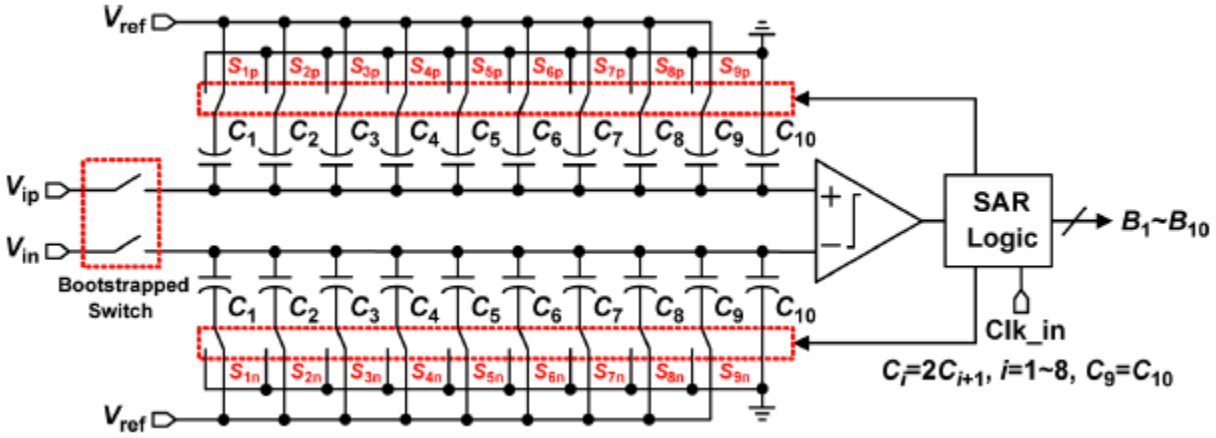
Split Capacitor Array

[A. Agnes et a., "A 9.4-ENOB 1V 3.8 µW 100kS/s SAR ADC with time-domain comparator," *ISSCC 2008*]



- Smaller number of unit elements, but needs calibration
  - Sensitive to parasitic capacitor on secondary summing node

Monotonic Switching Scheme

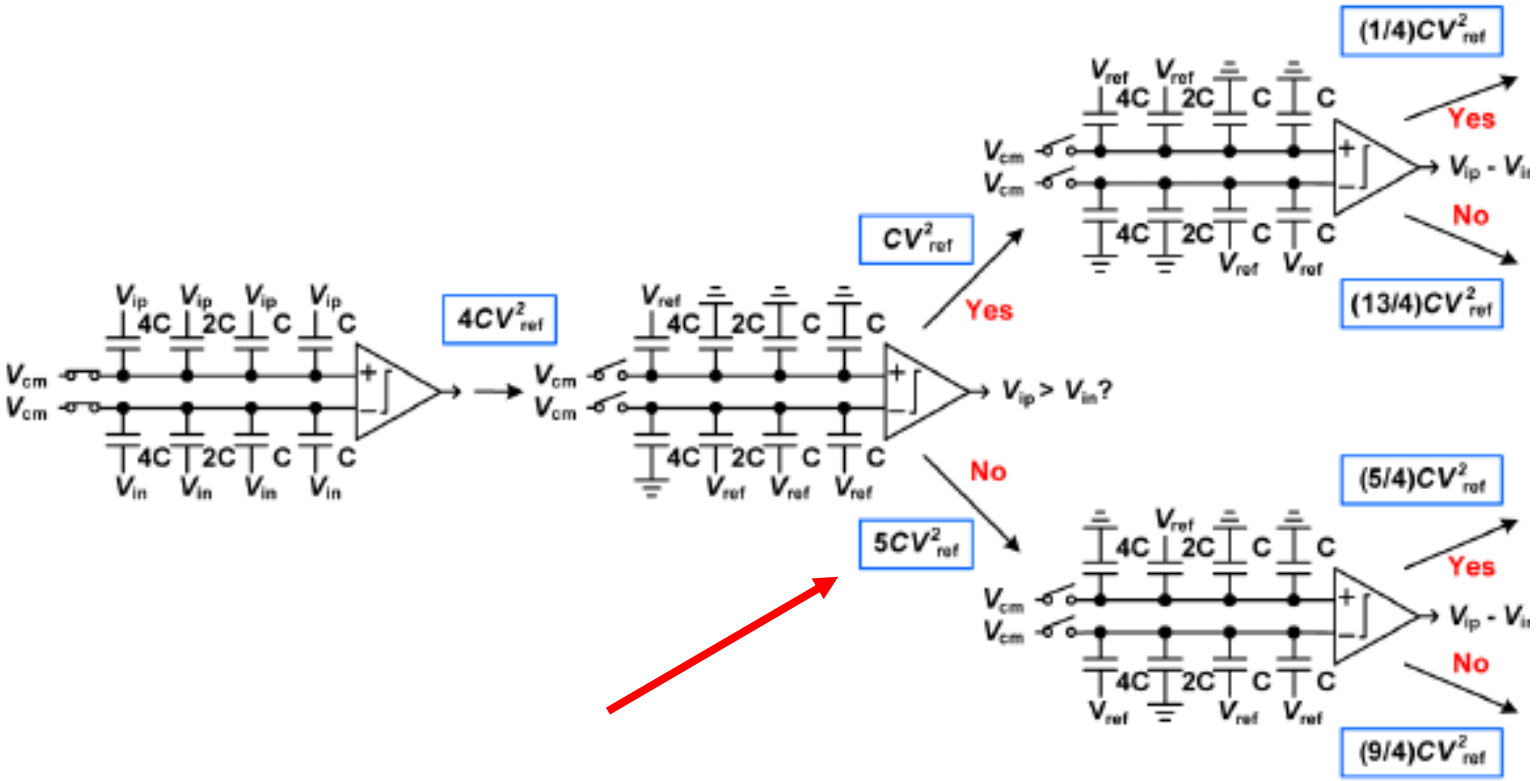


[C.-C. Liu et al., "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010]

- Top-plate sampling
- Compare before switching (B-1 single-ended switches for B bits)
- Parasitic capacitor C_p (not shown) leads to gain error
- Comparator common-mode

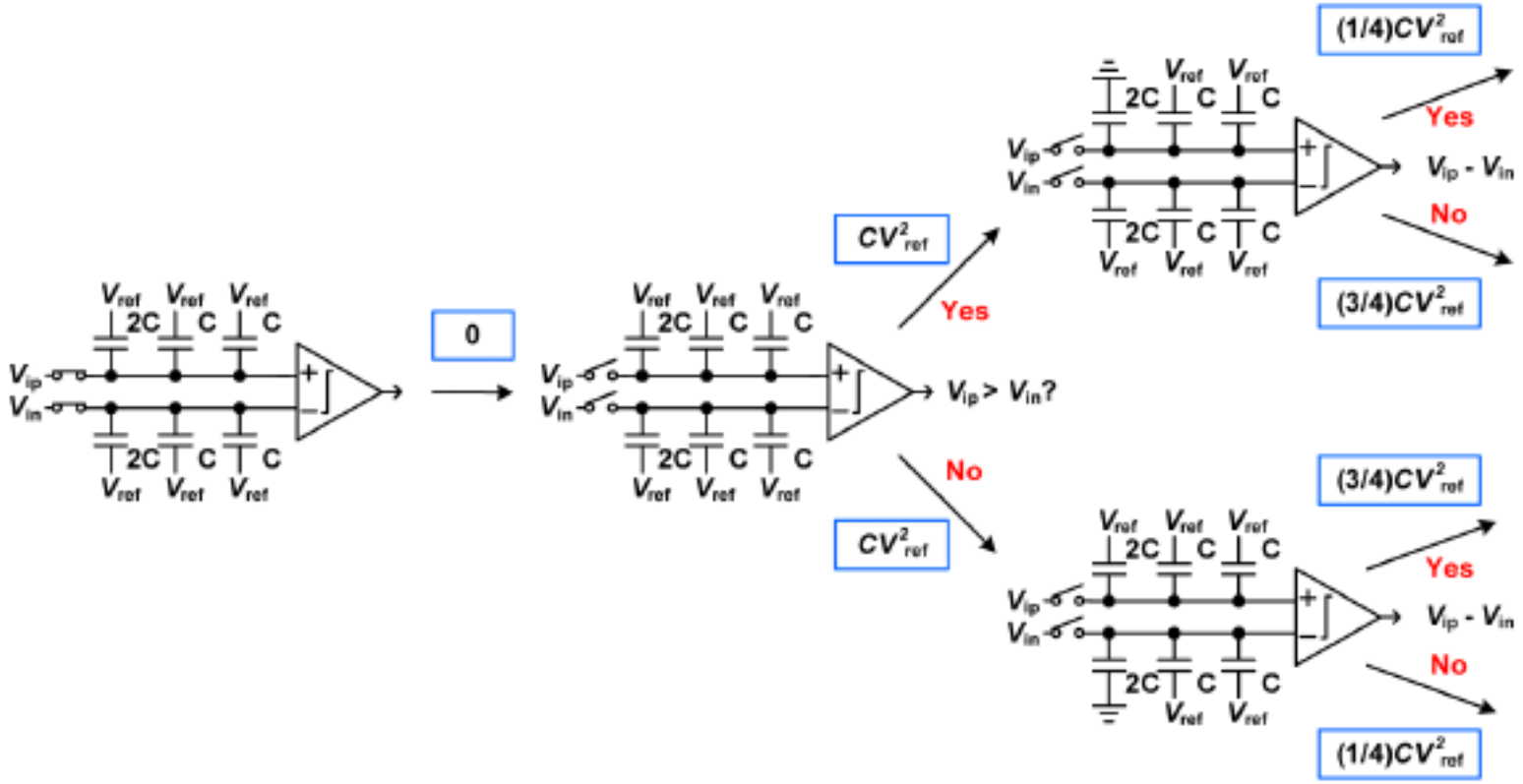
Monotonic Switching Scheme

- Conventional Switching Scheme



Monotonic Switching Scheme

- Monotonic Switching Scheme



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Successive Approximation ADC

SAR Techniques

- Small custom unit capacitors for low- to mid-resolution SAR ADC
- DAC schemes and switching schemes for low power or lower area
- Self-timed comparator or asynchronous SAR
  - At most 2 critical comparator decisions
  - Optimize time needed for comparator
- Redundant SAR
  - Make SAR robust against DAC settling errors and comparator noise
- SAR DAC Calibration
  - DAC non-linearity
  - Digital overhead

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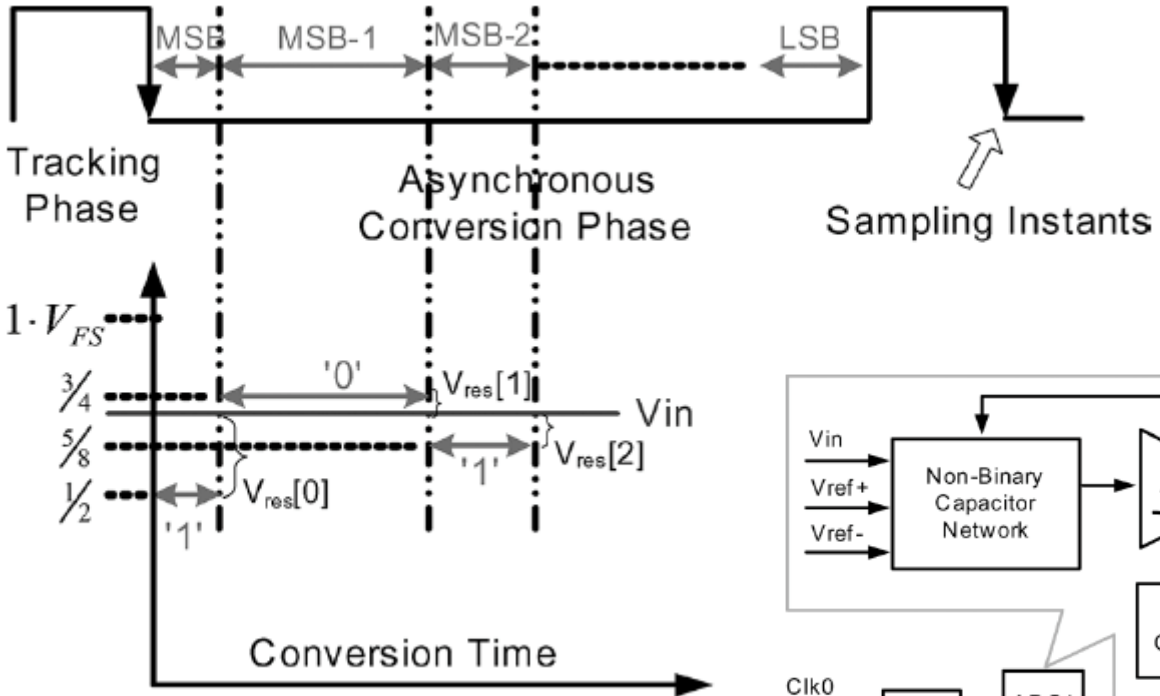
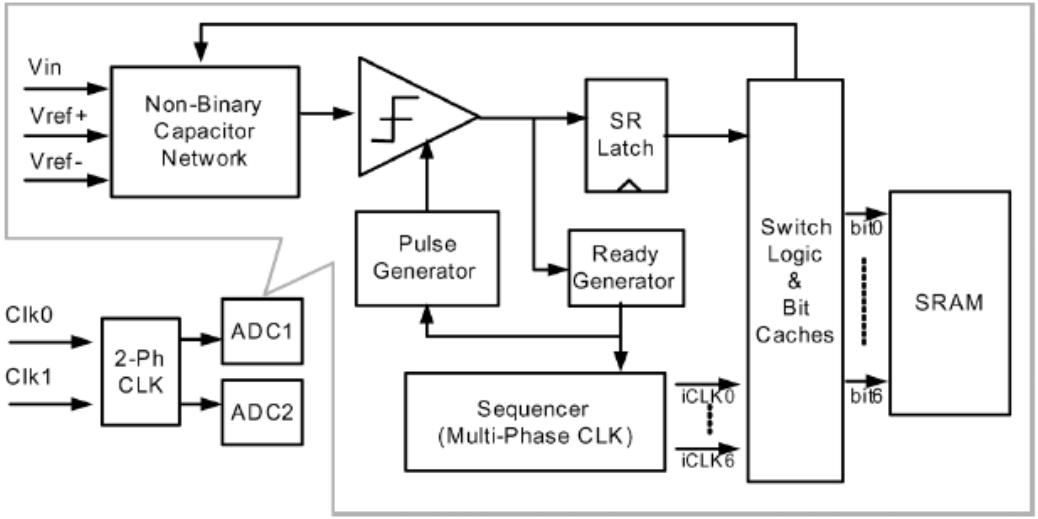
Asynchronous SAR ADC

Asynchrous SAR ADC

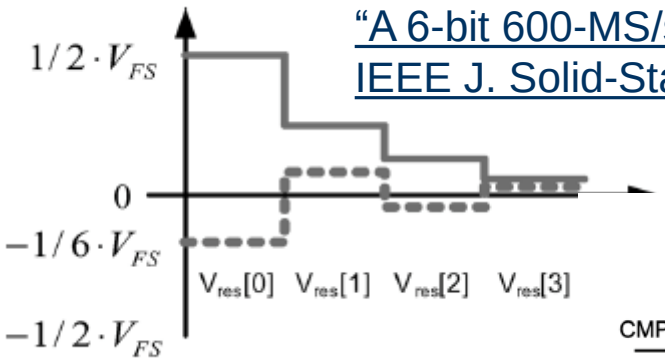


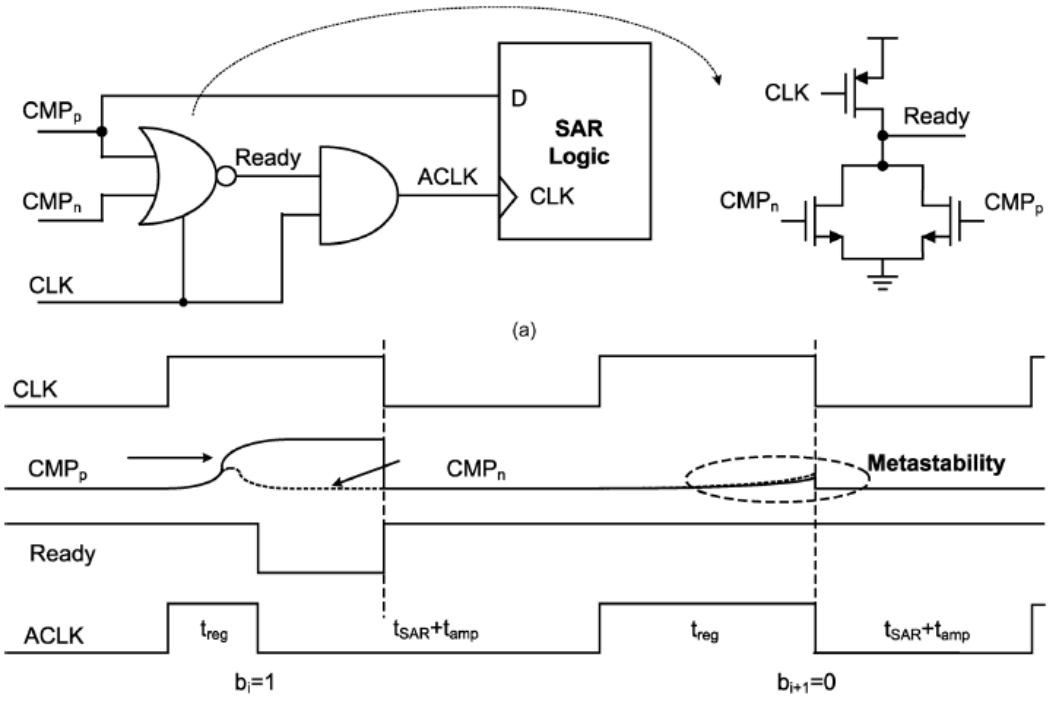


[S. W. M. Chen and R. W. Brodersen,
"A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13- m CMOS,"
IEEE J. Solid-State Circuits, vol. 41, no. 12, pp. 2669–2680, Dec. 2006]

Asynchronous SAR ADC: Metastability

[S. W. M. Chen and R. W. Brodersen,
"A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13- m CMOS,"
IEEE J. Solid-State Circuits, vol. 41, no. 12, pp. 2669–2680, Dec. 2006]





[W. Liu, P. Huang, and Y. Chiu,
"A 12-bit, 45-MS/s, 3-mW redundant Successive-Approximation-Register Analog-to-Digital converter with digital calibration," IEEE J. Solid-State Circuits, vol. 46, no. 11, pp. 2661– 2672, Nov. 2011]

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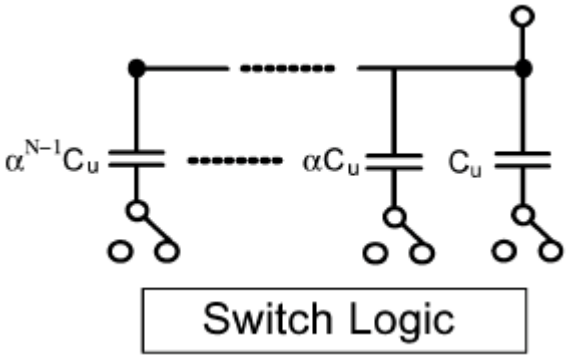
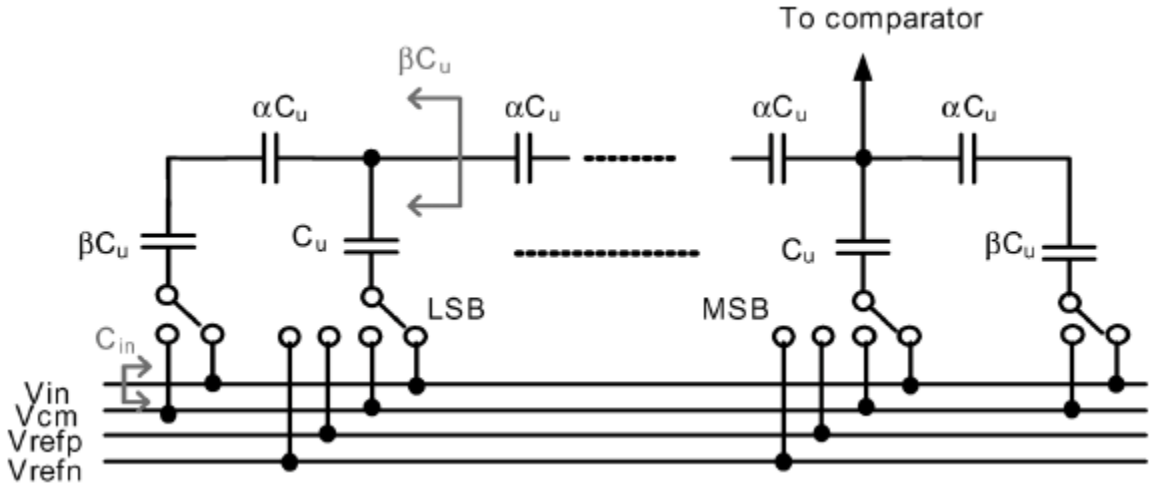
SAR ADC Redundancy

Redundant Non-Binary DAC



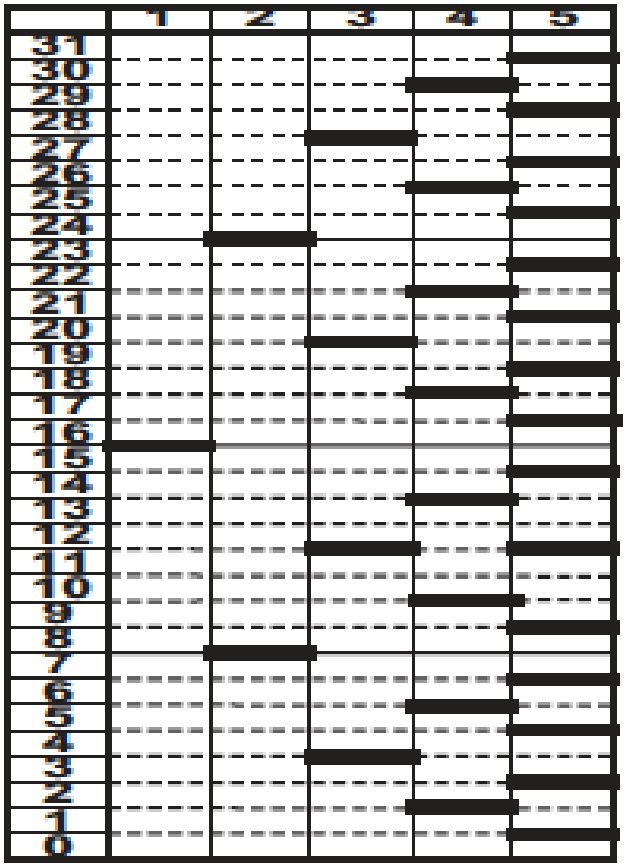


$$\begin{cases} \beta = 1 + \alpha \| \beta \\ \text{Radix} = 1 + (\beta/\alpha) \end{cases}$$

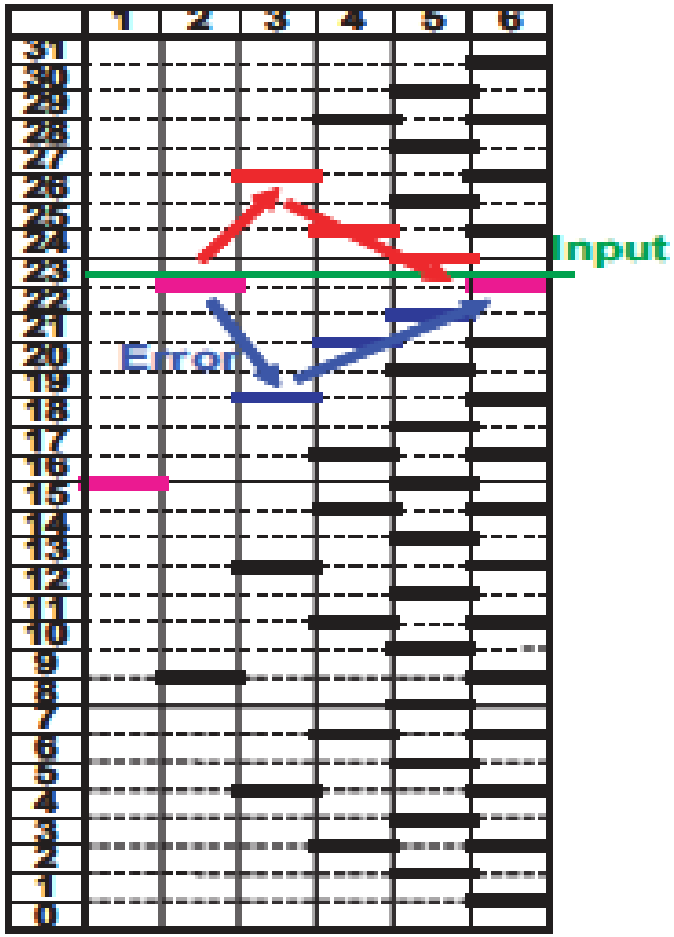
- Non-binary DAC (with 1 < Radix < 2) allows for recovery of erroneous comparator decisions, due to:
  - Incomplete DAC settling
  - Comparator noise

Non-binary Search

[Ogowa, “SAR ADC Algorithm with Redundancy”, 2008]

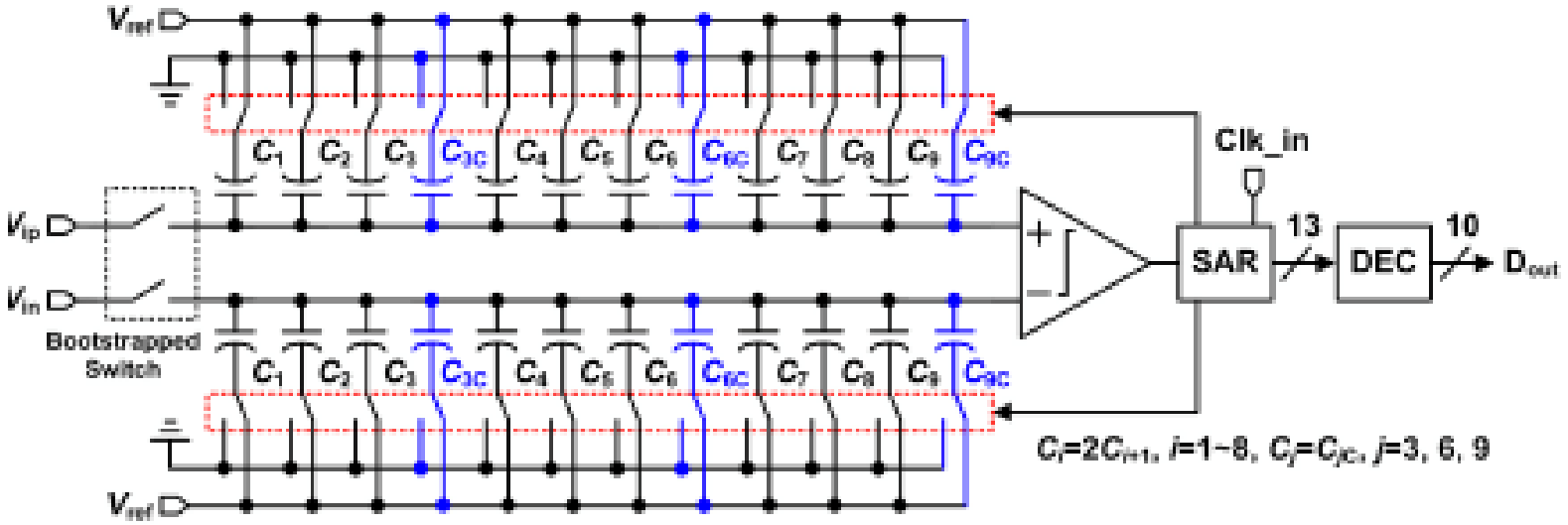


Binary Search (5b / 5 steps)

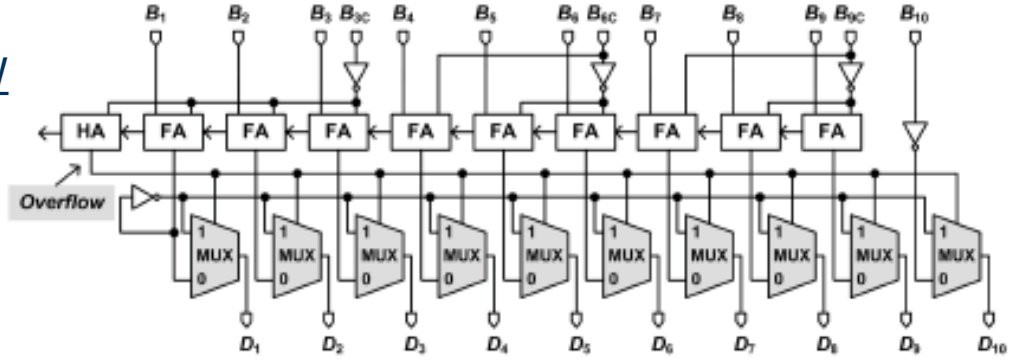


Non-Binary Search (5b / 6 steps)

Redundant Binary DAC



[C.-C. Liu et al., "A 10b 100ms/s 1.13mW SAR ADC with binary-scaled error compensation," in 2010 IEEE ISSCC, pp. 386–387]



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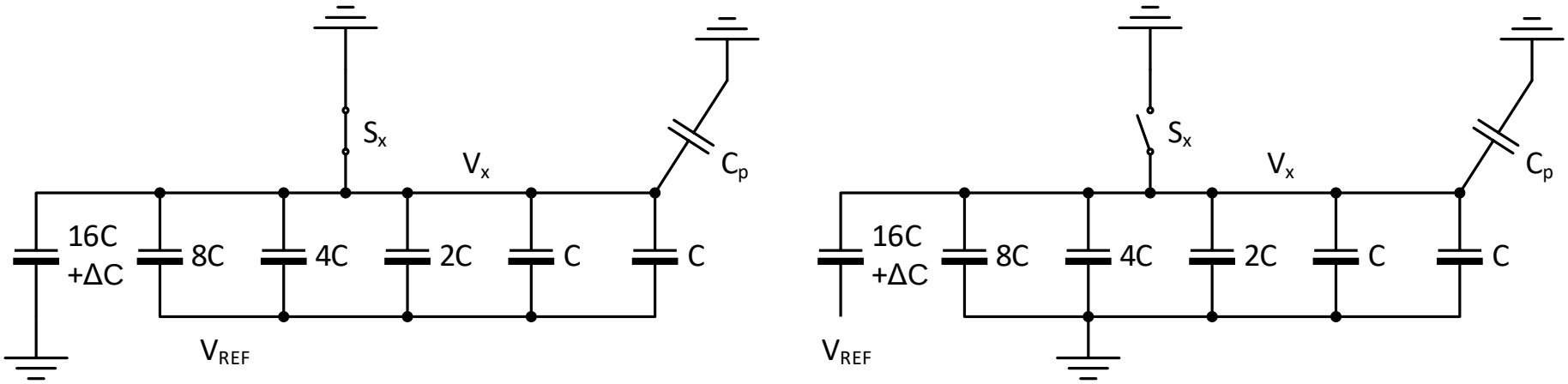
SAR ADC DAC Calibration

Johan Vanderhaegen
University of California, Berkeley
jpv@eecs.berkeley.edu

DAC Calibration Scheme (5-bit Example)



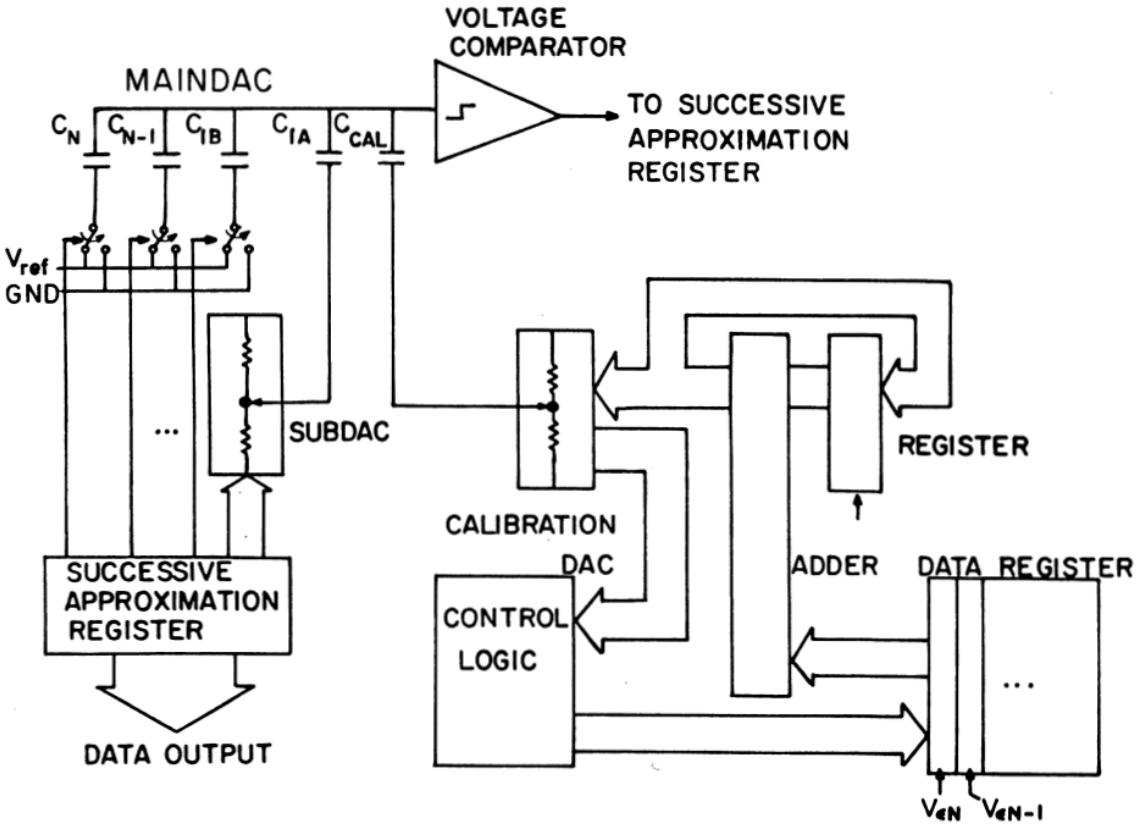
- Voltage V_x after opening S_x and switching cap voltages for MSB:

$$V_{x_1} = \frac{\Delta C}{C_{TOTAL}} V_{REF}$$

- Use calibration DAC to digitize residual and to correct conversion

[H.-S. Lee, "Self-calibration techniques for successive approximation analog- to-Digital converters," PhD thesis, University of California at Berkeley, 1984]

DAC Calibration Scheme



[H.-S. Lee, "Self-calibration techniques for successive approximation analog- to-Digital converters, " PhD thesis, University of California at Berkeley, 1984]

- Digital overhead