EE240C: Analog-Digital Interface Integrated Circuits **2019**

Homework #2

(due Wed 10/2/2019; submit through bCourses)

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Problem 1. Spectral Analysis

Download the file `hw2_p1_data.mat` from the course website assignments folder. It contains the output of a 12-bit ADC with a sampling frequency of 25 MHz and a full-scale range of $[-1, +1]$. The input was a full-scale sinusoidal signal.

a) Plot the spectrum from 0 to $f_s/2$ using FFT without averaging. The y axis should be in dBFS while the x axis should be in MHz.

b) What is the frequency f_{in} of the sinusoidal signal at the input of the ADC?

c) Compute the following metrics: SNR, SNDR, ENOB, THD, SFDR.

d) Which non-ideality is limiting the SFDR in this case?

Problem 2. Current Steering DACs

a) Read the following paper: C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2," IEEE J. Solid-State Circuits, Vol.33, pp. 1948–1958, Dec. 1998.

b) In the above reference, it was found that for the given objectives, a thermometer/ binary partition of 8/2 is most suitable. Your task in this problem is to re-optimize this DAC for 65nm technology with a different set of process parameters, without altering its basic structure. The design variables to be optimized are:

Parameter	Description
B_t	Number of bits in thermometer section
A_{unit}	Area of unit current source

Your target specs and process parameters are:

Parameter	Description	Value
B	Resolution	12 bits
INLspec	Worst case integral nonlinearity	< 2 LSB
DNLspec	Worst case differential nonlinearity	< 0.5 LSB
Y	Target yield	99%
A_{decode}	Approximate decoder and routing area	$2^{B_t}\ 200\,\text{um}^2$
A_{total}	Total DAC area (to be minimized)	$2^B\ A_{\text{u}nit} + A_{\text{decode}}$
k_{u}	Unit element matching parameter	3 %um
σ_{u}	Standard deviation of unit element mismatch	$k_{\text{u}}/\sqrt{A_{\text{unit}}}$

(a) Following the procedure outlined in the reference, answer the following **using only hand calculations** (After the equations are written by hand, it is ok to use Matlab to perform a sweep across **integer** values of B_{t}):

- What values of A_{unit} and B_{t} actually minimize the total area?
- What is the minimum total area (in mm^2)?

(b) Create a plot similar to Fig. 9 of the reference paper to illustrate the "minimum area" design. In this diagram, plot the total DAC area in mm^2 (log scale) versus the design parameter B_{t} (linear scale in bits).

Problem 3. Flash ADC

Consider a 6-bit flash ADC with an ideal reference resistor string and $V_{\text{REF}} = 1.8\,\text{V}$. Assume that the pre-amps have an offset voltage with standard deviation $\sigma_{\text{offset}} = 3\,\text{mV}$ and the comparators are ideal. For simplicity, assume that the first and last preamp have zero offset.

a) What are the standard deviations of the converter's DNL and INL? (Note that DNL and INL are always stated in terms of LSB).

b) How will the σ_{DNL} and σ_{INL} be affected by 4x interpolation (M=4)? (For a constant LSB)

Problem 4. kT/C Noise

Shown below in figure 1 is the schematic of an NMOS sampler used in the front-end of a B-bit ADC. The RC time constant of this circuit was chosen such that it settles to within 1 LSB in one half clock period.

Derive an expression for the total thermal noise of the sampler in terms of the switch resistance R, the number of bits B, the sampling rate f_s, the Boltzmann constant k, and the absolute temperature T.

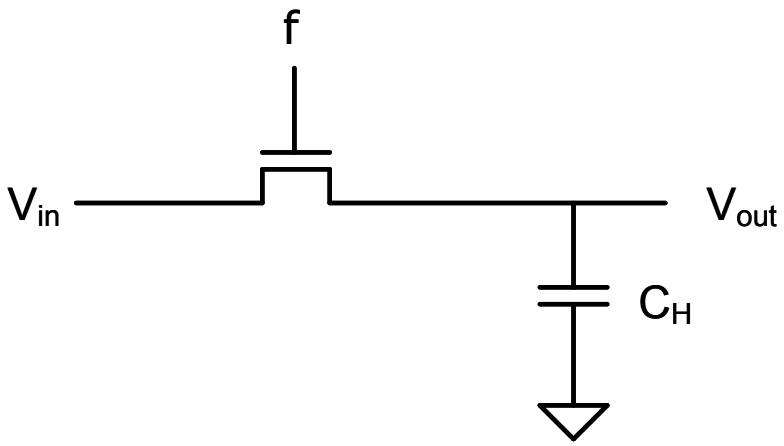

Figure 1: NMOS sampling switch