EE 240C
Analog-Digital Interface Integrated Circuits

Dynamic Errors

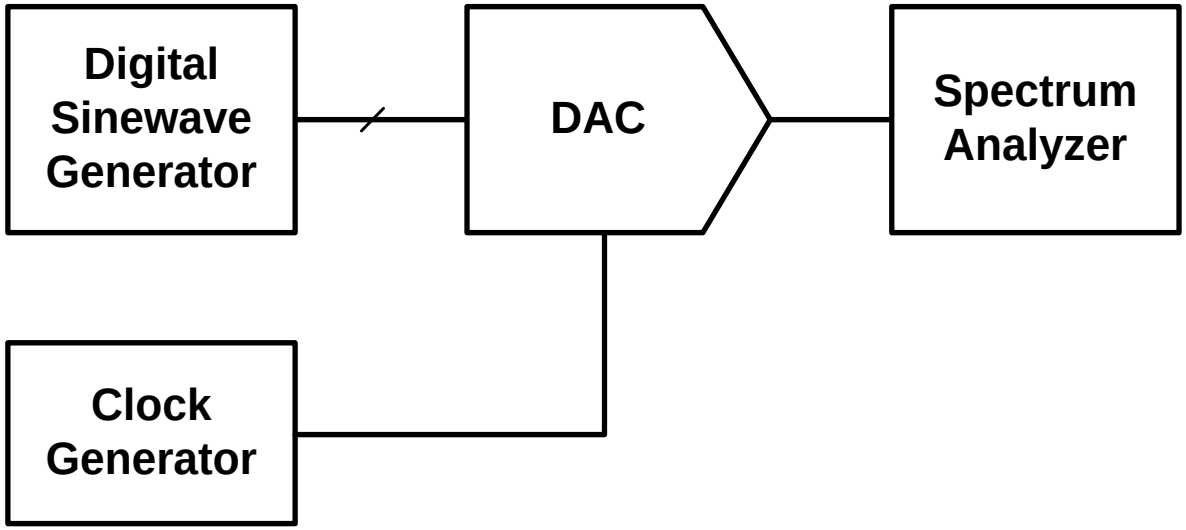
Dynamic Performance Metrics

- Time domain
  - Glitch impulse, aperture uncertainty, settling time, …
  - We'll look at these later, in the context of specific circuits
- Frequency domain
  - Performance metrics follow from looking at converter or building block output spectrum
    - "Spectral performance metrics"
  - Basic idea: Apply one or more tones at converter input
    - Expect same tone(s) at output, all other frequency components represent nonidealities
  - Important to realize that both static (DNL, INL) and dynamic errors contribute to frequency domain non-ideality

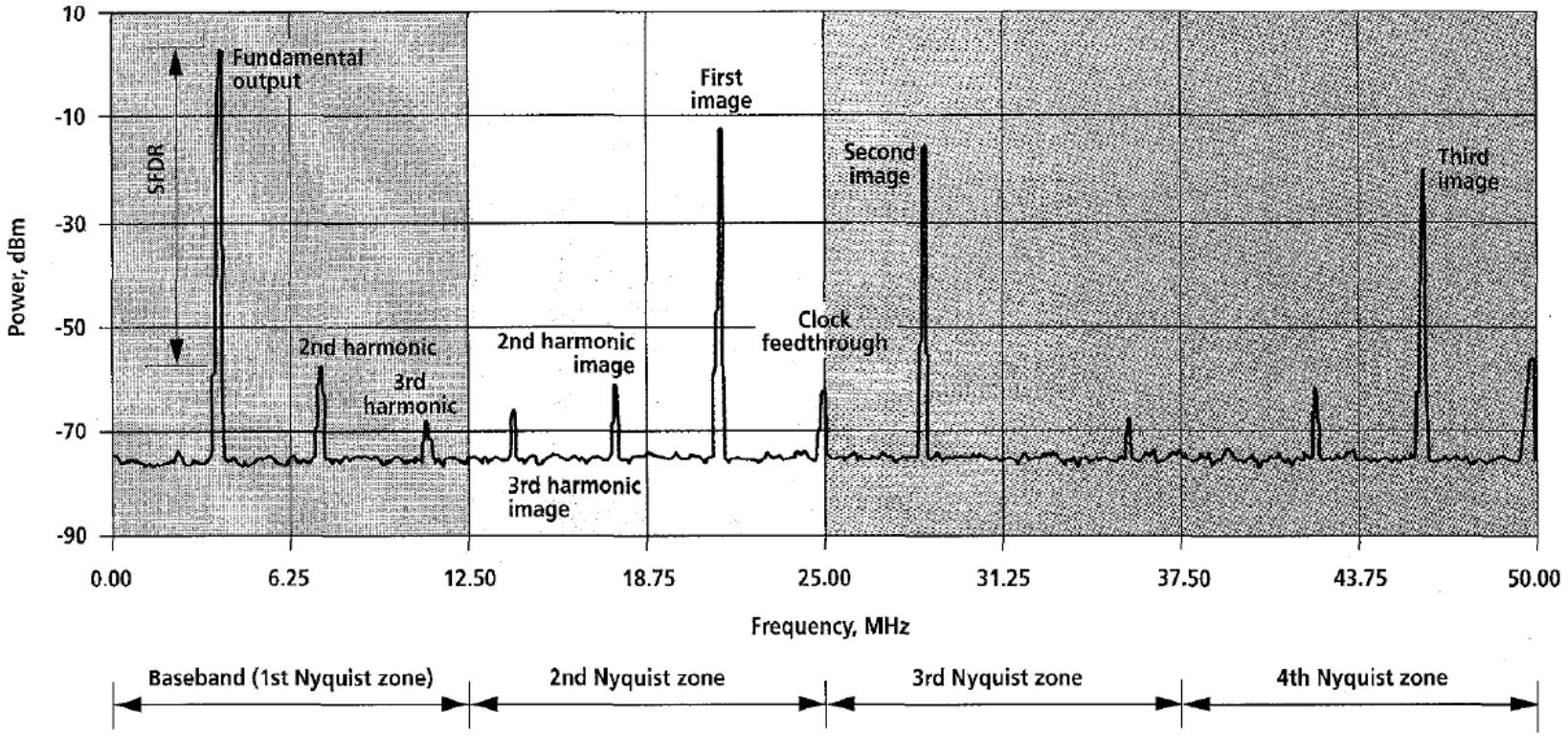
Alphabet Soup of Spectral Metrics

- SNR – Signal-to-noise ratio
- SNDR (SINAD) – Signal-to-(noise+distortion) ratio
- ENOB – Effective number of bits
- DR – Dynamic range
- SFDR – Spurious free dynamic range
- THD – Total harmonic distortion
- ERBW – Effective Resolution Bandwidth
- IMD – Intermodulation distortion
- MTPR – Multi-tone power ratio

DAC Tone Test/Simulation

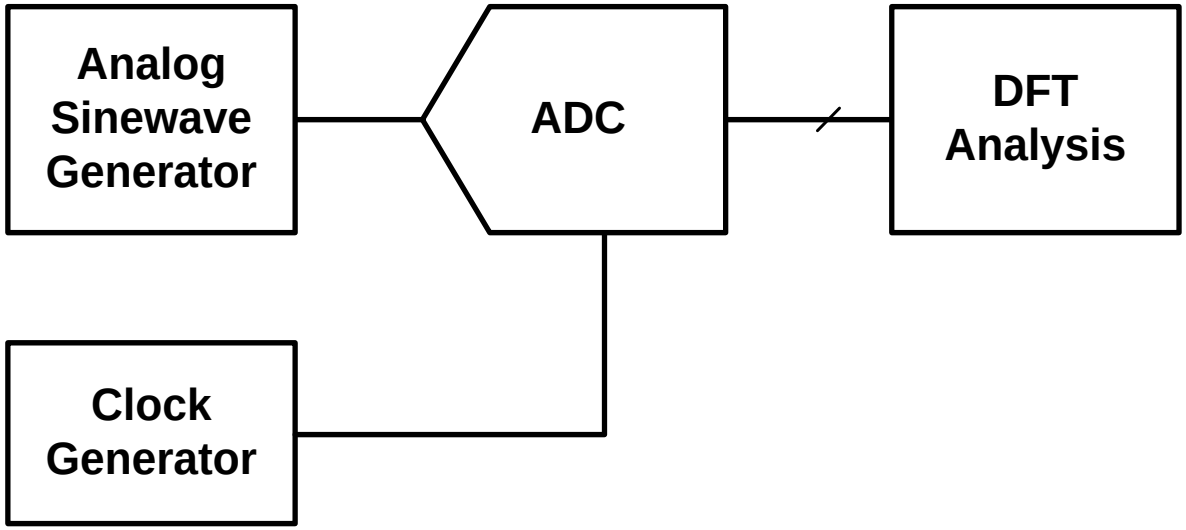


Typical DAC Output Spectrum



[Hendriks, "Specifying Communications DACs, IEEE Spectrum, July 1997]

ADC Tone Test/Simulation



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Spectral Analysis

Discrete Fourier Transform

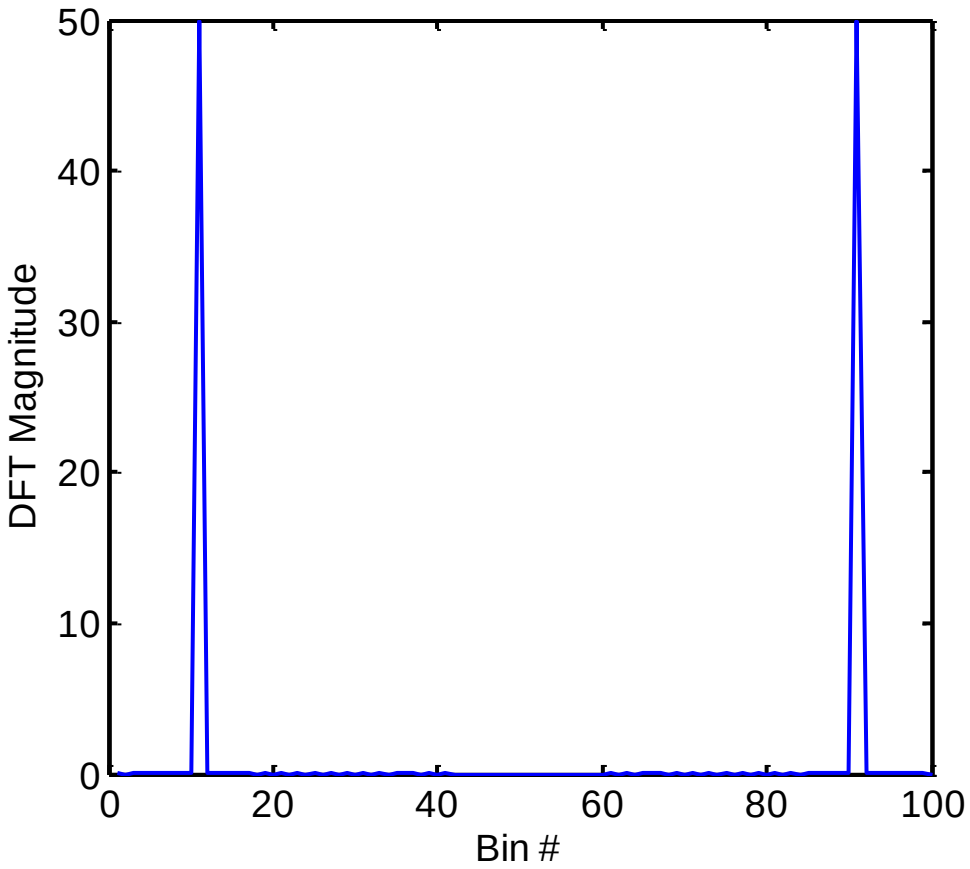
- DFT takes a block of N time domain samples (spaced $T_s=1/f_s$) and yields a set of N frequency bins

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi kn/N}$$

- Bin k represents frequency content at $k \cdot f_s/N$ [Hz]
- DFT frequency resolution
  - Proportional to $1/(N \cdot T_s)$ in [Hz/bin]
  - $N \cdot T_s$ is total time spent gathering samples
- A DFT with $N=2^{\text{integer}}$ can be found using a computationally efficient algorithm
  - FFT = Fast Fourier Transform

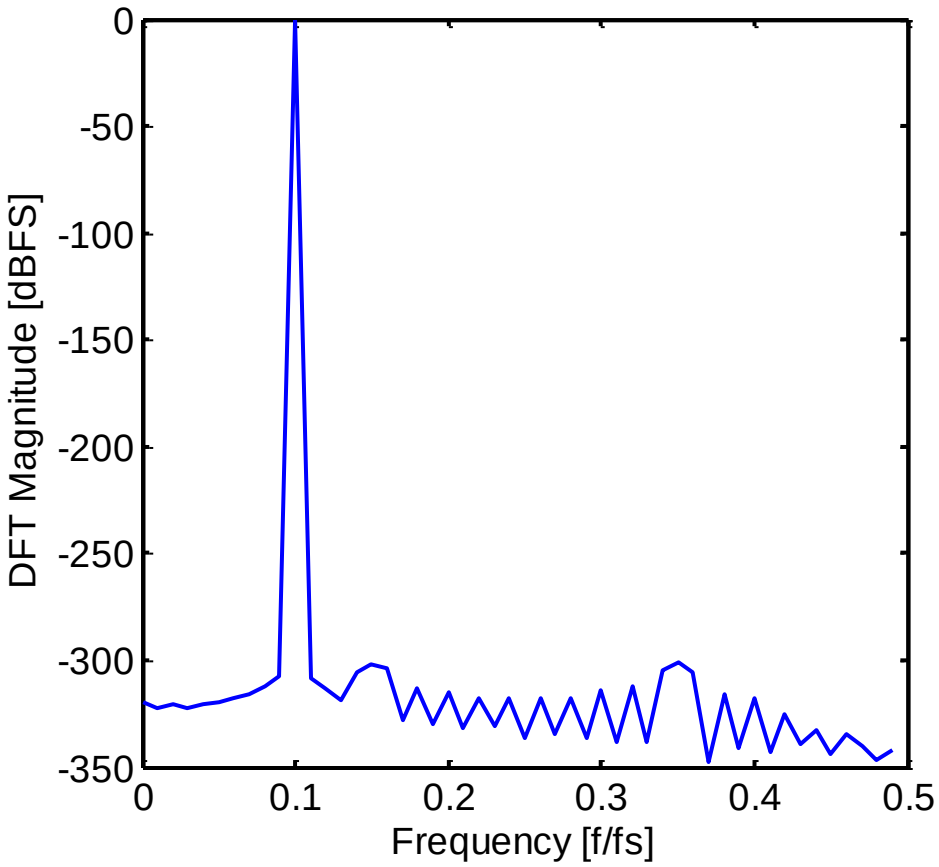
Matlab Example

```
N  = 100;
fs = 1000;
fx = 100;

x = cos(2*pi*fx/fs*[0:N-1]);
s = abs(fft(x));
plot(s, 'linewidth', 2);
```



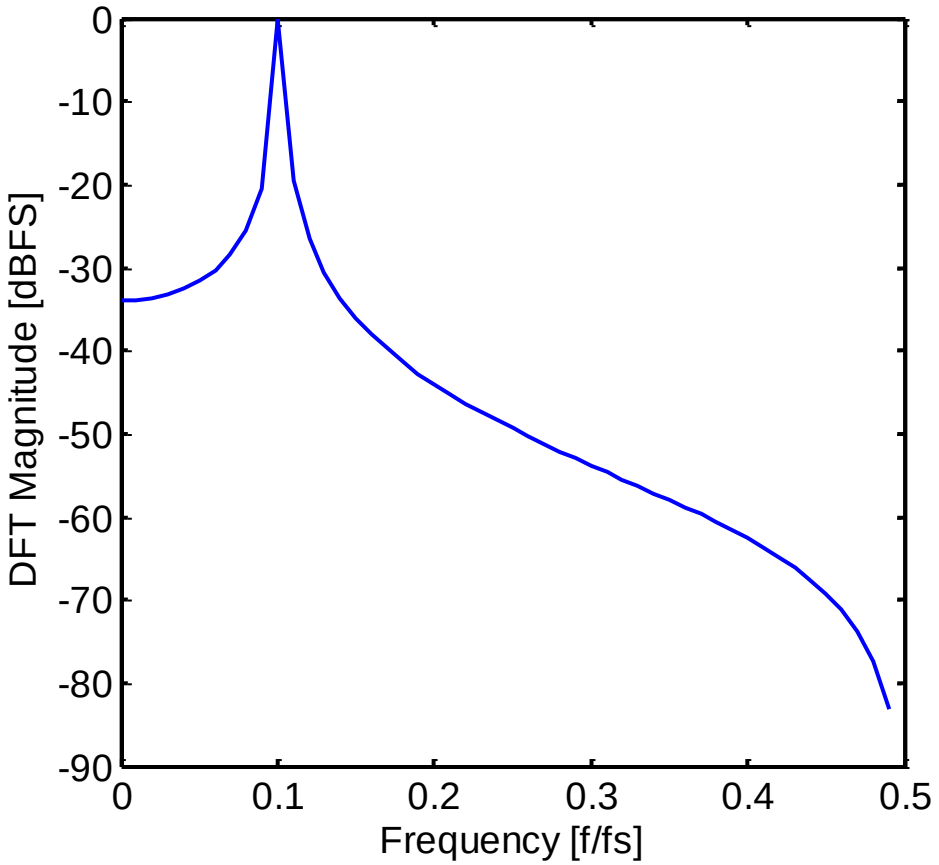
Normalized Plot with Frequency Axis

```
N  = 100;
fs = 1000;
fx = 100;
FS = 1; % full-scale amplitude

x = FS*cos(2*pi*fx/fs*[0:N-1]);
s = abs(fft(x));
% remove redundant half of spectrum
s = s(1:end/2);
% normalize magnitudes to dBFS
% dbFS = dB relative to full-scale
s = 20*log10(2*s/N/FS);
% frequency vector
f = [0:N/2-1]/N;

plot(f, s, 'linewidth', 2);
xlabel('Frequency [f/fs]')
ylabel('DFT Magnitude [dBFS]')
```



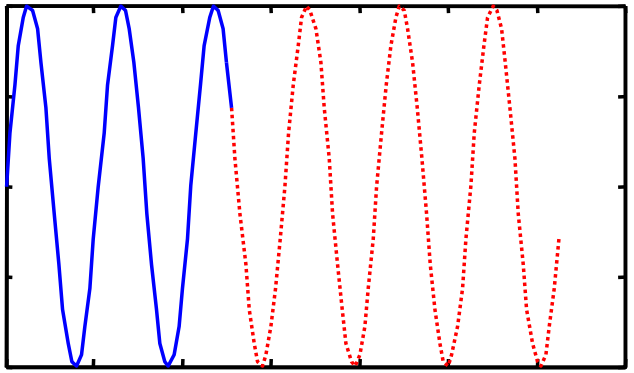
Another Example

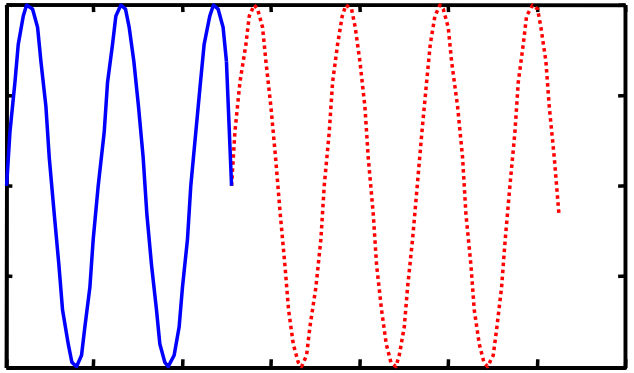
- Same as before, but now $f_x=101$
- This doesn't look the spectrum of a sinusoid…
- What's going on?



Spectral Leakage

- DFT implicitly assumes that data repeats every N samples
- A sequence that contains a non-integer number of sine wave cycles has discontinuities in its periodic repetition
  - Discontinuity looks like a high frequency signal component
  - Power spreads across spectrum
- Two ways to deal with this
  - Ensure integer number of periods
  - Windowing

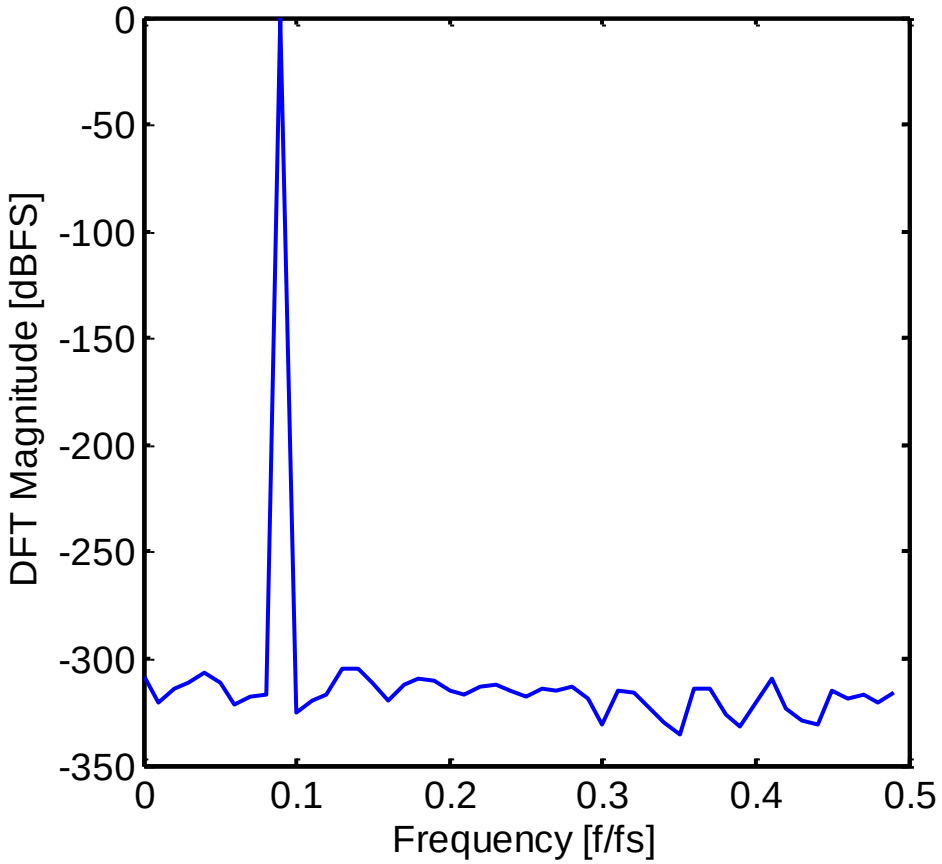




Integer Number of Cycles

```
N  = 100;
cycles = 9;
fs = 1000;
fx = fs*cycles/N;
```

- Usable test frequencies are limited to a multiple of f_s/N

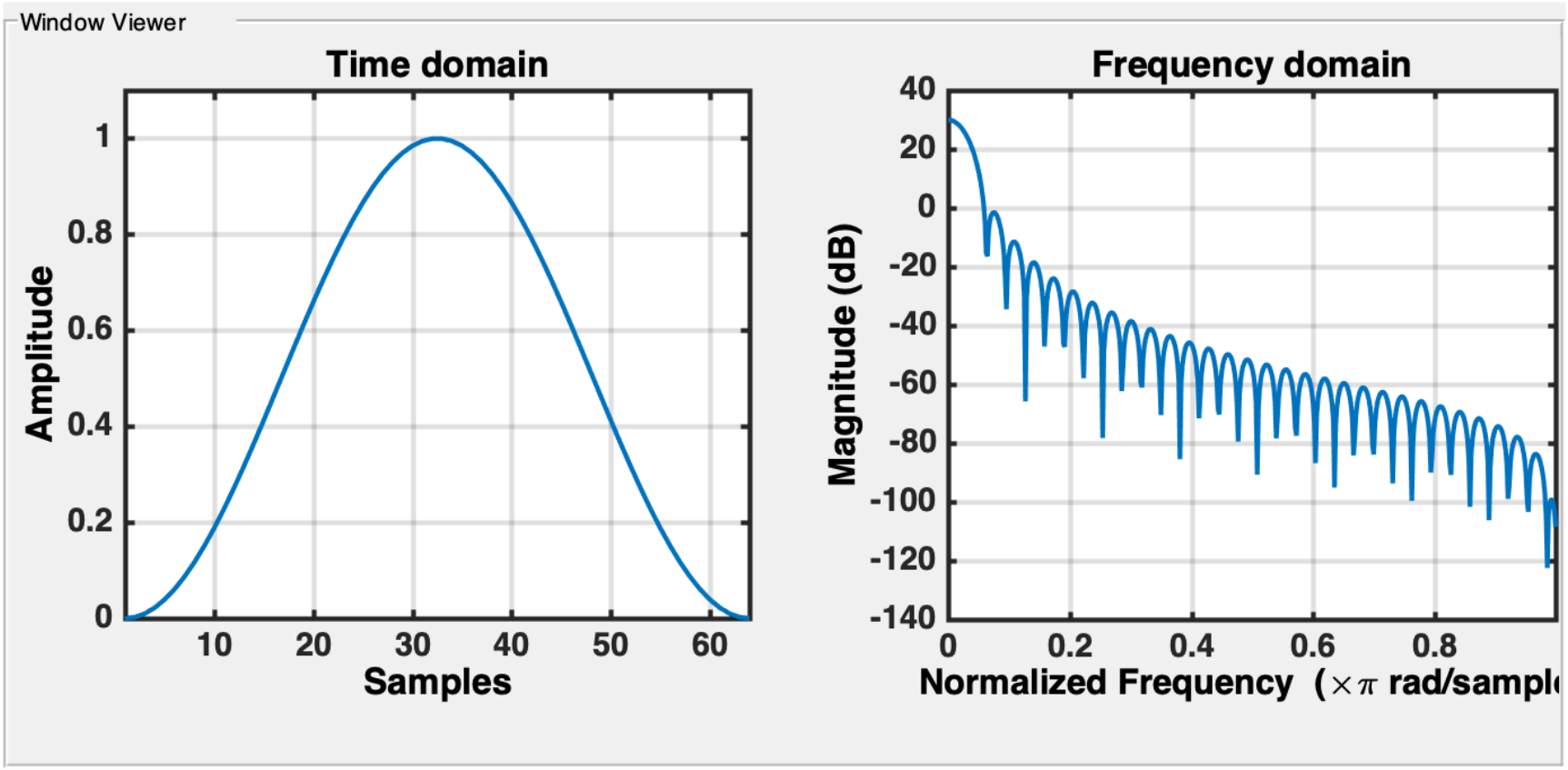


Windowing

- Spectral leakage can be attenuated by windowing the time samples prior to the DFT
- Windows taper smoothly down to zero at the beginning and the end of the observation window
- Time domain samples are multiplied by window coefficients on a sample-by-sample basis
  - Means convolution in frequency
  - Sine wave tone and other spectral components smear out over several bins
- Lots of window functions to chose from
  - Tradeoff: attenuation versus smearing
- Example: Hann Window

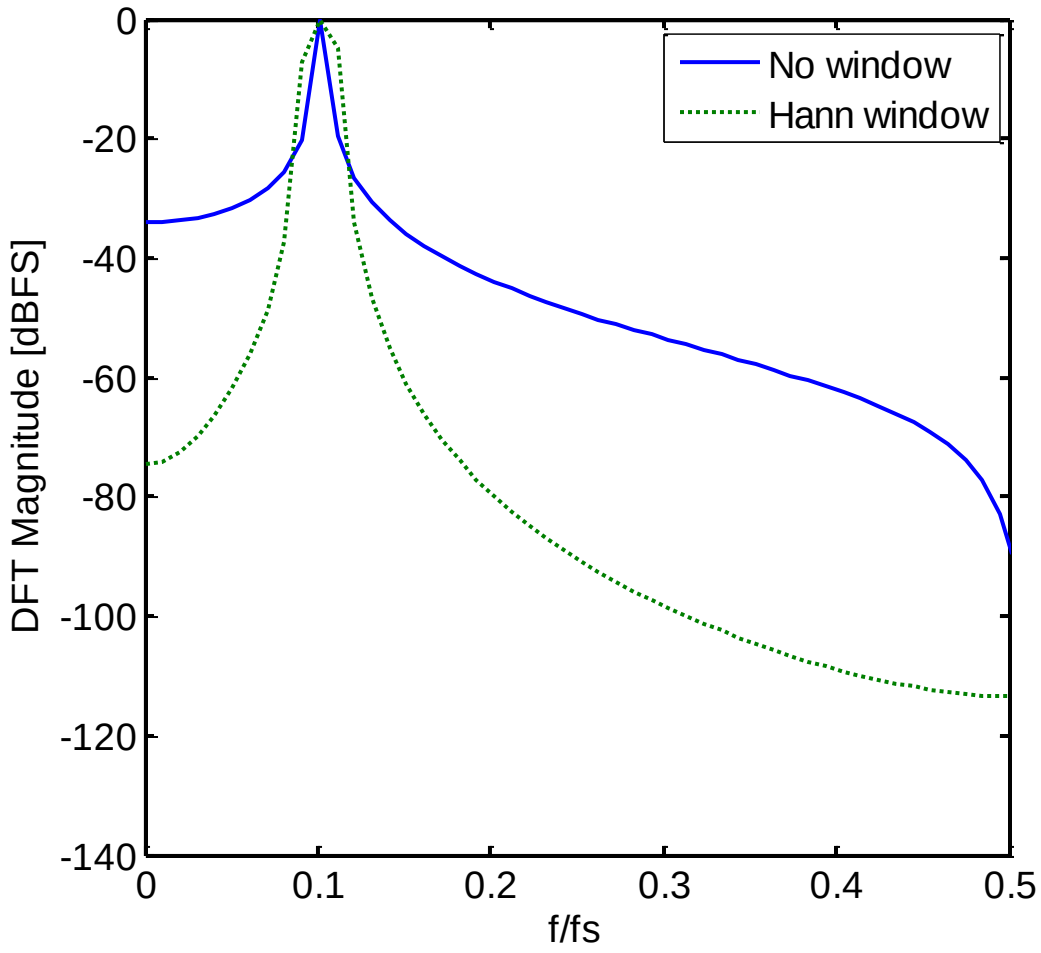
Hann Window

```
N=64;
wvtool(hann(N))
```



Spectrum with Window

```
N  = 100;
fs = 1000;
fx = 101;
A  = 1;

x = A*cos(2*pi*fx/fs*[0:N-1]);
s  = abs(fft(x));
x1 = x.*hann(N);
s1 = abs(fft(x1));
```



Integer Cycles versus Windowing

- Integer number of cycles
  - Test signal falls into single DFT bin
  - Requires careful choice of signal frequency
  - Ideal for simulations
  - For lab measurements, lock sampling and signal frequency generators (PLL)
    - "Coherent sampling“: $f_{\text{in}} = \frac{J}{M} f_s$ for M samples and GCD(J,M)=1
- Windowing
  - No restrictions on signal frequency
  - Signal and harmonics distributed over several DFT bins
    - Beware of smeared out nonidealities…
  - Requires more samples for given accuracy
- More info
  - http://www.maxim-ic.com/appnotes.cfm/appnote_number/1040

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Converter Spectral Analysis

Quantization Noise Spectrum

Example:

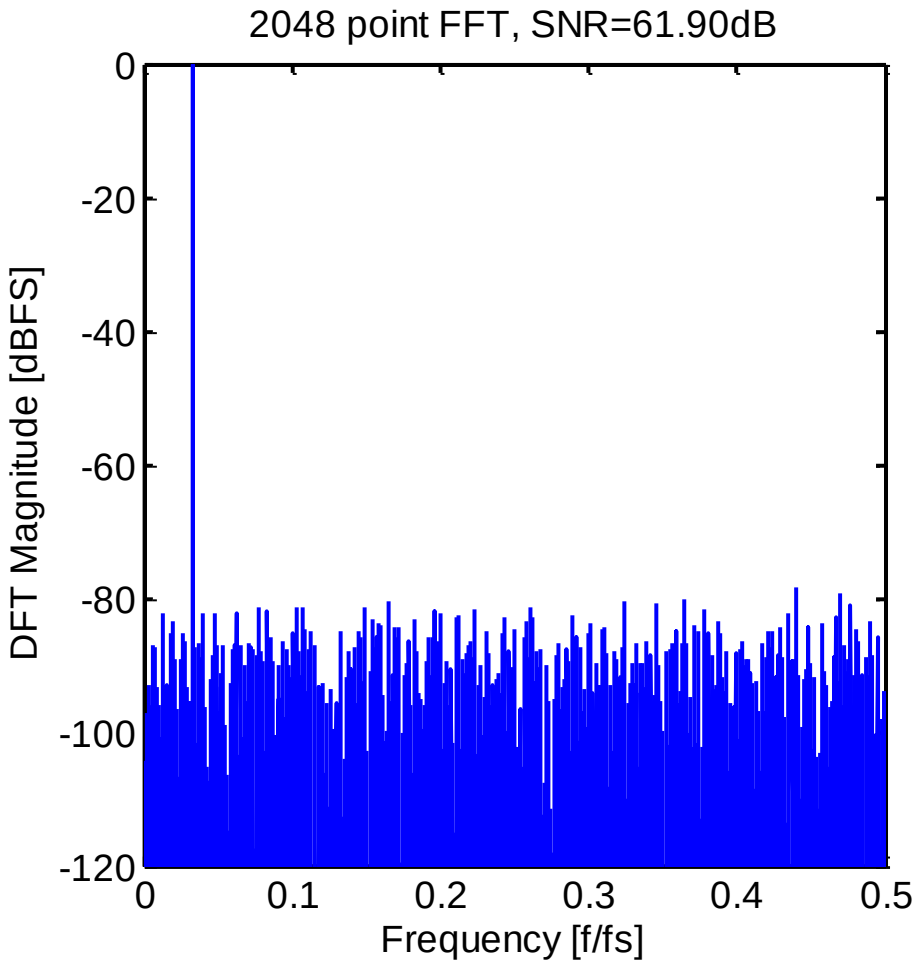
- Spectral analysis to evaluate (simulated) quantizer performance
- First look at quantization noise introduced by an ideal quantizer

```
N  = 2048;
cycles = 67;
fs = 1000;
fx = fs*cycles/N;
LSB = 2/2^10;

%generate signal, quantize (mid-tread) and take FFT
x = cos(2*pi*fx/fs*[0:N-1]);
x = round(x/LSB)*LSB;
s  = abs(fft(x));
s = s(1:end/2)/N*2;

% calculate SNR
sigbin = 1 + cycles;
noise = [s(1:sigbin-1), s(sigbin+1:end)];
snr = 10*log10( s(sigbin)^2/sum(noise.^2) );
```

Spectrum with Quantization Noise

- 0 dBFS = full-scale sinewave
- Spectrum looks fairly uniform
  Is this expected?
- Signal-to-quantization noise ratio equals power in signal bin (just one for coherent sampling), divided by sum of power in all noise bins
- Compare with "theory":

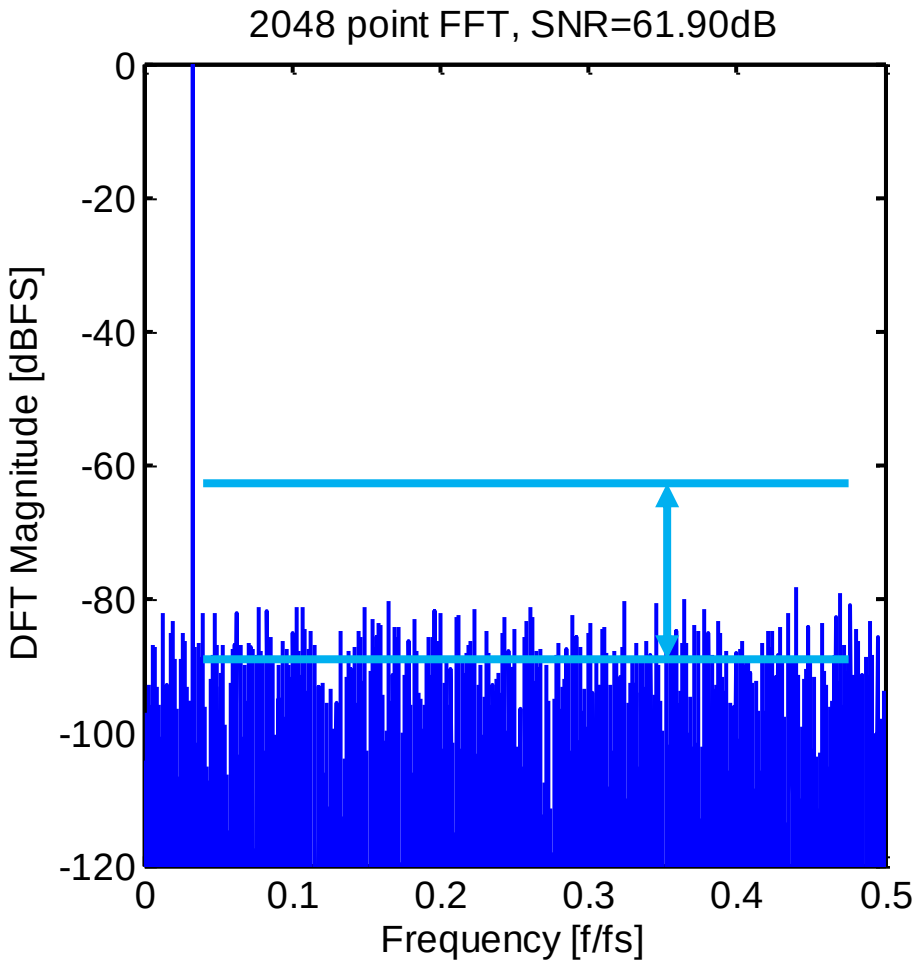
$$\begin{aligned}\text{SQNR} &= \frac{\text{Signal Power}}{\text{Quantization Noise Power}} \\ &= 6.02 \cdot N + 1.76\ [dB] \\ &= 61.9\ dB\end{aligned}$$



FFT Noise Floor

$$N_{floor} = -61.9\ dBc - 10\log\left(\frac{2048}{2}\right)$$
$$= -61.9\ dBc - 30.1\ dB$$
$$= -92\ dBc$$

- How could we lower the noise floor?
- Depends on FFT size
- Plot is “useless” if FFT size is not specified!

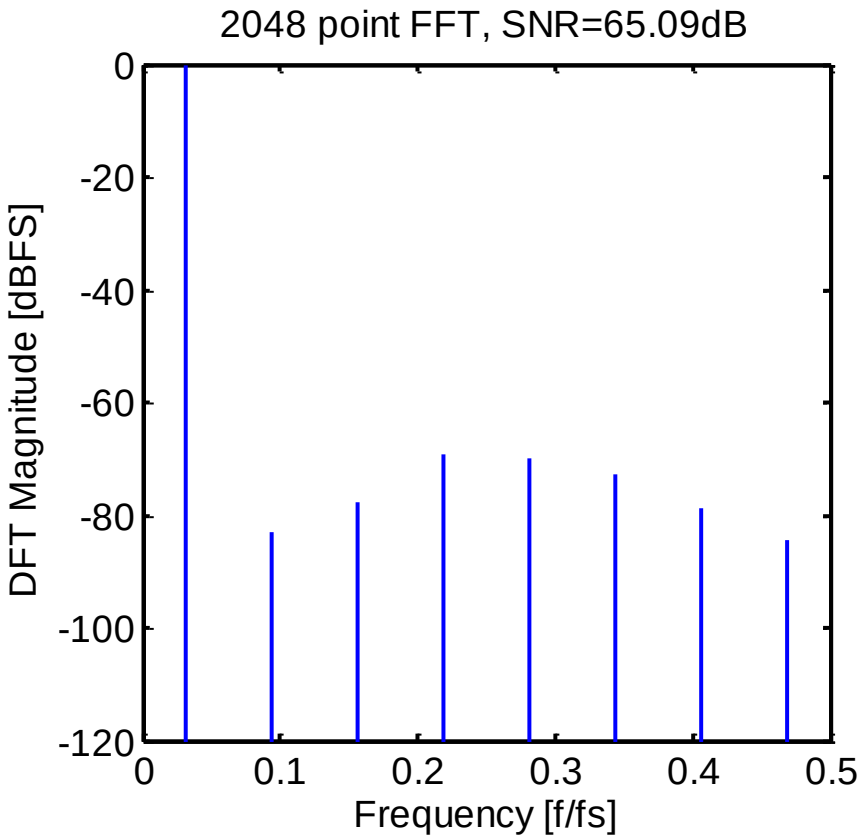


DFT Plot Annotation

- DFT plots are fairly meaningless unless you clearly specifiy the underlying conditions
- Most common annotation
  - Specify how many DFT points were used (N)
- Less common options
  - Shift DFT noise floor by $10\log_{10}(N/2)$dB
  - Normalize with respect to bin width in Hz and express noise as power spectral density
    - "Noise power in 1 Hz bandwidth„
- DFT should be averaged (e.g. using pwelch in MATLAB)
- Scaling: dBFS vs sinewave power (spectrum analyzer) vs power-spectral density (digital signal processing)

Periodic Quantization Noise

- Same as before, but cycles = 64 (instead of 67)
- $f_x = f_s \cdot 64/2048 = f_s/32$
- Quantization noise is highly deterministic and periodic
- For more random and "white" quantizion noise, it is best to make N and cycles mutually prime
  - GCD(N,cycles)=1

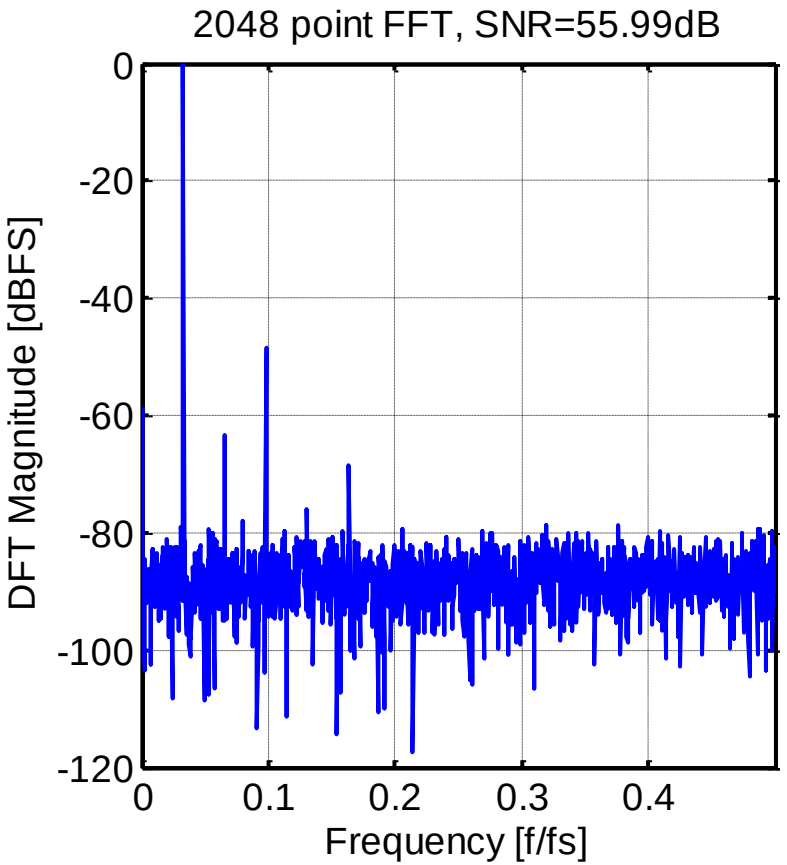


Typical ADC Output Spectrum

- Fairly uniform noise floor due to additional electronic noise
- Harmonics due to nonlinearities
- Definition of SNR

$$\text{SNR} = \frac{\text{Signal Power}}{\text{Total Noise Power}}$$

- Total noise power includes all bins except DC, signal, and 2nd through 7th harmonic
  - Both quantization noise and electronic noise affect SNR



SNDR and ENOB

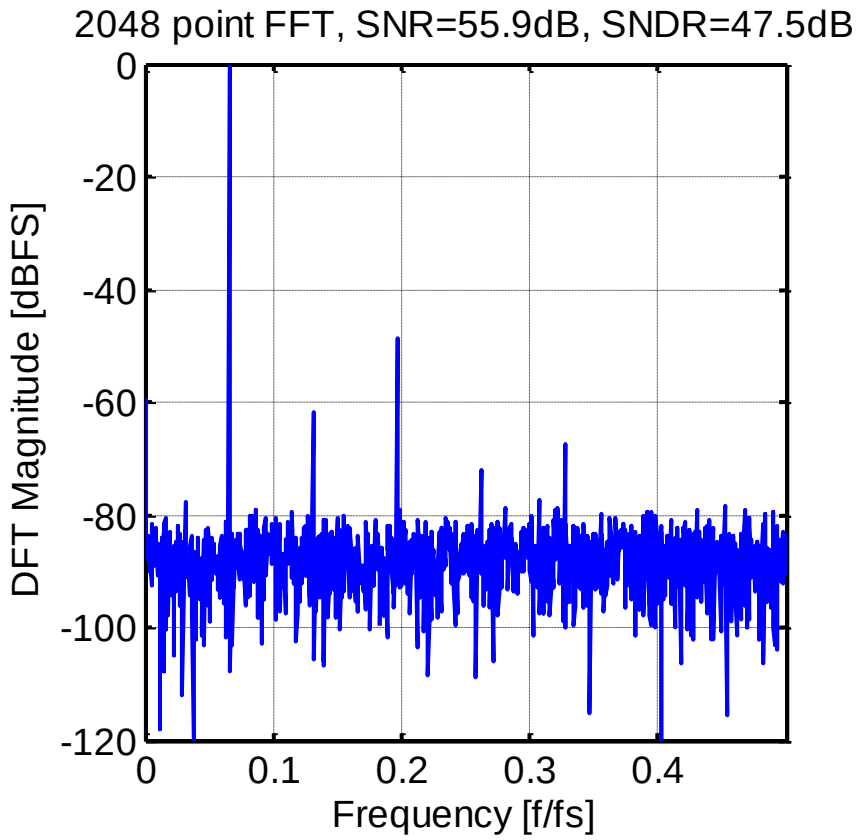
- Definition

$$\text{SNDR} = \frac{\text{Signal Power}}{\text{Noise and Distortion Power}}$$

- Noise and distortion power includes all bins except DC and signal

- Effective number of bits

$$\text{ENOB} = \frac{\text{SNDR(dB)} - 1.76\text{dB}}{6.02\text{dB}}$$



Effective Number of Bits

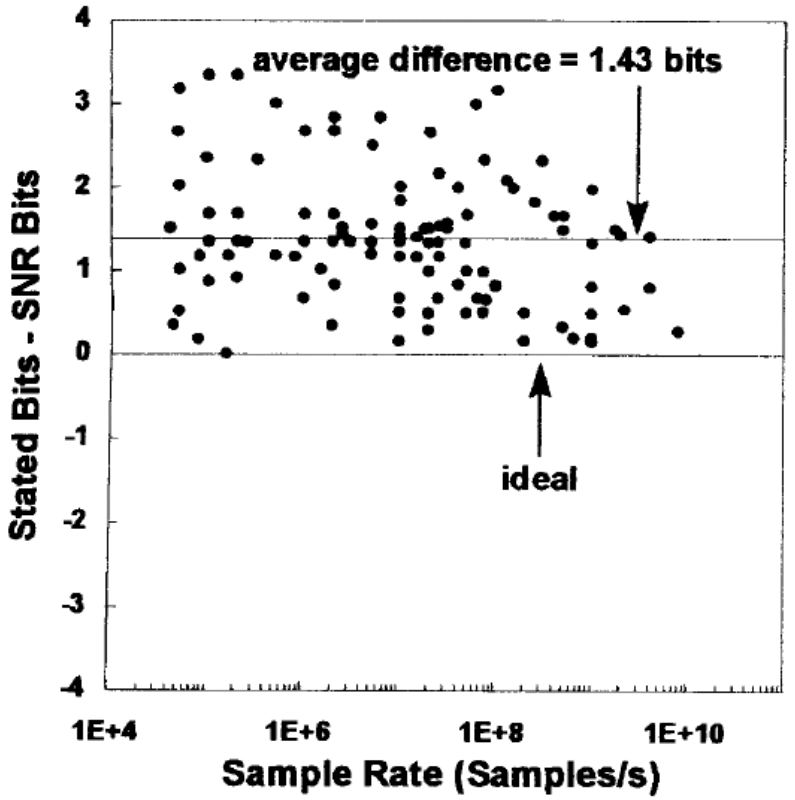
- Is a 10-Bit converter with 47.5dB SNDR really a 10-bit converter?

$$\text{ENOB} = \frac{47.5dB - 1.76\text{dB}}{6.02\text{dB}} = 7.6$$

- We get ideal ENOB only for zero electronic noise, perfect transfer function with zero INL, ...
- Low electronic noise is costly
  - Cutting thermal noise down by 2x, can cost 4x in power dissipation
- Rule of thumb for good power efficiency: ENOB < B-1
  - B is the "number of wires" coming out of the ADC or the so called "stated resolution"

Survey Data

$$\text{SNRBits} = \frac{\text{SNR(dB)-1.76dB}}{\text{6.02dB}}$$



R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. on Selected Areas in Communications*, pp. 539-50, April 1999

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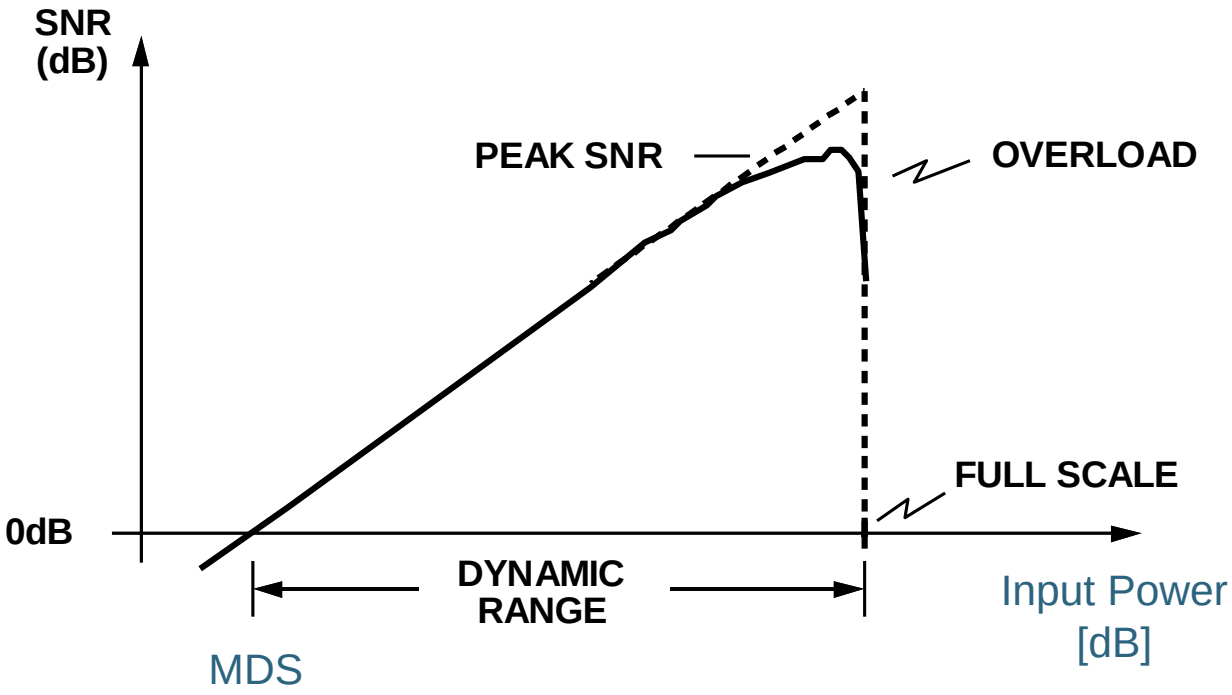
Dynamic Range & Distortion

Dynamic Range

$$\text{DR} = \frac{\text{Maximum Signal Power}}{\text{Minimum Detectable Signal}} \geq \text{SNR}_{\text{peak}}$$

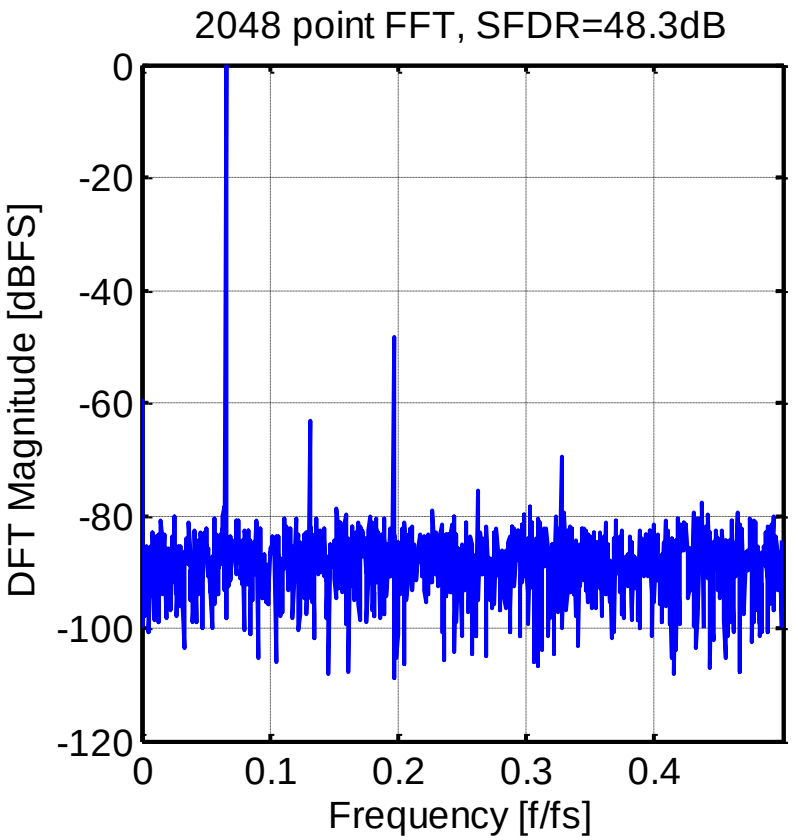


SFDR

- Definition of "Spurious Free Dynamic Range"

$$\text{SFDR} = \frac{\text{Signal Power}}{\text{Largest Spurious Power}}$$

- Largest spur is often (but not necessarily) a harmonic of the input tone
- SFDR represent smallest value of signal that can be distinguished from large interfering signal



SDR and THD

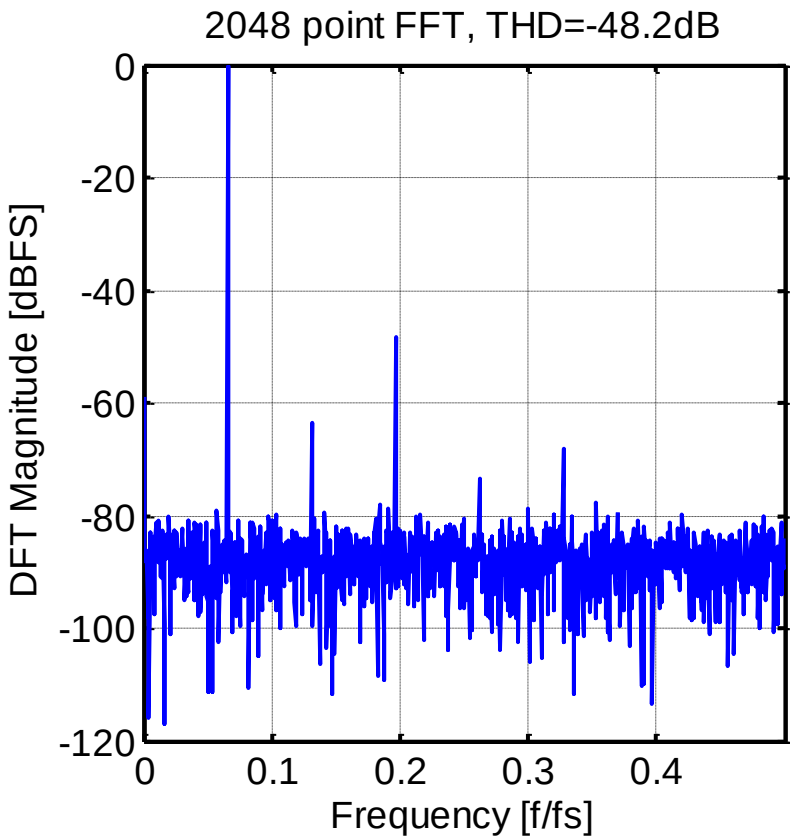
- Signal-to-distortion ratio

$$\text{SDR} = \frac{\text{Signal Power}}{\text{Total Distortion Power}}$$

- Total harmonic distortion

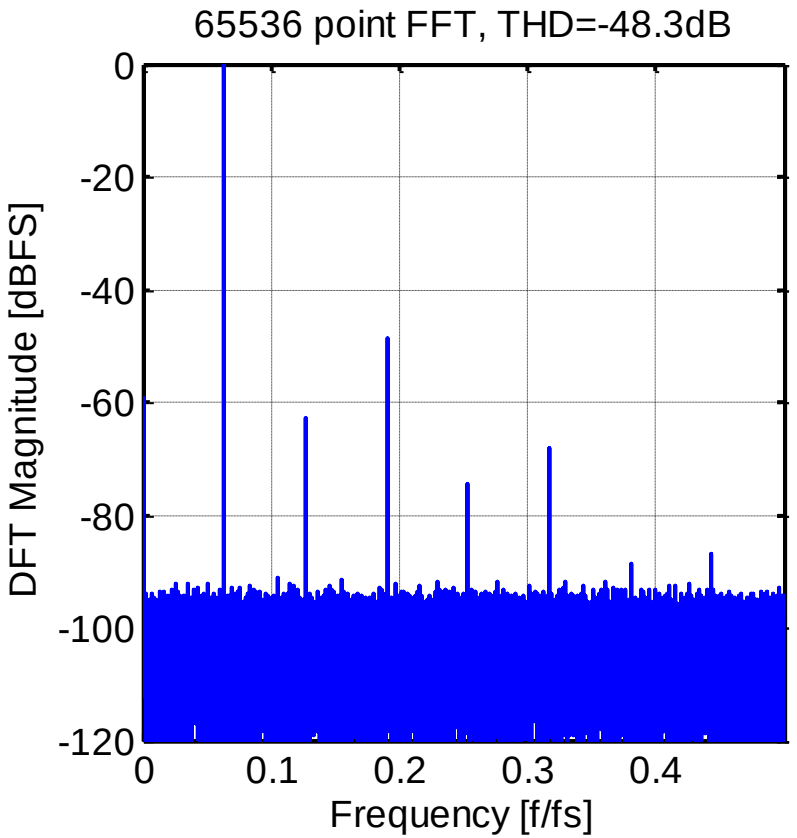
$$\text{THD} = \frac{\text{Total Distortion Power}}{\text{Signal Power}} = \frac{1}{\text{SDR}}$$

- By convention, total distortion power consists of 2nd through 7th harmonic
- Is there a 6th and 7th harmonic in the plot to the right?



Lowering the Noise Floor

- Increasing the FFT size let's us lower the noise floor and reveal low level harmonics



Aliasing

- Harmonics can appear at "arbitrary" frequencies due to aliasing

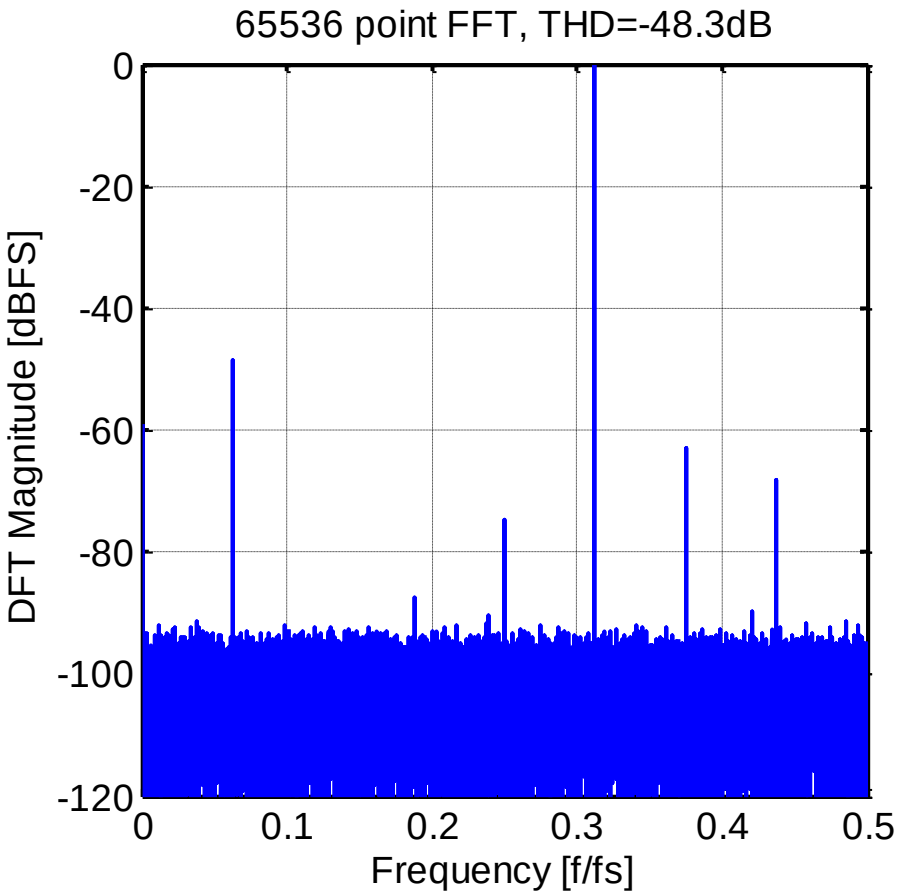
$f_1 = f_x = 0.3125\ f_s$

$f_2 = 2\ f_1 = 0.6250\ f_s \rightarrow 0.3750\ f_s$

$f_3 = 3\ f_1 = 0.9375\ f_s \rightarrow 0.0625\ f_s$

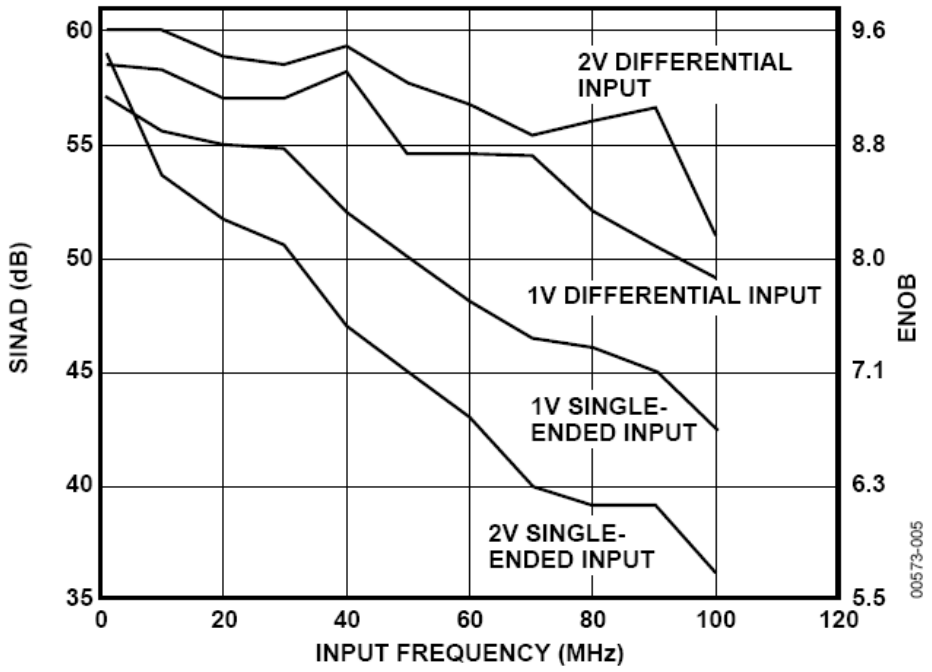
$f_4 = 4\ f_1 = 1.2500\ f_s \rightarrow 0.2500\ f_s$

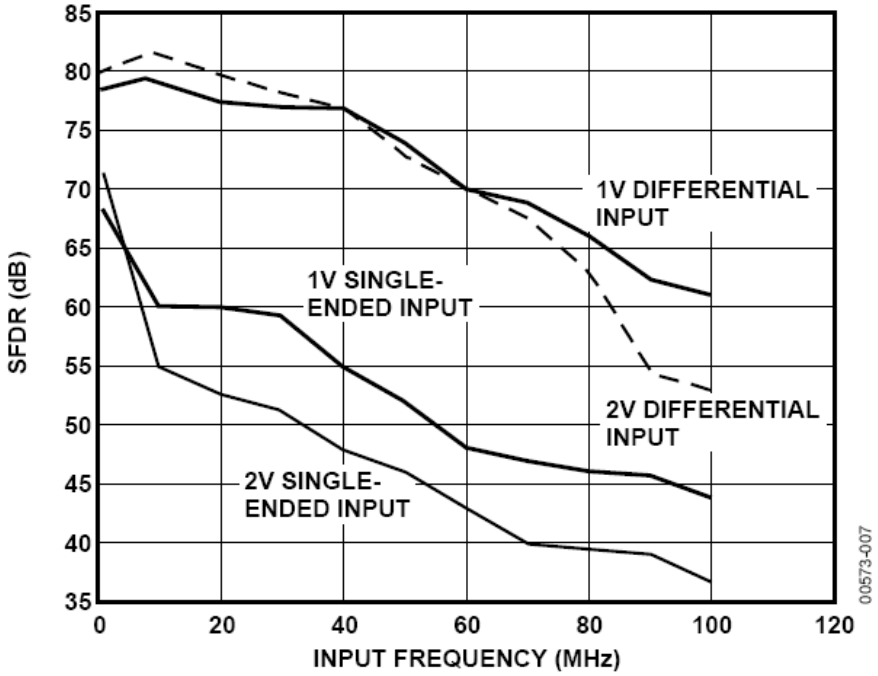
$f_5 = 5\ f_1 = 1.5625\ f_s \rightarrow 0.4375\ f_s$



Frequency Dependence

- Metrics generally depend on frequency
  - Sampling frequency and input frequency





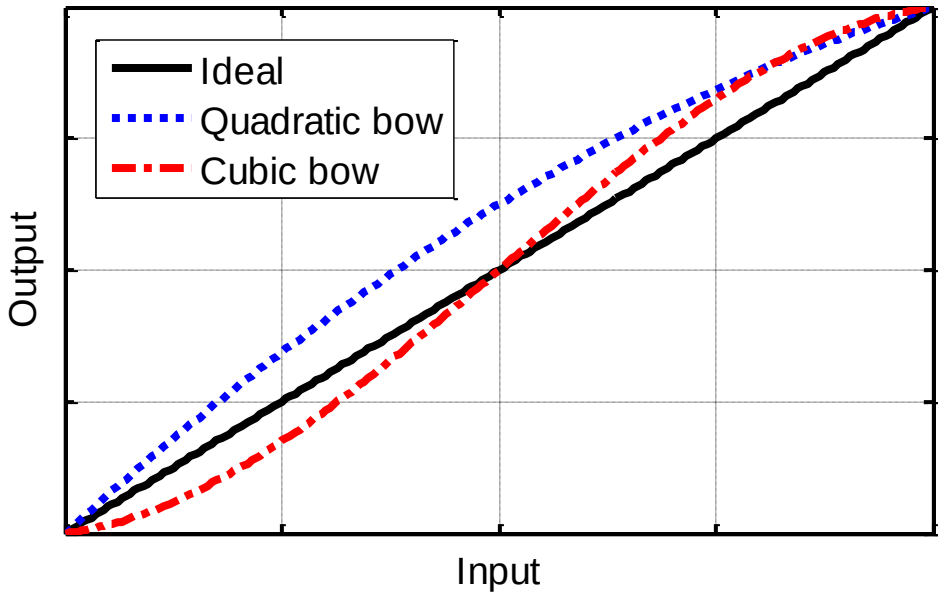
[Analog Devices, AD9203 Datasheet]

ERBW

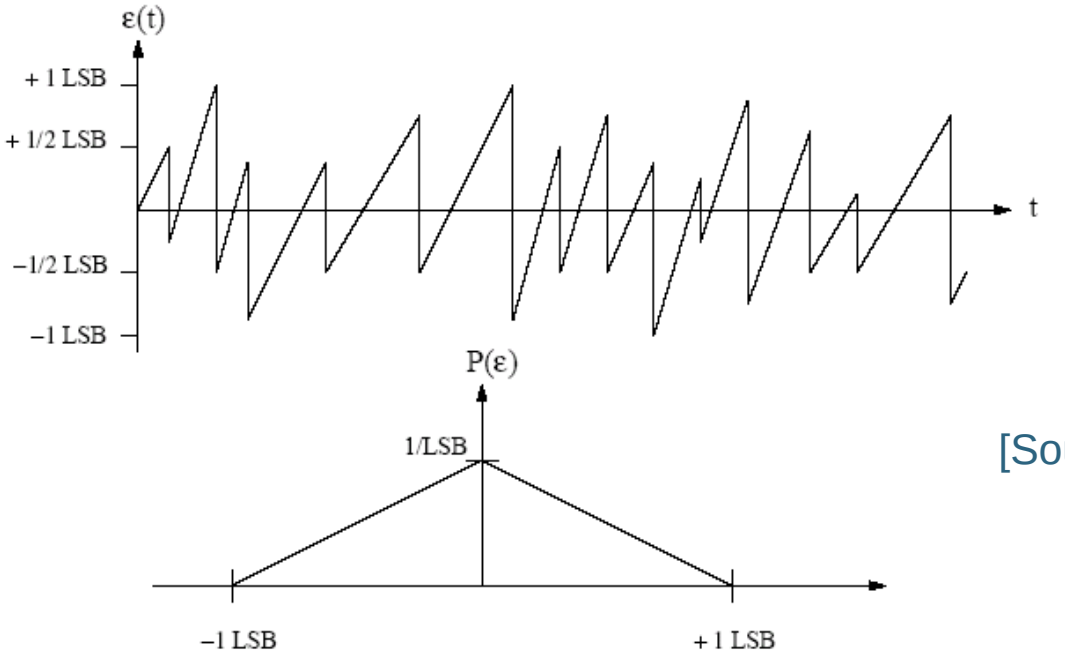
- Defined as the input frequency at which the SNDR of a converter has dropped by 3dB
  - Equivalent to a 0.5-bit loss in ENOB
- ERBW > $f_s/2$ is not uncommon, especially in converters designed for sub-sampling applications

Relationship Between INL and SFDR

- At low input frequencies, finite SFDR is mostly due to INL
- Quadratic/cubic bow gives rise to second/third order harmonic
- Rule of thumb: SFDR ≅ 20log(2^B/INL)
  - E.g. 1 LSB INL, 10 bits → SFDR ≅ 60dB



SNR Degradation due to DNL (1)



[Source: Ion Opris]

- For an ideal quantizer we assumed uniform quatization error over $\pm\Delta/2$
- Let's add uniform DNL over $\pm$ 0.5 LSB and repeat math...

SNR Degradation due to DNL (2)

- Integrate triangular pdf

$$\overline{e^2} = 2\int_0^{+\Delta}\left(1-\frac{e}{\Delta}\right)\frac{e^2}{\Delta}de = \frac{\Delta^2}{6} \qquad \Rightarrow \text{SNR} = 6.02\cdot B - 1.25 \ \text{[dB]}$$

3dB

- Compare to ideal quantizer

$$\overline{e^2} = \int_{-\Delta/2}^{+\Delta/2}\frac{e^2}{\Delta}de = \frac{\Delta^2}{12} \qquad \Rightarrow \text{SNR} = 6.02\cdot B + 1.76 \ \text{[dB]}$$

- Bottom line: non-zero DNL across many codes can easily cost a few dB in SNR
  - "DNL noise"

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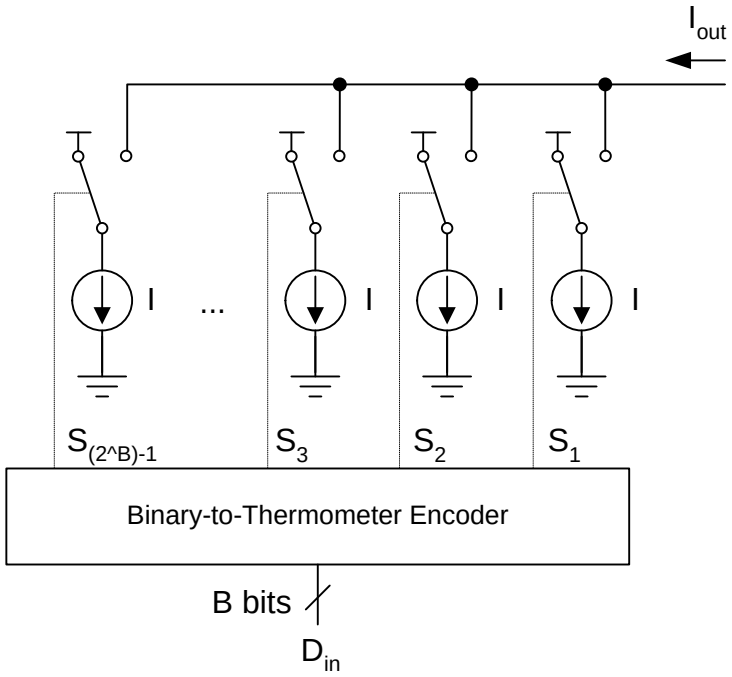
Error Sources

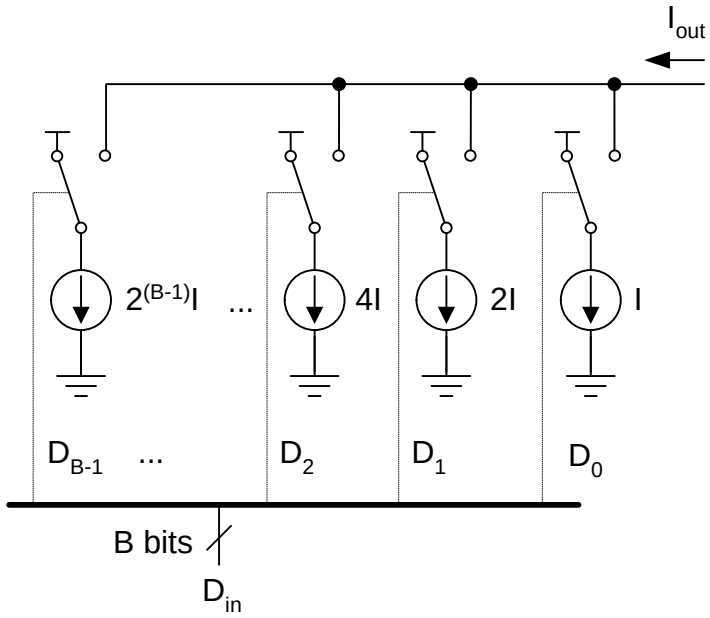
Motivation: Current DAC ("M-DAC")

Unit Element



2^B-1 switches

Binary Weighted

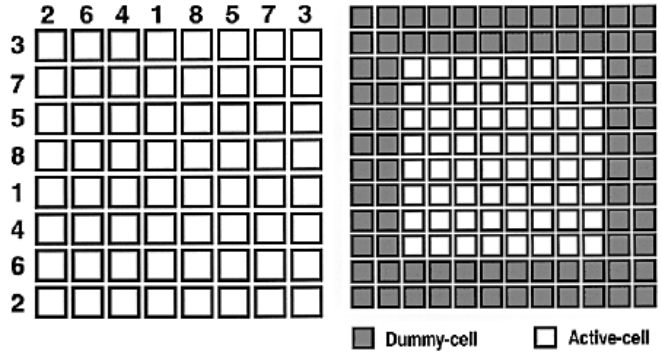


B switches

How do their DNL and INL compare?

Static Errors – Systematic

- Unit element mismatch cause INL and DNL errors
- Types of errors
  1. Systematic errors
     - Affect all circuits uniformly
     - E.g.
       - Contact and wiring resistance (IR drop)
       - Edge effects, process gradients
       - Finite current source output resistance
     - Can (in theory) be mitigated by proper layout and design



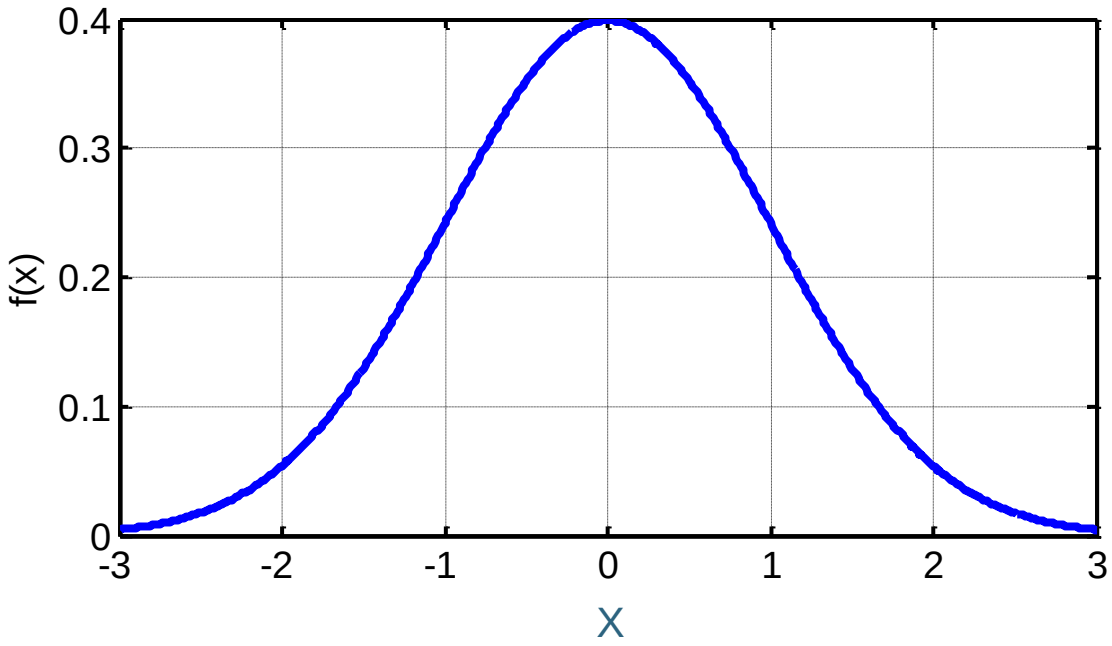
E.g.
[Lin, JSSC 12/98],
[Van der Plas, JSSC 12/99]

Static Errors – Random

2. Random errors
   - Vary randomly from device to device
   - Caused e.g. by material roughness, randomness in etching, …
   - Usually well approximated by a Gaussian PDF (central limit theorem)
   - References
     - C. Conroy et al., “Statistical Design Techniques for D/A Converters,” IEEE J. Solid-State Ckts., pp. 1118-28, Aug. 1989.
     - P. Crippa, et al., "A statistical methodology for the design of high-performance CMOS current-steering digital-to-analog converters," IEEE Trans. CAD of ICs and Syst. pp. 377-394, Apr. 2002.
     - M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits,* vol. 24, pp. 1433 - 1439, October 1989.
     - Jeroen A. Croon, Maarten Rosmeulen, Stefaan Decoutere, Willy Sansen, Herman E. Maes; *An easy-to-use mismatch model for the MOS transistor*, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1056 - 1064, August 2002.

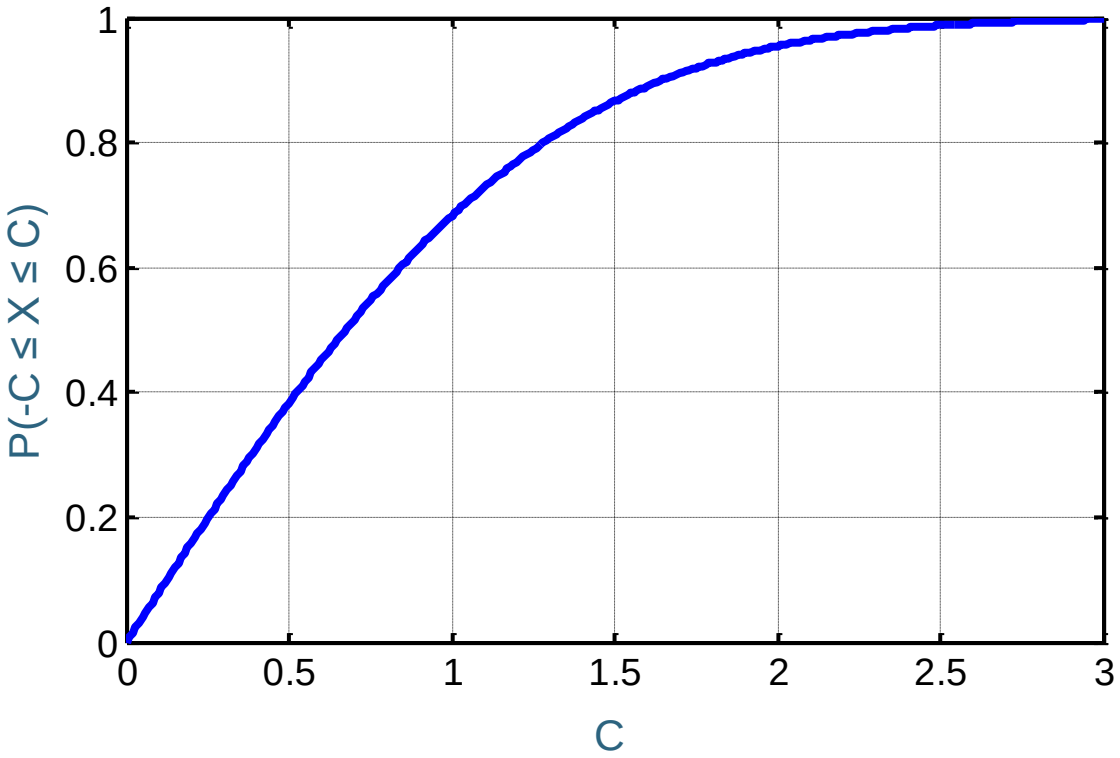
Gaussian Distribution

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \qquad X = \frac{x-\mu}{\sigma}$$



Yield (1)

$$P(-C \le X \le +C) = \frac{1}{\sqrt{2\pi}} \int_{-C}^{+C} e^{-\frac{X^2}{2}} dX = \text{erf}\left(\frac{C}{\sqrt{2}}\right)$$



Yield (2)

C	P(−C ≤ X ≤ C) [%]	C	P(−C ≤ X ≤ C) [%]
0.2000	15.8519	2.2000	97.2193
0.4000	31.0843	2.4000	98.3605
0.6000	45.1494	2.6000	99.0678
0.8000	57.6289	2.8000	99.4890
1.0000	68.2689	3.0000	99.7300
1.2000	76.9861	3.2000	99.8626
1.4000	83.8487	3.4000	99.9326
1.6000	89.0401	3.6000	99.9682
1.8000	92.8139	3.8000	99.9855
2.0000	95.4500	4.0000	99.9937

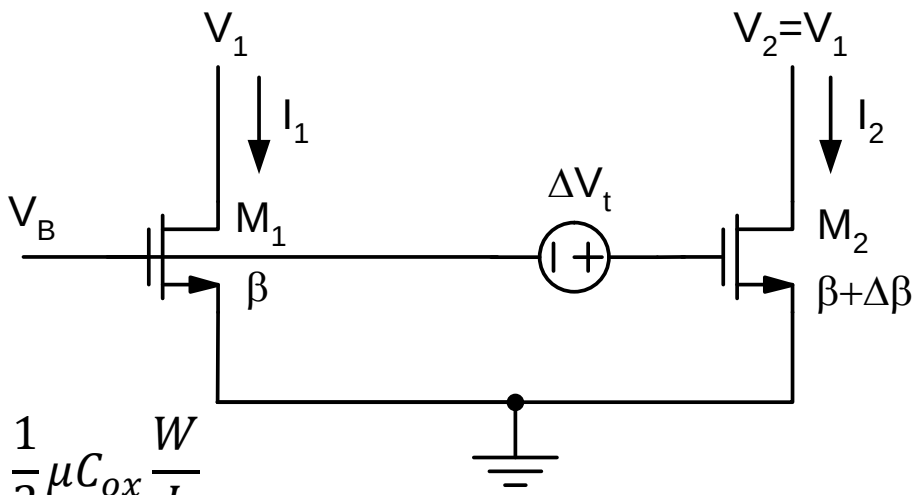
Example

- Measurements show that the current in a production lot of current sources follows a Gaussian distribution with σ = 0.1 mA and μ = 10 mA
  - What fraction of current sources is within ±3% (or ±1%) of the mean?
- Relative matching ("coefficient of variation")

$$\sigma_u = \frac{\sigma}{\mu} = \text{stdev}\left(\frac{\Delta I}{I}\right) = \frac{0.1mA}{10mA} = 1\%$$

- Fraction of current sources within 3%
  - C = 3 → 99.73%
- Fraction of current sources within 1%
  - C = 1 → 68.27%

Mismatch in MOS Current Sources



$$\beta = \frac{1}{2}\mu C_{ox}\frac{W}{L}$$

$$\Delta I = I_1 - I_2 \cong -g_m \Delta V_t + I_1 \frac{\Delta\beta}{\beta}$$

$$\frac{\Delta I}{I_1} \cong -\frac{g_m}{I_1}\Delta V_t + \frac{\Delta\beta}{\beta}$$

$$\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}} \qquad \sigma_{\frac{\Delta\beta}{\beta}} = \frac{A_\beta}{\sqrt{WL}}$$

- Example
  - W=500μm, L=0.2μm, g_m/I_D=10S/A, A_{Vt}=5mV-μm, A_β=1%-μm

$$\sigma_{\frac{\Delta I}{I_1}} = \sqrt{\left(10\frac{S}{A}\cdot\frac{5mV}{10}\right)^2 + \left(\frac{1\%}{10}\right)^2} = \sqrt{(0.5\%)^2 + (0.1\%)^2} = 0.51\%$$

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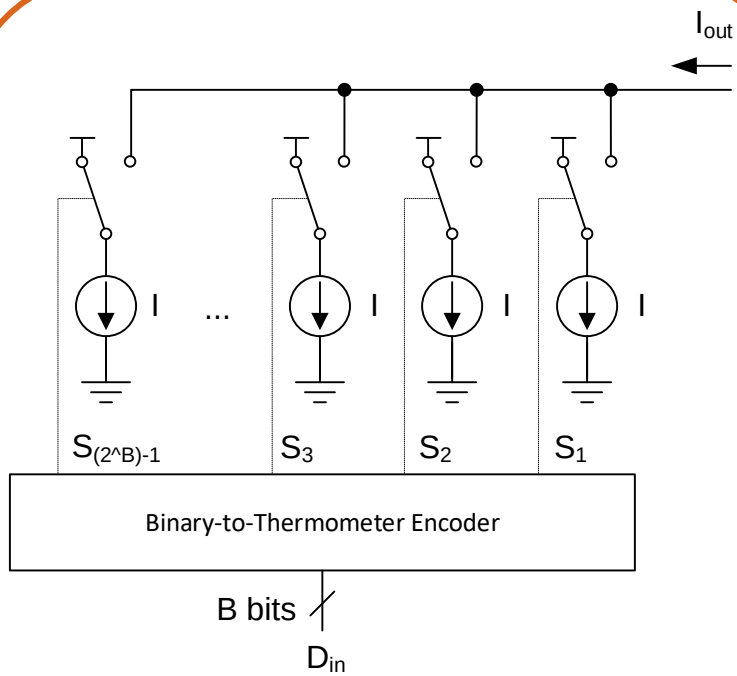
DNL & INL of Unit Element DAC

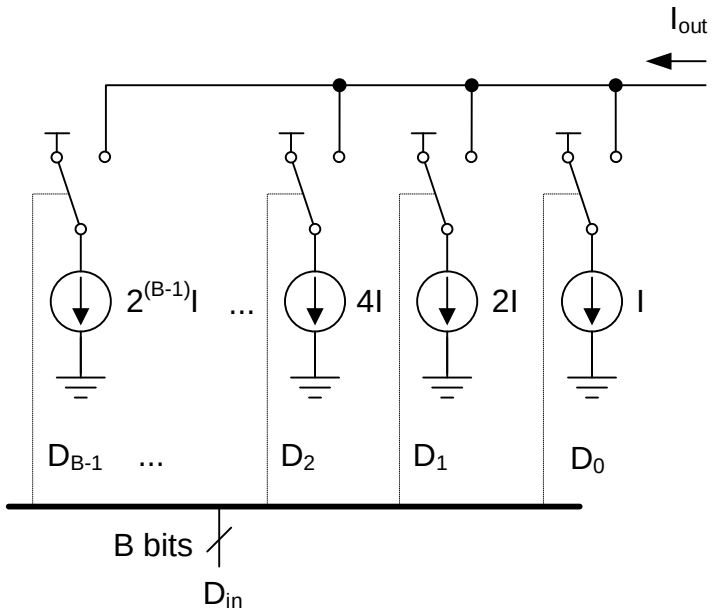
Unit Element DAC

Unit Element



2^B-1 switches

Binary Weighted



B switches

DNL of Unit Element DAC

$$\mathrm{DNL}(k) = \frac{\mathrm{Step}(k) - \mathrm{Step}_{\mathrm{avg}}}{\mathrm{Step}_{\mathrm{avg}}} = \frac{I_k - \frac{1}{N}\sum_{j=1}^{N} I_j}{\frac{1}{N}\sum_{j=1}^{N} I_j} \cong \frac{I_k - I}{I} = \frac{\Delta I}{I}$$

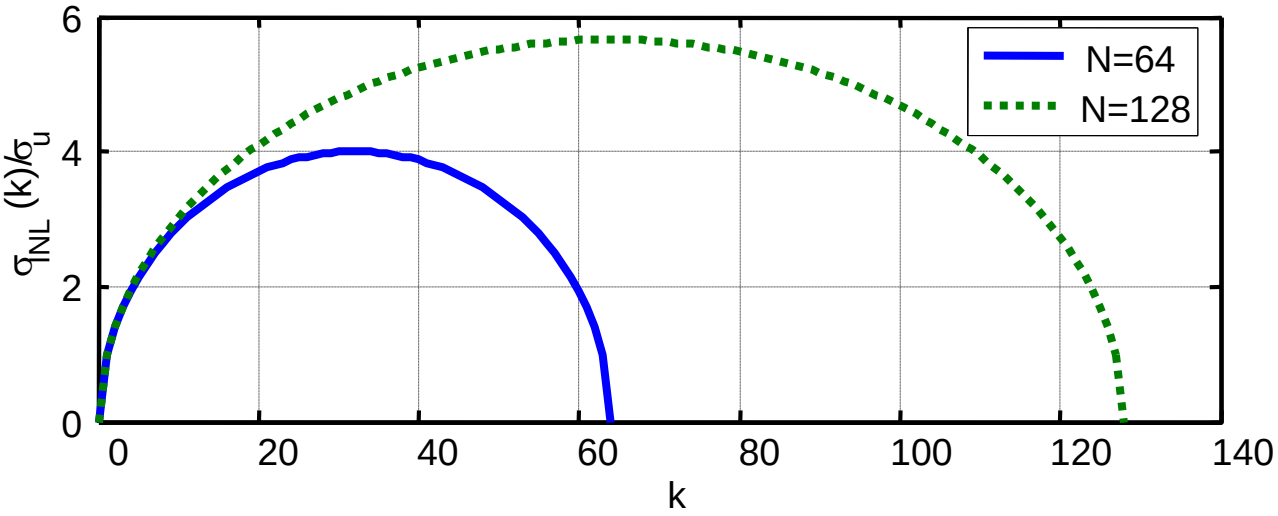
$$\mathrm{stdev}(\mathrm{DNL}(k)) = \mathrm{stdev}\left(\frac{\Delta I}{I}\right) = \sigma_u$$

- Standard deviation of DNL for each code is simply equal to relative matching (σ_u) of unit elements
- Example
  - Say we have unit elements with σ_u = 1% and want 99.73% of all converters to meet the spec
  - Which DNL specification value should go into the datasheet?

DNL Yield Example

- First cut solution
  - For 99.73% yield, need C = 3
  - $\sigma_{DNL} = \sigma_u = 1\%$
  - $3\ \sigma_{DNL} = 3\%$
  - DNL specification for a yield of 99.73% is ±0.03 LSB
    - Independent of target resolution (?)
- Not quite right
  - Must keep in mind that a converter will meet specs only if all codes meet DNL spec, i.e. $DNL(k) < DNL_{spec}$ for all k
  - A converter with more codes is less likely to have all codes meet the specification
  - E.g. for 12-Bit DAC, DNL spec should be ±0.0497 LSB
  - In practice: also affected by correlations → use (Monte Carlo) simulation & measurements

INL



- Standard deviation of INL is maximum at mid-scale (k=N/2)

$$\sigma_{\text{INL}} \cong \sigma_u \sqrt{\frac{N}{2}\left(1 - \frac{N/2}{N}\right)} = \frac{1}{2}\sigma_u\sqrt{N} \cong \frac{1}{2}\sigma_u\sqrt{2^B}$$

- For derivation of this result see
  [Kuboki et al., IEEE Trans. Circuits & Systems, 6/1982]

Maximum Achievable Resolution for INL

$$B \cong \log_2\left(4\left[\frac{\sigma_{\text{INL}}}{\sigma_u}\right]^2\right) = 2 + 2\log_2\left(\frac{\sigma_{\text{INL}}}{\sigma_u}\right)$$

- Example: σ_{INL}= 0.1 LSB (at mid-scale code)

σ_u	B
1%	8.6
0.5%	10.6
0.2%	13.3
0.1%	15.3

INL Yield

- Again, we should ask how many DACs will meet the spec for a given σ_{INL} (worst code)
  - It turns out that this is a difficult math problem
- Two solutions
  - Do the math
    - G. I. Radulov et al., "Brownian-Bridge-Based Statistical Analysis of the DAC INL Caused by Current Mismatch," IEEE TCAS II, pp. 146-150, Feb. 2007.
  - Yield simulations
- Good rule of thumb
  - For high target yield (>95%), the probability of "all codes meet INL spec" is very close to "worst code meets INL spec"

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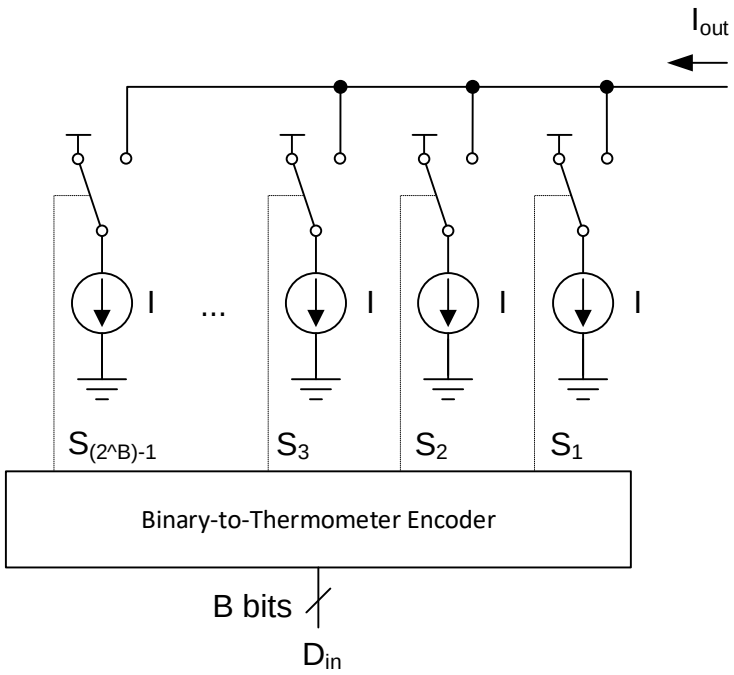
DNL & INL of Binary Weighted DAC

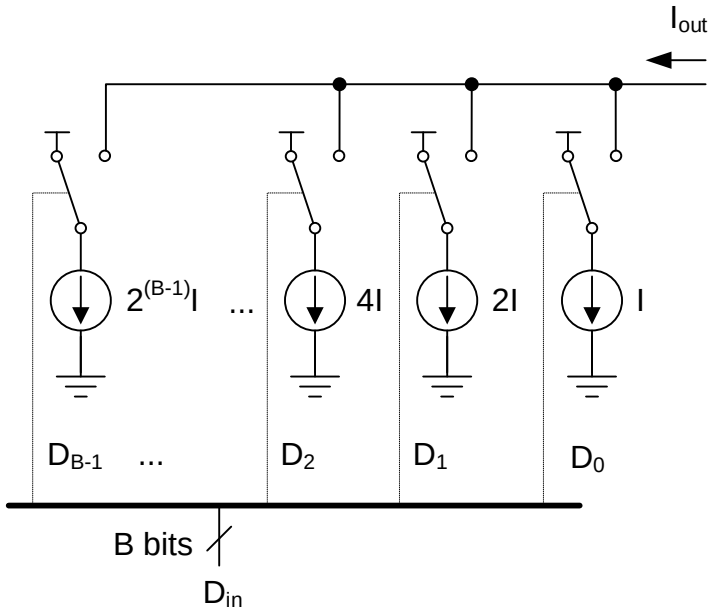
Unit Element DAC

Unit Element



2^B-1 switches

Binary Weighted

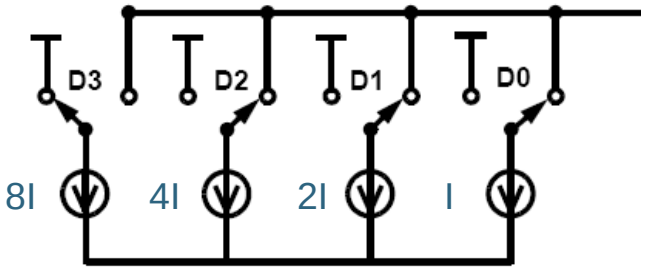


B switches

DNL/INL of Binary Weighted DAC

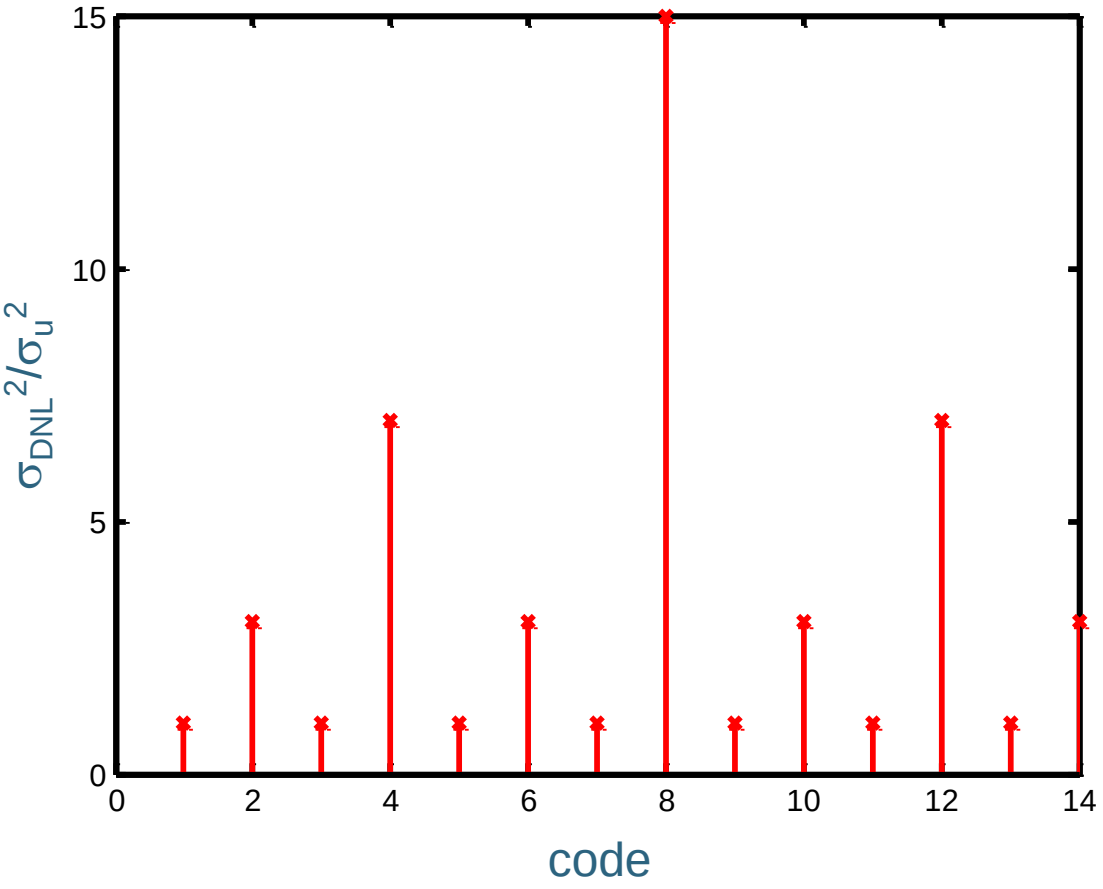
- INL same as for thermometer DAC
  - Why?
- DNL is not same for all codes, but depends on transition
- Consider worst case: 0111 … → 1000 …
  - Turning on MSB and turning off all LSBs

$$\sigma_{DNL}^2 = \underbrace{\left(2^{B-1}-1\right)\sigma_u^2}_{0111\ldots} + \underbrace{\left(2^{B-1}\right)\sigma_u^2}_{1000\ldots} = \left(2^B-1\right)\sigma_u^2$$

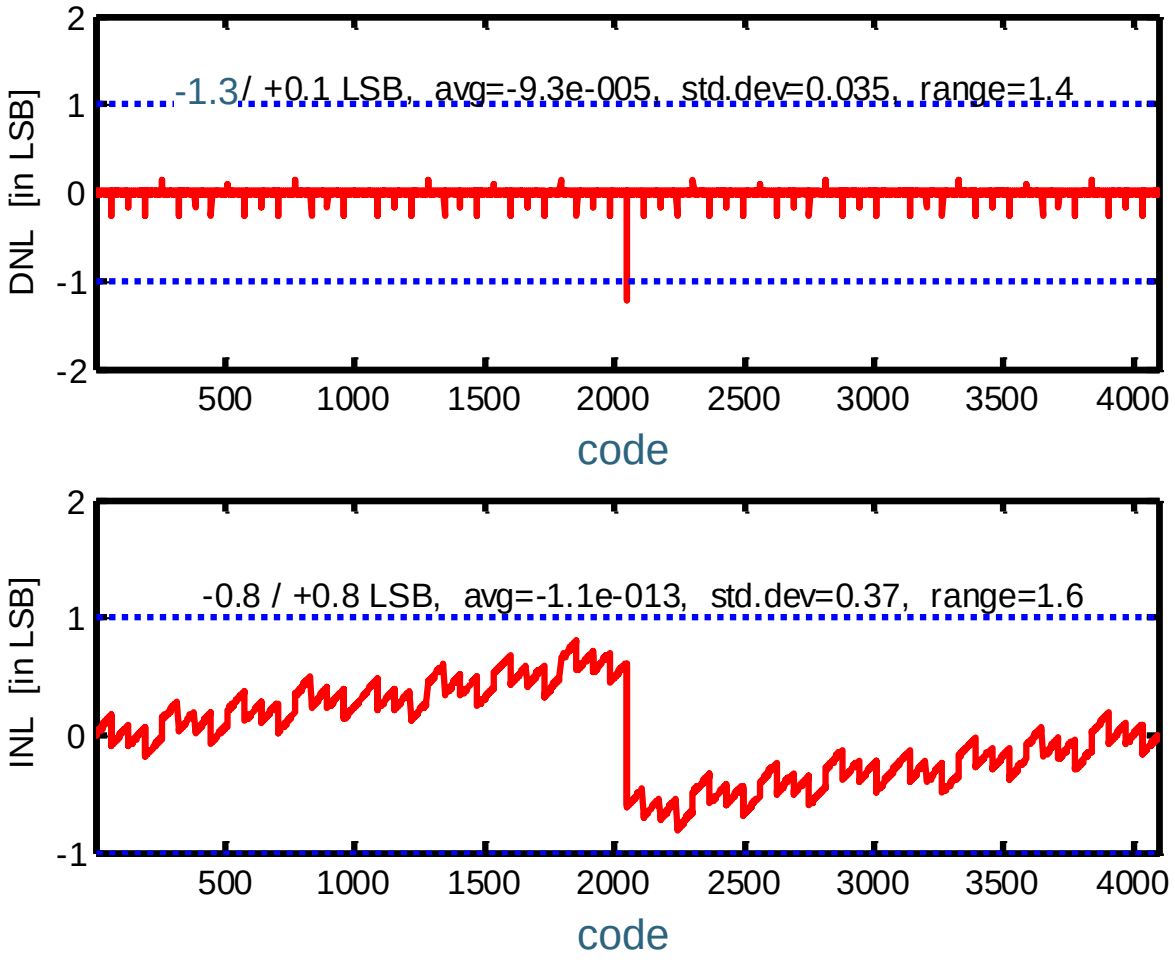


- Example
  - B = 12, σ_u = 1% → σ_{DNL} = 0.64 LSB
  - Much worse than thermometer DAC

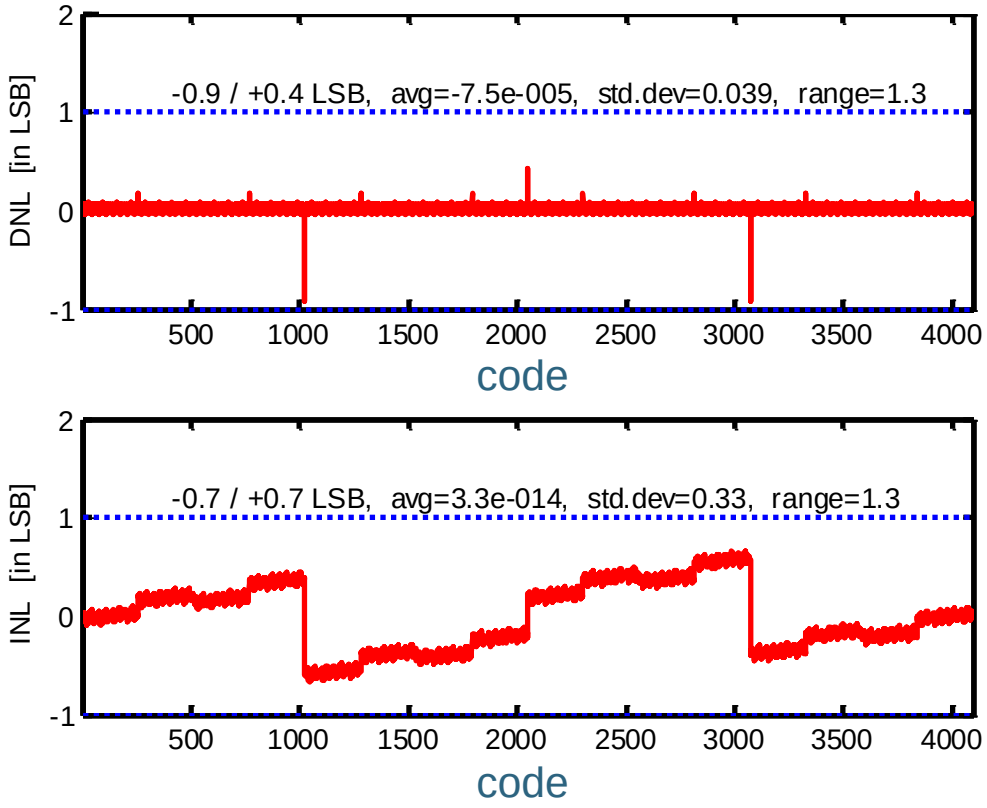
σ_{DNL} (4-bit Example)



Simulation Example



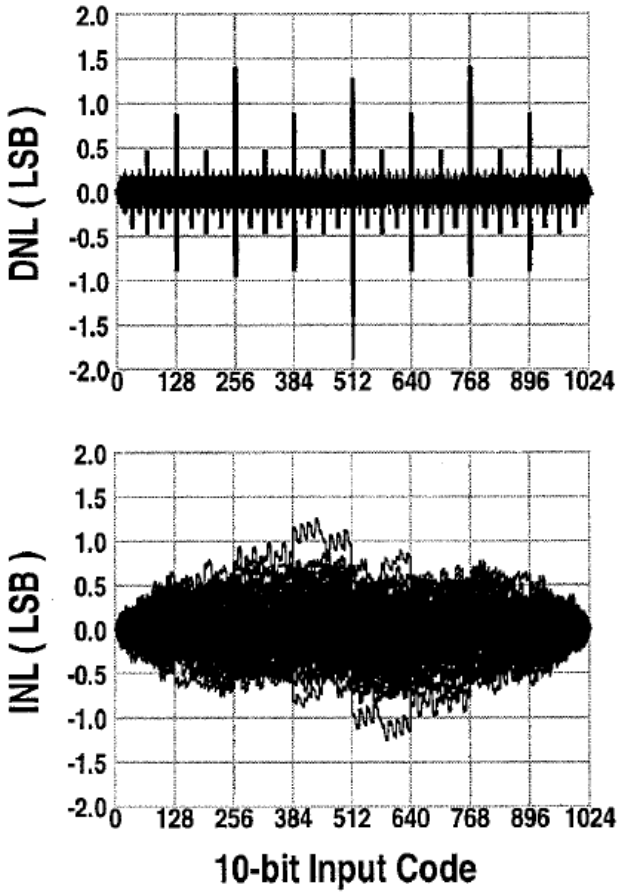
Another Random Run



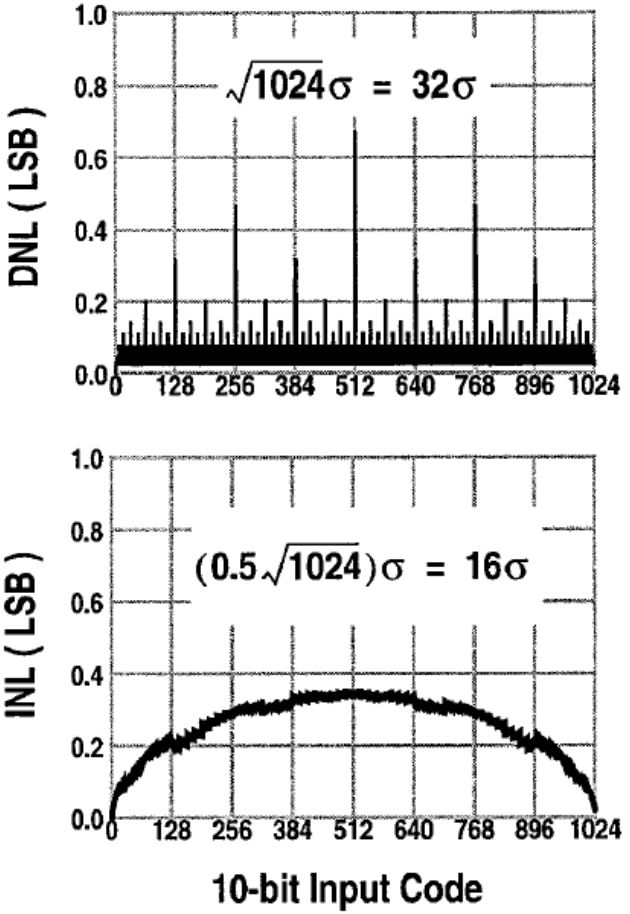
- Peak DNL not at mid-scale!
  - Important to realize that this is just one single statistical outcome…

Multiple Simulation Runs (100)

Overlay Plot



RMS DNL and INL



[Lin & Bult, JSSC 12/1998]

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Segmented DAC

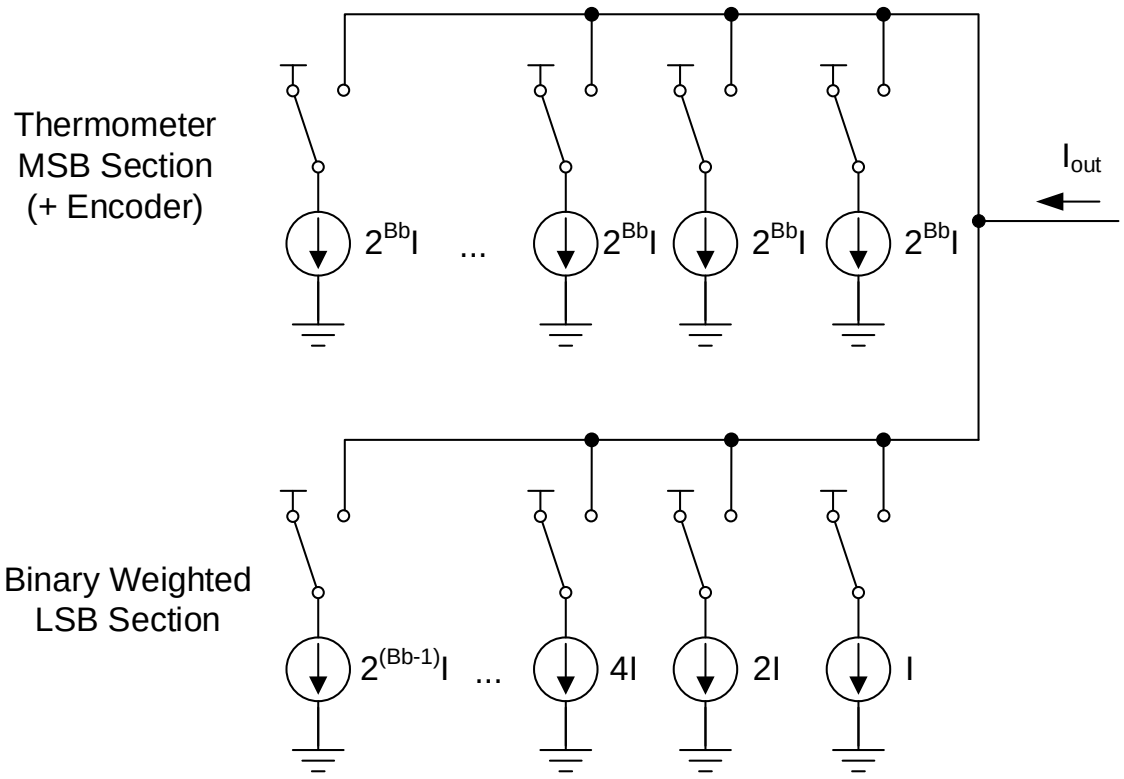
Comparison

	Unit Element	Compromise?	Binary Weighted
σ_{INL} (worst case)	$\cong \frac{1}{2}\sigma_u\sqrt{2^B}$		
σ_{DNL} (worst case)	$\cong \sigma_u$	?	$\cong \sigma_u\sqrt{2^B-1}$
Number of Switched Elements	2^B-1	?	B

Example (B=16, σ_u=0.5%)

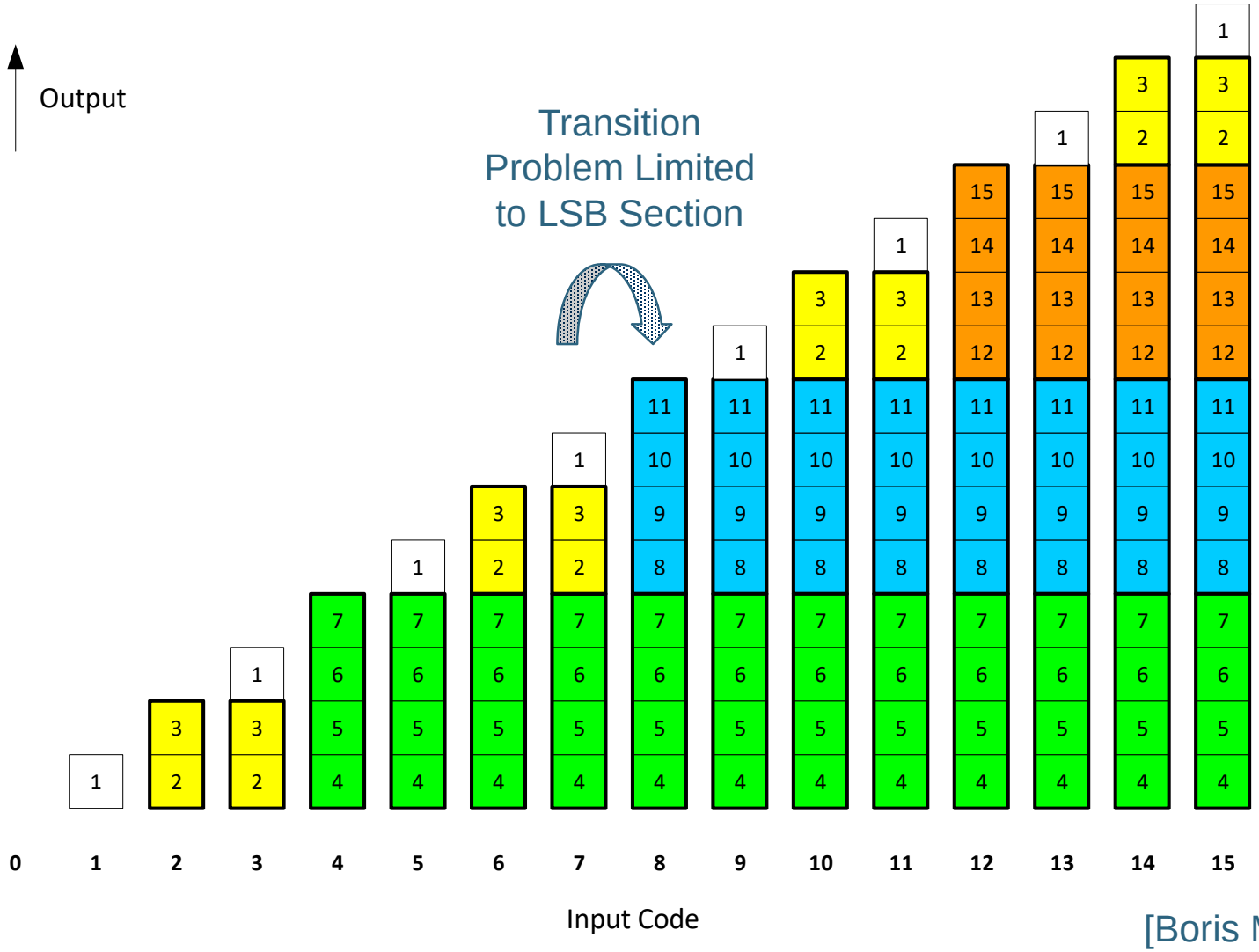
DAC Architecture	σ_{INL} (worst)	σ_{DNL} (worst)	Number of Switched Elements
Unit Element	0.64	0.005	65535
Binary Weighted	0.64	1.28	16
Compromise?	?	?	?

Segmented DAC



- Binary weighted section with B_b bits
- Thermometer section with $B_t = B - B_b$ bits
- Typically $B_t \sim 4 \ldots 8$
- Reasonably small encoder
- Easier to achieve monotonicity

Segmented DAC (2-2)



[Boris Murmann]

Comparison

	Thermometer	Segmented	Binary Weighted
σ_{INL} (worst case)	$\cong \frac{1}{2}\sigma_u\sqrt{2^B}$		
σ_{DNL} (worst case)	$\cong \sigma_u$	$\cong \sigma_u\sqrt{2^{B_b+1}-1}$	$\cong \sigma_u\sqrt{2^B-1}$
Number of Switched Elements	2^B-1	$B_b+2^{B_t}-1$	B

Example (B=12, σ_u=1%)

DAC Architecture	σ_{INL} (worst)	σ_{DNL} (worst)	Number of Switched Elements
Thermometer	0.32	0.01	4095
Binary Weighted	0.32	0.64	12
Segmented (B_b=7, B_t=5)	0.32	0.16	38

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Dynamic DAC Errors

Dynamic DAC Errors (1)

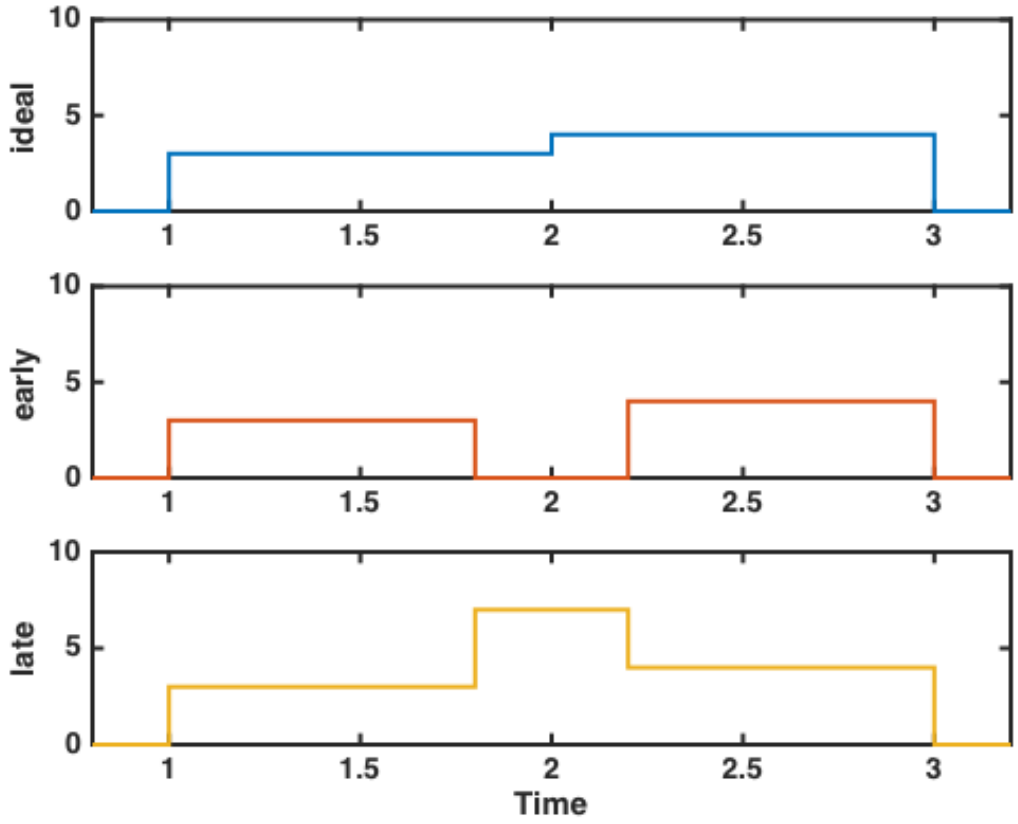
- Finite settling time and slewing
  - Finite RC time constant
  - Signal dependent slewing
- Feedthrough
  - Coupling from switch signals to DAC output
  - Clock feedthrough
- Glitches due to timing errors
  - Current sources won't switch simultaneously

Dynamic DAC Errors (2)

- References
  - Gustavsson, Chapter 12
  - M. Albiol, J.L. Gonzalez, E. Alarcon, "Mismatch and dynamic modeling of current sources in current-steering CMOS D/A converters," IEEE TCAS I, pp. 159-169, Jan. 2004
  - Doris, van Roermund, Leenaerts, Wide-Bandwidth High Dynamic Range D/A Converters, Springer 2006.
  - T. Chen and G.G.E. Gielen, "The analysis and improvement of a current-steering DAC's dynamic SFDR," IEEE Trans. Ckts. Syst. I, pp. 3-15, Jan. 2006.

Glitch Impulse (1)

- DAC output waveform depends on timing
  - Consider binary weighted DAC transition 0111… → 1000…



Ideal

LSBs early, MSB late

LSBs late, MSB early

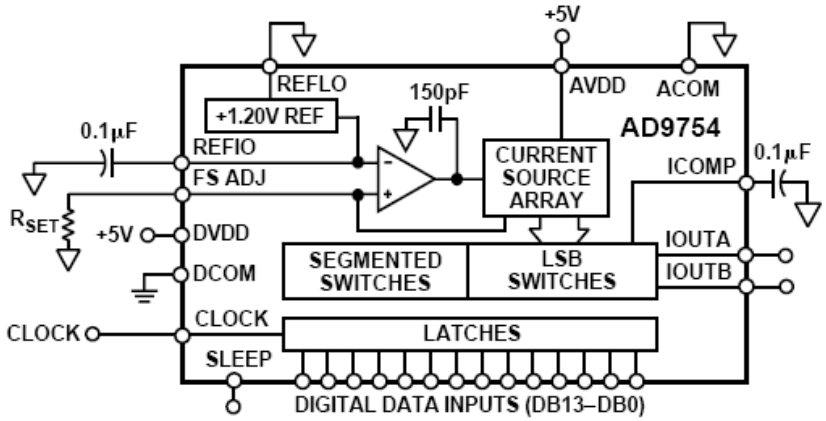
Glitch Impulse (2)

- Worst case glitch impulse (area): $\propto \Delta t \, 2^{B-1}$
- LSB area: $\propto T$
- Need $\Delta t \, 2^{B-1} << T$ which implies $\Delta t << T/2^{-B+1}$

f_s [MHz]	B	Δt [ps]
1	12	<< 488
20	16	<< 1.5
1000	10	<< 2

- Need low jitter clock & distribution

Commercial Example



AD9754

DYNAMIC SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	125			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		35		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)		30		pA/√Hz

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DAC Implementation

Implementation Example

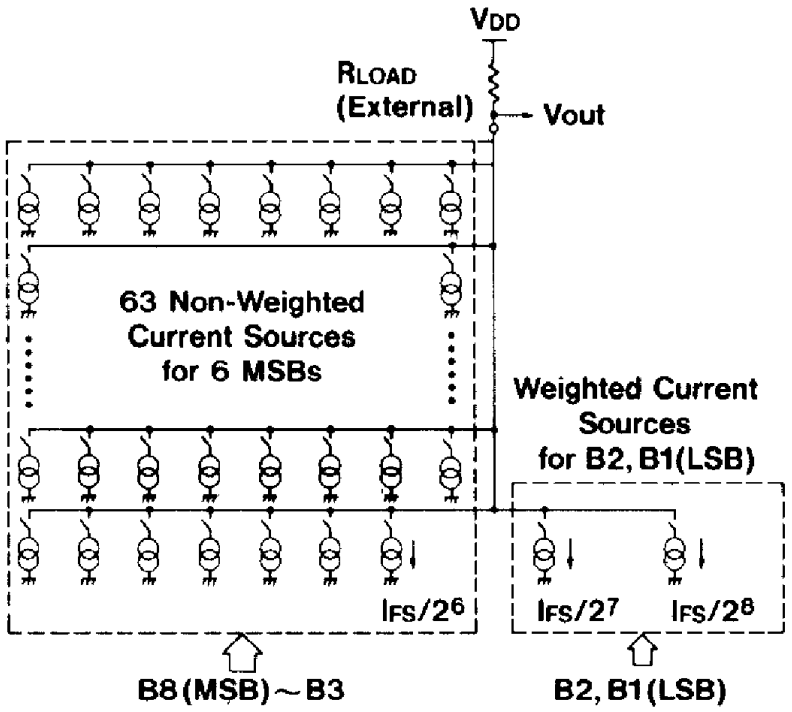


Fig. 1. Basic architecture of the DAC.

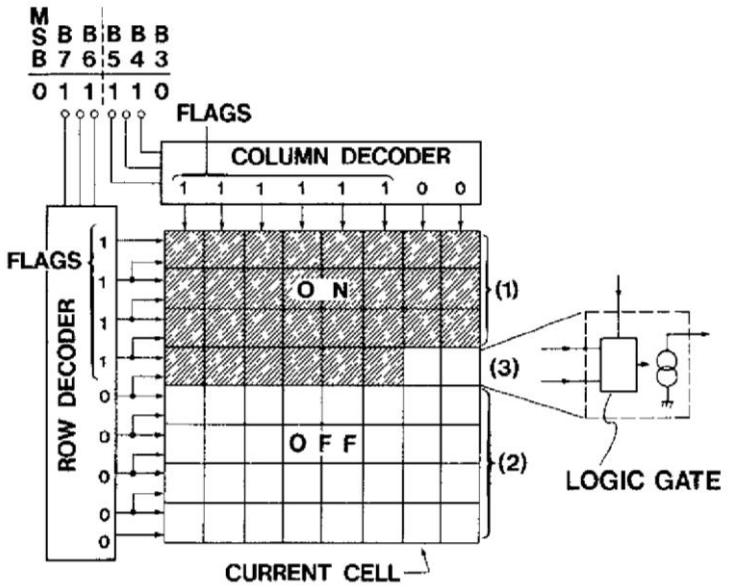
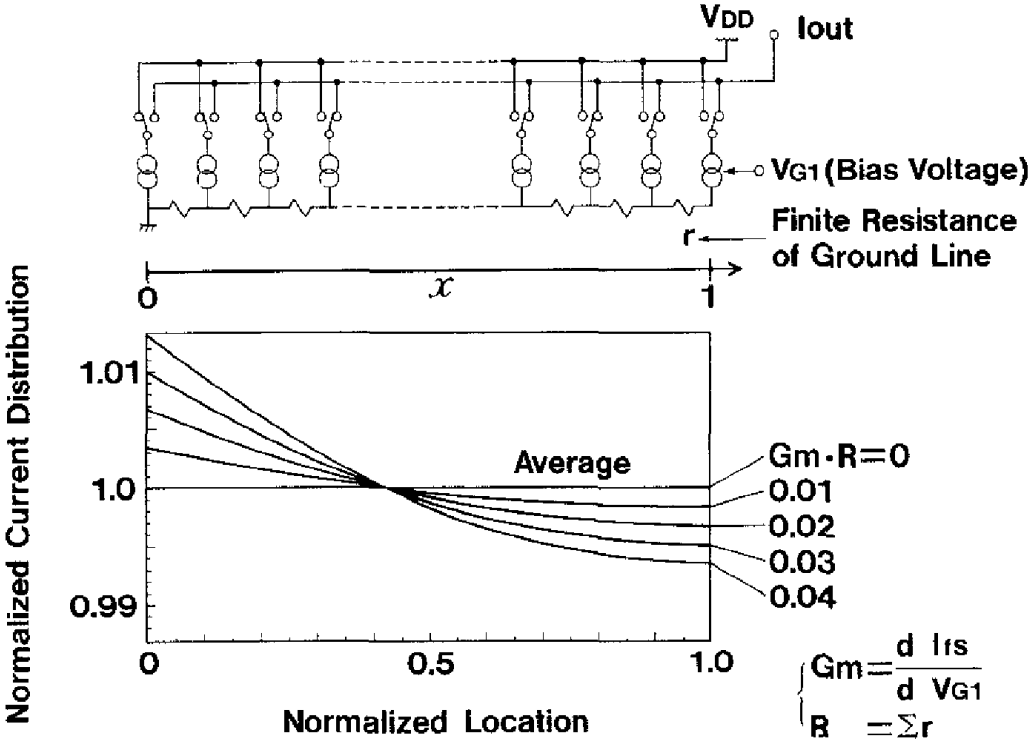


Fig. 2. Two-step decoding.

[T. Miki, Y. Nakamura, M. Nakaya, S. Asai, Y. Akasaka, and Y. Horiba, "An 80-MHz 8-bit CMOS D/A Converter," IEEE J. of Solid-State Circuits, pp. 983-988, Dec. 1986.]

Mitigating IR Drop



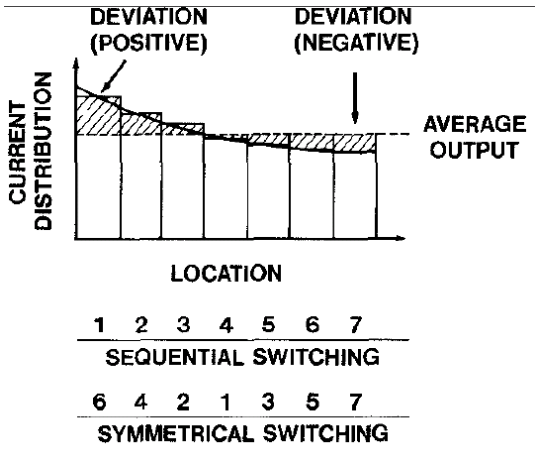
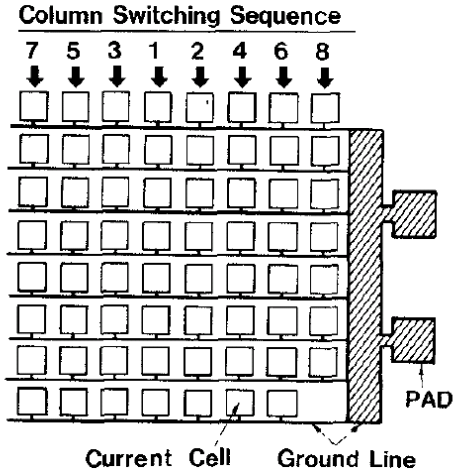
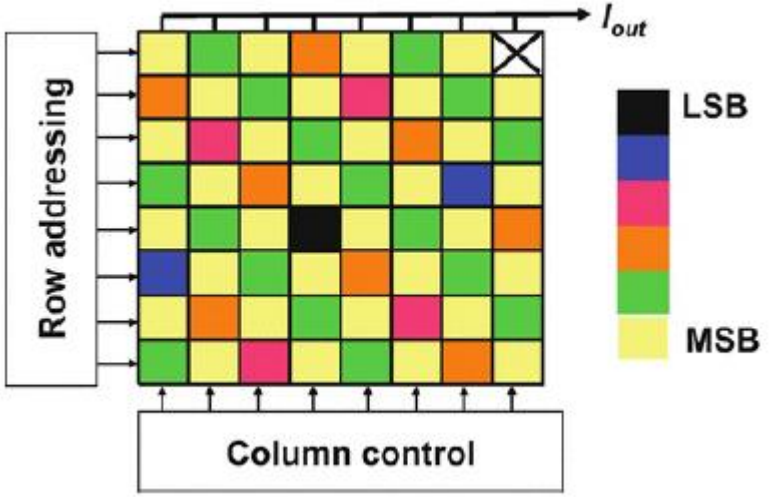


Fig. 9. Symmetrical switching.



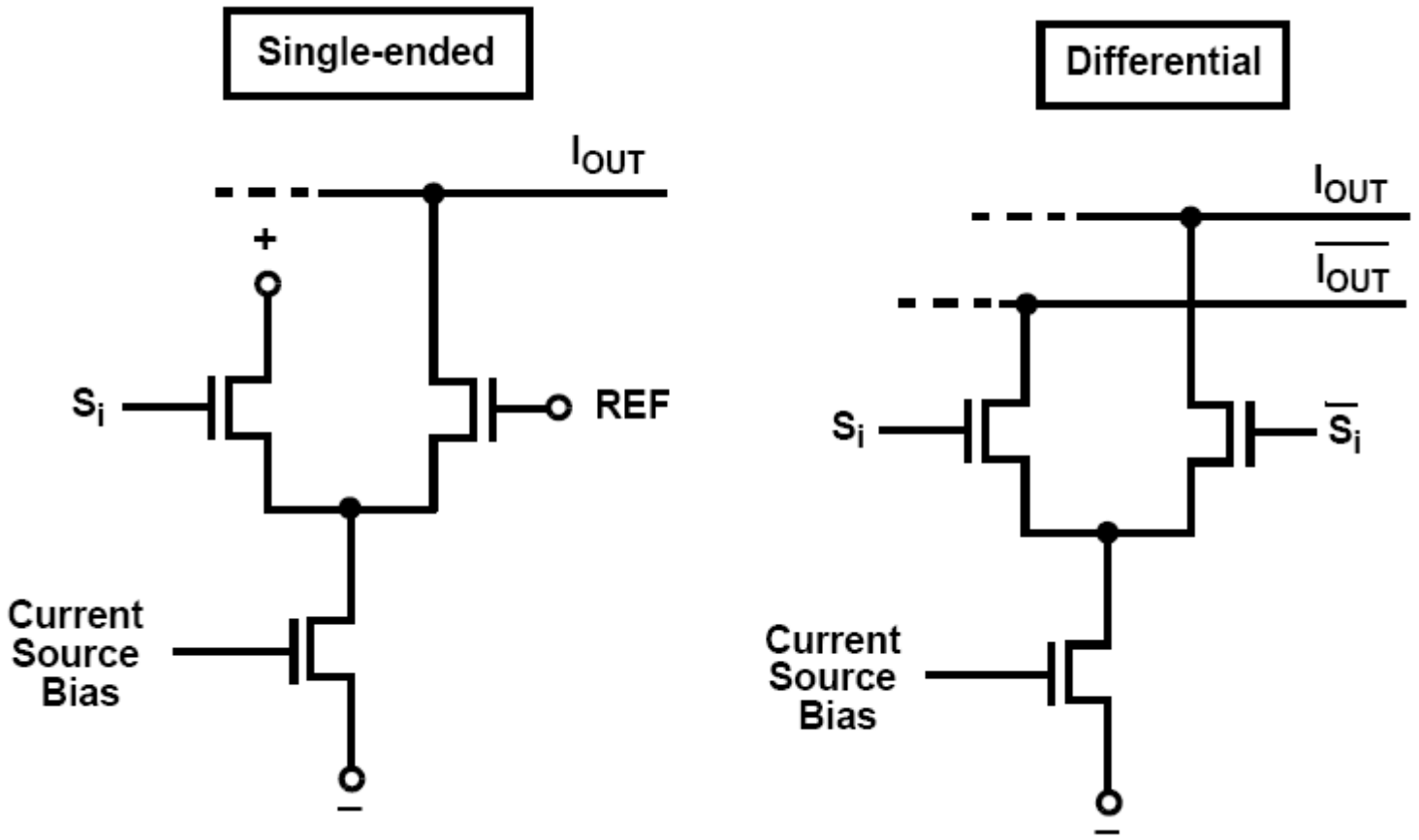
Common Centroid Layout Example

- Common centroid binary weighted array
- To cancel gradients
  - Process
  - IR drop
  - Timing



[Bastiaansen, Corne, et al. "A 10-bit 40 MHz 0.8 μm CMOS current-output D/A converter." *Solid-State Circuits Conference, 1990. ESSCIRC'90. Sixteenth European*. Vol. 1. IEEE, 1990.]
[M. Pelgrom, *Analog-to-Digital Conversion*, 3rd Ed.]

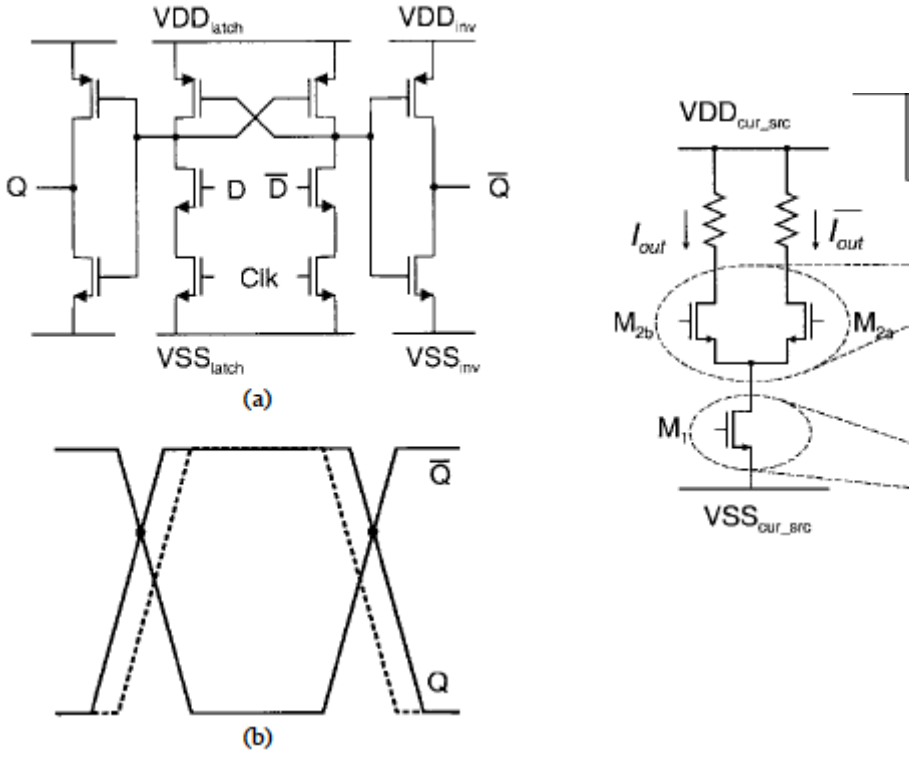
Basic Differential Pair Switch



Commonly Used Techniques

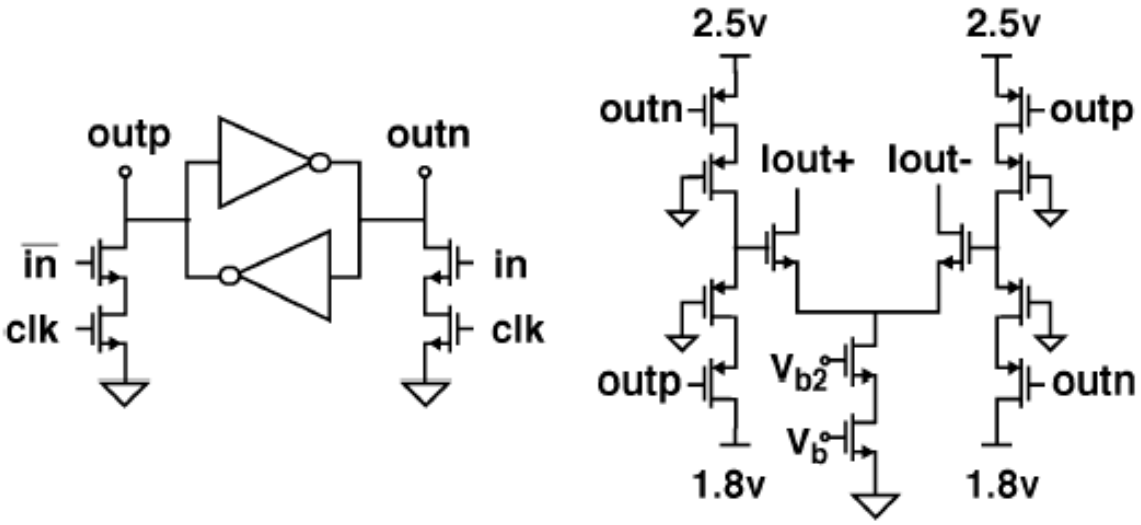
- Retiming
  - Latches in (or close to) each current cell
  - Latch controlled by global clock to ensure that current cells switch simultaneously (independent of decoder delays)
- Make before break
  - Ensure uninterrupted current flow, so that tail current source remains active
- Low swing driver
  - Drive differential pair with low swing to minimize coupling from control signals to output
- Cascoded tail current source for high output impedance
  - Ensures that overall impedance at output nodes is code independent (necessary for good INL)

Example Retiming Latch



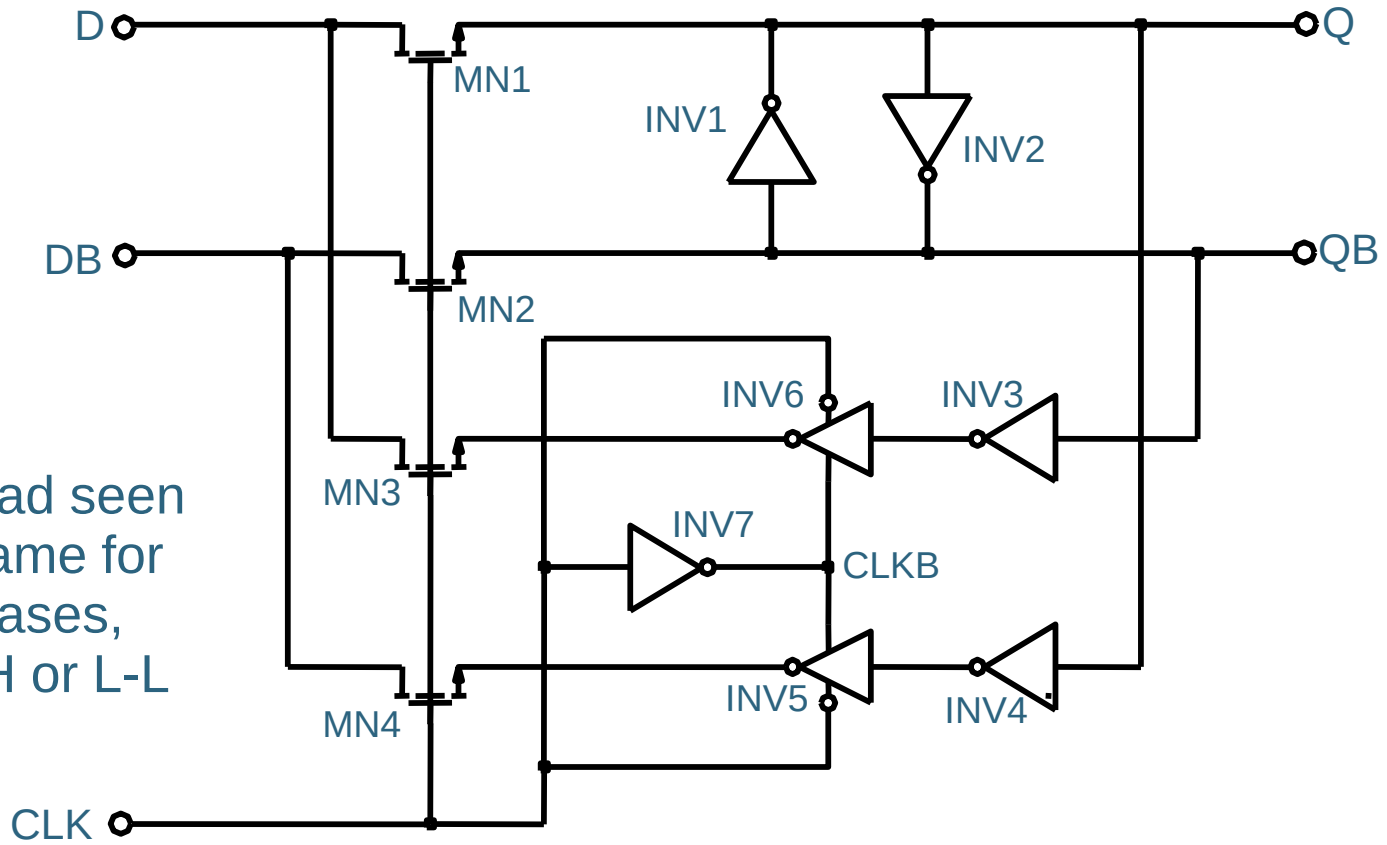
[Van der Plas, JSSC 12/99]

Example Current Cell Implementation



[Barkin & Wooley, JSSC 4/2004]

Constant Clock Load Latch



Capacitive load seen at CLK the same for all possible cases, H-L, L-H, H-H or L-L

Mercer, *US patent ,7,023,255 4/4/2006*