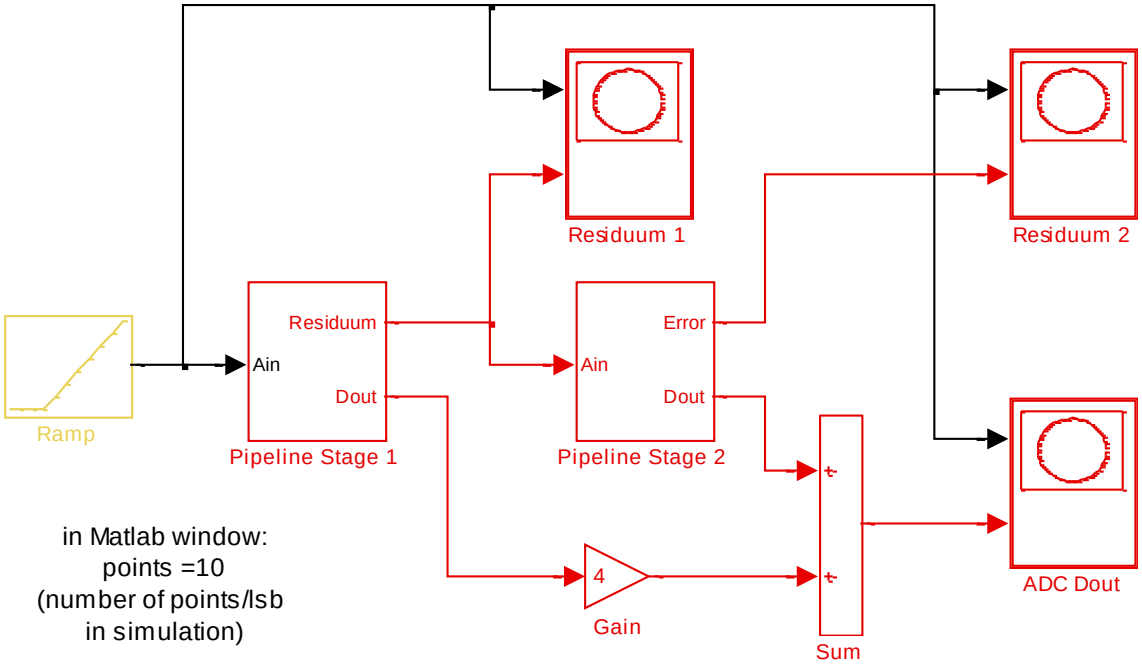
EE 240C
Analog-Digital Interface Integrated Circuits

Pipeline Design & Error Sources

Questions

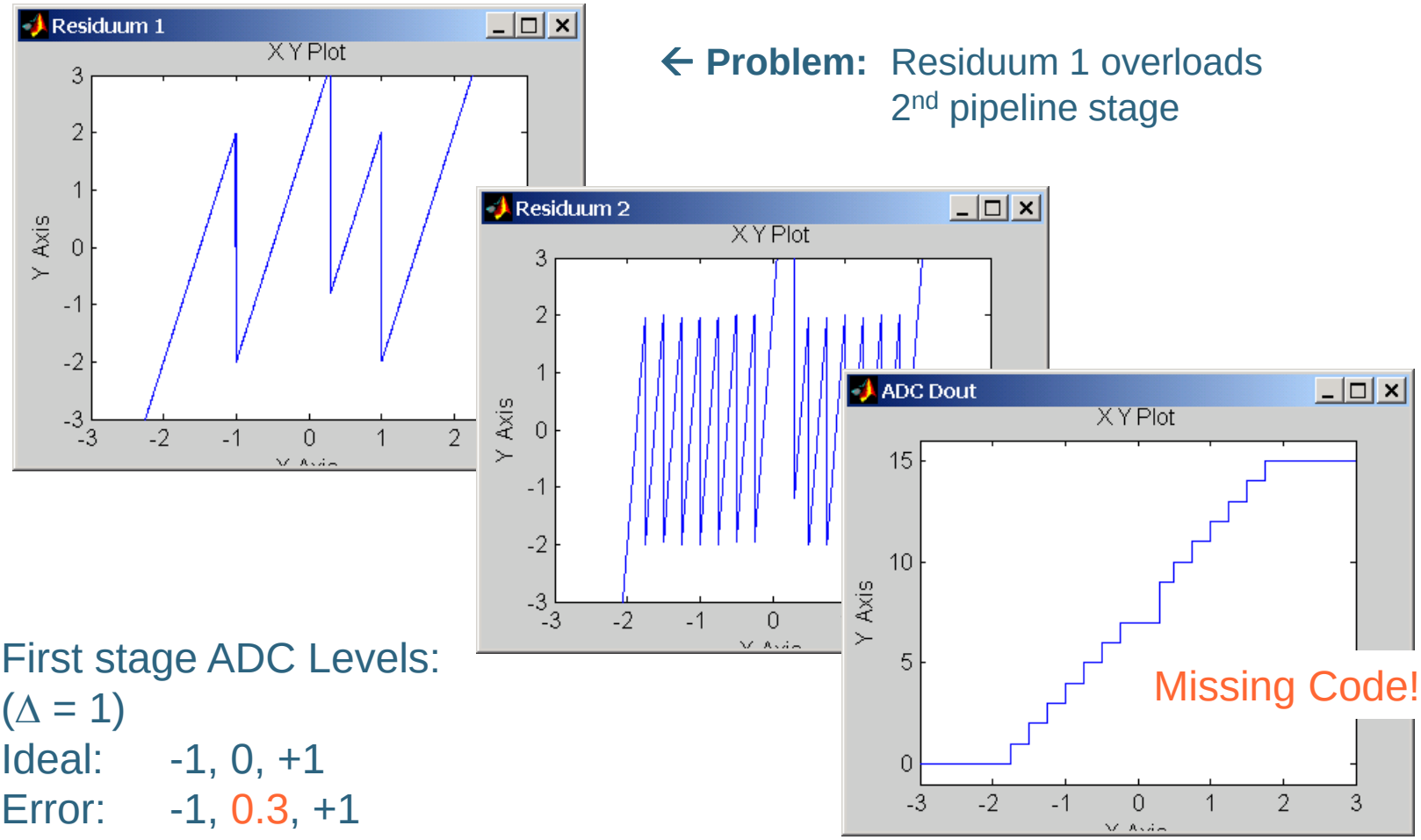
- How to pick stage gain G for a given sub-ADC resolution?
- Impact and compensation of nonidealities?
  - Sub-ADC errors
  - Amplifier offset
  - Amplifier gain error
  - Sub-DAC error
- Begin to explore these questions using a simple example
  - First stage with 2-bit sub-ADC, followed by 2-bit backend

Comparator Offset



See Matlab/Simulink L18_pipe_2bps_error.mdl

Comparator Offset

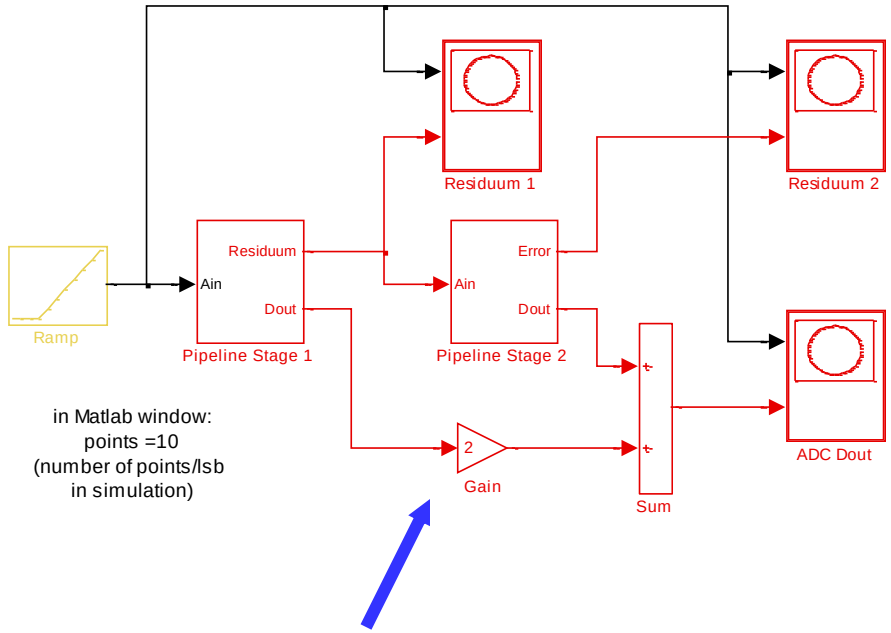


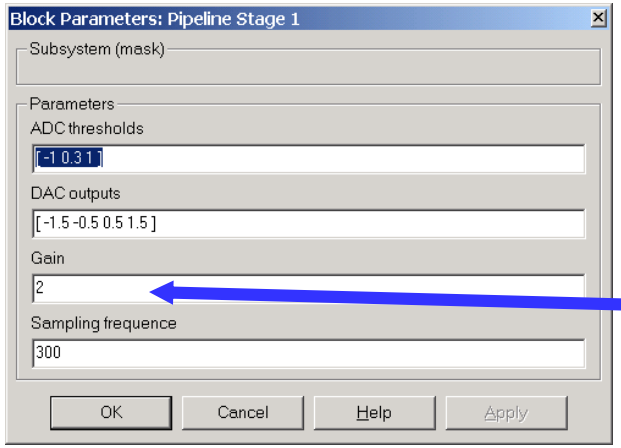
← **Problem:** Residuum 1 overloads 2nd pipeline stage

First stage ADC Levels:
($\Delta = 1$)
Ideal: -1, 0, +1
Error: -1, 0.3, +1

Digital Correction

Pipeline ADC, 2 bits per stage
Interstage gain = 2 for digital correction

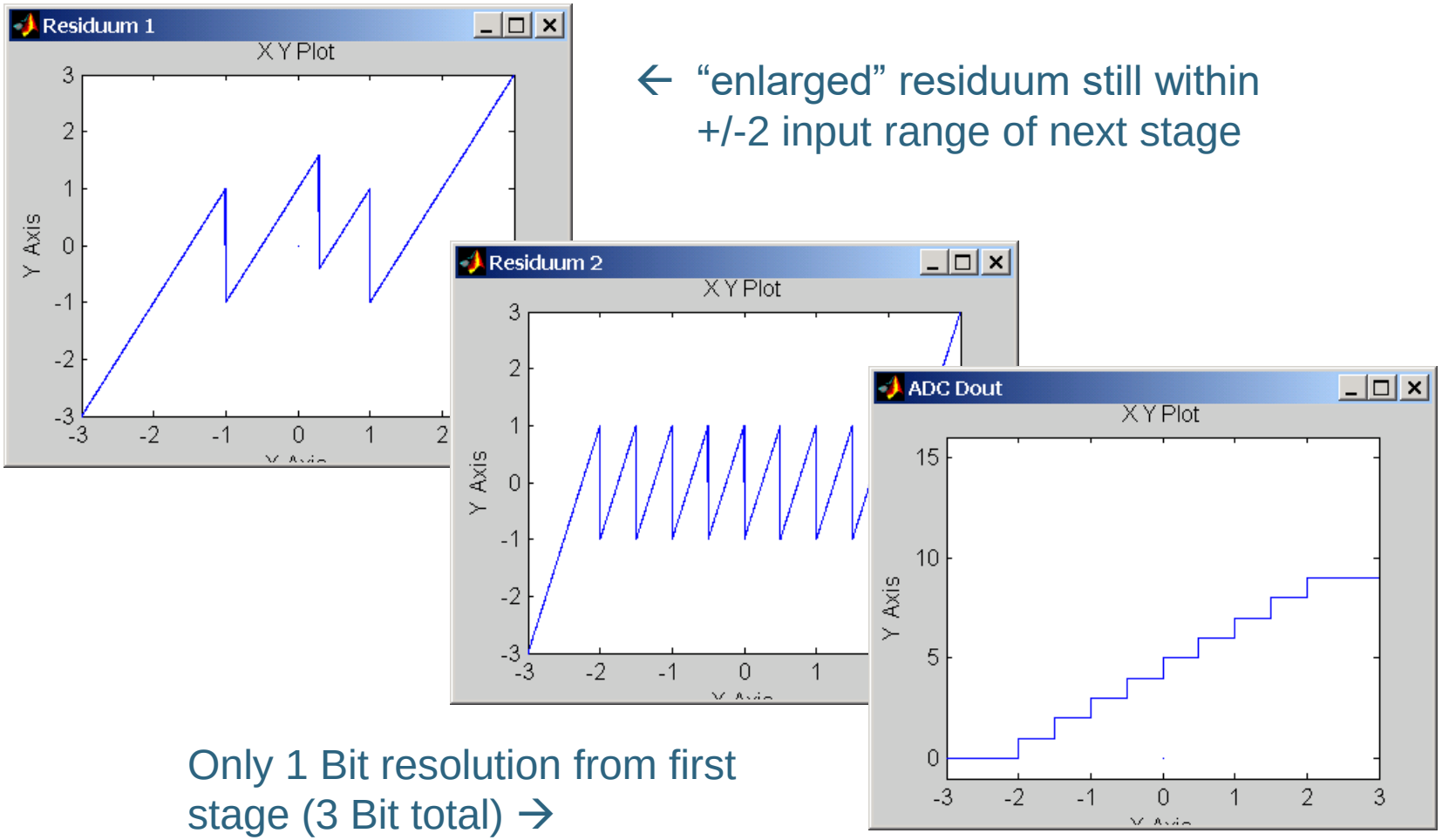




Reduced interstage gain:

- No overload (due to comparator offset)
- Reduced input (only 1 bit resolution per stage)

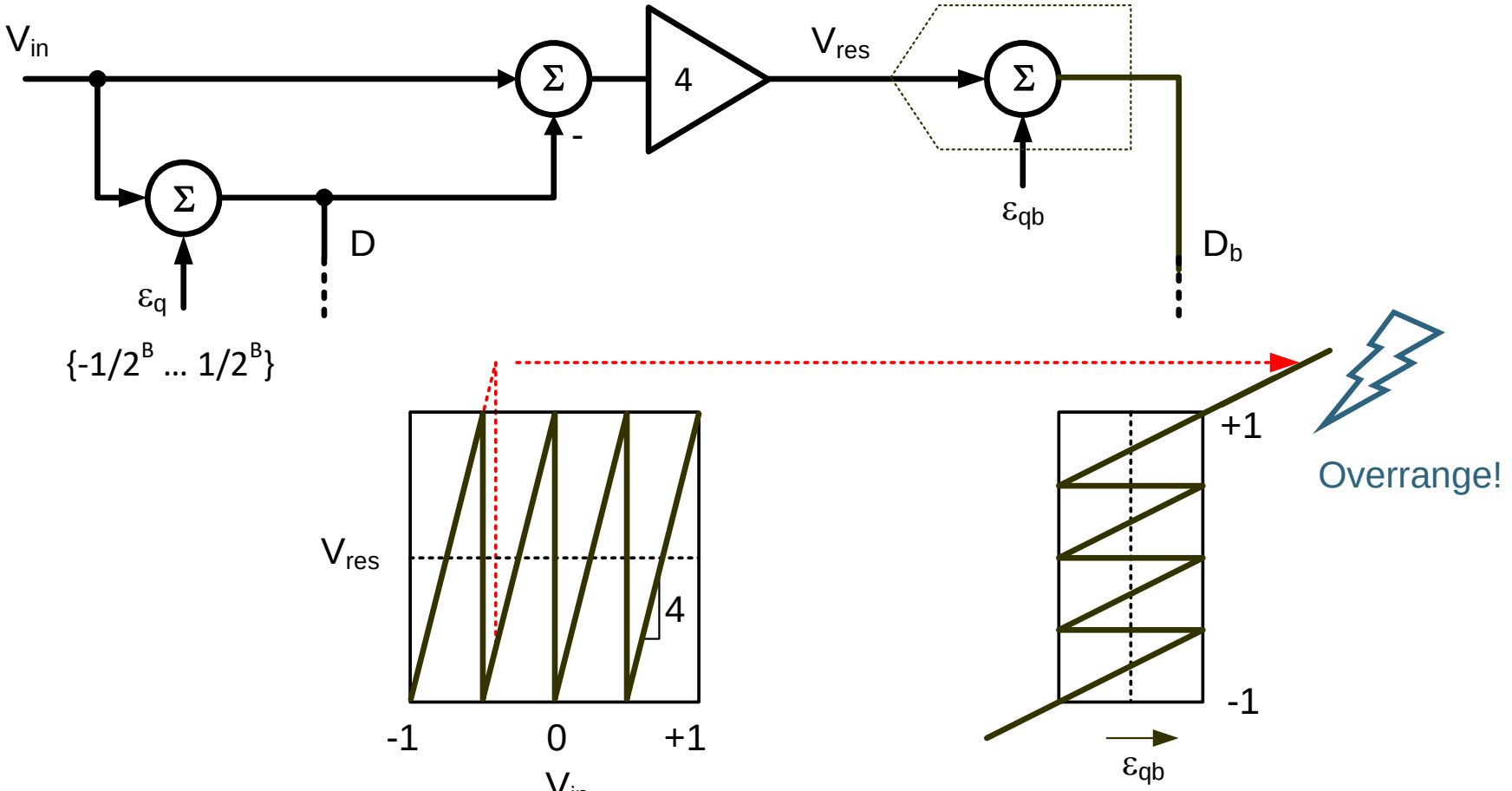
Digital Correction



← "enlarged" residuum still within +/-2 input range of next stage

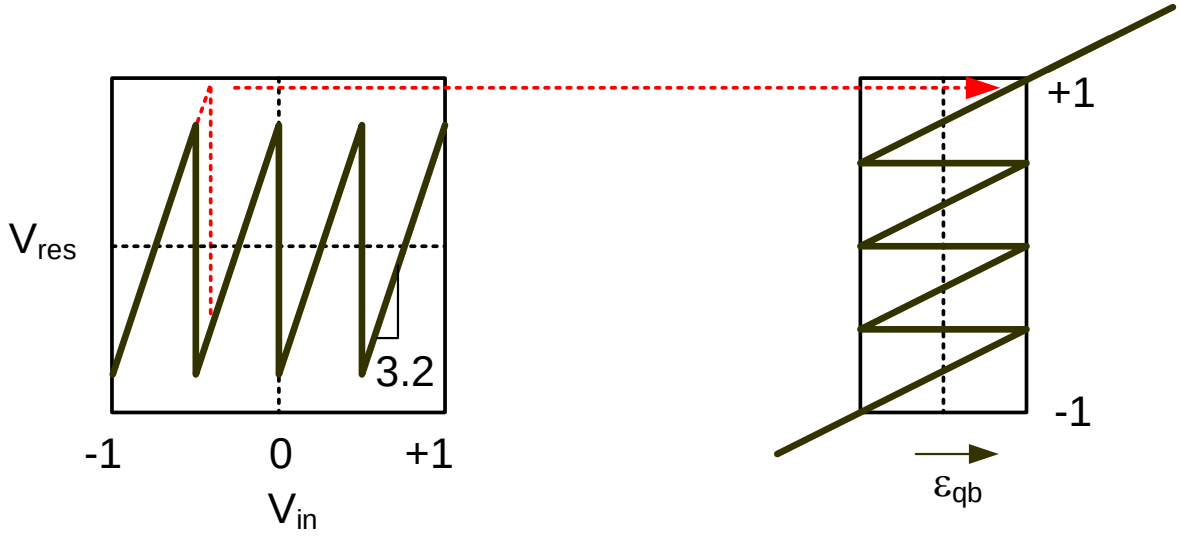
Only 1 Bit resolution from first stage (3 Bit total) →

Issue with $G=2^B$



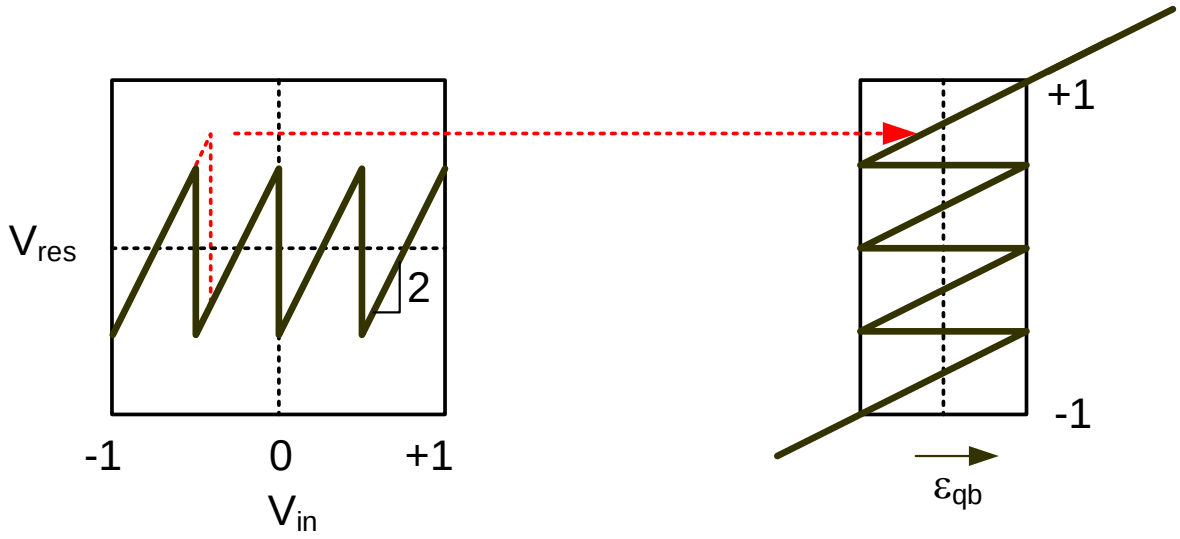
- Any error in sub-ADC decision levels will overload backend ADC and thereby deteriorate ADC transfer function

Idea #1: G slightly less than 2^B



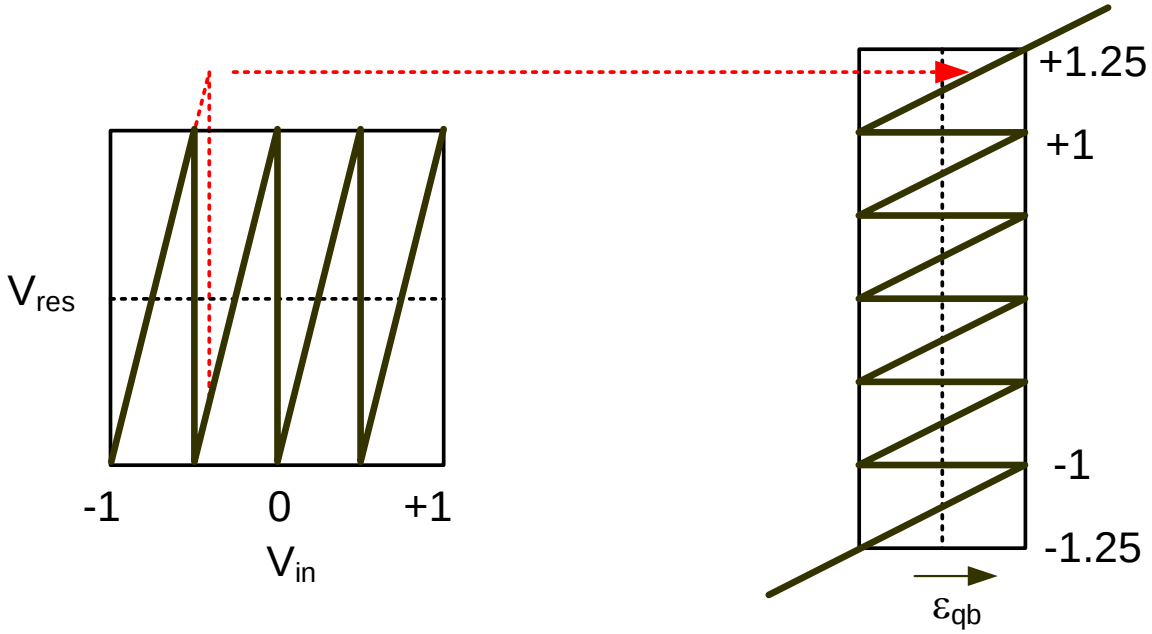
- Effective stage resolution can be non-integer ($R=\log_2 G$)
  - E.g. $R = \log_2 3.2 = 1.68$ bits
- See e.g. [Karanicolas 1993]

Idea #2: G < 2^B, but Power of Two



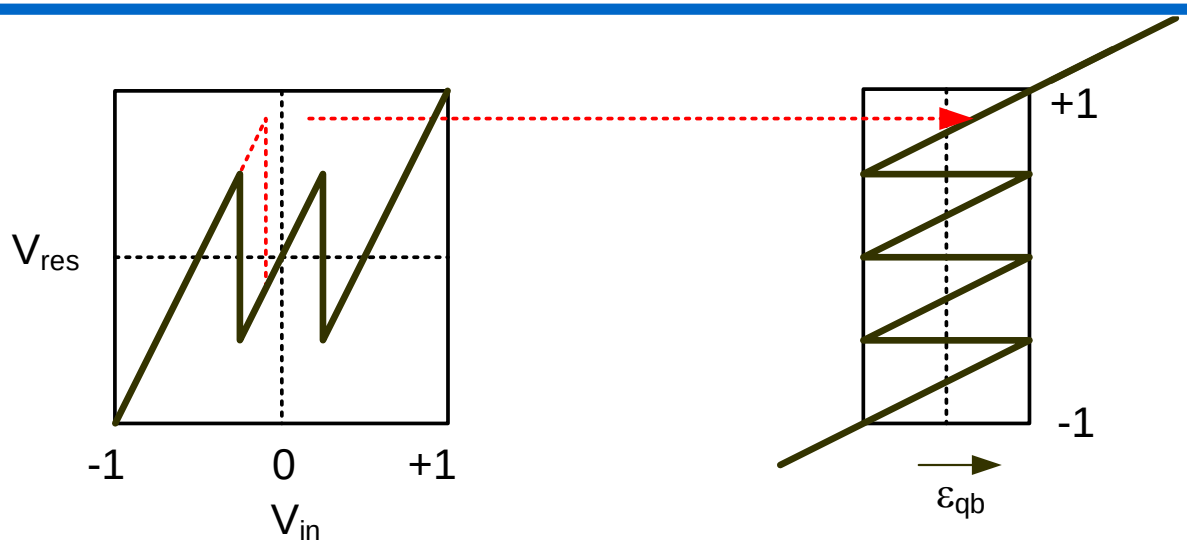
- Effective stage resolution is an integer
  - E.g. $R = \log_2 2 = 1 = B-1$
  - Digital hardware requires only a few adders, no need to implement fractional weights
- See e.g. [Mehr 2000]

Idea #3: G=2^B, Extended Backend Range



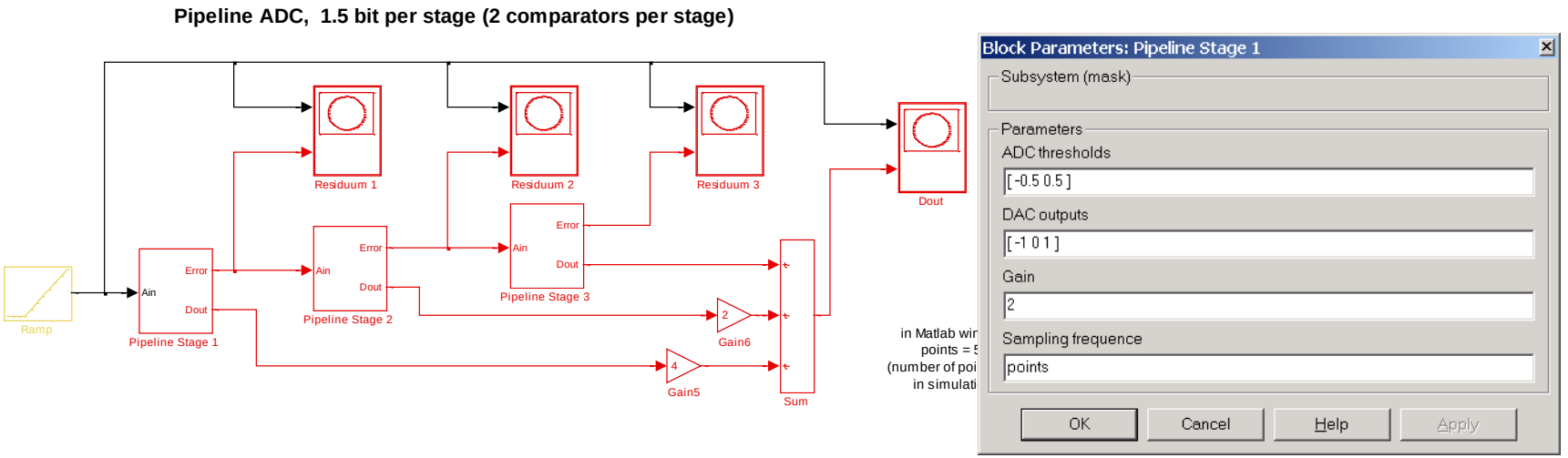
- No redundancy in stage with errors
- Extra decision levels in succeeding stage used to bring residue "back into the box"
- See e.g. [Opris 1998]

Variant of Idea #2: "1.5-bit stage"



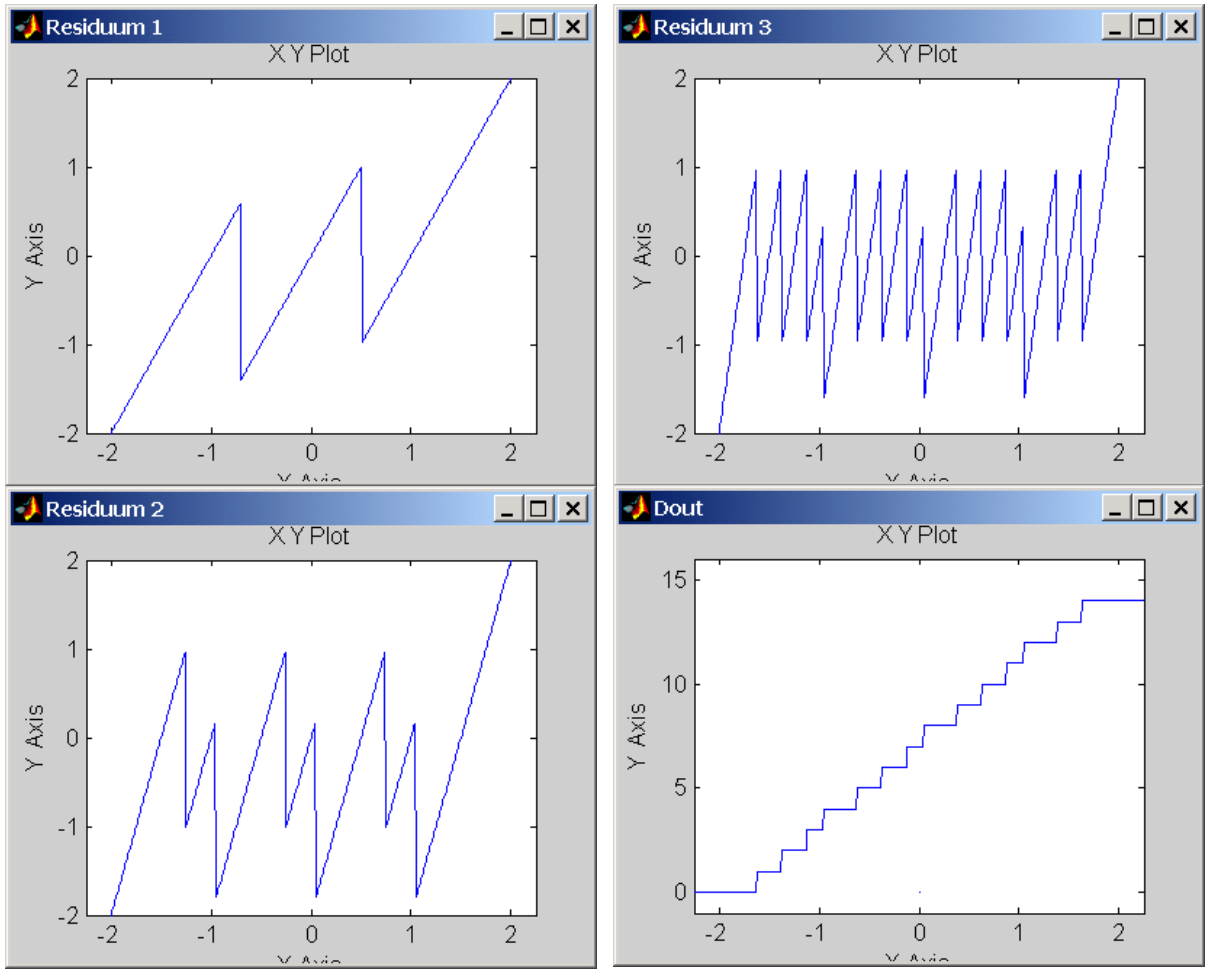
- Sub-ADC decision levels placed to minimize comparator count
- Can accommodate errors up to ±¼
- B = $\log_2(2+1)$ = 1.589 (sub-ADC resolution)
- R = $\log_2 2$ = 1 (effective stage resolution)
- See e.g. [Lewis 1992]

“1.5-bps” Stage



- A full bit of “overrange” is excessive for typical comparator offset
  - → use only 2 (rather than 3) comparators and G=2
- 3 DAC levels → lb(3) = 1.585 Bits
- Overall resolution:
  - 1 bps for all stages but last
  - 1.585 Bit for last

1.5-bps Pipeline



- What is the maximum offset that can be corrected?
- What is the offset of each comparator in this example?

Ref: S. Lewis et al, "A 10-b 20-Msample/s Analog-to-Digital Converter," J. Solid-State Circ., pp. 351-8, March 1992.

Summary on Sub-ADC Redundancy

- We can tolerate sub-ADC errors as long as
  - The residue stays "inside the box", or
  - Another stage downstream returns the residue "into the box" before it gets clipped or reaches the last quantizer
- This result applies to any stage in an n-stage pipeline
  - Can always decompose pipeline into single stage + backend ADC
- In literature, sub-ADC redundancy schemes are often called "digital correction"
- There is no explicit error correction!
  - Sub-ADC errors are absorbed in the same way as their inherent quantization error
    - Provided there is no clipping …

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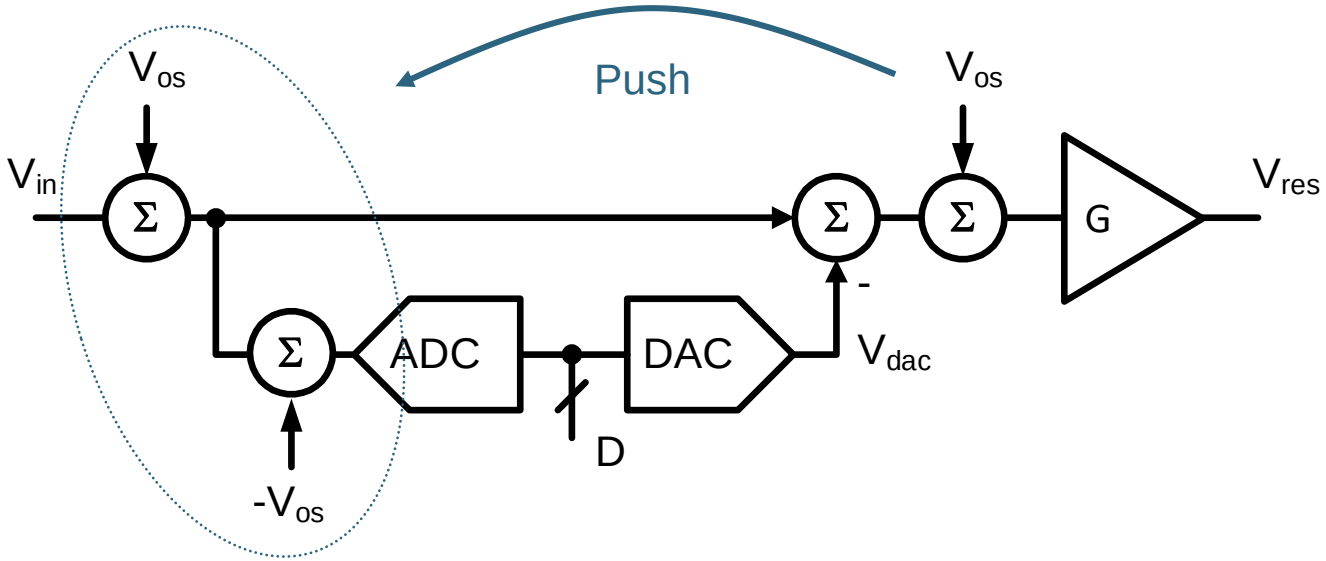
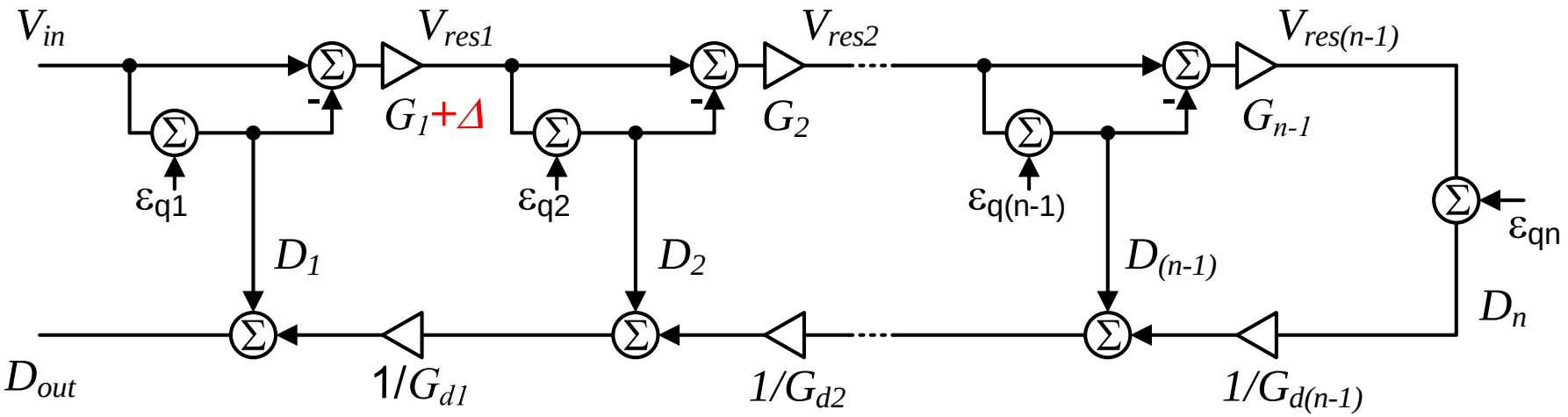
Pipeline Amplifier Errors

Amplifier Offset



- Amplifier offset can be referred toward stage input and results in
  - Global offset
    - Usually no problem, unless "absolute ADC accuracy" is required
  - Sub-ADC offset
    - Easily accommodated through redundancy

Gain Errors



$$D_{out} = V_{in} + \varepsilon_{q1}\left(1 - \frac{G_1 + \Delta}{G_{d1}}\right) + \ldots + \frac{\varepsilon_{qn}}{\prod_{j=1}^{n-1} G_{dj}}$$

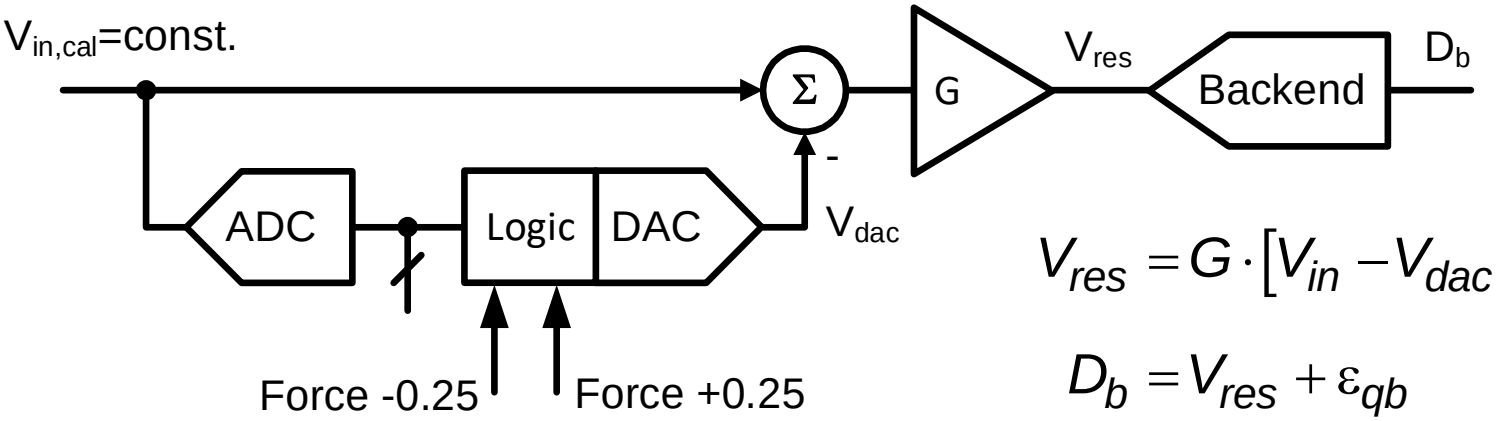
- Want to make $G_{d1} = G_1 + \Delta$

Digital Gain Calibration (1)

- Error in analog gain is not a problem as long as "digital gain term" is adjusted appropriately
- Problem
  - Need to measure analog gain precisely
- Example
  - Digital calibration of a 1-bit first stage with 1-bit redundancy (R=1, B=2)

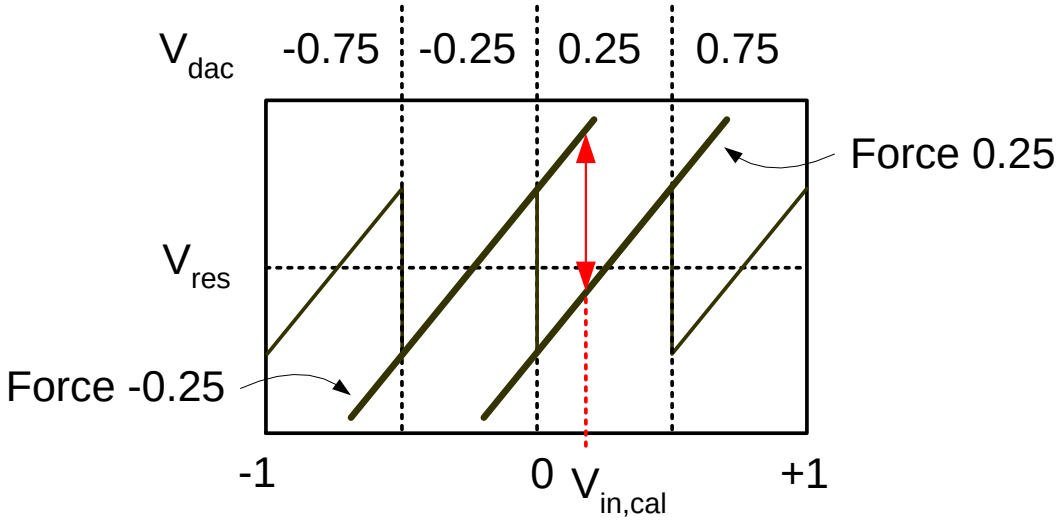
- Note
  - Even if all G_{dj} are perfectly adjusted to reflect the analog gains, the ADC will have non-zero DNL and INL, bounded by ±0.5LSB. This can be explained by the fact that the residue transitions may not correspond to integer multiples of the backend-LSB. This can cause non-uniformity in the ADC transfer function (DNL, INL) and also non-monotonicity (see [Markus, 2005]).
  - In case this cannot be tolerated
    - Add redundant bits to ADC backend (after combining all bits, final result can be truncated back), or
    - Calibrate analog gain terms

Digital Gain Calibration (2)



$$V_{res} = G \cdot [V_{in} - V_{dac}]$$

$$D_b = V_{res} + \varepsilon_{qb}$$



Digital Gain Calibration (3)

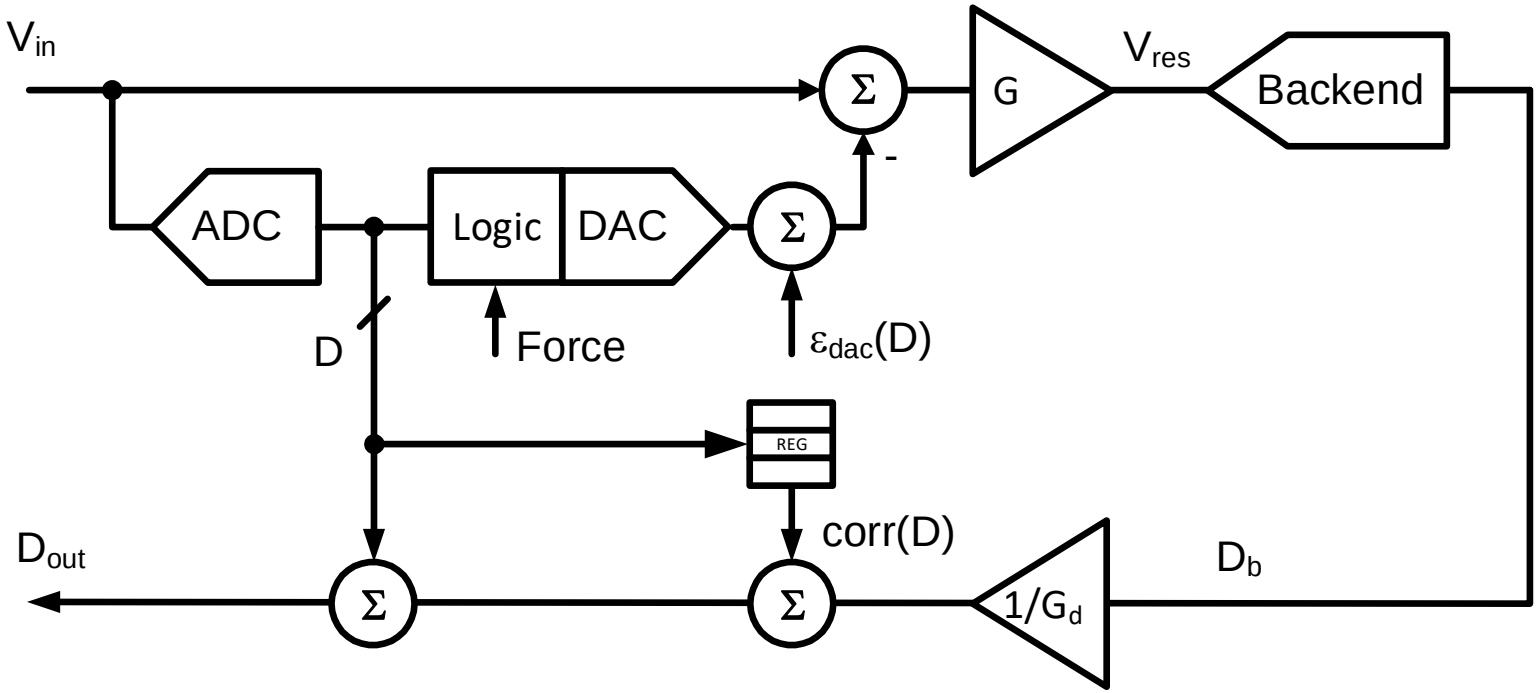
Step1: $$D_b^{(1)} = G \cdot [V_{in} + 0.25] + \varepsilon_{qb}^{(1)}$$

Step2: $$D_b^{(2)} = G \cdot [V_{in} - 0.25] + \varepsilon_{qb}^{(2)}$$

$$D_b^{(1)} - D_b^{(2)} = 0.5 \cdot G + \varepsilon_{qb}^{(1)} - \varepsilon_{qb}^{(2)}$$

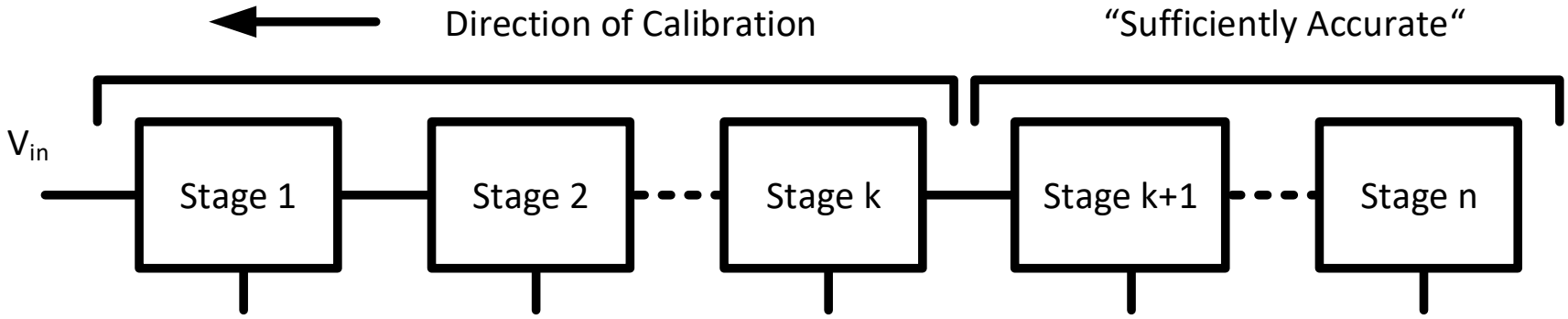
- Can minimize impact of quantization error using
  - Averaging (thermal noise dither)
  - Extra backend resolution

DAC Calibration



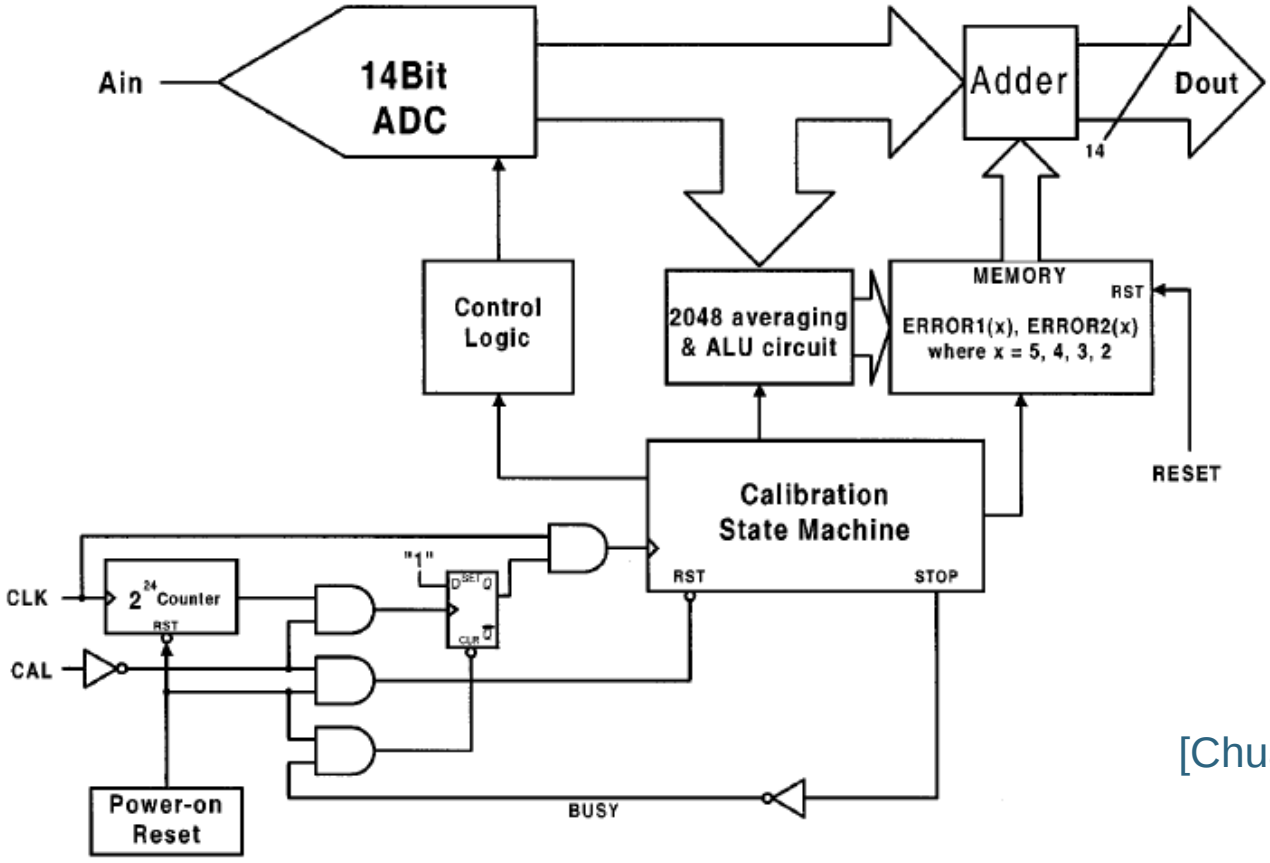
- Essentially same concept as gain calibration
  - Step through DAC codes and use backend to measure errors
- Store coefficients for each DAC transition in a look-up table

Recursive Stage Calibration



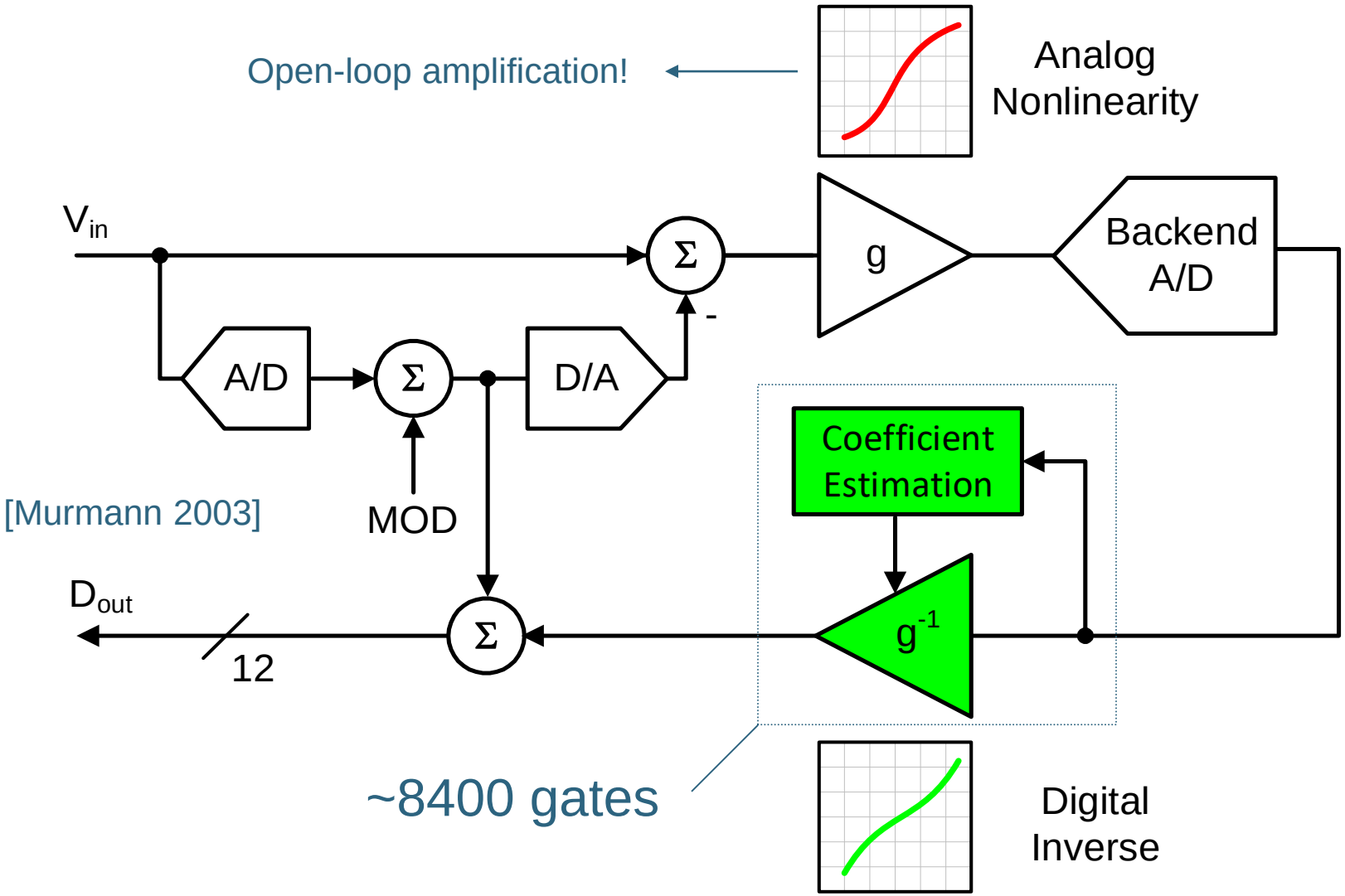
- First few stages have most stringent accuracy requirements
  - Errors of later stages are attenuated by aggregate gain
- Commonly used algorithm [Karanicolas 1993]
  - Take ADC offline
  - Measure least significant stage that needs calibration first
  - Move to next significant stage and continue toward stage 1

Calibration Hardware Example



[Chuang 2002]

Non-Linear Gain Calibration



Alternative Schemes

- Other foreground calibration schemes
  - Calibrate ADC starting from first stage [Singer 2000]
  - Connect stages in a circular loop [Soenen 1995]
- Background calibration
  - See e.g. [Ming 2001]
  - Makes sense primarily when calibration parameters are expected to drift
    - Capacitor ratios do not drift!
    - Background calibration is justifiable e.g. when drift in OTA open-loop gain is an issue

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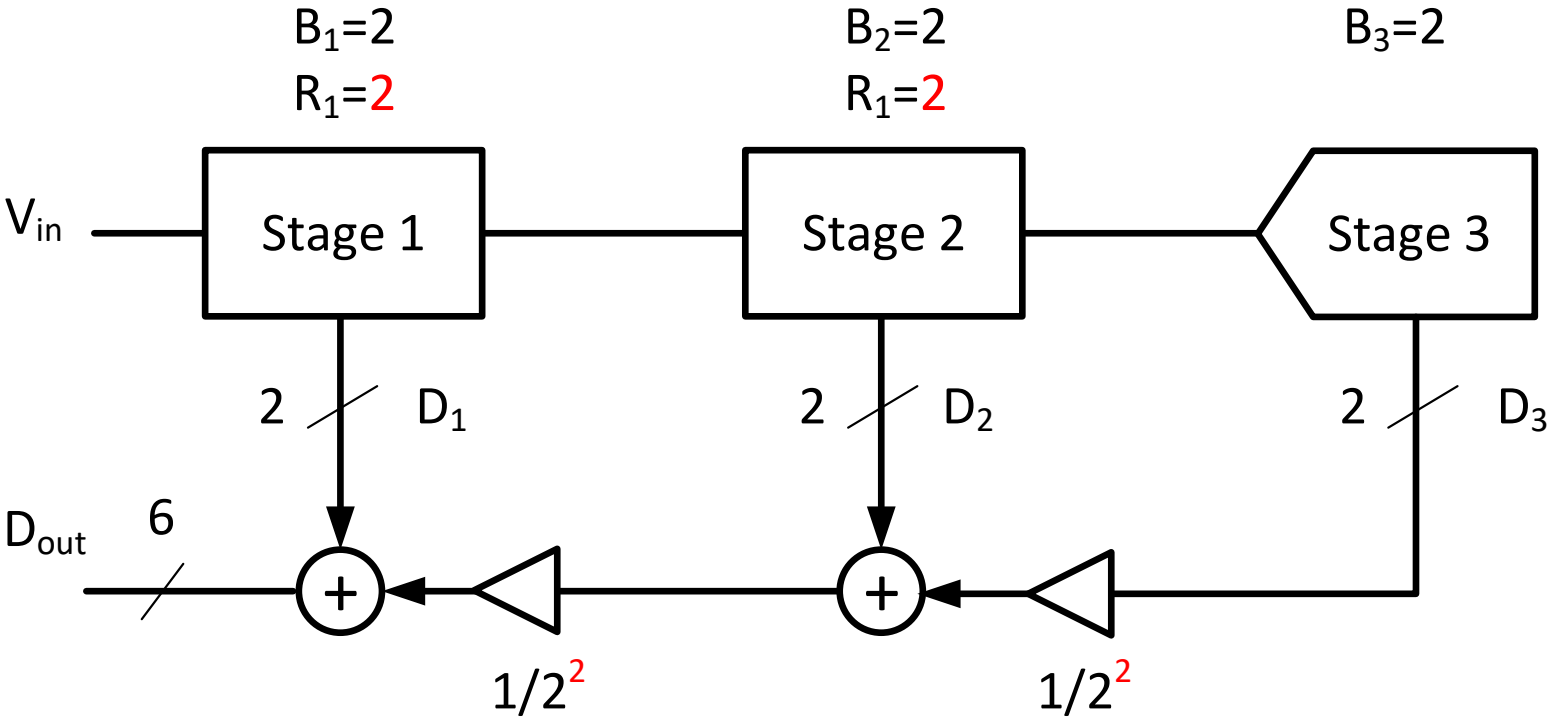
Pipeline Digital Backend

Combining the Bits (1)

- Example1: Three 2-bit stages, no redundancy

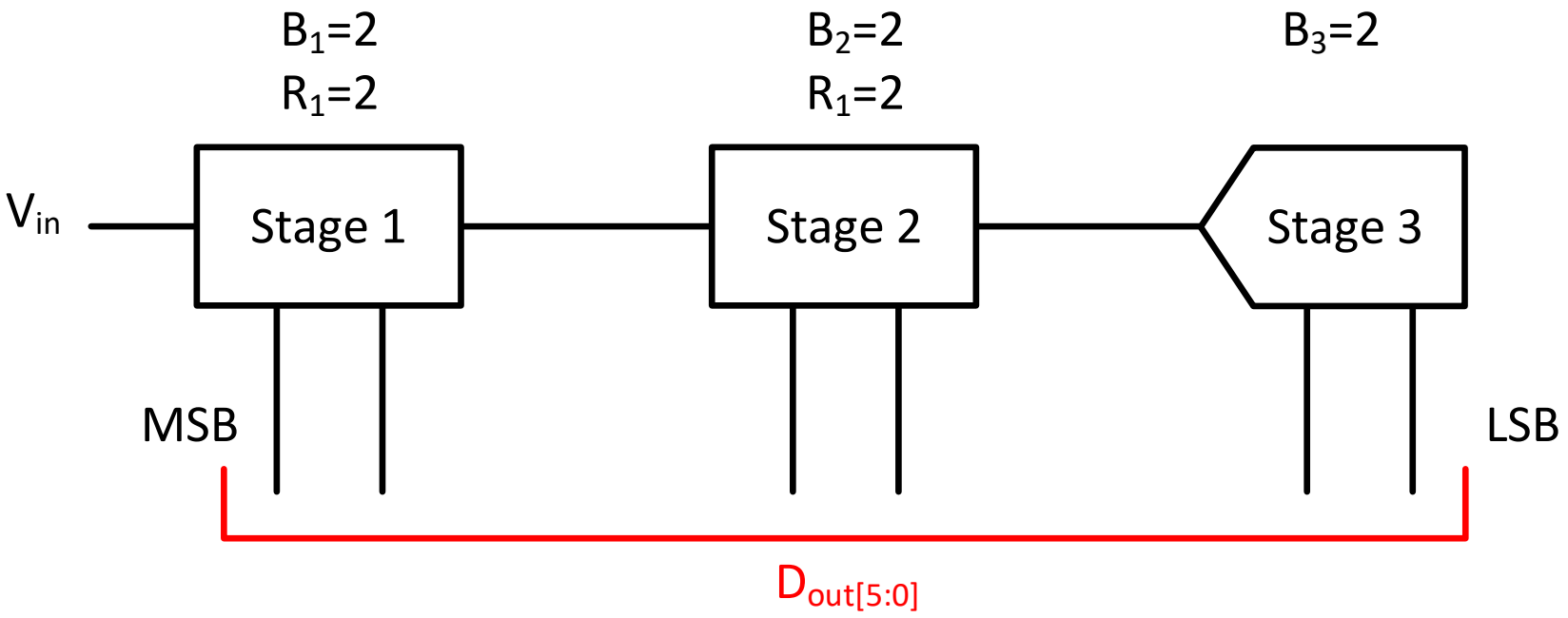


$$D_{out} = D_1 + \frac{1}{4}D_2 + \frac{1}{16}D_3$$

Combining the Bits (2)

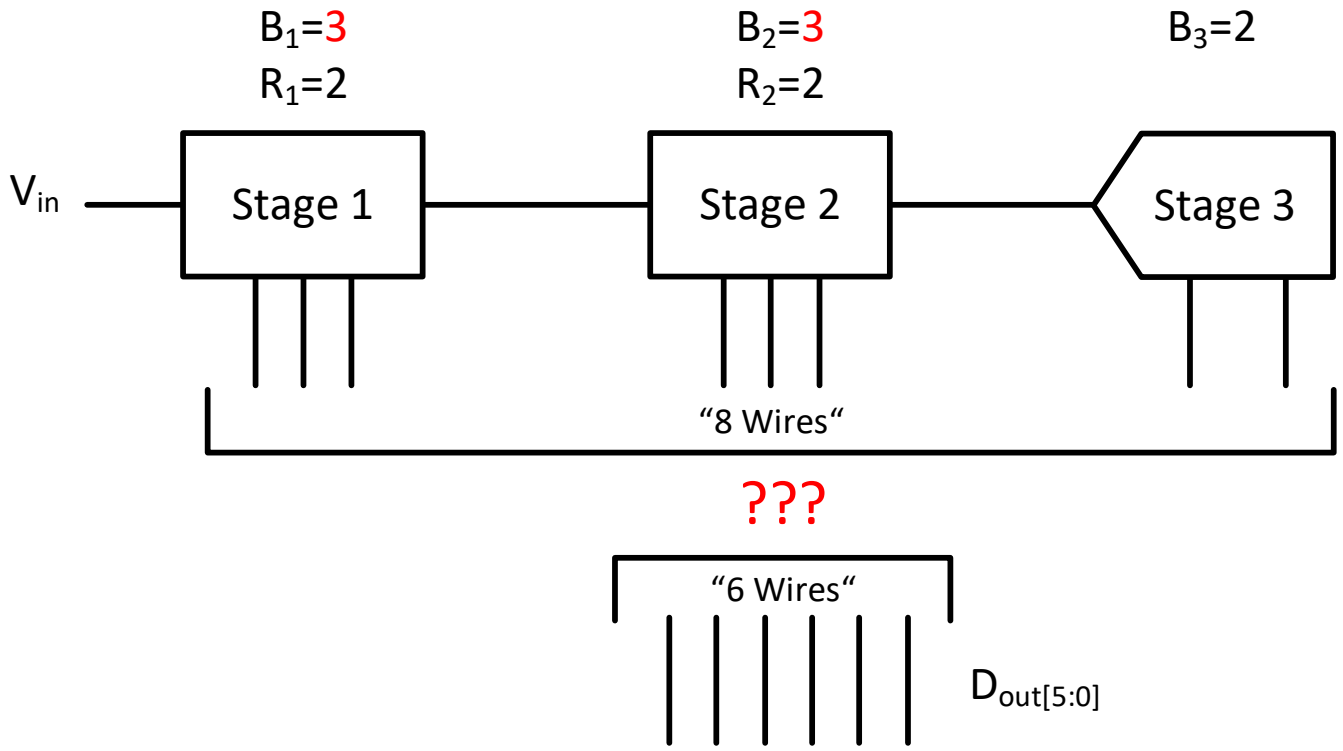
```
D1      XX
D2        XX
D3          XX
------------
Dout    DDDDDD
```

- Only bit shifts
- No arithmetic circuits needed



Combining the Bits (3)

- Example2: Three 2-bit stages, one bit redundancy in stages 1 and 2 (6-bit aggregate ADC resolution)

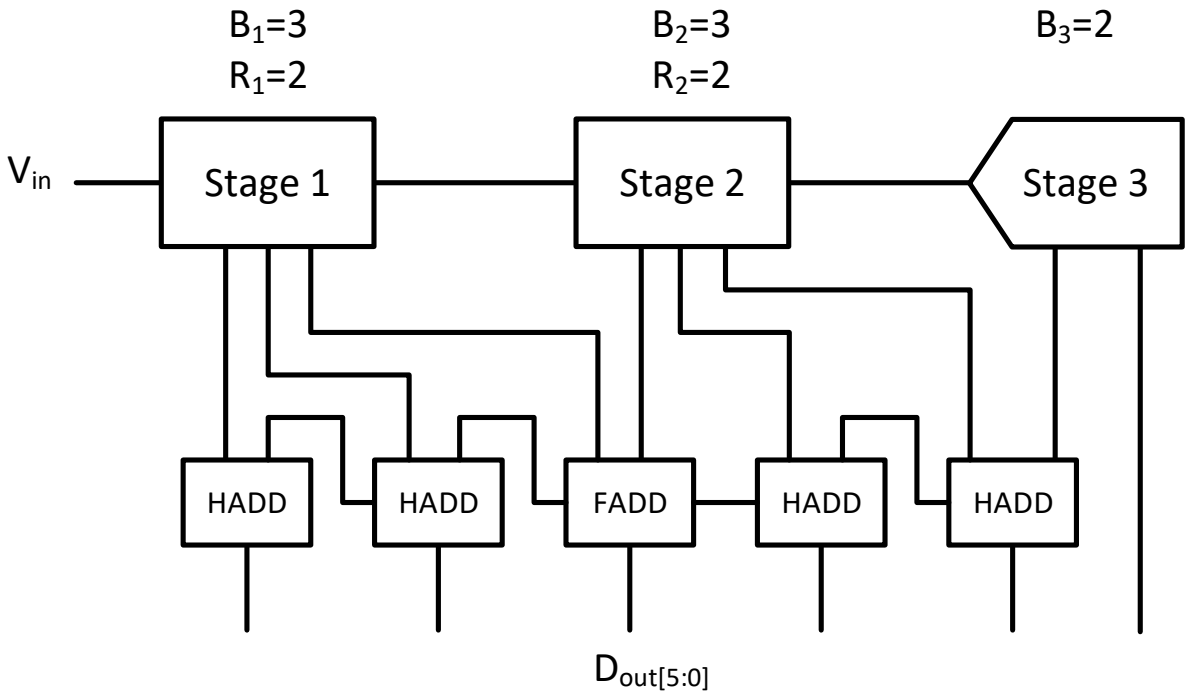


Combining the Bits (4)

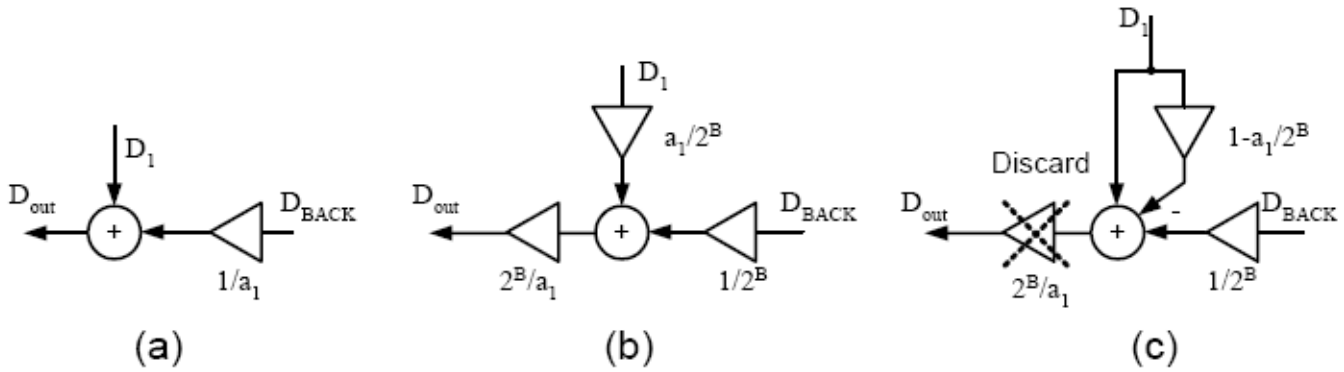
$$D_{out} = D_1 + \frac{1}{4}D_2 + \frac{1}{16}D_3$$

```
D1      XXX
D2        XXX
D3          XX
------------
Dout    DDDDDD
```

- Bits overlap
- Need adders



Combining the Bits (5)



- For fractional weights (e.g. radix <2), there is no need to implement complex multipliers
- Can still use simple bit shifts; push actual multiplication into low-resolution output
  - E.g. a 1x10 bit multiplication needs only one adder…
- See e.g. [Karanicolas 1993]

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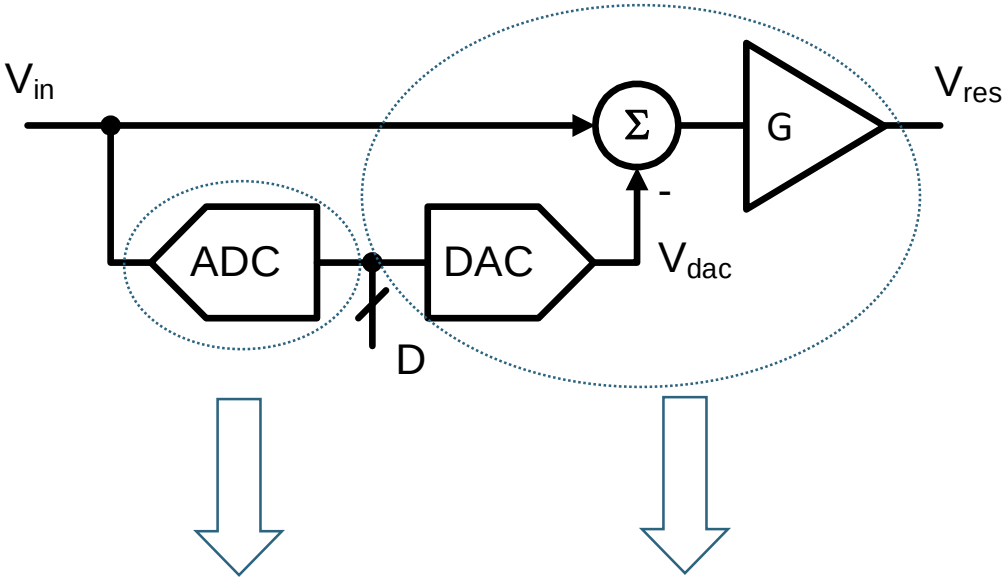
Pipeline Implementation Considerations

Outline

- Background
  - History and state-of the art performance
  - General idea of multi-step A/D conversion
- Pipeline ADC basics
  - Ideal block diagram and operation, impact of block nonidealities
- Ways to deal with nonidealities
  - Redundancy, calibration
- CMOS implementation details
  - Stage scaling, MDAC design
- Architectural options
  - OTA sharing, SHA-less front-end
- Research topics

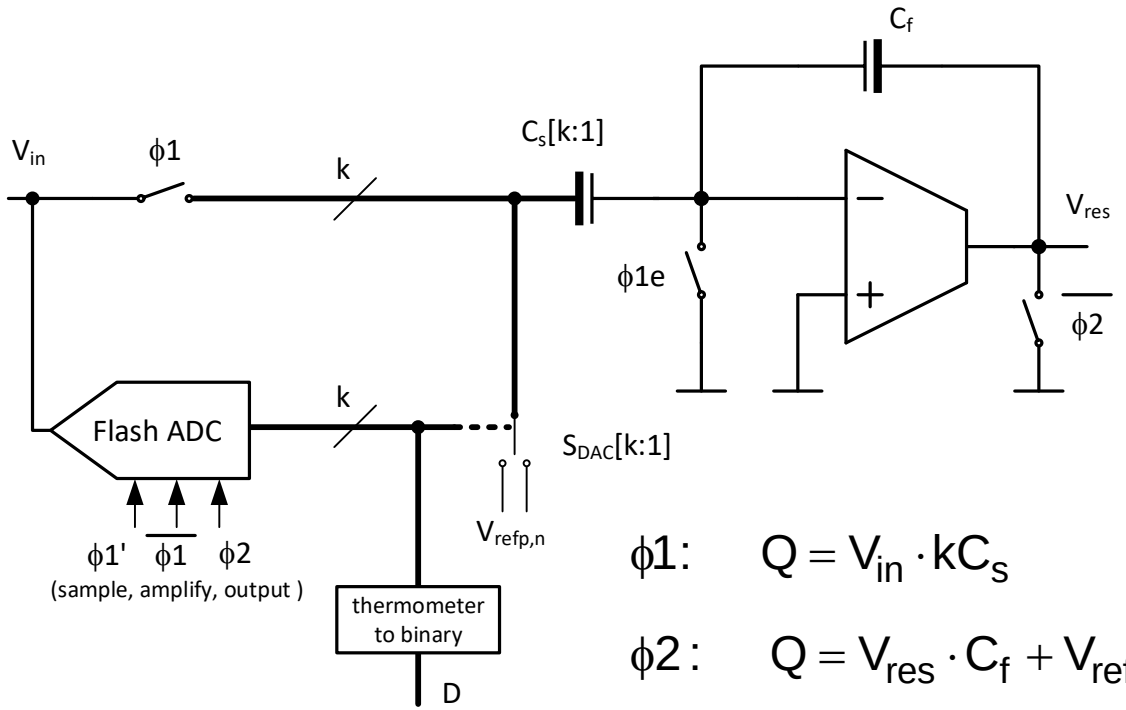
Stage Implementation



Flash ADC

"MDAC" Switched-Capacitor Circuit

Generic Circuit



$$\phi 1: \quad Q = V_{in} \cdot kC_s$$

$$\phi 2: \quad Q = V_{res} \cdot C_f + V_{refp} \cdot mC_s + V_{refn} \cdot (k-m)C_s$$

$$\therefore -V_{res} = \frac{kC_s}{C_f} V_{in} - \frac{mC_s}{C_f} V_{refp} + \frac{(k-m)C_s}{C_f} V_{refn}$$

$$= G \cdot (V_{in} - V_{dac})$$

Endless List of Design Parameters

- Stage resolution, stage scaling factor
- Stage redundancy
- Thermal noise/quantization noise ratio
- OTA architecture
  - OTA sharing?
- Switch topologies
- Comparator architecture
- Front-end SHA vs. SHA-less design
- Calibration approach (if needed)
- Technology and technology options (e.g. capacitors)

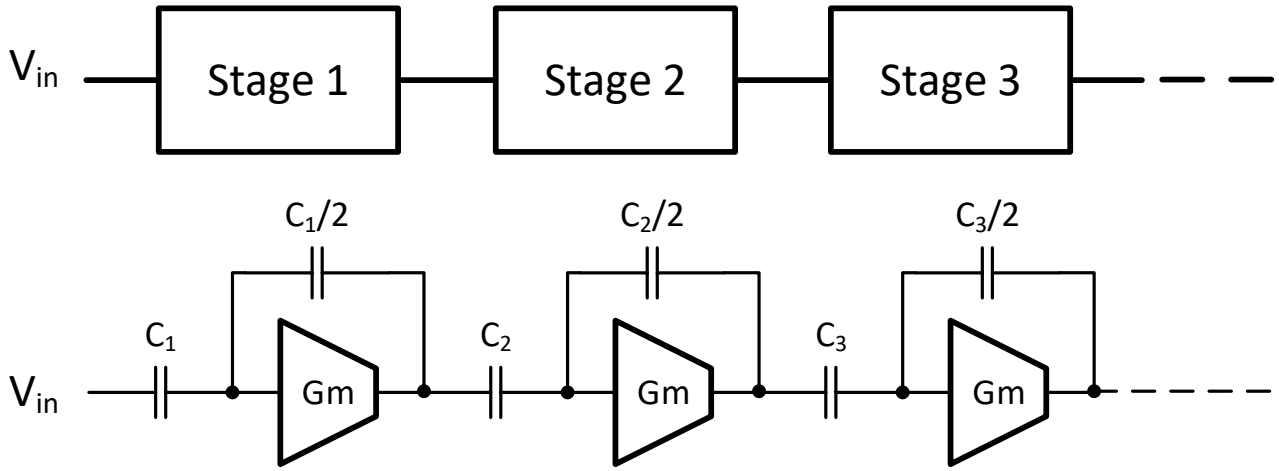
➢ A very complex optimization problem!

Thermal Noise Considerations

- Total input referred noise
  - Thermal noise + quantization noise
  - Costly to make thermal noise smaller than quantization noise
- Example: V_{FS}=1V, 10-bit ADC
  - $N_{quant}=LSB^2/12=(1V/2^{10})^2/12=(280\mu Vrms)^2$
  - Design for total input referred thermal noise ~280μVrms or larger, if SNR target allows
- Total input referred thermal noise is the sum of noise in all stages
  - How should we distribute the total thermal noise budget among the stages?
  - Let's look at an example…

Stage Scaling (1)

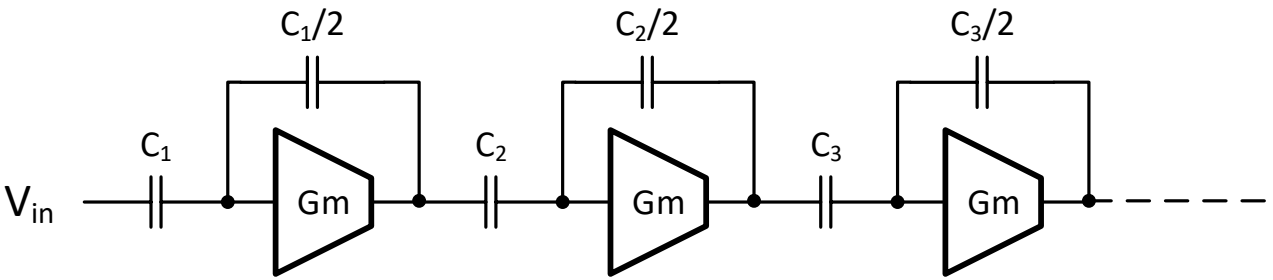
- Example: Pipeline using 1-bit (effective) stages (G=2)



- Total input referred noise power

$$N_{tot} \propto kT\left[\frac{1}{C_1}+\frac{1}{4C_2}+\frac{1}{16C_3}+\ldots\right]$$

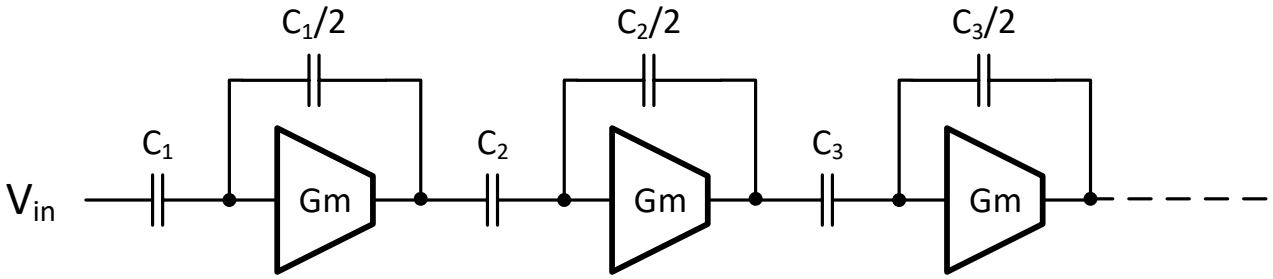
Stage Scaling (2)



$$N_{tot} \propto kT\left[\frac{1}{C_1}+\frac{1}{4C_2}+\frac{1}{16C_3}+\ldots\right]$$

- If we make all caps the same size, backend stages contribute very little noise
- Wasteful, because Power ~ G_m ~ C

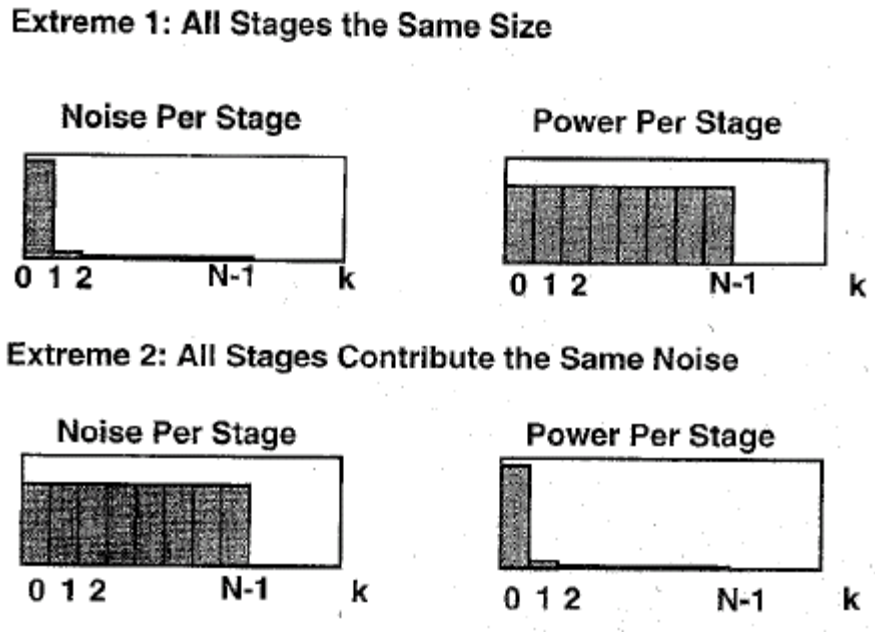
Stage Scaling (3)



$$N_{tot} \propto kT\left[\frac{1}{C_1}+\frac{1}{4C_2}+\frac{1}{16C_3}+\ldots\right]$$

- How about scaling caps down by 2^2=4x per stage?
  - Same amount of noise from every stage
  - All stages contribute significant noise
  - Noise from first few stages must be reduced
  - Power ~ G_m ~ C goes up!

Stage Scaling (4)

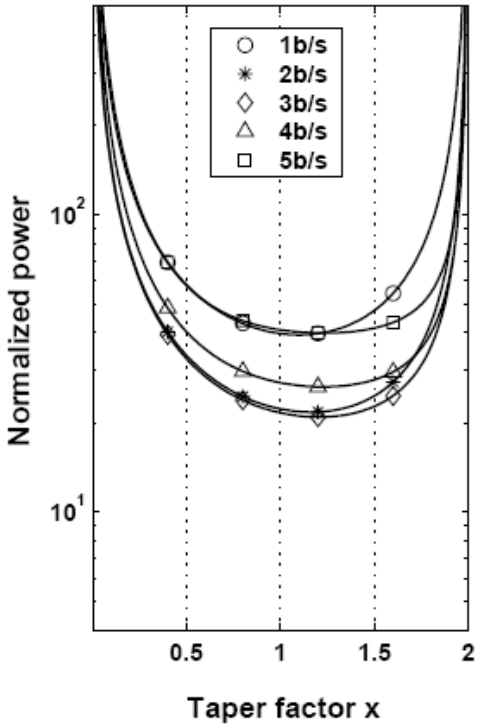


[Cline 1996]

- Optimum capacitior scaling lies approximately midway between these two extremes

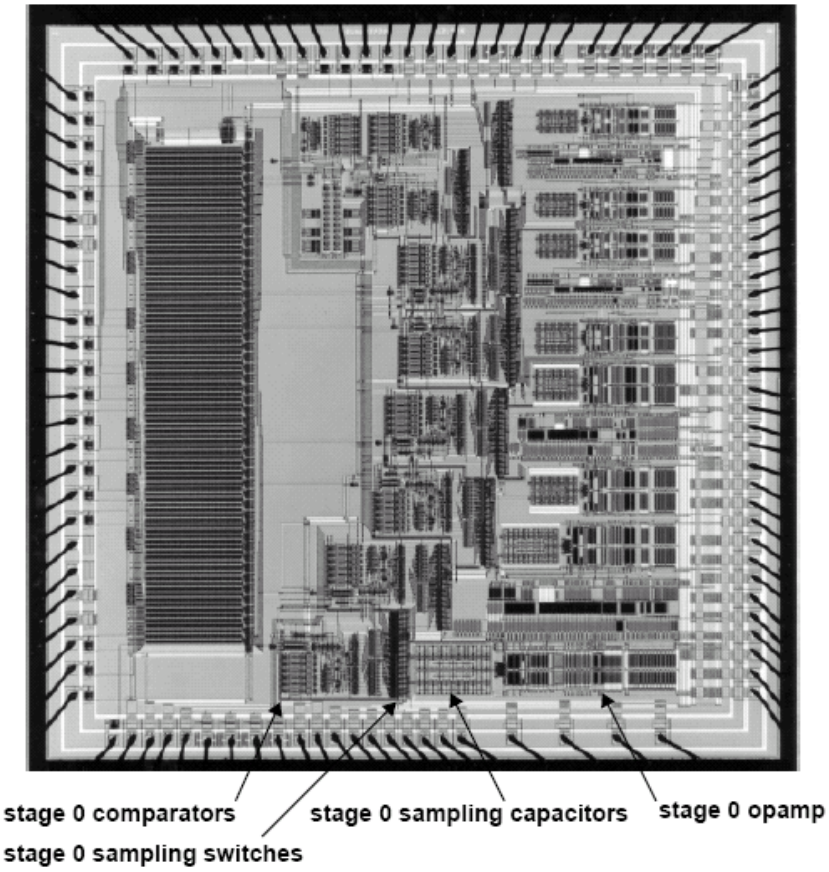
Shallow Optimum

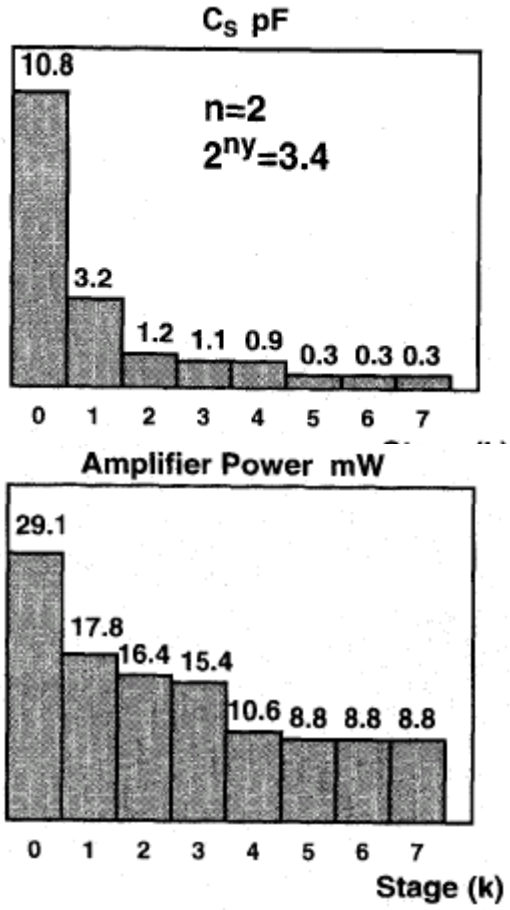
[Chiu 2004]



Capacitor scaling factor = 2^{Rx} $x=1 \Rightarrow$ scaling exactly by stage gain

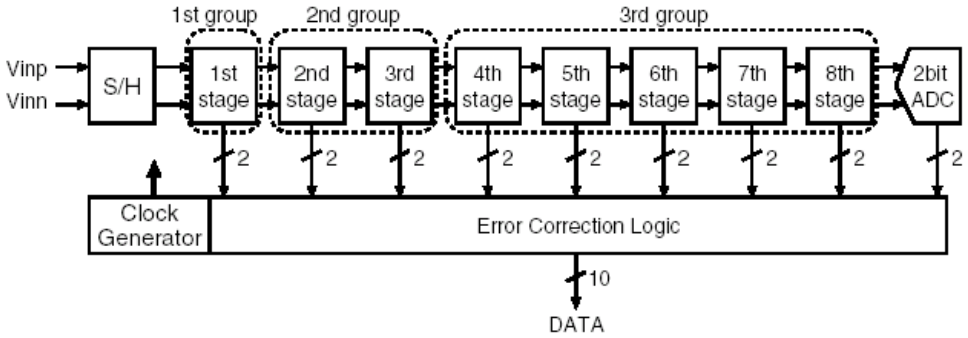
Stage Scaling Examples (1)

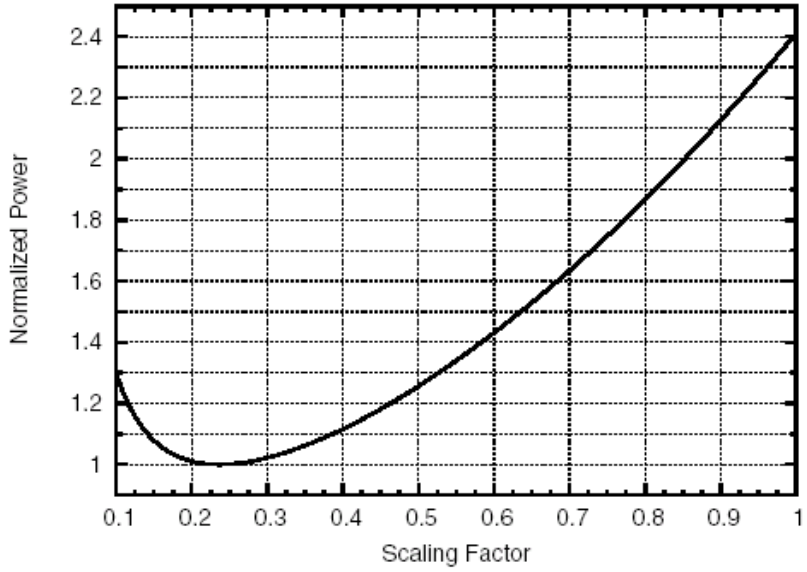




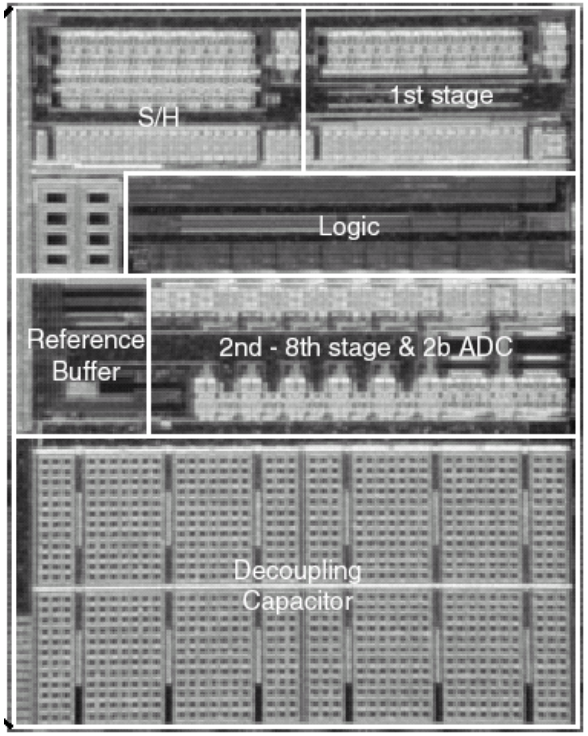
[Cline 1996]

Stage Scaling Examples (2)





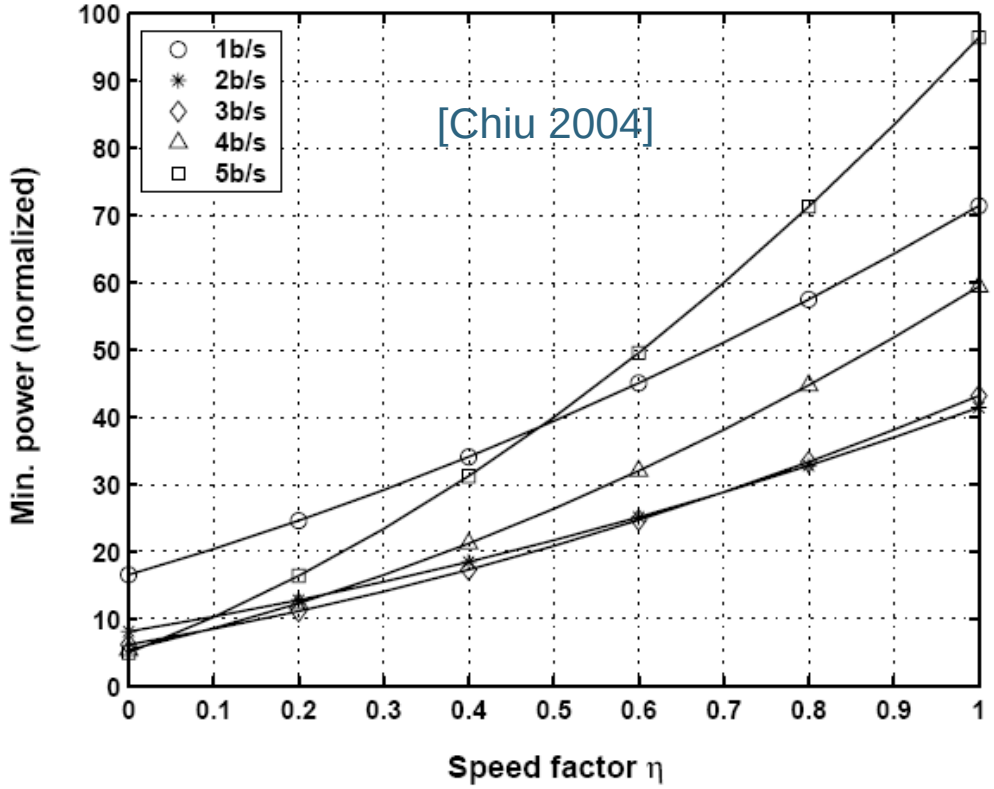
[Ishii 2005]



How Many Bits Per Stage?

- Low per-stage resolution (e.g. 1-bit effective)
  - – Need many stages
  - + OTAs have small closed loop gain, large feedback factor
    - High speed
- High per-stage resolution (e.g. 3-bit effective)
  - + Fewer stages
  - – OTAs can be power hungry, especially at high speed
  - – Significant loading from flash-ADC
  - – First stage output precision is significantly below overall ADC precision
- Qualitative conclusion
  - – Use low per-stage resolution for very high speed designs
  - – Try higher resolution stages when power efficiency is most important constraint

Power Tradeoff is Fairly Flat!



η = parasitic cap at output/total sampling cap in each stage (junctions, wires, switches, …)

- ADC power varies by only ~2x across different stage resolutions!

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Pipeline Examples

Examples

Reference	[Yoshioka, 2007]	[Jeon, 2007]	[Loloee 2002]	[Bogner 2006]
Technology	90nm	90nm	0.18um	0.13um
Bits	10	10	12	14
Bits/Stage	1-1-1-1-1-1-1-3	2-2-2-4	1-1-1-1-1-1-1-1-1-1-2	3-3-2-2-4
SNDR [dB]	~56	~54	~65	~64
Speed [MS/s]	80	30	80	100
Power [mW]	13.3	4.7	260	224
mW/MS/s	0.17	0.16	3.25	2.24

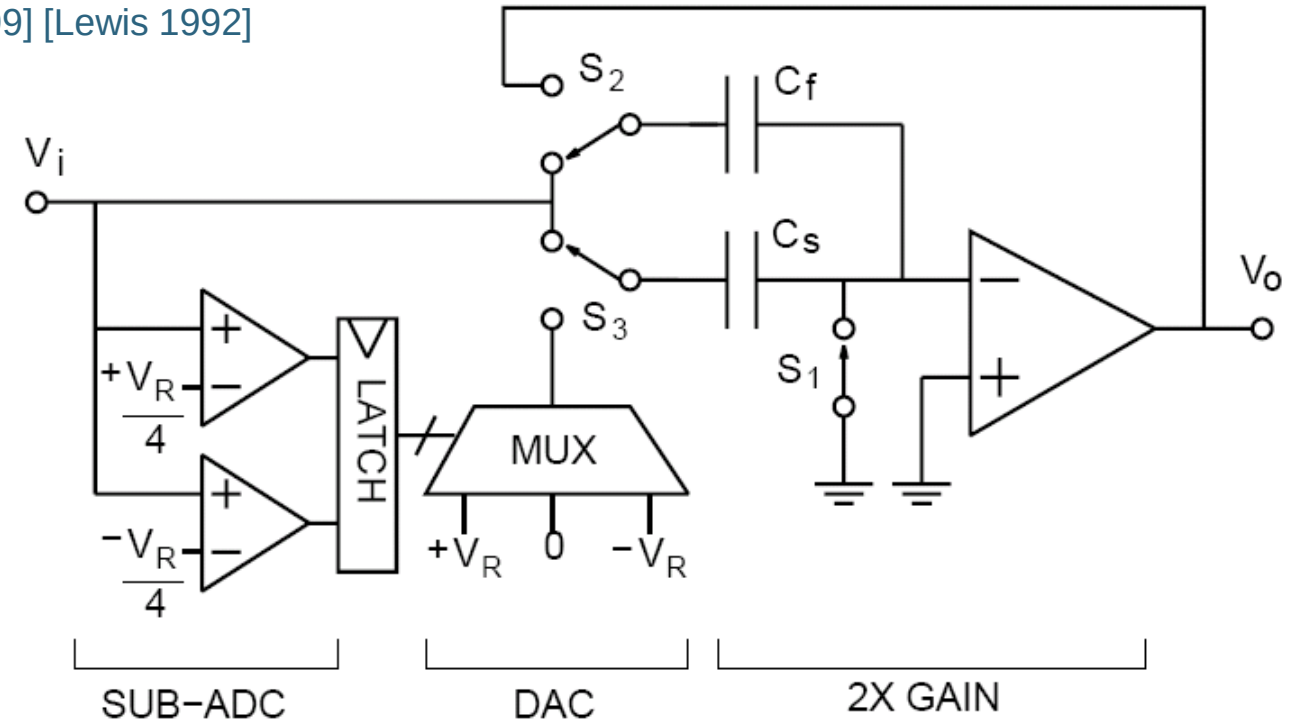
- Low power is possible for a wide range of architectures!

Re-Cap

- Choosing the "optimum" per-stage resolution and stage scaling scheme is a non-trivial task
  - But – optima are shallow!
- Quality of transistor level design and optimization is at least as important (if not more important than) architectural optimization …
- Next, look at circuit design details
  - Assume we're trying to build a 10-bit pipeline
    - Technology feature size ~0.18μm or smaller
    - Moderate to high-speed ~100MS/s
    - 1-bit effective/stage, using "1.5-bit" stage topology
    - Dedicated front-end SHA

1.5-Bit Stage Implementation

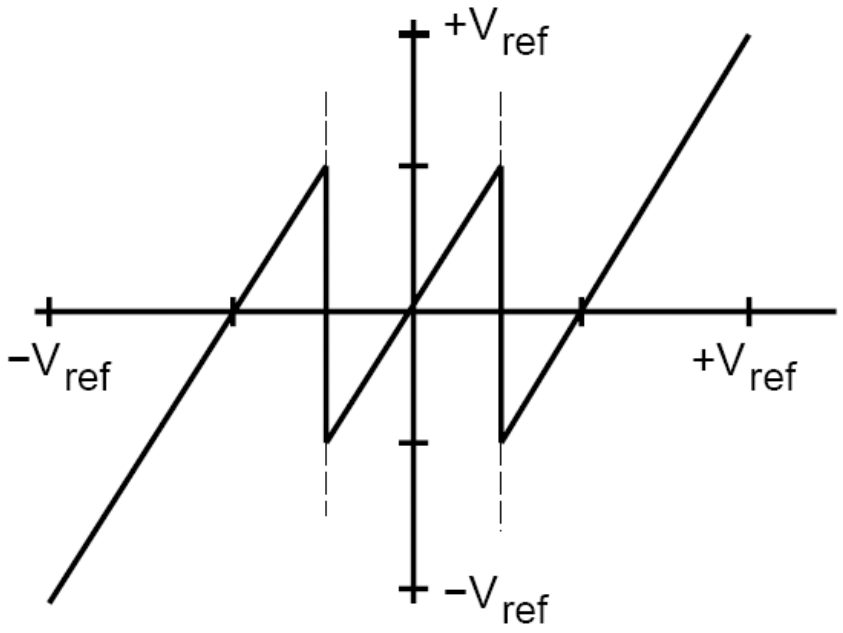
[Abo 1999] [Lewis 1992]



- C_f is used as sampling cap during acquisition phase, as feedback cap in redistribution phase
  - Helps improve feedback factor (max. 1/3 → max. 1/2)

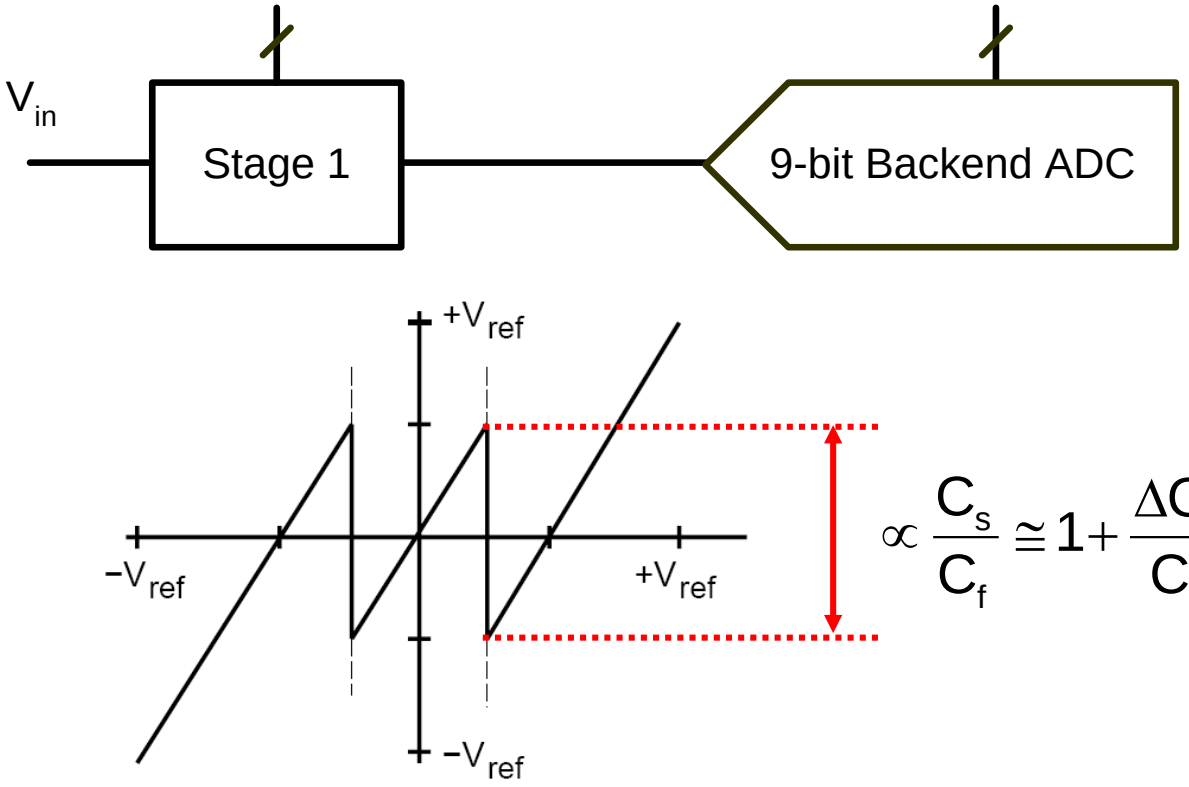
Residue Plot

$$V_o = \begin{cases} \left(1 + \frac{C_s}{C_f}\right) V_i - \frac{C_s}{C_f} V_{ref} & \text{if } V_i > V_{ref}/4 \\ \left(1 + \frac{C_s}{C_f}\right) V_i & \text{if } -V_{ref}/4 \leq V_i \leq +V_{ref}/4 \\ \left(1 + \frac{C_s}{C_f}\right) V_i + \frac{C_s}{C_f} V_{ref} & \text{if } V_i < -V_{ref}/4 \end{cases}$$



[Abo 1999]

Stage 1 Matching Requirements



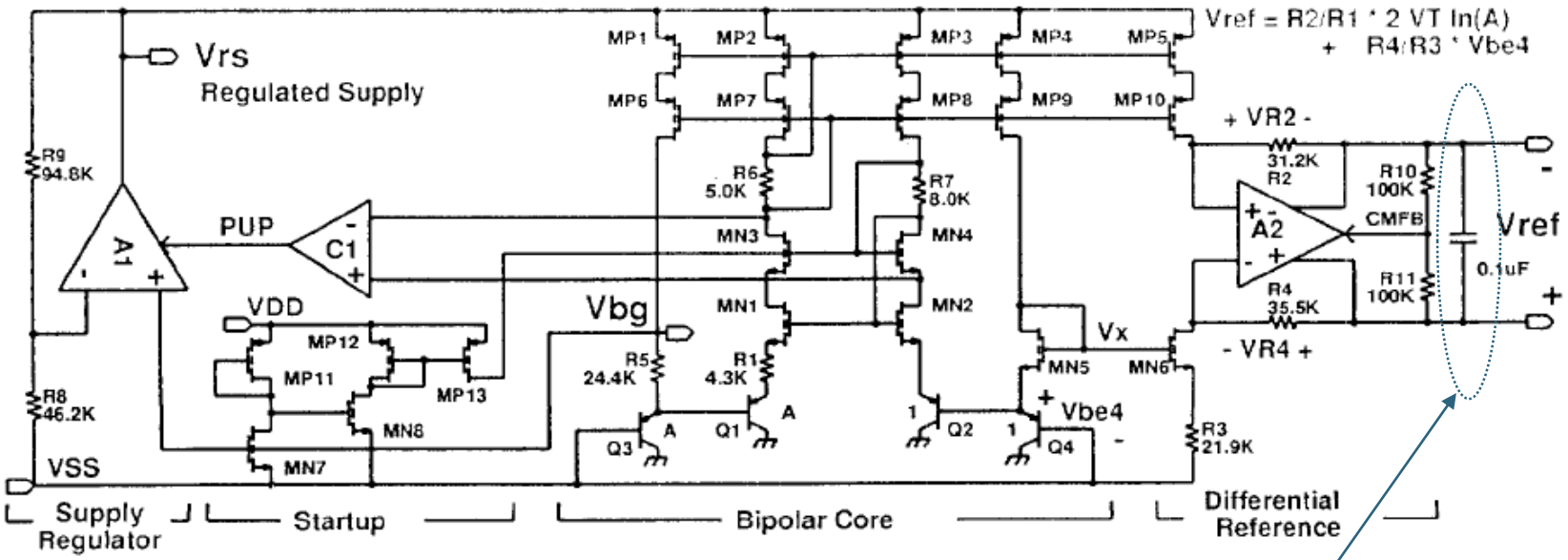
- Error in residue transition must be accurate to within a fraction of 9-bit backend LSB
  - Typically want $\Delta C/C$ ~0.1% or better

Capacitor Matching

- 0.1% "easily" achievable in current technologies
  - Even with metal sandwich caps, see e.g. [Verma 2006]
    - Beware of metal density related issues
  - For MIMCap matching data see e.g. [Diaz 2003]
- What if we needed much higher resolution than 10 bits?
  - Digital calibration
  - Multi-bit first stage
    - Each extra bit resolved in the first stage alleviates precision requirements on residue transition by 2x
    - For fixed capacitor matching, can show that each (effective) bit moved into the first stage
      - Improves DNL by 2x
      - Improves INL by sqrt(2)x
    - Multi-bit examples: [Singer 1996] [Kelly 2001] [Lee 2007]

Typical Reference Generator

[Brooks 1994]

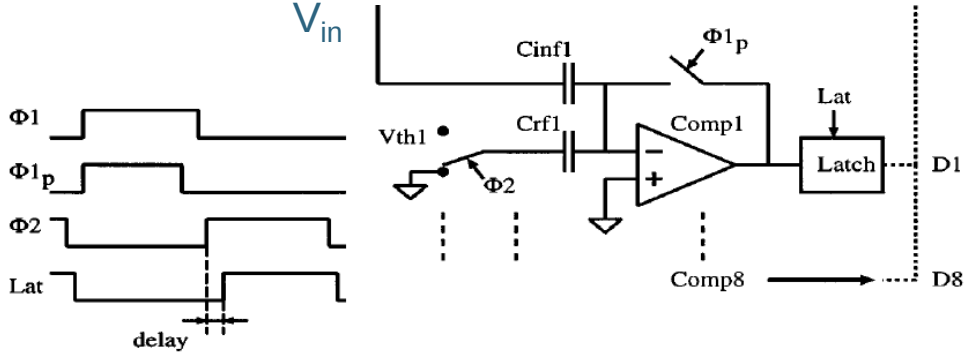


External decoupling caps provide dynamic currents
⇒ Low power reference buffer

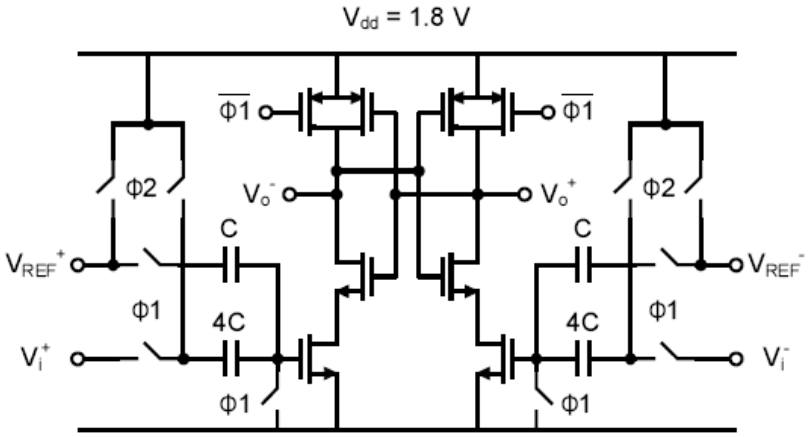
Comparators

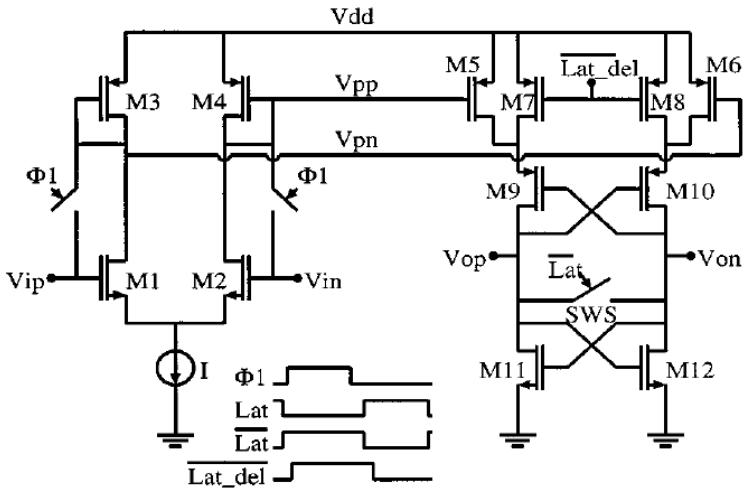
- Can tolerate large offsets and large noise with appropriate redundancy
- Consume negligible power in a good design
  - 50–100μW or less per comparator
- Lots of implementation options
  - Resistive/capacitive reference generation
  - Different pre-amp/latch topologies
  - …

Comparator Examples



[Chiu 2004]





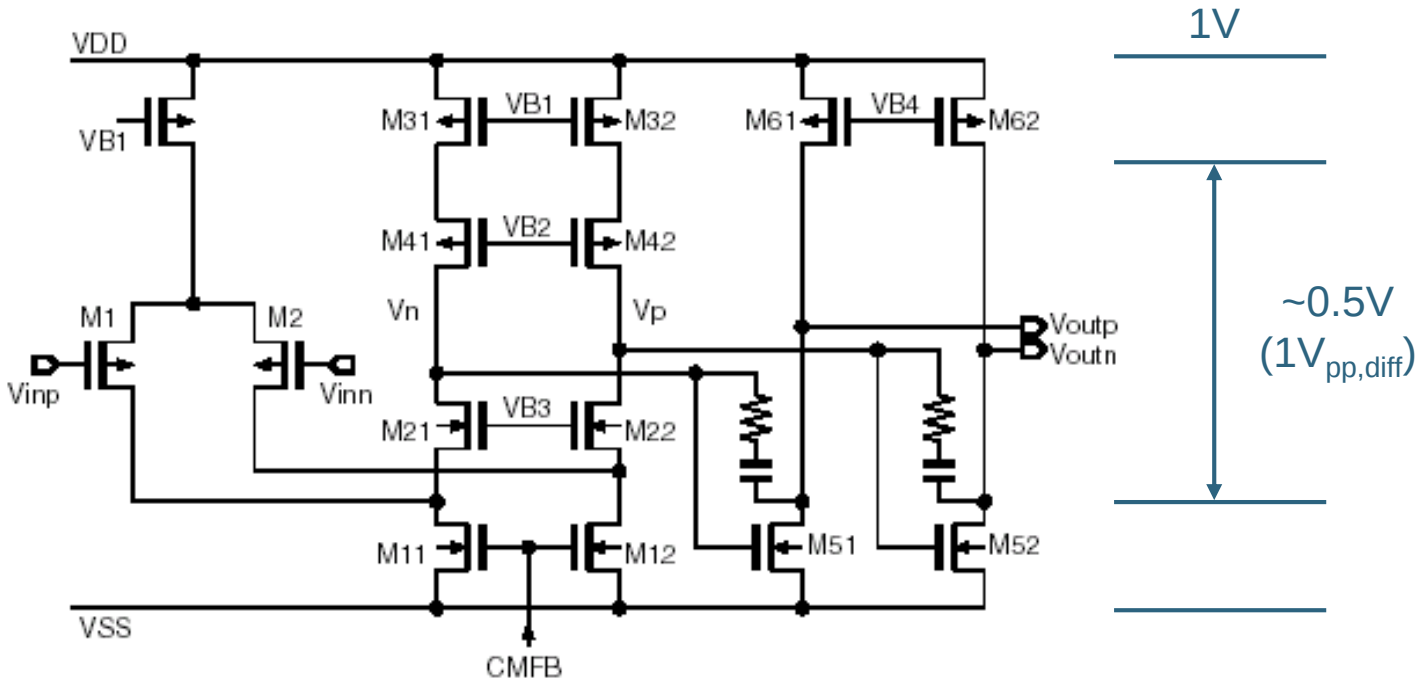
[Mehr 2000]

OTA Design Considerations

- Static amplifier error = 1/(DC Loop Gain)
  - E.g. for 0.1% accuracy in first stage of 10-bit ADC, need loop gain > 60dB
- Dynamic settling error
  - Typically want to settle outputs to ~1/8 LSB accuracy within 1/2 clock cycle
- Thermal noise
  - Size capacitors to satisfy kT/C noise requirement
- Start by picking an OTA topology that will deliver sufficient gain
  - Or think about ways to compensate finite gain error …
- General references on OTA design
  - 240B [Boser 2005], [Murmann], [Alon]

Two-Stage Folded Cascode OTA

[Ishii 2005]



- Works down to VDD=1V with reasonable output swing
- Gain ~ $(g_m r_o)^3$ ~ 10^3 = 60dB
- Use gain boosting to achieve larger gain

How Fast Can We Go? (1)

- Non-dominant pole in two-stage amplifier hard to move past $f_T/5$
- For 73 degrees phase margin (optimum for fast settling), loop crossover frequency is 1/3 of non-dominant pole frequency
- Settling linearly to 0.1% precision takes 7 loop time constants; typically budget ~10 time constants
- Ideally, we'd have 1/2 clock cycle to settle linearly, but there is some time needed for slewing and non-overlap clock timing
  - Assume 60% of half cycle is available for linear settling
- In summary

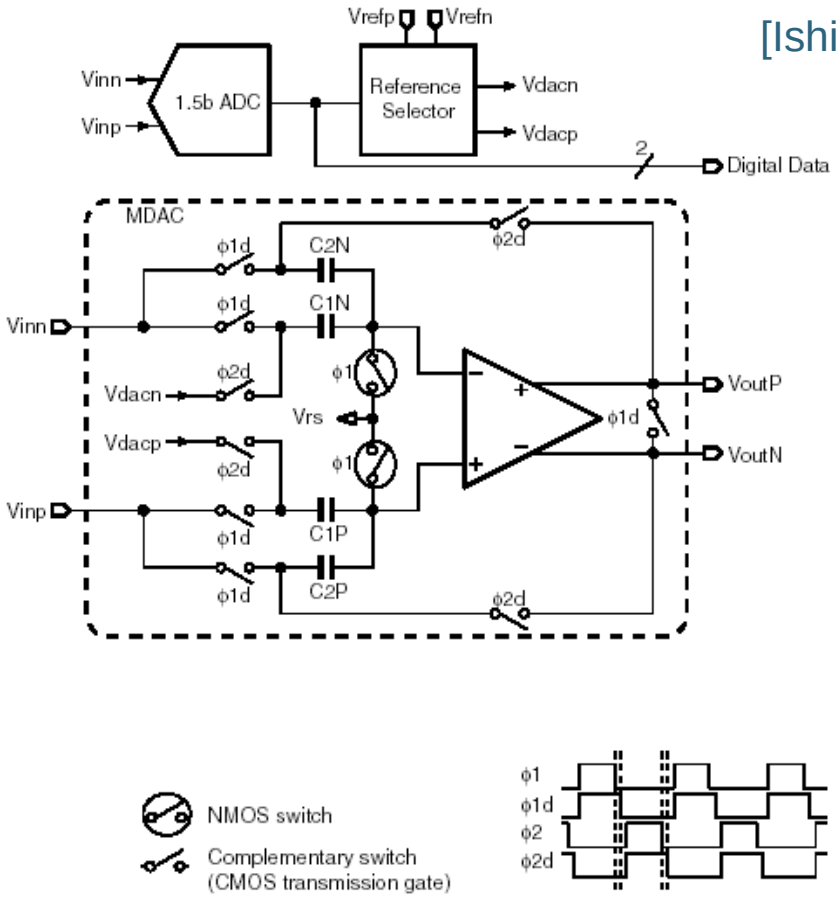
$$f_{CLK,max} = \frac{f_T}{5}\frac{1}{3}\cdot 2\pi \cdot \frac{1}{10}0.5\cdot 0.6 = \frac{f_T}{80}$$

How Fast Can We Go? (2)

Technology	NMOS f_T (at moderate V_{GS}-V_t ~150mV)	$f_{CLK,max} = f_T/80$
0.35um	10GHz	125 MHz
0.18um	30GHz	375 MHz
90nm	90GHz	1.125GHz

- Sampling speeds of 200-300MHz are "easily" achievable modern technologies
  - f_T is no longer a showstopper
  - Speed ultimately constrained by power, power efficiency and/or clock jitter

Switches



[Ishii 2005]

- Make switch RC ~ 10 times faster than OTA
  - Avoids speed degradation
  - Minimizes switch noise contribution
    - See e.g. [Schreier 2005]
  - Avoids stability issues due to poles in feedback network
- Three choices for switches
  - Single N or P device
  - Transmission gate
  - Bootstrapped NMOS
    - For high swing nodes that require constant R_{on}

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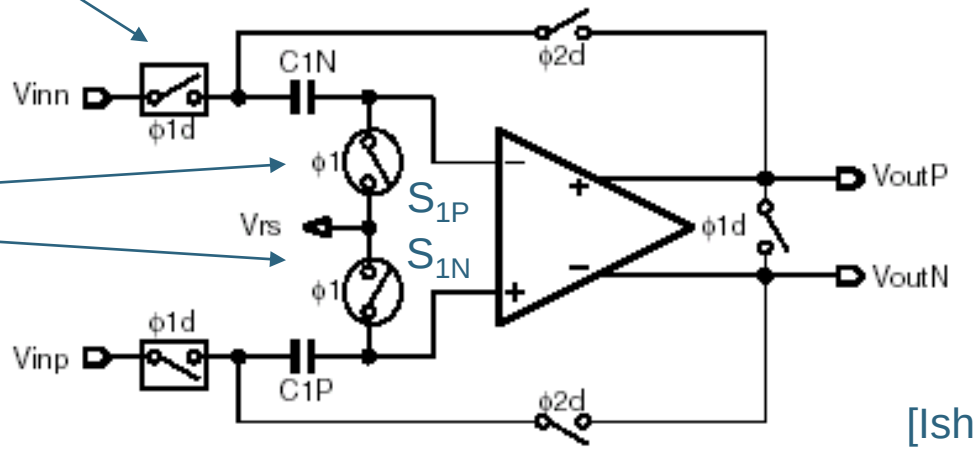
Pipeline SHA

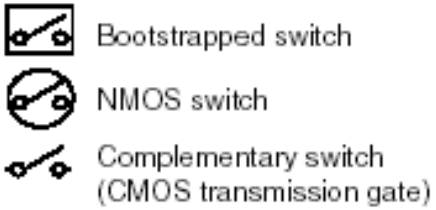
Front-End SHA

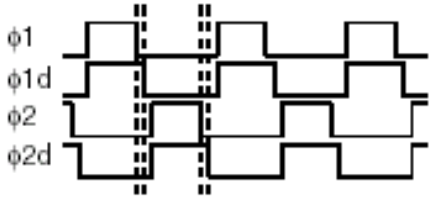
Need constant R_{ON} here to minimize signal dependent charge injection from S_{1N}, S_{1P}

Minimize Jitter!

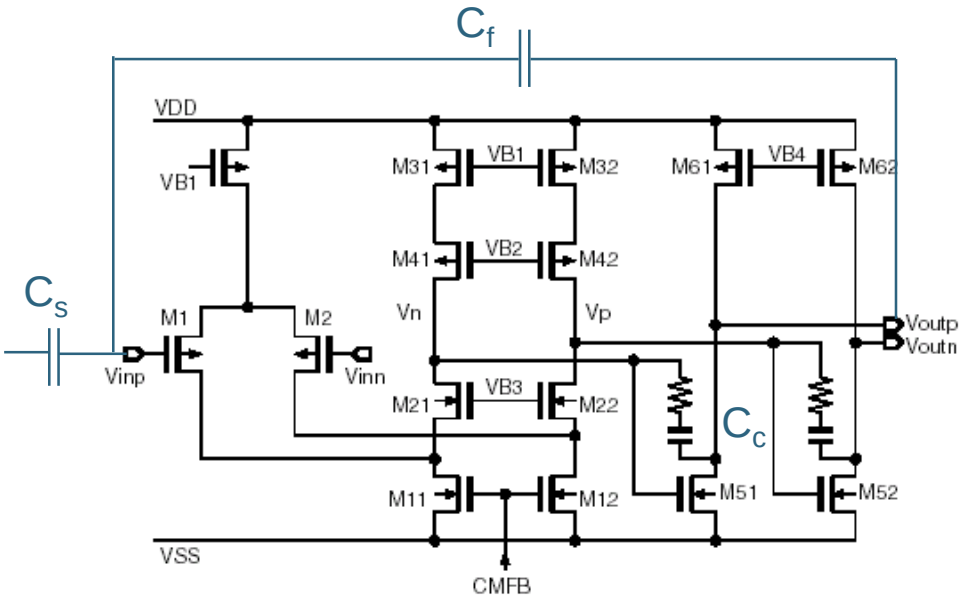


[Ishii 2005]





Total Integrated OTA Noise (1)



$$N_1 = 1 + \frac{g_{m11} + g_{m31}}{g_{m1}} \cong 2...4$$

$$N_2 = 1 + \frac{g_{m61}}{g_{m51}} \cong 2$$

$$\overline{V_{od}^2} = \underbrace{2\frac{1}{\beta}\cdot\gamma\cdot N_1\frac{kT}{C_c}}_{\text{OTA Stage 1}} + \underbrace{2(\gamma\cdot N_2 + 1)\frac{kT}{C_{Ltot}}}_{\text{OTA Stage 2}}$$

ignore in first cut design

$$\beta = \frac{C_f}{C_f + C_s + C_{gs1}}$$

$$C_{Ltot} = C_L + (1-\beta)C_f + C_{parasitic}$$

Total Integrated OTA Noise (2)

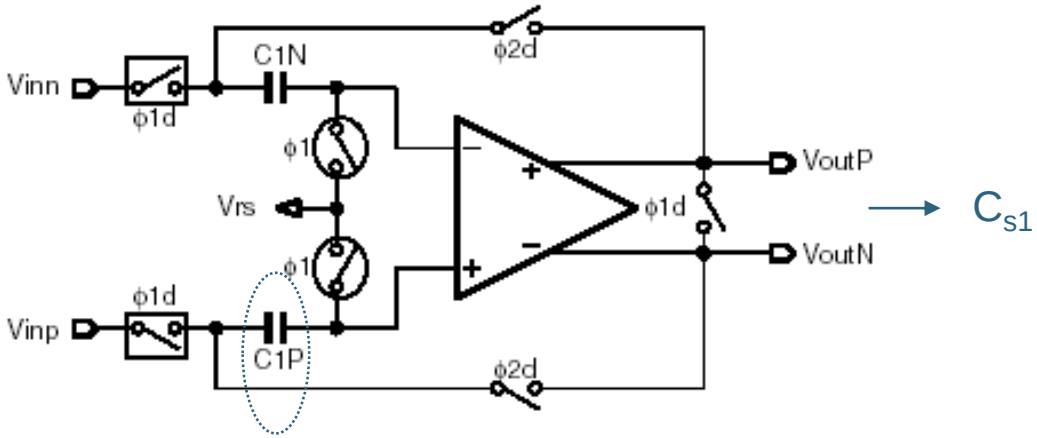
- Assuming $\gamma=1$, $N_1=N_2=2$

$$\overline{V_{od}^2} = 4\frac{1}{\beta}\cdot\frac{kT}{C_c} + 6\frac{kT}{C_{Ltot}}$$

- OTA noise partitioning problem
  - How should we split noise between stage1 and stage2 terms?
- In this design example we'll use a 2/3, 1/3 split
  - This is yet another design/optimization parameter
- With this assumption, we have

$$\overline{V_{od}^2} = 18\frac{kT}{C_{Ltot}} \qquad C_c = \frac{C_{Ltot}}{3\beta}$$

SHA Noise



C_{s1}

C_{s0} → Design choice: $C_{s0} = C_{s1}$

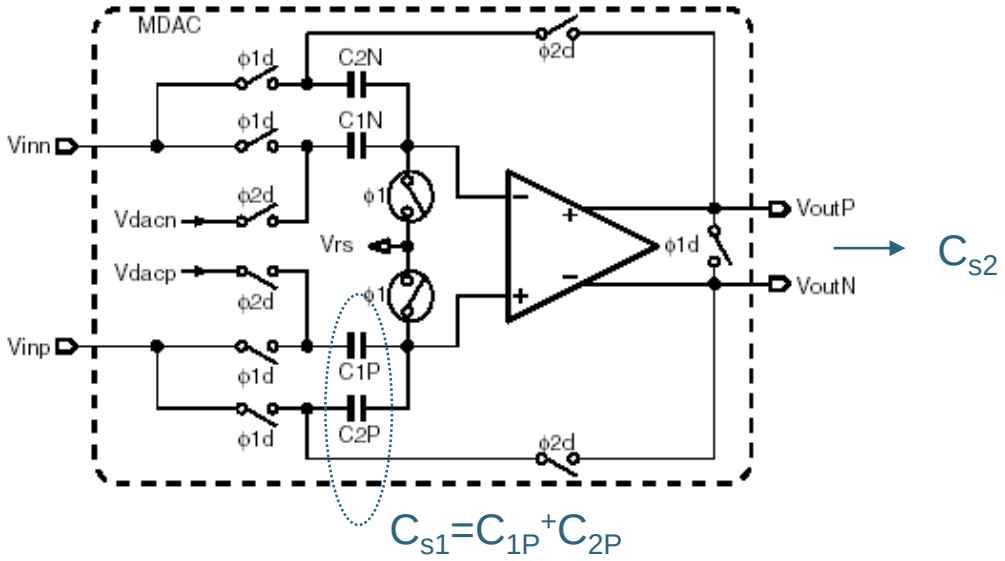
$$\beta = \frac{C_{s0}}{C_{s0} + C_{gs1}} \cong \frac{1}{2}$$

$$C_{Ltot} = C_{s1} + \left(1 - \frac{1}{2}\right)\frac{C_{s0}}{2}$$

From sample phase (ϕ1)

$$\overline{V_{od,0}^2} = \overline{V_{id,0}^2} = 18\frac{kT}{C_{s1} + C_{s0}/4} + \frac{kT}{C_{s0}} \cong 16\frac{kT}{C_{s1}}$$

Stage 1 Noise



$$\beta = \frac{C_{s1}/2}{C_{s1}+C_{gs1}} \cong \frac{1}{3}$$

$$\overline{V_{od,1}^2} = 18\frac{kT}{C_{s2}+C_{s1}/3}$$

$$C_{Ltot} = C_{s2} + \left(1-\frac{1}{3}\right)\frac{C_{s1}}{2}$$

$$\overline{V_{id,1}^2} = \frac{18}{2^2}\frac{kT}{C_{s2}+C_{s1}/3}$$

Noise Budgeting

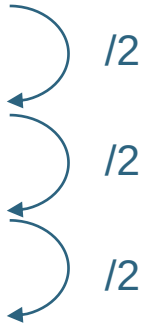
- Total input referred noise budget, assuming $V_{FS,diff}=1V$
  - $N_{thermal} = N_{quant}=LSB^2/12=(1V/2^{10})^2/12=(280\mu Vrms)^2$
- Reasonable "first cut" partitioning of input referred noise
  - SHA → 1/2
  - Stage 1 → 1/4
  - All remaining stages → 1/4

$$\overline{V_{id,0}^2} = 16\frac{kT}{C_{s1}} = \frac{1}{2}(280\mu Vrms)^2 \Rightarrow C_{s1} = 1.66pF$$

$$\overline{V_{id,1}^2} = \frac{9}{2}\frac{kT}{C_{s2}+C_{s1}/3} = \frac{1}{4}(280\mu Vrms)^2 \Rightarrow C_{s2} = 0.38pF$$

Capacitor Sizes

C_{s0}	1.66pF
C_{s1}	1.66pF
C_{s2}	0.38pF
C_{s3}	190fF
C_{s4}	85fF
C_{s5}	42.fF (minimum)
…	…
C_{s10}	42.fF (minimum)



- Now refine these numbers using simulation and Excel spreadsheet
  - Iterate over assumptions/design choices to optimize design

Reality Check

[Honda 2007]

STAGE	C_s [pF]	Power [mW]
S/H	2.0	3.5
STAGE1	1.0	3.0
STAGE2	0.5	2.0
STAGE3	0.3	2.0
STAGE4	0.3	1.8
STAGE5	0.16	1.8
STAGE6	0.16	1.5
STAGE7-10	0.1	1.5
Others [Bias circuits, Clock gen.]		5.0
Total static power		26.6

Technology	90nm digital CMOS
Supply voltage	1.0 V
Resolution	10 bits
Sampling rate	100 MSample/s
Full scale analog input	0.8 V_{pp}
Maximum DNL	-0.7/+0.3 LSB
Maximum INL	-0.6/+0.7 LSB
SNDR ($F_{in} \cong$ 10MHz)	55.3dB
SFDR ($F_{in} \cong$ 10MHz)	71.5dB
Total power consumption	33mW
Packaging	Chip-on-board
Active area	1.3mm×3.1mm

- Not too far off from a practical design…

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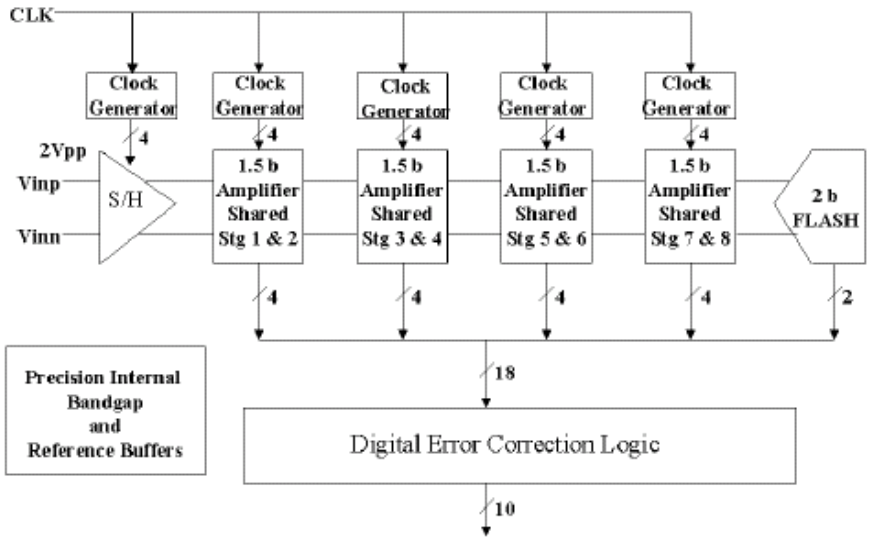
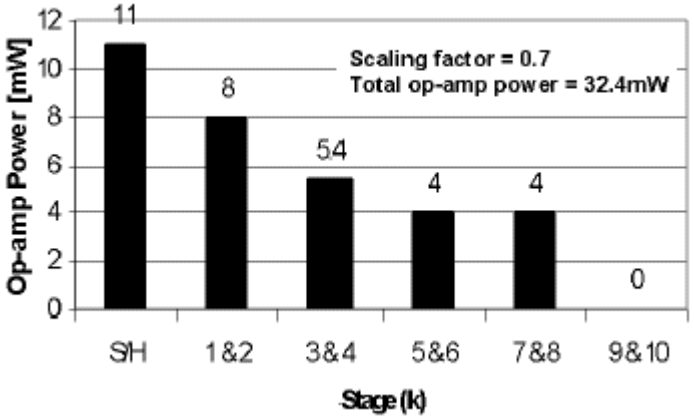
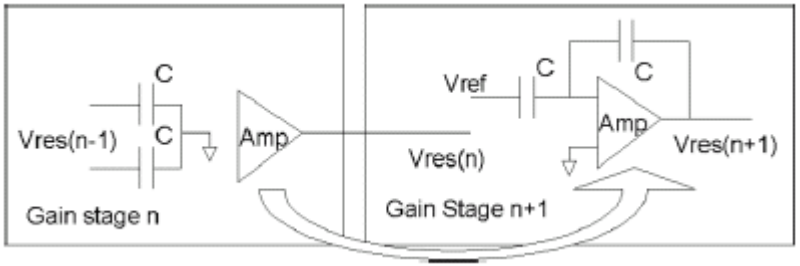
Pipeline Optimizations

Amplifier Sharing (1)



[Min 2003]

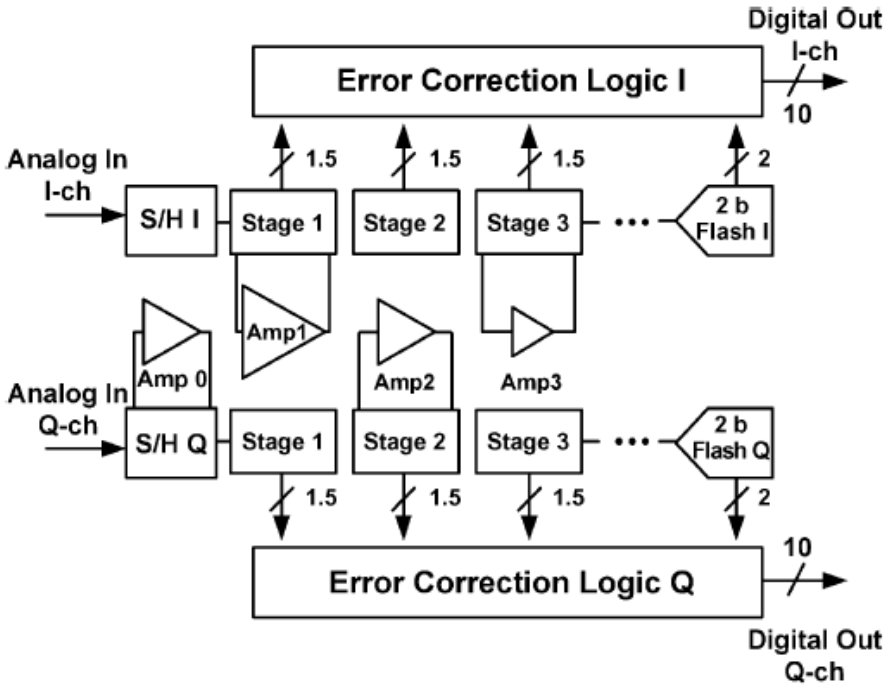




- Limited power savings because amplifiers have different specs

Amplifier Sharing (2)

[Kurose 2006]

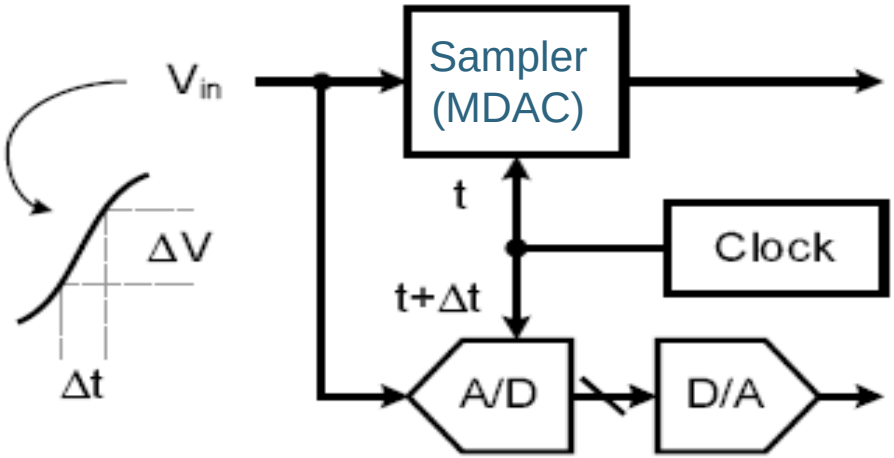


Technology	90-nm 1-P 7-M CMOS
Supply Voltage	1.2 V
Resolution	10 bit
Sampling Rate	200 MSPS
Full Scale	$0.8V_{p\text{-}p}$
DNL	+0.66/-0.61 LSB
INL	+0.90/-1.00 LSB
SFDR	66.5 dB
SNR	57.4 dB@Fin=9.9 MHz 55.6 dB@Fin=89.9 MHz
SNDR	54.4 dB@Fin=9.9 MHz 53.6 dB@Fin=89.9 MHz
ENOB	8.7 bit@Fin=9.9 MHz 8.6 bit@Fin=89.9 MHz
I/Q Isolation	>59 dB
Area	1.8 mm × 1.4 mm (2 ch)
Power	54.6 mW/ch

- Sharing of amplifiers is most efficiently done in a pair of converters that process I/Q signals

SHA-Less Architectures (1)

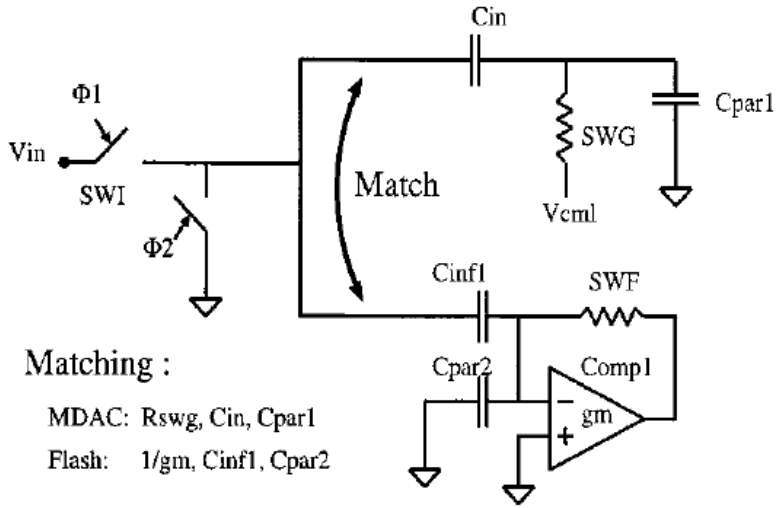
- Motivation
  - SHA can burn up to 1/3 of total ADC power
- Removing front-end SHA creates acquisition timing mismatch issue between first stage MDAC & Flash



[Chiu 2004]

SHA-Less Architectures (2)

- Strategies
  - Use first stage with large redundancy; this can help absorb fairly large skew errors
  - Try to match sampling sub-ADC/MDAC networks
    - Bandwidth and clock timing



[Mehr 2000]

Fig. 5. Matching input networks for the MDAC and the flash comparators.

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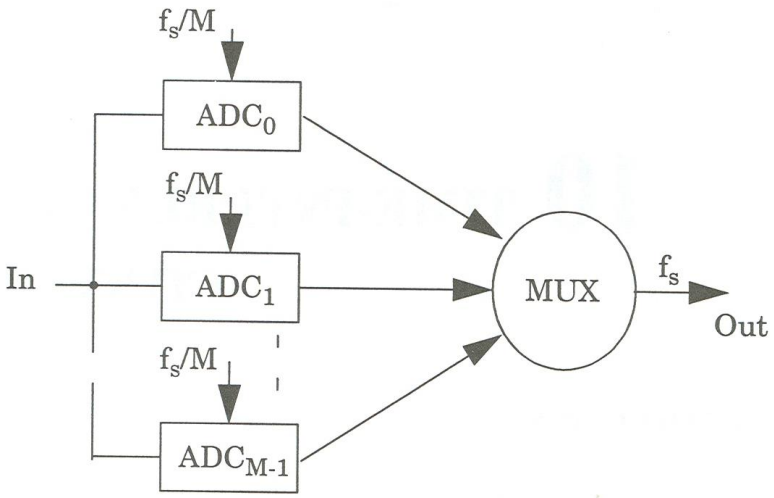
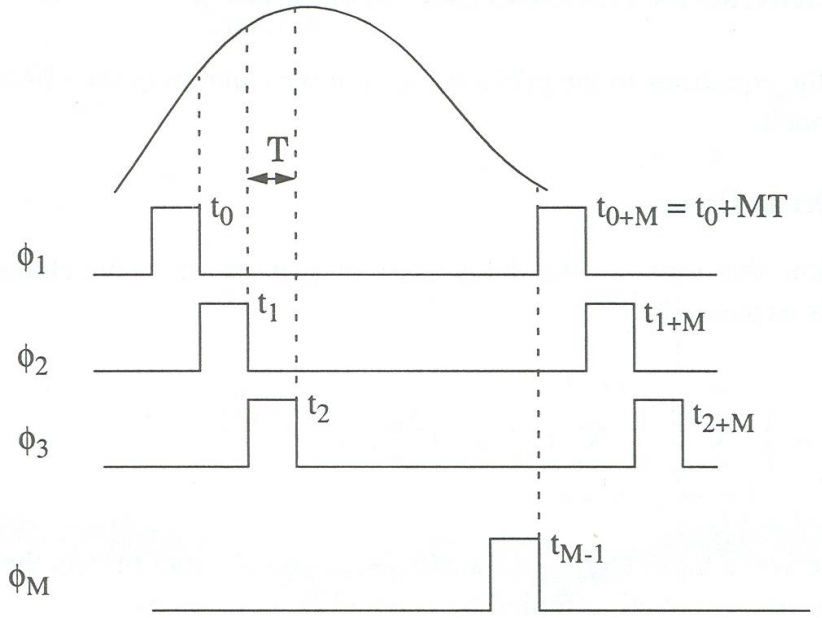
EE 240C
Analog-Digital Interface Integrated Circuits

Time Interleaved ADCs

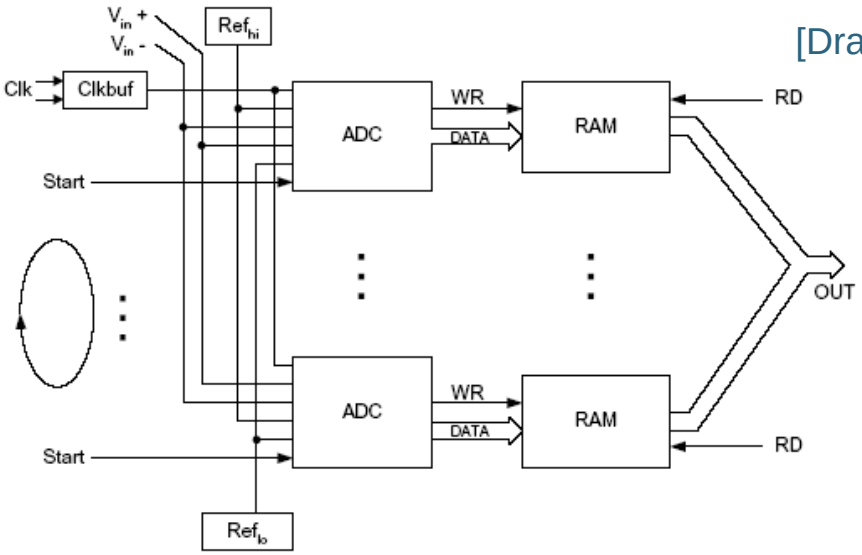
Time Interleaved ADCs



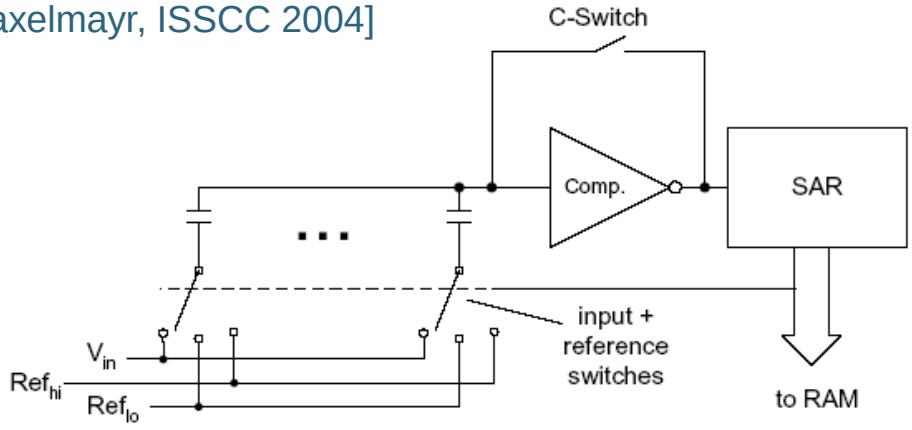


- Idea: Run M ADCs in parallel to obtain an aggregate throughput rate of M·fs
- Catch: Each ADC still needs an acquisition bandwidth that is commensurate with maximum input frequency

Example (1)

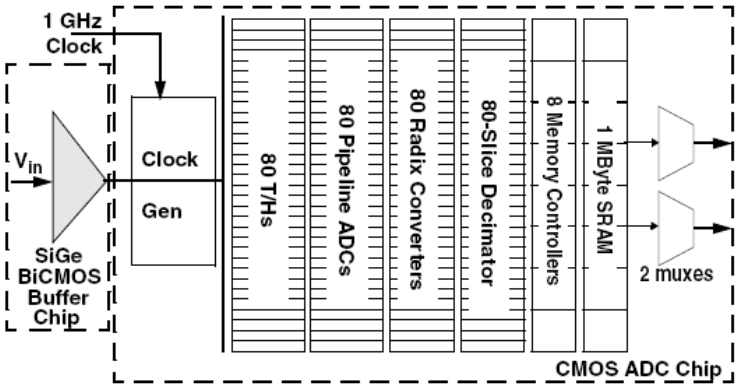


[Draxelmayr, ISSCC 2004]



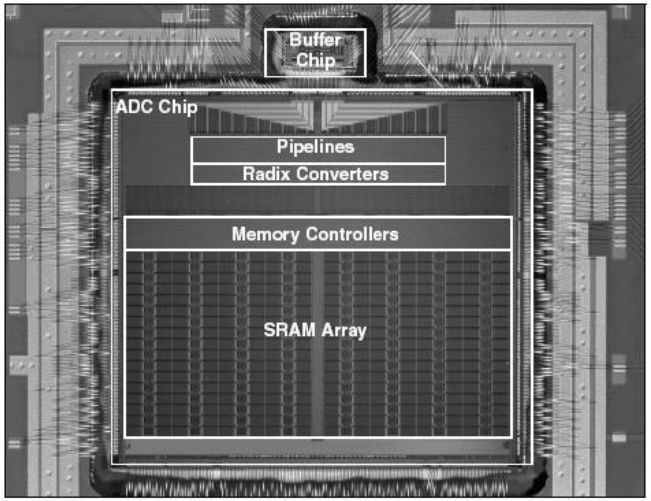
- Idea
  - Interleave several "slow" SAR ADCs to get high throughput while maintaining low complexity and good power efficiency
- Array consists of eight 6-bit ADCs, each running at 75 MS/s
  - 8 cycles per ADC (2 for acquisition, 6 for conversion)
  - Aggregate throughput is 600MS/s, power=10mW in 90-nm CMOS technology

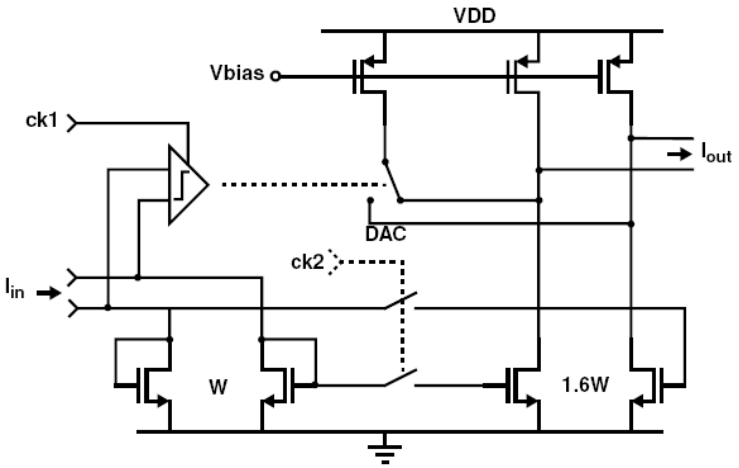
Example (2)



[Poulton, ISSCC 2003]

Sample Rate	20 GSa/s	
Resolution	8 bits	
INL Intrinsic With linearity correction	 ±1.7 LSBs ±0.4 LSBs	
DNL	±0.3 LSBs	
Bandwidth	6.6 GHz	
Accuracy @ 500 MHz input @ 6 GHz input	 6.5 effective bits 4.6 effective bits	
Jitter	0.7 ps rms	
Input Range	0.25 Vpk differential	
	Buffer Chip	**ADC Chip**
Input Capacitance	0.2 pF	4 pF
Power	1 W	9 W
Chip Size	1.2 x 2.6 mm	14 x 14 mm
Technology	40-GHz SiGe BiCMOS	0.18-mm CMOS
Transistors	1000	50M
Package	438-ball BGA	



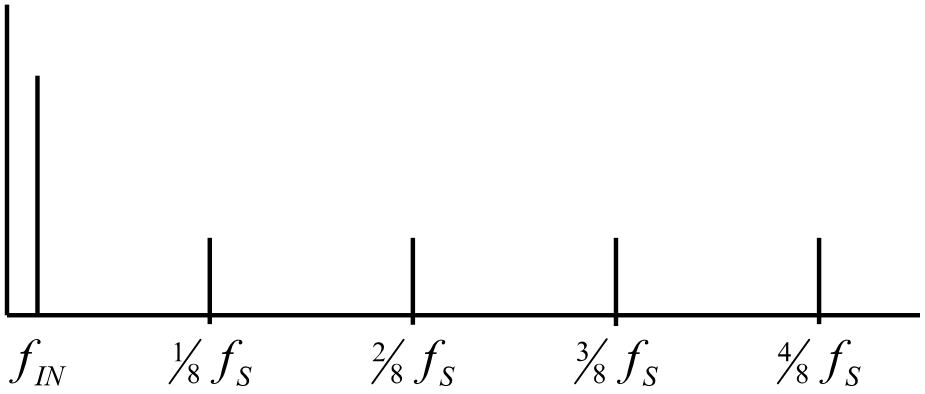


Issues with Time Interleaving

- Offset mismatch → easy to calibrate
  - Each channel will have a different offset
  - Output will contain a periodic error sequence that manifest itself as spurs in the output spectrum
- Gain mismatch → easy to calibrate
  - Channels may also have slightly different gain
  - Results in amplitude modulation
- Phase skew / Timing mismatch
  - Hard to guarantee precise phase relationship between individual channel clocks
  - Results in phase modulation (similar to aperture uncertainty)
- Bandwidth mismatch
  - Results in phase and amplitude modulation
- Solutions
  - "Careful design"
  - Analog or digital calibration (See e.g. [Jamal, JSSC 12/2002])

Tones due to channel mismatch

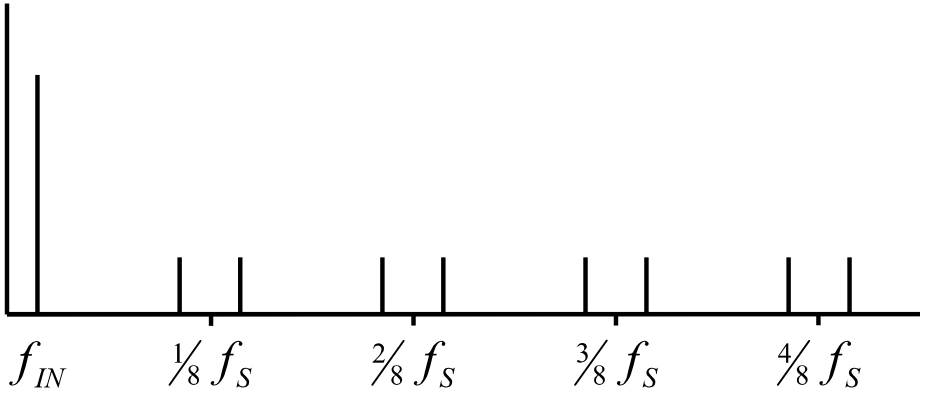
offset mismatch



(a)

M channels with offset differences
→ tones at m f_s/M for m = 0, 1, … M-1

gain or phase mismatch



(b)

M channels with gain or timing differences
→ tones at m $f_s/M \pm f_{in}$

[S. Louwsma, E. van Tuijl, and B. Nauta, *Time-interleaved Analog-to- Digital Converters* Springer Netherlands, 2011]

- Mismatch → periodic with period M T_s
  → frequency domain: tones at multiples of f_s / M

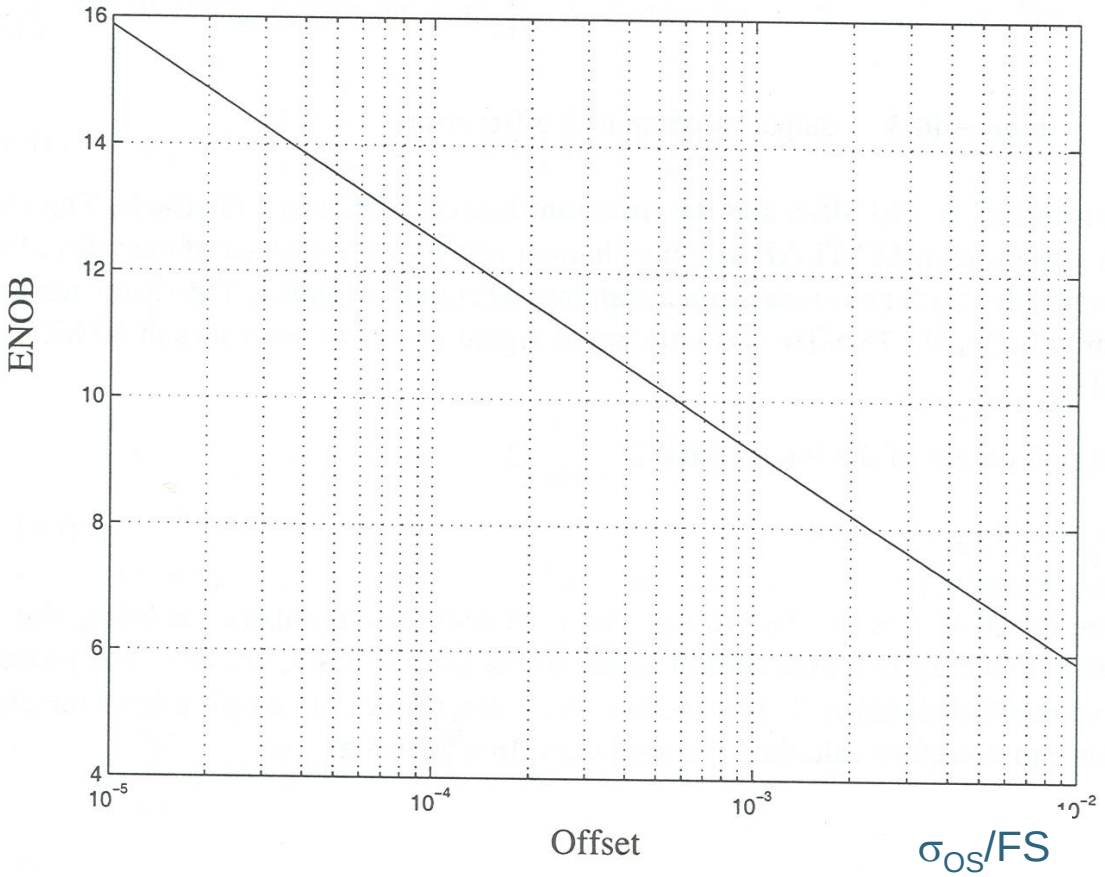
- Offset mismatch: additive

$$x[n] + \text{offset}[n] \rightarrow \text{X(f)} + \sum Om\,(f\ - m\frac{f_s}{M})$$

- Gain mismatch: multiplicative in time domain

$$x[n]\ (1 + \text{gain}[n])\ \rightarrow X(f) \star \left(\delta(f) + \sum G_m(f\ - m\frac{f_s}{M})\right)$$

Impact of Offset Mismatch



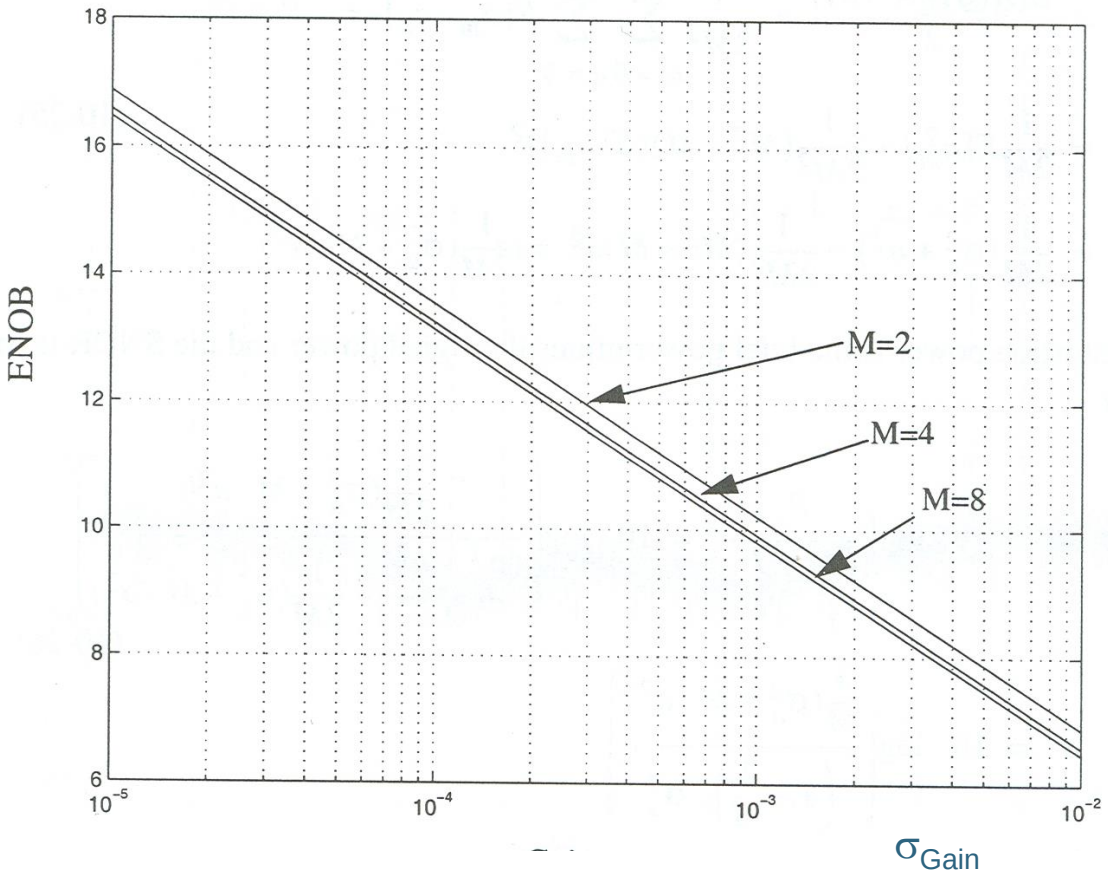
[Gustavsson, p.262]

$$\mathrm{SNDR}_{\mathrm{offset}} \leq 10\log_{10}\frac{M}{M-1}\frac{A^2}{2{\sigma_{\mathrm{offset}}}^2}$$

M: interleaving factor
A: amplitude
σ_{offset}: offset std dev

- E.g. FS=1V, σ_{OS}=1mV ⇒ ENOB~9bits!

Impact of Gain Mismatch



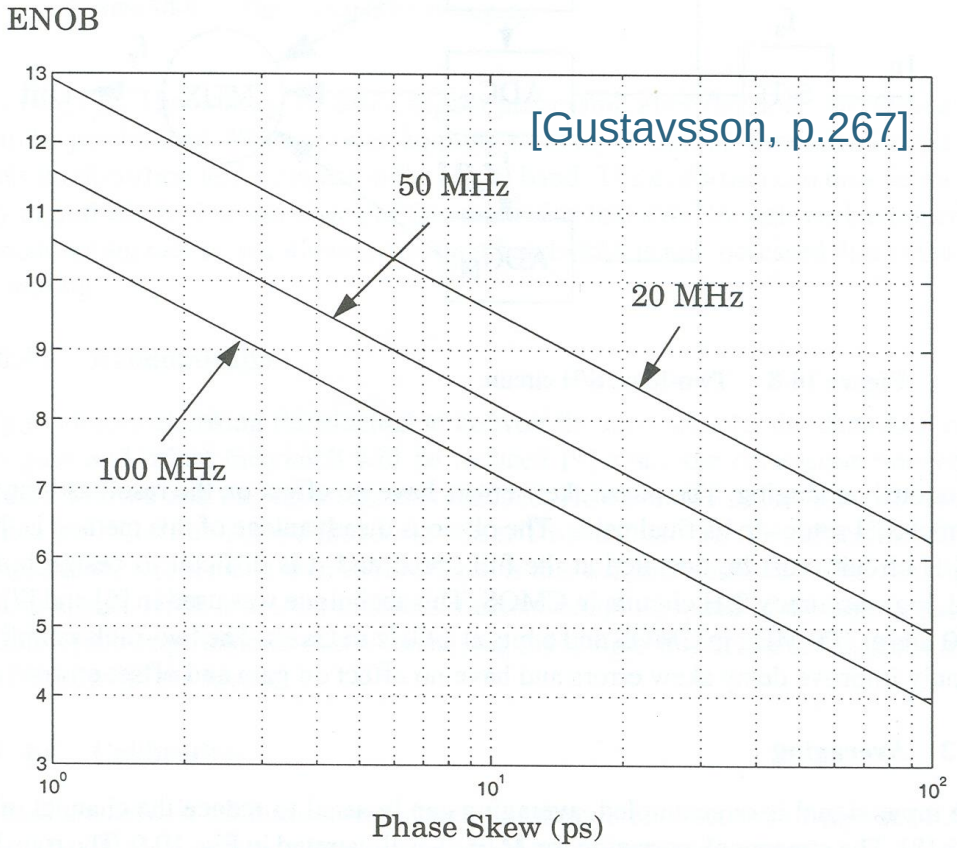
[Gustavsson, p.266]

$$\text{SNDR}_{\text{gain}} \leq 10 \log_{10} \frac{M}{M-1} \frac{G^2}{{\sigma_G}^2}$$

M: interleaving factor
G: gain
σ_{offset}: gain std dev

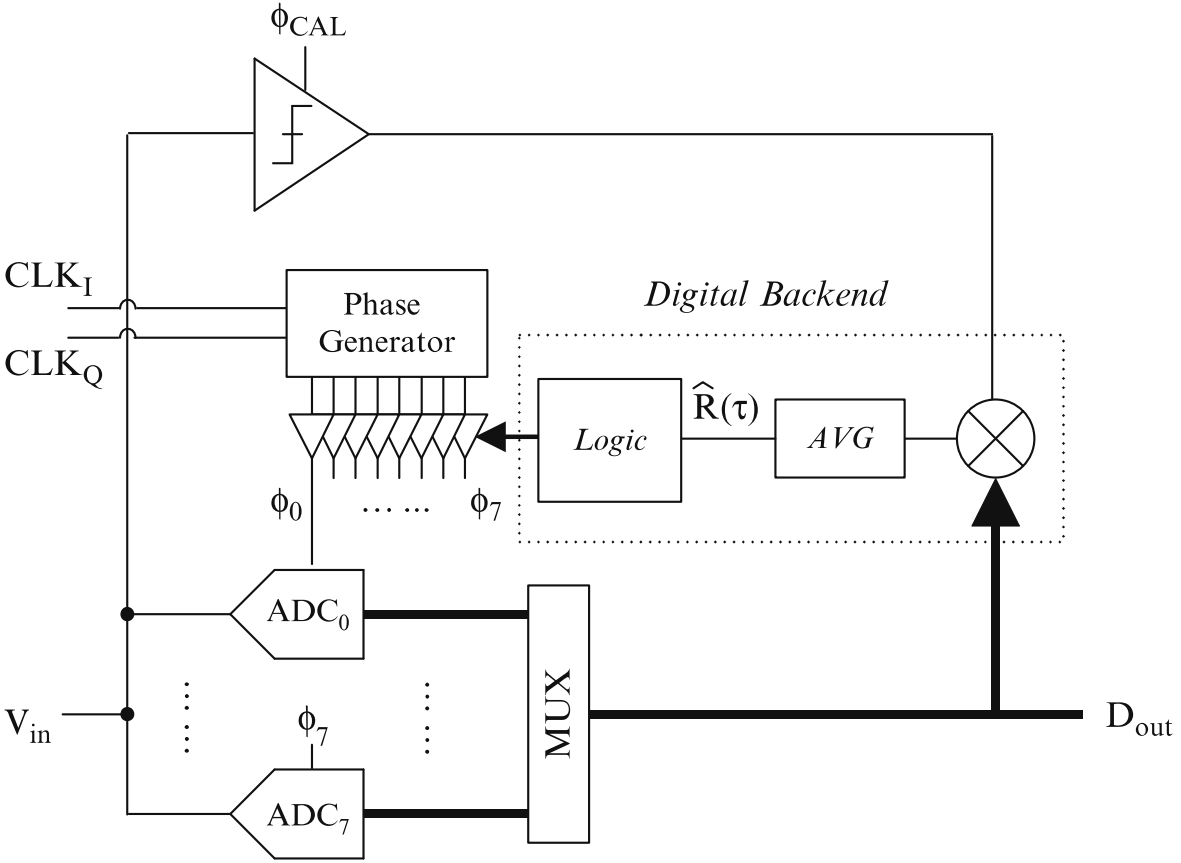
- E.g. σ_{Gain}=0.1% $\Rightarrow$ ENOB~10bits

Impact of Phase Skew / Timing Mismatch



- Above chart is for M=4 channels
- E.g. f_{in}=100MHz, phase skew=3ps ⇒ ENOB~9bits!

Example of Background Calibration for Timing Mismatch



[M. El-Chammas and B. Murmann, *Background Calibration of Time-Interleaved Data Converters*. Springer-Verlag New York, 2012]