EE 240C Project: ADC Modeling and Non-Ideality Analysis

1 Choice of Architecture

The desired specs for the ADC are listed in Table 1.

Table 1: ADC Specifications

Parameter	**Value**
Bandwidth	$\geq$ 12.5 MHz
Dynamic Range	$\geq$ 70 dB
Signal to Noise and Distortion Ratio	$\geq$ 65 dB
Power Consumption	minimize

I looked at Boris Murmann's 2012 ADC survey. His plots are in Figure 1.

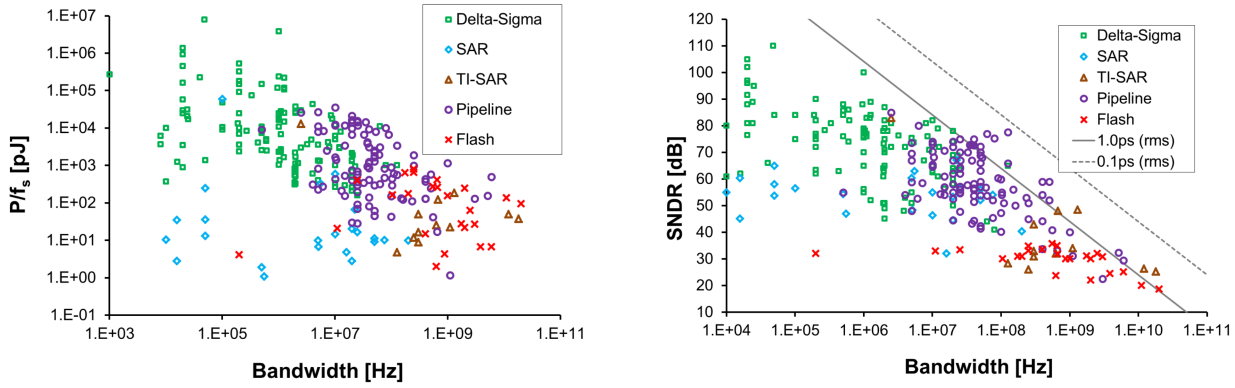

Figure 1: Plots from Murmann's (2012) ADC survey

Clearly a flash architecture cannot reasonably meet the SNDR requirement and would be more suitable for a higher bandwidth requirement. The SAR architecture seems to deliver the best power efficiency, but it looks like the SOTA SAR ADCs cannot achieve a SNDR higher than 70 dB which makes achieving 65 dB a difficult proposition for this architecture.

The dynamic range spec translates to a 12-bit ADC, and scanning the table of ADC papers from Murmann's spreadsheet, either a pipeline or sigma-delta architecture seems appropriate. According to figures from Pavan ("Understanding Delta-Sigma ADCs"), the sigma-delta ADC requires an oversampling ratio of 32-64 for a low-order modulator (2-3) and an OSR of 16-32 for a high-order modulator (4-6) to achieve SQNR above 65 dB. This figure doesn't account for other noise sources from the SC stages used for error feedback, the sampling capacitor, or distortion. This means the ADC has to run at $f_{adc} = 12.5 \cdot 2 \cdot \text{OSR}$ which is 400 - 800 MHz, imposing additional power requirements on the SAH stage to achieve settling time requirements.

In contrast the SAH and gain stages of the pipeline ADC can run at the Nyquist rate, and it should be able to achieve the SNDR spec. I will design a model of a pipeline ADC.