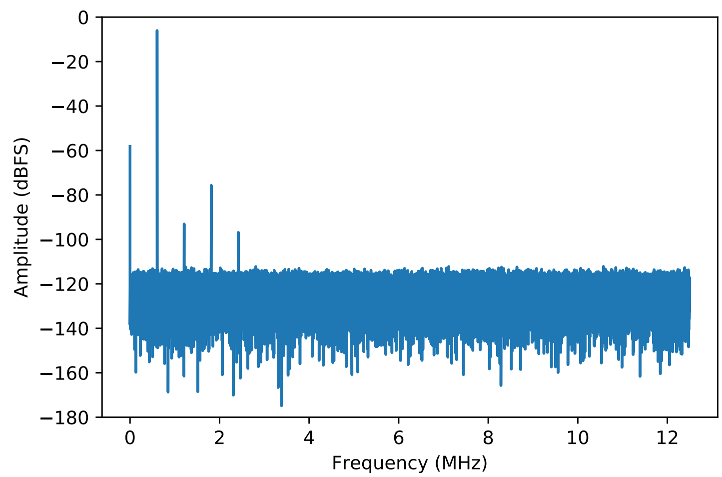
EE 240C Homework 2

Vighnesh Iyer

October 1, 2019

Problem 1: Spectral Analysis

a) Plot the spectrum from 0 to $f_s/2$ using FFT without averaging. The y-axis should be in dBFS while the x axis should be in MHz.



b) What is the frequency f_{in} of the sinusoidal signal at the input of the ADC?

The frequency bin with the maximum amplitude is 3171 which corresponds to a frequency of 0.605 MHz.

c) Compute the following metrics: SNR, SNDR, ENOB, THD, SFDR.

- SNR $= \frac{P_{sig}}{P_{noise}}$ where P_{noise} excludes DC, the signal, and the 2-7th harmonic.
  SNR = 67.9 dB.
- SNDR $= \frac{P_{sig}}{P_{noise}}$ where P_{noise} excludes DC and the signal, but includes the harmonics.
  SNDR = 65.65 dB. This is close to the SNR which makes sense since the harmonics are well below the signal.
- ENOB $= \frac{SNDR(dB)-1.76dB}{6.02dB}$ = 10.6 bits
- THD $= \frac{P_{distortion}}{P_{sig}}$ = -69.5 dB
- SFDR $= \frac{P_{spur,max}}{P_{sig}}$ = 69.6 dB

d) Which non-ideality is limiting the SFDR in this case?

The INL seems to limiting the SFDR. From the equation in lecture $SFDR = 20\log_{10}(2^B/INL)$ which for a 12-bit ADC and 1 LSB of INL equals 72 dB SFDR, which is close to the computed value.

Problem 2: Current Steering DACs

a) To meet the yield requirements for INL and DNL, 2 inequalities can be written. We use 2.6 stddevs as the point for 99% yield.

$$\sigma_{INL} = \frac{1}{2}\sigma_u\sqrt{2^B} = \frac{1}{2}\frac{k_u}{\sqrt{A_{unit}}}\sqrt{2^B}$$
$$2.6\sigma INL < 2 \text{ LSB}$$
$$A_{unit} > \left(\frac{2.6}{2}\frac{k_u\sqrt{2^B}}{2}\right)^2$$

$$\sigma_{DNL} = \sigma_u\sqrt{2^{B_b+1}-1} = \frac{k_u}{\sqrt{A_{unit}}}\sqrt{2^{B_b+1}-1}$$
$$2.6\sigma DNL < 0.5 \text{ LSB}$$
$$A_{unit} > \left(\frac{2.6k_u\sqrt{2^{B_b+1}-1}}{0.5}\right)^2$$

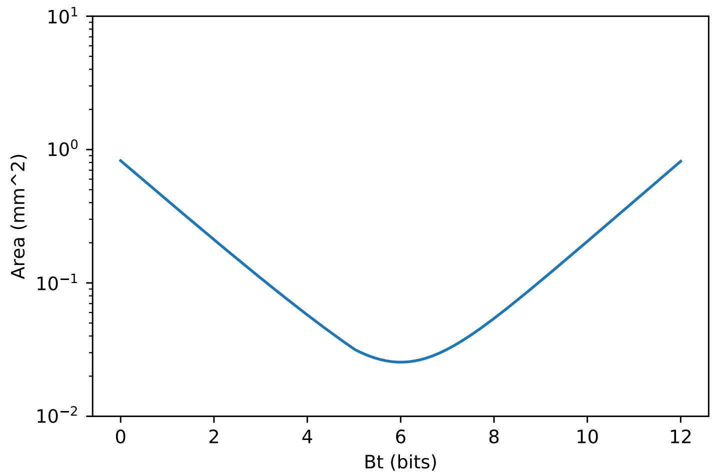
The greater value of A_{unit} from these inequalities will be used to compute the total area. Values of B_b are swept in Python:

```
ku = 0.03
inl_a_unit = lambda B: ((2.6/2) * (ku * np.sqrt(2**B)) / 2)**2
dnl_a_unit = lambda Bb: ((2.6/0.5) * ku * np.sqrt(2**(Bb+1) - 1))**2
for Bb in range(12):
    a_unit_1 = inl_a_unit(12)
    a_unit_2 = dnl_a_unit(Bb)
    a_unit = max(a_unit_1, a_unit_2)
    area = (2**(12-Bb))*200 + (2**12)*a_unit
    print(Bb, area, a_unit)
```

```
0 825579.536384 1.557504
1 415979.536384 1.557504
2 211179.536384 1.557504
3 108779.536384 1.557504
4 57579.536384 1.557504
5 31979.536384 1.557504
6 25459.392512 3.0906719999999996
7 31818.46528 6.20568
8 54136.61081599999 12.435695999999998
9 103572.90188800002 24.895728000000005
10 204845.48403199998 49.815791999999995
11 408590.64832 99.65592
```

The optimal point is at $B_b = 6$ and $B_t = 6$.

b) I used the same script as above to generate data to make the plot.



Flash ADC

6-bit flash ADC with ideal resistor string and $V_{ref} = 1.8$V. $\sigma_{offset} = 3$ mV. First and last preamp have no offset.

a) Find $\sigma_{DNL}, \sigma_{INL}$

From a Maxim document:

$$DNL(D) = \left| \frac{V_{D+1} - V_D}{V_{lsb,ideal}} - 1 \right|$$

where V_D is the input voltage at which the digital output code transitions to D. DNL is defined for $0 < D < 2^N - 2$. The comparator offset can be added to each term of V_D:

$$\begin{aligned}
DNL(d) &= \left| \frac{(V_{D+1} + V_{off,D+1}) - (V_D + V_{off,D})}{V_{lsb,ideal}} - 1 \right| \\
\sigma^2_{DNL} &= E[DNL^2] - E[DNL]^2 \\
E[DNL]^2 &= 0 \\
E[DNL^2] &\to \left(\frac{(V_{D+1} + V_{off,D+1}) - (V_D + V_{off,D})}{V_{lsb,ideal}} - 1 \right)^2 \\
&= \left(\frac{V_{lsb} + V_{off,D+1} - V_{off,D} - V_{lsb}}{V_{lsb}} \right)^2 \\
&= \left(\frac{V_{off,D+1} - V_{off,D}}{V_{lsb}} \right)^2 \\
&= \frac{V^2_{off,D+1} - 2V_{off,D+1}V_{off,D} + V^2_{off,D}}{V^2_{lsb}} \\
&\to \frac{E[V^2_{off,D+1}] - 2E[V_{off,D+1}V_{off,D}] + E[V^2_{off,D}]}{V^2_{lsb}} \\
&= \frac{2\sigma^2_{offset}}{V^2_{lsb}} \\
\sigma_{DNL} &= \sqrt{2}\frac{\sigma_{offset}}{V_{lsb}} = \sqrt{2}\frac{3 \text{ mV}}{1.8/2^6} = 0.151 \text{ LSB}
\end{aligned}$$

From a Maxim document:

$$INL(D) = \left| \frac{V_D - V_{zero}}{V_{lsb}} - D \right|$$

where V_D is the analog value for output code D and D ranges from $0 < D < 2^N - 1$. V_{zero} is the minimum analog input for an all zero output code, which in our case is 0 V.

Adding an offset:

$$\begin{aligned}
INL(D) &= \left| \frac{V_{D,nom} + V_{off} - DV_{lsb}}{V_{lsb}} \right| \\
V_{D,nom} &= V_{lsb}D \\
INL(D) &= \left| \frac{DV_{lsb} + V_{off} - DV_{lsb}}{V_{lsb}} \right| \\
&= \left| \frac{V_{off}}{V_{lsb}} \right| \\
\sigma_{INL} &= \frac{\sigma_{offset}}{V_{lsb}} = 0.11 \text{ LSB}
\end{aligned}$$

b) How are σ_{DNL} and σ_{INL} affected by 4x interpolation ($M = 4$)?

The effective offset of the preamps is divided by the interpolation factor, so both σ_{INL} and σ_{DNL} should be reduced by 4x.

kT/C Noise