IEEE SOLID-STATE CIRCUITS SOCIETY
Where ICs are in IEEE

Solid-State Circuits Society

"Where ICs are in the IEEE"

Professional Organization

- 10,000 members
- 70+ chapters located worldwide
- Foster information exchange in electronics
  - Distinguished Lectures
  - Online tutorials
  - International and regional conferences
  - Journals & magazines
- Part of IEEE with 400,000 members

IEEE SOLID-STATE CIRCUITS SOCIETY
Where ICs are in IEEE

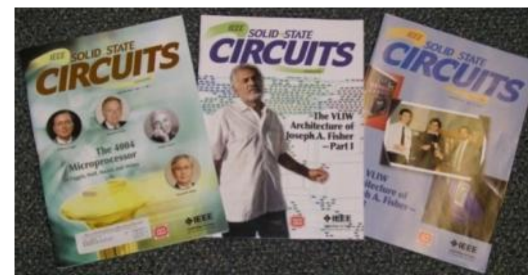
Publications & Conferences

Journal of Solid-State Circuits (JSSC)

- #1 technical source for circuits
- Most downloaded IEEE journal articles
- Top cited reference in US Patent applications

Solid-Sate Circuits Magazine

- Discusses historical milestones, trends and future developments
- Articles by leaders from industry and academia in a tutorial and editorial style



International and Regional Conferences

- 4 International Sponsored Conferences
- Technically co-sponsored conferences

ISSCC
A-SSCC
IEEE Asian Solid-State Circuits Conference
CICC
IEEE Custom Integrated Circuits Conference
VLSI
CIRCUITS SYMPOSIUM

Chapter & DL Events

Swedish SOC Conference (May 2011)

Annual SSCS DL Tour

Individual DL Presentations

SSCS-Italy: International Analog VLSI Workshop (September 2011)

Why join IEEE and SSCS?

Knowledge …

staying current with the fast changing world of solid-state circuit technology

Community …

local and global activities, unparalleled networking opportunities, chapter activities, electing IEEE SSCS leadership

Profession …

empowering members to build and own their careers, mentoring, making the world a better place

Recognition …

Best Paper Awards, IEEE Fellow & Field Awards, Student Travel Grants & Pre-doctoral Achievement Award …

Getting Involved

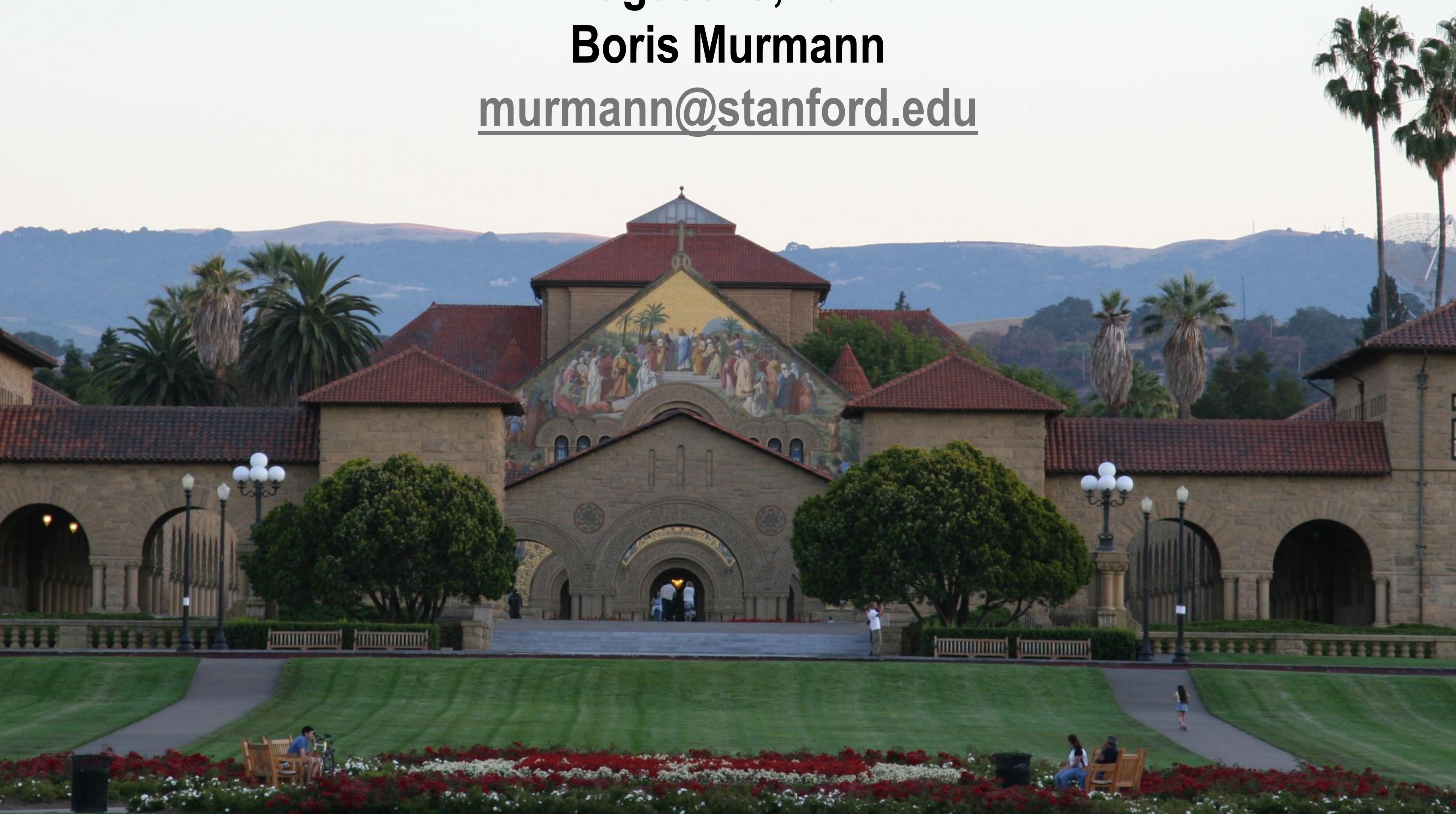
- Organize chapter events
- Participate in & organize conferences
- As an author
- As a reviewer
- Compete in a student design contest
- Nominate senior members & fellows

Energy Limits in A/D Converters

August 29, 2012

Boris Murmann

murmann@stanford.edu



A/D Converter ca. 1954

- 19" × 15" × 26"
- 150 lbs
- 500W
- $8,500.00

P/f_s = 500W/50kS/s = 10mJ

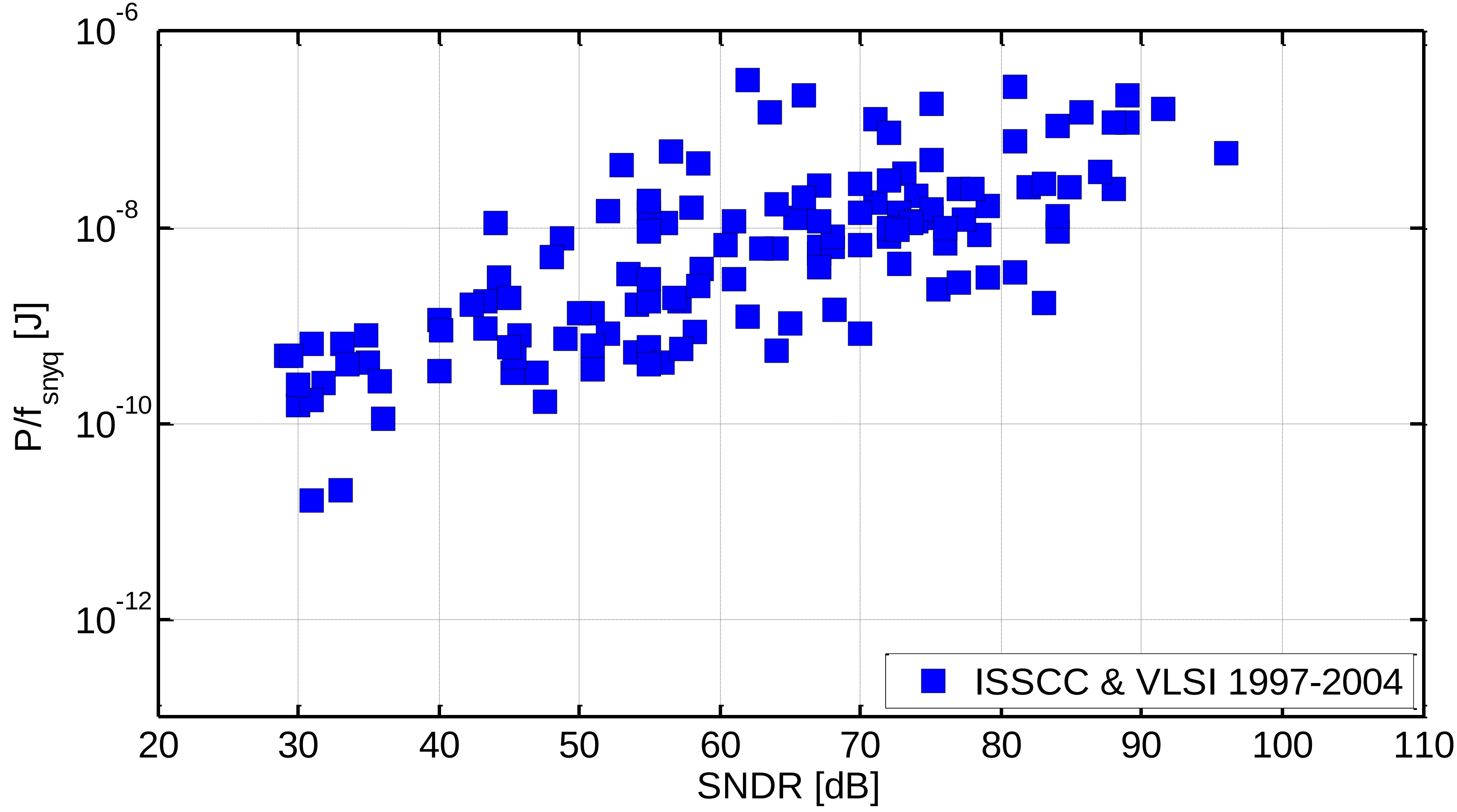
Courtesy,
Analogic Corporation
8 Centennial Drive
Peabody, MA 01960

http://www.analogic.com

Figure 4.3: *1954 "DATRAC" 11-bit, 50-kSPS SAR ADC*
Designed by Bernard M. Gordon at EPSCO

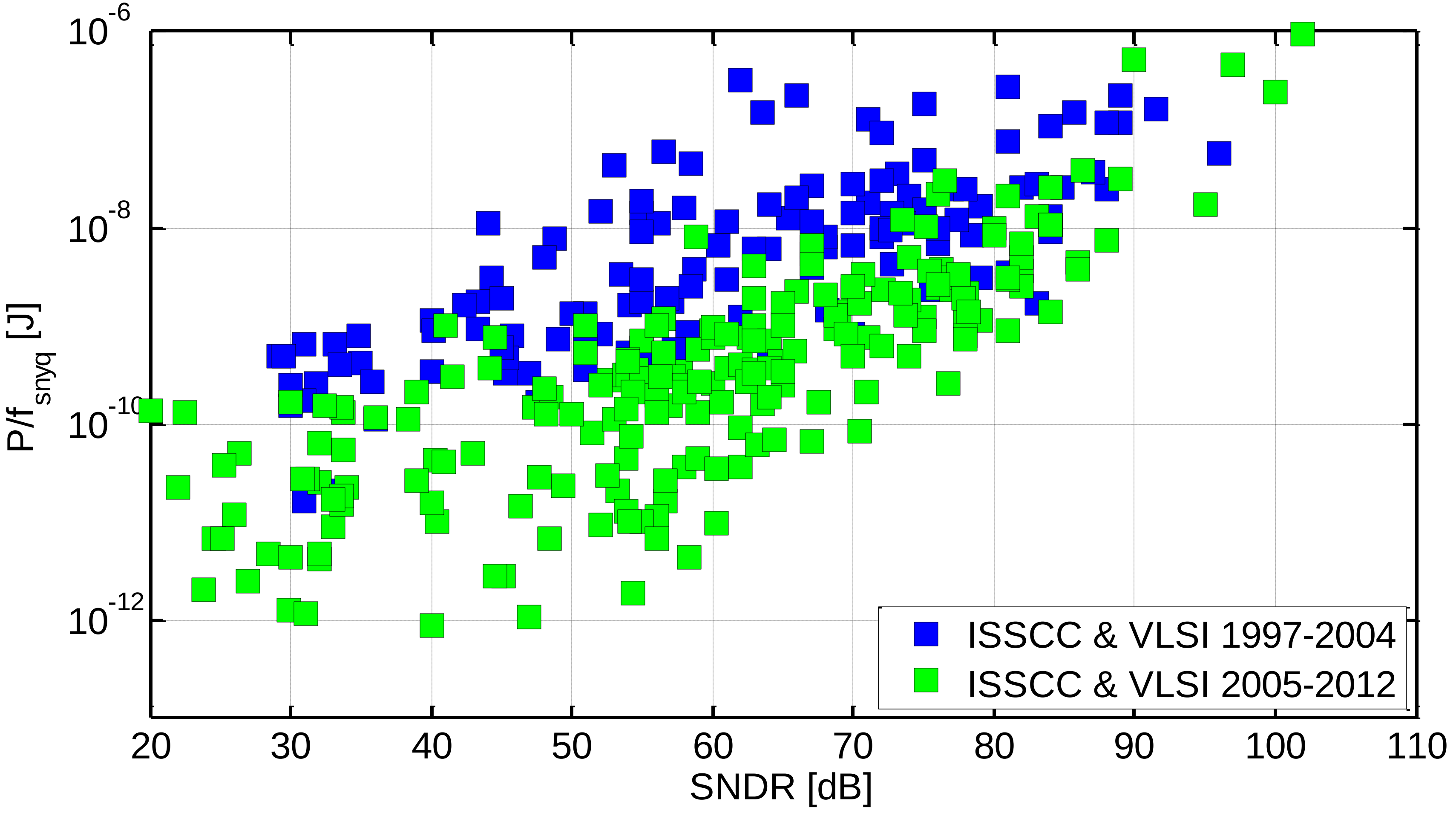
http://www.analog.com/library/analogDialogue/archives/39-06/data_conversion_handbook.html

ADC Landscape in 2004



B. Murmann, "ADC Performance Survey 1997-2012," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html

ADC Landscape in 2012



B. Murmann, "ADC Performance Survey 1997-2012," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html

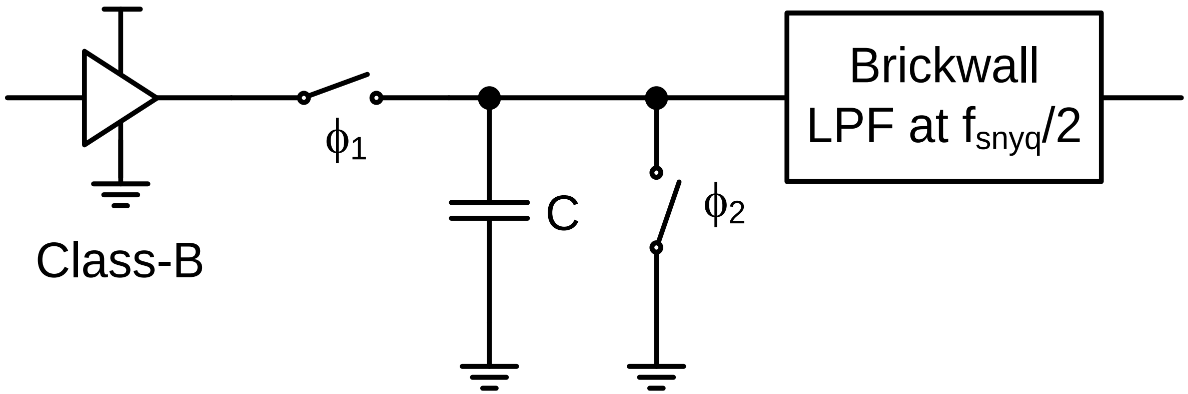
Observation

- ADCs have become substantially "greener" over the years
- Questions
  - How much more improvement can we hope for?
  - What are the trends and limits for today's popular architectures?
  - Can we benefit from further process technology scaling?

Outline

- **Fundamental limit**
- **General trend analysis**
- **Architecture-specific analysis**
  - **Flash**
  - **Pipeline**
  - **SAR**
  - **Delta-Sigma**
- **Summary**

Fundamental Limit



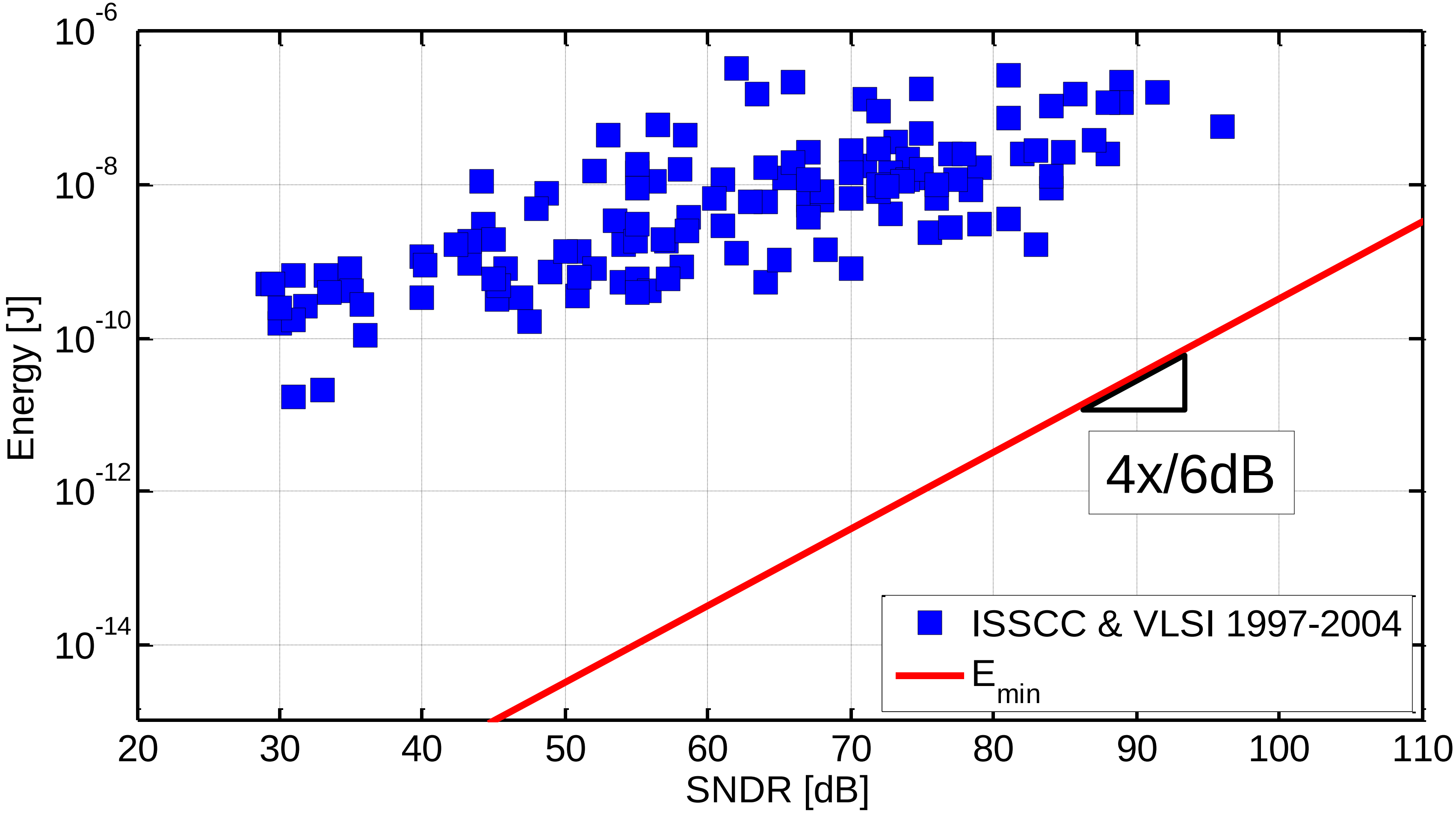
$$\mathrm{SNR} = \frac{\frac{1}{2}\left(\frac{V_{FS}}{2}\right)^2}{\frac{kT}{C}} \underbrace{\frac{f_s}{f_{snyq}}}_{\text{OSR}}$$

$$P_{min} = CV_{FS}f_s \cdot V_{DD} \qquad V_{DD} = V_{FS}$$

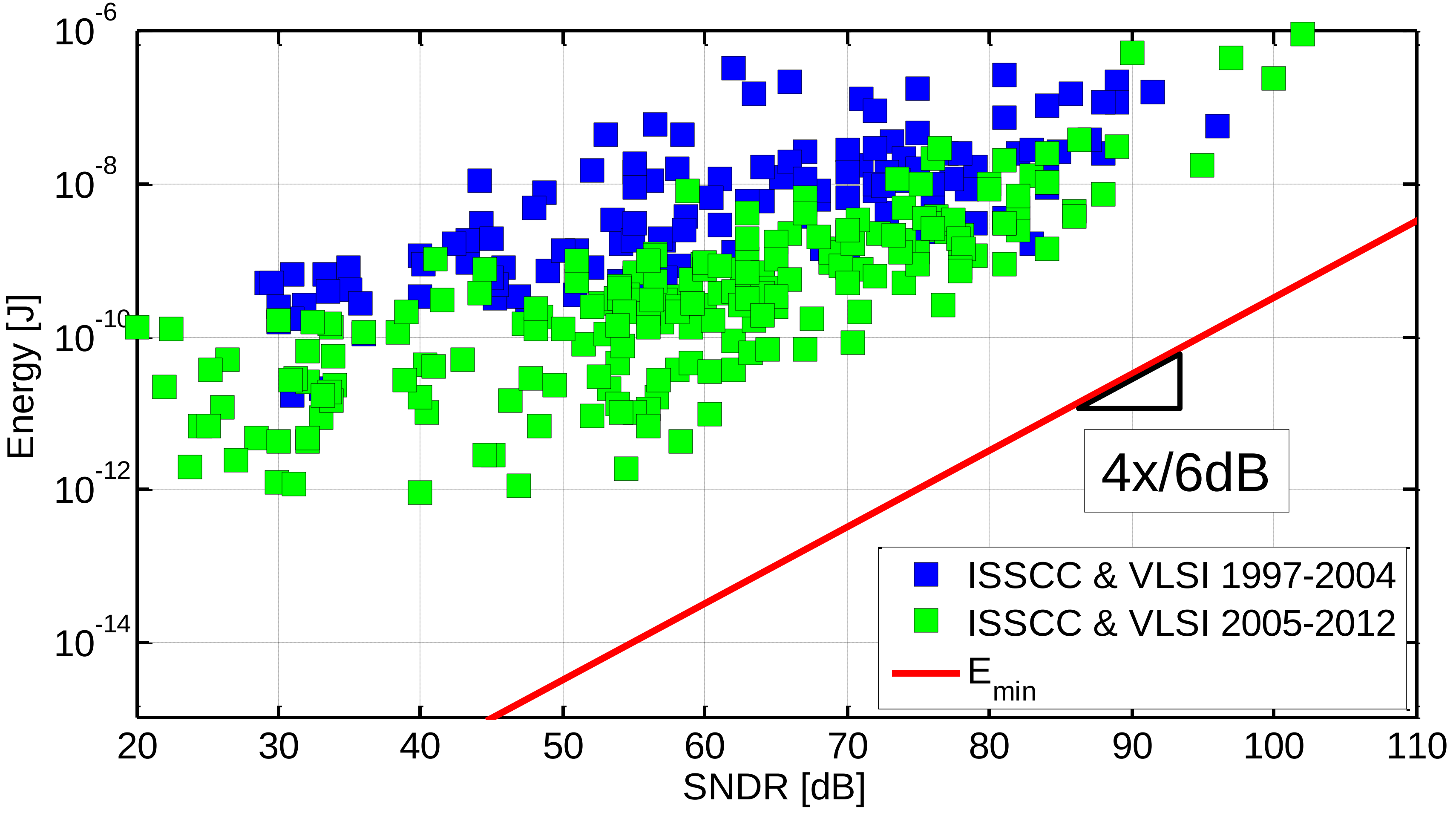
$$\boxed{E_{min} = \frac{P_{min}}{f_{snyq}} = 8kT \cdot \mathrm{SNR}}$$

[Hosticka, Proc. IEEE 1985; Vittoz, ISCAS 1990]

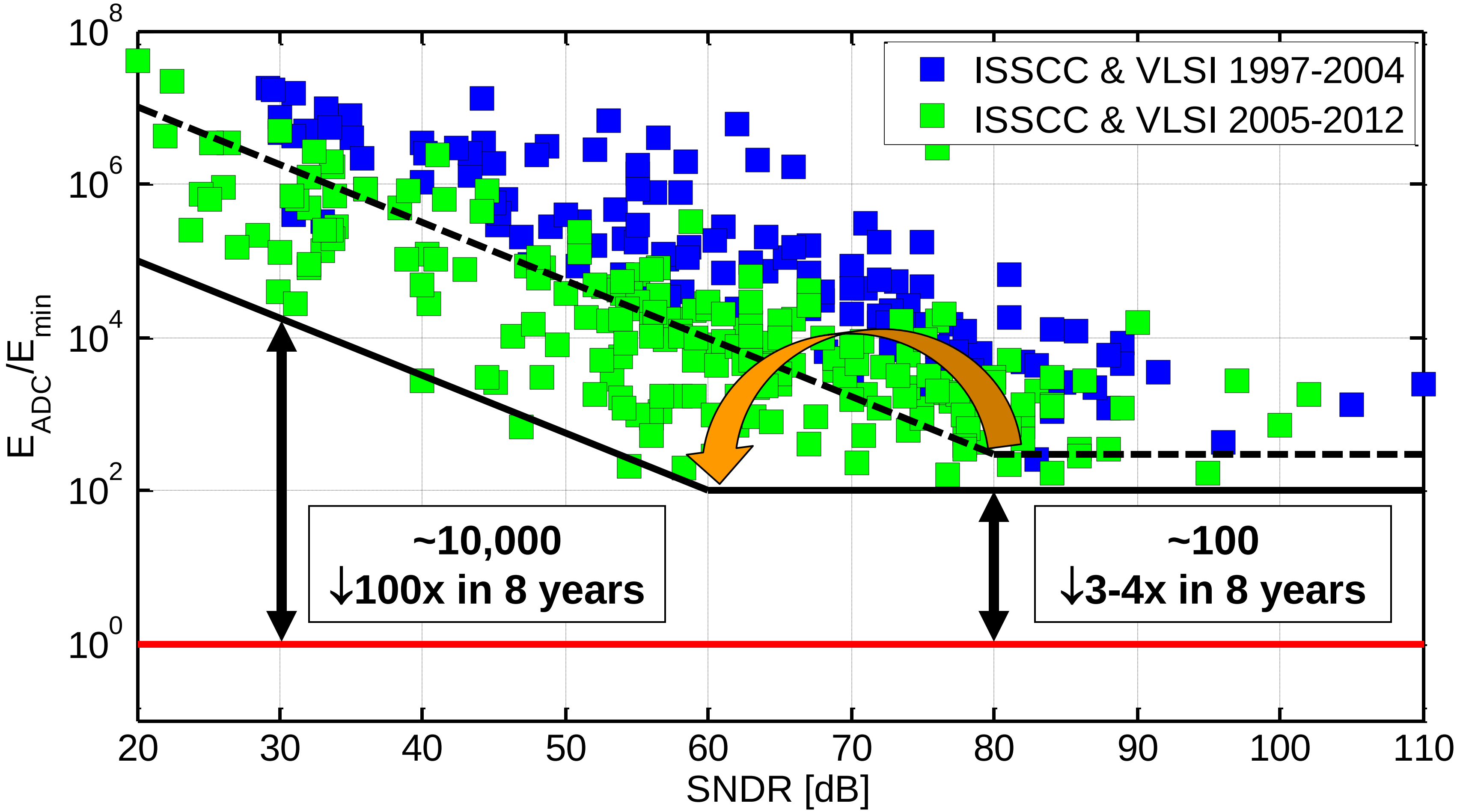
ADC Landscape in 2004



ADC Landscape in 2012



Normalized Plot



Aside: Figure of Merit Considerations

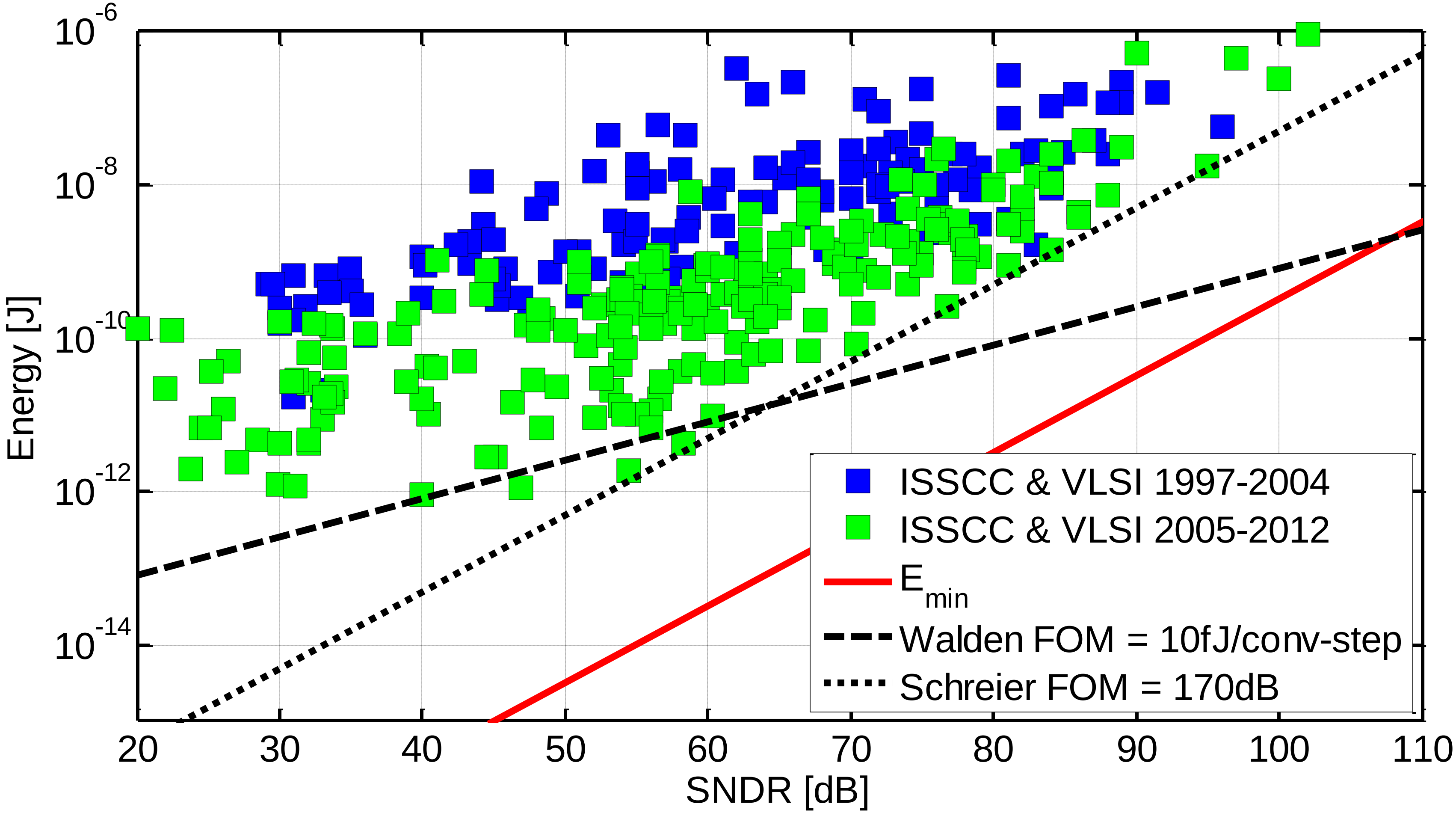
- **There are (at least) two widely used ADC figures of merit (FOM) used in literature**
- **Walden FOM**
  - **Energy increases 2x per bit (ENOB)**
  - **Empirical**

$$\boxed{\mathrm{FOM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \cdot f_{snyq}}}$$

- **Schreier FOM**
  - **Energy increases 4x per bit (DR)**
  - **Thermal**
  - **Ignores distortion**

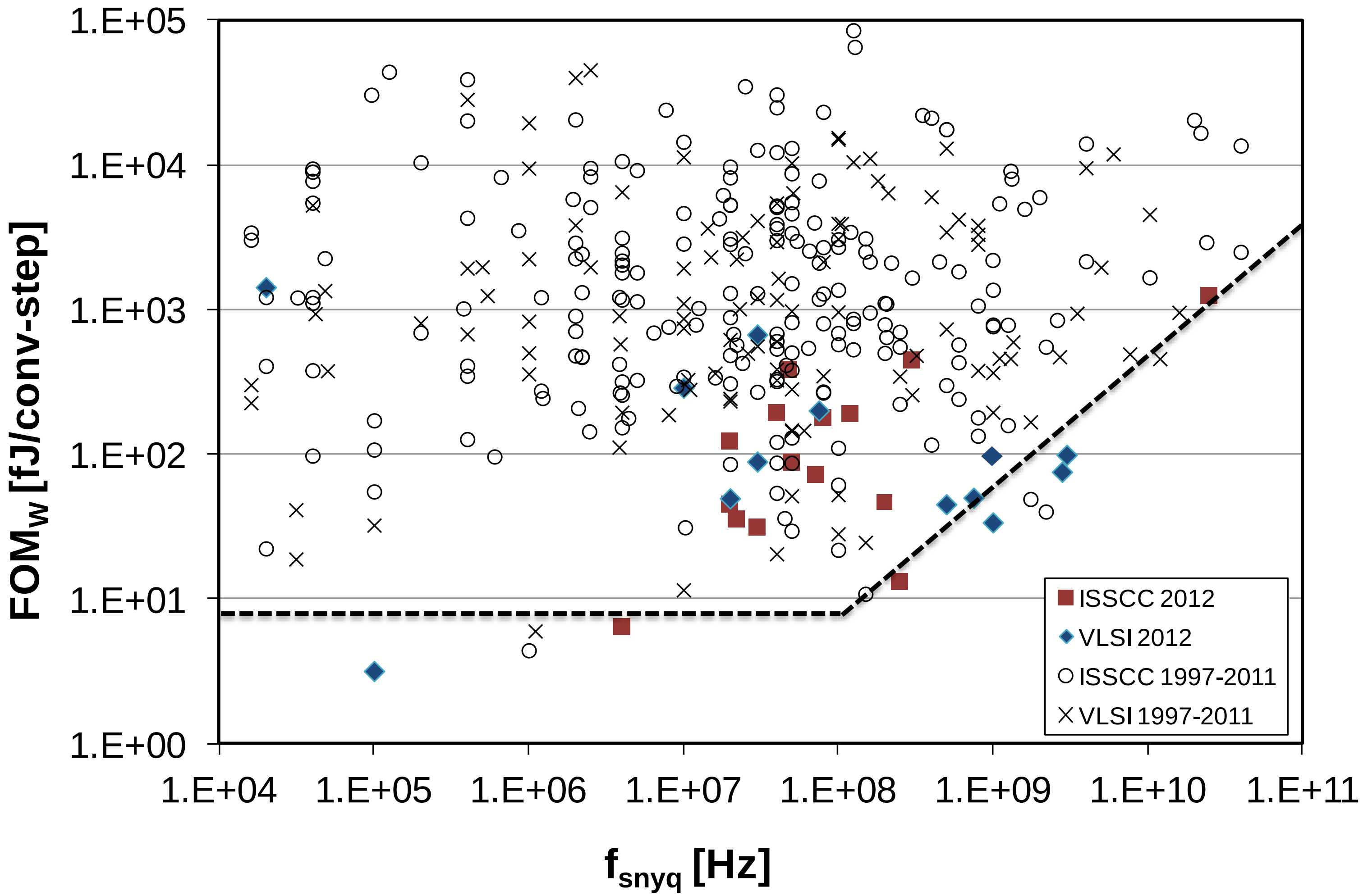
$$\boxed{\mathrm{FOM} = \mathrm{DR(dB)} + 10\log\left(\frac{\mathrm{BW}}{\mathrm{P}}\right)}$$

FOM Lines



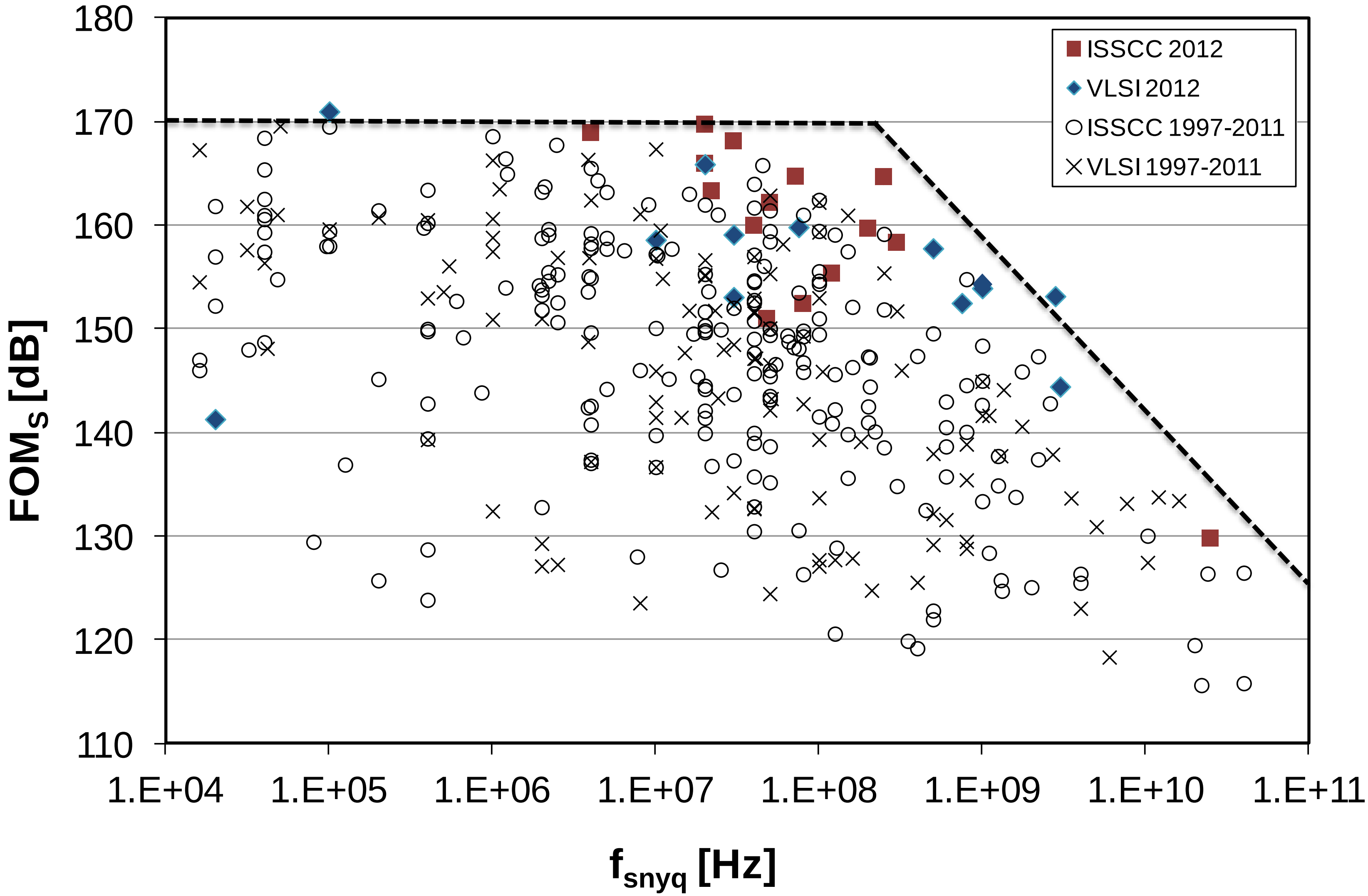
- **Best to use thermal FOM for designs above 60dB**

Walden FOM vs. Speed

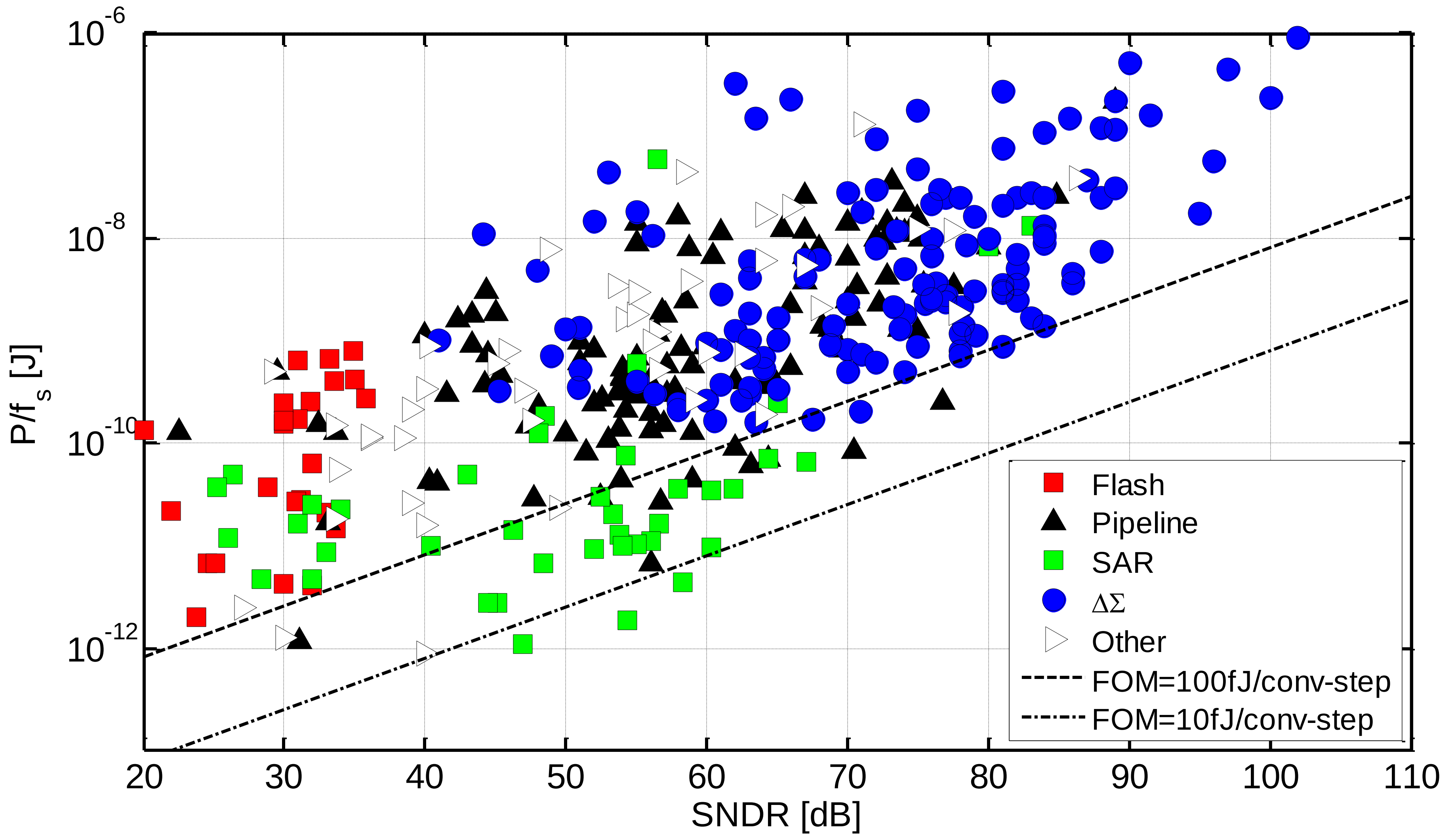


- **FOM "corner" around 100…300MHz**

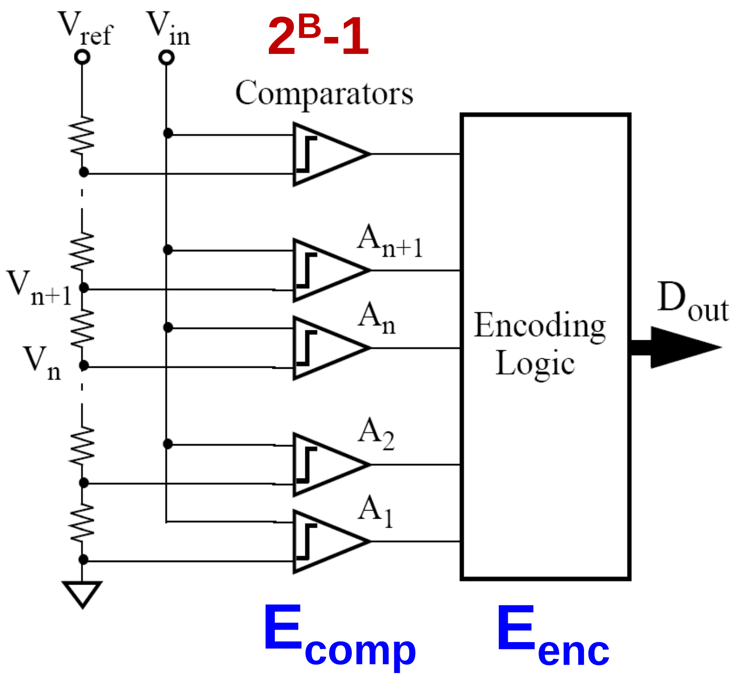
Schreier FOM vs. Speed

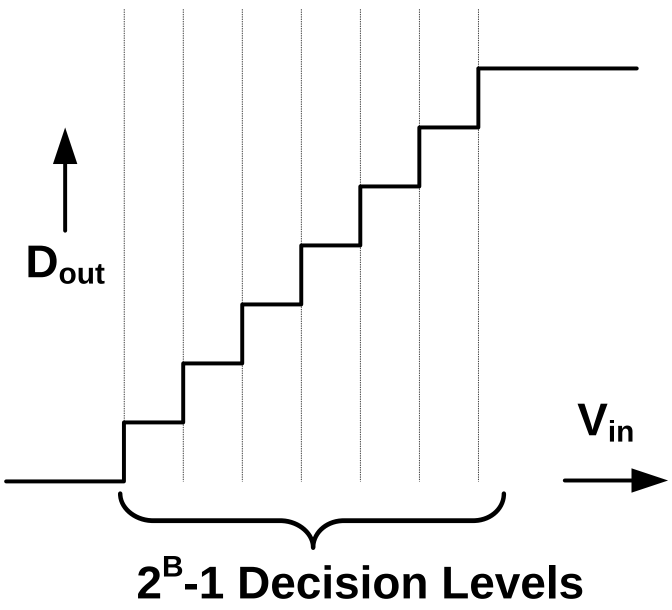


Energy by Architecture



Flash ADC

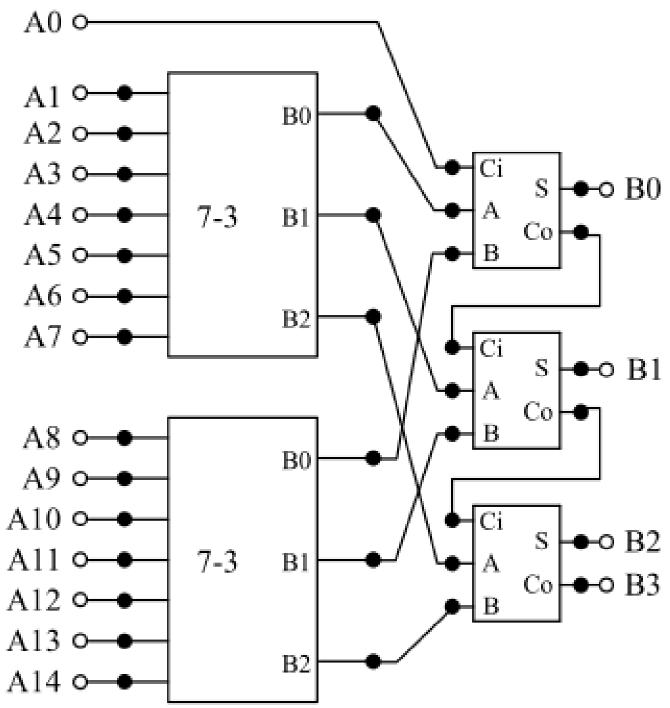




- **High Speed**
  - **Limited by single comparator plus encoding logic**
- **High complexity, high input capacitance**
  - **Typically use for resolutions up to 6 bits**

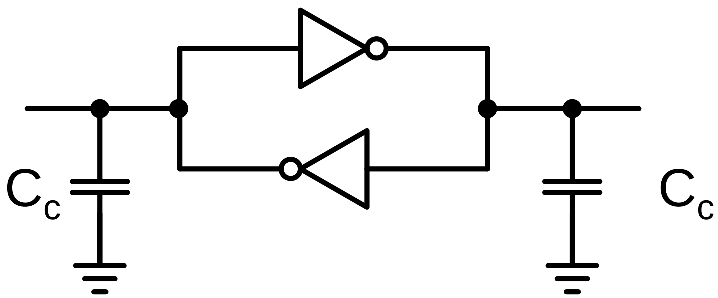
Encoder

- **Assume a Wallace encoder ("ones counter")**
- **Uses ~2^B–B full adders, equivalent to ~ 5·(2^B–B) gates**



$$E_{enc} \cong 5 \cdot \left(2^B - B\right) \cdot E_{gate}$$

Matching-Limited Comparator



Simple Dynamic Latch

Assuming C_{cmin} = 5fF
for wires, clocking, etc.

$$\sigma_{VOS}^2 \cong \frac{A_{VT}^2}{WL} = A_{VT}^2 \frac{C_c}{C_{ox}}$$

Offset

$$C_c = \frac{A_{VT}^2 C_{ox}}{\sigma_{VOS}^2} + C_{c\,min}$$

Required capacitance

$$3\sigma_{VOS} = \frac{1}{4}\frac{V_{inpp}}{2^B}$$

Confidence interval

$$B \cong \frac{SNR[dB]+3}{6}$$

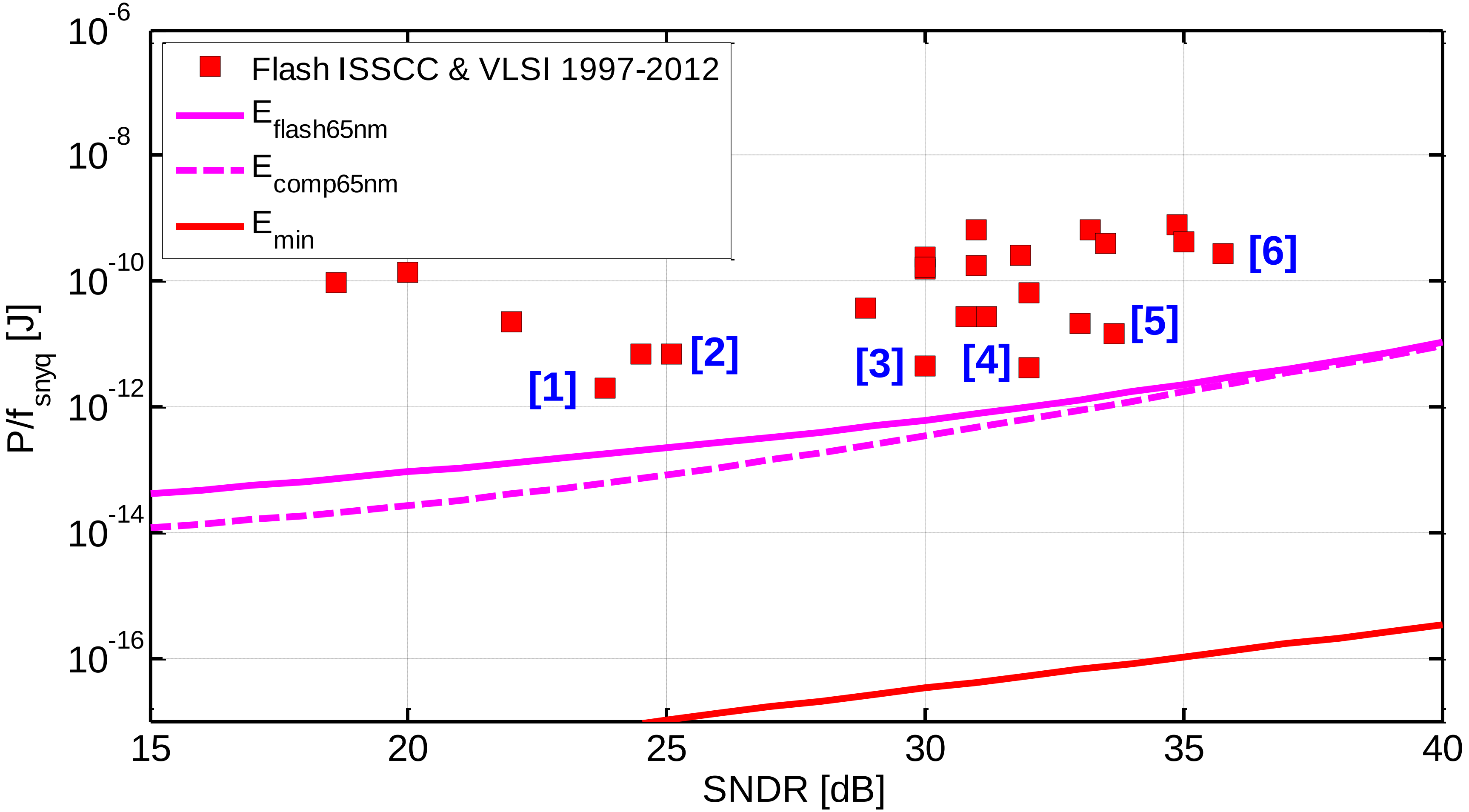
3dB penalty accounts for "DNL noise"

$$E_{comp} \cong \left(144 \cdot 2^{2B} \cdot \underbrace{C_{ox}A_{VT}^2}_{\text{Matching Energy}} \cdot \frac{V_{DD}^2}{V_{inpp}^2} + C_{c\,min}V_{DD}^2\right) \cdot \left(2^B - 1\right)$$

Typical Process Parameters

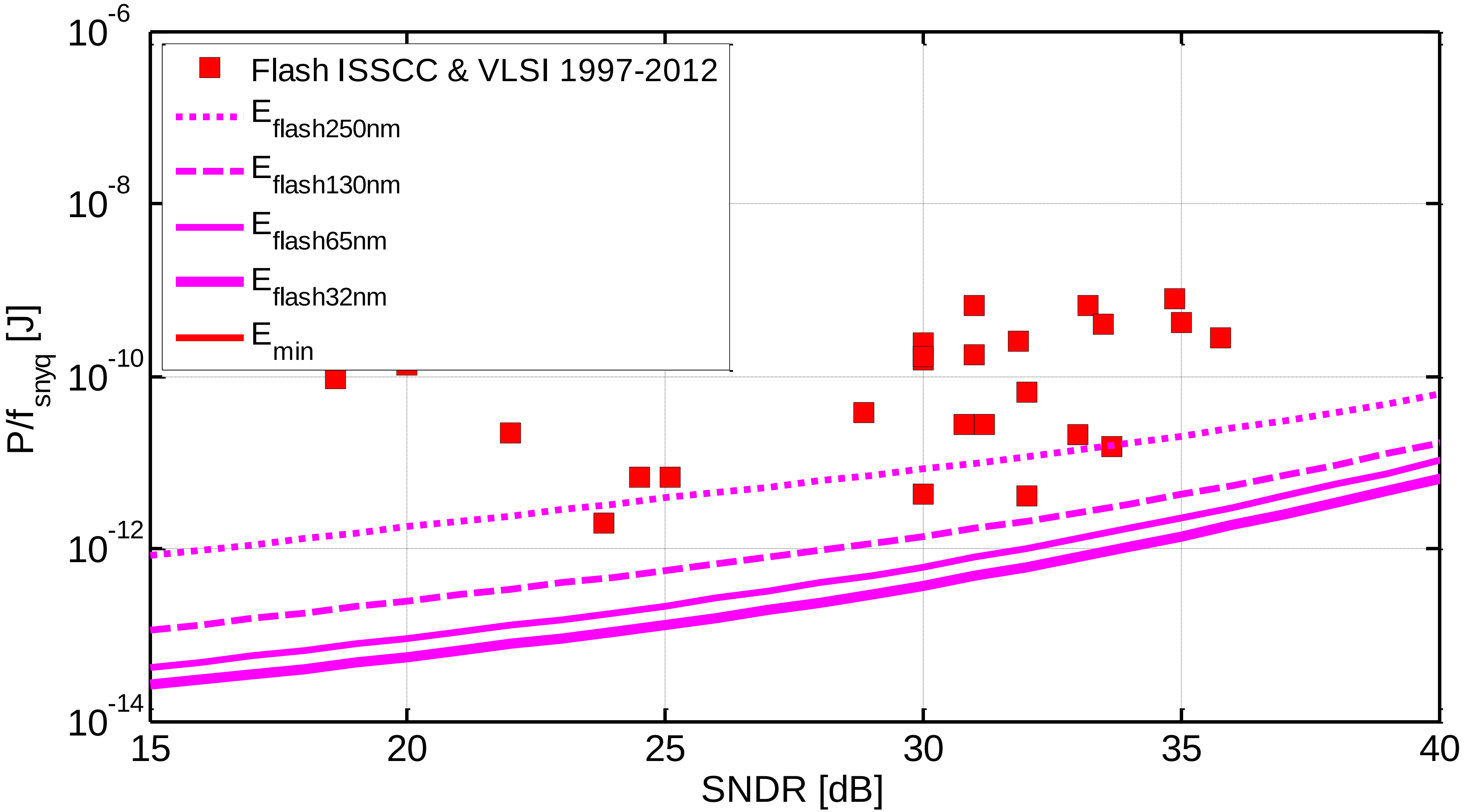
Process [nm]	A_{VT} [mV-μm]	C_{ox} [fF/μm²]	$A_{VT}^2 C_{ox}/kT$	E_{gate} [fJ]
250	8	9	139	80
130	4	14	54	10
65	3	17	37	3
32	1.5	43	23	1.5

Comparison to State-of-the-Art

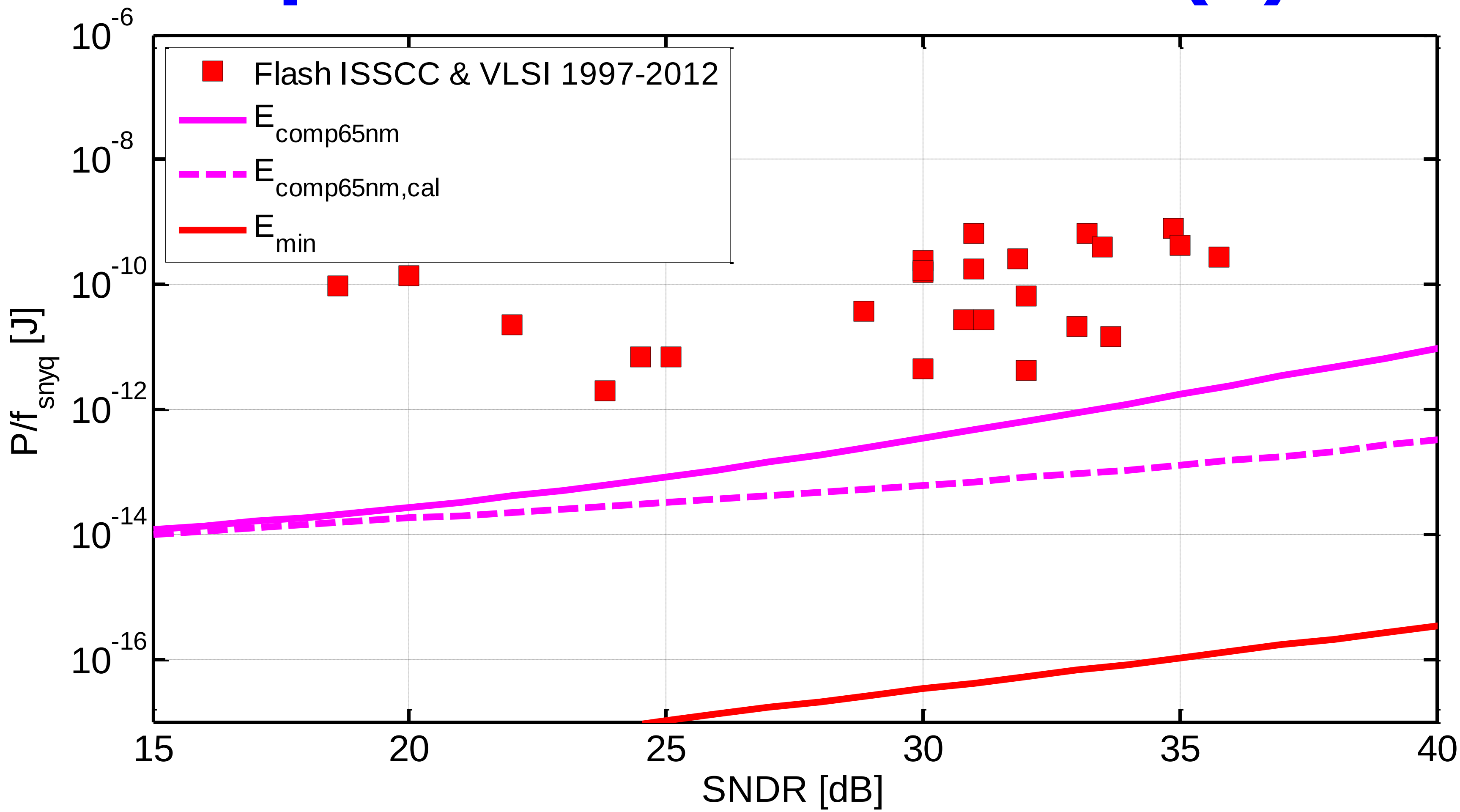


[1] Van der Plas, ISSCC 2006
[2] El-Chammas, VLSI 2010
[3] Verbruggen, VLSI 2008
[4] Daly, ISSCC 2008
[5] Chen, VLSI 2008
[6] Geelen, ISSCC 2001 (!)

Impact of Scaling



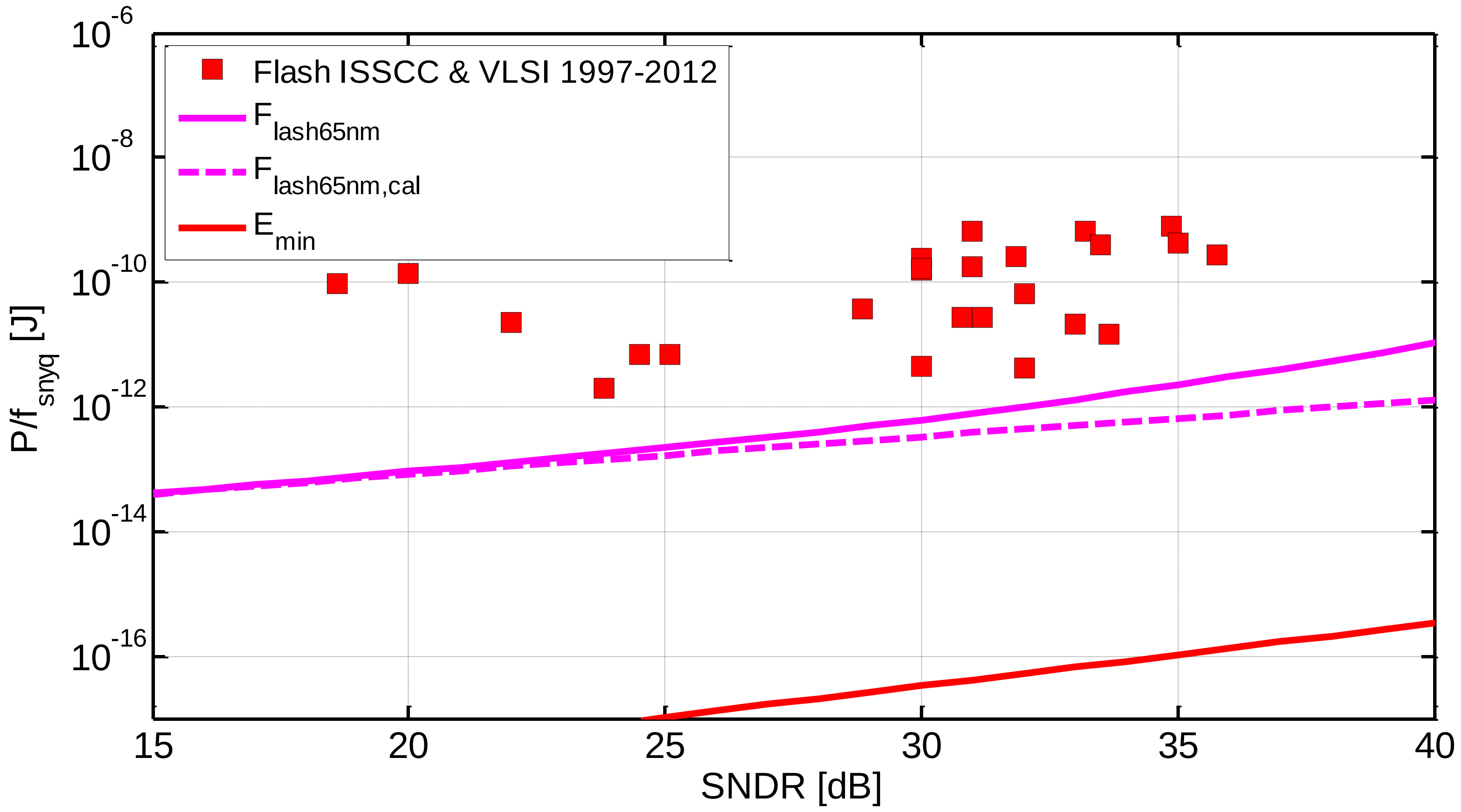
Impact of Calibration (1)



- **Important to realize that only comparator power reduces**

$$3\sigma_{VOS} = \frac{1}{4}\frac{V_{inpp}}{2^{B-B_{cal}}} \qquad B_{cal} \cong 3$$

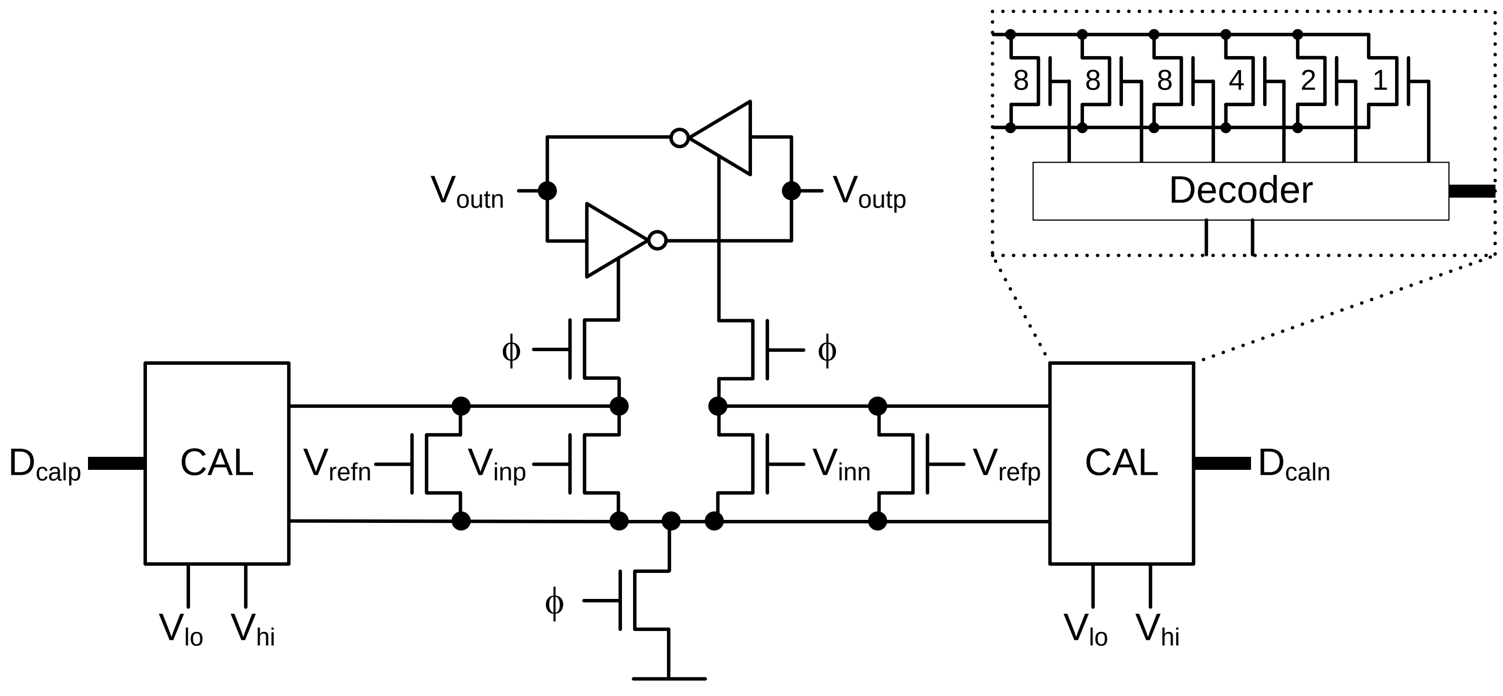
Impact of Calibration (2)



Ways to Approach E_{min} (1)

- **Offset calibrate each comparator**
  - **Using trim-DACs**

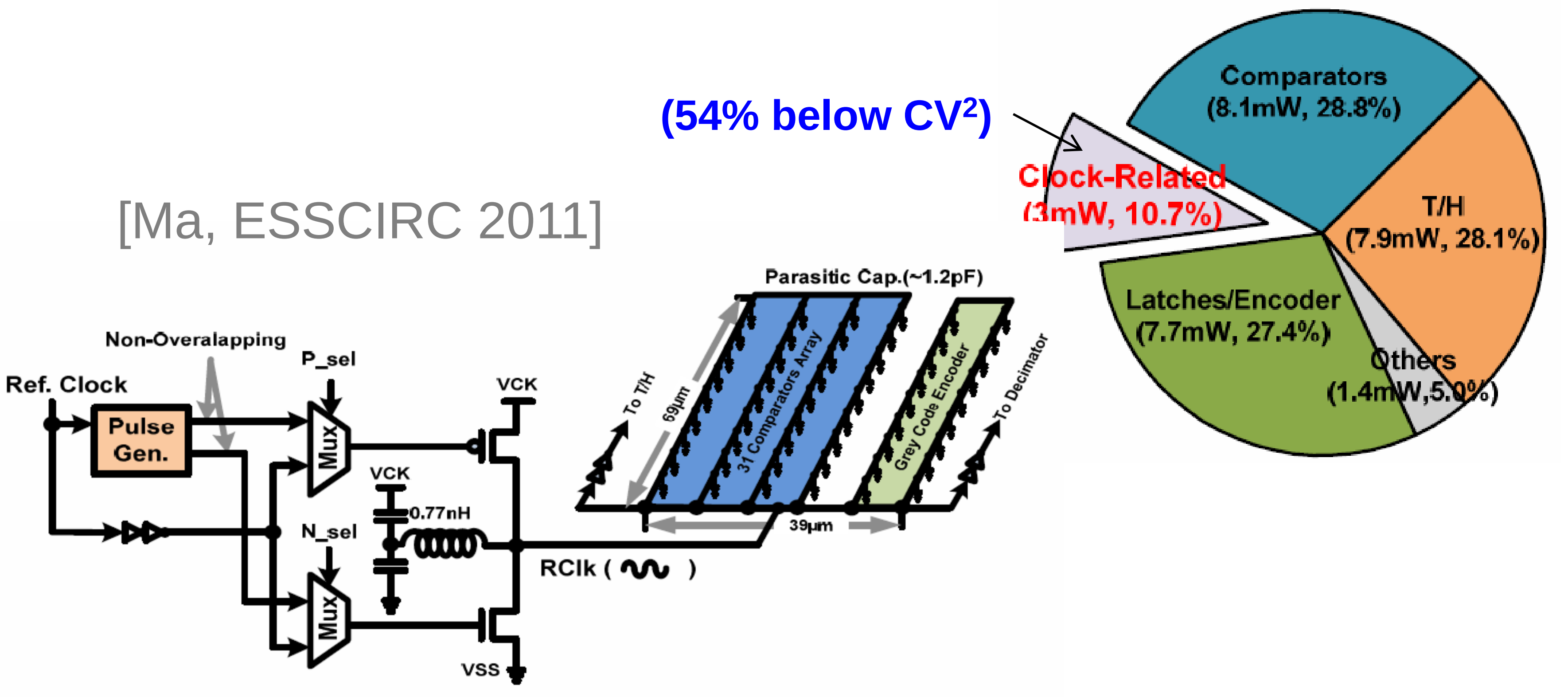
[El-Chammas, VLSI 2010]



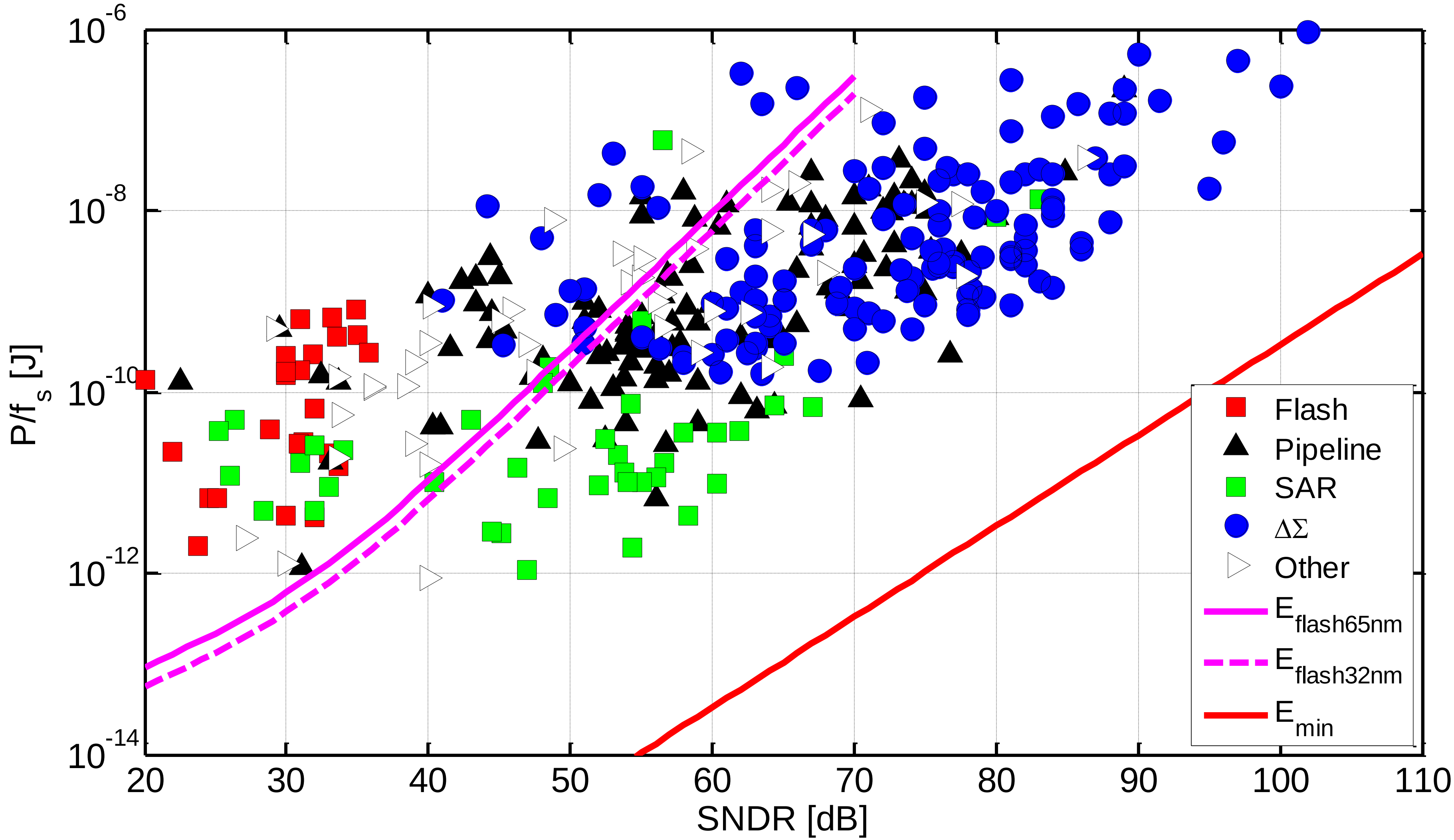
Ways to Approach E_{min} (2)

- **Find ways to reduce clock power**
- **Example: resonant clocking**

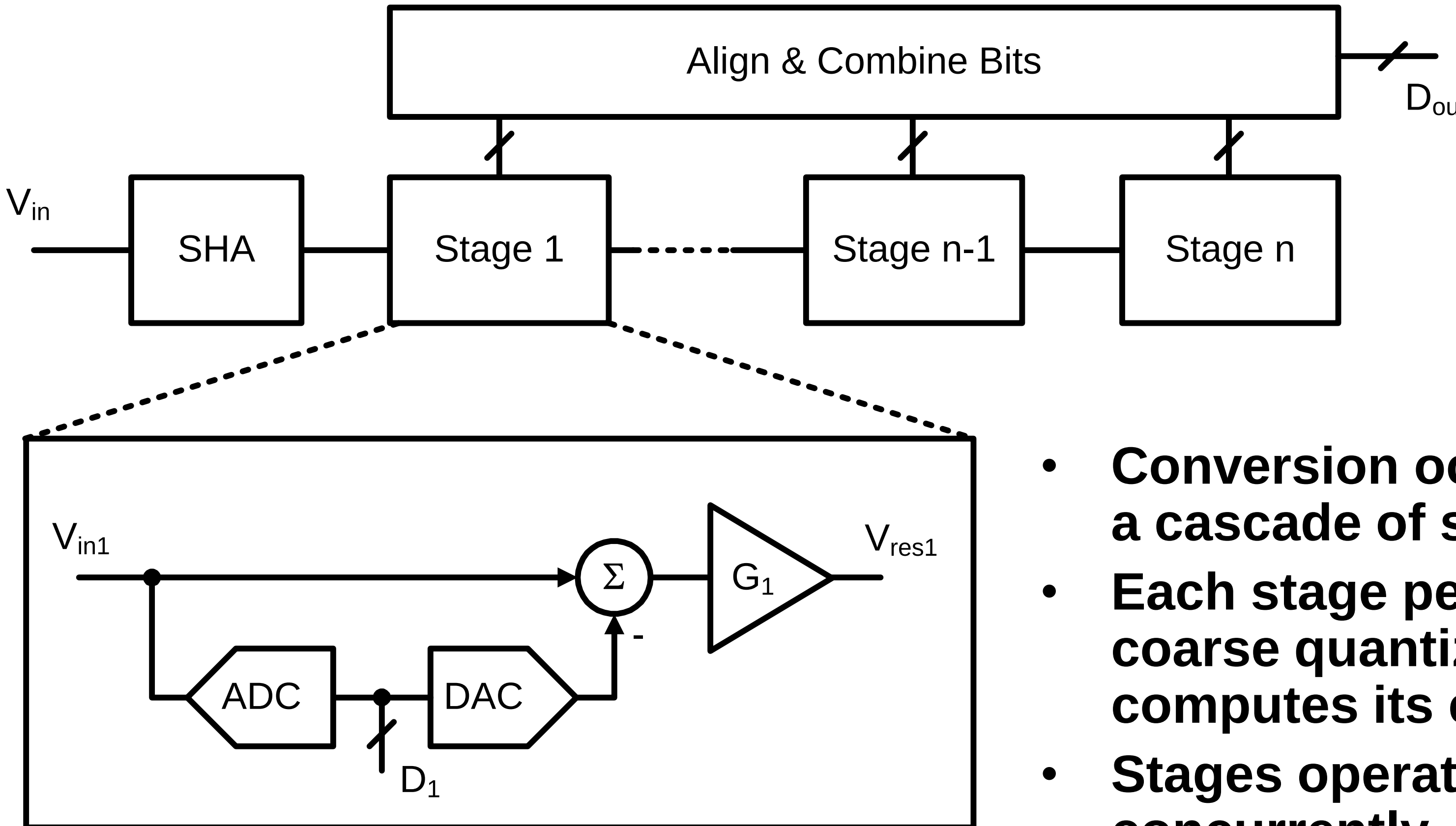
[Ma, ESSCIRC 2011]



Raison D'Être for Architectures Other than Flash…

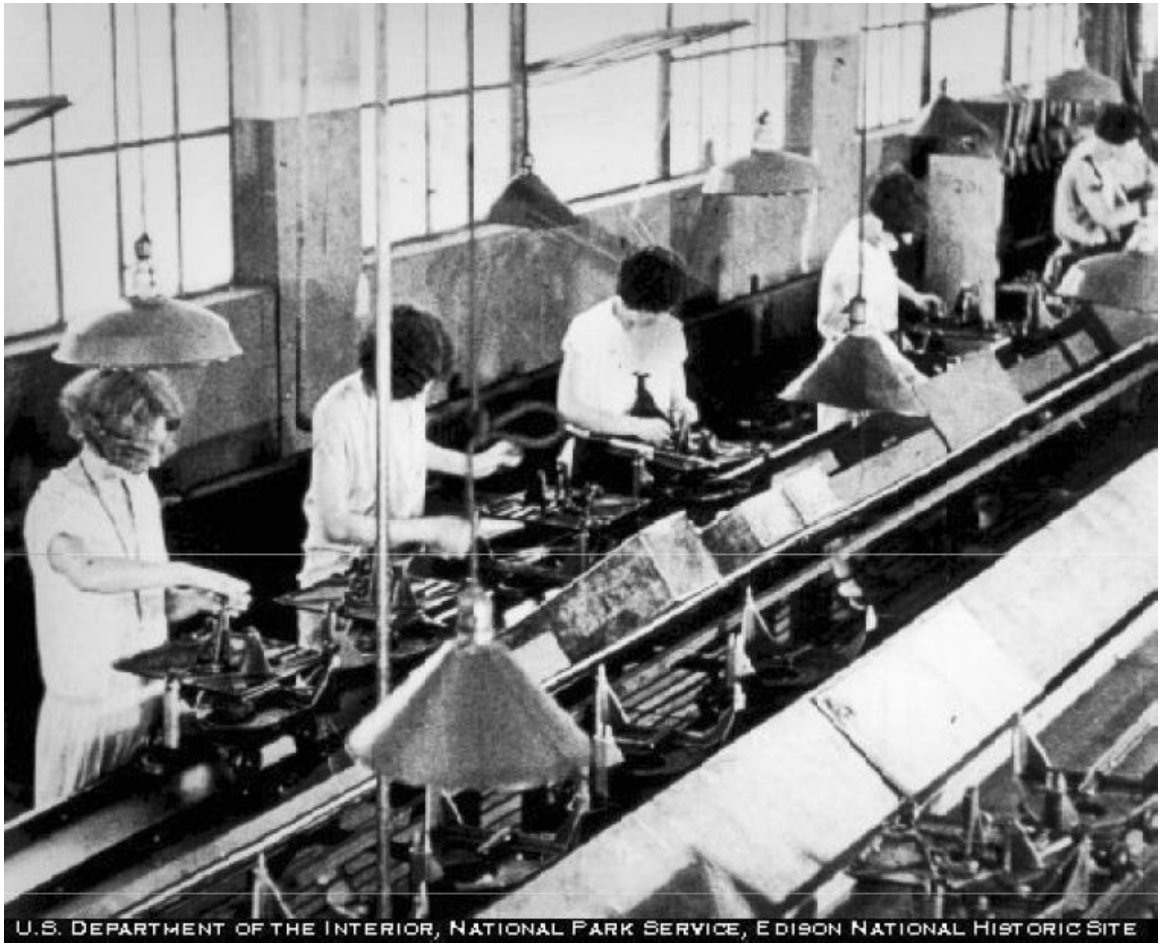


Pipeline ADC



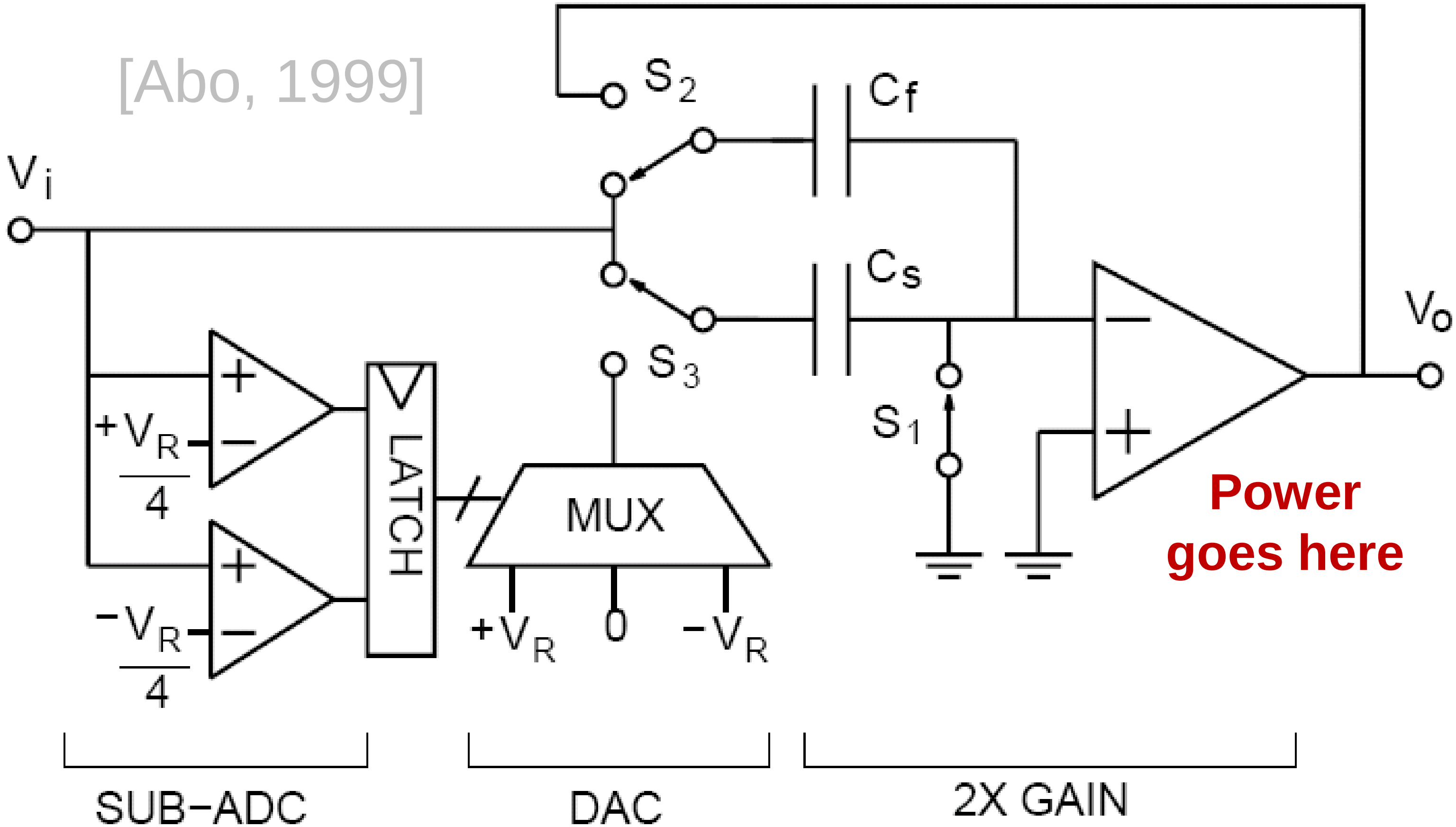
- Conversion occurs along a cascade of stages
- Each stage performs a coarse quantization and computes its error (V_{res})
- Stages operate concurrently
  - Throughput is set by the speed of one single stage

Pipelining – A Very Old Idea



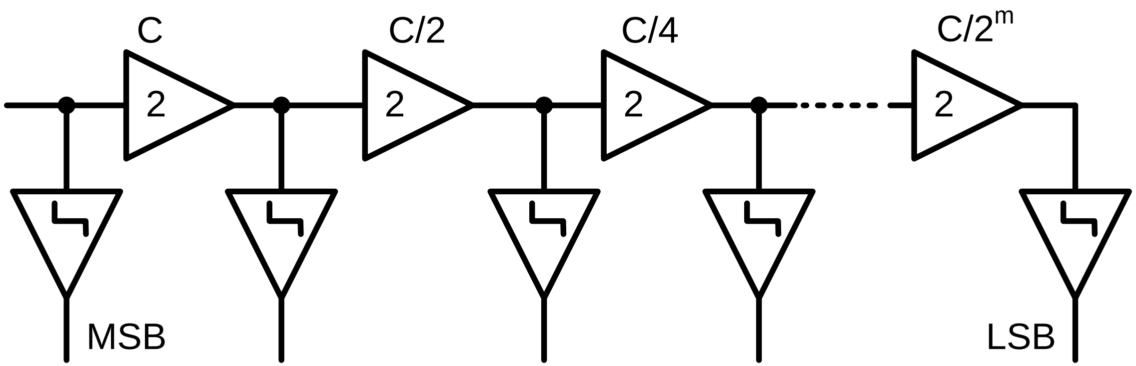
Typical Stage Implementation

[Abo, 1999]



Power goes here

Simplified Model for Energy Calculation

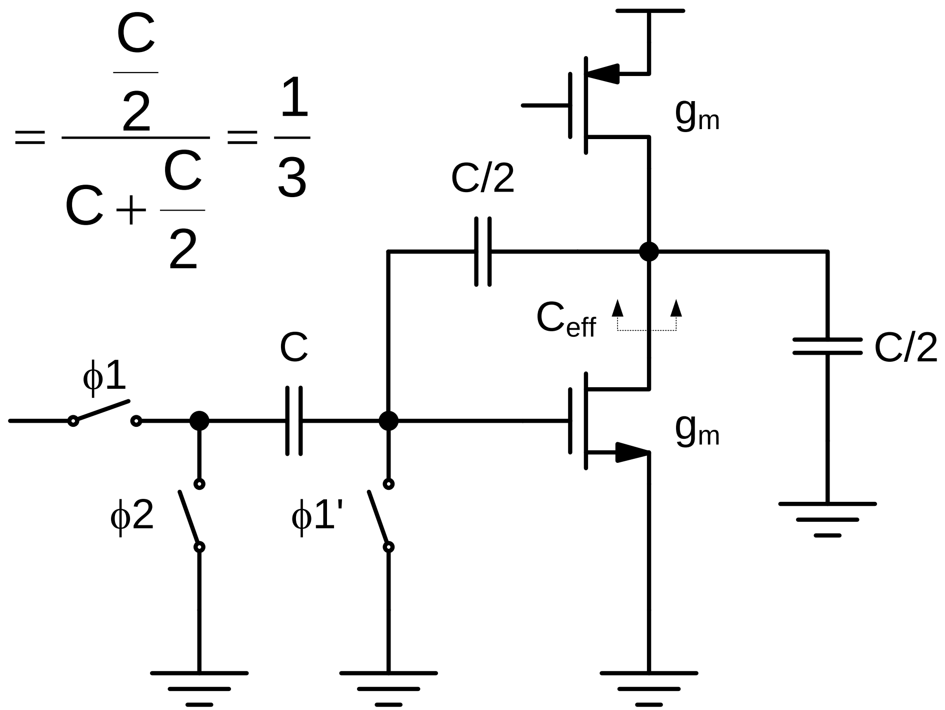


- **Considering the most basic case**
  - **Stage gain = 2 → 1 bit resolution per stage**
  - **Capacitances scaled down by a factor of two from stage to stage (first order optimum)**
  - **No front-end track-and-hold**
  - **Neglect comparator energy**

Simplified Gain Stage Model

Feedback factor

$$\beta = \frac{\frac{C}{2}}{C + \frac{C}{2}} = \frac{1}{3}$$



Assumptions

Closed-loop gain = 2

Infinite transistor f_T (C_{gs}=0)

Thermal noise factor γ= 1, no flicker noise

Bias device has same noise as amplifier device

Linear settling only (no slewing)

$$C_{eff} = \frac{C}{2}(1-\beta) + \frac{C}{2} = \frac{5}{6}C$$

Effective load capacitance

$$N_{out} = 2\frac{1}{\beta}\frac{kT}{C_{eff}} = 6\frac{kT}{C_{eff}} = 5\frac{kT}{C}$$

Total integrated output noise

Total Pipeline Noise

$$N_{in,tot} = \underbrace{\frac{kT}{C}\left(1+\frac{1}{2}\right)}_{\textbf{First sampler}} + 5\frac{kT}{C}\left\{\frac{1}{2^2} + \frac{1}{\frac{1}{2}4^2} + \frac{1}{\frac{1}{4}8^2} + \ldots\right\}$$

$$= \frac{3}{2}\frac{kT}{C} + 5\frac{kT}{C}\left\{\frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \ldots\right\}$$

$$\cong 4\frac{kT}{C}$$

Key Constraints

$$SNR \cong \frac{\frac{1}{2}\left(\frac{V_{inpp}}{2}\right)^2}{4\frac{kT}{C}}$$

Thermal noise sets C

$$\tau = \frac{C_{eff}}{\beta g_m} = \frac{T_s/2}{\ln\left(\frac{1}{\varepsilon_d}\right)} \cong \frac{T_s/2}{\ln\left(\sqrt{SNR}\right)}$$

Settling time sets g_m

$$P = V_{DD}\frac{g_m}{\left(\frac{g_m}{I_D}\right)}$$

g_m sets power

Pulling It All Together

$$E_{pipe} = \underbrace{640}_{\substack{\text{Excess noise}\\ \text{Non-unity feedback}\\ \text{factor}}} \cdot kT \cdot SNDR \cdot \overbrace{\ln\left(\sqrt{SNDR}\right)}^{\substack{\text{Settling}\\ \text{“Number of } \tau\text{”}}} \cdot \underbrace{\left(\frac{V_{DD}}{V_{inpp}}\right)^2}_{\substack{\text{Supply}\\ \text{utilization}}} \cdot \overbrace{\frac{1}{V_{DD}}}^{V_{DD}\text{ penalty}} \cdot \underbrace{\frac{1}{\frac{g_m}{I_D}}}_{\substack{\text{Transconductor}\\ \text{efficiency}}}$$

- For SNDR = {60..80}dB, V_{DD}=1V, g_m/I_D=1/(1.5kT/q), V_{inpp}=2/3V, the entire expression becomes

$$E_{pipe} \cong \{388...517\} \cdot kT \cdot SNDR$$

- For realistic numbers at low resolution, we must introduce a bound for minimum component sizes

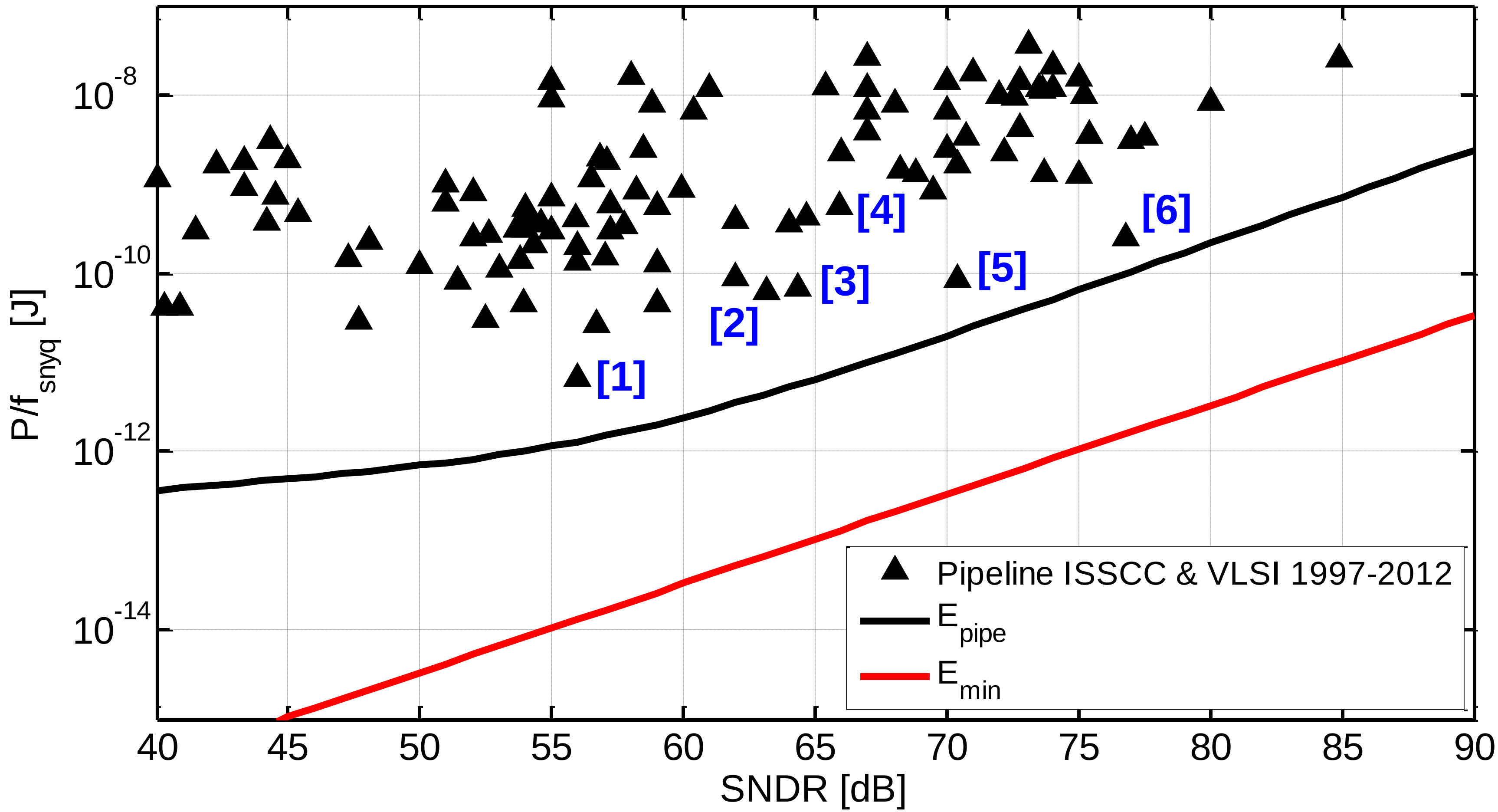
Energy Bound

- **Assume that in each stage $C_{eff} > C_{effmin} = 50fF$**
- **For n stages, detailed analysis shows that this leads to a minimum energy of**

$$E_{pipe,min} = 2n \cdot C_{eff\,min} V_{DD} \frac{\ln\left(\sqrt{SNDR}\right)}{\beta\left(\frac{g_m}{I_D}\right)}$$

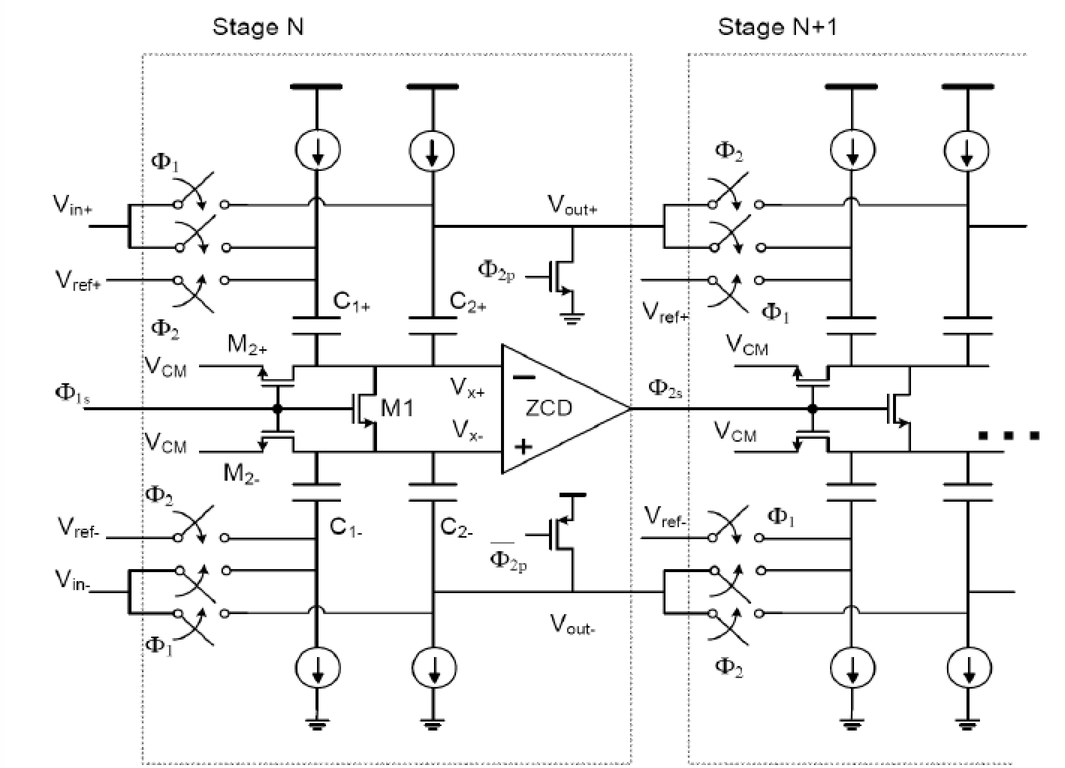
- **Adding this overhead to E_{pipe} gives the energy curve shown on the next slide**

Comparison to State-of-the-Art



[1] Verbruggen, ISSCC 2012
[2] Chu, VLSI 2010
[3] Lee, VLSI 2010
[4] Anthony, VLSI 2008
[5] Lee, ISSCC 2012
[6] Hershberg, ISSCC 2012

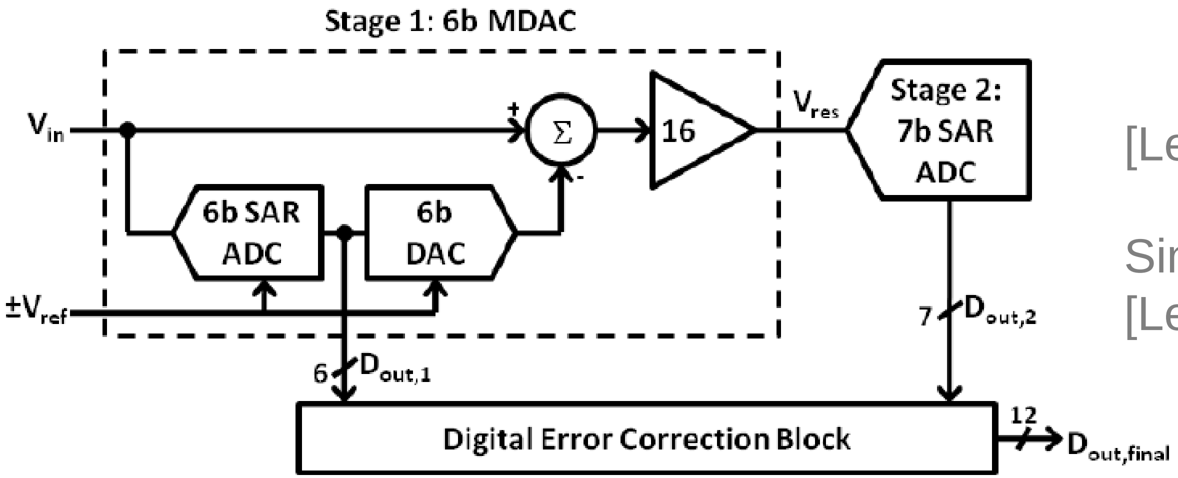
Ways to Approach E_{min} (1)



[Chu, VLSI 2010]

- **Comparator-based SC circuits replace op-amps with comparators**
- **Current ramp outputs**
  - **Essentially “class-B” (all charge goes to load)**

Ways to Approach E_{min} (2)

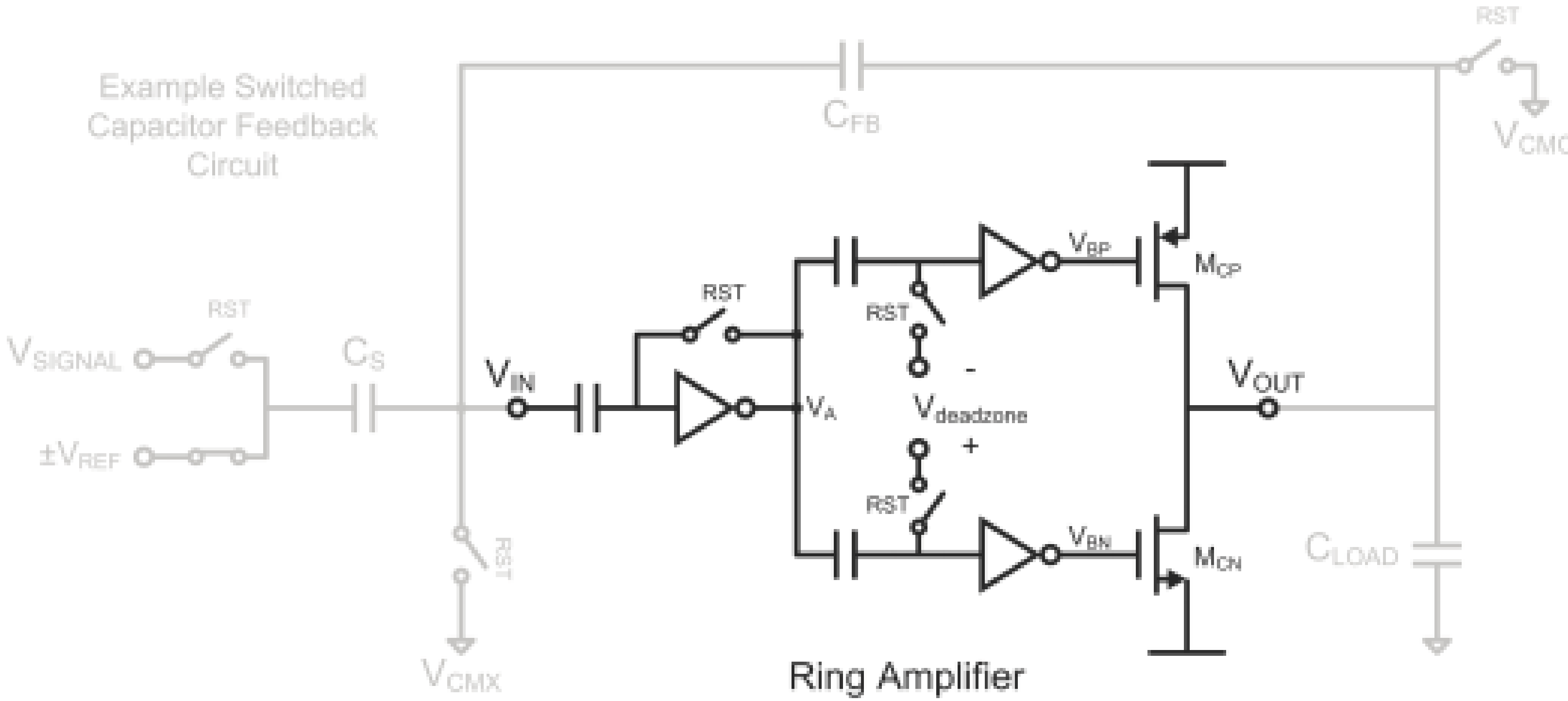


[Lee, VLSI 2010]

Similar:
[Lee, ISSCC 2012]

- **Use only one residue amplifier**
- **Build sub-ADCs using energy efficient SAR ADCs**
- **Essential idea: minimize overhead as much as possible**

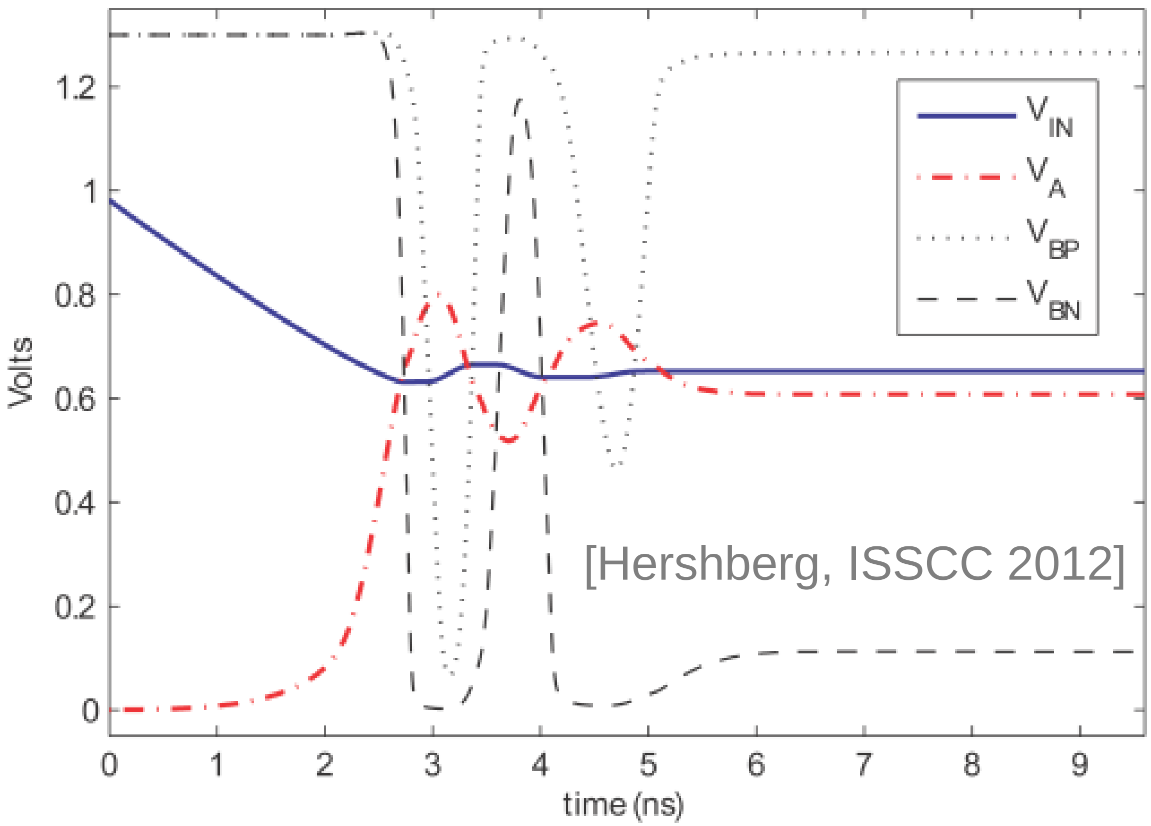
Ways to Approach E_{min} (3)



[Hershberg, ISSCC 2012]

- **Completely new idea: ring amplifier**
  - **As in "ring oscillator"**

Ways to Approach E_{min} (4)



- **Class-C-like oscillations until charge transfer is complete**
  - **Very energy efficient**

Expected Impact of Technology Scaling

- **Low resolution (SNDR ~ 40-60dB)**
  - **Continue to benefit from scaling**
  - **Expect energy reductions due to reduced C_{min} and reduction of CV^2-type contributors**
- **High resolution (SNDR ~ 70dB+)**
  - **It appears that future improvements will have to come from architectural innovation**
  - **Technology scaling will not help much and is in fact often perceived as a negative factor in noise limited designs (due to reduced V_{DD})**
    - **Let's have a closer look at this…**

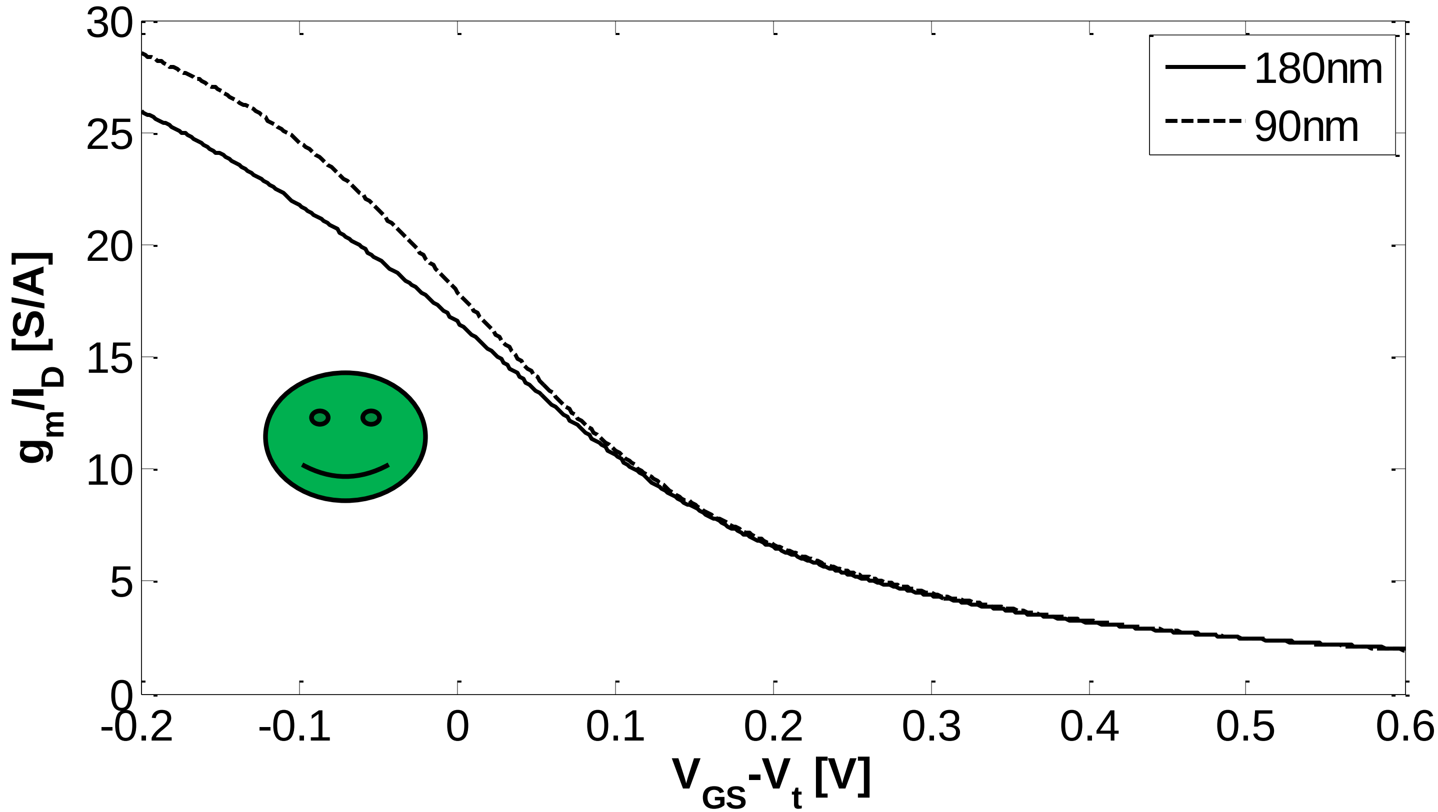
A Closer Look at the Impact of Technology Scaling

- **As we have shown**

$$E \propto \frac{1}{V_{DD}} \cdot \left(\frac{V_{DD}}{V_{inpp}}\right)^2 \cdot \frac{1}{\left(\frac{g_m}{I_D}\right)}$$

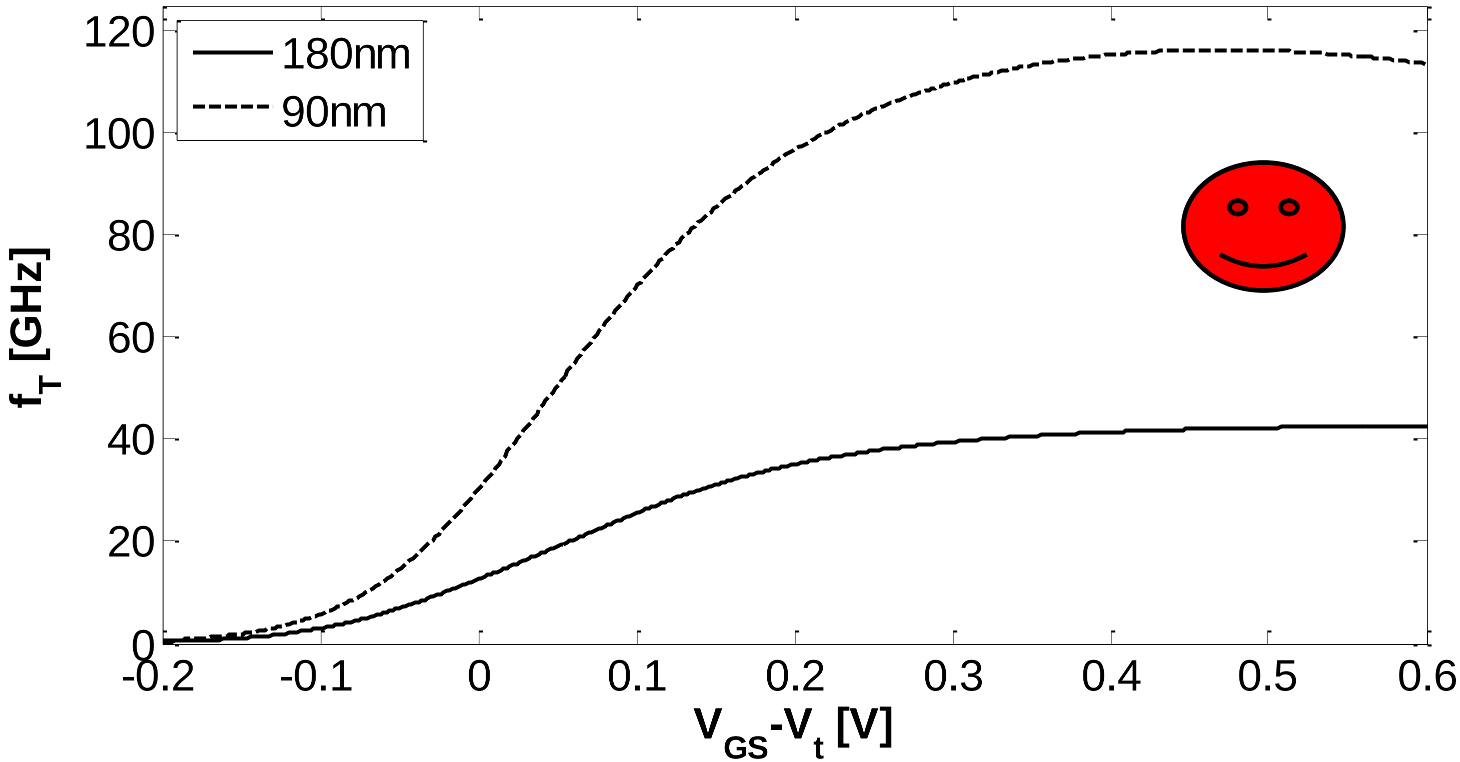
- **Low V_{DD} hurts, indeed, but one should realize that this is not the only factor**
- **Designers have worked hard to maintain (if not improve) V_{inpp}/V_{DD} in low-voltage designs**
- **How about g_m/I_D?**

g_m/I_D Considerations (1)



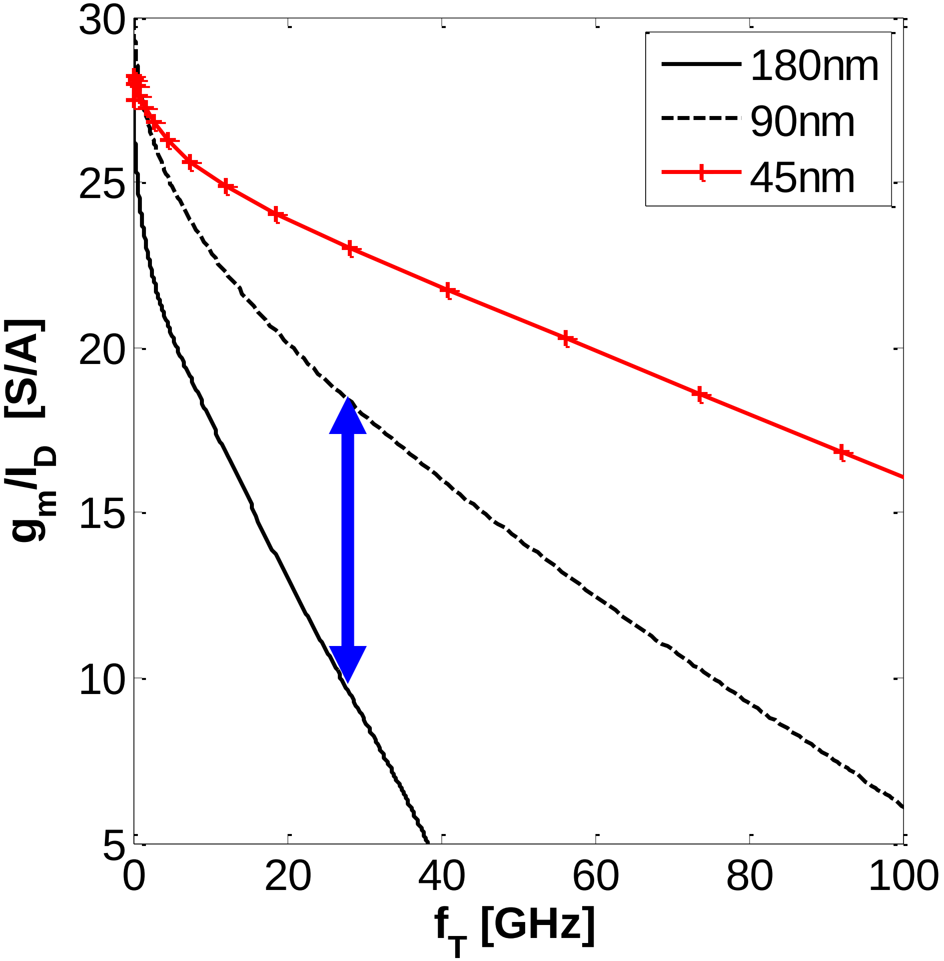
- **Largest value occurs in subthreshold ~$(1.5 \cdot kT/q)^{-1}$**
- **Range of g_m/I_D does not scale (much) with technology**

g_m/I_D Considerations (2)



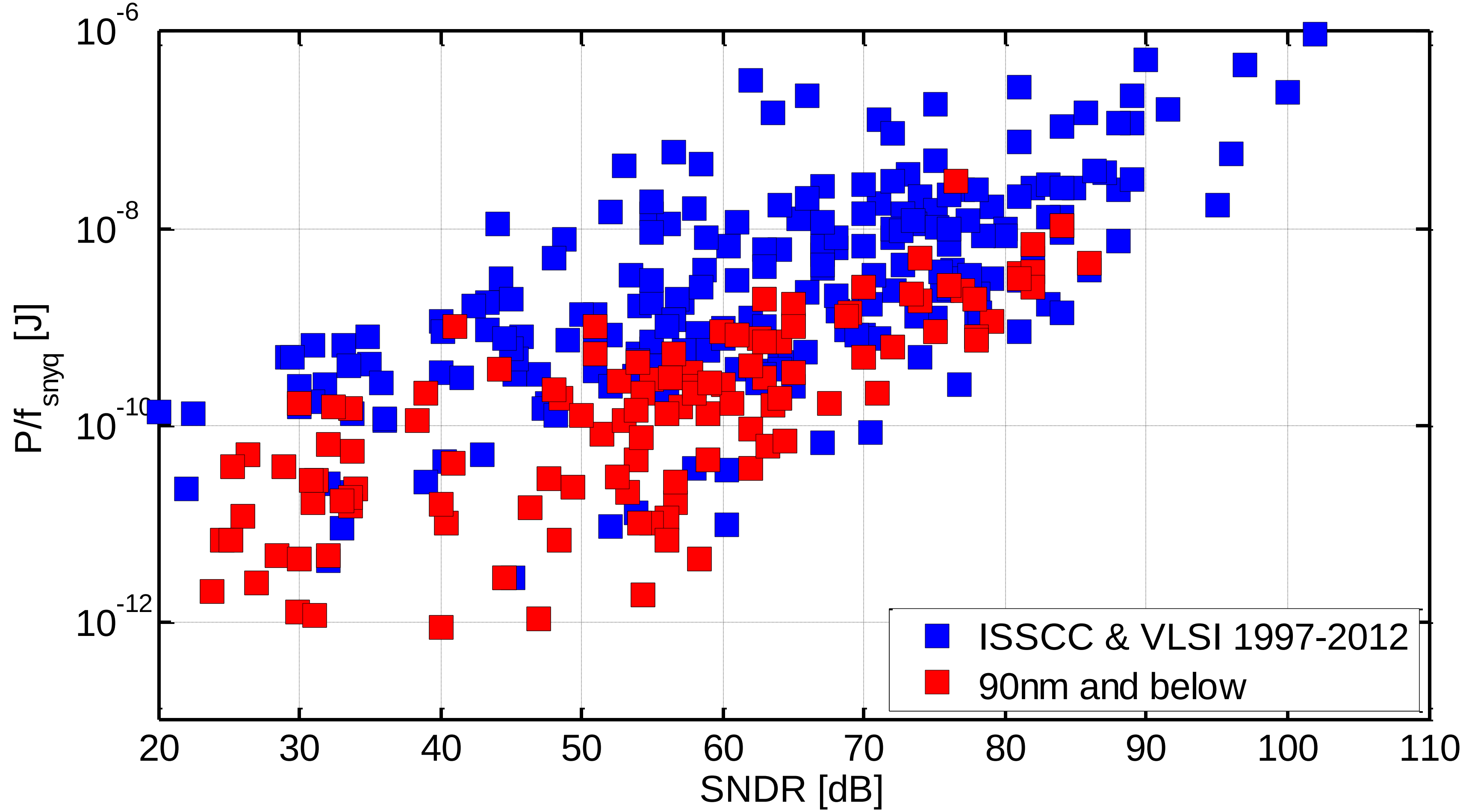
- f_T is small in subthreshold region
- Must look at g_m/I_D for given f_T requirement to compare technologies

g_m/I_D Considerations (3)

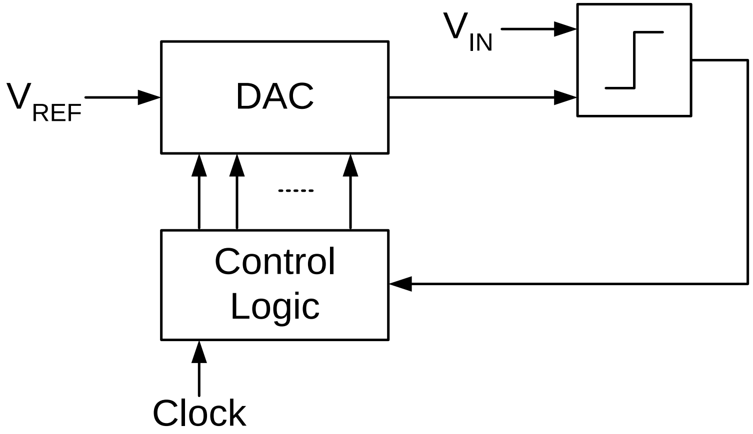


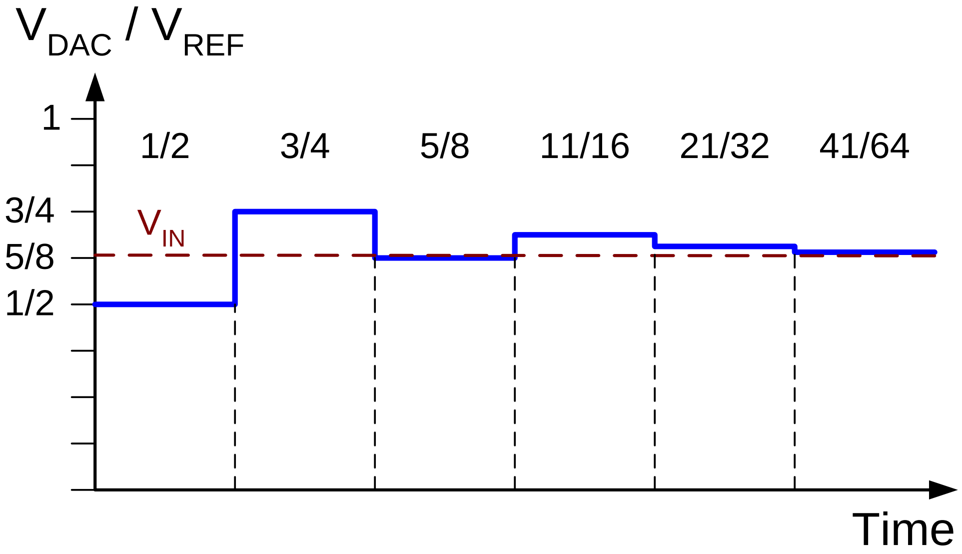
- **Example**
  - **f_T = 30GHz**
  - **90nm: g_m/I_D = 18S/A**
  - **180nm: g_m/I_D = 9S/A**
- **For a given f_T, 90nm device takes less current to produce same g_m**
  - **Helps mitigate, if not eliminate penalty due to lower V_{DD} (!)**

ADC Energy for 90nm and Below



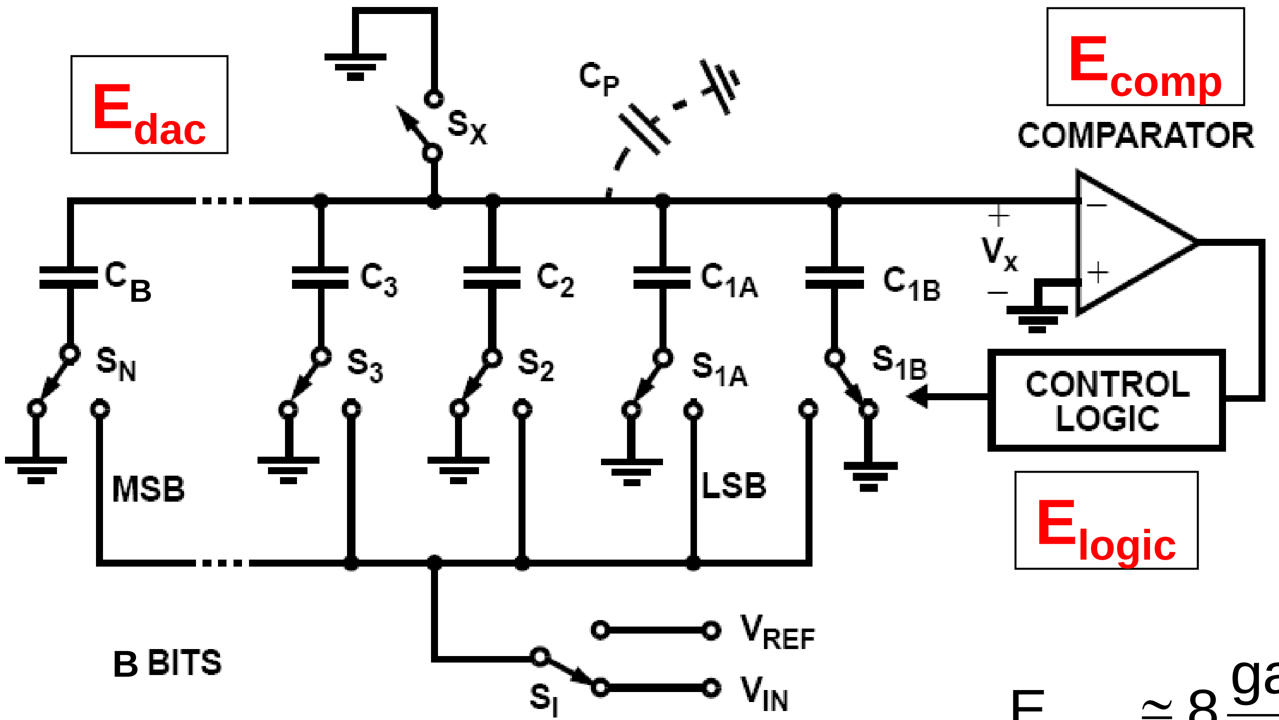
Successive Approximation Register ADC





- **Input is approximated via a binary search**
- **Relatively low complexity**
- **Moderate speed, since at least B+1 clock cycles are needed for one conversion**
- **Precision is determined by DAC and comparator**

Classical Implementation



$$E_{logic} \cong 8\frac{\text{gates}}{\text{bit}} \cdot \frac{2\text{fJ}}{\text{gate}} \cdot B$$

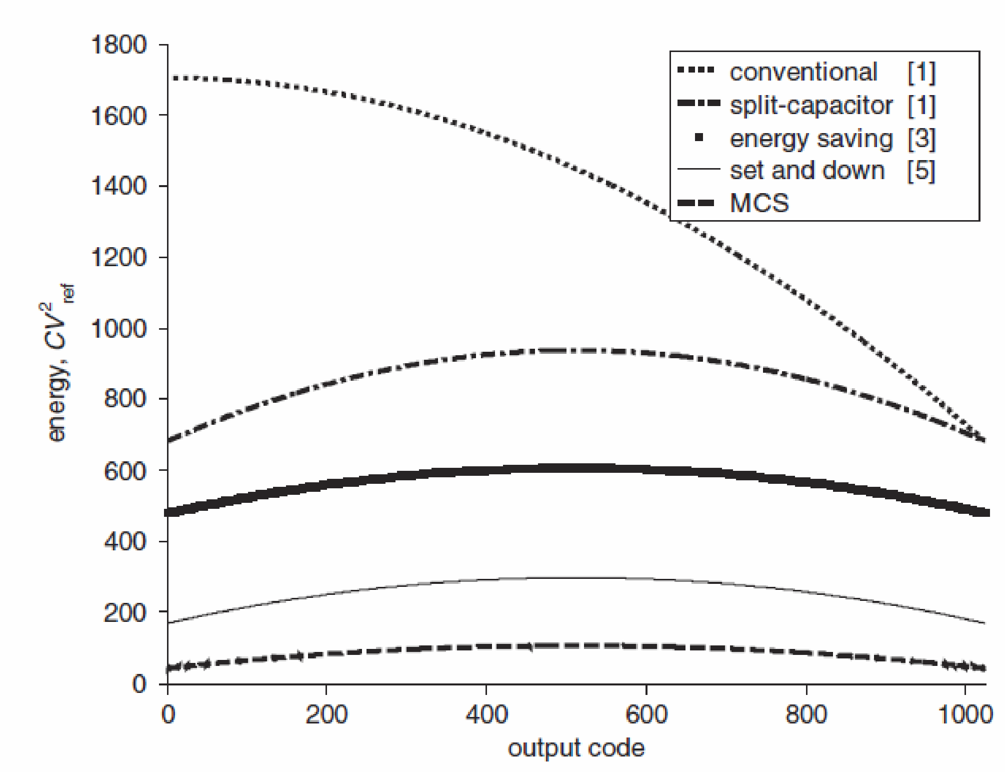
[McCreary, JSSC 12/1975]

(somewhat optimistic)

DAC Energy

- **Is a strong function of the switching scheme**
- **Excluding adiabatic approaches, the "merged capacitor switching" scheme achieves minimum possible energy**

[Hariprasath, Electronics Lett., 4/2010]



$$E_{dac} \cong \sum_{i=1}^{n-1} 2^{n-3-2i}\left(2^{i}-1\right)CV_{ref}^{2}$$

For 10 bits:

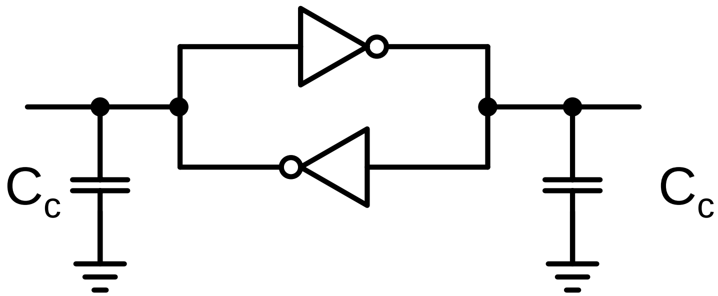
$$E_{dac} \cong 85CV_{ref}^{2}$$

DAC Unit Capacitor Size (C)

- **Is either set by noise, matching, or minimum realizable capacitance (assume C_{min} = 0.5fF)**
- **We will exclude matching limitations here, since these can be addressed through calibration**
- **Assuming that one third of the total noise power is allocated for the DAC, we have**

$$SNR \cong \frac{\frac{1}{2}\left(\frac{V_{inpp}}{2}\right)^2}{\frac{kT}{2^B C} + N_{comp} + N_{quant}} \qquad C = 24kT \cdot SNR \cdot \frac{1}{2^B \cdot V_{inpp}^2} + C_{min}$$

Comparator



Simple Dynamic Latch

(Assuming C_{cmin} = 5fF)

$$N_{in} \cong \frac{kT}{C_c}$$

Thermal Noise

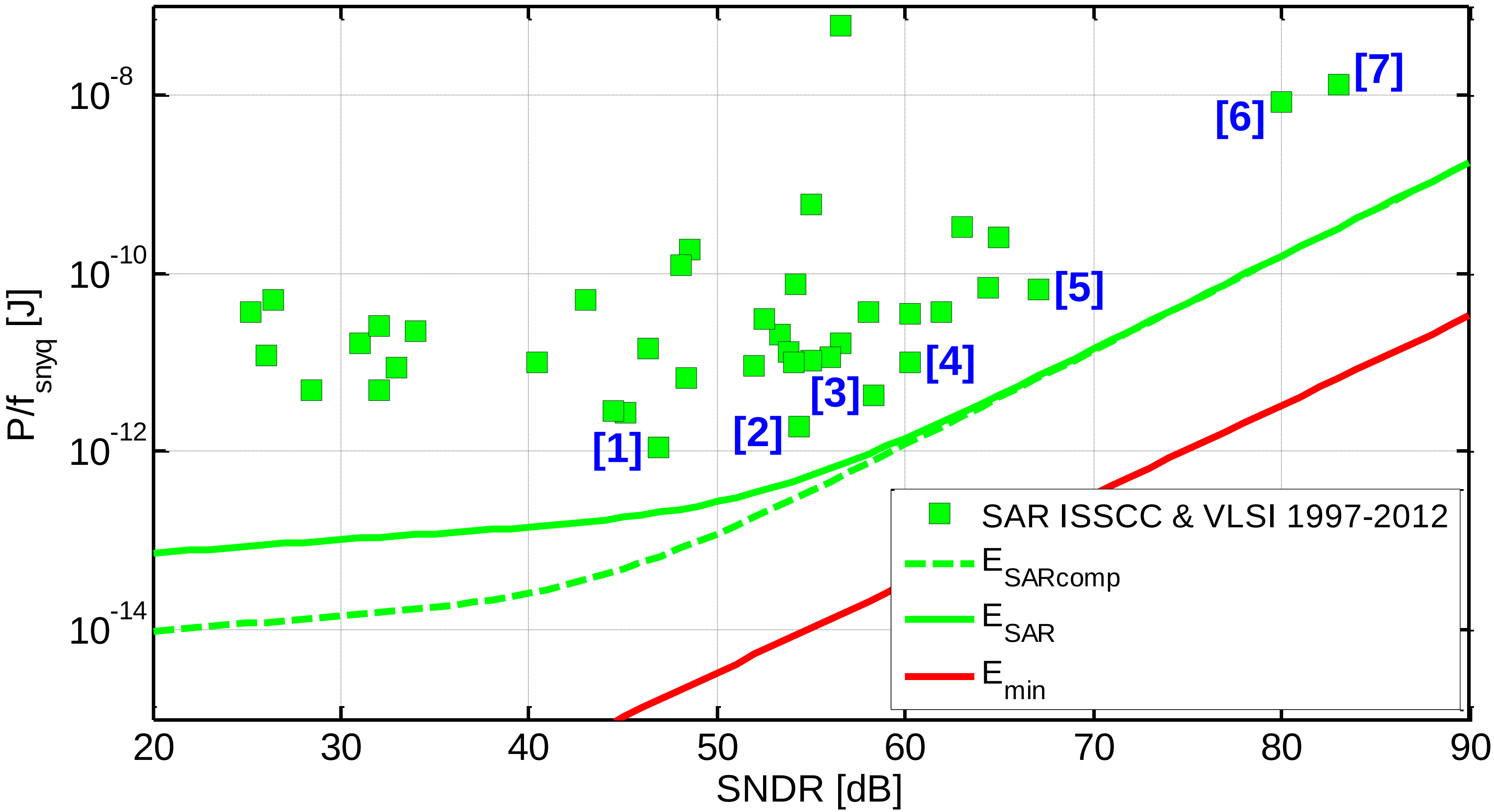
$$C_c = 24kT \cdot SNR \cdot \frac{1}{V_{inpp}^2} + C_{c\,min}$$

$$B \cong \frac{SNR[dB] - 3}{6}$$

$$E_{comp} \cong \left(24kT \cdot SNR \cdot \frac{V_{DD}^2}{V_{inpp}^2} + C_{c\,min} V_{DD}^2 \right) \cdot \frac{1}{2} \cdot B$$

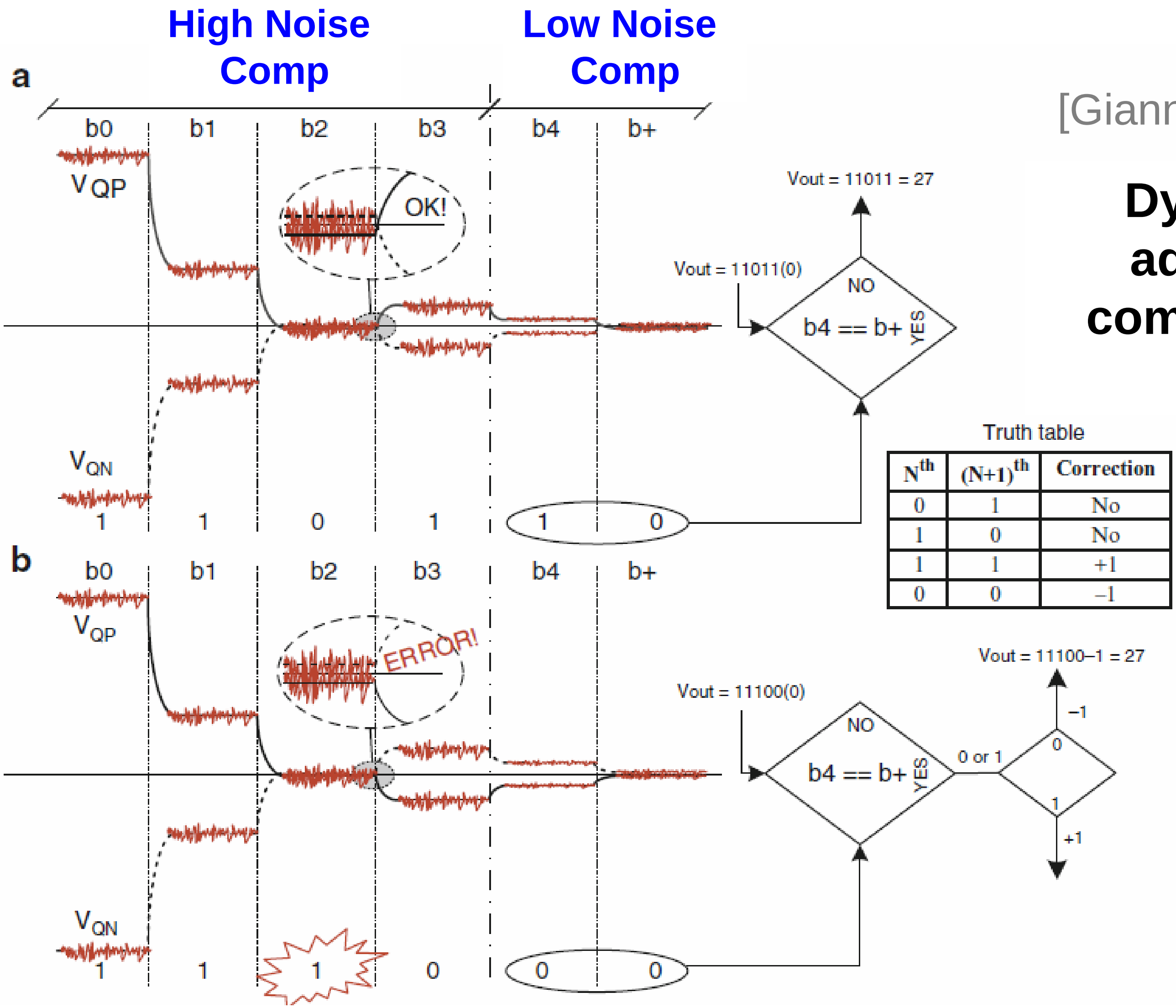
Switching probability

Comparison to State-of-the-Art



[1] Shikata, VLSI 2011
[2] Van Elzakker, ISSCC 2008
[3] Harpe, ISSCC 2012
[4] Liu, VLSI 2010
[5] Liu, ISSCC 2010
[6] Hurrell, ISSCC 2010
[7] Hesener, ISSCC 2007

Ways to Approach E_{min} (1)



Truth table

N^{th}	$(N+1)^{th}$	Correction
0	1	No
1	0	No
1	1	+1
0	0	–1

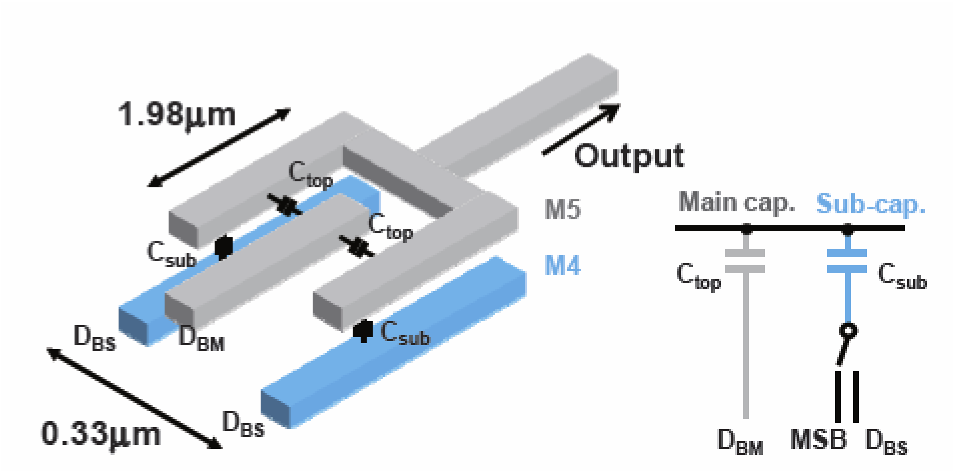
[Giannini, ISSCC 2008]

Dynamic Noise adjustment for comparator power savings

Ways to Approach E_{min} (2)

- **Minimize unit caps as much as possible for moderate resolution designs**
  - **Scaling helps!**

0.5fF unit capacitors

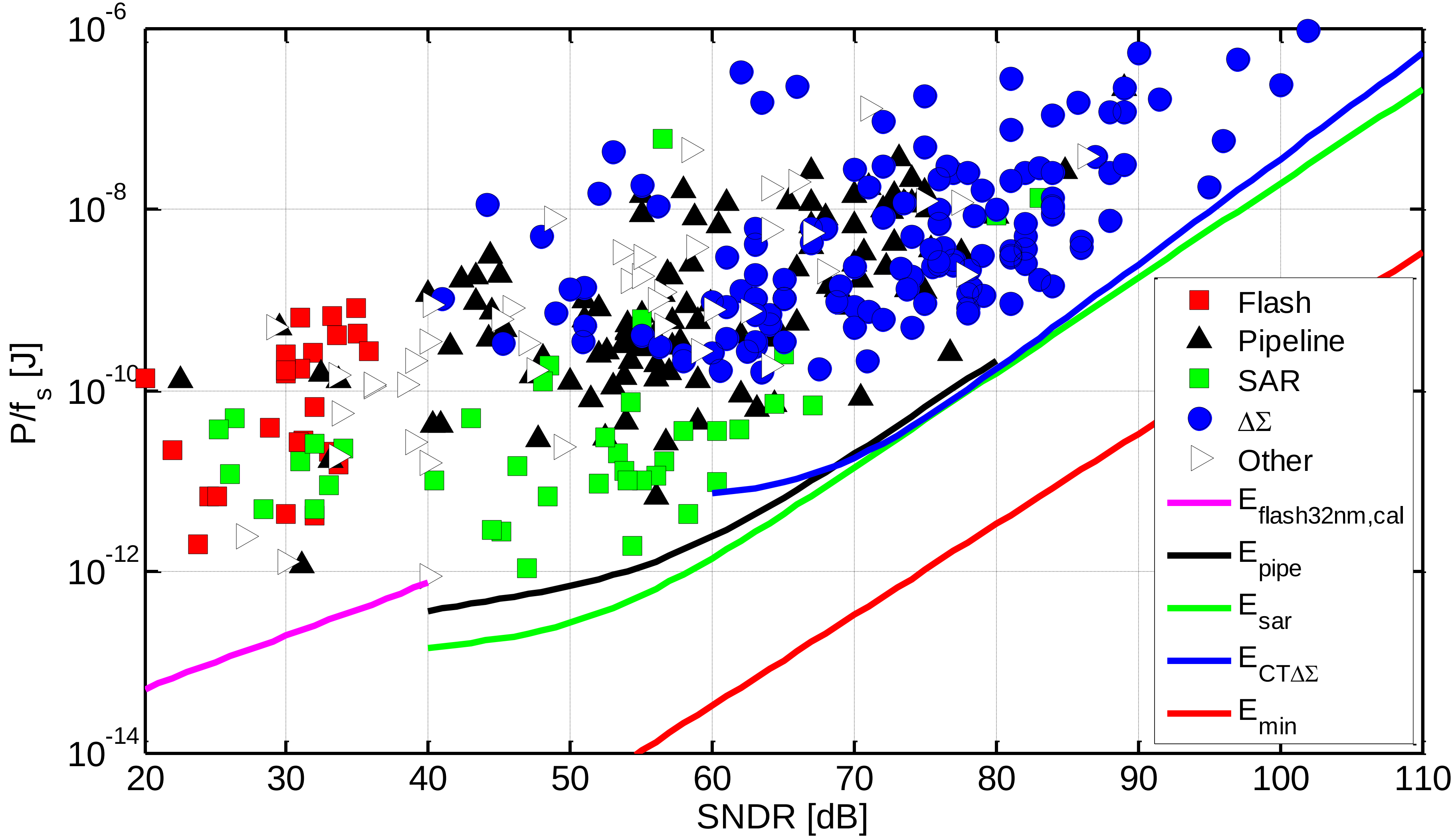


[Shikata, VLSI 2011]

Delta-Sigma ADCs

- Discrete time
  - Energy is dominated by the first-stage switched-capacitor integrator
  - Energy analysis is similar to that of a pipeline stage
- Continuous time
  - Energy is dominated by the noise and distortion requirements of the first-stage continuous time integrator
  - Noise sets resistance level, distortion sets amplifier current level
  - Interestingly, this leads to about the same energy limits as in a discrete-time design

Overall Picture

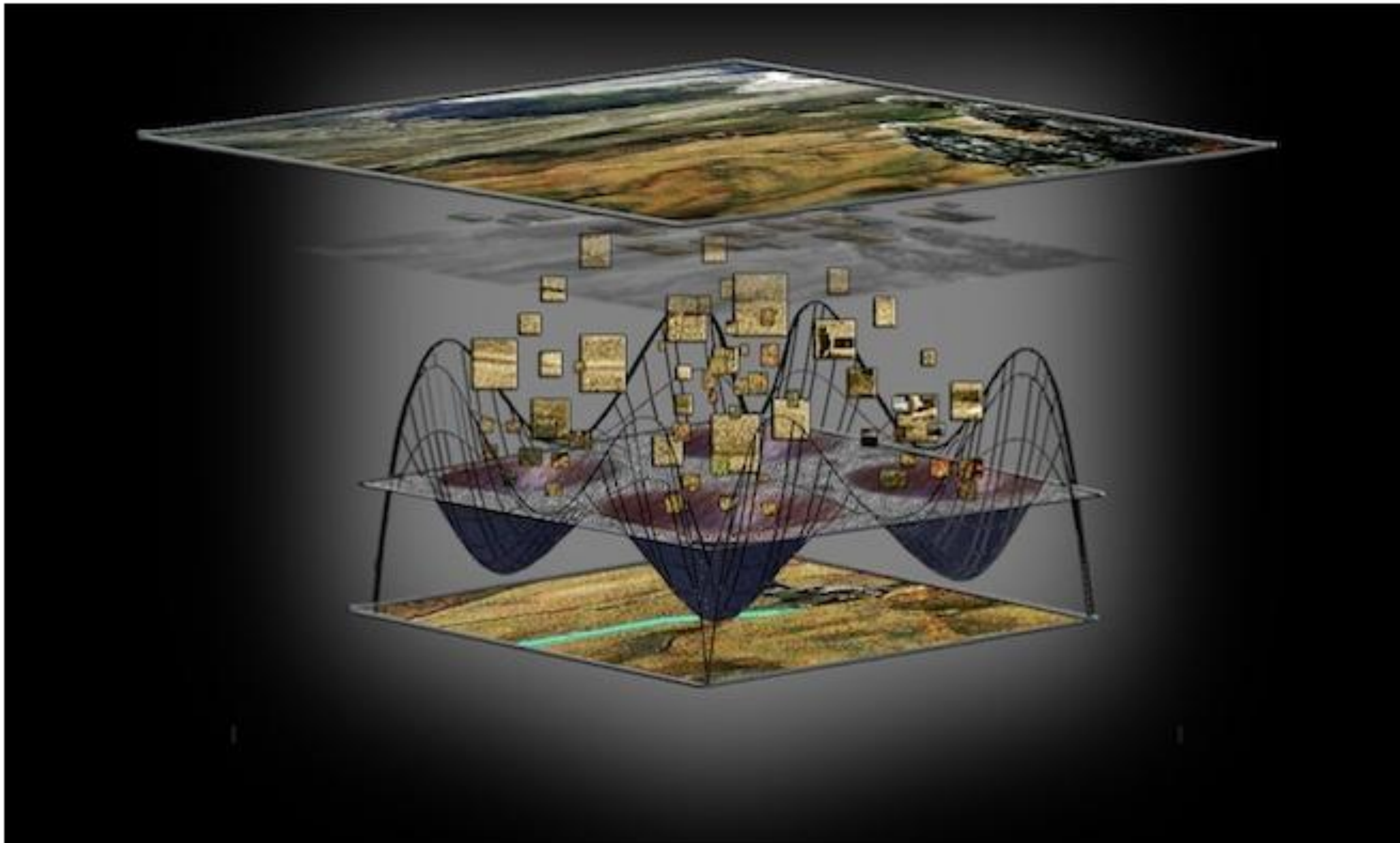


Summary

- **No matter how you look at it, today's ADCs are <u>extremely</u> well optimized**
- **The main trend is that the "thermal knee" shifts very rapidly toward lower resolutions**
  - **Thanks to process scaling and creative design**
- **At high resolution, we seem to be stuck at E/E_{min}~100**
  - **The factor 100 is due to architectural complexity and inefficiency: excess noise, signal < supply, non-noise limited circuitry, class-A biasing, …**
- **This will be very hard to change**
  - **Scaling won't help (much)**
  - **Some of the recent data points already use class-B-like amplification**
  - **Can we somehow recycle the signal charge?**
- **Are there completely new ways to approach A/D conversion?**

Darpa Has Seen the Future of Computing ... And It's Analog

BY ROBERT MCMILLAN 08.22.12 6:30 AM



How would non-digital chips work? Darpa paints a picture. Image: Darpa

http://www.wired.com/wiredenterprise/2012/08/upside/