EE 241B HW2 Writeup

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Contents

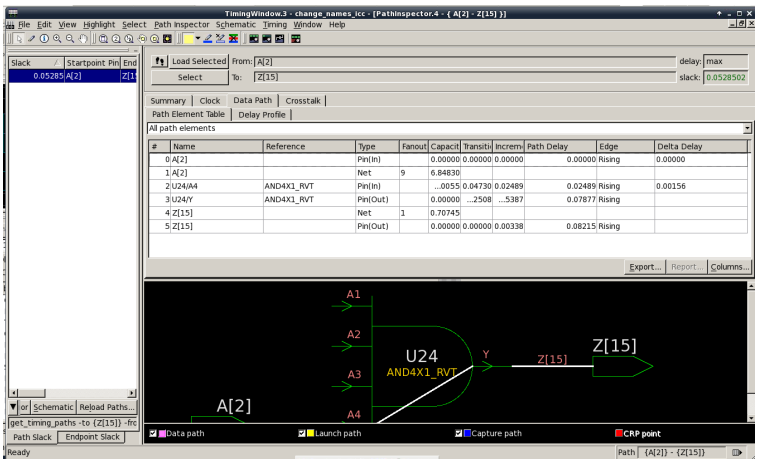
1 Extracting and Simulating a Synthesized Design

We start with an already placed and routed 4-bit decoder and we go through the flow of extracting parasitics, running LVS, and running SPICE simulations of the extracted schematic.

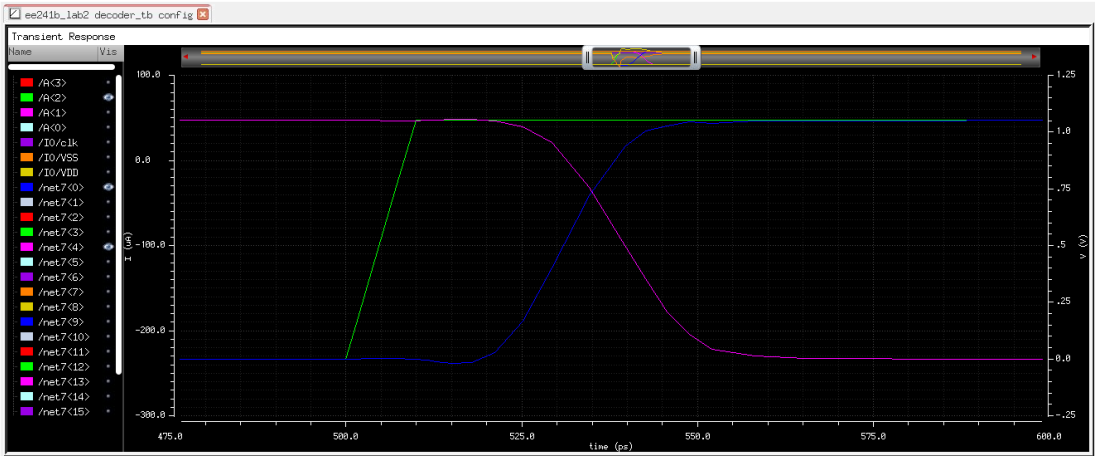
1.1 Delay of a Path

For the path from A[2] to Z[15] rise, what is the delay measured by IC Compiler, SPICE simulation without extracted parasitics, and SPICE simulation with parasitics?

- IC Compiler: 0.08215 ns



- SPICE without parasitics

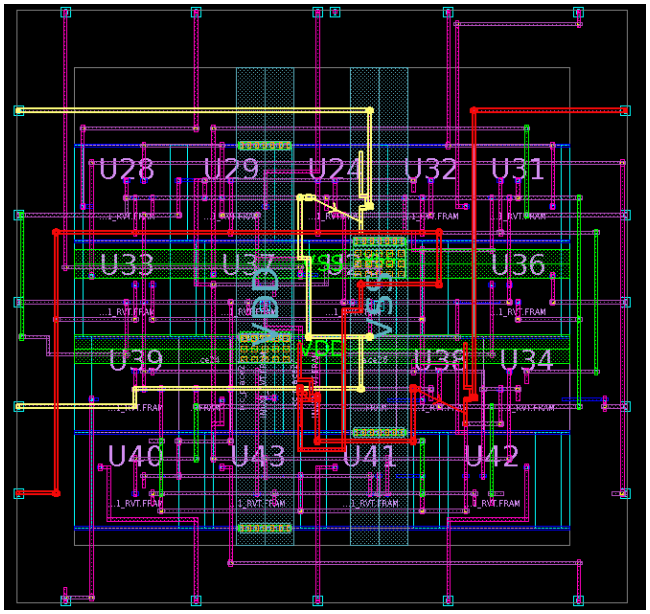


- SPICE with parasitics

1.2 ICC Critical Path + Special Path

We display the critical path in ICC and also highlight the special path noted above from the rise of A[2] to the rise of Z[15].

The critical path is from rising A[3] to falling Z[5], and it has a negative slack of -0.00263 ns. It is highlighted in red. The special path above is highlighted in yellow.



1.3 Power Estimate Accuracy Analysis

We run the functional testbench that counts from A=0000 to A=1111 and report the power measured by Primetime, the SPICE simulation, and the mixed-signal simulation.

- Primetime
- SPICE
- Mixed-Signal

1.4 Voltage Scaling Power Estimates

We run the mixed-signal simulation at 1.05V, 0.8V, 0.6V, and 0.4V and measure the average power for each voltage. We then convert average power to energy/op in terms of J/op and uW/Mhz. These results are compared to the theoretically predicted active energy savings for voltage scaling based on the 1.05V result.

The clock period will have to increase for lower supply voltages to compensate for increased delay.

2 FF and Latch Based Timing

3 Variability and Timing Simulations

A PMOS/NMOS DC Characterization SPICE Sim