EE 241B HW3 Writeup

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Contents

1 Building and Characterizing a Standard Cell

1.1 Flow and Decoder Delay Using Custom Cell

We go through the tutorial to design a custom NAND2 standard cell. We first record the critical path of the 3-8 decoder used in the previous lab with the NAND2 cell supplied with the design kit. The critical path goes from `A[3]` to `Z[5]` and it has a delay of 0.1376 ns.

We then tell DC and ICC to use our custom standard cell and we measure the critical path again. The critical path now goes from `A[0]` to `Z[14]` and has a delay of 0.1019 ns, which is an improvement over the previous ICC run. However, looking at the final Verilog netlist from ICC only 2 instances of our `NAND2X1B_RVT` cell exist. However, after running only DC, there were many instances of our custom cell. It seems that ICC did some optimization and swapped out most of those custom cells for standard cells from the design kit.

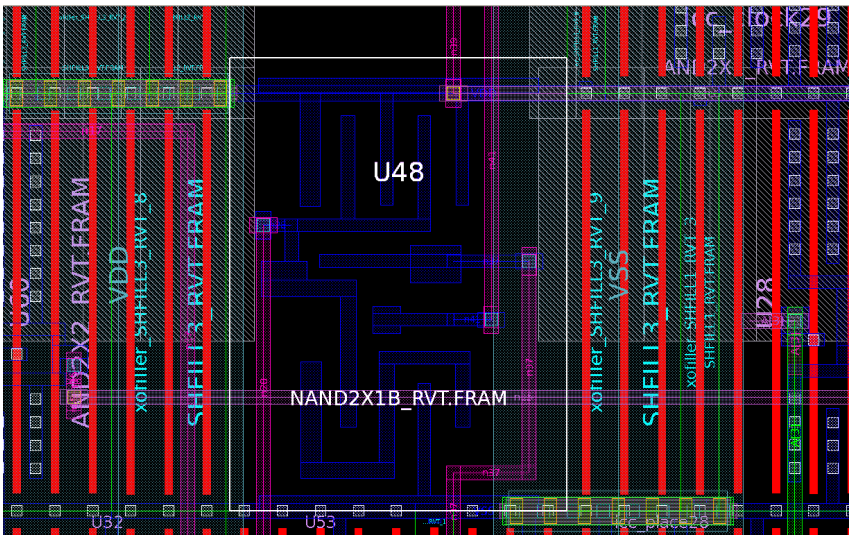


Figure 1: An instance of the NAND2X1B_RVT cell in ICC with visible M1 polygons.

1.2 Standard Cell Inverter Variation Impact vs V_{DD}

We run a 300 point Monte Carlo simulation and plot the mean and sigma for the input-rising/output-falling delay of the `INVX0_RVT` standard cell for V_{DD} between 0.2 and 1.05. We fix an input slope of 10ps and a 1fF load. This part was done by exporting a netlist from Virtuoso and using commandline HSPICE for the simulation.

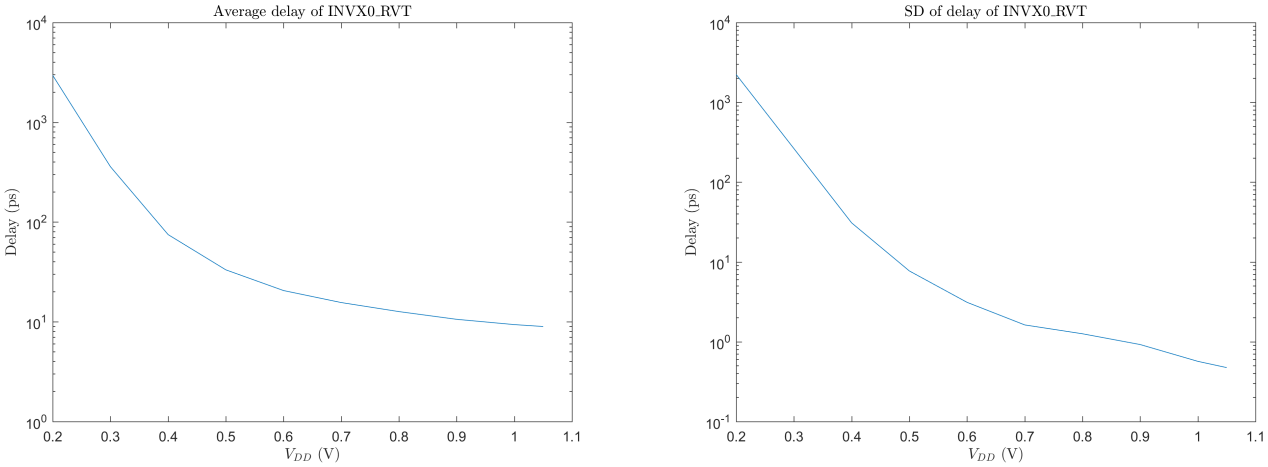
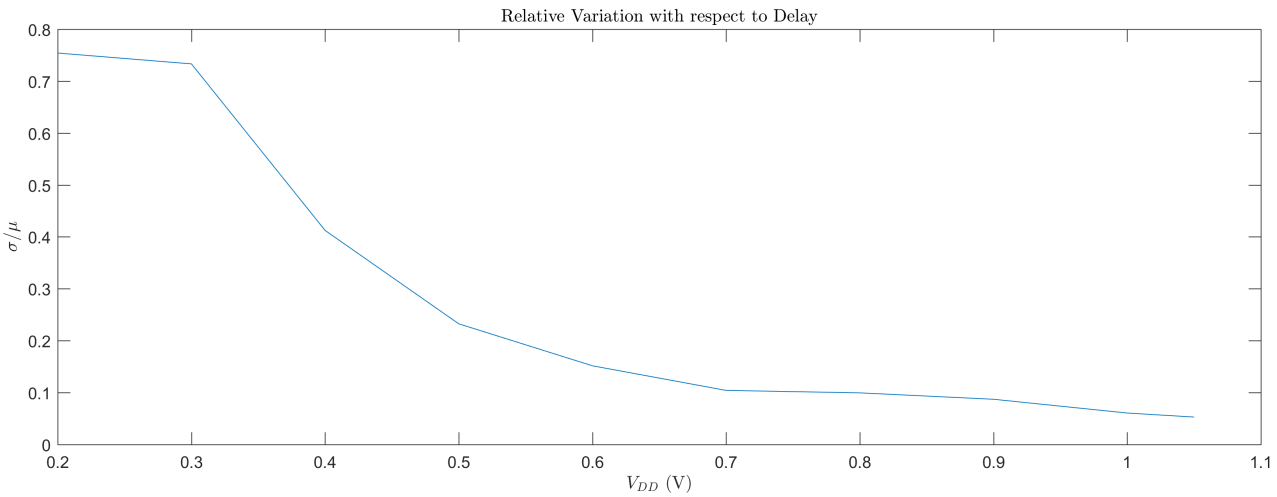
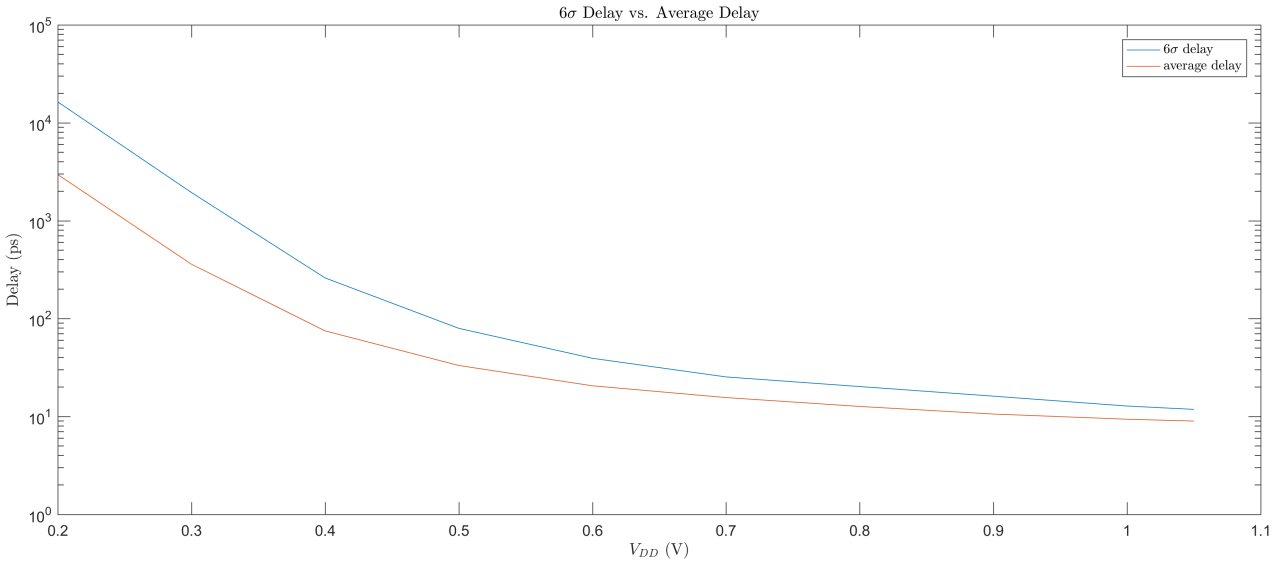


Figure 2: Plot is log-scale in y-axis.

We then plot σ/μ vs. V_{DD}.



Finally we plot the delay of a 6σ cell relative to the mean vs. V_{DD}.



Variation has a larger effect at low voltages since our mismatch model works by setting V_{th} of each transistor using a probability distribution with a $\sigma_{V_{th}}$. At lower voltages, the transistor has an operating voltage around its threshold voltage and thus makes the variation more pronounced.

1.3 Delay Distributions for Different V_{DD}

We create histograms and fit a normal curve for the delay at 0.6V and 1.05V.

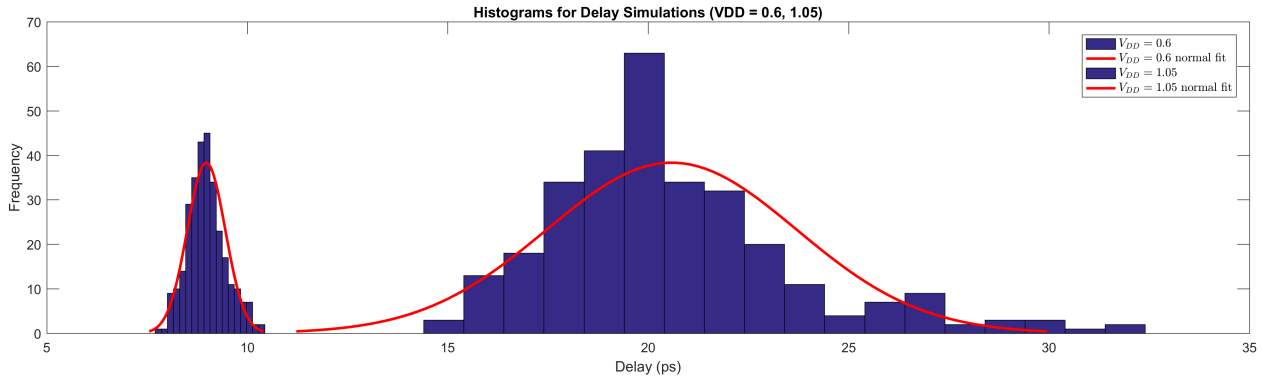


Figure 3: Two histograms that contain delays from the 300 point monte carlo sim. Left histogram is at $V_{DD} = 1.05V$ and right histogram is at $V_{DD} = 0.6V$.

The histogram for $V_{DD} = 1.05V$ is roughly Gaussian and can be closely approximated with a normal distribution. However the histogram for $V_{DD} = 0.6V$ is asymmetric and a Gaussian is a poor fit for it. There is a long right tail, and it comes about due to a certain transistor having a much higher V_{th} which increases its delay a lot more at a lower V_{DD}.

1.4 $\sigma_{V_{th}}$ and Monte Carlo in MATLAB

We compute $\sigma_{V_{th}}$ for the NMOS in `INVX0_RVT`. As per the Pelgrom mismatch model:

$$\sigma_{V_{th}} = \frac{A_{V_t}}{\sqrt{W \cdot L}} = \frac{2}{\sqrt{W \cdot L \cdot 1e6 \cdot 1e6}} \text{ mV} \tag{1}$$

In this design kit, A_{V_t} is set to 2 $mV \cdot \mu m$. The minimally sized inverter contains an NMOS with a width of 520nm and length of 30nm. Thus, we get $\sigma_{V_{th}} = 16.01$ mV for the NMOS.

Now we use the alpha-power law's equation for I_{on} and parameter values $K = 1.7\text{e-}4, V_{th} = 0.336, \alpha = 1.36$. We find the equation for the delay of an inverter assuming maximum current for a transition from V_{DD} to $V_{DD}/2$. We also estimate $\Delta T = C\Delta V/I$ where $\Delta V = V_{DD}/2$ and $C \approx 1.5$ fF.

$$I_{on} = K(V_{gs} - V_{th})^{\alpha}$$
$$\Delta T = \frac{C \cdot 0.5 V_{DD}}{K(V_{DD} - V_{th} + \Delta V_{th})^{\alpha}}$$

We use MATLAB to run a Monte Carlo simulation on this delay model for $V_{DD} = 0.5, 1.05$ V and compare it with the HSPICE results in the previous section. We get 600 samples from a $(0, \sigma_{V_{th}})$ normal distribution and plug those samples into the delay formula for different values of V_{DD}.

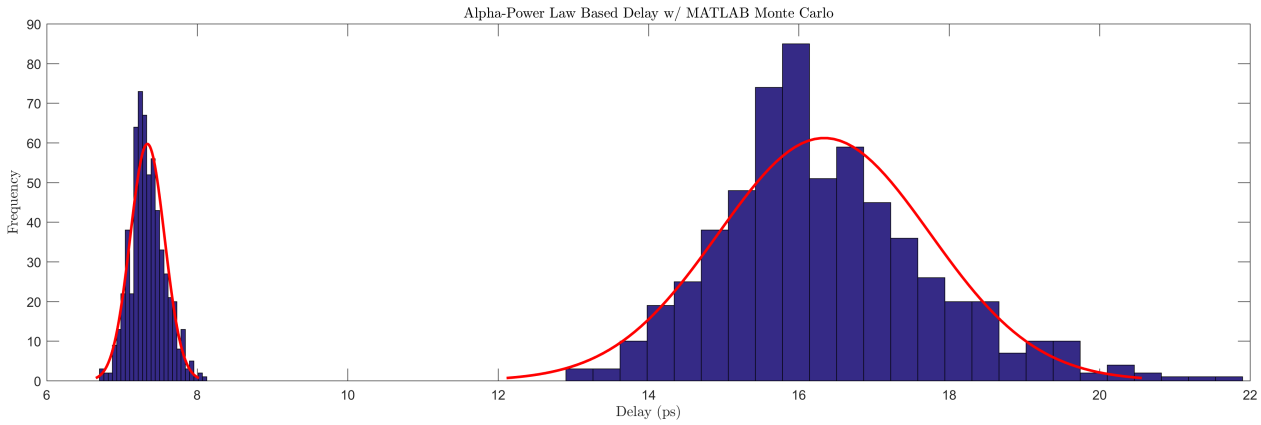


Figure 4: Two histograms that contain delays from the MATLAB monte carlo sim (600 points). Left histogram is at $V_{DD} = 1.05V$ and right histogram is at $V_{DD} = 0.6V$.

We see similar output from the MATLAB Monte Carlo and the HSPICE Monte Carlo. The delay distribution for $V_{DD} = 1.05$V is narrow and approximately normal, while the delay distribution for $V_{DD} = 0.6$V is much wider and has a long right tail. Based on the delay equation, the distribution should approach a Gaussian with increasing V_{DD}.

2 Flip-Flops

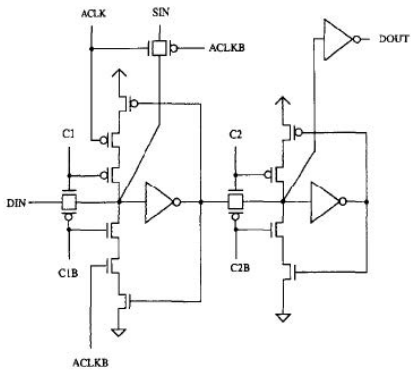


Figure 5: A schematic of a sequential circuit.

2.1 Identify Circuit

Assuming that C1 and C2 are opposite phases of the same clock, the circuit above implements a **D-type flip-flop** using a master-slave latch topology.

When C1 is high, the first transmission gate is transparent and the data is allowed to settle at the input of the second transmission gate. At the moment that C2 goes high, C1 goes low to close

off any further input changes, and the output reflects the 'last' value that passed through the first transmission gate while C1 was high.

The rest of the circuitry serves to make the flip-flop static by providing feedback into the storage nodes and there is an additional transmission gate that can be used by a scan chain.

2.2 FF Timing Characteristics

Assuming that the NMOS and PMOS devices have the same mobility and are all symmetrically sized, order the following timing parameters by magnitude: setup time, hold time, clock-output delay.

The setup time is approximately equal to the time it takes for an input signal at `DIN` to race past the first transmission gate, after which the gate can become opaque. The hold time is close to 0 since after C2 goes high the first transmission gate becomes opaque and `DIN` can't influence the flip-flop anyways. Also, the storage node doesn't need `DIN` after the rising edge of C2. The clock to output delay is approximately equal to the delay through the second transmission gate and an inverter.

So in order of smallest to largest: **hold time, setup time, clock to output delay**.

3 Timing