EE 241B HW4 Writeup

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1 Delay Replicas

Your design has a critical path of 20 FO4 inverter delays at the nominal supply voltage. Your friend has suggested to design a replica circuit consisting of N FO1 inverters (where N is approximately 40.

1.1 Replica Design

Design the actual replica made of N-1 identical stages with the Nth stage having an increased fanout to match the actual critical path. What is the fanout of the Nth stage?

We begin by calculating the critical path delay in terms of minimally sized inverter delays t_{inv} using the method of logical effort. We first define all the variables that are used for logical effort delay calculations.

$$
\begin{aligned}
f &= \text{ fanout of single stage} = C_{out}/C_{in} \\
F &= \text{ total fanout} = C_{L,total}/C_{in} \\
\text{EF} &= \text{ effective fanout} = \text{LE}f \\
p &= \text{ intrinsic delay (ratio of PMOS to NMOS capacitance)}; p_{inv} = \gamma \\
\text{LE} &= \text{ logical effort} = (R_{eq,gate}C_{in,gate})/(R_{eq,inv}C_{in,inv}); LE_{inv} = 1 \\
\text{b} &= \text{ branching factor} = \frac{C_{L,on-path} + C_{L,off-path}}{C_{L,on-path}} \\
\text{PE} &= \text{ path effort} = (\prod \text{LE})(\prod b)F \\
t_{p,gate} &= t_{inv}(p + \text{LE}f) = t_{inv}(p + \text{EF})
\end{aligned}
$$

Now we calculate the critical path delay.

$$
\begin{aligned}
t_{delay,inv} &= t_{inv}(p_{inv} + \mathrm{LE}f) \\
t_{delay,inv} &= t_{inv}(\gamma + 4) \\
t_{delay,crit-path} &= t_{delay,inv} \cdot N_{stages} = 20 \cdot t_{inv}(\gamma + 4)
\end{aligned}
$$

Let's now consider the path that consists of 39 FO1 inverters and 1 larger inverter. We can break this path's delay into 2 sub-delays.

$$
\begin{aligned}
t_{delay,replica1} &= 39 \cdot t_{inv}(\gamma + 1) \\
t_{delay,replaca2} &= t_{inv}(\gamma + f_{last,stage}) \\
t_{delay,replica} &= 39 t_{inv}(\gamma + 1) + t_{inv}(\gamma + f_{last,stage}) \\
\text{Set } t_{delay,replica} &= t_{delay,crit-path}
\end{aligned}
$$