EE241 Advanced Digital Integrated Circuits **Spring 2017.**

HOMEWORK 2. **Due: Wednesday, March 8, 2017.**

This is an individual assignment!

1. Extracting and simulating the synthesized design.

In the first lab, we have created a design by using a strictly digital ('VLSI') design flow. In this assignment, we will extract the synthesized and automatically placed and routed design to look under its hood. We will compare the results of dynamic simulation to the static timing analysis. To do this, please work through the tutorial entitled: Using VLSI Flow Outputs, then turn in:

a) For the path A[2] rise to Z[15] rise, report the delay measured by IC Compiler, SPICE simulated without extracted parasitics, and SPICE simulated with parasitics

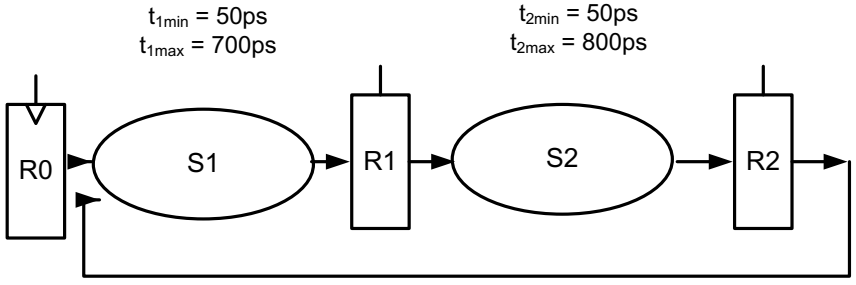
b) A screenshot of the critical path highlighted in IC Compiler showing the wires that contribute to the path from a)

c) For the functional testbench that counts from A=0000 to A=1111, report the power measured by Primetime, the SPICE simulation, and the mixed-signal simulation.

d) Run the mixed-mode simulation at 1.05V, 0.8V, 0.6V, and 0.4V and measure the average power at each point. Then convert average power to energy/op in terms of J/op and uW/Mhz. Compare these results from the theoretically predicted active energy savings for voltage scaling based on the 1.05V result and discuss possible reasons for the discrepency (Hint: think about leakage). Note that you will need to increase the clock period of the simulation for lower supply voltages. Make a reasonable assumption: you can either run a simulation to find the FO4 at different voltages to scale appropriately, or use trial and error to set a clock period that still yields correct results in the simulation output.

2. Timing

A logic path is shown in figure. Logic bubbles contain static logic with min and max delays.



a) If the registers R1 and R2 are positive edge triggered ($t_{su} = t_h = t_{clk\text{-}Q}$ = 100ps), what is the minimum clock cycle that this system can operate at? Skew is zero.

b) If R1 and R2 are level –sensitive, label the clock phases so the system operates correctly.

c) What is the shortest clock cycle in a latch-based system ($t_{su} = t_h = t_{clk\text{-}Q} = t_{D\text{-}Q} = 100ps$). Clock has a 50% duty cycle, and you can only use two phases for clocking. Skew is still zero.

d) Repeat c) with worst-case skew of 100ps.

3. Variability and Timing

In this problem we will investigate the impact of various types of variability on our transistor performance. A slide deck will be posted on Piazza with some tips for setting up the various variability simulations.

First record the nominal (TT) FO4 (fan out of 4) low to high and high to low delays of an inverter. You can size the inverter for minimum average delay (as in to homework 1). Make sure to use the 4 cascaded inverters set-up, and measure the delay of the second inverter, as shown in lecture.

a) How does the delay of the inverter change across the various corners (SS, FF, SF and FS)?
b) The transistor models use the Pelgrom mismatch model with Avt = 2mV*um. Run a 300-point Monte Carlo simulation, and report the standard deviation of the delay, as well as the minimum and maximum delays observed.
c) How does the delay of the inverter change if the circuit was operated at 0 and 100 degrees C?
d) If your critical path consisted of 7 FO4 inverter stages, how would you set the nominal clock period? How much slower would the clock have to be set under worst-case global conditions, and 3 sigma threshold variation?