

# EE 241B HW3 Writeup

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## 1 Building and Characterizing a Standard Cell

### 1.1 Flow and Decoder Delay Using Custom Cell

We go through the tutorial to design a custom NAND2 standard cell. We first record the critical path of the 3-8 decoder used in the previous lab with the NAND2 cell supplied with the design kit. The critical path goes from A[3] to Z[5] and it has a delay of 0.1376 ns.

We then tell DC and ICC to use our custom standard cell and we measure the critical path again. The critical path now goes from A[0] to Z[14] and has a delay of 0.1019 ns, which is an improvement over the previous ICC run. However, looking at the final Verilog netlist from ICC only 2 instances of our NAND2X1B\_RVT cell exist. However, after running only DC, there were many instances of our custom cell. It seems that ICC did some optimization and swapped out most of those custom cells for standard cells from the design kit.

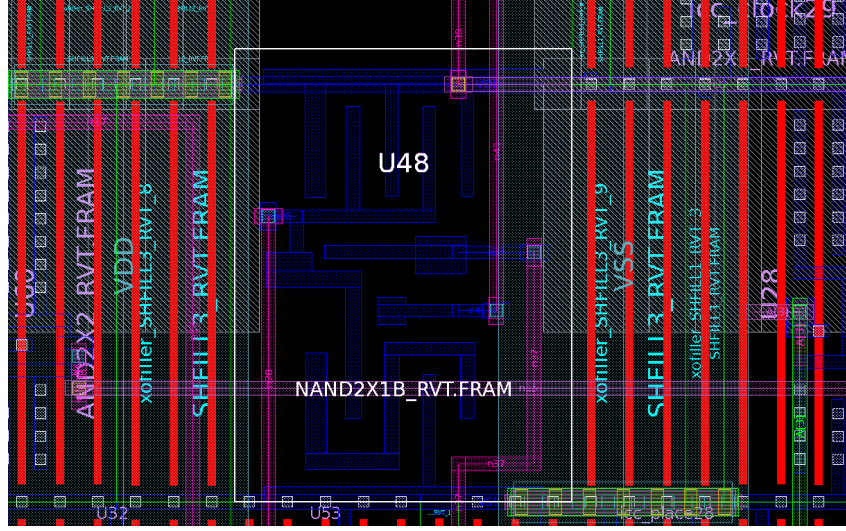


Figure 1: An instance of the NAND2X1B\_RVT cell in ICC with visible M1 polygons.

## 1.2 Standard Cell Inverter Variation Impact vs $V_{DD}$

We run a 300 point Monte Carlo simulation and plot the mean and sigma for the input-rising/output-falling delay of the INVX0\_RVT standard cell for  $V_{DD}$  between 0.2 and 1.05. We fix an input slope of 10ps and a 1fF load. This part was done by exporting a netlist from Virtuoso and using commandline HSPICE for the simulation.

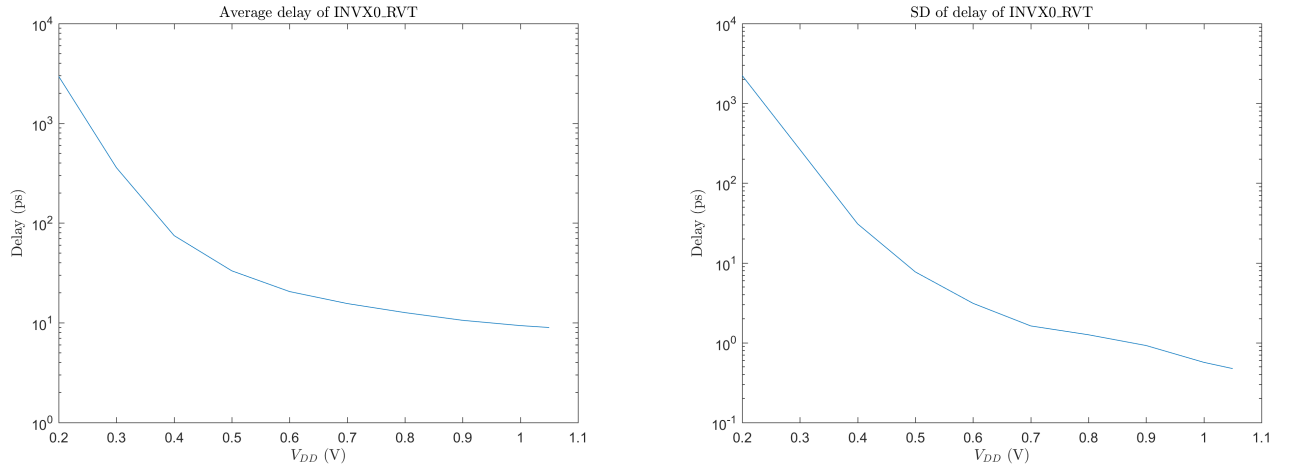
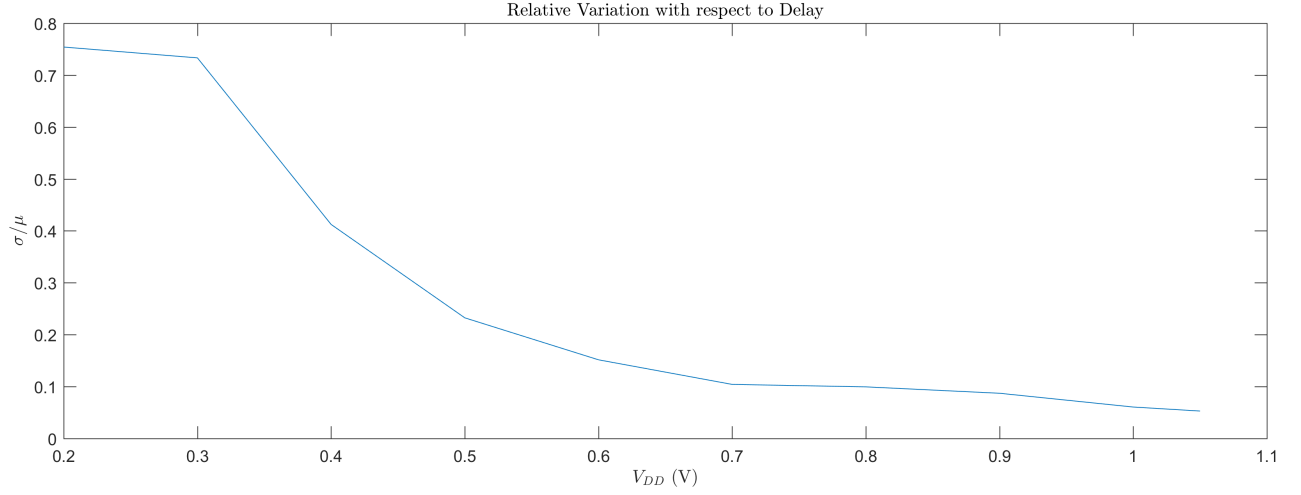
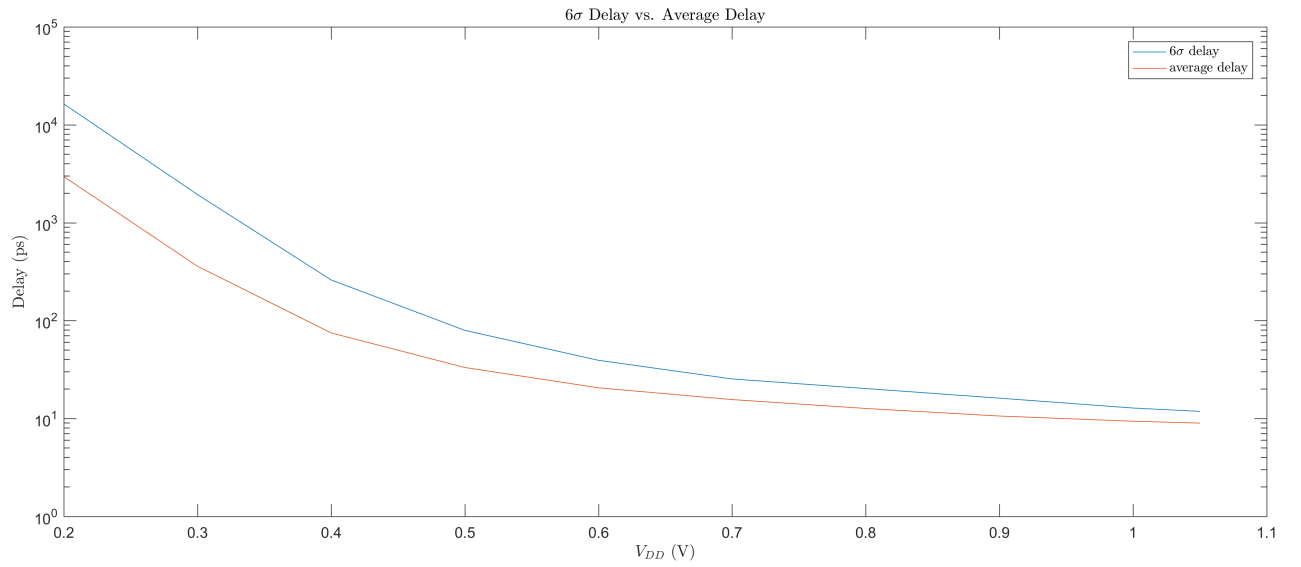


Figure 2: Plot is log-scale in y-axis.

We then plot  $\sigma/\mu$  vs.  $V_{DD}$ .



Finally we plot the delay of a  $6\sigma$  cell relative to the mean vs.  $V_{DD}$ .



Variation has a larger effect at low voltages since our mismatch model works by setting  $V_{th}$  of each transistor using a probability distribution with a  $\sigma_{V_{th}}$ . At lower voltages, the transistor has an operating voltage around its threshold voltage and thus makes the variation more pronounced.

### 1.3 Delay Distributions for Different $V_{DD}$

We create histograms and fit a normal curve for the delay at 0.6V and 1.05V.

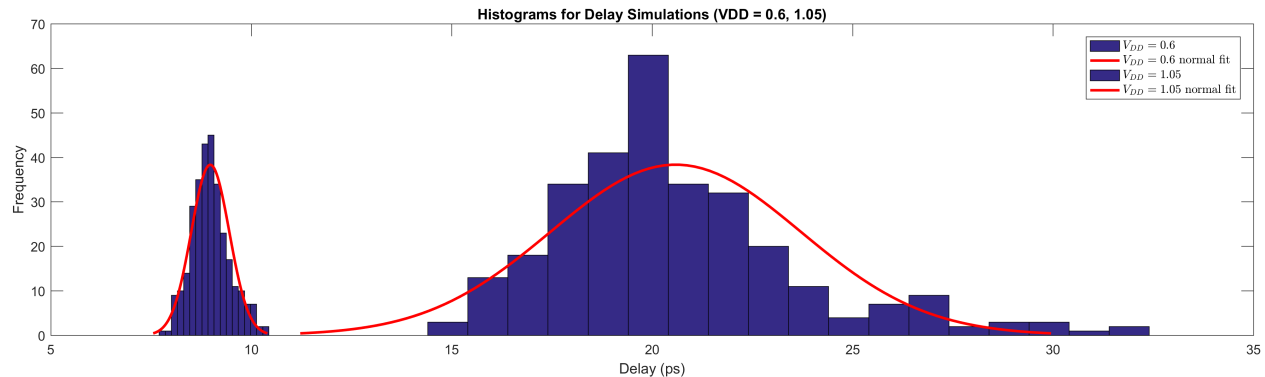


Figure 3: Two histograms that contain delays from the 300 point monte carlo sim. Left histogram is at  $V_{DD} = 1.05V$  and right histogram is at  $V_{DD} = 0.6V$ .

The histogram for  $V_{DD} = 1.05V$  is roughly Gaussian and can be closely approximated with a normal distribution. However the histogram for  $V_{DD} = 0.6V$  is asymmetric and a Gaussian is a poor fit for it. There is a long right tail, and it comes about due to a certain transistor having a much higher  $V_{th}$  which increases its delay a lot more at a lower  $V_{DD}$ .

## 1.4 $\sigma_{V_{th}}$ and Monte Carlo in MATLAB

## 2 Flip-Flops

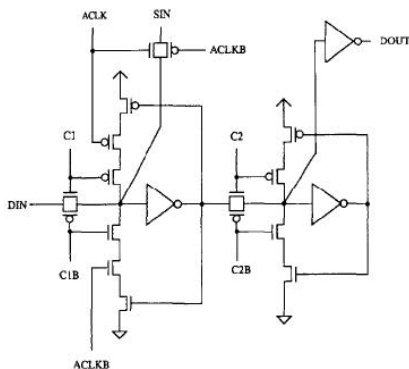


Figure 4: A schematic of a sequential circuit.

### 2.1 Identify Circuit

Assuming that C1 and C2 are opposite phases of the same clock, the circuit above implements a **D-type flip-flop** using a master-slave latch topology.

When C1 is high, the first transmission gate is transparent and the data is allowed to settle at the input of the second transmission gate. At the moment that C2 goes high, C1 goes low to close

off any further input changes, and the output reflects the 'last' value that passed through the first transmission gate while C1 was high.

The rest of the circuitry serves to make the flip-flop static by providing feedback into the storage nodes and there is an additional transmission gate that can be used by a scan chain.

## **2.2 FF Timing Characteristics**

Assuming that the NMOS and PMOS devices have the same mobility and are all symmetrically sized, order the following timing parameters by magnitude: setup time, hold time, clock-output delay.

The setup time is approximately equal to the time it takes for an input signal at DIN to race past the first transmission gate, after which the gate can become opaque. The hold time is close to 0 since after C2 goes high