EE290C Homework 1 Solutions

Chisel Simulation

1) The interpreter is better for small unit tests because it has very low start-up time. For small designs or for a small number of cycles, the start-up time of the Verilator simulator may be as long or longer than the rest of the simulation. However, Verilator is significantly faster after it starts up, so for integration tests that run on larger designs for more cycles it is the superior option.

2) For the interpreter:

$$f_1 \approx \frac{10000 - 10}{0.228 - 0.025} = 49\text{kHz}$$

$$f_{51} \approx \frac{10000 - 10}{19.510 - 0.275} = 519\text{Hz}$$

$$f_{101} \approx \frac{1000 - 10}{3.147 - 0.305} = 318\text{Hz}$$

For Verilator:

$$f_1 \approx \frac{10000 - 10}{1.670 - 1.350} = 31\text{kHz}$$

$$f_{51} \approx \frac{10000 - 10}{1.625 - 1.426} = 50\text{kHz}$$

$$f_{101} \approx \frac{10000 - 10}{1.782 - 1.460} = 31\text{kHz}$$

3) The FPGA is orders of magnitude faster than simulation, but it takes a long time to go from RTL to the FPGA. To find the break-even point, solve

$$T_s + T_c * c = 15 \times 60 + 10^{-7} * c$$

where T_s is the startup time of a simulation method and T_c is the time per cycle of a simulation method.

10^{-7} is negligible compared to each T_c and T_s are negligible compared to 15 minutes, so

$$c \approx \frac{15 \times 60}{T_c}$$

For complexity = 1, the interpreter is best for long simulations and $c \approx 44$ million cycles. For complexity = 51 and 101, Verilator is best for long simulations and $c \approx 28$ million cycles for complexity = 101 and $c \approx 45$ million cycles for complexity = 51.