On the Design of Constant Settling Time AGC Circuits

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***Abstract*— The generalized design of Automatic Gain Control (AGC) circuits that have constant settling time is described. Each of the major components of the AGC circuit is modeled and the criteria to obtain a gain settling time independent of the absolute gain are determined. The method developed works with arbitrary monotonic nonlinear functions in the gain control characteristic of the variable gain amplifier. Several AGC circuits are simulated at the behavioral level to show the benefits of the technique developed.**

***Index Terms*— Automatic gain control, peak detector, programmable gain amplifier, variable gain amplifier.**

I. Introduction

AUTOMATIC Gain Control (AGC) circuits are employed in many systems where the amplitude of an incoming signal can vary over a wide dynamic range. The role of the AGC circuit is to provide a relatively constant output amplitude so that circuits following the AGC circuit require less dynamic range. If the signal level changes are much slower than the information rate contained in the signal, then an AGC circuit can be used to provide a signal with a well-defined average level to downstream circuits. In most system applications, the time to adjust the gain in response to an input amplitude change should remain constant, independent of the input amplitude level and hence gain setting of the amplifier. Achieving a constant gain settling time permits the AGC loop's bandwidth to be maximized for fast signal acquisition while maintaining stability over all operating conditions. A generalized AGC loop is modeled and analyzed in this paper, and criteria are developed for constant settling time gain acquisition. The method developed allows arbitrary monotonic nonlinear gain control functions to be used.

The paper is organized as follows. Section II reviews fundamental issues in the design and application of AGC circuits, and the need for a constant settling time response. An AGC loop model that will be used for derivations throughout the paper is developed, and the classical exponential constraint on the gain characteristic of a Variable Gain Amplifier (VGA), to obtain constant settling time [1]–[4], is derived. Section III generalizes the analysis to obtain AGC constant acquisition time with arbitrary monotonic nonlinear gain control functions. Circuit structures at the block level are shown that can be readily implemented in MOS and other mainstream technologies. Section IV analyzes circuit nonidealities that can impact the performance and stability of the technique developed. Section V provides behavioral level simulations of the various AGC circuits to show the performance that can be achieved; and Section VI discusses the benefits of this technique when applied to digital AGC circuits. Conclusions are provided in Section VII.

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II. AGC Loop Fundamentals

AGC circuits are widely applied in digital communication systems, disk drive read channels, and many other systems as shown in Fig. 1. Usually, error free recovery of data from the input signal cannot occur until the AGC circuit has adjusted the amplitude of the incoming signal. Such amplitude acquisition usually occurs during a preamble where known data are transmitted. The preamble duration must exceed the acquisition or settling time of the AGC loop, but its duration should be minimized for efficient use of the channel bandwidth. If the AGC circuit is designed such that the acquisition time is a function of the input amplitude, then the preamble is forced to be longer in duration than the slowest possible AGC circuit acquisition time. Consequently, to optimize system performance, the AGC loop settling time should be well defined and signal independent.

The AGC loop depicted in Fig. 2 consists of a variable gain amplifier (VGA), a peak detector, and a loop filter. The AGC loop is *in general* a nonlinear system having a gain acquisition settling time that is input signal level dependent. With the addition of the logarithmic function shown in dotted lines and appropriate design of the loop components, the AGC system can operate *linearly in decibels* [4]. This simply means that if the amplitude of the input and output signals of the AGC are expressed in decibels (dB), then the system response can be made linear with respect to these quantities. The derivations that follow will make these issues clear.

Without loss of generality all signals shown will be expressed as voltages. The gain of the VGA, $G(V_C)$, is controlled with the voltage signal V_C. The peak detector and loop filter form a feedback circuit that monitors the peak amplitude, $A_{\rm OUT}$, of the output signal $V_{\rm OUT}$ and adjusts the VGA gain until the *measured* peak amplitude, V_P, is made equal to the DC reference voltage, V_{REF}. The output of the AGC circuit is simply the gain times the input signal: $V_{\rm OUT}(t) = G(V_C)V_{\rm IN}(t)$.

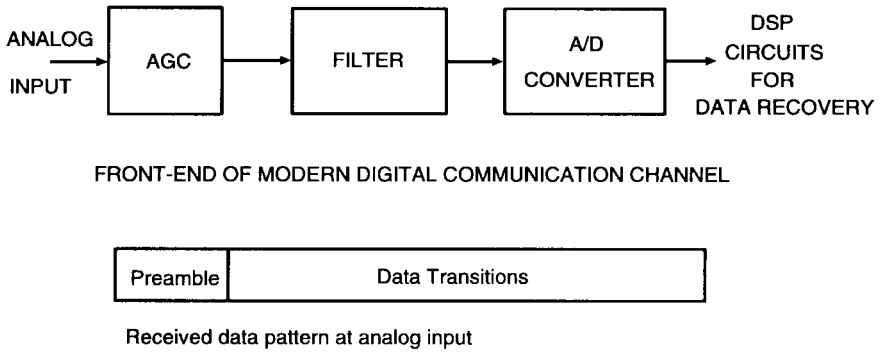

Fig. 1. AGC circuit application.

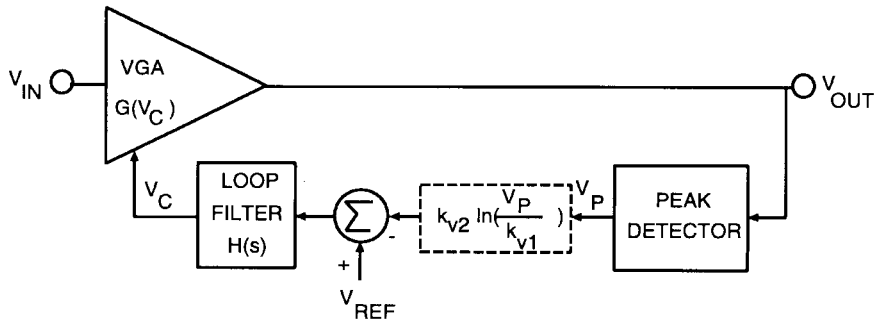

Fig. 2. AGC circuit block diagram.

Since the feedback loop only responds to the peak amplitude, the amplitude of $V_{\rm OUT}$ is

$$A_{\rm OUT} = G(V_C)A_{\rm IN} \tag{1}$$

where $A_{\rm IN}$ is the peak amplitude of $V_{\rm IN}$.

The equivalent representation of an AGC circuit, shown in Fig. 3, is derived as follows. First, the feedback loop of an AGC circuit only operates on signal amplitudes; hence the AGC input and output signals are represented only in terms of their amplitudes $A_{\rm IN}(t)$ and $A_{\rm OUT}(t)$, respectively. Second, since the VGA multiplies the input amplitude, $A_{\rm IN}$, by $G(V_C)$ as shown in (1), an equivalent representation is

$$A_{\rm OUT} = k_{v1} \exp\left[\ln\left[G(V_C)\right] + \ln\left[\frac{A_{\rm IN}}{k_{v1}}\right]\right]. \tag{2}$$

k_{v1} is a constant with the same units as $A_{\rm IN}$ and $A_{\rm OUT}$ (e.g., volts). The AGC model in Fig. 3 uses (2), but duplicates the $k_{v1}\exp(\ )$ function inside and outside the outlined block so that $x(t)$ and $y(t)$ represent the input and output amplitudes of the AGC, expressed in decibels within a constant of proportionality. Similarly, the z input shown is the value of V_{REF} expressed in dB within a constant. The peak detector in Fig. 2 will be assumed to extract the peak amplitude of $V_{\rm OUT}(t)$ linearly and much faster than the basic operation of the loop so that $V_P = A_{\rm OUT}$. Hence, the peak detector is *not explicitly* shown in Fig. 3. Finally, the loop filter in Fig. 2 is shown as an integrator in Fig. 3, with $H(s) = G_{M2}/sC$.

The model in Fig. 3 helps to simplify the mathematical derivations in this section and aids intuition. Similar modeling methods are used in [16] for log-domain filters. Constant settling time operation of the AGC circuit simply requires that the system enclosed in dotted lines with input $x(t)$ and output $y(t)$ be linear. Since $x(t)$ is the input amplitude, $A_{\rm in}(t)$ in decibels and $y(t)$ is the output amplitude $A_{\rm OUT}(t)$ in dB, then a linear response from $x(t)$ to $y(t)$ means the AGC circuit's amplitude response from input to output will be *linear in* dB.

The classical result for constant settling time of the AGC loop will be derived next and will include the logarithmic amplifier shown with dotted lines in Fig. 2. (See the Appendix for the derivation with this logarithmic amplifier removed.) Results of these derivations will be used in the next section where generalized constraints for constant settling time are developed.

The output $y(t)$ in Fig. 3 is given by

$$y(t) = x(t) + \ln\ G(V_C). \tag{3}$$

The gain control voltage is derived as

$$V_C(t) = \int_0^t \frac{G_{M2}}{C}\left\{k_{v1}e^z - k_{v2}\ \ln[e^{y(\tau)}]\right\} d\tau. \tag{4}$$

Taking the derivative of (3) and substituting in the derivative of (4), the following expression is obtained:

$$\frac{dy}{dt} = \frac{dx}{dt} + \frac{1}{G(V_C)}\frac{dG}{dV_C}\frac{G_{M2}}{C}\left[k_{v1}e^z - k_{v2}\ \ln e^{y(t)}\right]. \tag{5}$$

Equation (5) describes a nonlinear system response of $y(t)$ to an input $x(t)$ unless constraints are placed on the functions. Many constraints exist, but here those with practical circuit implementations are analyzed. The first step toward obtaining a linear relationship between $x(t)$ and $y(t)$ is to force the coefficient in the second term of (5) to equal a constant, k_x,

$$\frac{1}{G(V_C)}\frac{dG}{dV_C}\frac{G_{M2}}{C} = k_x. \tag{6}$$

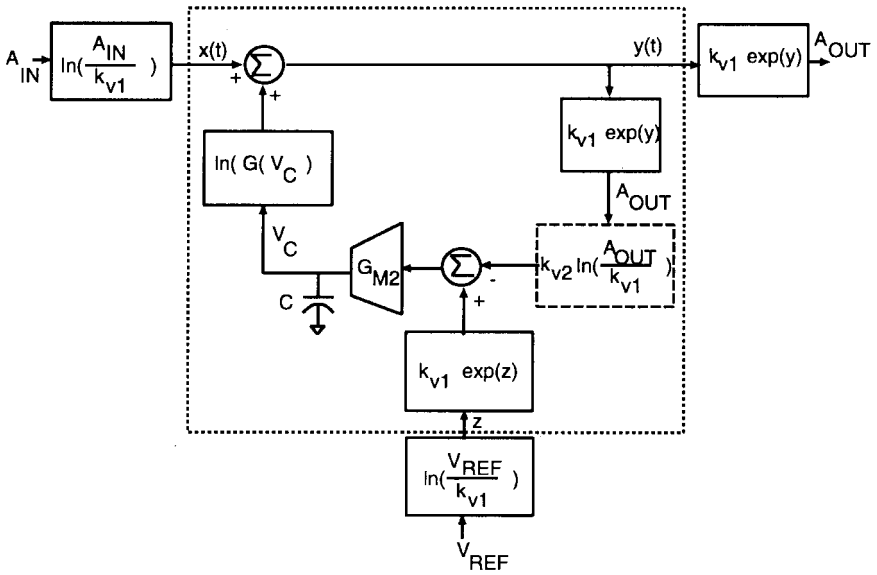

Fig. 3. Model of generalized AGC circuit.

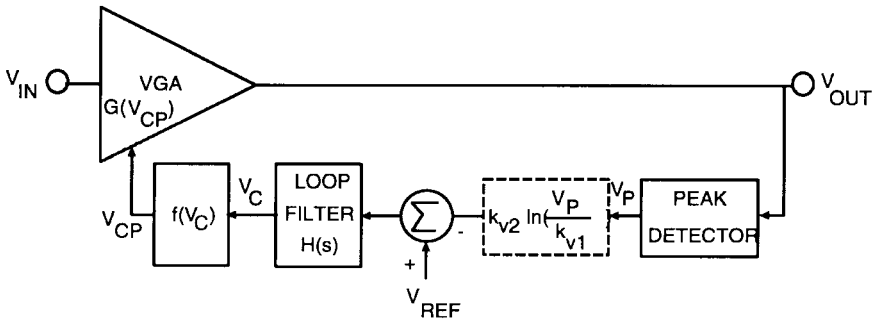

Fig. 4. AGC circuit with predistorted gain control voltage.

Equation (5) can be rewritten with (6) substituted in to yield

$$\frac{dy}{dt} + k_x k_{v2} y(t) = \frac{dx}{dt} + k_x V_{REF} \tag{7}$$

where, from Fig. 3, the equality of $k_{v1}e^z$ to V_{REF} is used. Equation (7) describes a first-order linear system having a high pass response from the input $x(t)$ to the output $y(t)$. The time constant, τ, of the system is given by

$$\tau = \frac{1}{k_x k_{v2}} = \left[\frac{1}{G(V_C)}\,\frac{dG}{dV_C}\,\frac{G_{M2}}{C}\,k_{v2}\right]^{-1}. \tag{8}$$

The classical criterion for constant settling time of the AGC loop assumes that G_{M2} and C are constants in (6) and (8), forcing the gain control function of the VGA to satisfy the following constraint:

$$\frac{1}{G(V_C)}\,\frac{dG(V_C)}{dV_C} = k_{G1} \tag{9}$$

where k_{G1} is a constant. Rearranging this equation and integrating both sides of the resulting equation produces the well-known exponential gain characteristic of the VGA [1]–[4]

$$G(V_C) = k_{G2}e^{k_{G1}V_C} \tag{10}$$

where k_{G2} is a constant of integration. One can easily determine that the gain in decibels (dB) should vary linearly with the control signal, V_C.

Using (10) for an exponential VGA gain characteristic and (8), the time constant of the AGC loop *with* a logarithmic amplifier included, is

$$\tau_{\text{exp-log}} = \frac{C}{G_{M2}k_{G1}k_{v2}}. \tag{11}$$

With the constraints provided, the AGC loop will operate as a linear system in decibels for *any* change in input amplitude. For example, if the input has a step increase in amplitude of 3 dB, the output will have a step increase of 3 dB and decay exponentially to within 1.1 dB of the final value after a single time constant.

III. Generalized Settling Time Constraints

The straightforward method of achieving constant settling time is to design a VGA that has an exponential gain characteristic with respect to V_C as shown in (10). In bipolar or BiCMOS technology, the exponential function is readily available with the base-emitter voltage to collector current characteristic; however, achieving an exponential relationship in CMOS and other technologies is less obvious [8], [9].

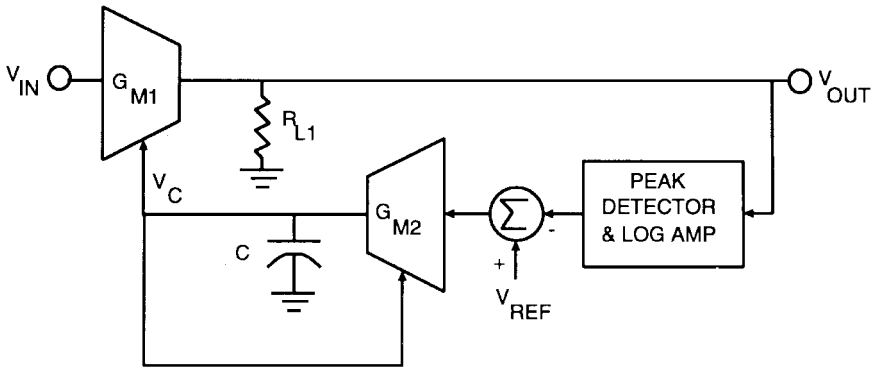

Fig. 5. Constant settling time AGC with VGA gain and G_{M2} linearly controlled by V_C.

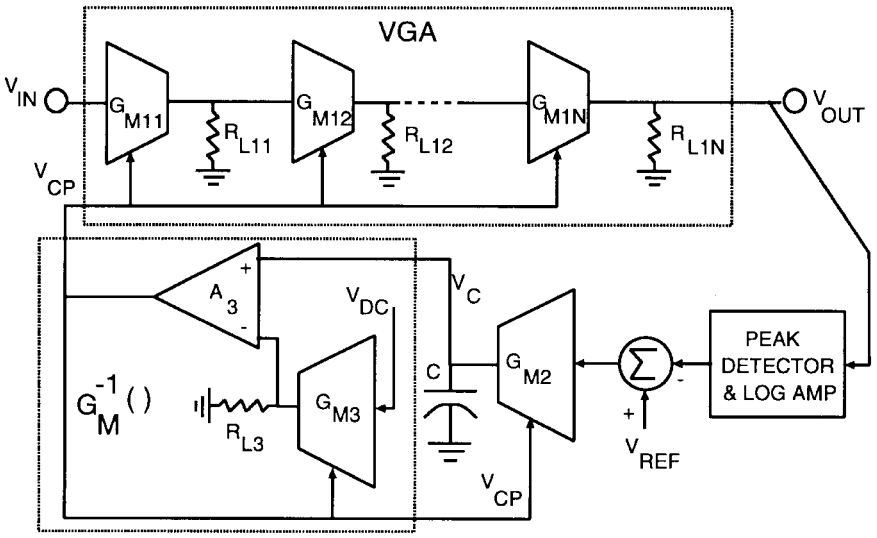

Fig. 6. Constant settling time AGC circuit with arbitrary VGA gain and G_{M2} control characteristic.

Several solutions exist. The first is simply to create a gain function that uses a piecewise linear approximation to the exponential function [5]. Such a method can work reasonably well; however, the derivative of the gain with respect to the control signal, dG/dV_C, will have discontinuities, potentially complicating circuit operation.

The second solution is to predistort the control voltage, V_C, with an additional block prior to the VGA, so that the overall gain response is exponential. This scheme is depicted in Fig. 4. The nonlinear function, $f(V_C)$, is chosen such that $G[f(V_C)] = k_{G2}e^{k_{G1}V_C}$. $f(V_C)$ must be designed with accurate modeling of $G(V_{CP})$ and the target exponential functions.

With both of these solutions, approximation of the exponential function is required; however, maintaining a good fit over all processing and temperature changes may be difficult.

Finally, if the gain function is of the form e^w, the exponential function can be approximated by a function of the form

$$e^w \approx \frac{(1+w/2)}{(1-w/2)}. \tag{12}$$

Circuit implementations for such a function have been used in several AGC circuits [6], [8], [10].

The AGC loop will behave as a first-order linear system in dB if k_x remains signal independent [see (6)]. In classical designs, k_x was held constant by designing the VGA to have an exponential gain characteristic while the ratio G_{M2}/C was held constant. Rather than assuming a linear time invariant loop filter as in classical designs, an additional degree of freedom is obtained if the loop filter is made nonlinear. With this additional degree of freedom, the VGA no longer requires an exponential characteristic. Recently, the general subject of companding and log-domain filters that are externally linear but internally nonlinear has received considerable attention [11]–[14], [16]. The nonlinear filters developed here have similarities to the generalized companding techniques presented in [14].

The nonlinear loop filter can in general have either G_{M2} or C signal dependent. Here, the capacitance is assumed to be fixed and linear, while G_{M2} is signal dependent. Note that although (4) and (5) were derived assuming that G_{M2} and C were constants, the derivation of (5) remains unchanged even when G_{M2} is a function of V_C. Therefore, using (6), the requirement for constant AGC settling time can be rewritten as

$$\frac{G_{M2}(V_C)}{G(V_C)}\,\frac{dG(V_C)}{dV_C} = k_x C = \text{constant}. \tag{13}$$

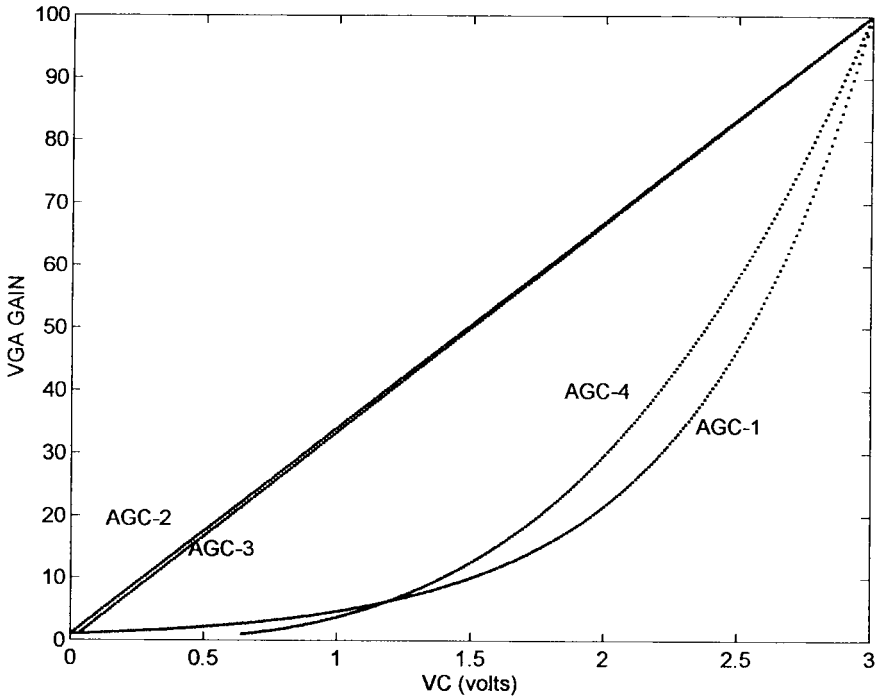

Fig. 7. VGA gain versus V_C for AGC-1, AGC-2, AGC-3, and AGC-4.

Many possible functions $G_{M2}(V_C)$ and $G(V_C)$ exist that will satisfy (13). In this paper, two specific cases that yield practical implementations are considered.

A. Linear Variation of VGA Gain with V_C

First, consider the case where the VGA gain varies linearly with the control voltage, V_C. In this situation, $dG(V_C)/dV_C$ is a constant so (13) will be satisfied if the ratio of $G_{M2}(V_C)$ to $G(V_C)$ is made constant. Equations (14)–(16) below impose constraints on the VGA gain characteristic, and loop filter nonlinearity (i.e., transconductor) in order to satisfy (13).

$$G(V_C) = G_{M1}(V_C)R_{L1} \tag{14}$$

$$G_{M1}(V_C) = k_1 G_M(V_C) = k_1[a_0 + a_1 V_C] \tag{15}$$

$$G_{M2}(V_C) = k_2 G_M(V_C) = k_2[a_0 + a_1 V_C] \tag{16}$$

where k_1, k_2, a_0, and a_1 are constants. An AGC implementation satisfying (13)–(16) is shown in Fig. 5. The VGA gain, $G(V_C)$, is realized with a transconductance amplifier loaded by resistance R_{L1}. This open loop VGA structure is typically used in wideband applications such as in disk drive read channels [8]–[10].

Since the VGA and loop filter use exactly the same gain setting function $G_M(V_C)$, within a constant of proportionality, good tracking over processing and temperature in an integrated circuit (IC) implementation will be achieved and maintaining a constant ratio of $G_{M2}(V_C)/G(V_C)$ in (13) will be obtained. Ideally, the AGC time constant for such a design will be signal independent and will have a value of

$$\tau = \frac{C}{k_2 a_1 k_{v2}}. \tag{17}$$

Linear variation of the VGA gain with the control signal, V_C, is readily achieved in virtually all analog IC technologies since linear elements such as resistors are standard components. Nonideal effects and variation of the AGC settling time due to mismatches in $G_{M1}(V_C)$ and $G_{M2}(V_C)$ are considered in Section IV.

B. Nonlinear Variation of VGA Gain with Control Signal

The constraint of a VGA with a linear relationship to V_C is unnecessary to satisfy (13) and hence yield an AGC circuit that is linear in dB. This section shows that (13) can be satisfied for *any* monotonic nonlinear VGA gain versus control signal relationship provided that G_{M2} has the *same* nonlinear function within a constant of proportionality.

If the inverse function of the nonlinearity can be generated electrically, then G_{M2} can be made to vary linearly with V_C and the gain per stage in a multistage VGA will also vary linearly with V_C. The AGC operation, except the circuit to generate the inverse function, can then be modeled analogously to that shown in Fig. 5.

The generalized AGC loop structure achieving constant gain acquisition settling time with arbitrary monotonic nonlinearities in the gain control function is shown in Fig. 6. For generality, the VGA is assumed to be a multistage amplifier. The VGA gain $G(V_{CP})$ and integrator transconductance $G_{M2}(V_{CP})$ are nonlinear with respect to V_{CP}.

All the transconductance amplifiers in the VGA of Fig. 6 have the same nonlinear controlling function, $G_M(V_{CP})$, except for a constant of proportionality, k_{ij}. The transconductances in the VGA are

$$G_{M1j}(V_{CP}) = k_{1j} G_M(V_{CP}), \qquad \text{for} \quad j = 1, \cdots, N \tag{18}$$

and the remaining two transconductances are

$$G_{Mi}(V_{CP}) = k_i G_M(V_{CP}), \qquad \text{for} \quad i = 2, 3. \tag{19}$$

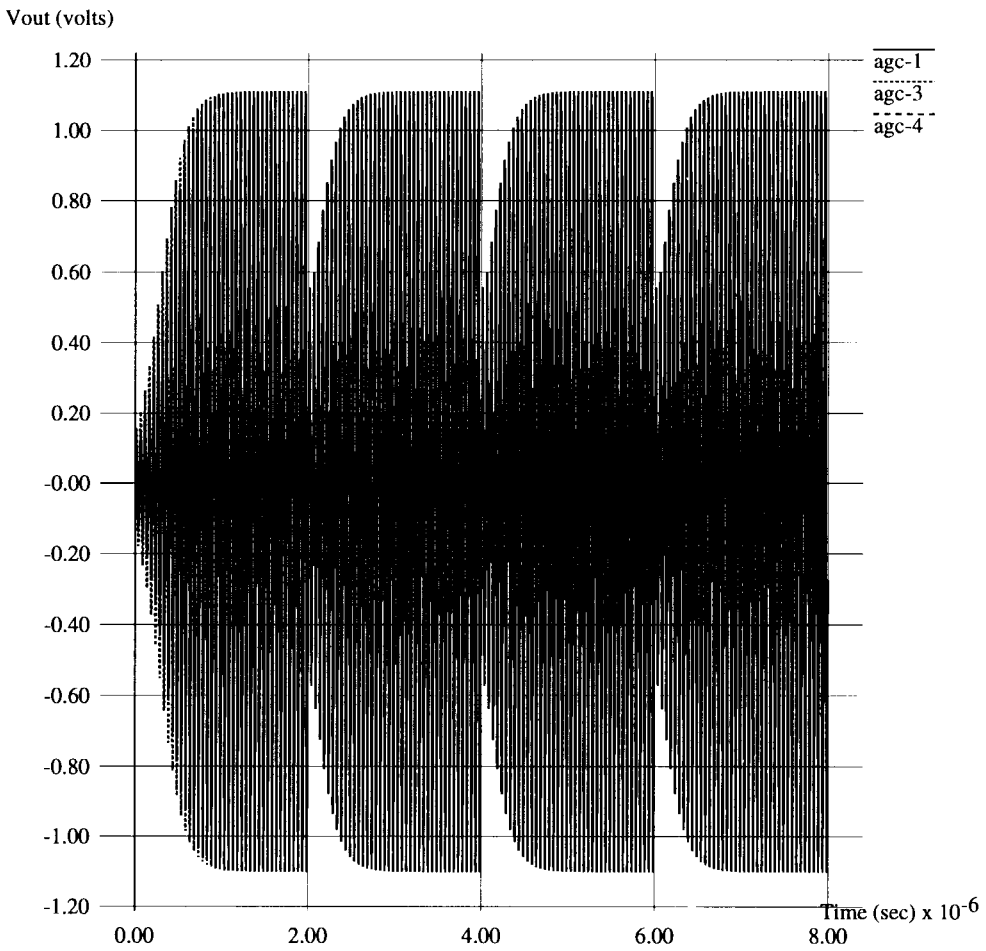

Fig. 8. Responses of AGC-1, AGC-3, and AGC-4 to a 20 MHz sinusoidal input initially at 100 mV_{pk}, decreasing by 6 dB every 2 μs.

Transconductance $G_{M3}(V_{CP})$ replicates the nonlinearity of the VGA and integrator transconductors and is used to generate the inverse transconductance function. The negative feedback loop with the ideal opamp, A_3, forces $V_C = k_3 G_M(V_{CP}) V_{DC} R_{L3}$; hence, the inverse function is generated as

$$V_{CP} = G_M^{-1}\left(\frac{V_C}{k_3 R_{L3} V_{DC}}\right). \tag{20}$$

For the inverse function ${G_M}^{-1}(\cdot)$ to exist, $G_M(\cdot)$ must be monotonic.

The VGA gain is the product of the gains of the N stages and is

$$G(V_{CP}) = \prod_{j=1}^{N} k_{1j} G_M(V_{CP}) R_{L1j}. \tag{21}$$

Using (20), the VGA gain as a function of V_C is

$$G(V_C) = \left[\frac{V_C}{k_3 R_{L3} V_{DC}}\right]^N \prod_{j=1}^{N} k_{1j} R_{L1j}. \tag{22}$$

Similarly, the variation of the loop filter's transconductance is

$$G_{M2}(V_C) = \frac{k_2 V_C}{k_3 R_{L3} V_{DC}}. \tag{23}$$

Using (8), (22), and (23), the overall time constant of the AGC circuit in Fig. 6 can be derived to be

$$\tau_{LOOP\text{-}NL} = \frac{C R_{L3}}{N} \frac{k_3}{k_2} \frac{V_{DC}}{k_{v2}}. \tag{24}$$

Note that this derivation assumed that the logarithmic amplifier was used in the AGC loop so the circuit will behave linearly in dB for large and small signals. If the logarithmic amplifier is not used, then (24) should be modified by substituting V_{REF} in place of k_{v2}. (See the Appendix.)

Examining the circuits in Figs. 5 and 6, the feedback loop can become broken *indefinitely* if the variable transconductance of the integrator becomes zero. With the appropriate design of $G_{M2}(V_C)$ in Fig. 5, the zero gain state can be prevented. In contrast, the integrator of Fig. 6 will become disabled if V_C ever becomes zero independent of the nonlinearity design [see (22)]. Therefore, any practical circuit implementation would require an additional nonlinearity, such as a clamp, to prevent V_C from reaching zero. Referring to Fig. 6 and (22), notice that to maintain nonzero VGA gain, V_C must also be nonzero.

IV. Analysis of Circuit Nonidealities

Several nonidealities can occur that will impact the performance of the constant settling time approach using arbitrary

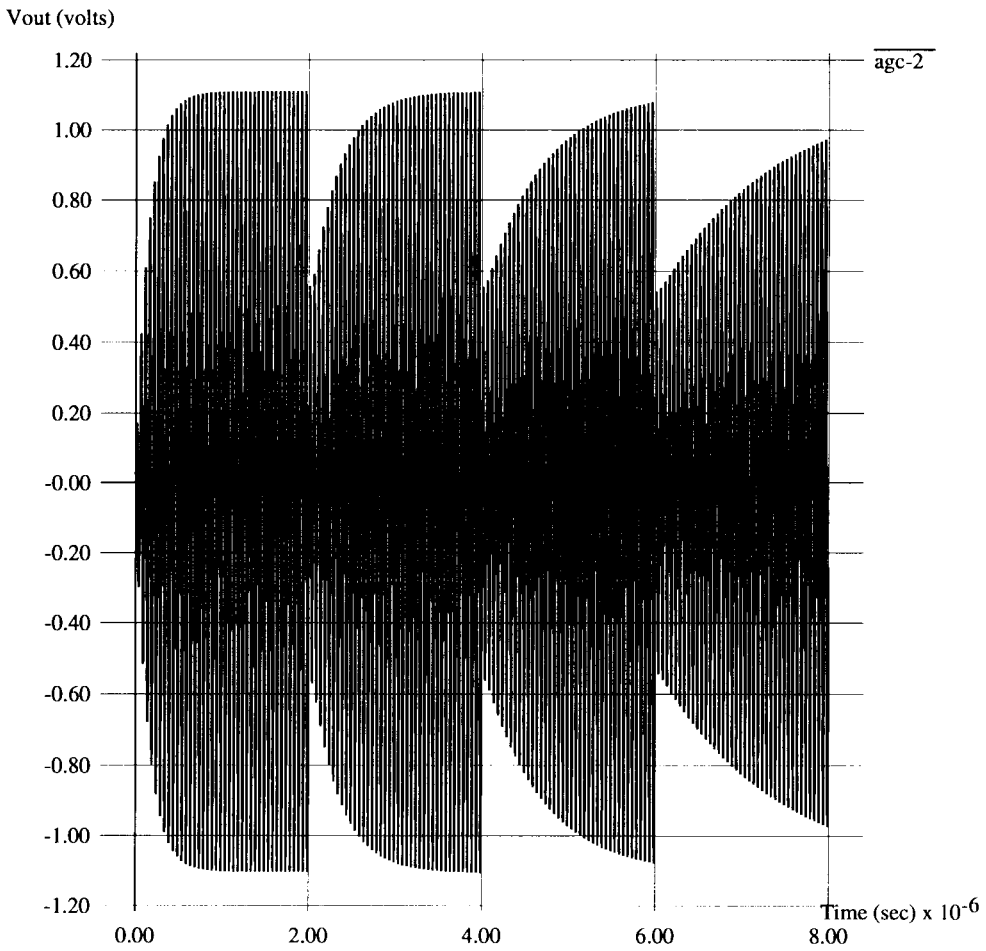

Fig. 9. Response of AGC-2 to a 20 MHz sinusoidal input initially at 100 mV_{pk}, decreasing by 6 dB every 2 μs.

nonlinear VGA gain functions. The approaches developed in this paper, depicted in Figs. 5 and 6, achieve a fixed settling time constant provided that all the variable transconductance amplifiers track one another. Below, the effect of mismatches on the resulting settling time is analyzed. Additionally, the stability of the feedback loop in the inverse transconductance generation circuit of Fig. 6 is analyzed.

A. Mismatch Effects

An AGC circuit that has a fixed acquisition time independent of input signal level equivalently has a fixed time constant independent of the VGA gain setting. To examine small matching errors, it is instructive to evaluate the sensitivity of the time constant, τ, with respect to the gain setting. Using the classical definition of sensitivity

$$S_G^\tau = \frac{G}{\tau}\frac{\partial \tau}{\partial G} = \frac{G}{\tau}\frac{\partial \tau}{\partial V_C}\frac{1}{\dfrac{\partial G}{\partial V_C}}. \tag{25}$$

Using the expression for τ in (8), the sensitivity can be evaluated as

$$S_G^\tau = 1 - \frac{G}{G_{M2}}\frac{\dfrac{\partial G_{M2}}{\partial V_C}}{\dfrac{\partial G}{\partial V_C}} - G\frac{\dfrac{\partial^2 G}{\partial V_C^2}}{\left[\dfrac{\partial G}{\partial V_C}\right]^2}. \tag{26}$$

As an example, the sensitivity of τ to G for an AGC with linear VGA gain control as in Fig. 5 is analyzed. Assume that the VGA gain is given by (14) and (15), while the transconductance, $G_{M2}(V_C)$, is given by

$$G_{M2} = k_2[a_0(1+\alpha) + a_1(1+\beta)V_C] \tag{27}$$

where α and β represent mismatch effects. The sensitivity of τ to the VGA gain is then

$$S_G^\tau = 1 - \frac{a_0(1+\beta) + a_1(1+\beta)V_C}{a_0(1+\alpha) + a_1(1+\beta)V_C}. \tag{28}$$

Clearly for high gain, $V_C \gg (a_0/a_1)$, the sensitivity approaches zero. For low gain, $V_C \ll (a_0/a_1)$, the sensitivity is approximately $S_G^\tau \approx \alpha - \beta$. Although the sensitivity of the settling time is not zero at low gain settings, it is linearly related to the mismatches of the transconductance amplifiers. Since in modern IC technologies, matching of like devices can be better than 0.5%, the AGC settling time will remain nearly constant.

The sensitivity of the settling time for the circuit of Fig. 6 can be derived using (8) and will be similar to that of the AGC in Fig. 5, because the inverse transconductance generating function (implemented with G_{M3} and associated circuits) forces both G_{M1} and G_{M2} to vary linearly with V_C. However, the additional matching requirement of G_{M3} to G_{M1} and G_{M2}

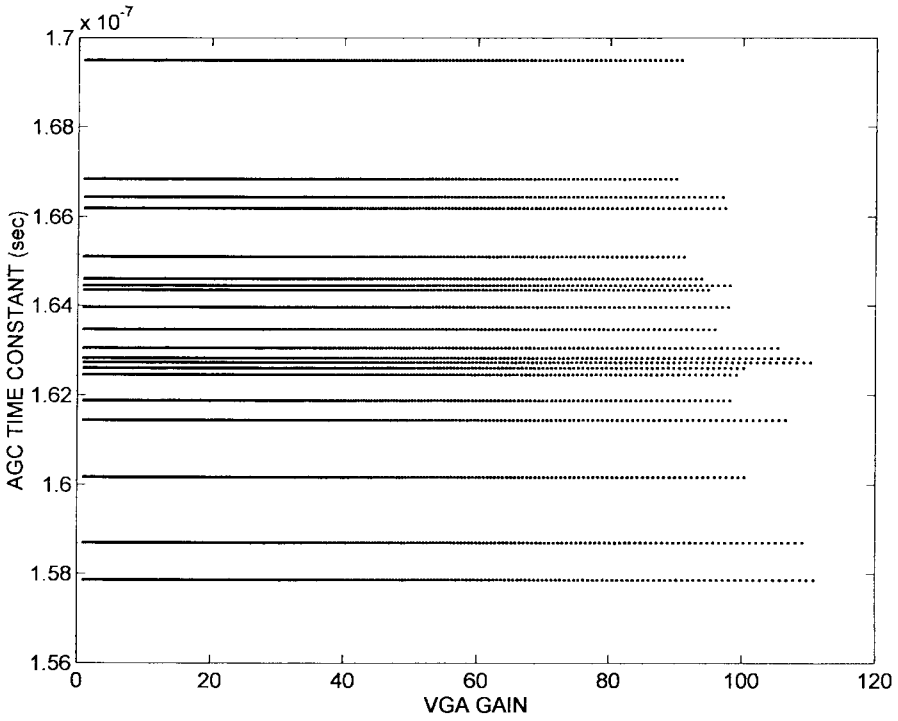

Fig. 10. AGC-1 settling time versus gain for $\pm 2\%$ variations.

will result in a higher sensitivity. Simulations for this case are presented in Section V.

B. Stability of $G_M^{-1}(\ )$ Circuit

The $G_M^{-1}(\ )$ circuit in Fig. 6 contains a negative feedback loop that is now examined for stability by deriving the gain around the loop of G_{M3}, R_{L3}, and A_3. Assume first that amplifier A_3 can be modeled with a single dominant pole, ω_{P1}, and has a DC gain of $A_3(0)$. Also assume that a delay exists between the assertion of the control signal V_{CP} and the changing of the transconductance G_{M3}. Such delay can be modeled with a single pole at frequency ω_{P2}. The small-signal loop gain is of the form

$$T(s) = A_3(s)\left[\frac{1}{s/\omega_{p2}+1}\right]\frac{\partial V_x}{\partial V_{CP}} \tag{29}$$

where V_X is the voltage developed across R_{L3}. In general, $G_{M3}(V_{CP})$ will be nonlinear with respect to V_{CP} and can be expressed in a series as

$$\begin{aligned} G_{M3}(V_{CP}) &= k_3 G_{M3}(V_{CP}) \\ &= k_3[b_0 + b_1 V_{CP} + b_2 V_{CP}^2 + b_3 V_{CP}^3 + \cdots]. \end{aligned} \tag{30}$$

The loop gain is then

$$\begin{aligned} T(s) = &\left[\frac{A_3(0)}{s/\omega_{p1}+1}\right]\left[\frac{1}{s/\omega_{p2}+1}\right] R_{L3} V_{DC} k_3 \\ &\cdot [b_1 + 2b_2 V_{CP\text{-}op} + 3b_3 V_{CP\text{-}op}^2 + \cdots]. \end{aligned} \tag{31}$$

$V_{\text{CP-op}}$ is the bias point at which the small-signal linearization is performed. Stability of the feedback loop can be guaranteed over all possible values of $V_{CP\text{-}op}$ with known phase-lag and phase-lead and compensation techniques [15].

V. AGC Circuit Simulations

Behavioral level simulations are given in this section to compare the operation of four different AGC amplifier designs. The first set of simulations shows the basic operation of the AGC's, while the second set evaluates the settling time with random mismatches. For simplicity, none of the AGC circuits uses the logarithmic amplifier shown with dotted lines in Fig. 2.

The AGC amplifiers are designed to the following high-level specifications: 1) gain range from 0 to 40 dB; 2) nominal output level of 1 V_{peak}; 3) input frequency range from 20 to 100 MHz; 4) nominal gain acquisition time constant of $0.163\ \mu$s; 5) peak detector droop rate of 5 V/μs; and 6) V_C range from 0–3 V, maximum.

The peak detector will be modeled as instantaneously capturing positive peaks; however, in the absence of a peak, the detector will droop at a constant rate. This model is analogous to most IC designs that use a capacitor to hold the peaks and a constant current source for droop.

All four designs use an integrating capacitor of $C = 25$ pF in the loop filter and the peak detector hold capacitor is chosen to be 2 pF with a droop current of 10 μA.

- **AGC-1—** *VGA with Exponential Gain Control:* This VGA circuit is a classical design obeying (10) with parameters: $k_{G1} = 1.535, k_{G2} = 1.0$, and $G_{M2} = 100\ \mu$A/V. No clamping is provided on V_C.
- **AGC-2—** *VGA with Linear Gain Control:* The gain equation of this VGA is $G(V_C) = 1.0 + 33.0V_C$. The overall AGC structure is given in Fig. 2 with no corrective action taken to maintain constant loop dynamics. Since the settling time will vary with gain level, the loop time constant was designed to the $0.163\ \mu$s at a gain level

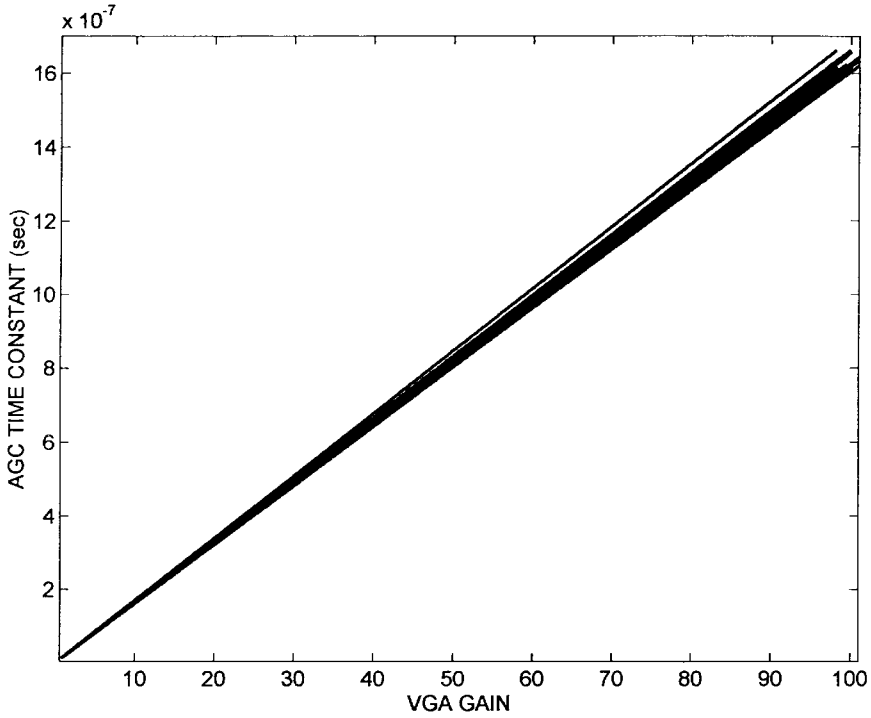

Fig. 11. AGC-2 settling time versus gain for $\pm 2\%$ variations.

of 20 dB. The transconductance amplifier in the loop filter has a gain of $G_{M2} = 46.5$ μA/V. No clamping is provided on V_C.

- **AGC-3—** *VGA with Arbitrary Monotonic Nonlinear Gain Gontrol (1 stage):* This circuit is a single-stage version of the AGC circuit shown in Fig. 6 (i.e., $N = 1$). The constants in the nonlinear transconductance gain function, $G_M(V_{CP})$, given by (30), are $b_0 = 0.001, b_1 = 0.04, b_2 = 0.002$, and $b_3 = -0.002$. These chosen parameters provide a gently saturating transconductance characteristic as V_{CP} approaches 3 V. The other circuit parameters in (22)–(24) are: $k_{11} = 1.0, k_2 = 1.535 \times 10^{-1}, k_3 = 1.0, R_{L11} = 33.3$ kΩ, $R_{L3} = 1.0$ kΩ and $V_{DC} = 1.0$ V. To prevent the feedback loop from becoming disabled, V_C is prevented from reaching 0 volts and is clamped from 30 mV to 3 V to cover the entire gain range.
- **AGC-4—** *VGA with Arbitrary Monotonic Nonlinear Gain Gontrol (3 stages):* This circuit is a three-stage version of the AGC circuit shown in Fig. 6. The circuit parameters for this circuit are the same as AGC-3 except that $R_{L11} = R_{L12} = R_{L13} = 1.547$ k$\Omega, k_2 = 5.117 \times 10^{-2}$, and V_C is clamped to a minimum level of 0.645 V.

The VGA gains are plotted versus V_C for all the circuits in Fig. 7. Note that the nonlinearity correction has already been applied to AGC-3 and AGC-4 in Fig. 7. Hence, the gain of AGC-3 is linear with V_C and the gain of AGC-4 increases as ${V_C}^3$ since a three stage VGA is employed. [See (22).] Note that although AGC-2 and AGC-3 show a linear gain response to V_C, the circuits behave quite differently because AGC-2 has a fixed-loop filter where as AGC-3 has a nonlinear filter.

Each of the circuits was driven with a 20 MHz sine wave whose initial input amplitude was 100 $\mathrm{mV_{pk}}$, but every 2 μs the input signal strength was reduced by 6 dB. The response of AGC-1, AGC-3, and AGC-4 to this input signal is shown in Fig. 8. Except for a small difference in the initial startup transient, the responses are indistinguishable, as expected. In contrast, the response of AGC-2 shown in Fig. 9 has a gain acquisition response time that increases as the input signal amplitude decreases [7]. AGC-1, AGC-3, and AGC-4 settle to within 5% (i.e., 0.4 dB) of the final value within 0.5 μs as expected (i.e., 3τ), whereas the AGC-2 settling varies widely [7]. Simulation of the AGC circuits with increasing input signal strength shows similar results.

A. Settling Time with Random Mismatches

The settling time of the four AGC circuits is now evaluated when random component variations are considered. For each AGC circuit, the parameters were permitted to vary randomly by ± 2 and 20 simulations were performed over the full range of the control voltage V_C. The settling time was evaluated numerically based on (8) and plotted as a function of the VGA gain.

The settling time of AGC-1 is plotted in Fig. 10 under the conditions of random errors in G_{M2}, k_{G1}, and k_{G2}. The settling time remains independent of the gain as expected, but does vary due to the random errors. The settling time of AGC-2 is plotted versus gain in Fig. 11 for random variation of a_0 and a_1. As expected, the dominant settling time variation is proportional to the VGA gain, but the random component variations change the slope of this characteristic. The settling time of AGC-3 is plotted versus gain in Fig. 12 for independent random variations in each b_i of G_{M1}, G_{M2}, and

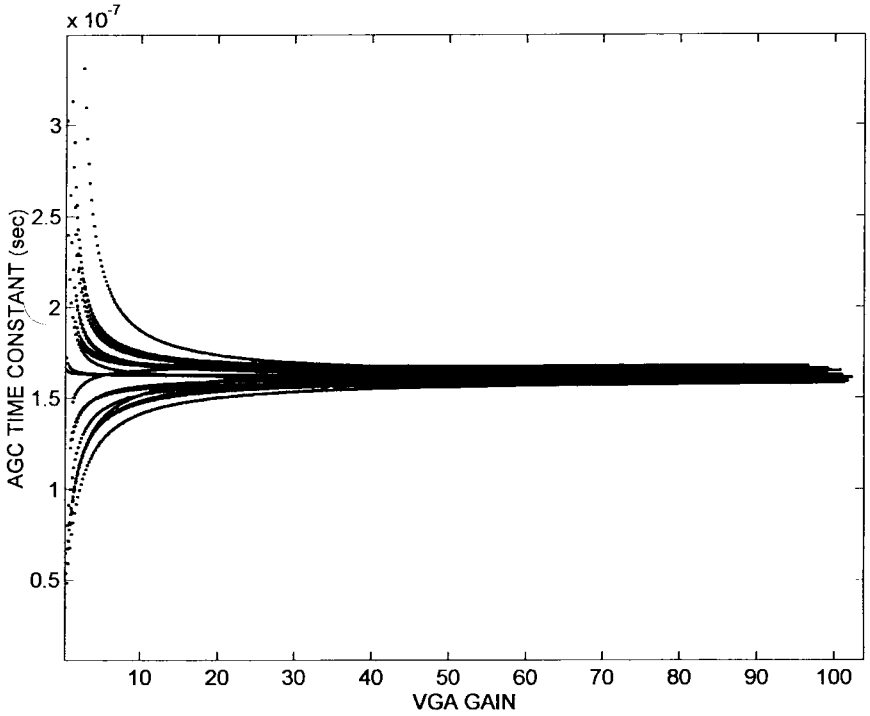

Fig. 12. AGC-3 Settling time versus gain for $\pm 2\%$ variations.

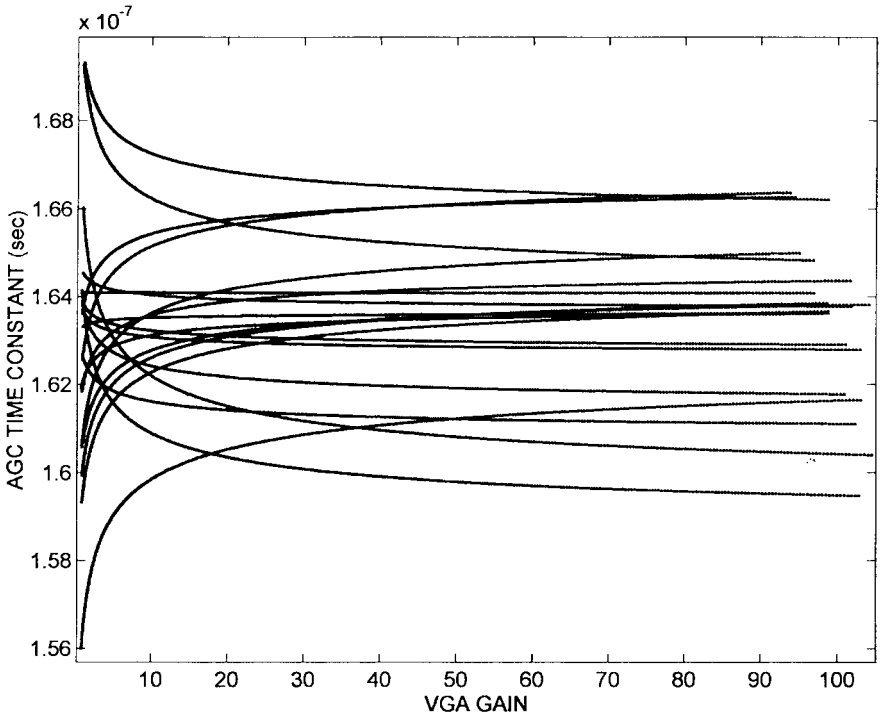

Fig. 13. AGC-4 settling time versus gain for $\pm 2\%$ variations.

G_{M3}. The variation in settling time is maximum at low VGA gain and converges to the nominal value at higher gain levels. This observation is consistent with the sensitivity derivations in Section IV. Finally, the settling time of AGC-4 is plotted versus gain in Fig. 13 for independent random variations in each b_i of $G_{M11}, G_{M12}, G_{M13}, G_{M2}$, and G_{M3}. The variation in settling time is maximum at low VGA gain and converges to the nominal value at higher gain levels.

Clearly constant settling time can be met in practice with the circuit concepts developed and with the matching levels available in modern IC technologies.

VI. Digital AGC Loops

The concepts developed in the paper are fully applicable to digital AGC loops. Consider the digital AGC loop in Fig. 14 that is modeled after the analog design of Fig. 5. The digital

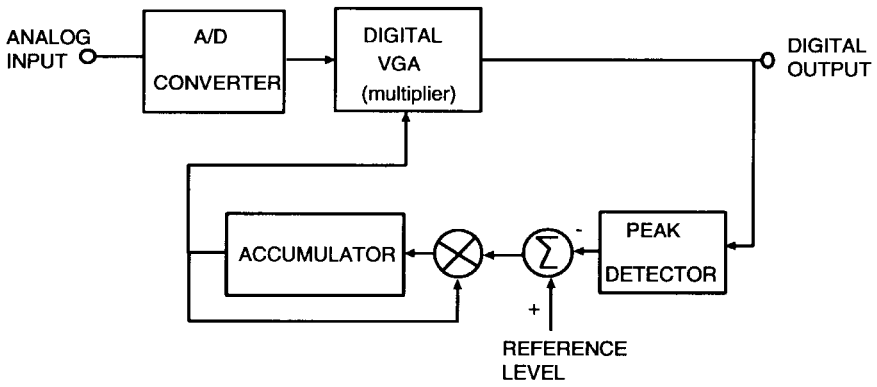

Fig. 14. Digital AGC loop.

VGA is implemented with a multiplier so its gain will vary linearly with the output of the accumulator. The accumulator, a discrete-time integrator, requires a gain that is proportional to its output level in order for the AGC algorithm to have a fixed settling time. The nonlinear accumulator is achieved by preceding the linear accumulator with a multiplier. The approach in Fig. 14, requires only two multiply operations. In contrast, if a linear accumulator and exponential VGA were used, evaluation of the exponential function via a series expansion would require a large number of multiply operations. The approach in Fig. 14 clearly has computational advantages. Mixed analog–digital AGC loops that use an analog VGA with gain proportional to control signal can also benefit from the technique developed.

VII. Conclusions

This paper has developed a general method of achieving constant gain acquisition times in AGC circuits without the need for a VGA with an exponential gain control characteristic. In analog implementations, the method uses matched transconductance amplifiers with arbitrary monotonic gain control characteristics to achieve the constant settling time. Matching transconductance amplifier characteristics within a few percent is readily achievable in IC technologies and is adequate to obtain robust designs based on the technique developed. The AGC loop technique can be applied to digital or mixed analog–digital AGC circuits, and often results in less multiply operations than existing techniques. Constant gain settling time design permits the speed of the AGC acquisition to be maximized while maintaining stability. Additionally, having well-defined loop dynamics eases the implementation of stable AGC circuits and may facilitate the use of higher order loop filters.

Appendix
AGC Loop Without Log Amplifier

In many AGC systems, the logarithmic amplifier shown with dotted lines in Fig. 2 is omitted. The objective of constant settling time can still be met under certain *small-signal* approximations. The key assumption in the following derivation will be that the output amplitude of the AGC loop is operating near its fully converged state (i.e., $A_{\rm OUT} \approx V_{\rm REF}$).

Using (5) and (6) and eliminating the logarithmic function in Fig. 2 shown with dotted lines, the following relationship is obtained:

$$\frac{dy}{dt} = \frac{dx}{dt} + k_x[V_{REF} - k_{v1}e^{y(t)}]. \tag{32}$$

The system response is nonlinear even with a constant k_x due to $e^{y(t)}$. If the changes in the input and output amplitude levels are small, then the exponential $e^{y(t)}$ in (32) can be expanded in a Taylor series. Assume that the AGC loop is initially converged, such that the output amplitude, $A_{\rm OUT}$, equals $V_{\rm REF}$. Referring to Fig. 3, this implies that $y(t) = z$ and the Taylor series expansion is

$$e^{y(t)} \approx e^z[1 + y(t) - z + \cdots]. \tag{33}$$

Since $k_{v1}e^z = V_{REF}$, (32) can be rewritten as

$$\frac{dy}{dt} + k_x V_{REF}\ y(t) = \frac{dx}{dt} + k_x V_{REF}\ \ln\left(\frac{V_{REF}}{k_{v1}}\right). \tag{34}$$

The first-order linear system described by (34) has a high pass response with a time constant of

$$\tau = \frac{1}{k_x V_{REF}} = \left[\frac{1}{G(V_C)}\ \frac{dG}{dV_C}\ \frac{G_{M2}}{C}\ V_{REF}\right]^{-1}. \tag{35}$$

If the loop filter components G_{m2} and C are linear and time invariant, then the constraint on constant settling time for the AGC loop is that the VGA has an exponential gain control characteristic as in (10). Under these conditions, the AGC loop *without* a logarithmic amplifier has a time constant given by

$$\tau_{\rm exp} = \frac{C}{G_{M2}k_{G1}V_{REF}}. \tag{36}$$

Notice that the settling time is a function of the input variable, V_{REF}, indicating the system is fundamentally nonlinear. By changing V_{REF}, the operating point where the small-signal approximation was made changes, and hence the AGC loop parameters change, as should be expected. In contrast, notice in (11) the time constant is independent of any "bias" quantities since the AGC loop is perfectly modeled as a linear system, for input/output quantities in decibels.

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