Analog AGC Circuitry for a CMOS WLAN Receiver

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***Abstract*—The IEEE 802.11a standard uses orthogonal frequency division multiplexing (OFDM) to allow high data rates in multipath WLAN environments. The high peak-to-average power ratio (PAPR) of OFDM signals, along with stringent settling-time constraints, make conventional closed-loop automatic gain control (AGC) schemes impractical for WLAN receivers. In a direct conversion receiver, AGC and channel-select filtering are performed by analog baseband circuitry. A baseband signal processor using a new open-loop analog gain-control algorithm for OFDM is described. The new AGC algorithm uses switched coarse gain-setting steps followed by an analog open-loop fine gain-setting step to set the final gain of variable gain amplifiers (VGAs). The AGC was implemented in a 0.18-μm CMOS process using newly designed circuits including linear VGAs, RMS detectors, and current-mode computation circuitry. Simulation and measurement results verify that the new AGC circuit converges with gain error less than 1 dB to the desired level within 5.6 μs.**

***Index Terms*—Automatic gain control (AGC), CMOS integrated circuits, IEEE 802.11a, OFDM, translinear circuits, variable gain amplifier (VGA), wireless LAN.**

I. Introduction

AUTOMATIC gain control (AGC) is an essential function in wireless local-area network (WLAN) receivers because the power received through the wireless channel is unpredictable. The AGC circuitry maintains a desired output signal amplitude with input signals of variable strength. In the IEEE 802.11a WLAN system, data pass through the channel in packets consisting of preamble, header and data segments. The receiver estimates the channel's characteristics during reception of the preamble. These characteristics are assumed to stay constant throughout the transmission of the whole packet, typically up to 1 ms. The preamble consists of 10 repetitions of a predefined data stream called a short training symbol (10×0.8 μs) and two repetitions of a long training symbol (2×4 μs). While multipath effects can significantly alter the waveform, the channel characteristics change slowly enough to be considered constant throughout the entire packet. Thus, the received signal is essentially repeated during each short training symbol time, and its characteristics are used to establish the amplitude and phase references for the whole packet. In the proposed receiver system, seven of the repeated short training symbols (5.6 μs) are used for AGC convergence [1]. Once the gain has been optimized, the rest of the preamble time is available to the digital signal processor (DSP).

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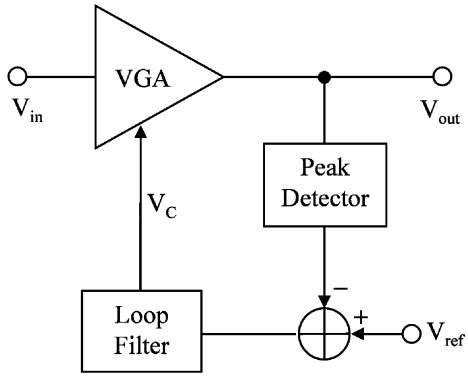

Fig. 1. Conventional AGC loop composed of VGA, peak detector, and loop filter.

Conventional closed-loop analog AGCs use feedback loops to adjust the gain of the variable-gain amplifiers (VGA) to get the desired output signal strength. In such AGC loops, as shown in Fig. 1, signal amplitude is typically estimated using a peak detector. This adequately represents the amplitude of signals with fixed peak-to-average power ratio (PAPR) such as sinusoids, but is unreliable for high-PAPR signals. The problem is worsened by the short time (0.8 μs) available for estimating amplitude in 802.11a applications. For proper operation of closed-loop AGCs, the time to determine amplitude must be much less than the time constant of the loop filter [2]. As the input amplitude changes, the detected output amplitude is compared to the desired DC amplitude and the difference error is fed back to adjust the gain of the VGA to provide constant output amplitude. The negative feedback loop continuously responds to input amplitude variation, but for stability the loop response must be slow.

These issues precluded the use of a conventional AGC loop in this application. The baseband processor presented here uses a new open-loop AGC algorithm. The AGC uses pseudo-RMS detection, which has been found to be adequate for estimating OFDM amplitude using received 0.8 μs short training symbols [3]. The AGC sets gain to within 1 dB of its optimal value within the time for seven short training symbols.

Many WLAN receivers use digital signal processing to implement much of the AGC function. Implementing the AGC in analog circuitry offers lower system power, allowing the DSP to sleep most of the time, using the analog chain to monitor activity. The analog approach presented here can also reduce circuit complexity by eliminating digital-to-analog conversion for the gain control, and avoiding the need for calibrated gain stages.

Section II of this paper describes the receiver architecture and the gain and filtering requirements for the analog baseband signal chain. Section III describes the new open-loop AGC

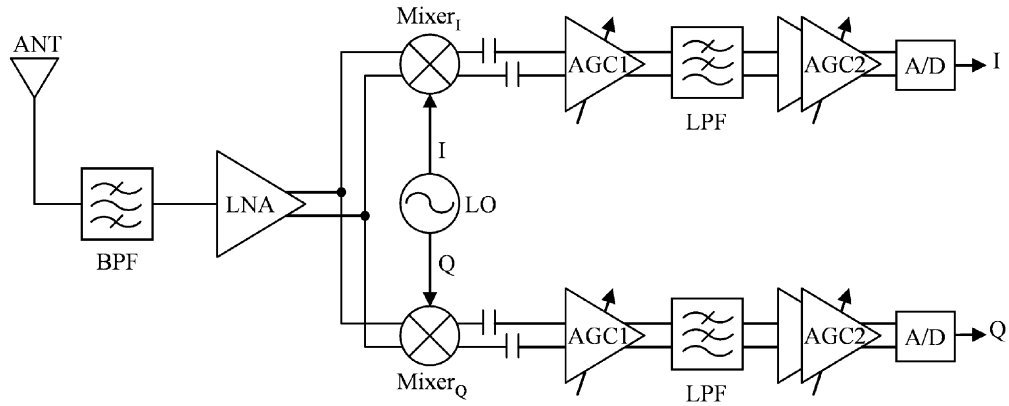

Fig. 2. Architecture for the 5-GHz WLAN receiver.

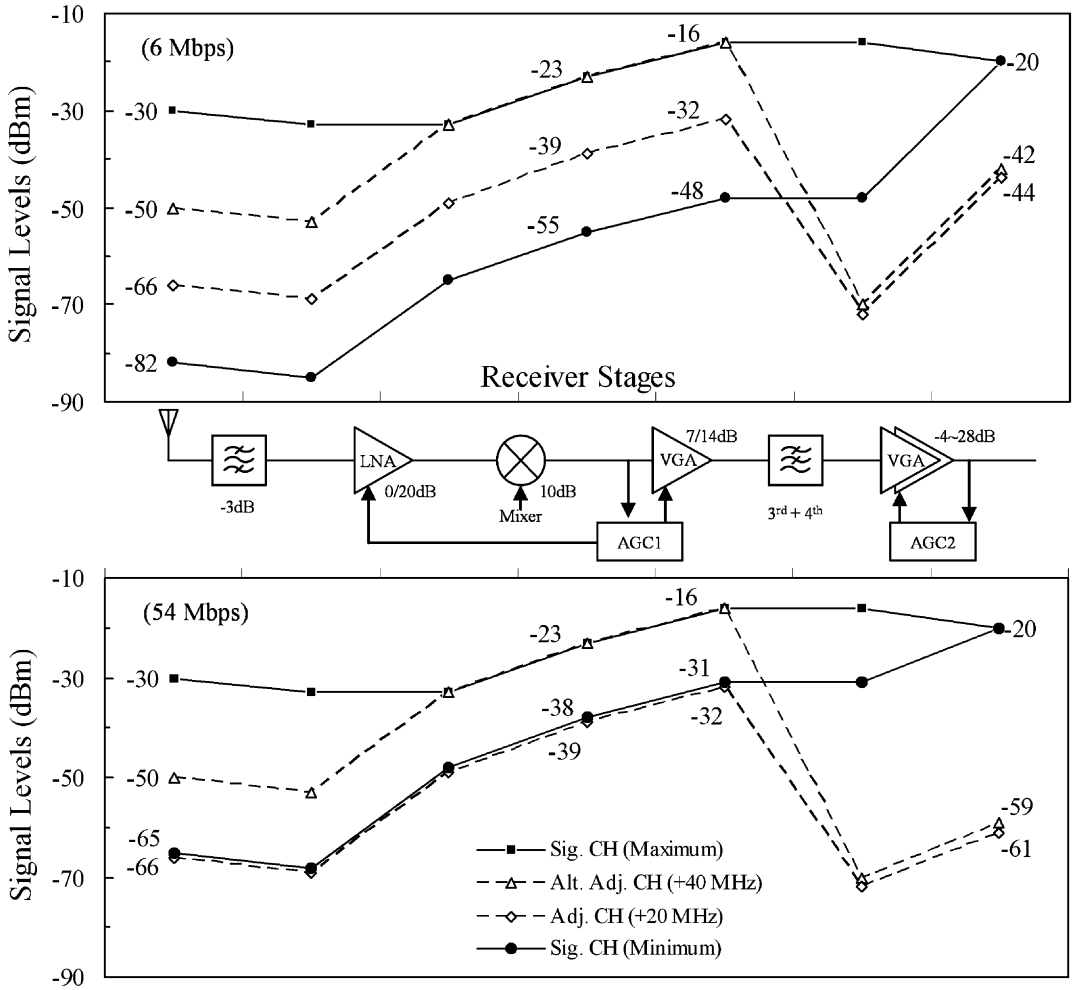

Fig. 3. Receiver gain distribution plots for 6 and 54 Mb/s data rates.

algorithm. Implementation of the AGC circuit and verification through simulations and measurements are described in Sections IV and V.

II. Analog Baseband Signal Chain

Direct conversion is usually preferred over superheterodyne architectures for fully integrated WLAN receivers because its simplicity outweighs drawbacks such as 1/f noise and DC-offset sensitivity [4]. The baseband processor described here is part of a direct-conversion receiver. As depicted in Fig. 2, the receiver consists of a bandpass filter, low-noise amplifier (LNA), plus mixers, low-pass filters, AGC amplifiers, and analog-to-digital (A/D) converters for the I and Q channels. The RF portions of the receiver have the following gains: -3 dB for the (off-chip) bandpass filter, 0 or $+20$ dB (selectable) for the LNA and $+10$ dB for the mixers. The AGC amplifiers supply the rest

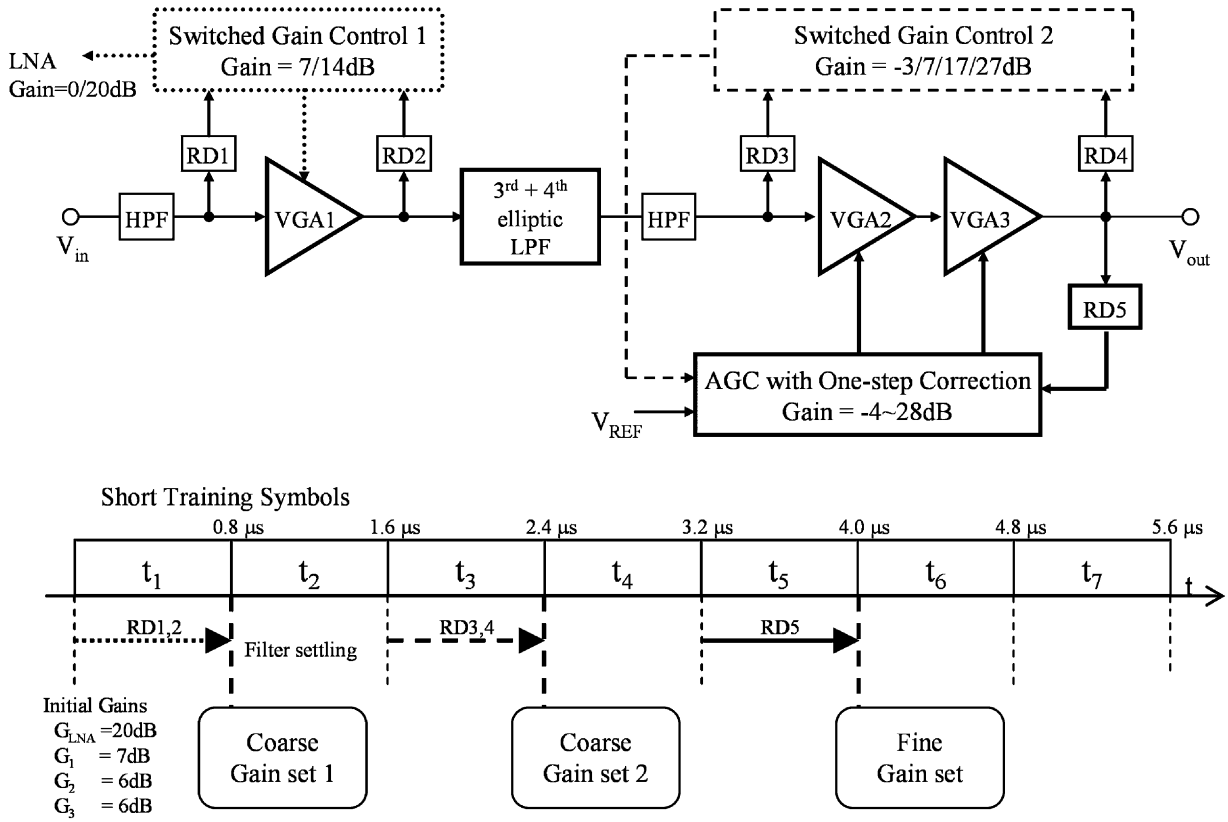

Fig. 4. Architecture of the proposed AGC algorithm.

of the gain and the low-pass filters provide channel-selection to meet the receiver specifications.

The 802.11a standard lists the receiver selectivity and sensitivity specifications for various data rates, which are selected automatically depending on channel conditions. The sensitivity (minimum receivable in-band signal strength), maximum in-band signal strength, and the A/D converters' input signal range determine the required range of gain. The minimum rejection requirements for worst-case adjacent-channel and alternate-adjacent channel (two channels from the desired channel) signals set the filter selectivity requirements.

Because the signal is split into I and Q channels, the channel-select filter cutoff frequency is half the bandwidth. The signal occupies 16.6 MHz within the allocated 20 MHz channel and there is 3.4 MHz spacing between channels. Thus, the pass-band edge frequency is 8.3 MHz. The minimum stop-band attenuations for the adjacent and alternate adjacent channels are 34 dB @ 20 MHz and 49 dB @ 40 MHz, respectively. Some of the channel-select filtering could have been provided using digital filtering in the DSP. However, this places more stringent requirements on the dynamic range of the analog signal processing chain and the analog-to-digital converter. As discussed previously, the mostly analog approach also allows the DSP to sleep more of the time. The filter was designed as a cascade of a third-order and a fourth-order elliptic transconductance-C filter. This design provided faster settling (lower group-delay variation) than a seventh-order elliptic filter with similar selectivity. The filter achieves 40 dB attenuation at 20 MHz and 54 dB at 40 MHz. It settles to within 1 dB in 0.6 μs.

Gain is provided by three VGA stages. The signals before and after the channel-select filter are very different; the pre-filter signal potentially includes large out-of-band signal energy. Using separate AGC loops, one before the filter, allows the gain for each signal to be optimized separately, offering much better worst-case dynamic range. The pre-filter AGC loop selects the gain of the LNA to 0 or 20 dB and selects the gain of the first VGA to $+7$ or $+14$ dB so that the composite (desired channel plus adjacent channels) signal is near the input saturation point of the filter. The post-filter AGC sets the gain of two VGA stages so that the in-channel signal has the desired output amplitude. Using two AGC loops provides higher overall dynamic range with lower AGC gain range than a single pre- or post-filter loop would. The gain for the two post-filter VGA stages is continuously variable from -4 dB to $+16$ dB per stage (-8 dB to $+32$ dB for the cascaded pair of stages). This includes 4 dB margins at each end of the range to ensure adequate gain adjustment range.

Fig. 3 shows how signal levels vary throughout the receiver chain for maximum and minimum in-channel signals and worst-case adjacent and alternate-adjacent signals, for the slowest and fastest data rates.

III. AGC Algorithm

As illustrated in Fig. 4, the AGC operates in three phases: two switched coarse gain-setting phases, followed by an open-loop fine gain-setting phase. The coarse gain-setting steps ensure that all of the gain and filter stages operate linearly, with the gain set within ± 5 dB of its optimal value. The fine step sets the final

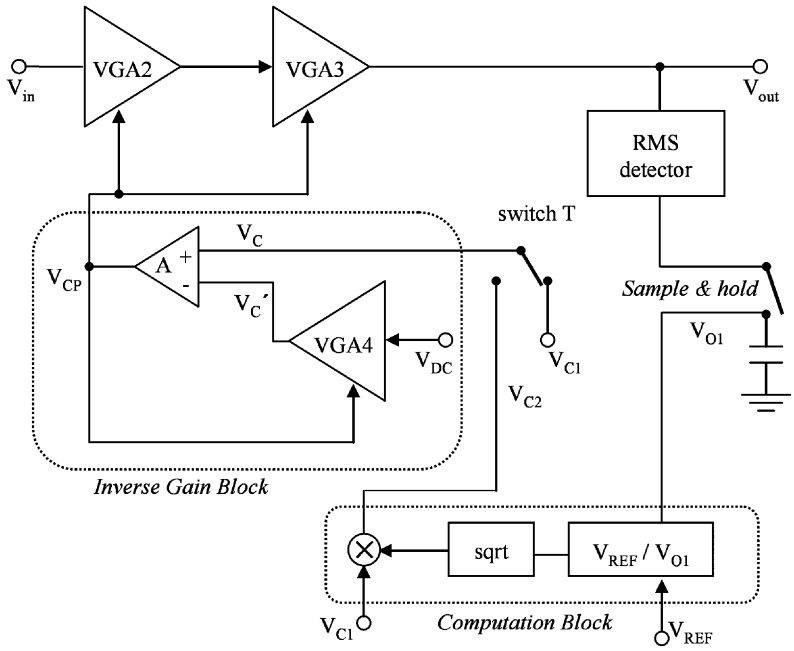

Fig. 5. AGC with one-step correction: the fine gain-setting phase.

gain to within ± 1 dB of its optimal value. Before the reception of each packet, gains are initialized to 20 dB for the LNA, 7 dB for VGA1 and 6 dB each for VGA2 and VGA3. During the first short training symbol time (t_1: 0 to 0.8 μs), RMS detectors RD1 and RD2, located before and after VGA1, estimate the signal amplitude. These values are sampled and held, and are used by the logic block "Switched Gain Control 1" to select the gains of the LNA and VGA1. The LNA gain is set to 0 dB if the output of RD1 is greater than -23 dBm (corresponding to 71 mV in 1 kΩ); if the output of RD2 is less than -23 dBm, the gain of VGA1 is set to 14 dB; otherwise, the LNA and VGA1 keep their initial gains. After the filter output settles during the second short training symbol time, the post-filter AGC "Switched Gain Control 2" selects the combined gain of the second and third VGAs to -3, 7, 17, or 27 dB, based on the amplitude found during time t_3 (1.6 to 2.4 μs) using RMS detectors RD3 and RD4, located before and after the cascade of VGAs. The combined gain of VGAs 2 and 3 is set to -3 dB if the output of RD3 is greater than -30 dBm or to 7 /17 dB if the output of RD4 is greater than $-20/-30$ dBm; if the output of RD4 is less than -30 dBm, the overall gain of VGAs 2 and 3 is set to 27 dB.

How are the required gain-control voltages determined? It is difficult to design a VGA with a predictable gain versus gain-control-voltage relationship, especially in short-channel CMOS technologies. As shown in Fig. 5, an inverse-gain block is used to set the required gain accurately using feedback [2]. Based on the comparisons during time t_3, one of four values is selected for V_{C1}. During t_4, switch T connects the selected V_{C1} to op-amp A's V_C input. The feedback automatically determines the gain-control voltage V_{CP} required to set the gain of VGA4 to $A_{v1} = V_{C1}/V_{\rm DC}$, where $V_{\rm DC}$ is an arbitrary small voltage. VGA2 and VGA3 are matched to VGA4, so their gains are also set to A_{v1}. Note that V_{C1}, $V_{\rm DC}$, and the derivative of the VGA gain with respect to V_{CP} must all have the same sign to allow loop stability.

The fine gain-setting phase "AGC with One-Step Correction" determines the final gains of VGAs 2 and 3. With the gain set as just described, RMS detector RD5 detects the output signal strength using the fifth short training symbol (t_5: 3.2 to 4.0 μs). RD5's output V_{O1} is sampled and held, and the result, $V_{O1} = A_{v1}^2 \cdot V_{\rm in}$, is used in computing the final gain-control signal for VGA2 and VGA3. The gain needed for VGAs 2 and 3 to set the output amplitude to the desired level $V_{\rm REF}$ is

$$A_{v2} = A_{v1} \cdot \sqrt{\left(\frac{V_{\rm REF}}{V_{O1}}\right)}. \tag{1}$$

The computation block computes the new value V_{C2} for the V_C input to the inverse-gain block needed to satisfy that relationship. The required value is

$$V_{C2} = V_{C1} \cdot \sqrt{\left(\frac{V_{\rm REF}}{V_{O1}}\right)}. \tag{2}$$

The computed V_{C2} value is sampled and held, and is applied through switch T to set the final gain to the required value. The overall AGC loop is never closed, avoiding the settling-time limits of a conventional closed-loop AGC. The computed final gain is held constant throughout the transmission of the packet. Note that both I and Q channels should share a single AGC loop for gain control.

IV. Circuit Implementation

The portion of the AGC circuits following the channel-selection filter in Fig. 4, including two VGAs, switched gain-control block 2 and the fine AGC with one-step correction, was designed based on the TSMC 0.18-μm CMOS process. Except for some parts of the analog computation block, all of the circuits were designed with fully differential circuitry.

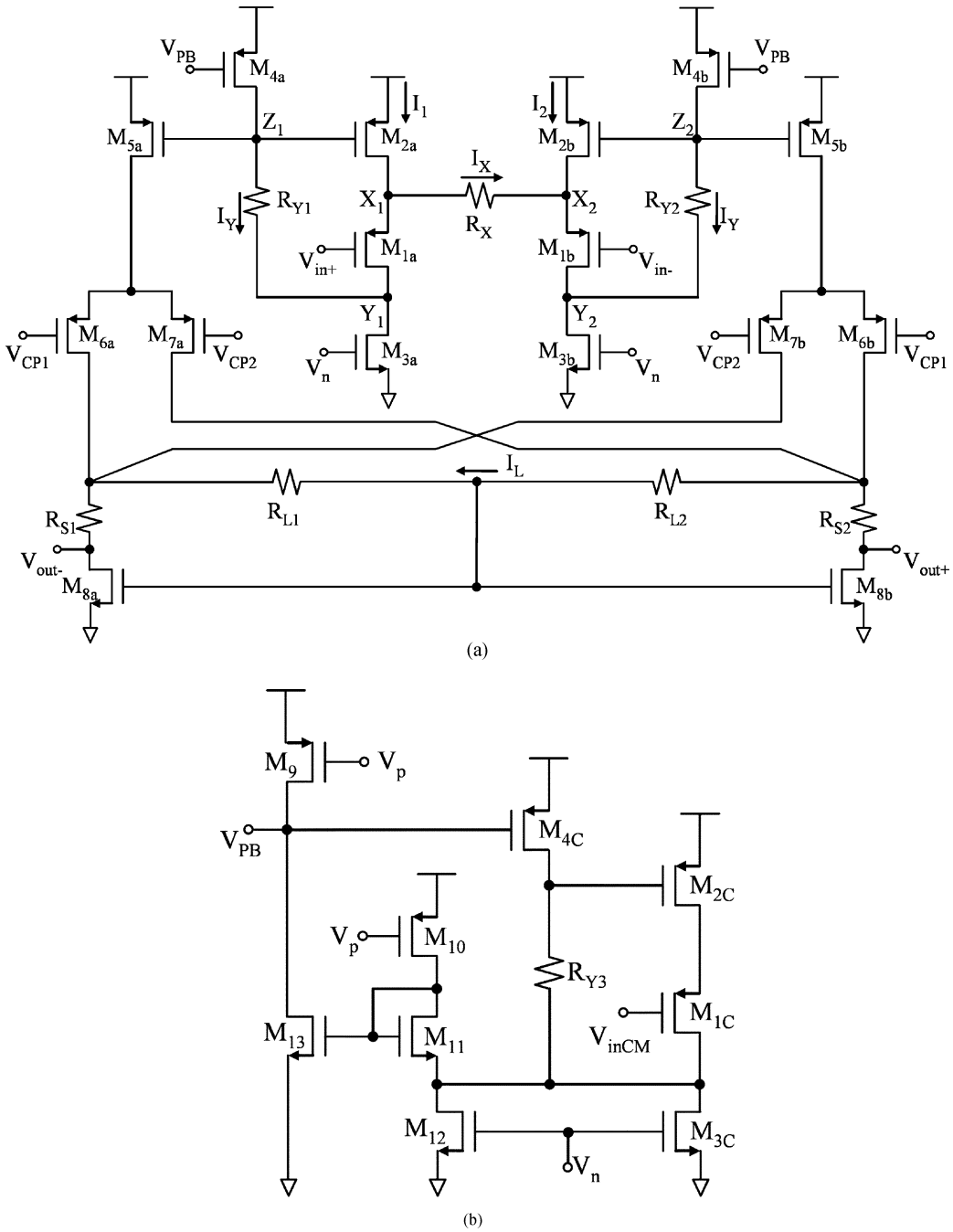

Fig. 6. Schematic of (a) the proposed VGA and (b) the replica bias circuit.

A. Variable Gain Amplifier

The VGA must provide controllable gain, while maintaining good linearity. However, because the inverse-gain block is used, the relationship of the gain-control voltage to the gain does not need to follow any special form. To ensure linearity, the VGA uses a differential input circuit with transconductance Gm set by a fixed resistor. Cross-coupled differential pairs control the gain by steering a variable fraction of the signal to the differential fixed-resistor load.

The VGA schematic is shown in Fig. 6(a). Differential input $V_{\rm in} = V_{\rm in+} - V_{\rm in-}$ is applied between the gates of source-followers M_{1a} and M_{1b}, which are connected in feedback loops with M_{2a} and M_{2b} to form a pair of so-called flipped voltage followers (FVFs) [5]. The FVFs force constant current in M_{1a} and M_{1b} so that nodes X_1 and X_2 follow $V_{\rm in+}$ and $V_{\rm in-}$ with constant V_{GS} offset. Thus, the current I_X through fixed resistor R_X is accurately proportional to $V_{\rm in}$. The difference of currents I_1 and I_2 is

$$I_1 - I_2 = 2 \cdot I_x = 2 \cdot G_m \cdot V_{\rm in} \tag{3}$$

where $G_m = 2/R_X$. I_1 and I_2 are passed to the transconductor output using current mirrors M_2/M_5.

The voltages V_{CP1} and V_{CP2} on the gates of the M_6/M_7 differential pairs control how much of the transconductor current passes to the load. V_{CP1} and V_{CP2} are the outputs of a differential difference amplifier (DDA), which uses common-mode feed-

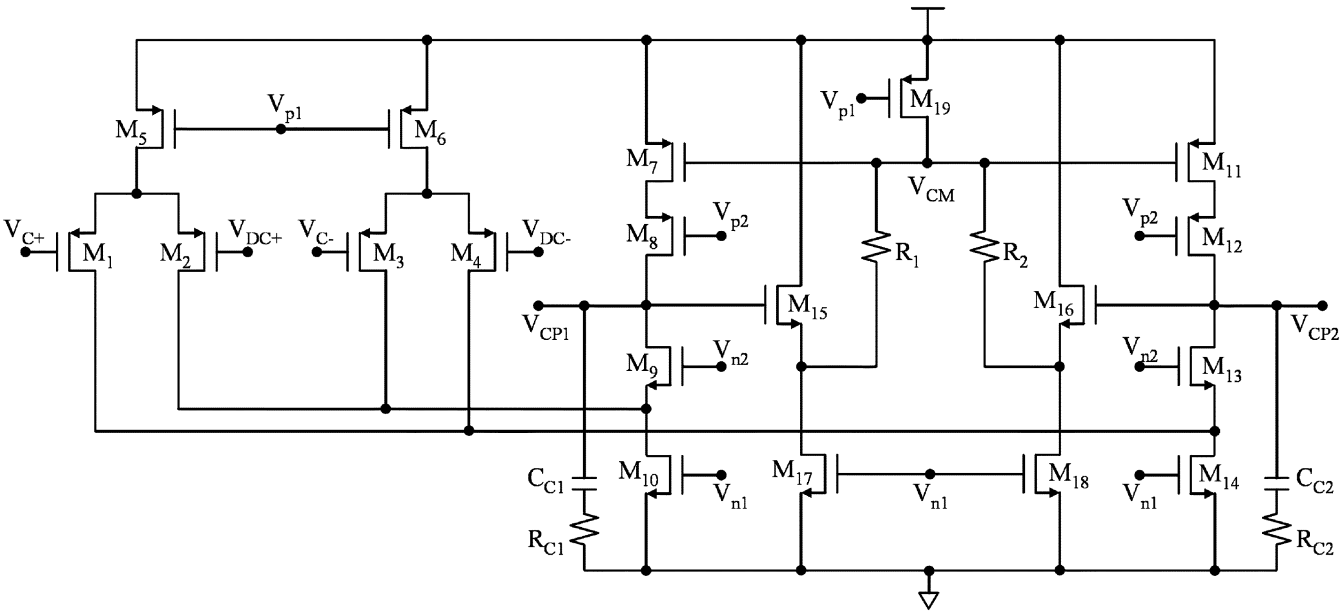

Fig. 7. Schematic of the differential difference amplifier.

back (CMFB) to set the average of V_{CP1} and V_{CP2} to about 0.6 V below the positive supply voltage, V_{DD}. The DDA circuit will be described in more detail later. System operation ensures that $V_{CP1} > V_{CP2}$. For large $V_{CP1} - V_{CP2}$, most of the signal current is passed to the differential load current I_L, and the gain approaches its maximum value, $2 \cdot R_L/R_X$, where $R_L = R_{L1} = R_{L2}$. For small $V_{CP1} - V_{CP2}$, the gain is nearly zero. In all cases, the common-mode (CM) current is constant at about $I_{CM} = (I_1 + I_2)/2$. The cascaded VGA stages are direct-coupled, so the output CM voltage must match the VGAs' input CM range. The load circuit uses level-shift resistors R_{S1} and R_{S2} to lower the CM output voltage to $V_{GS8} - I_{CM} \cdot R_S$, typically about 0.5 V. The VGA circuit consumes total current of 1.5 mA.

Voltages in the VGA are highly constrained. If the input CM voltage is too low, M_1 will go triode on signal peaks, and if it is too high, M_2 will go triode. To maximize the input range, resistors R_{Y1} and R_{Y2} are placed in the feedback paths of the FVFs to shift the drain voltages of M_1 and M_3 closer to the negative supply rail by $I_Y \cdot R_Y$. The situation is complicated further because for constant I_Y, nodes X, Y and Z are all referred to V_{DD}, which may vary $\pm 10\%$ ($1.6\ \text{V} < V_{DD} < 2.0\ \text{V}$). To address this, current sources M_{4a} and M_{4b} are controlled by a voltage V_{PB} that is generated by a replica bias circuit [Fig. 6(b)]. The replica circuit adjusts V_{PB} so that the drain voltages of M_{1a} and M_{1b} in Fig. 6(a) equal the source voltage of M_{11}, which is referenced to ground rather than to V_{DD}. $I_Y \cdot R_{Y1}$ and $I_Y \cdot R_{Y2}$ vary with V_{DD}, so that node voltages Z_1 and Z_2 vary with V_{DD} while the voltages at nodes Y_1 and Y_2 are almost fixed, typically about 0.65 V. The replica circuit has three feedback loops: two negative loops (M_4–M_2–M_1–M_{11}–M_{13} and M_2–M_1–R_Y) and a positive feedback loop (M_4–R_Y–M_{11}–M_{13}). The presence of the positive feedback loop raises concerns that multiple operating points may be possible [6], but detailed simulations showed that no undesired operating points exist.

The VGA structure shows good linearity with a large gain range. However, tradeoffs were needed among gain range, linearity, noise, bandwidth and current consumption. M_1, M_6, and M_7 use near-minimum channels to enhance frequency response and linearity. The short channels increase flicker noise, so pMOS devices were chosen for these devices. Relatively long transistors with relatively high $V_{GS} - V_T$ were used for current sources M_2, M_3, M_4, M_5, and M_8. This enhances matching, output resistance and flicker noise. Channel widths were chosen to optimize tradeoffs among noise and current consumption while meeting frequency response specifications.

B. DDA

The inverse-gain block used fully differential circuits throughout. Op-amp A in Fig. 5 was implemented using a differential difference amplifier (DDA), as shown in Fig. 7. The DDA is the differential generalization of a single-ended op amp, with a pair of differential inputs, and differential output with CMFB [7]. The CMFB circuit uses source followers M_{15} and M_{16} and equal resistors R_1 and R_2 to average the outputs. R_1 and R_2 also serve as level-shifters, producing a CM voltage referenced to V_{DD}, as required for the V_{CP} control inputs of the VGA. The inverse-gain and CMFB loops are compensated using two grounded capacitors ($C_{C1} = C_{C2} = 10$ pF) and series-connected resistors ($R_{C1} = R_{C2} = 200\ \Omega$). The DDA consumes total current of 350 μA.

C. RMS Detector

The RMS detector estimates the amplitude of the output signal, integrated over the duration of one short training symbol. (The circuit should perhaps be called a "pseudo-RMS" detector, because it does not implement the RMS function very accurately. Simulations showed that accurate RMS detection was not needed.) The dynamic range of the circuit is rather narrow, which is acceptable because the coarse gain-setting step ensures the signals are not far from their optimal value. As shown in Fig. 8, the detector output voltage ($V_{\text{out}+} - V_{\text{out}-}$) is stored as the difference of the V_{GS}'s of a pair of diode-connected

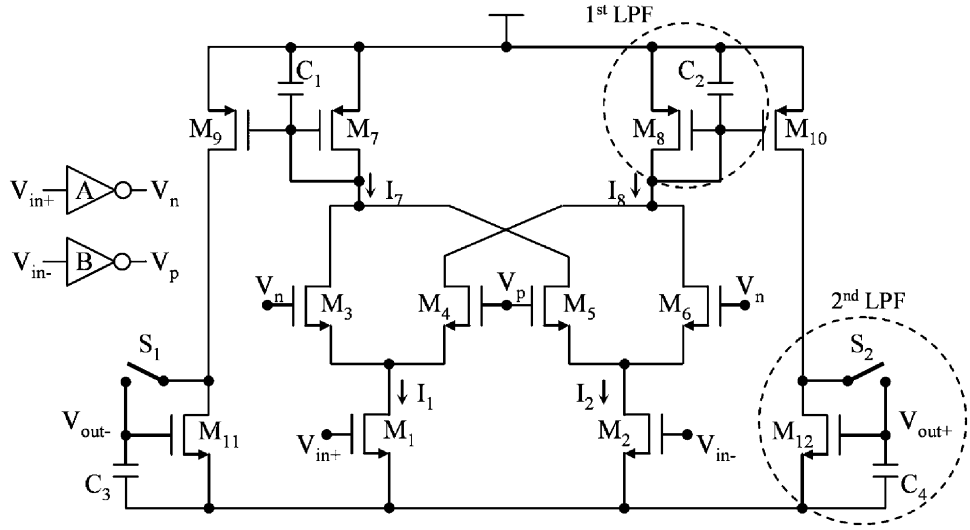

Fig. 8. Schematic of the RMS detector.

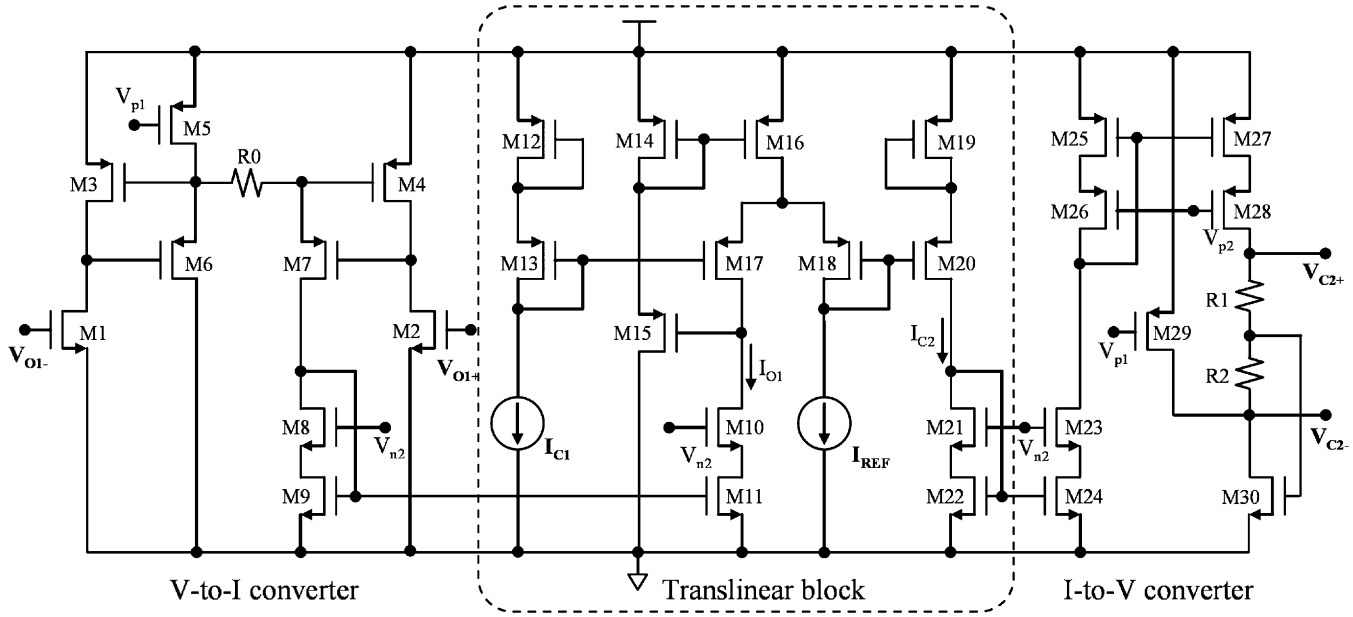

Fig. 9. Analog computation circuits.

nMOS transistors (M_{11} and M_{12}). This signal is sampled and held on storage capacitors connected to the gates of nMOS transistors. differential outputs $V_{\text{in}+}$ and $V_{\text{in}-}$ from a VGA are fed to the gates of long-channel (2 μm) nMOS FETs M_1 and M_2, which are operated in strong inversion to provide a squaring function [8]. Cross-coupled nMOS differential pairs M_3–M_6 full-wave rectify the currents of M_1 and M_2. The differential pairs must work as switches, so their gate voltages are driven by the input signals $V_{\text{in}+}$ and $V_{\text{in}-}$, boosted by amplifiers A and B. The full-wave rectified currents I_7 and I_8 are averaged and square-rooted to complete the amplitude detection. A cascade of two first-order low-pass filters does the averaging. The on-chip capacitors are $C_1 = C_2 = 4$ pF and $C_3 = C_4 = 10$ pF. After the 0.8 μs averaging time, small-geometry nMOS switches S_1 and S_2 open, and C_3 and C_4 hold the stored voltage, which is represented differentially. The amplitude signal is strictly positive, with $V_{\text{out}+} > V_{\text{out}-}$. The RMS detector consumes total current of 40 μA.

D. Computation Block

The computation circuit computes the final gain-control voltage V_{C2}, based on the previous gain-control voltage V_{C1}, the previous RMS output V_{O1} and the desired output V_{REF}, according to (2). The computation uses single-ended translinear circuits, which require FET operation in subthreshold. Thus, we need to linearly convert differential voltages V_{C1}, V_{O1}, and V_{REF} to small (< 1 μA) single-ended currents. The V-to-I converter for V_{O1} is shown in Fig. 9. M_3–M_6 and M_4–M_7 form shunt feedback loops that provide a low-impedance copy of $V_{\text{out}+} - V_{\text{out}-}$ (from the RMS detector, Fig. 8) across 30 kΩ resistor R_0. Current from M_5 ensures that M_6 is on for all input voltages. The current in R_0 passes through M_7 and is mirrored

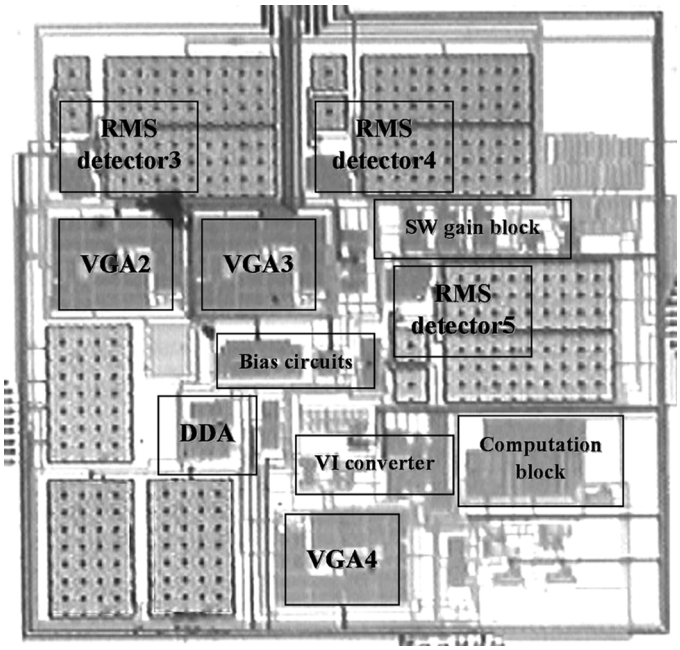

Fig. 10. Die photo of the analog AGC circuitry.

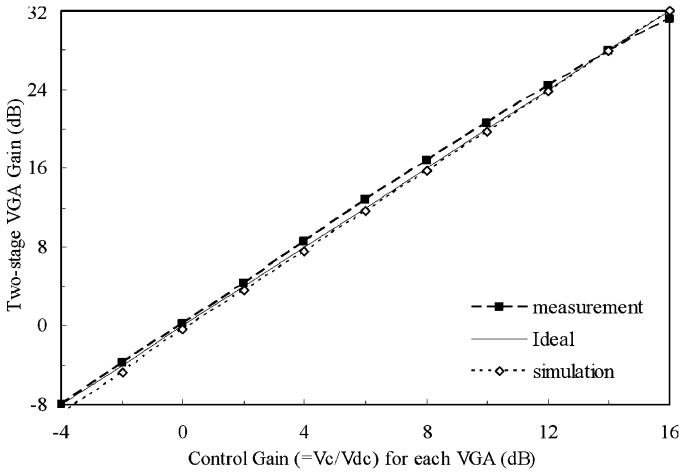

Fig. 11. Gain control curve for the two-stage VGA. Ideally, the inverse-gain circuit sets the gain of each VGA stage to VC/VDC.

by M_8–M_{11}, a 4:1 attenuating current mirror, to produce a small linear current I_{O1} proportional to V_{O1}. Similar circuits are used to produce I_{C1} and $I_{\rm REF}$.

The analog computation is performed using transistors M_{12}–M_{20}. Applying the translinear principle [9] for FETs in weak inversion yields

$$-V_{GS\_C1}-V_{GS_C1}+V_{GS_O1}-V_{GS\_REF}+V_{GS_C2}+V_{GS_C2}=0 \quad (4)$$

$$-lnI_{C1}-lnI_{C1}+lnI_{O1}-lnI_{\rm REF}+lnI_{C2}+lnI_{C2}=0 \quad (5)$$

$$lnI_{C2}^2-lnI_{C1}^2=lnI_{\rm REF}-lnI_{O1} \quad (6)$$

$$ln\left(\frac{I_{C2}}{I_{C1}}\right)^2=ln\left(\frac{I_{\rm REF}}{I_{O1}}\right) \quad (7)$$

$$I_{C2}=I_{C1}\cdot\sqrt{\left(\frac{I_{\rm REF}}{I_{O1}}\right)}. \quad (8)$$

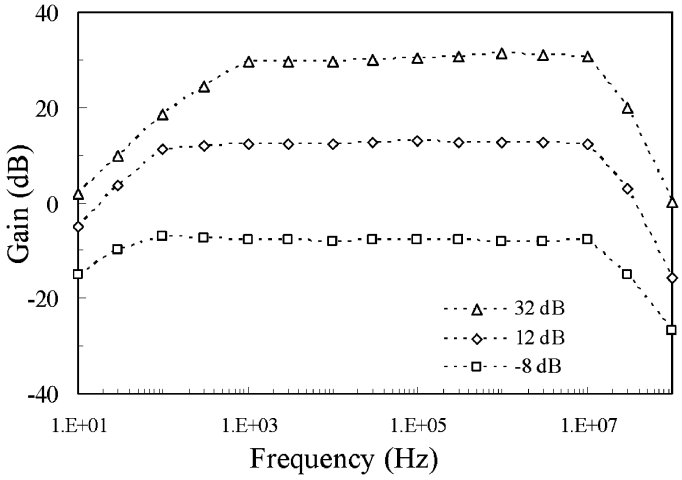

Fig. 12. Frequency response of the two-stage VGA.

The core transistors have large W/L to ensure weak inversion operation with currents up to 1 μA. M_{13}, M_{17}, M_{18} and M_{20} have separate n-wells to avoid errors due to bulk effect.

The computed current I_{C2} is stepped up by 4:1 amplifying current mirrors M_{25}–M_{28}. The amplified output current flows in equal-valued resistors R_1 and R_2 to produce the differential output voltage V_{C2} between the top of R_1 and the bottom of R_2. The V_{GS} of M_{30} sets the common-mode voltage, with M_{29} supplying common-mode current. The computation block consumes total current of 30 μA.

E. Gain-Select Resistor Array and Other Circuits

The four selectable gains used in "Switched Gain Control Block 2", plus the reference voltages $V_{\rm REF}$, $V_{\rm DC}$, and other key voltages are provided by an on-chip reference voltage generator so that all gains are ultimately set by resistor ratios. The resistors in the array use parallel and series combinations of unit resistors to enhance matching [10].

Several other circuits were designed but are not described here for space reasons. These include the *Gm-C* filter, comparators and digital control circuits for switched-gain control, and on-chip bias-generation circuitry.

V. Simulation and Measurement Results

The post-filter AGC circuits described in Section IV were fabricated in the TSMC 0.18-μm single-poly six-metal CMOS process available through MOSIS. The die photo is shown in Fig. 10. The fabricated parts were packaged in a 40-pin ceramic DIP package.

The two-stage VGA was measured using sine-wave input signals from an Agilent 33120A. Output signals were measured using an Agilent 54622D oscilloscope. Measurements of the gain-control function in Fig. 11 match simulation results closely. Measured frequency responses of the two-stage VGA with gains of -8, $+12$, and $+32$ dB gain are shown in Fig. 12. The results verify the circuit can pass the required bandwidth of 156.25 kHz to 8.3 MHz. The low-frequency response is controlled by the off-chip input coupling capacitor and the on-chip feedback resistor used to establish the operating point. Measurements showed that the VGA met these specifications for $1.6\ {\rm V} < V_{DD} < 2.0\ {\rm V}$.

TABLE I
SIMULATION AND MEASUREMENT RESULTS FOR THE POST-FILTER AGC

	Simulation	Measurement
Process	0.18 μm CMOS 1P6M	0.18 μm CMOS 1P6M
Die size (with 40 pads)	2.85 x 2.85 mm^2	2.85 x 2.85 mm^2
Die size (AGC only)	0.75 x 0.75 mm^2	0.75 x 0.75 mm^2
Power supply	(1.6 to 2.0) V	(1.6 to 2.0) V
I_{total}	5.6 mA	5.8 mA
AGC output voltage	500 mV_{pp_diff}	500 mV_{pp_diff}
2-stage VGA frequency response (±1.5 dB)	1 kHz to 16 MHz	0.8 kHz to 18 MHz
AGC gain range	-8 to 32 dB	-8 to 32 dB
AGC gain accuracy	±1 dB	--
AGC settling time	4.8 μs	--
Input referred noise (@ 0 dB gain)	77.5 nV/√Hz	--
THD (with 1 MHz tone)	1.0 % @ 32 dB gain 1.4 % @ -8 dB gain	--

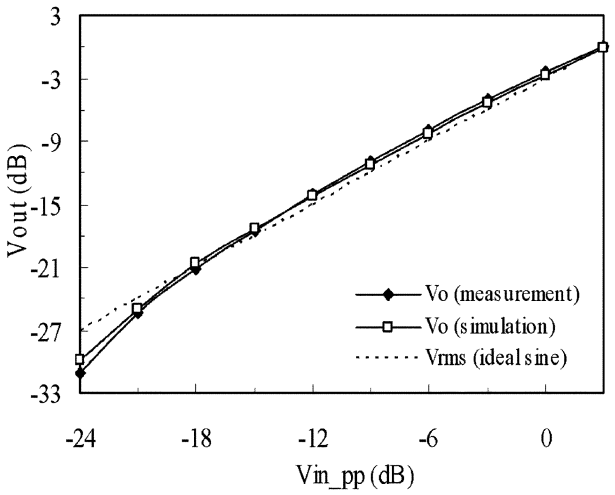

Fig. 13. Input–output linearity of the simple RMS detector.

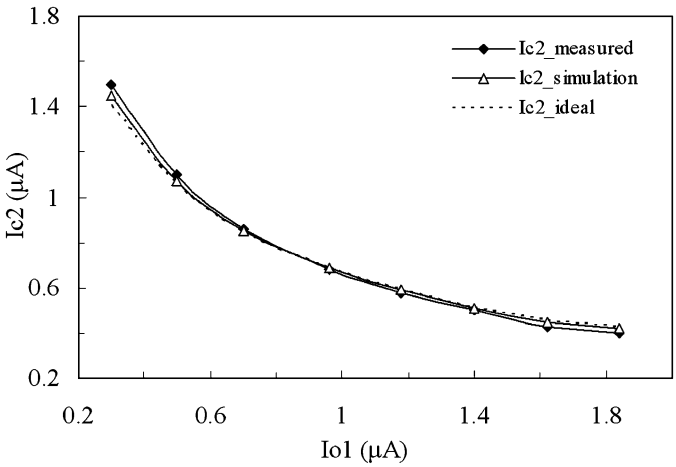

Fig. 14. Input–output characteristics of the current-mode computation block. The ideal response is $I_{C2} = I_{C1} \cdot \sqrt{(I_{\mathrm{REF}}/I_{O1})}$.

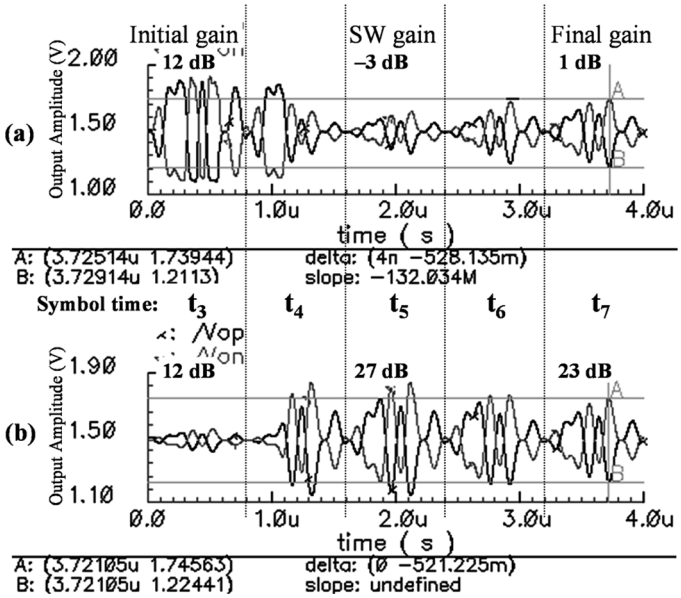

Fig. 15. AGC performance with OFDM signals: (a) low gain (1 dB) adjustment from high input level (gain error: 0.47 dB) and (b) high gain (23 dB) adjustment from low input level (gain error: 0.36 dB).

Fig. 13 is the input–output plot of the RMS detector with sinusoidal input. The measurements agree well with simulations. The modest deviations from ideal behavior are acceptable for meeting system gain-accuracy specifications. Results of simulations using random OFDM signals are not shown, but accuracy is comparable to the sine wave results.

Typical input–output characteristics of the current-mode computation block are shown in Fig. 14. In measurements and simulations, this circuit was found to be accurate to within 0.5 dB over its operating range.

The convergence of the AGC with OFDM signals was simulated using SPECTRE. The results are shown in Fig. 15. The

AGC uses symbol times t_3 through t_7. The gain for the two-stage VGA was initialized to 12 dB. The switched gain is selected during t_4 and the final gain is adjusted during t_6. The post-filter AGC adjusts signals to the desired level with gain error less than 1 dB over the whole gain range. Table I summarizes the simulation and measurement results for the signal chain.

VI. Conclusion

Analog baseband AGC circuitry using a new open-loop analog gain-control algorithm for an OFDM WLAN receiver has been presented. The circuit detects signal strength from repeated OFDM short training symbols and uses an inverse-gain feedback technique with an open-loop computation for rapid yet accurate gain control. Newly designed fully differential linear VGAs, simple RMS detectors, and current-mode computation circuitry are shown to be well-suited for use in OFDM AGC systems. The new AGC circuit needs just seven OFDM short training symbols (5.6 μs) to adjust the gain to the desired level with gain error less than 1 dB.

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