EE290C HW 2

Vighnesh Iyer

September 6, 2018

1 Bitwidth Inference

For the 'Example' circuit, use FIRRTL's conservative bitwidth inference rules to derive the widths of registers `sum` and `prod` and output `out`. Check the results using the FIRRTL compiler.

$$
\begin{aligned}
w_{sum} &= \max(w_a, w_b) + 1 = 5 \\
w_{prod} &= w_{sum} + w_c = 8 \\
w_{out} &= \max(w_{prod}, w_{sum}) + 1 = 9
\end{aligned}
$$

The generated Verilog from running `firrtl -i hw2.fir -o hw2.v` contains these lines which verify the width calculation.

```
module Example( // @[:hw2.fir@2.4]
  input        clk, // @[:hw2.fir@3.8]
  input  [3:0] a, // @[:hw2.fir@4.8]
  input  [1:0] b, // @[:hw2.fir@5.8]
  input  [2:0] c, // @[:hw2.fir@6.8]
  output [8:0] out // @[:hw2.fir@7.8]
);
  reg [4:0] sum; // @[:hw2.fir@9.8]
  reg [7:0] prod; // @[:hw2.fir@10.8]
  ...
endmodule
```

2 Chisel Generator Bootcamp

The IPython notebooks and HTML are attached for bootcamp sections 2.3-2.5 and 3.1-3.2.