



{address: 0x8000_0012, timestamp: 11, data: 0x0126, is_store: True, writer_id: 1}

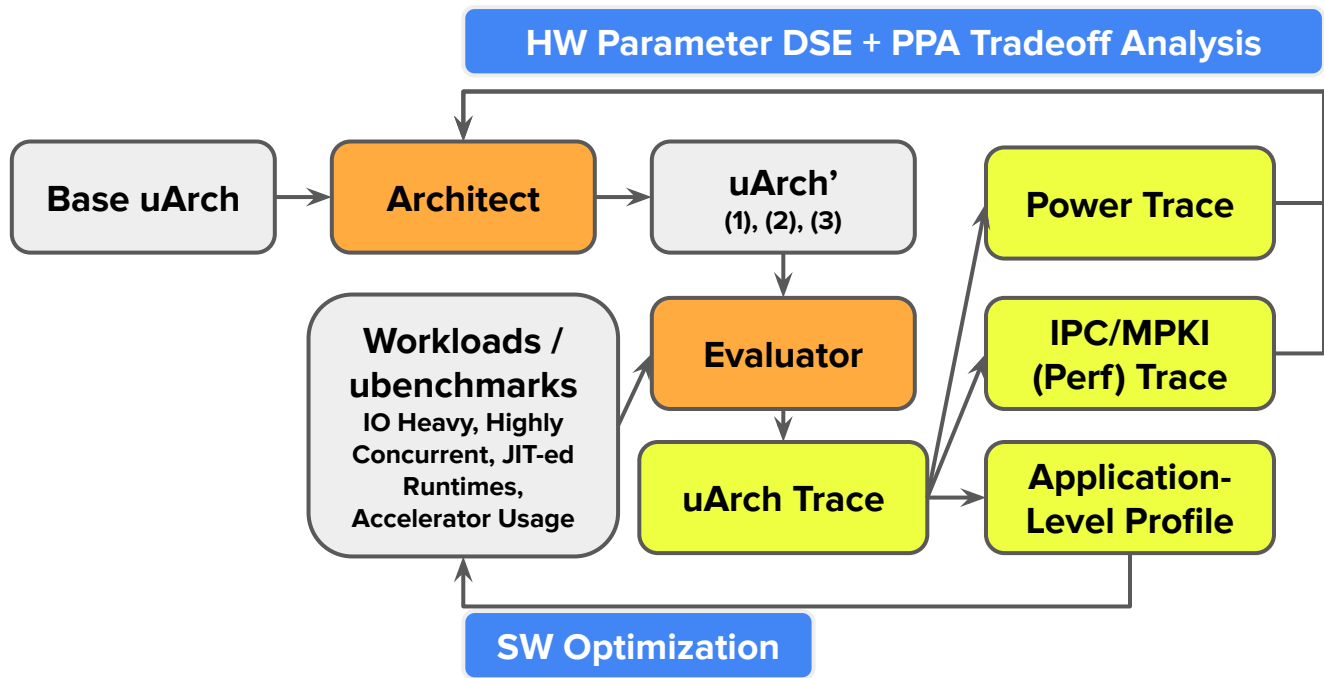
{address: 0x8000_0100, timestamp: 15, data: 0x0235, is_store: False, writer_id: 1}

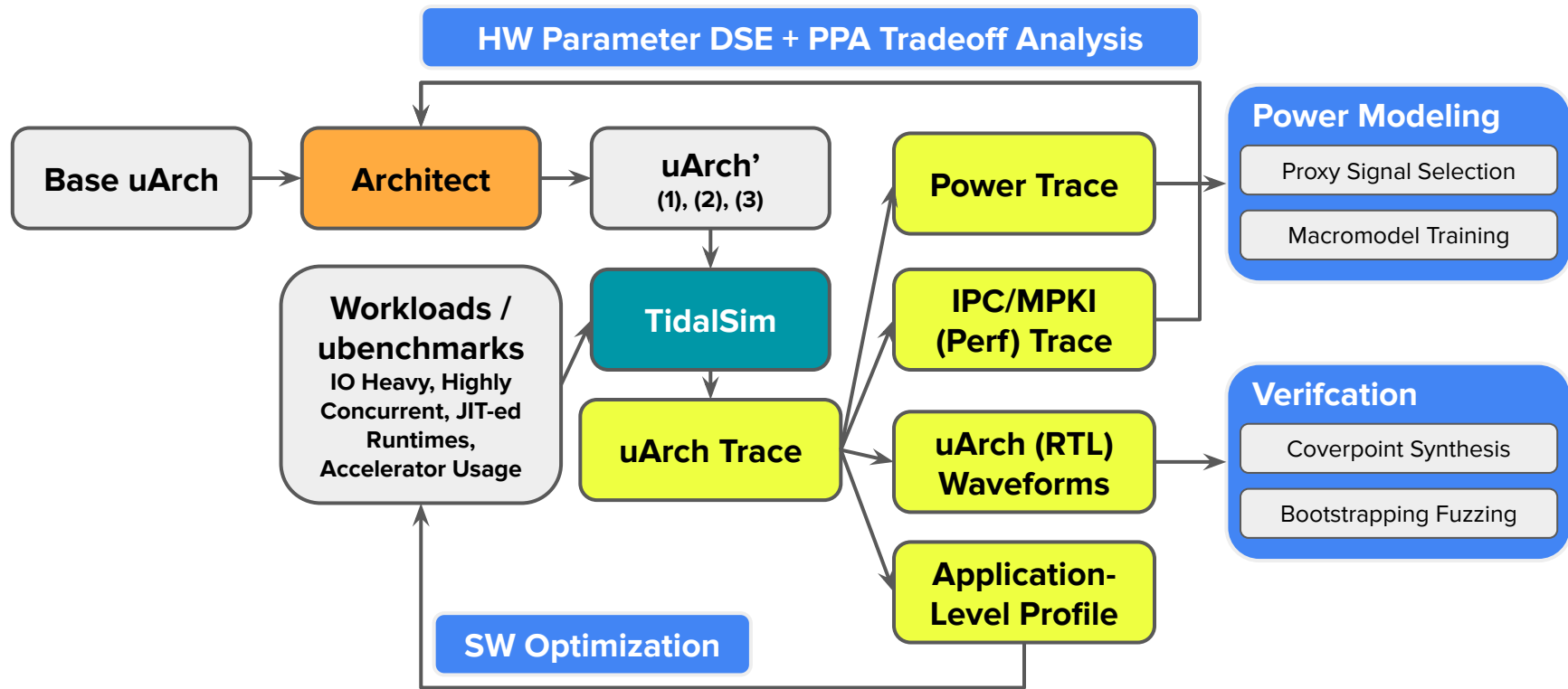


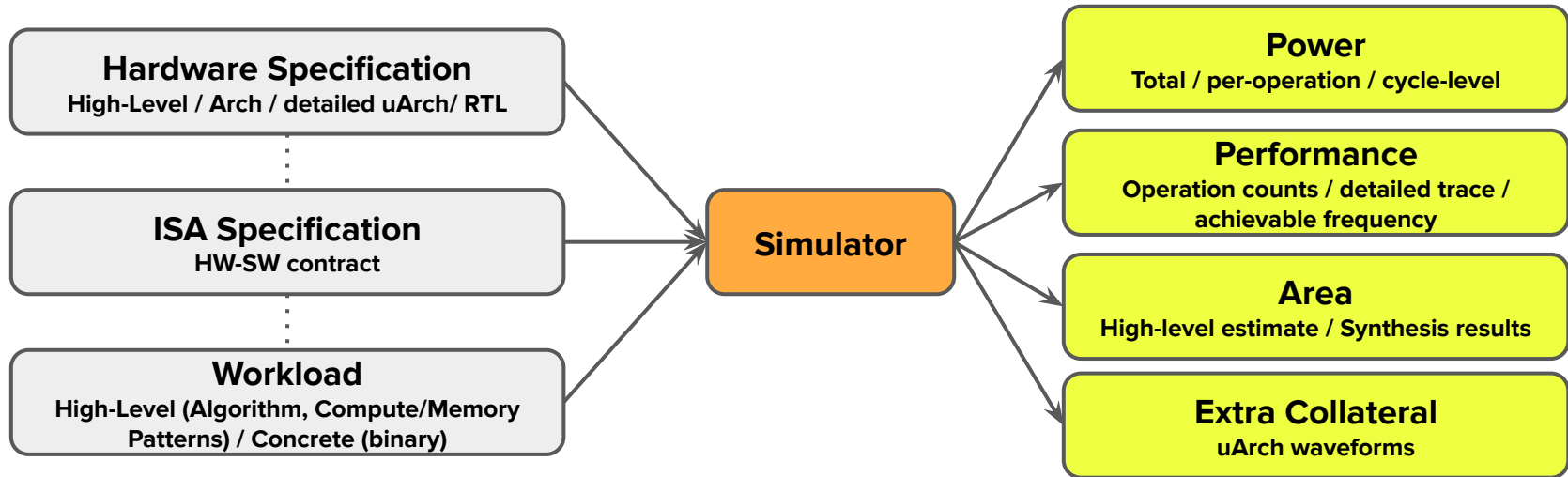
Address	Last Read Timestamp	Last Write Timestamp	Writer ID	Last Updated Value
0x8000_0010	10	5 11	1	0x012600fc
0x8000_0100	15	7	1	0x00000235
0x8000_0020		12	1	0x00000140
⋮				

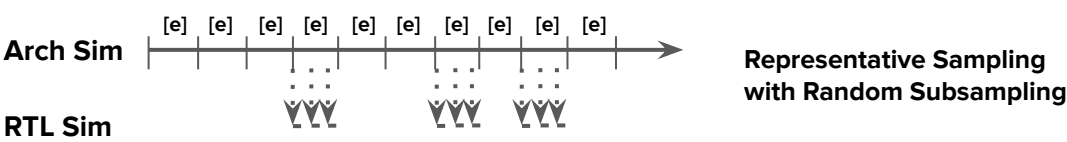
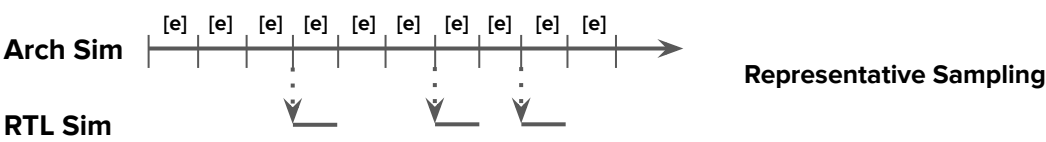
4B cache lines, 2-way set associative, 16 sets, write allocate, LRU eviction

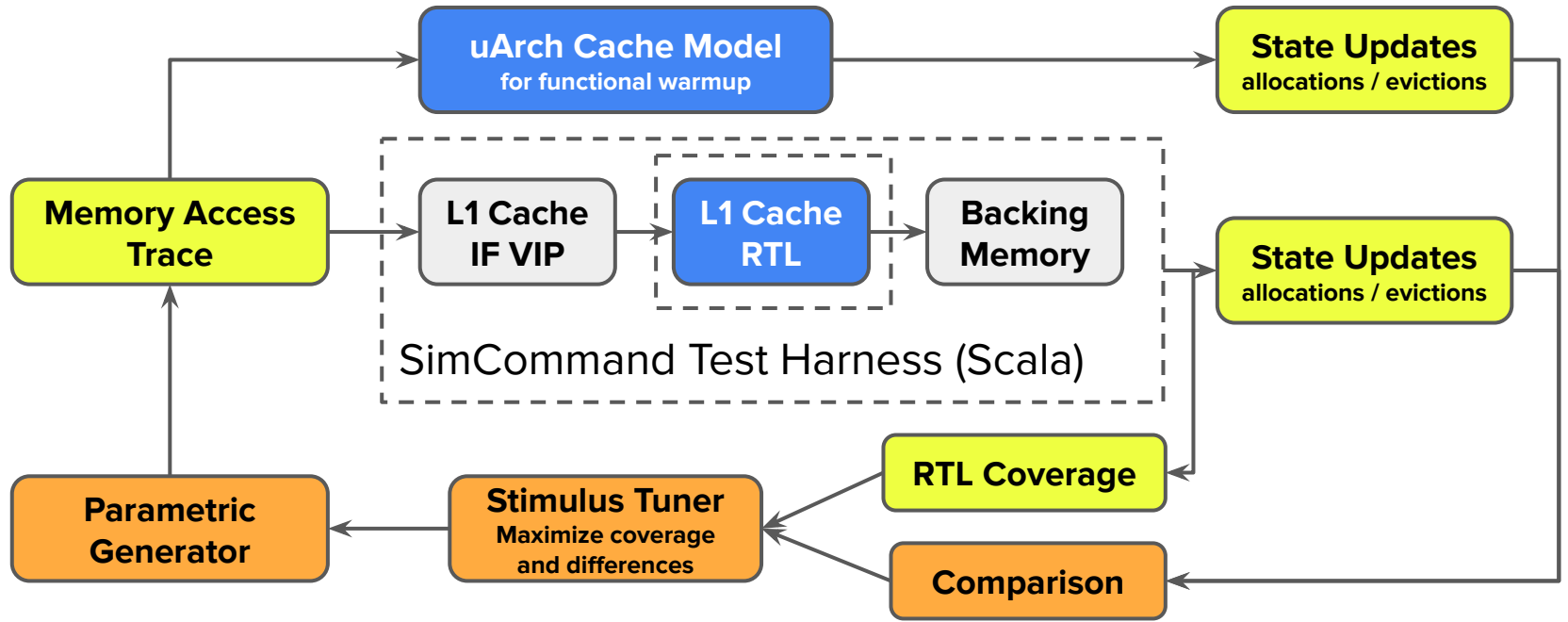
Address	Last Read Timestamp	Last Write Timestamp	Writer ID	Last Updated Value
0x8000_0010	10	11	1	0x012600fc
0x8000_0100	15	7	1	0x00000235
0x8000_0020		12	1	0x00000140
⋮				
0x8000_0014	32	22	1	0x00000098



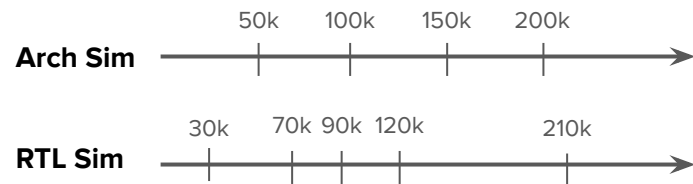




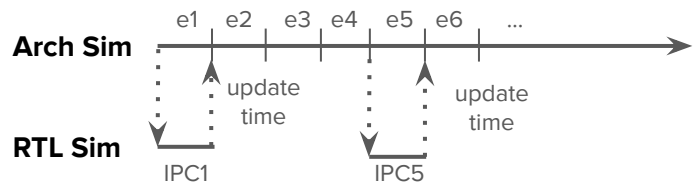




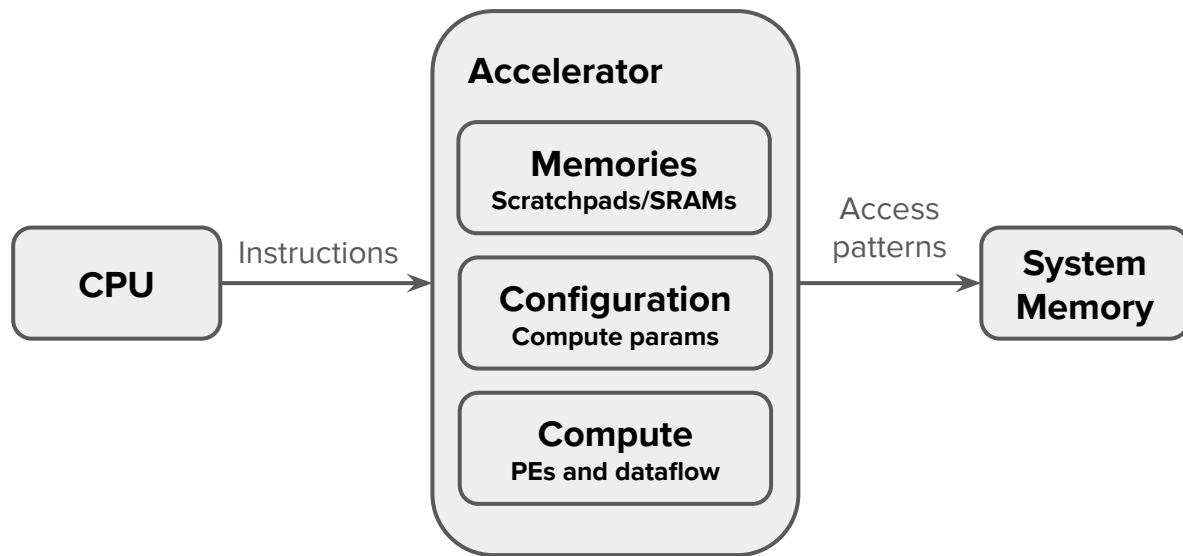
**Timer interrupt points by
dynamic instruction count**



**RTL and Arch sim
increasingly drift out of sync!**



**Use feedback from RTL sim
to arch sim to estimate time
advancement via embedding
similarity**



Architecture Design

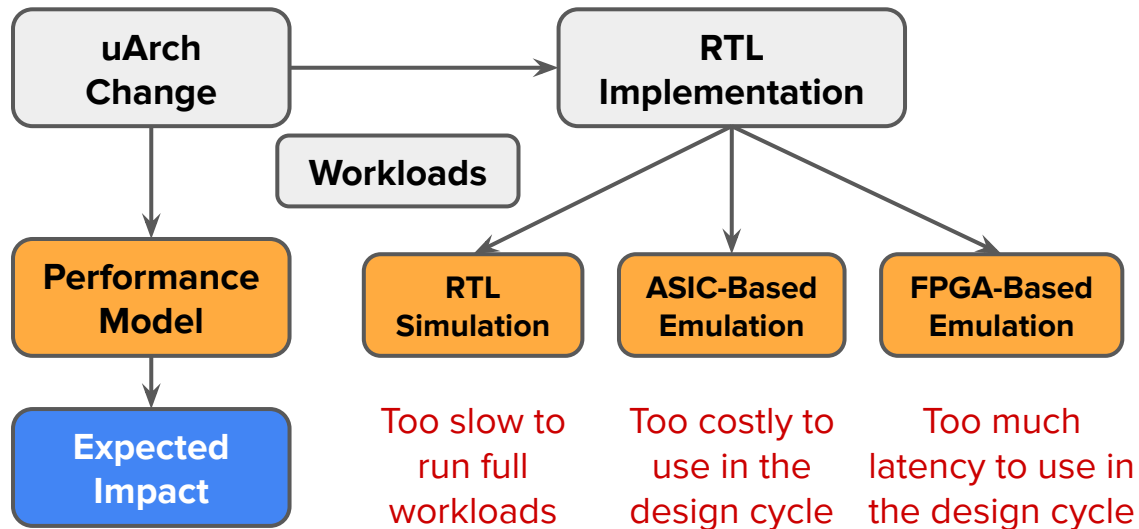
Performance Modeling

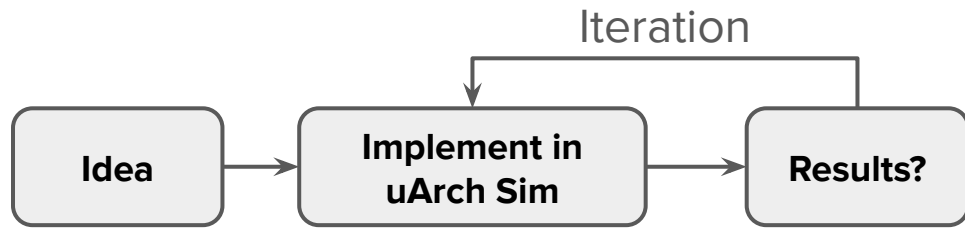
RTL Implementation

Verification

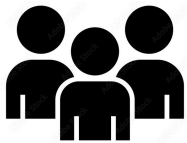
**Need to validate performance
impact of RTL changes**







uArch simulators
are untrustworthy
and have
unbounded
modeling errors



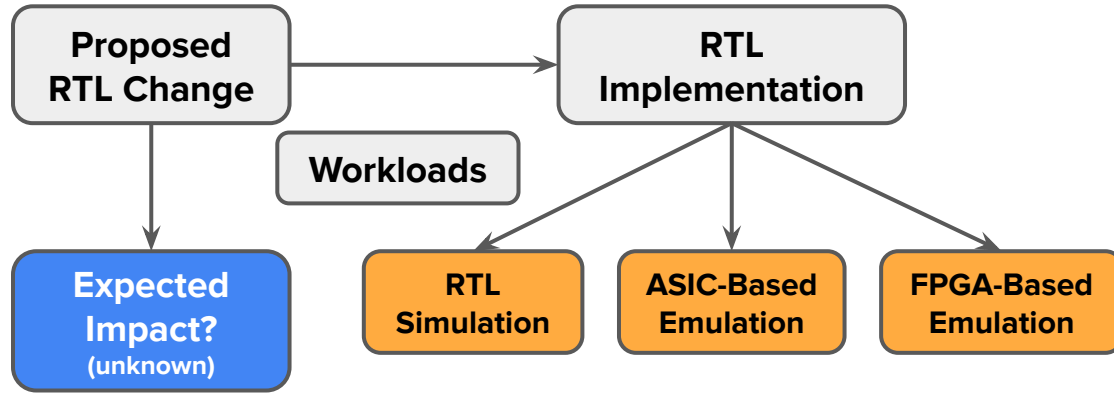
Small teams can't
afford to allocate
people to
performance
modeling

Architecture

Perf Modeling

RTL Design

Verification



Too slow to run
full workloads

Cost-constrained teams may
not have these options