DRILLS: Debugging RTL Intelligently with Localization from Long-Simulation

VIGHNESH IYER and DONGGYU KIM, UC Berkeley

With increasing RTL design complexity it is increasingly difficult to debug why a subset of tests fail in chip-level emulation. Commonly, realistic workloads are run on RTL being emulated on an FPGA and from the use of powerful DSLs (Chisel) and higher levels of abstraction (HLS), the number of subtle bugs present in a design also increases. Many design bugs are difficult to catch with unit testing...

1 INTRODUCTION

Specification mining is a technique to extract LTL properties from a set of traces of signals. This technique can be applied for several purposes in the domain of digital hardware verification including:

(1) Developing a suite of assertions to be used for design regressions: once a design is mature, most of the interface boundary specifications are well defined and fine-grained assertions derived from specification mining can help catch regressions when design refinements or optimizations are being made.

(2) A starting point for formally specifying a design: once a design can pass random-stimulus based and directed unit tests, specification mining can be used to extract properties that have been consistently observed in the test waveforms. These properties can then be used as assertions to prove formally.

(3) Early anomaly detection and localization on long-running tests on mature RTL: if a specific test fails on an RTL design while many other tests pass, specification mining can reveal *where and when* a failing test begins to produce unusual behavior in the RTL, guiding the designer to the bug location.

In this report, we will focus on applying specification mining to address the last point above.

1.1 Motivation

RTL designs are increasing in complexity and are thus more prone to having subtle bugs that are not caught in regular verification flows. Typical techniques such as randomized-stimulus testing, directed testing, and fuzz testing have a difficult time catching bugs that require the RTL be put into a very specific state.

These subtle bugs are usually caught when performing chip emulation or FPGA prototyping when running realistic workloads on the RTL. Real workloads usually involve traces that are billion of cycles long, and are thus too slow to perform using RTL simulation which provides full design visibility. DESSERT[19] demonstrates a technique to capture full-visibility waveform traces from fast running FPGA simulation. Using DESSERT, an out-of-order RISC-V processor (BOOM[5]) is deterministically emulated on an FPGA with runtime assertion monitors while running the SPEC2017 benchmark suite. During the execution of several tests, synthesized assertions were violated which revealed there exists some subtle bugs in the core causing some benchmarks to fail.

Authors' address: Vighnesh Iyer, vighnesh.iyer@berkeley.edu; Donggyu Kim, dgkim@berkeley.edu, UC Berkeley.

While these assertions are useful for catching errors, they are very high-level and don't direct the designer to where a bug originated. As an example, the "`Pipeline has hung`" assertion (in BOOM) is generated with the following Chisel code:

```
// detect pipeline freezes and throw error
val idle_cycles = freechips.rocketchip.util.WideCounter(32)
when (rob.io.commit.valids.asUInt.orR ||
      csr.io.csr_stall ||
      io.rocc.busy ||
      reset.asBool) {
  idle_cycles := 0.U
}
assert (!(idle_cycles.value(13)), "Pipeline has hung.")
```

In words, this says, "If there is a good reason to stall the pipeline, reset `idle_cycles`, otherwise let it tick up to 13 before declaring something has gone wrong." This assertion does not give any insight as to what bad event happened, or when and where it happened. Since these assertions are thrown after billions of cycles it is possible that some μ-arch state was corrupted early in the simulation and only triggered this assertion much later during execution. DESSERT enables extracting waveforms for a variable number of cycles before the assertion triggers, but even with the waveform dumps in hand, the designer was unable to localize the bug. Our aim in developing this specification mining tool is to hunt out the locations of these trickly bugs in BOOM and fix them.

1.2 Hypothesis

Mature RTL designs (like BOOM) pass almost all tests run on them, including a full set of ISA tests, a boot of Linux, and real applications running on an OS. If a test fails on a mature design, we hypothesize that an *assumption* the designer made about the RTL was violated somewhere and at some time during the failing test execution, that was not violated on any successful test execution. These assumptions can include believing that a certain register cannot hold certain values or higher-level properties such as: "the memory system will respond to my request within 5 cycles".

We believe specification mining can be used to extract designer assumptions about the RTL design by mining fine-grained LTL properties on waveforms of successful test executions. These mined properties can be added to the RTL design as assertions and replaying the failing test should cause a violation of a mined property. These violations can be used to catch a faulty assumption *earlier and with greater locality* than the high-level assertions originally present in the design.

1.3 Problem Definition

Given:

- An RTL design driven with only one global clock
- A large set of VCD (value change dump) files produced when running a full suite of tests in an RTL simulator
- One or just a few failing tests in the suite characterized by a failed high-level assertion, hanging/global timeout, or a bad exit code

Produce:

- A set of mined LTL properties involving signals (combinational nets and registers) of the RTL design that aren't violated on any passing test
- A method of ranking the mined LTL properties
- A program that can check a VCD against the mined properties to find any violations for that execution trace

2 APPROACH

Our plan is to first create the products above with a small RTL design. We use `riscv-mini`[18], a simple 3-stage in-order RISC-V processor as the RTL we will use to test the specification mining engine. `riscv-mini` has real instruction and data caches and implements the RV32UI ISA subset which is capable of running the entire `riscv-tests`[37] test suite. The test suite contains a comprehensive set of ISA tests and benchmarks which will be used to generate the VCD files for mining.

2.1 Prior Work

Specification mining has been applied to both software and hardware verification.

2.2 High-Level Flow

The long-term plan is to leverage the spec mining engine and the prior work of DESSERT to provide an FPGA-acclererated debugging platform. We plan to take waveforms of successful test executions from RTL simulation and FPGA emulation of BOOM and feed the spec mining engine to infer LTL properties. The buggy RTL is instrumented by taking the LTL properties and converting them to property monitor FSMs which are stiched into the original design. The assertions are synthesized for FPGA emulation using the same methodology described in DESSERT, and the failing tests are executed. It is our hope that the failing tests will trigger failures in the mined properties before the failure becomes visible to the user (via a high-level assertion violation, hanging/timout, or a bad exit code).
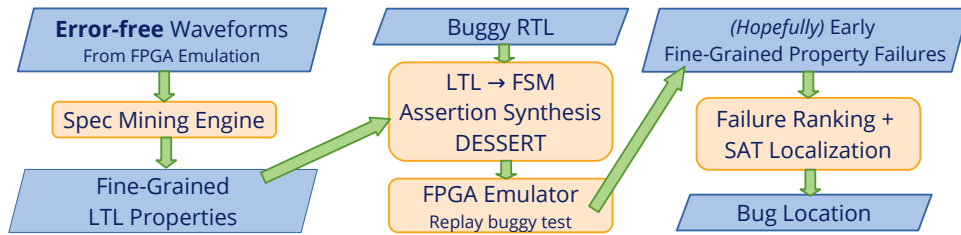

Fig. 1. The proposed tool flow to use specification mining and FPGA-accelerated simulation to pinpoint bug locations in for an RTL design .

The mined properties which were violated can be ranked based on the time of their violation and we can use the SAT localization techniques mentioned above to further pinpoint the bug location.

3 ALGORITHMS

3.1 Delta Traces

3.2 LTL Templates

3.3 Mining with Automata

3.4 Merging Properties

3.5 Checking Against VCDs

4 CHALLENGES

5 RESULTS

6 COURSE-RELATED

6.1 Roles

6.2 Usage of Class Topics

6.3 Feedback

Journals use one of three template styles. All but three ACM journals use the `acmsmall` template style:

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- `acmlarge`: Used by JOCCH and TAP.
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- `acmconf`: The default proceedings template style.
- `sigchi`: Used for SIGCHI conference articles.
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```

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π	1 in 5	Common in math
$	4 in 5	Used in business
Ψ_1^2	1 in 40,000	Unexplained usage

Table 2. Some Typical Commands

Command	A Number	Comments
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\table	300	For tables
\table*	400	For wider tables

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You may want to display math equations in three distinct styles: inline, numbered or non-numbered display. Each of the three are discussed in the next sections.

15.1 Inline (In-text) Equations

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15.2 Display Equations

A numbered display equation—one set off by vertical space from the text and centered horizontally—is produced by the **equation** environment. An unnumbered display equation is produced by the **displaymath** environment.

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$$\lim_{n\to\infty} x = 0 \tag{1}$$

Notice how it is formatted somewhat differently in the **displaymath** environment. Now, we'll enter an unnumbered equation:

$$\sum_{i=0}^{\infty} x + 1$$

and follow it with another numbered equation:

$$\sum_{i=0}^{\infty} x_i = \int_0^{\pi+2} f \tag{2}$$

just to demonstrate LaTeX's able handling of numbering.

16 FIGURES

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```
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  \caption{figure caption}
  \Description{figure description}
\end{teaserfigure}
```

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```

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18 ACKNOWLEDGMENTS

Identification of funding sources and other support, and thanks to individuals and groups that assisted in the research and the preparation of the work should be included in an acknowledgment section, which is placed just before the reference section in your document.

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...
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```

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19 APPENDICES

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```
\appendix
```

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- sidebar: Place formatted text in the margin.
- marginfigure: Place a figure in the margin.
- margintable: Place a table in the margin.

ACKNOWLEDGMENTS

To Robert, for the bagels and explaining CMYK and color spaces.

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A RESEARCH METHODS

A.1 Part One

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