DRILLS: Debugging RTL Intelligently with Localization from Long Simulation

Specification mining using trace dumps derived from long-running FPGA emulation to localize bugs in complex digital designs

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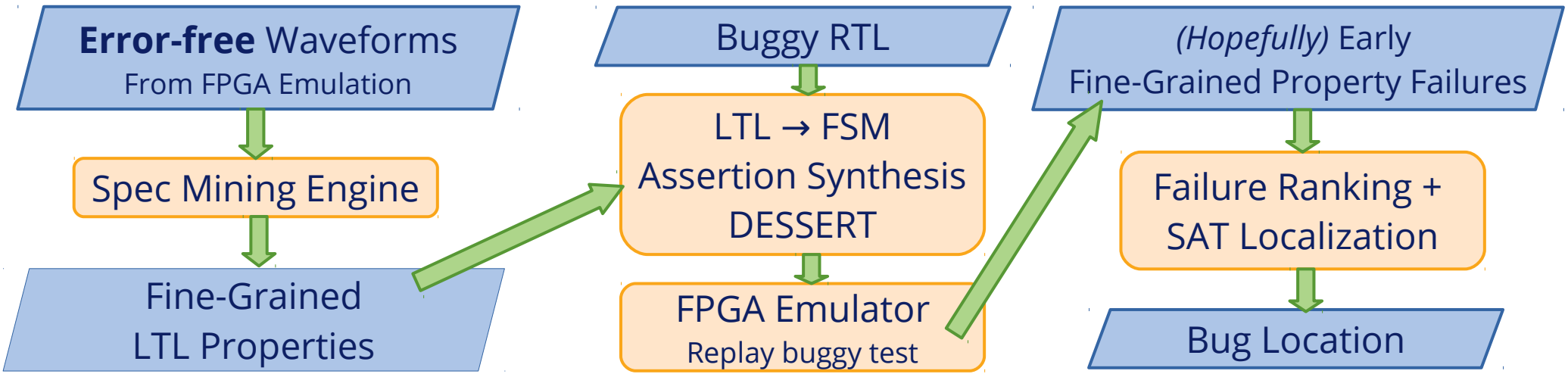
Problem Definition

- Higher RTL design productivity (Chisel, HLS) enables larger digital designs (e.g. BOOM-v2), but that means more bugs
- Tricky bugs only manifest after trillions of cycles (e.g. running SPEC2017) as high-level assertion failures
  - Pipeline hung, invalid writeback in ROB (see DESSERT [FPL'18])
- Even with a waveform, it is impossible or very laborious to figure out where the bug originated. *Can we automate this process?*
- **Problem**: given many error-free traces and one error trace, localize the likely bug location by module or line of RTL and find the fine-grained implicit properties which were violated.

Proposed Approach

- Prior work used mux instrumentation, SAT, and unrolling over a few cycles to find signals that if modified would mitigate an assertion failure
  - Offers little design intuition and scales poorly for large designs or a deep trace
- Specification mining [Li '10] is a technique to extract fine-grained (Σ = 2,3) LTL properties (based on a set of templates) from execution traces
  - We will add additional LTL templates, and will apply this technique to large designs



Current Status

- Working on reproducing spec mining engine from prior work
  - Extracting delta event traces from VCD (value change dump)
  - Mining basic LTL property templates from delta events:
    - Alternating: Δa **A** Δb
    - Until: **G**($\Delta a \rightarrow$ **X** (a **U** Δb))
    - Next: **G**($\Delta a \rightarrow$ **X** Δb)
    - Eventual: **G**($\Delta a \rightarrow$ **X F** Δb)
- Thinking about how to extend the spec mining work
  - Alternative LTL templates (that consider explicit cycle counts)
  - Different types of events to extract from a VCD (delta events on a bus may not be meaningful, can extract events on known interfaces like ready/valid)