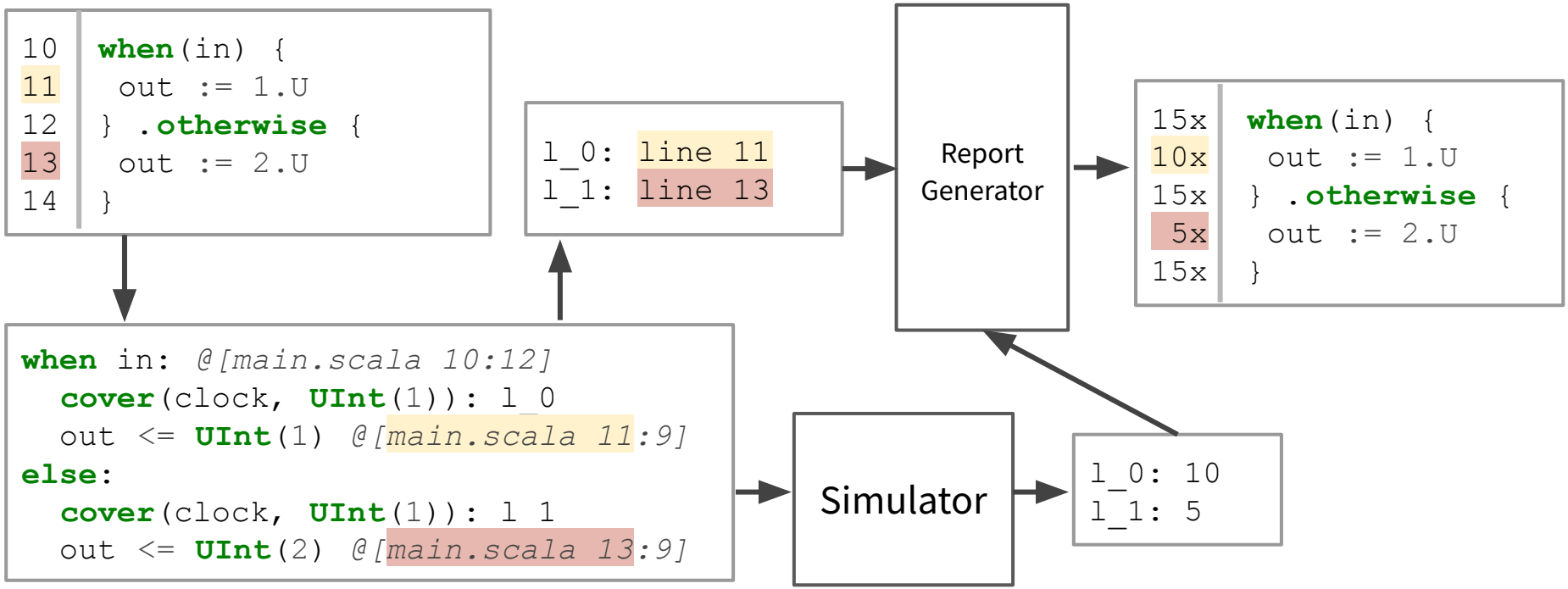
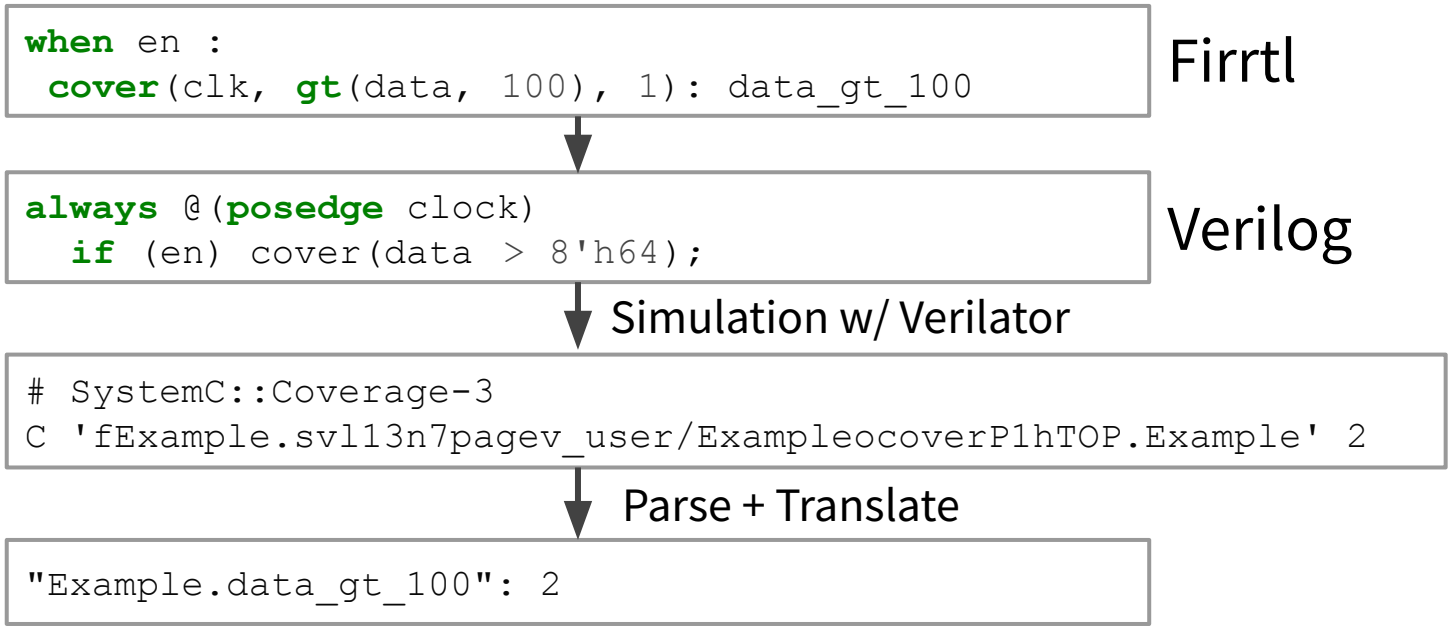
```
10  when(in) {
11    out := 1.U
12  } .otherwise {
13    out := 2.U
14  }
```

compiling to Verilog loses information

```
assign out = in ? 2'h1 : 2'h2;
```


10 when(in) {
11 out := 1.U
12 } .otherwise {
13 out := 2.U
14 }
when in: @[main.scala 10:12]
cover(clock, UInt(1)): l_0
out <= UInt(1) @[main.scala 11:9]
else:
cover(clock, UInt(1)): l_1
out <= UInt(2) @[main.scala 13:9]
l_0: line 11
l_1: line 13
Report Generator
15x when(in) {
10x out := 1.U
15x } .otherwise {
5x out := 2.U
15x }
Simulator
l_0: 10
l_1: 5


when en :
cover(clk, gt(data, 100), 1): data_gt_100
Firrtl
always @(posedge clock)
if (en) cover(data > 8'h64);
Verilog
Simulation w/ Verilator
SystemC::Coverage-3
C 'fExample.svl13n7pagev_user/ExampleocoverP1hTOP.Example' 2
Parse + Translate
"Example.data_gt_100": 2

	Line	Toggle	FSM	Ready/Valid	Mux Toggle	Condition
Verilator	✅/✅	✅/✅	✅/X	✅/X	✅/X	X
Treadle	✅/X	✅/X	✅/X	✅/X	✅/X	X
Firesim	✅/X	✅/X	✅/X	✅/X	✅/X	X
Yosys (Formal)	✅/X	✅/X	✅/X	✅/X	✅/X	X
ESSENT	✅/X	✅/X	✅/X	✅/X	✅/X	X