Er.S.VIGNESH

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Technically Curious and Growth-Driven Engineer with hands-on expertise in Bench characterization, mixed-signal IP (ADC/DAC) validation and Python-based test case automation and optimizing validation flows to reduce test cycle time. Currently expanding knowledge in Electrical validation of High Speed Interfaces , including PCIe, DDR, USB, and compliance testing using Keysight Automated Test Apps.

EDUCATION

- **Bachelor of Engineering –** Electronics and Telecommunications Engineering **| CGPA: 8.41**
  Karpagam College of Engineering | 2021 – 2025 |

EXPERIENCE

- **Silicon Validation Engineer - I (Bench Characterization) |**
  Organization: Tessolve Semiconductor Pvt. Ltd., Bengaluru **| July 2025 – Present**
  - Validation of RF Bias Controller IP Includes 12 bit DACs, 13 bit ADC, high side current-sense amplifiers, and temperature sensor**.**
  - Worked on Test Program Optimization ,reducing overall Test cycle time from 13 hours to 8 hours.
  - Learning Electrical validation of high-speed interfaces including PCIe, DDR, and USB. and High Speed Digital Instruments including Infinium UXR Scope, BERT, and DCA and Getting Familiar with Compliance testing and Keysight Automated Compliance test Apps.

TECHNICAL SUMMARY

- **Lab Equipment:** Keysight Infiniium UXR-Series Scope, M8045A BERT, ML4039B BERT,MSO , SMU, DAQ, DMM.
- **High Speed Interfaces** - PCIe, DDR , USB
- **Programming Skills -** Python, Verilog, Embedded C, C Programming, Assembly Language (8051& RISC-V)
- **Design & Simulation Softwares -** Cadence Virtuoso, Xilinx ISE , eSIM, Icarus iverilog, KiCAD, LTSpice, NGSpice

INTERNSHIPS

- **Silicon Validation Trainee (Bench Characterization) | Tessolve Semiconductor Pvt. Ltd., Bengaluru | Jan – July 2025**
  - Gained Expertise in bench characterization & Silicon Bring up and mixed signal validation, post-silicon debugging, and lab automation using Python.
  - Hands on training on high-speed Interfaces Includng PCIe , DDR , USB and Electrical validation using Keysight Infiniium UXR-Series oscilloscope, M8045A and eye diagram evaluation , jitter analysis and Compliance Testing
- **Summer Intern – VLSI Design | Kurukshetra University, Haryana | May 2023 – July 2023**
  - Designed and simulated low-power CMOS analog and digital circuits using Cadence Virtuoso.
- **FOSSEE Summer Fellow – eSIM EDA | IIT Bombay, Maharashtra | September 2023**
  - Enhanced subcircuit development for analog IC libraries.
  - Improved the functionality of the eSIM EDA tool for educational and design purposes.

PROFESSIONAL CERTIFICATIONS & BADGES

- **Keysight Digital Badge**
  - High-Speed Digital Design and Simulation
  - Automated Testing for High-Speed Digital Standards
  - Receiver and Bit Error rate Testing (BERT) Basics
  - Mastering PCIe Measurement Techniques
  - Deep Dive on Oscilloscopes
  - Oscilloscopes Triggering Fundamentals
- **NPTEL Certifications**
  - VLSI Design flow RTL to GDS
  - Digital Circuits
  - System Design Through Verilog
  - Microprocessor & Microcontroller
  - Introduction to C-programming
  - Basics Electrical Circuits
- **NPTEL Lab Certification - Electronics Devices and characterization - WEL Laboratory,IIT Bombay**
- **Purdue University & Intel - Semiconductor Fabrication 101**
- **Great Learning - Python Certification**
- **GATE 2024 - EC Domain - Score 261**