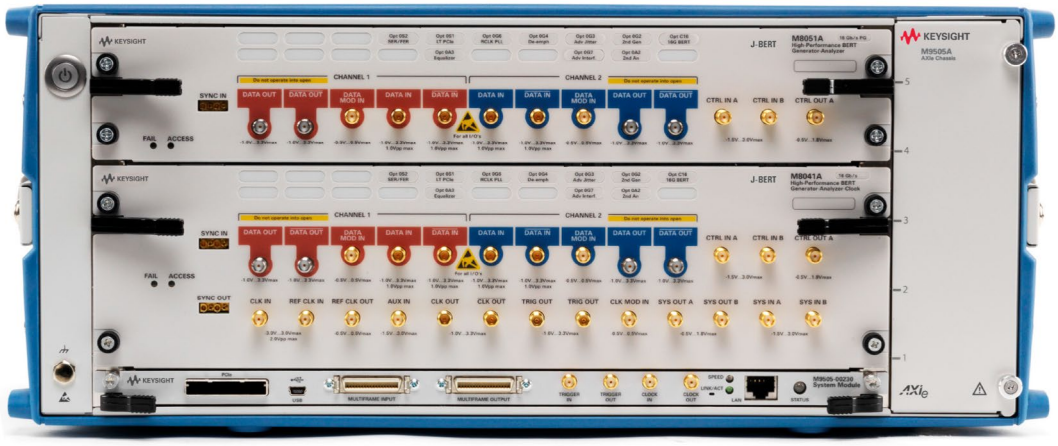
Keysight Technologies

Understanding PCI Express® 3.0 Physical Layer Receiver Testing

Application Note



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Overview

PCI Express® (PCIe®) technology has become the interconnect of choice for high-performance applications, including server, peripherals, graphics, imaging, and storage I/O. Designers of PCIe systems and devices are faced with the demand for ever-increasing speeds that can interoperate with the exploding number of PCIe-based devices.

As a broadly adopted technology standard, PCIe benefits from several decades of innovations with universal support in all major operating systems, a robust device discovery and configuration mechanism, and comprehensive power management capabilities that very few, if any, of the other I/O technologies can match. PCIe technology has a flexible, layered protocol that enables innovations to occur at each layer of the architecture, independent of the other layers.

The PCIe standard provides a way for multiple vendors to manufacture devices that can work together. The PCIe standard is on its 3rd generation with a 4th generation under development. PCIe is a serial point-to-point, multi-lane interconnect between two devices, which means it communicates directly with devices via a switch that directs data flow. This allows for “hot swapping” or “hot plugging,” meaning cards in PCIe slots can be changed without powering down the computer. It also offers scalable performance based on the number of signal lanes implemented on the PCIe interconnect. Each serial link transfers data in one direction only and can be routed as a differential trace pair, relatively independent of the other links. Each receiver/transmitter pair is called a lane. Physical layer testing is done on each PCIe lane. The need for robust testing for standards compliance remains critical.

The standards that comprise PCIe are managed by a non-profit organization called the Peripheral Component Interconnect Special Interest Group (PCI-SIG®). The PCI-SIG is run by a board of nine member-companies. Their efforts are divided across distinct parts of the specification. The electrical specification workgroup defines the electrical characteristics of the SerDes (serializer/deserializer), drivers, receivers, and equalizers. The protocol workgroup focuses on the link, protocol, and transactions.

PCIe Benefits

High performance	Low cost	Power management
– Low overhead – Full duplex, multiple outstanding requests – Scalable port width (x1 to x32) – Scalable link speed (2.5 /5.0 /8.0 GT/s/per lane)	– High volume/commodity – Can eliminate the host bus adapter (HBA) cost	– Direct attach to CPU can eliminate HBA power – Various low power levels (L0, L1, L2)

Background: PCIe Layers and Testing Requirements

Validating designs for PCIe performance involves characterizing the reference clock and data signals. There are three different categories of testing required to reach compliance; physical layer, datalink layer and interoperability tests. Products must successfully pass all of these at an official PCI-SIG workshop using the approved test fixtures to be deemed compliant and branded as an approved PCIe device. Key parameters include Phase-Locked Loop (PLL) bandwidth and peaking.

Figure 1 illustrates the different layers within the PCIe protocol and which of those layers apply to the different PCI-SIG test requirements.

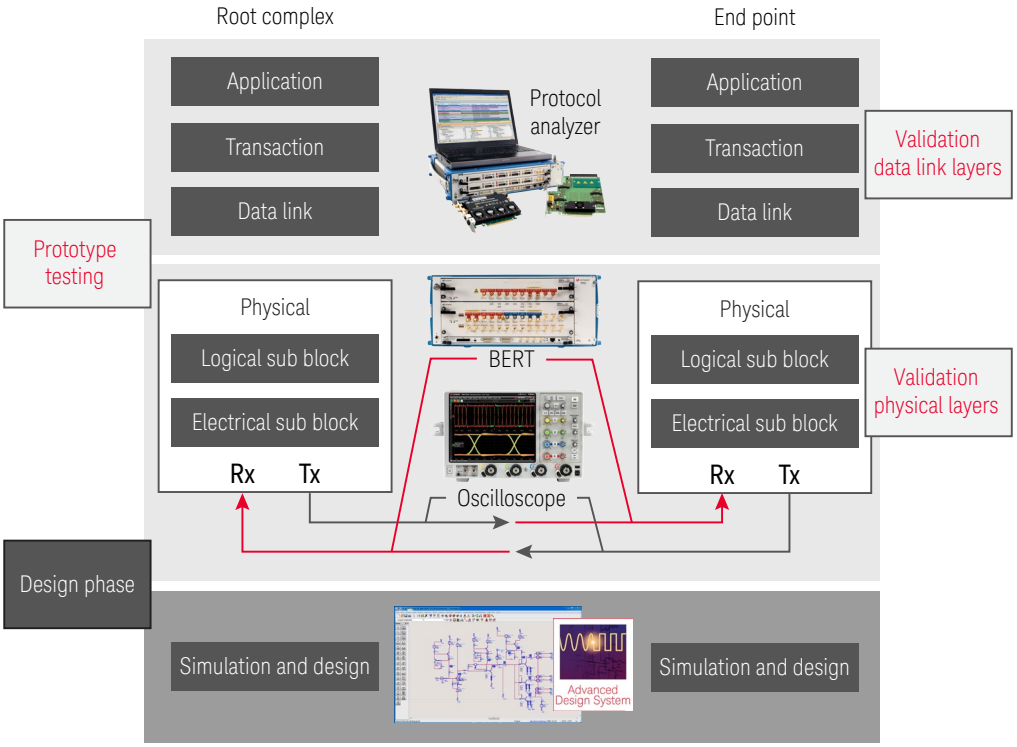


Figure 1. Visual representation of the layers and where testing occurs for each layer within a PCIe-based device.

For the physical layer there are two different specifications approved by the PCI-SIG, a Base spec and a PCIe Card Electromechanical (CEM) spec. The Base specification defines electrical performance at the die-pad of the device; the CEM specification defines performance at the connector. The two specifications operate independently. The Base spec is used for testing at the chip, new ICs for example, and has a larger set of tests that are run. For each of these specifications, physical layer transmitter and receiver testing must be done.

ICs with PCIe ports must be validated to ensure they meet PCIe specifications. The PCIe Base specification is the foundation for the PCIe specification framework. From a physical layer perspective, it specifies transmitter, channel, and receiver parameters as well as possible clocking architectures and the logical sub block. This application note focuses on receiver testing. (For a more in-depth understanding of the Tx and protocol-level testing processes and challenges, see 5992-0864EN *Successful PCI Express® Physical Layer Transmitter Testing* and 5992-0865EN *Data Link and Transaction Layer Testing for PCI Express® & NVMe™.*)

Challenge: Newer PCIe Generations Require Receiver Validation Tests

PCIe Rx test requirements and calibration methodologies are not the same for the different transfer rates of PCIe. Changes occurred for receiver testing with the PCIe 3.0 specification and will continue to evolve for PCIe 4.0. The table below summarizes some of the biggest changes in moving from PCIe 2.0 at 5 GT/s to PCIe 3.0 at 8 GT/s from a receiver testing standpoint.

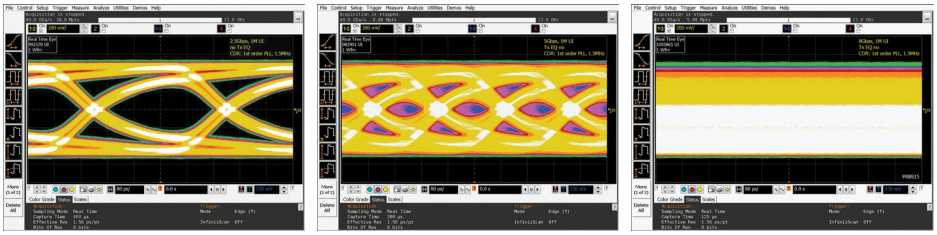
For the PCIe 3.0 specification, the reference point moved into the chip and the composition of the stress signal became more complex. The methodology describing the inter-symbol interference (ISI) channel to be used for Rx testing differs for 2.5 GT/s, 5 GT/s, 8 GT/s, and 16 GT/s. Because PCIe specifications require backward compatibility, a device validated at a higher data rate must be fully interoperable with lower data rates as well.

What is new for PCIe 3.0 Rx testing?

- Required as part of PCI-SIG specification compliance
- Test point moved inside the chip
- Jitter permeations became much more complex
- Equalization (EQ) at both Tx and Rx is now required

PCIe version	1.0a	1.1	2.0	3.0	4.0
Data transfer rate	2.5 GT/s	2.5 GT/s	5.0 GT/s (2.5 GT/s)	8.0 GT/s (2.5 & 5.0 GT/s)	16.0 GT/s (2.5, 5.0 & 8.0 GT/s)
Data fundamental frequency	1.25 GHz	1.25 GHz	2.5 GHz	4.0 GHz	8.0 GHz
Data encoding	PRBS 16 scrambling and 8b10b coding	PRBS 16 scrambling and 8b10b coding	PRBS 16 scrambling and 8b10b coding	2.5 and 5 GT/s: PRBS 16 scrambling and 8b10b coding 8 GT/s: PRBS 23 scrambling and 128b130b coding	2.5 and 5 GT/s: PRBS 16 scrambling and 8b10b coding 8 and 16 GT/s: PRBS 23 Scrambling and 128b130b coding
Total bandwidth for x16 link	~6.4 GB/s	~6.4 GB/s	~12.8 GB/s	~25.6 GB/s	~32 GB/s
Key changes	– Initial release	– Tighter jitter and reference clock tests	– Speed – Cable specification – PLL bandwidth test – Tighter jitter and reference clock tests – New de-emphasis levels	– Speed – Higher PLL bandwidth – More complex de-emphasis – PRBS 23 scrambling	– Speed – Shorter channel – Single connector – More transmit de-emphasis states – More taps on DFE – Much smaller RX eye height.
Physical layer test requirements	Tx	Tx	Tx, PLL	Tx, PLL, Rx	Tx, PLL, Rx

Figure 2 illustrates why some of these tests are now required. With the PCIe 3.0 specification and speeds beyond 5 GT/s, the eye at the receiver becomes closed. While transmitter validation continues to be an important element of PCIe testing, the device is dependent on the capabilities of the receiver in order to ensure the ability to meet the defined BER for PCIe of 10^{-12}. Receiver tests for speeds of 8 GT/s and 16 GT/s, as is possible in the PCIe 3.0 and 4.0 specifications, are the critical components of validation and ensuring interoperability of the systems.



PCIe 1.0
2.5 GT/s receiver eye

PCIe 2.0
5 GT/s receiver eye

PCIe 3.0
8 GT/s receiver eye

Figure 2. PCI Express eye diagrams as speed has increased generation to generation. The eye diagram for 8.0 GT/s and above is completely closed.

With an 8 GT/s signal, PCIe becomes a closed eye specification. A consequence of a closed eye specification with PCIe 3.0 and 8 GT/s is the receiver (Rx) can't "see" what the transmitter (Tx) sends, therefore the Rx negotiates with the Tx a proper Tx equalization to ensure a sufficiently open eye after the Rx equalizers. This negotiation is called link equalization training. These tests added with PCIe 3.0 are critical for success in 8 GT/s PCIe 3.0 and above.

Understanding Equalization (EQ)

Transmitters and receivers must communicate so that 1's and 0's can be identified correctly. This becomes a problem for fast data rates. Channel insertion loss between the Rx and Tx attenuate high frequency signal content. Certain patterns of 1's and 0's cause inter-symbol interference (ISI) that further degrade the eye.

Both Tx and Rx have equalization techniques that can be applied to help compensate for channel insertion loss and ISI. Beginning with PCIe 2.0 technology, transmitters began using equalization. Transmitter equalization in the time domain can be thought of as signal shaping. When transitions occur, the signal amplitude is exaggerated. This is known as pre-emphasis or de-emphasis and is shown in Figure 3a. Pre-emphasis and de-emphasis are identical. For those that use the top of the waveform as the reference, the lower-power state of the waveform is de-emphasized. For those who consider the lower-power state of the waveform as the reference, the heightened transitions are pre-emphasized. Transmitter equalization also involves pre-shoot. Using these techniques at the transmitter side, when a signal crosses the channel and arrives at the receiver, it will have a cleaner eye. For Rx testing, the BERT pattern generation block generates signals with equalization consistent with what a transmitter would generate.

Figure 3a. To help the transmitter create an eye that is cleaner when received at the pins of the receiver, the transmitter uses equalization techniques to compensate for channel insertion loss and ISI. For Rx testing, BERTs emulate equalization techniques that a transmitter will use.

Beginning with PCIe 3.0, links began incorporating both Tx equalization as described above and Rx equalization inside the IC. This was necessary since despite implementing Tx equalization, resulting eyes at the receiver were too small. Rx equalization involves two key techniques. One of these is CTLE, continuous-time linear equalization. The CTLE filters serial Rx input data to "boost" high frequency content to compensate for attenuation in the channel. DFE, decision feedback equalization, is used in combination with CTLEs, and zeroes out residual ISI remaining at the output of CTLE. This is done by subtracting out channel impulse responses of previous data bits to zero out ISI contributions on the current bit (Figure 3b). For Tx testing, oscilloscopes have application software that allows them to emulate equalization found inside the receiver IC.

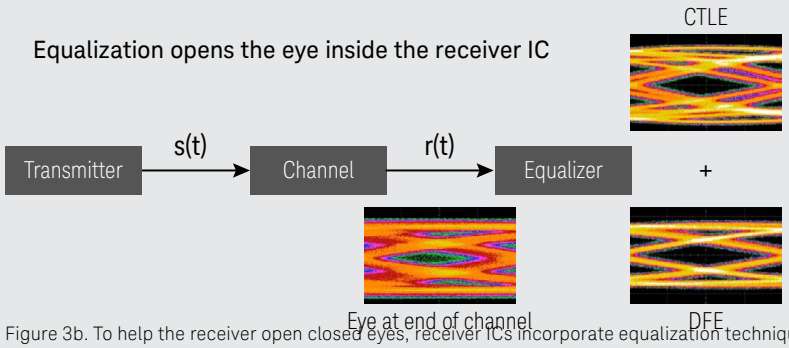


Figure 3b. To help the receiver open closed eyes, receiver ICs incorporate equalization techniques to compensate for channel insertion loss and ISI. These filters include CTLEs and DFEs. For Tx testing, oscilloscopes emulate the receiver equalization to show users what the eye looks like inside the receiver. The error detector functional block in the BERT opens the eye for error rate measurements.

Rx Test Specifications

Rx testing is used to determine the receiver's capability to properly detect the digital signal content, even for worst-case impaired input signals. For this testing, the input of the Rx under test is stimulated with a calibrated stressed eye signal from a bit error ratio tester's pattern generator (BERT PG).

This signal is composed of the impairments to be expected at the Rx input when it is operating in a target system. These include timing impairments, such as jitter, superimposed voltages, and ISI caused by channel loss emulating crosstalk. The latter is sometimes called noise, which implies a Gaussian distribution. For test purposes, this noise voltage is of sinusoidal shape. The intent of Rx testing is to send a stressed signal that is just on the edge of being within compliance, and see if the DUT receiver can process it.

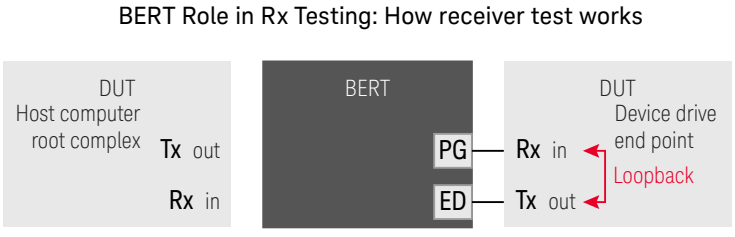


Figure 4. The BERT acts as the Tx out of the DUT to test if the receiver is working. It creates a series of signals from its pattern generator (PG), looks at what it gets back from the loopback in its error detector (ED), and determines how close that is to the original transmission.

KEY PCIe 3.0 8 GT/s receiver tests

- Rx Tolerance Tests: Verify receiver ability to work properly on worst case eyes
- Stressed voltage test base: Focus on tight eye height
- Stressed jitter test base: Focus on tight eye width in combination with jitter tolerance (JTOL) curve
- Jitter tolerance test CEM: Stressed Rx test with minimal eye width & eye height but JTOL curve is not checked
- Link EQ Rx test CEM: Verify the optimization algorithms for Tx equalization and Rx equalization function. The stress signal applied is identical to the jitter tolerance CEM test. Note: It is essential that all phases of the link EQ training are performed.

Correct detection of the digital content can be checked with the BERT's error detector (ED), after the Rx output signal is looped back internally through the Tx of the DUT (the Tx is assumed to operate error free[1])(Figure 4). The Rx specification dictates a complex jitter mixture to stress the device under test and ensure it can still parse information.

While receiver designs operating at 2.5 GT/s and 5.0 GT/s could rely solely on transmitter EQ and be implemented without receiver equalization, the increased transmission rate via basically the same channel makes Rx EQ necessary and consequently testing of receiver gain more important. Tx EQ was extended with pre-shoot next to de-emphasis. The Link Training Status State Machine (LTSSM) was extended by a mechanism which allows an Rx to request Tx EQ changes during link training.

The Base specification and the CEM specification have chosen different simulation and calibration approaches. Calibration for each specific component of jitter is required.

A calibration according to the Base specification simulates the entire receiver stress signal based on a channel measurement via a step response, and stressors are input parameters to the simulation. The simulation tool recommended is SEASIM, a python script available from the PCI-SIG webpage. Based on the simulation, the stressor parameters required to achieve the necessary eye height (EH) and eye width (EW) have to be determined. The stressors are then calibrated to the parameters determined by the simulation at more suitable test points to reduce measurement uncertainty as much as possible.

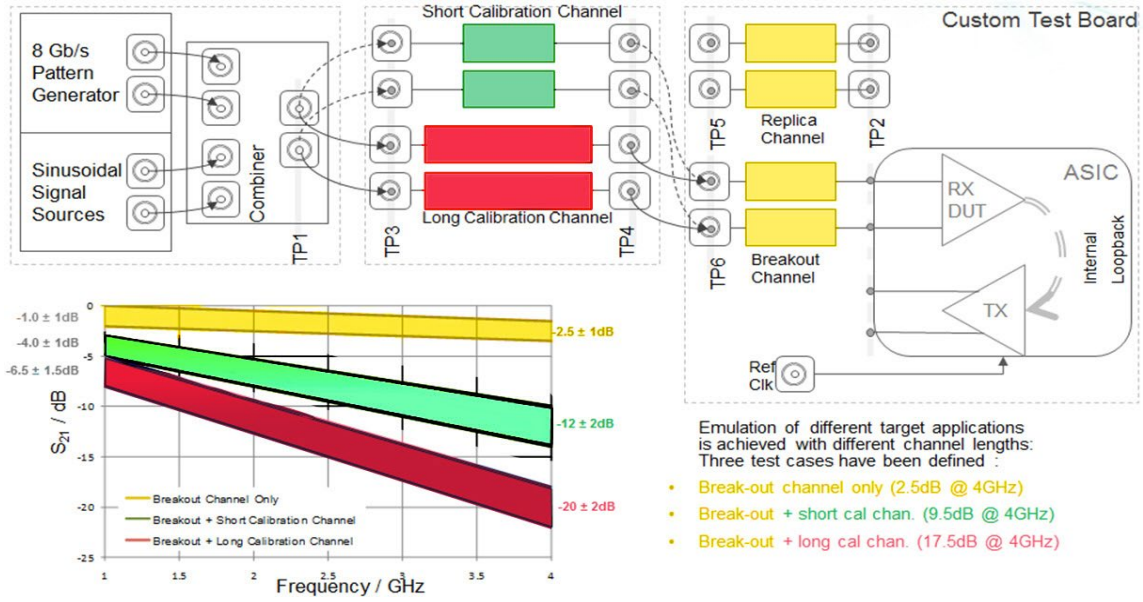


Figure 5. Base specification test points for 8 GT/s receiver calibration

The Base specification Rx test is broken down into two major tests: stressed voltage test and stressed jitter test. The stressed voltage test is performed for three different test cases: no channel, short channel, and long channel (Figure 5); the stressed jitter test uses the long channel only. The stressed voltage test puts more emphasis on EH and requires an amplitude stressor in the form of a differential mode sinusoidal interference (DM-SI) and common mode sinusoidal interference (CM-SI) in addition to jitter stressors. As a result, a complete base specification Rx test for 8 GT/s is comprised of four different Rx tests.

1. In this context "error free" is equivalent to a detection with a BER lower than a specified value, very often 10^{-12}.

The PCIe Base specification is the most relevant for chipset testing, where both synchronous and asynchronous operations are supported. Three different types of clocking architectures are possible:

1. Common reference clock (CC), which is synchronous
2. Data clocked (DC), which can be either synchronous or asynchronous
3. Independent reference clock (IR), which is asynchronous

Different test requirements are defined for 8 GT/s and 16 GT/s Rx testing for synchronous and asynchronous operation. (See Figure 6 for common PCIe acronym glossary).

Originally, asynchronous operation was allowed in the absence of spread spectrum clocking (SSC) only. Separate reference clock no SSC (SRNS) is used to describe asynchronous operation without SSC and separate reference clock independent SSC (SRIS) is used to describe asynchronous operation with SSC.

CC	Common reference clock
DC	Data clocked
IR	Independent reference clock
DM-SI	Differential mode sinusoidal interference
CM-SI	Common mode sinusoidal interference
SSC	Spread spectrum clocking
SRNS	Separate reference clock no SSC
SRIS	Separate reference clock independent of SSC
RJ, SJ	Random jitter, sinusoidal jitter
EH, EW	Eye height, eye width

Figure 6. TLP: PCIe Clock Glossary Reference

With the addition of SRIS to the base specification, two jitter tolerance masks were introduced.

- CC is tested without SSC except if a system is tested and SSC cannot be turned off.
- SRNS is always tested without SSC and SRIS is tested with SSC activated but the modulation profile differs for the stressed voltage test and stressed jitter test.

In the case of a stressed voltage test, a triangular down spread is used while a sinusoidal down spread is used for stressed jitter test.

The CEM specification calibration procedure is based on a measurement of the stress signal with activated stressors. A measurement analysis software called SigTest is used to determine RJ, SJ, EH, and EW. SigTest is a software package available from the PCI-SIG and compiles the entire set of tests defined to test all aspects of the PCIe standard. It is the software package that is used for all PCIe electrical testing at compliance workshops. SigTest embeds the behavioral Rx package and simulates equalization stages and clock recovery according to the reference receiver.

The CEM specification Rx tests combine the long channel stressed voltage test and stressed jitter test into one Rx test to reduce test time at workshops. For the same reason, it does not check the sinusoidal jitter (SJ) template outlined in the Base specification. An additional difference between the CEM and Base specification is that CM-SI is not part of the stressor mix to reduce the complexity of the test setup required at workshops.

The Rx link equalization test is different from a standard jitter tolerance in terms of the method used to train the DUT into loopback. Loopback for a standard jitter tolerance can be forced or trained through the LTSSM state configuration while for the receiver link equalization test, the receiver needs to be trained through “L0” and “recovery” states.

PCIe 4.0 (16 GT/s) Rx Testing

Currently, the PCI-SIG is focused on the fourth generation of PCIe technology. To move from 8GT/s (3.0) to 16GT/s (4.0), techniques from the previous generation will have to be pushed even further. This includes Rx equalization as well as using statistical techniques to analyze channel compliance.

The major breakthroughs of 3.0, such as moving from 8b/10b encoding to 128b/130b (which afforded a 20% performance improvement), are not available for the next-generation release. Achieving PCIe 4.0’s target of 16 GT/s will require the cumulative effect of many smaller adjustments across the transmitter, channel, and receiver in order to be successful.

PCIe 4.0 will have a shorter length of the channel. PCIe 3.0 was designed to operate with a maximum 50 cm (20 inch) channel with two connectors, supporting a 20 dB of loss at Nyquist (4 GHz). For 4.0, the Nyquist frequency must increase to 8 GHz, which subsequently incurs additional insertion loss. Without mitigating technology, the channel length for PCIe 4.0 is going to be significantly shorter and will likely support only one connector.

Doubling the data rate and shortening the PCIe 4.0 channel will result in much greater eye closure than that seen in the previous release. Even higher channel loss and increased ISI will require more robust Tx and Rx equalization for accurate operation.

Keysight Solutions

It is important that the portfolio of PCIe design and measurement solutions (from physical layer Tx and Rx characterization, interconnect, software simulations, and protocol layers) cover and map to the development of the next generations of PCIe standards. Keysight has a complete portfolio to design, simulate, and test interconnects, transmission lines, physical layer Tx and Rx tests, and data link and transaction layer tests at the protocol level. In addition to test solutions, Keysight's skilled application engineers with access to PCIe experts can help you with your PCIe test challenges.

Keysight J-BERT M8020A & N5990A test automation platform

The J-BERT M8020A High-Performance BERT is a scalable system for computer bus as well as datacenter interface applications. The design of the J-BERT M8020A was developed for the needs of PCIe Rx testing. The extension of stress sources, integration of de-emphasis into each pattern generator data output and EQ capabilities into each error detector data input, and integrated reference clock multipliers all simplify the PCIe Rx test setups greatly.

The M8041A BERT module of the J-BERT M8020A BERT system offers data ranges up to 8.5 Gb/s or up to 16.2 Gb/s. The 16.2 Gb/s version allows testing of receivers for all four transfer rates.

The J-BERT M8020A BERT system includes support for LTSSM, enabling real hand-shaking for device loopback training through configuration and recovery for PCIe at 8 GT/s. The J-BERT M8020A is designed to help master both current (PCIe 3.0) and next-generation (PCIe 4.0) Rx designs. The applicable specification defined by the target device, transfer speeds, and clocking-operations mode will determine the required Rx test setup.

De-emphasis output stages, reference clock multipliers, stressors, and CDR and CTLE for the BERT ED are all integrated into the J-BERT M8020A. This minimizes the necessary components for receiver test to the BERT itself, DC blocks, reference channel + test fixtures, and an oscilloscope for calibration.

Differences in specification reference points, specification and calibration methods for the transfer rates and between Base and CEM Specifications make receiver testing and stress signal calibration a challenging task. Some of the calibration steps are tedious and time consuming. Test automation software significantly reduces calibration errors and the time an operator needs to attend to a calibration or test.

The J-BERT M8020A BERT is supported by the N5990A Test Automation Platform for PCIe. Keysight's N5990A Test Automation Platform offers a complete PCI Express receiver test suite. It is the only test automation software covering all transfer rates, Base specification as well as CEM / PHY test specification testing for AICs, and systems as well as clocking architectures including the new SRIS use case.

The implemented calibration procedures use the PCI-SIG SEASIM and SigTest when required. User interaction is required only when setup changes need to be performed. Next to compliance testing, the N5990A-101 PCI Express Rx test suite offers extensive characterization tests like tolerance tests and sensitivity tests. Two different methods to determine the most suitable Tx EQ combination for a DUT for 8 GT/s are included.

Keysight Product Info Highlights: J-BERT M8020A

- Data rates up to 8.5/16 Gb/s for pattern generator and error detector
- Four 16 Gb/s BERT channels in a 5-slot AXIe chassis. Expandable to 32 Gb/s with M8061A multiplexer
- Integrated and calibrated jitter injection: RJ, PJ1, PJ2, SJ, BUJ, sinusoidal interference(com-mon-mode and differential-mode), SSC (triangular and arbitrary, residual)
- 8-tap de-emphasis (positive and negative) up to 20 dB
- Integrated and adjustable ISI for loss emulation
- Interactive link training for PCIe
- Built-in clock data recovery and equalization
- Designed for both current PCIe 3.0 & upcoming PCIe 4.0 specs

Keysight Product Info Highlights: N5990A-101 PCIe Rx Test Suite

- One-button compliance test
- Expert mode for unique in-depth, automated characterization and margin test
- Unified test structure and user interface for a wide range of high-speed digital buses
- Test libraries, optimized for ease of use, minimum test, and significantly reduced calibration times
- Automated single and multi-lane measurements
- Powerful interfaces to data bases and web servers

Summary

Faster PCIe standards introduce new challenges for receiver testing and verification. PCIe 3.0 (8 GT/s) doubled the speed of the previous generation and required both Tx and Rx equalization techniques. PCIe 4.0 (16 GT/s) will require even more equalization, and the channel will be shortened from the previous generation.

While transmitter validation will continue to be an important element of PCIe testing, devices are dependent on the capabilities of the receiver in order to ensure the ability to meet the defined BER for PCIe, 10^{-12}. Rx analysis is now critical to PCIe validation and ensuring interoperability of systems.

Keysight's J-BERT M8020A was developed for the needs for the current PCIe 3.0 and upcoming PCIe 4.0 Rx testing standards. A suitable test set-up based on the J-BERT M8020A and automation of the calibration procedure is available with Keysight's N5990A Test Automation Platform.

Keysight hardware, software, and application experts can help you debug tests and verify PCIe compliance quickly, independent of which PCIe standard you are targeting.

Keysight gets involved, you benefit

Keysight's solutions for digital applications are driven and supported by Keysight experts that are involved in the various international standard committees. We call it the Keysight Digital Test Standards Program. Our experts are active in the Joint Electronic Devices Engineering Council (JEDEC), PCI Special Interest Group (PCI-SIG®), Video Electronics Standards Association (VESA), Serial ATA International Organization (SATA-IO), USB-Implementers Forum (USB-IF), Mobile Industry Processor Interface (MIPI) Alliance, and many others. Our involvement in these standards groups and their related workshops, plugfests, and seminars enables Keysight to bring the right solutions to the market when our customers need them.

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