module testbench;

// Inputs

reg clk;

reg d;

reg rst;

// Outputs

wire q;

// Instantiate the Unit Under Test (UUT)

dff uut (

.clk(clk),

.d(d),

.rst(rst),

.q(q)

);

always #2 clk = ~clk;

initial begin

// Initialize Inputs

clk = 1;

d = 1;

rst = 0;

// Wait 100 ns for global reset to finish

#100 d= 0;

        #100 d=1;

// Add stimulus here

end

endmodule

On Thu, Feb 13, 2014 at 5:03 PM, Navya Arunselvan <[navya.arunselvan@gmail.com](mailto:navya.arunselvan@gmail.com)> wrote:

module dff(clk,d,rst,q);

input clk;

input d;

input rst;

output q;

reg q;

always @(posedge clk)

begin

if(rst)

q=0;

else

q=d;

end

endmodule