Project Questions (EL 203)

Instructions:

1. Report should be limited to 5 pages.
2. Extra credit will be given for novelty in your solution.
3. Report should not include any VHDL code.
4. Use snippets of the code to explain the ASM/SM.
5. You may use HDL/codes from any source. In such a case please provide the reference and give credits to the originator. In the absence of it, you will be awarded a zero in the assignment.
6. Understand the designs steps even if you may not have directly contributed to that part.
7. Clearly write your contributions in your report.
8. Your design should be a demonstrable.

For each of these projects, choose an appropriate FPGA as a target device and carry out the following steps:

1. Work out an overall design strategy for the system and draw block diagrams. Divide the system into modules if appropriate. Develop an algorithm, SM charts, or state graphs as appropriate for each module. Unless otherwise specified, your design should be a synchronous system with appropriate circuits added to synchronize the inputs with the clock.

2. Write synthesizable VHDL code for each module, simulate it, and debug it. To avoid timing problems in the hardware, use signals instead of variables and make sure the code synthesizes without latches. Use test benches when appropriate to verify correct operation of each module.

3. Integrate the VHDL code for the modules, simulate, and test the overall system.

4. Make any needed changes and synthesize the VHDL code for the target device. Simulate the system after synthesis.

5. Generate a bit file for the target device and download it. Verify that the hardware works correctly.