

NEXT-White experiment energy plane electronics design

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Abstract

NEXT-White (NEW) experiment is looking for the neutrinoless double beta decay of ^{136}Xe , and therefore requires good level of radiopurity. To this end, the PMTs used for the energy measurement and their electronics have been designed and implemented in the NEXT-White (NEW) demonstrator not only considering the 1% energy resolution required but taking into account radiopurity limitations. The design was done to assure the required front-end electronics specifications such as linearity and low noise and also meet a low radioactivity level. In order to reduce low frequency noise effects and enhance detector's security a grounded cathode connection has been used. A detailed description of the electronics and required signal postprocessing to obtain a liner response and overcome AC coupling effects are provided.

Keywords:

Energy, plane, PMT, Calometry, Front-end electronics, FEE, ATCA, DSP, BLR

1. Introduction

NEXT (Neutrino Experiment with a Xenon TPC) [1] is a neutrinoless double-beta ($\beta\beta 0\nu$) decay experiment at the Canfranc Underground Laboratory (LSC) [2]. It seeks to detect the ($\beta\beta 0\nu$) decay of ^{136}Xe using a high pressure xenon gas TPC with electroluminescent (EL) amplification. The NEXT-White (NEW) detector (shown on figure 1), with an active xenon mass of about 10 kg at 15 bar, is the first NEXT prototype installed at Canfranc Underground Laboratory (LSC). It implements the NEXT detector concept tested in smaller prototypes using the same radiopure sensors and materials that will be used in the future NEXT-100, serving as a benchmark for technical solutions.

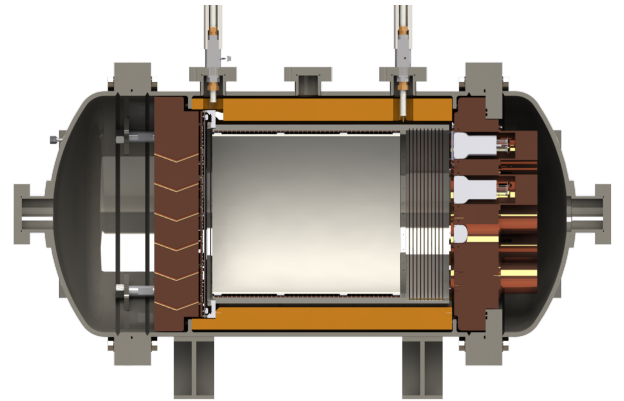


Figure 1: NEW detector

The NEW detector is fully operational at LSC. A low background run using depleted Xe is foreseen

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during 2018; these data will be essential to validate the background model of NEXT-100, based on the radiopurity measurements of all the relevant components.

A background of 4×10^{-4} counts $\text{keV}^{-1} \text{kg}^{-1} \text{y}^{-1}$ in the energy region of interest means the experiment is sensitive to a half life of up to 6×10^{25} years after running for 3 effective years [3, 4]. The required background level is achievable thanks to passive shielding, background discrimination techniques based on charged particle tracking [3, 5] and a thorough material radiopurity control.

The energy plane of NEW consists of a 12 cm thick copper support plate with 12 sapphire windows brazed in copper flanges and then screwed to the copper plate (figure 2). A 12 cm thick copper cap is placed behind each PMT, to shield the fiducial volume. The energy plane will be held at vacuum levels of less than 10^{-4} mbar. Twelve high-gain PMTs from Hamamatsu(R11410-10) [6] are optically coupled to the sapphire windows using NyoGel OCK-451, and held in place with a plastic support and spring. The external face of the windows is coated with tetraphenyl-butadiene (TPB) to shift the xenon VUV light to blue and coated with PDOT (poly(3,4-ethylenedioxythiophene)), a conductive polymer which stops the electric field from the TPC penetrating as far as the PMT dynodes.

The twelve PMTs are located 12 cm behind the TPC cathode and cover approximately 30% of its surface area. This level of coverage was chosen as a compromise between the need to collect as much light as possible and the need to minimize the number of sensors to reduce cost, technical complexity and radioactivity. The selected model R11410-10 is a 3" PMT specially developed for low-background operation, equipped with a synthetic fused silica window and a photocathode made of low temperature bialkali with high quantum efficiency.

2. PMT base circuit

The PMTs receive high voltage and have their signal extracted via kapton twisted cables connected to a feedthrough in the torispherical

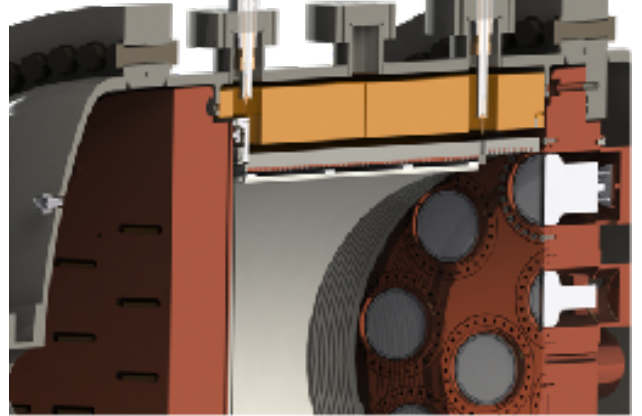


Figure 2: Energy plane detail

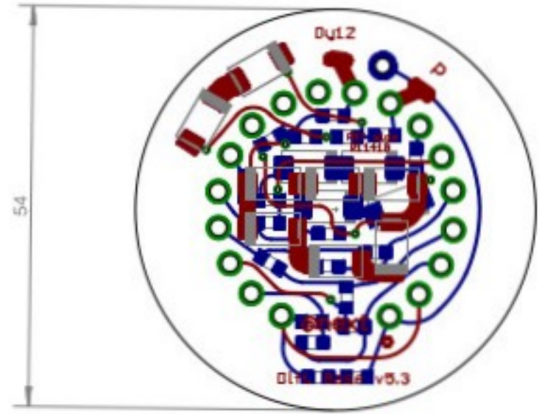


Figure 3: Base Circuit layout

head of the pressure vessel. The distribution of signal and bias voltage at each individual PMT is done by means of a circular kapton circuit board (PMT base) with receptacles for the eighteen PMT pins. The PMT base (figure 3) is covered with thermal epoxy (Araldite 2011®) to avoid dielectric breakdown in moderate vacuum or in a N2 atmosphere, backed with a 12-cm thick copper cap to shield the detector against external radiation and connected to the support plate to allow generated heat to be dissipated under vacuum conditions.

PMT bases must meet specifications such as low heat dissipation, excellent linearity and low radioactivity. Their design follows the manufacturer's reference scheme for grounded

cathode connection (figure 4) since the whole detector structure must be connected to earth for electrical safety reasons. In this configuration, the anode output must be AC coupled through an isolation high-voltage capacitor since anode output DC voltage equals the high voltage being applied to the PMT. The resistor chain acts as a voltage divider, defining the dynode-to-dynode voltages. Total voltage across the PMT (+HV in figure 4) is 1270 V, a trade-off between single photon detection capability and manufacturer's recommended high voltage range for best linearity.

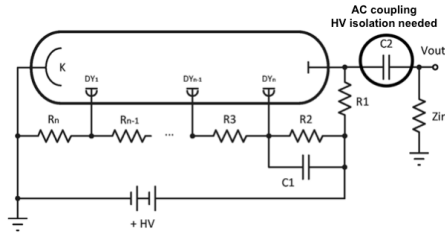


Figure 4: Grounded Cathode PMT connection scheme

2.1. Power dissipation

Taking into account static power consumption constraints, a lower limit for resistor values can be established. Manufacturer recommended ratios between the twelve dynode voltages allow us to define a set of values for base resistors (R1-R11, R13, R15 and R18 in figure 5, the actual PMT base circuit). Total power dissipation for each base depends on the exact high voltage supplied to the PMT and will lie in the range of [30-40] mW. Simulations with finite elements software (Comsol Multiphysics) have been carried out to study the heat flow in vacuum condition, yielding a harmless 3 °C increase above ambient temperature. This results was later verified in laboratory.

2.2. Optimizing the base circuit design

In order to enhance output signal quality and decrease distortion, resistors R12 and R14 in figure 5 are suggested by the manufacturer to limit the ringing effects due to impedance mismatch in

dynodes connections. On the other hand resistors R16 and R19 (equivalent to R1 in figure 4) isolate anode terminal from HV connection allowing signal output generation prior to AC coupling capacitor (C2 in figure 4).

The most important design requirement is linearity over the whole dynamic range, spanning from a single photon up to 100k photons. Signal length in NEW can vary from a few microseconds up to $\sim 150 \mu s$. The base circuit must provide enough charge for the PMT with negligible change in dynode-to-dynode voltage in any situation. Changes in these voltages introduce a time varying gain which acts as a nonlinear distortion mechanism and has a strong effect on linearity. Since each dynode stage increases the gain by a given factor (based on the geometry and characteristics of the PMT) the highest voltage drops will be located at the last stages where the amount of charge demanded by the dynodes is higher. Therefore, starting from the anode, a number of stages will be backed with capacitors (charge storages) to stabilize dynode voltages.

A trade-off between radiopurity limits [3] (as capacitors show a high activity in a number of radioisotopes) and linearity requires to carefully chose the minimum number of capacitors that allow to meet the linearity goal of a worst-case 1%.

The algorithm described in figure 6 was followed in order to reach the final circuit in figure 5. SPICE simulations allow to find out the required capacitor values, using as criteria a worst-case voltage drop between dynodes of 0.1%. A laboratory linearity test bench (including the PMT, base circuit, cabling and front-end electronics) determines the number of capacitor-backed stages to guarantee a 1% linearity.

In the test bench, a signal generator introduces a square voltage pulse with very short rise and fall edges into the LED (435 nm centered radiation spectrum). The amount of photons being generated is proportional to the length of the pulse. In order to avoid LED switching effects the minimum pulse length is 20 μs (the setting time of the LED is in order of 1 μs). The effect of LED output fluctuation is limited by averaging over 200 samples for each device under test. Additionally, a set of 90% attenuation optical filters were used directly coupled to the LED.

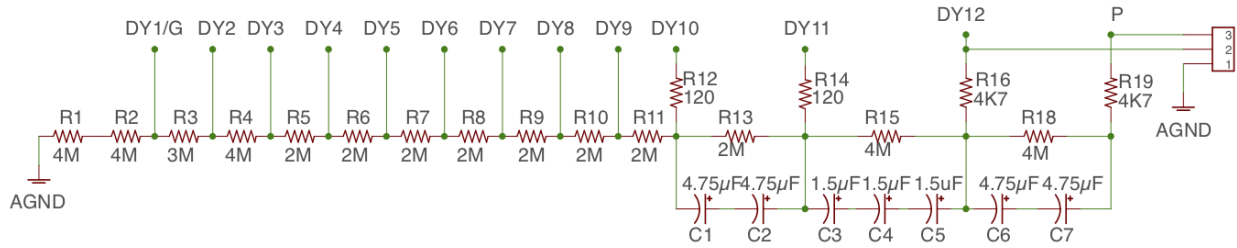


Figure 5: NEW base electronic design

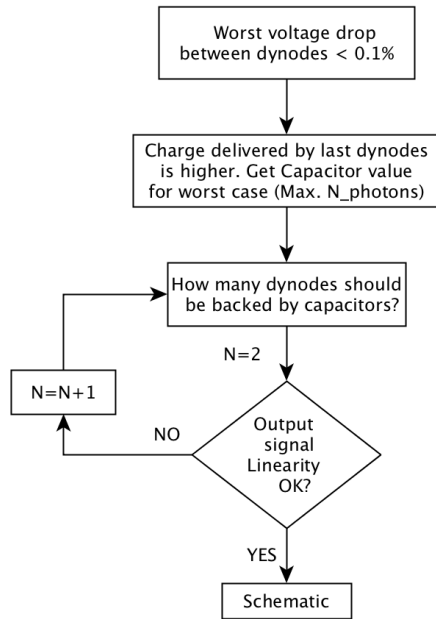


Figure 6: Algorithm for finding the PMT base component values

Signal Distortion

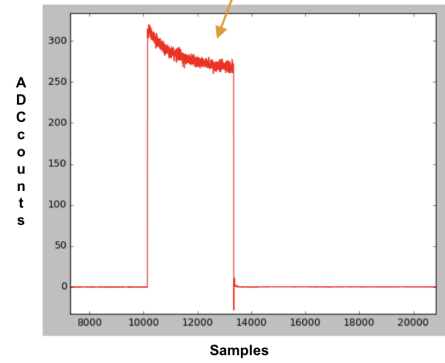


Figure 8: Linearity of the PMT base with 2 stage capacitors (5 units). 80us pulse

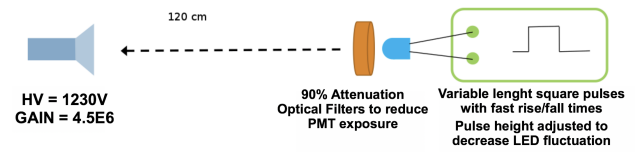


Figure 7: LED based PMT+FEE test bench for linearity measurements

A first proposal based on two stage coverage (5 capacitors to withstand the high voltage between terminals) was tested. Although generally this design shows good linearity, there remain some long-pulse-length signals with non-linear distortion in time (figure 8). The output signal does not show a typical overload effect which would appear in the case of a usual fall in the gain value for

high number of photons. The observed behavior is related to a distortion mechanism that appears due to charge redistribution in the base capacitors. It is possible for a capacitor which has been depleted to drain charge from the previous (left) capacitor in the chain. If the charge drained is too high, voltage drops accumulate, affecting overall gain. The length of signal pulse able to generate this distortion depends on the time constants of each stage and may change with voltage distribution among stages. The measured linearity¹ for two stage configuration is 1.95% for 100k photo electrons.

As a better capacitor coverage is required, a three-stage configuration is proposed. This circuit shows virtually no time distortion. The linearity fit gives a 0.38% for 140k photo electrons, exceeding the initial requirements for linearity (less than 1%).

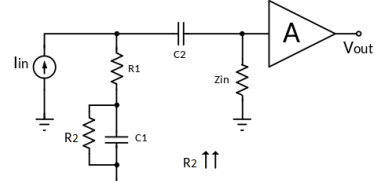
3. Front-end electronics

Front-End Electronics (FEE) and complementary Digital Signal Processing (DSP) techniques will be described in this section. Also data measurements taken in order to verify FEE behavior and validate DSP techniques will be presented.

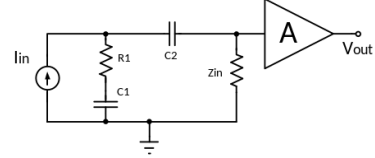
3.1. Grounded cathode connection

The use of an AC coupling scheme implies a high pass filter (HPF) will be created. Such a filter blocks DC component and attenuates frequency components below the cutoff frequency (f_{cutoff}). The whole model of FEE includes (see figure 9 (a)) last stage effect of the base ((R2 parallel with C1) + R1) by the pseudodifferential connection. In order to reduce complexity we assume R2 has such a high value that it can be neglected (figure 9 (b)). The PMT is modelled as a simple current source model. The Laplace transfer function of the whole system can be obtained as (eq. 1) and its f_{cutoff} can be approximated to (eq. 2) since C1 is greater than C2.

¹ Measured as the worst case desviation from the linear fit



(a) FEE + PMT base



(b) FEE + PMT base simplified

Figure 9: FEE Full model.

$$\frac{v_O}{i_I} = \frac{Z_{in}}{(1 + \frac{C_1}{C_2})} \frac{1 + R_1 C_1 s}{1 + \frac{(R_1 + Z_{in}) C_1}{(1 + \frac{C_1}{C_2})} s} \quad (1)$$

$$f_{cutoff} = \frac{1}{\frac{(R_1 + Z_{in}) C_1}{1 + \frac{C_1}{C_2}} \cdot 2\pi} \approx \frac{1}{(R_1 + Z_{in}) C_2 \cdot 2\pi} \quad (2)$$

$$f_{LFzero} = \frac{1}{R_1 C_1 \cdot 2\pi} \quad (3)$$

As stated in (eq. 1) HPF is modified by a zero at a lower frequency (f_{LFzero}) shown in (eq. 3) due to base circuit effect. The zero effect reduces low frequency range attenuation and modifies FEE frequency response whose final modulus and phase are shown on figure 10.

3.2. High τ constant value solution

Since the τ (time constant) of the equivalent circuit shown in figure 9b is proportional to the inverse of f_{cutoff} , a higher τ will attenuate a shorter range of frequencies producing a signal which closely resembles the original one. However there is a problem with the implementation of this solution: good quality AC coupling capacitors that can withstand high voltages typically have low

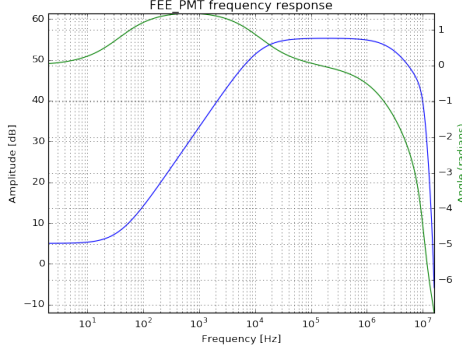


Figure 10: FEE Full Frequency Response.

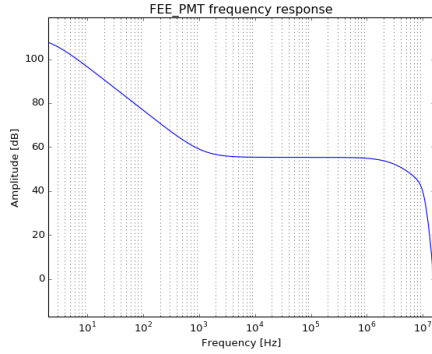


Figure 11: FEE Full Frequency Response for high τ solution.

nominal values. It is hard to find capacitors higher than ~ 10 nF that meet such specifications forcing the use of high value resistors.

Such high value resistors may amplify low frequency components as shown on figure 11. This effect will translate into additional baseline shifts or baseline wandering.

3.3. Digital Baseline Restoring alternative

Our proposal for this novel FEE design is to reduce the value of the R1 resistor. This would bring a wide swing in the baseline but it can be accurately recovered using a Digital Signal Processing algorithm once the AC coupled signal has been acquired. The decision has been taken based on the results shown in the previous section: extremely high resistor values gave results too close to the energy resolution limits, and second

order effects related to components parasitics might have a strong influence on final results. Moreover high impedance nodes such as the associated to high resistors are more sensitive to coupled external noise. As a result, a trade-off between low frequency effects suppression and feasibility of signal recovery has been established. The lower the f_{cutoff} the easier to recover the AC coupled signal but the higher the vulnerability to low frequency noise and baseline random walks that can have a very negative effect on energy resolution computation in long signals. A value of $R1=1600 \Omega$ has been chosen which gives a $f_{cutoff} = 10$ kHz. This should attenuate most of the common noises related to electrical engines and other industrial environment elements. Higher f_{cutoff} frequencies would provide a better filtering effect but also would reduce SNR due to the loss in signal amplitude in AC coupled signals.

Noise has been one of the most important specifications, carefully studied from the beginning in order to enhance energy resolution results. The active components in the FEE have been chosen mainly relying on their noise specs. The bandwidth of the FEE (3 MHz) has been chosen to make it work as a shaping filter stretching the time length of the single photo-electron (SPE) response. This last aims at improving the sampling operation carried out at the DAQ level due to its sampling frequency limit. However a rise in SPE length introduces an amplitude loss which must be compensated to keep a reasonable signal to noise ratio. This requires a trade-off between SPE length and filter gain.

A simplified version of the FEE is shown in figure 12. A pseudo-differential transmission has been chosen in order to reduce coupled noise which is expected to be high, since the distance between the FEE rack and the vessel is about 12 m. The AC coupled transmission enables the injection of the high voltage supply to the PMTs through the same signal cable. Assuming C2 AC coupling capacitor has a self resonant frequency (SRF) higher than the maximum estimated bandwidth of the FEE, the line termination (120Ω) will be implemented at Zin. This design choice also allows to terminate the common mode signal that travels along the transmission line and is expected to be quite high since a non-fully-differential transmission is being used. The common mode termination is implemented at the amplifier input (π type

termination with RA and RB).

Mirror capacitor C1 acts as base stabilizers in order to further enhance linearity in the PMT, so they should have a value similar to the PMT base capacitors.

3.4. Noise Measurements

In order to verify that the design specifications are met, noise measurements have been carried out both at testbench and at LSC NEXT installation. The results are shown in table 1.

Noise specs have been fulfilled with a worst case total noise of 0.8 LSB. The theoretically computed noise of the FEE was 0.35 LSB without power supply contribution. The indirectly measured FEE noise contribution is 0.36 LSB which is really close to specifications. Since the FEE is quite lower than the DAQ system contribution the design has accomplished its main goal. An improvement in noise specs probably would require a new DAQ system design.

3.5. Front-end electronics model for simulation

Once the design has been validated through real measurements it is important to build a simulation model which can help in the development of other parts of the project. This time the model has a high level of abstraction in order to be easily integrated with the software analysis modules, Python language with help of Numpy-Scipy libraries. The model comprises two different elements: the low frequency range which has already been developed (eq. ??) plus a fourth order low pass filter (due to the required shaping) with the right gain factor. The model response has been checked against SPICE simulations of the implemented FEE (figure 10).

Noise generation is introduced in the system to resemble the noise behavior of the real system, taking into account the filtering effect of every part. This is to say that for instance, the input equivalent noise of the FEE has been increased to simulate the observed effect given the 3 MHz bandwidth. The noise equivalent model of the FEE is shown on

figure 13 as well as the noise equations relative to the different noise contributions:

$$GAIN = FEE_{GAIN} \cdot DAQ_{GAIN} \quad (4)$$

$$vo_{Tn}^2 = v_{DAQn}^2(out) + v_{F+Pn}^2(out) \quad (5)$$

$$vo_{Tn}^2 = \int_0^{BW=3MHz} v_{F+Pn}^2 \cdot |G.H(jw)|^2 + \int_0^{BW=20MHz} v_{DAQn}^2 \cdot |DAQ_G.H(jw)|^2 \quad (6)$$

$$vo_{Tn(rms)} = \sqrt{vo_{Tn}^2} = 0.76LSB_{rms} \quad (7)$$

Where total Gain is the FEE gain multiplied by acquisition system gain. Moreover, the total noise (vo_{Tn}^2) is the DAQ out noise ($v_{DAQn}^2(out)$) plus the noise of the FEE and the PMT base ($v_{F+Pn}^2(out)$).

3.6. Digital Baseline Restoration procedure

The design trade-off chosen for this solution allowed a more relaxed FEE design, less prone to low frequency issues and less noisy in general relying on a Digital Signal Postprocessing (DSP) to recover the baseline distortion introduced by the AC coupling capacitor. The DSP algorithm is based on the implementation of a inverse function of a first order high pass filter (HPF). The impulse response of this inverse function has a structure composed of a delta in the origin plus a step function whose amplitude equals the value of $\frac{1}{\tau}$ where τ is $(R_1 + Z_{in}) \cdot C$ (eq. 10). This means that the convolution operation can be carried out using just an accumulator and a multiplier instead of a FIR filter.

$$HPF^{-1}(s) = 1 + \frac{1}{\tau \cdot s} \quad (9)$$

$$HPF^{-1}(t) = \delta(t) + \frac{1}{\tau} \int_0^t dt \quad (10)$$

An interesting advantage of this algorithm is that it doesn't have to work continuously, it only has to be activated when a pulse is detected and can be switched off when the pulse ends. This means that

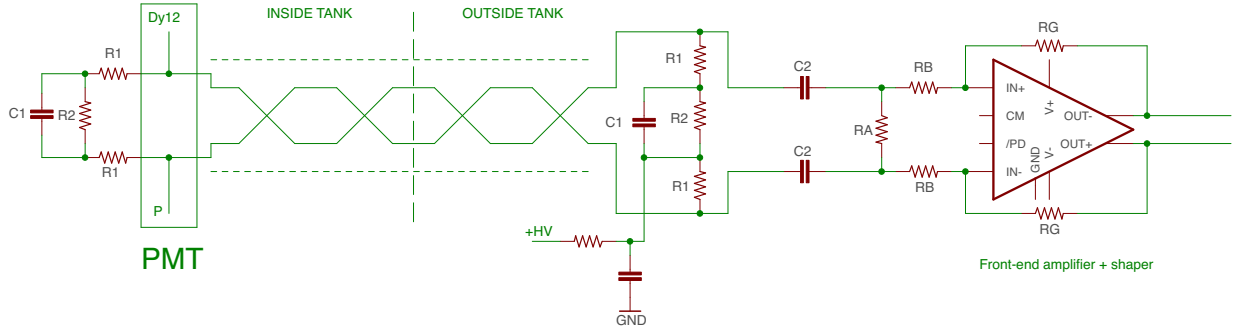


Figure 12: Simplified FEE Scheme

Table 1: Noise Measurements (in LSB_{rms})

		IFIC Laboratory	LSC NEXT
Direct Measurement	DAQ Sys.	0.64	0.66
	FEE + ATCA	0.75	0.75
	FEE + ATCA + PMT	0.76	0.8
Indirect Measurement	FEE	0.39	0.36
	PMT	0.12	0.28

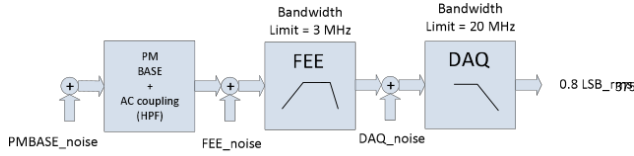


Figure 13: Noise generation scheme

an important amount of low frequency noise filtered by the AC coupling capacitor will not be restored since it is slower than the pulse length.

However, the low frequency zero introduced by the PMT base interaction adds a low amount of DC to the theoretically AC coupled output signal of the FEE. In order to nullify this effect a high pass filter (cleaning filter) with a cutoff frequency equal to the frequency of this zero is introduced previous to the Digital BaseLine Restoration (DBLR) algorithm. This completely cancels the DC effect so that the reconstructed signal shows no baseline shift at the end.

Since the BLR algorithm uses an accumulator, it

might be sensitive to noise and its effects must be studied not only as simple noise equivalent but also taking into account the effect of different frequency components. In case a non zero mean noise appears, the accumulator might get saturated. Typically the accumulator should end the deconvolution process in an empty state, however, low frequency components of the noise makes a small residue remain in the accumulator at the end. Due to finite sampling of the signals residue is not always random. For instance in a burst of short signals (photoelectrons) this residue tends to be positive because the pulses have a higher positive lobe. As a consequence the accumulator starts to rise without limit introducing a baseline shift in the output signal.

This novel DBLR algorithm introduces a control based on a smoothing function to deplete the residue remaining in the accumulator after a pulse reconstruction. The algorithm flowchart is shown in figure 14. In this algorithm the reconstruction process is started independently from the pulse start, and can be working indefinitely. The control relies on the accumulator operations that can be

Update or Discharge. When the DAQ signal rises above a threshold or the accumulator value is above another threshold (which is the condition for an active pulse) the accumulator is updated as in the original algorithm. However, when none of those conditions are met, which means that there is no active signal pulse, the accumulator is forced to a controlled discharge state. This discharge operation is carried out following a smooth curve so that the reconstructed signal shows no jumps or discontinuities.

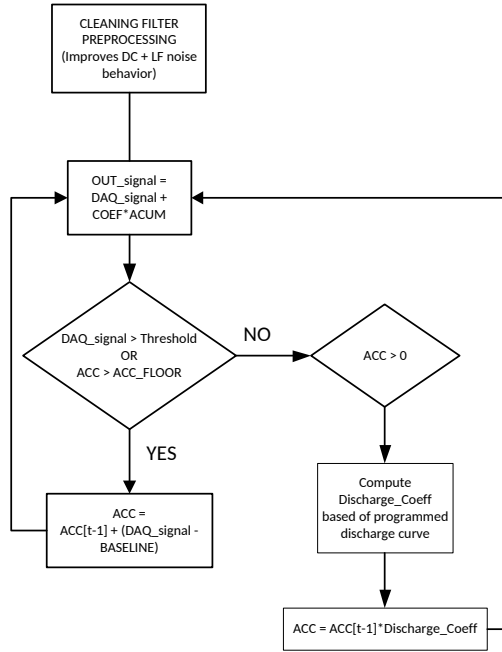


Figure 14: Accumulator based BLR

4. Data acquisition system implementation

In the NEXT experiment Data Acquisition System (DAQ), FPGA-based DAQ modules work in free-running mode, storing data continuously in a circular buffer, while an DAQ Trigger module processes trigger candidates received, generating a trigger accept signal that causes data to be sent to a PC farm [7]. Trigger candidates are generated for each PMT channel in the DAQ Data modules, since each PMTs channel is able to sense the primary and/or the secondary scintillation light produced in the chamber. The trigger candidates' generation is based on the early energy estimation of the events,

which requires at the same time a stable baseline [8]. As a consequence digital baseline restoration must be implemented online.

A similar version of the DBLR algorithm, introduced in subsection 3.6 and shown on figure 14 has been implemented. This DBLR block is activated whenever the input signal rises above a threshold thus producing an output signal with its baseline completely restored. The threshold is defined using signal baseline as a reference which requires a precise on-line baseline computation mechanism. A moving average filter has been used in this implementation. In order to avoid baseline shifts due to residues remaining in the accumulator, and further simplify the logic and use of FPGA resources in the DAQ and trigger modules, the control mechanism makes use of a simple linear smoothing function. As in the original algorithm, in case the accumulator is not completely empty when the reconstruction process ends, it must be automatically flushed.

The DBLR algorithm has been implemented in a Xilinx Virtex-6 FPGA (XC6VLX240T-1ff1156). There is a DBLR block per channel (12 PMT channels per ATCA-FEC module), and a preceding cleaning filter, both configurable. The implemented algorithm and the cleaning filter have been implemented in a 42-bit fixed point format (Q11.30). The format has been selected as a trade-off between algorithm stability and physical resources used.

5. Conclusion

Finally PMT base was designed and fabricated with the balance between the best possible response and radiopurity. After all the materials involved in the base were screened, we conclude that the level of radiopurity is good for us. This way we accomplish the radiopurity requirements as well as the electronics requirements.

Regarding front-end electronics, we simulated, designed, manufactured, mounted, tested and obtained the results that we expected. Once the electronics results were validated as good, we proceeded to build a simulation model. After that,

we started with the digital baseline restoration process.

The digital baseline reconstruction approach has been designed to reduce front-end electronics complexity thus improving its performance in terms of noise and linearity. Therefore the baseline recovery operation is computed in the digital domain where signal to noise ratio gets hardly affected.

Excellent results have been achieved in terms of noise and linearity with acceptable radiopurity levels. Figure 16 shows linearity measurements for the whole front-end including PMT (with its base), FEE and acquisition system. A set of light pulses with constant amplitude and variable length were used.

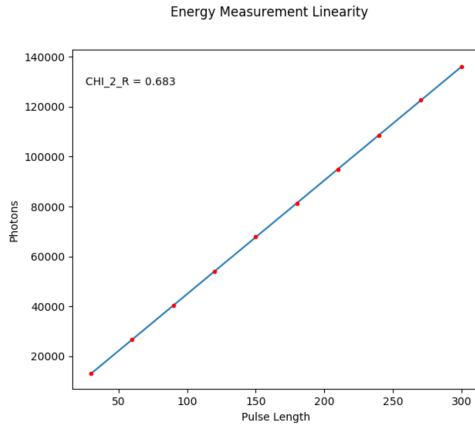
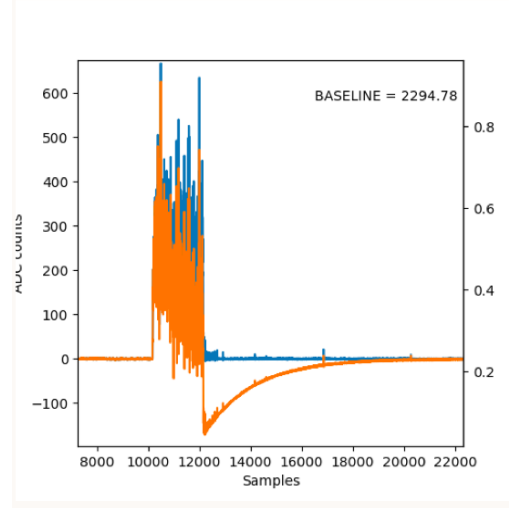


Figure 15: Linearity of the NEW base = 0.38% (140kpe)

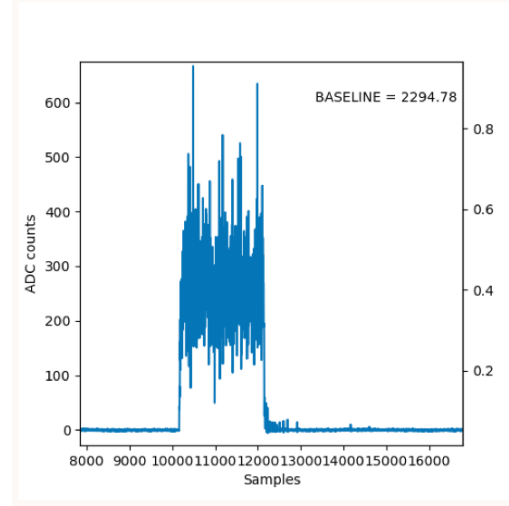
Figure 17 shows a real PMT signal with AC coupling effects (a) and the resulting signal after DBLR has been applied (b)

6. Acknowledgments

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(a) Blue - Real input signal; Orange - FEE output signal



(b) Digital baseline reconstruction applied

Figure 16: Signal of 50us pulse. 25865 pe. Noise 0.74 LSB

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