Student's Reg. No.: .....

**JECRC UNIVERSITY**
**End Term Examination May/June 2024**
**IV Semester B. Tech. (CSE)**
**Computer Organization and Design (BCO009A)**
**Duration: 3 Hours** **Marks: 100**

1. All questions are compulsory.
2. Programmable calculator is not permitted.
3. Draw figures wherever necessary.

CO1: To understand the basic structure and operation of digital computer.
CO2: To study the design of arithmetic and logic unit and implementation of fixed point and floating-point arithmetic operations.
CO3: To study the two types of control unit techniques and the concept of pipelining.
CO4: To study the hierarchical memory system including cache memories and virtual memory.
CO5: To study the different ways of communicating with I/O devices and standard I/O interfaces.

## Section A

**Answer the following questions.** **(2x5=10marks)**

1. [CO1] What is Half Subtractor? Give its Truth table.
2. [CO2] What are Canonical and Standard forms of Boolean functions?
3. [CO3] Difference between fixed point and floating point?
4. [CO4] The sign magnitude representation of -9
5. [CO5] Explain basic concept of **BUS control?**

## Section B

***Answer the following questions.*** **(7x5=35marks)**

1. [CO1] Why is memory hierarchy maintained in a computer system?
2. [CO2] Explain difference between static and dynamic memory?
3. [CO3] Differentiate between RISC versus CISC architecture?
4. [CO4] Differentiate between Static RAM and Dynamic RAM.
5. [CO5] Explain Polled and Interrupt-driven I/O with suitable structure.

## Section C

**Answer the following questions.** **(11x5=55marks)**

[CO1] An 8-bit register contains the binary value 10101010. What is the register value after arithmetic shift right? Starting from an initial number 10101010, determine the register value after an arithmetic shift left, and state whether there is an overflow.

1. [CO2] Explain Instruction Cycle and its steps also Explain the flowchart of Instruction Cycle.
2. [CO3] Solve (A+B*C)/(D+E-F) in 3,2,1 and 0 type of inspection format.
3. [CO4] A two –way set associative cache memory uses block of 4 words. The cache can accommodate a total o 2048 words from main memory. The main memory size is 128k* 32.
   (i) Formulate all pertinent information required to construct the cache memory.
   (ii) What is the size of cache memory and number of address bits required to define a block of main memory?
5. [CO5] Explain the following in detail:
   a. DMA Controller b. Hand Shaking c. DMA data trans