Mayank Aggarwal

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Education		
Bachelor of Technology, Electrical Engineering Indian Institute of Technology Patna	2012 - 2016	9.19/10 (Over 6 Semesters)
Higher Secondary (School) Certificate, C.B.S.E DN Model Sen. Sec. School, Punjab	2012	92%
Secondary School Certificate, Punjab School Education Board Navyug Shishu Mandir High School, Punjab	2010	88%

Internships / Work Experience

Tata Motors Ltd., Jamshedpur

(May,2015-June,2015)

Mentor: Mr. Santu Hore (Manager, Power Supply)

Title: To propose an efficient scheme for load balancing of power transformers and to analyze their efficiency.

- In first phase, analyzation of power distribution system was done and SLDs were generated for various substations.
- In second phase, load data collection of various transformers was done by regular visits to MRS and other substations.
- In third phase, out of multiple schemes possible by shifting loads from one transformer to another, our team analysed load curves of the cases possible and proposed the most efficient scheme and recommended modifications to be done in the existing structure.

North Eastern Space Applications Centre, Shillong

(May,2014 - June,2014)

Mentor: Mr. Anjan Debnath (Scientist & Engineer at ISRO)

• Introduced to general trends of satellite communication with special reference to GPS navigation technology. An exposure to atmospheric effects in SATCOM and IRNSS (Indian Regional Navigation Satellite System).

Projects

OFDM for High Rate Underwater Acoustic Communications

(Jan, 2015 -Mar, 2015)

Mentor: Dr. Preetam Kumar (Assistant Professor, Department Of Electrical Engineering, IIT Patna)

- Successfully realized MATLAB coding for OFDM Modulation using BPSK, QPSK & DQPSK, compared the bit error rate for both of them and analysed the simulation results with AWGN channel for varying SNRs.
- Conducted experiments for underwater and air medium using acoustic channel transmission using hydrophone,
 Transmitter and MATLAB package and concluded that DQPSK gives best result with minimum multipath interference.

Shape based Human activity recognition using ICA

(Feb, 2015 - Mar, 2015)

Mentor: Dr. Mahesh H Kolekar (Assistant Professor, Department Of Electrical Engineering, IIT Patna)

• Realized MATLAB code for Video Image Pre-processing to subtract out the background from recent frame of interest.

Based on pixel-intensity plots of various frames, a threshold intensity was set to check out the region of interest in frames.

VLSI design mini Projects

(Sep, 2014)

Mentor: Dr. Kailash Chandra Ray (Assistant Professor, Department Of Electrical Engineering, IIT Patna)

- FPGA Implementation of digital mean and median filters using behavioural and structural approach in Verilog HDL. Software tool used was Xilinx ISE and Bubble sort algorithm was used.
- FPGA implementation of scrolling text using "Hirose Connector with Display".

Arduino mini Projects

(Jan, 2014)

- Fabricated 7x14 LED matrix alongside a driver so as to realize display for patterns especially scrolling texts using Arduino.
- Built an autonomous Line Follower robot with accidental control technique that can follow the motion of the source robot without ever colliding with the source robot.

Technical Skills

Programming languages : C , Java

- **Design tools & Mathematical Processing**: Verilog HDL, Xilinx ISE , Matlab
- Microcontrollers & Microprocessors: Arduino micro-controller. microprocessor 8085. PIC18F

Extra Curricular Activities

- Performed Punjabi folk dance 'Bhangra' on Diwali Fest Reverberance' 13 IIT Patna.
- Organized a Circuit Design event in IIT Patna in which participants have to display some sequence of characters on led matrix.