Nishant Kumar

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EDUCATION

INDIAN INSTITUTE OF TECHNOLOGY, PATNA
Btech in Electrical Engineering
Expected May 2016
CPI: 8.09/10 (over 6 semesters)

SATYAM INTERNATIONAL SCHOOL
Grad. March 2011|Patna
Intermediate (CBSE)
aggregate: 77.4 %

D.A.V. PUBLIC SCHOOL
Grad. March 2009 |Patna
Metriculation (CBSE)
aggregate: 88.4 %

COURSEWORK

CORE COURSES
•VLSI Design
•Embedded System
•Digital Electronics
•Analog Electronics
•Digital Signal Processing
•Signals Systems
•Control System
•Electronics Instrumentation

MATH COURSES
•Probability Random Processes
•ODE and PDE
•Linear Algebra
•Complex Analysis
•Mathematical Methods
•Numerical Methods

SKILLS

PROGRAMMING
•C •PIC18 Assembly Language
• MATLAB •Java •Mathematica

DESIGN TOOLS
•Verilog HDL• Simulink•Pyxis schematic•Design Vision
•Eagle PCB design

PROJECTS

SEQUENTIAL QUADRATIC PROGRAMMING
2015-2016|Final Year BTech Project|Project-I(EE498) IIT PATNA
•The algorithm aims to solve nonlinearly constrained optimization problems.
•The final result of the project will be to apply the optimization algorithm to power system statements.

SOLAR CELL BATTERY CHARGER USING MAXIMUM POWER POINT TRACKING SCHEME
Spring 2015 |Academic project |Design Lab (EE304) IIT Patna
•The project aimed to design a battery charging system for charging rechargeable cellphone batteries at maximum efficiency with input as the solar power.
•Integrated chip LM2576 was used to maintain the constant current rating of the rechargeable battery.
•The final design was portable and was able to charge the Lumia cellphone battery successfully.

PCB DESIGNED BPSK MODULATION AND DEMODULATION
Nov2014–Communication System Lab, IIT Patna
•Designed binary phase shift keying modulation and demodulation circuit with the help of DipTrace software and successfully implemented on a full custom laboratory made printed circuit board.

WORK ON EMBEDDED SYSTEM AND VLSI DOMAIN
VLSI and Embedded Systems Lab, IIT Patna
•Worked on led matrix pattern generation, control of stepper motor and DC motor using PIC18f4550 microcontroller kit.
•Implemented an algorithm using Verilog HDL for scrolling roll number on a six set of seven segment displays, interfaced with Spartan 3E FPGA kit and further extended it on LCD display .
•Implemented the algorithm of mean and median filter on Spartan 3E FPGA kit.

POSITION OF RESPONSIBILITY

•Selected for the mentoring of RTDC project (Toxin detecting device in drinking water) in 2014
•Event organiser at Anwesha in 2014.
•Opted as a team member of security measure in Anwesha (IIT Patna techno-cultural fest) in 2013.

EXTRA-CURRICULAR ACTIVITIES

•Active member of Rural Technonlogy Development Club (RTDC).
•Mentored a project under RTDC that aims to conceptualize and successfully develop a prototype which will detect toxins in drinking water. This prototype will be designed to be low-cost and portable.
•Joined a survey team of Rural Technology Development Club for the study of rural background related technical problems.
•Have a hobby of playing basketball and chess.