Sayan Chakraborty

Resume

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Internship Experience

May 2015 - July 2015

HPA Team, Texas Instruments(India) Pvt. Ltd.

Estimation of DAC nonlinearity in multi-bit delta-sigma ADC

This project includes modelling of the delta-sigma ADC system, estimation of DAC errors based on proposed algorithm and testing the efficiency of the algorithm based on correction method proposed.Initial modelling was done on Matlab software and post simulation implementation is done on FPGA using VHDL and final correction has been done on Hobbes software using perl script.

December 2014

Performance Analysis Lab,IISc Bangalore

Application of Saddle Point Analysis in approximating Bit Error Rate

Simulated the probabilities of False Alarm in Sequential Probability Ratio Test, Random Walk Test etc. and compared these with those obtained analytically from saddle point approximations.

May 2013 – July 2013

Physics Lab, IIT Patna

Analysis of LCR circuit

Analysis of LCR circuit by explaining the deviation of its characteristics from theoretically predicted value by incorporating different parasitic models .

Relevant Courseworks

Basic Electrical Circuits(AA), Digital Circuits and Microprocessors(AA), Analog Integrated Circuits(AA), Principles of Communication(AA),Electrical Machines(AA),Probability theory(AA),Signal Systems and Networks(AB), Digital Signal Processing(AB), Object Oriented Programming and Data Structure(AB), Power Systems(AB),VLSI(BB),Embedded Systems(BB), Power Electronics(Ongoing), Wireless Integrated Circuits(Ongoing), Advanced Digital Communication(Ongoing)

Minor Projects

2014

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PCB designing of BPSK Transceiver

Designed a PCB Transceiver Model for BPSK modulation in communication lab,IIT Patna .

2015

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Data Transmission through Underwater Acoustic Channel and Video Transmission in Air using SDR

modulation schemes used were BPSK,QPSK,OQPSK and their comparative analysis was carried out and for video transmission 64QAM OFDM Nutaq picoSDR was used.

Education

2012 – Present **Indian Institute of Technology, Patna**
Btech.in Electrical Engineering [cpi: 9.21/10(upto 6th semester with departmental 2nd rank)]

2010–2012 **UttarparaGovt.HighSchool**
10+2 level [secured 88 percent marks]

2004–2010 **Baranagore R.K.M High School**
+10 level [secured 90.65 percent marks]

Technical skills

Programming: C, Java, Verilog HDL,VHDL,Perl, Assembly Language for microprocessor intel 8085, Assembly Language for PIC18f4550

Software: MATLAB,LaTeX, Mathematica, Microcal Origin, Xilinx ISE, Pyxis Schematic, Design Vision, Hobbes

Awards and Achievements

- Champion at Circuit Design Competition, Celesta12 Tech.fest of IIT Patna)
- Ranked 4496 among over 500k students allover India in IITJEE exam
- Ranked 2678 in AIEEE exam out of almost 500k students
- Elected as one of the Coordinators of Sparkonics Club(club for Electrical Engineers)
- Awarded certificate of appreciation for successfully presenting poster on Texas Instruments (India) Intern day.

ExtraCurricular Activities

Singing: Frontman at college band '8th Note'

Painting: Good skills of drawing

Social Activities: Prepares video lectures for under privileged rural students under Rural Technology Development Club, IIT Patna