Madhav Kumar Singh

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EDUCATION

IIT PATNA
B.Tech in Electrical Engineering
Graduating in May 2016
Cum. GPA : 8.5

SRI CHAITANYA VIDYANIKETAN
Grad. March 2012 | Vishakhapatnam
Intermediate(CBSE)
Percentage: 88.2%

ARMY PUBLIC SCHOOL
Grad. March 2010 | Ranchi
Metriculation(CBSE)
CGPA: 9.4

LINKS

LinkedIn:// **madhav-kumar-singh**
Gmail:// **madhavkrsingh15**
ResearchGate:// **Madhav-Singh3**

COURSEWORK

UNDERGRADUATE
Introduction to VLSI Design
Embedded System
Wireless Communication Integrated Circuits
Principal of Communication
Digital Circuits and Microprocessors
Signal and System
Digital Signal Processing
Analog Integrated Circuits
Control Systems
Electronic Instrumentation
Introduction to Numerical Methods
Infotainment

ONLINE COURSE
VLSI CAD : Logic to Layout

SKILLS

PROGRAMMING
Java • C • Matlab • LaTeX
Embedded C • Mathematica

DESIGN TOOLS
Verilog HDL • Pspice • Simulink • Virtuoso • Design Compiler • ModelSim • Catapult C

ASSEMBLY LANGUAGE
Intel 8085, PICs

EXPERIENCE

INRIA RENNES | Research Intern
May 2015 - July 2015 | France
Topic: Exploration of accuracy vs. performance through high-level synthesis of hardware accelerators

- From a set of signal and image processing benchmarks specified in floating point we generated different fixed-point specifications for different accuracy constraints and different architectures.
- Performed high-level synthesis and floating-point to fixed-point conversion of a set of applications (benchmarks) to demonstrate the potential of the tools developed in the host team at Inria.
- Proposed new algorithms for resource estimation in ID.Fix infrastructure

PROJECT

DESIGN AND IMPLEMENTATION OF QUADRUPLE FLOATING-POINT CORDIC
May 2014 – July 2014 | IIT Patna

- Proposed a new quadruple floating point CORDIC architecture to meet the demand of present and future dynamic range.
- Design was coded and simulated using Verilog HDL and synthesized using XST tool, targeting a commercially available FPGA device XCVLX110T-IFF1136.
- Application in robotics,image processing and communication systems.
- Paper related to this research is accepted in iNIS 2015.

DESIGN AND DEVELOPMENT OF REAL TIME EMBEDDED SYSTEM FOR TEXT EXTRACTION FROM IMAGE
Jan 2015 - April 2015

- Goal was to recognize and extract text of particular font in a real time image of documents by using a VGA camera.
- Technique used is based on Binarization, Contouring, Segmentation and Freeman chain code to identify the character on the document image.
- The system was implemented on NB3000XN Altium nanoboard interfaced with the PC using Altium designer software.

POSITION OF RESPONSIBILITY

- Co-Founder and Technical Coordinator of Rural Technology Development Club of IIT Patna.
- Coordinator of SPARKONICS(An Electrical and Electronics Club of IIT Patna).
- Event organizer at Anwesha(A Techno-Cultural Fest of IIT Patna) in 2014.
- Event organizer at Celesta(A Techno-Management Fest of IIT Patna) in 2013.

EXTRA-CURRICULAR ACTIVITIES

- Participated in Line Follower event in Anwesha 2k14.
- Participated in Robosoccer event in Anwesha 2k13.
- Surveyed a few villages of Bihar under RTDC, to get to know the technical problem faced by the rural people.
- Served as NCC Cadet for two years in Army Public School.
- Got selected for 2nd round in National Science Olympiad in 2011.