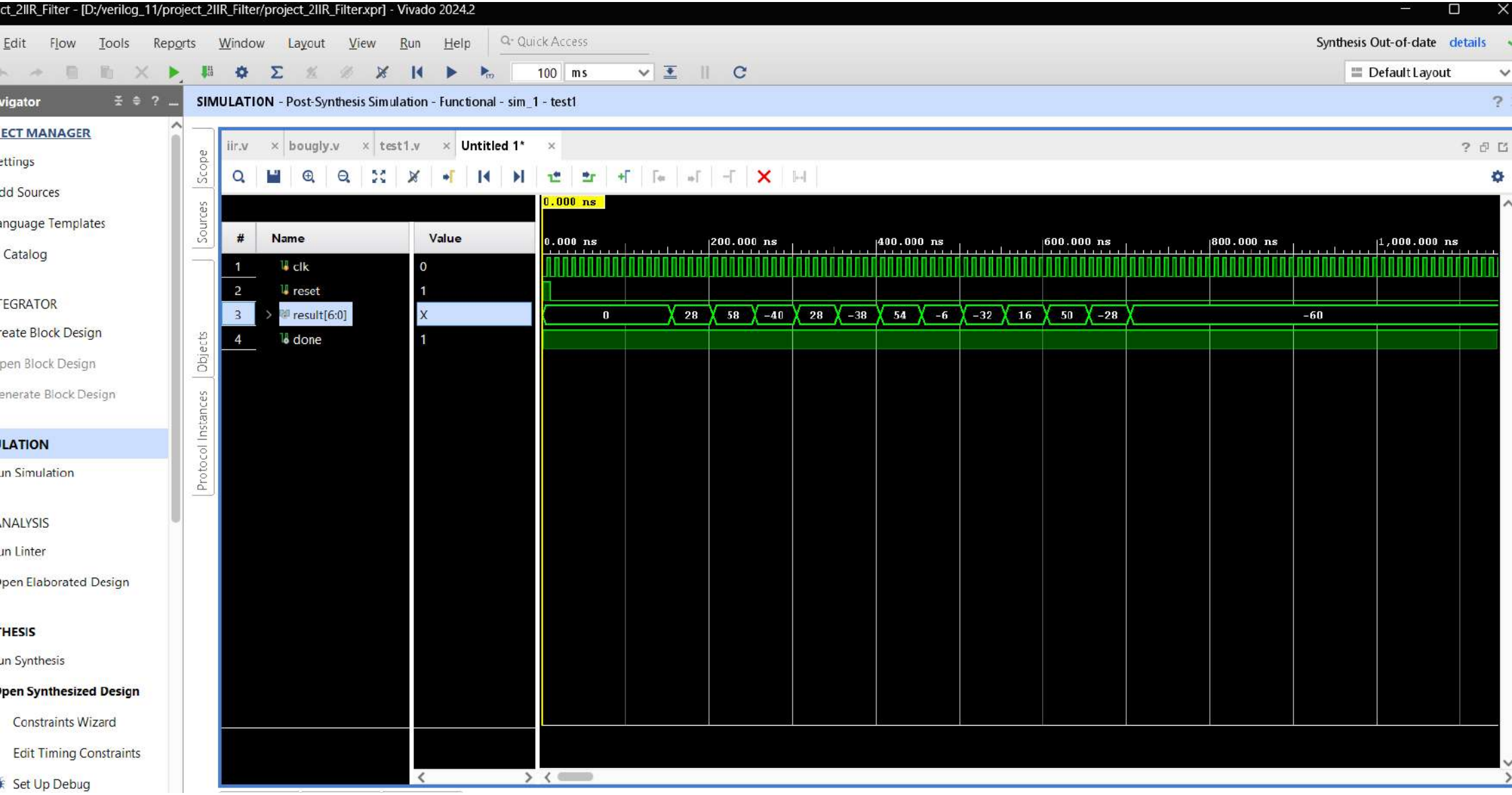
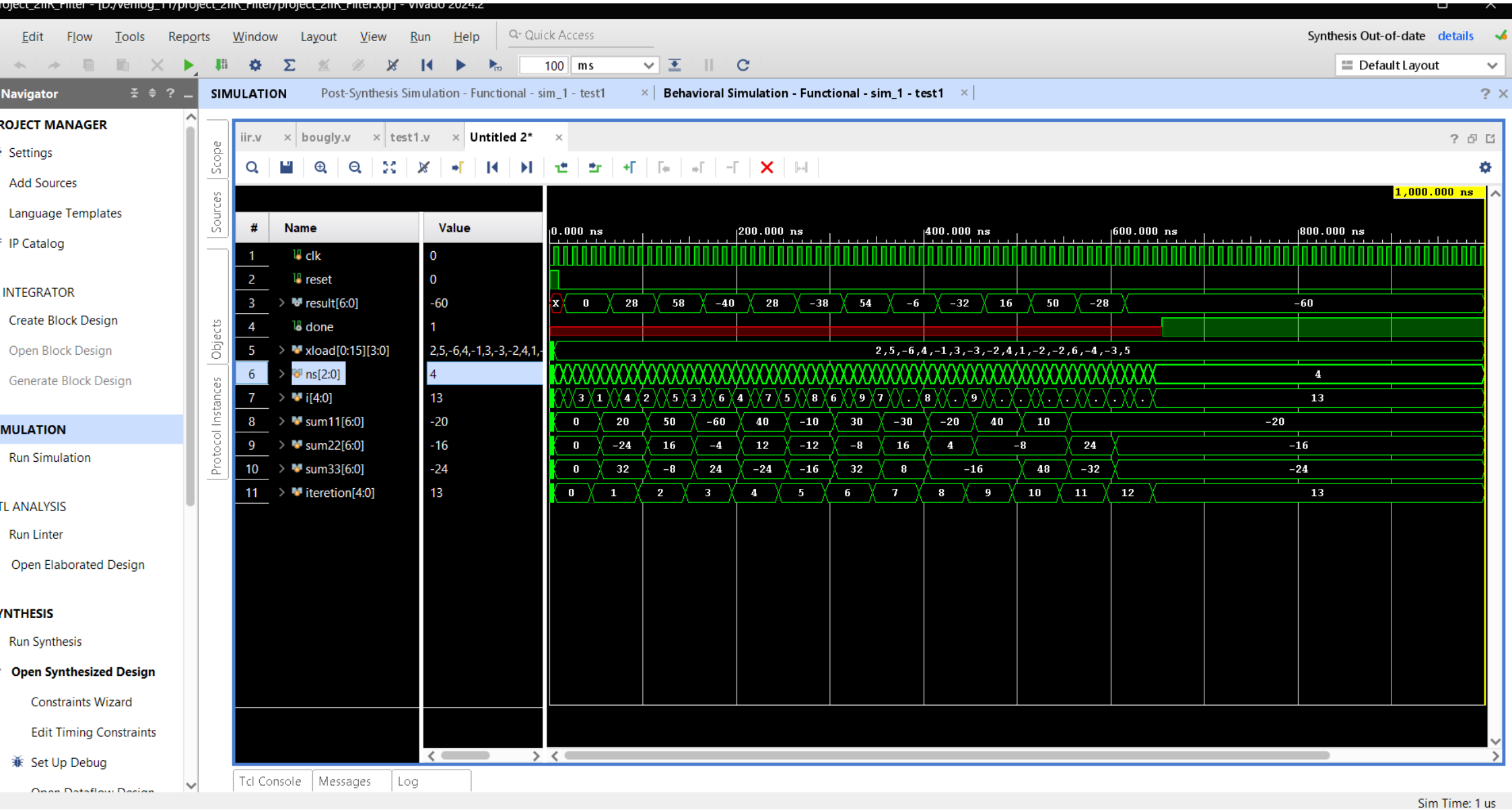

ct_2IIR_Filter - [D:/verilog_11/project_2IIR_Filter/project_2IIR_Filter.xpr] - Vivado 2024.2
Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Synthesis Out-of-date details
100 ms
Default Layout
SIMULATION - Post-Synthesis Simulation - Functional - sim_1 - test1
iir.v
bougly.v
test1.v
Untitled 1*
Scope
Sources
Objects
Protocol Instances
Name Value
1 clk 0
2 reset 1
3 result[6:0] X
4 done 1
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
0 28 58 -40 28 -38 54 -6 -32 16 50 -28 -60
ECT MANAGER
ettings
dd Sources
anguage Templates
Catalog
TEGRATOR
reate Block Design
pen Block Design
enerate Block Design
ULATION
un Simulation
ANALYSIS
un Linter
Open Elaborated Design
THESIS
un Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug


Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Synthesis Out-of-date details
100 ms
Default Layout
Navigator
SIMULATION
Post-Synthesis Simulation - Functional - sim_1 - test1
Behavioral Simulation - Functional - sim_1 - test1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
iir.v
bougly.v
test1.v
Untitled 2*
Scope
Sources
Objects
Protocol Instances
Name Value
1 clk 0
2 reset 0
3 result[6:0] -60
4 done 1
5 xload[0:15][3:0] 2,5,-6,4,-1,3,-3,-2,4,1,-
6 ns[2:0] 4
7 i[4:0] 13
8 sum11[6:0] -20
9 sum22[6:0] -16
10 sum33[6:0] -24
11 iteretion[4:0] 13
1,000.000 ns
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
Tcl Console
Messages
Log
Sim Time: 1 us

project_2IIR_Filter - [D:/verilog_11/project_2IIR_Filter/project_2IIR_Filter.xpr] - Vivado 2024.2

e Edit Flow Tools Reports Window Layout View Help Quick Access Synthesis Out-of-date

Timing Analysis

v Navigator

RTL ANALYSIS
- Run Linter
- Open Elaborated Design

SYNTHESIS
- Run Synthesis
- Open Synthesized Design
  - Constraints Wizard
  - Edit Timing Constraints
  - Set Up Debug
  - Open Dataflow Design
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Utilization
  - Report Power
  - Schematic

IMPLEMENTATION
- Run Implementation
- Open Implemented Design

SYNTHESIZED DESIGN * - xc7a200tisbv484-1L

Tcl Console | Messages | Log | Reports | Design Runs | Power | Timing

Summary

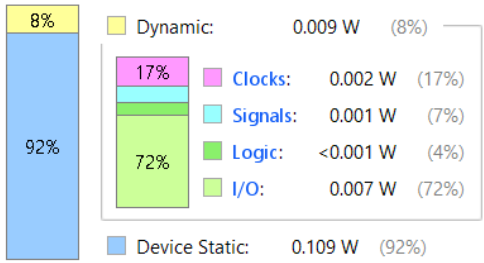
Settings
Summary (0.118 W, Margin: N/A)
Power Supply
Utilization Details
- Hierarchical (0.009 W)
- Clocks (0.002 W)
- Signals (0.001 W)
  - Data (0.001 W)
  - Clock Enable (<0.001 W)
  - Set/Reset (0 W)
- Logic (<0.001 W)
- I/O (0.007 W)

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

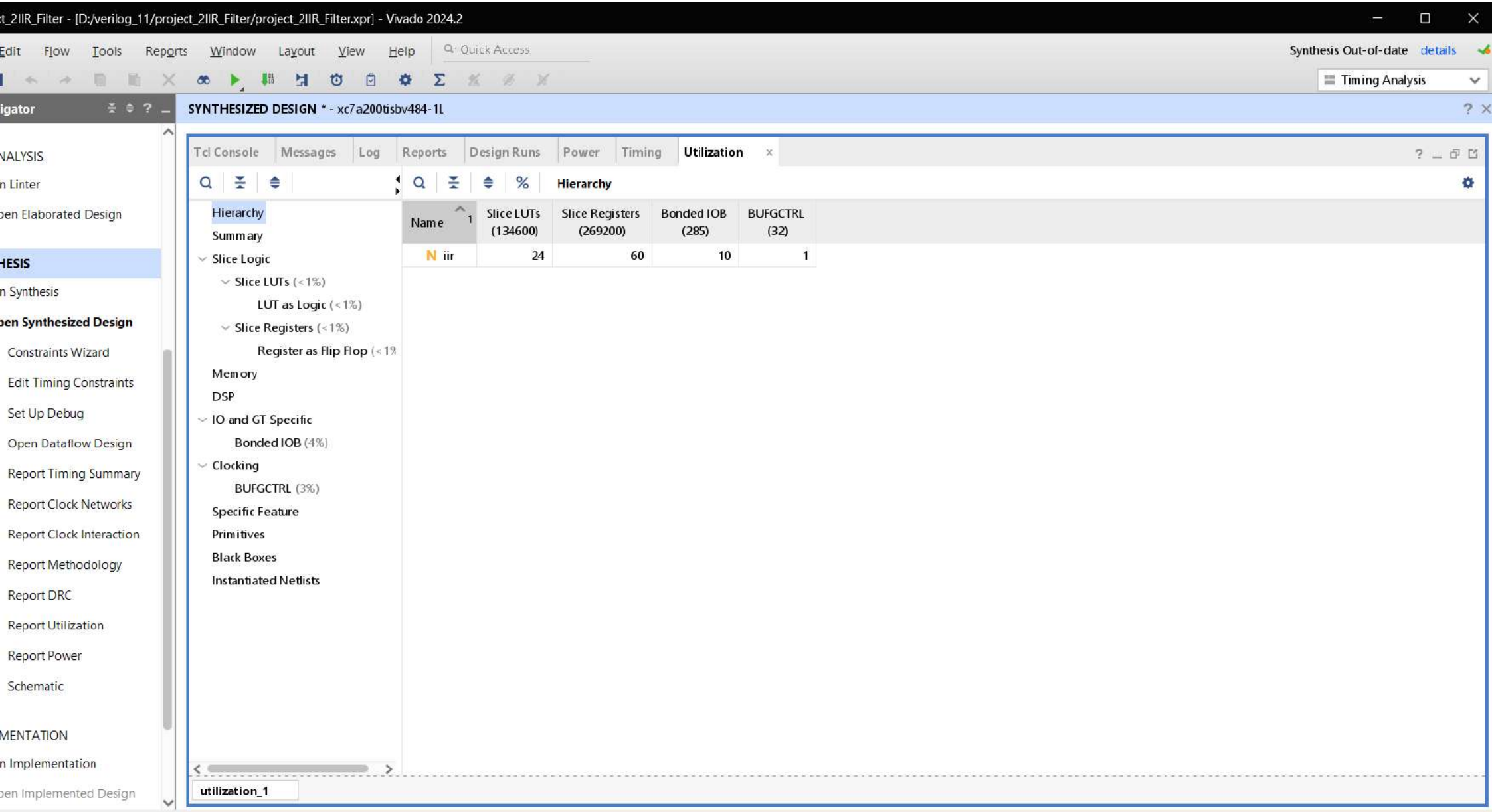
Total On-Chip Power:	**0.118 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.3°C**
Thermal Margin:	74.7°C (28.5 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	2.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

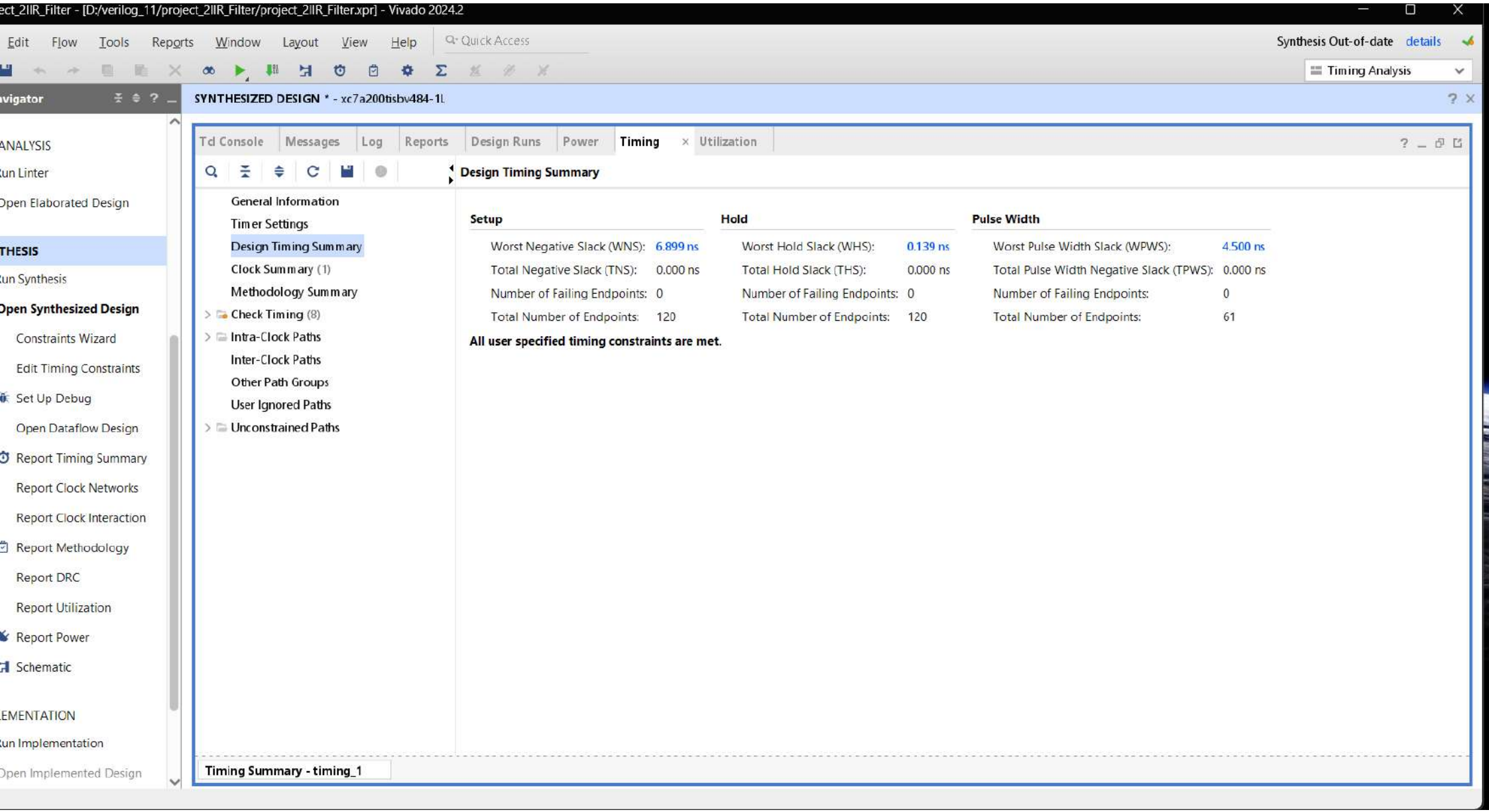
Launch Power Constraint Advisor to find and fix invalid switching activity

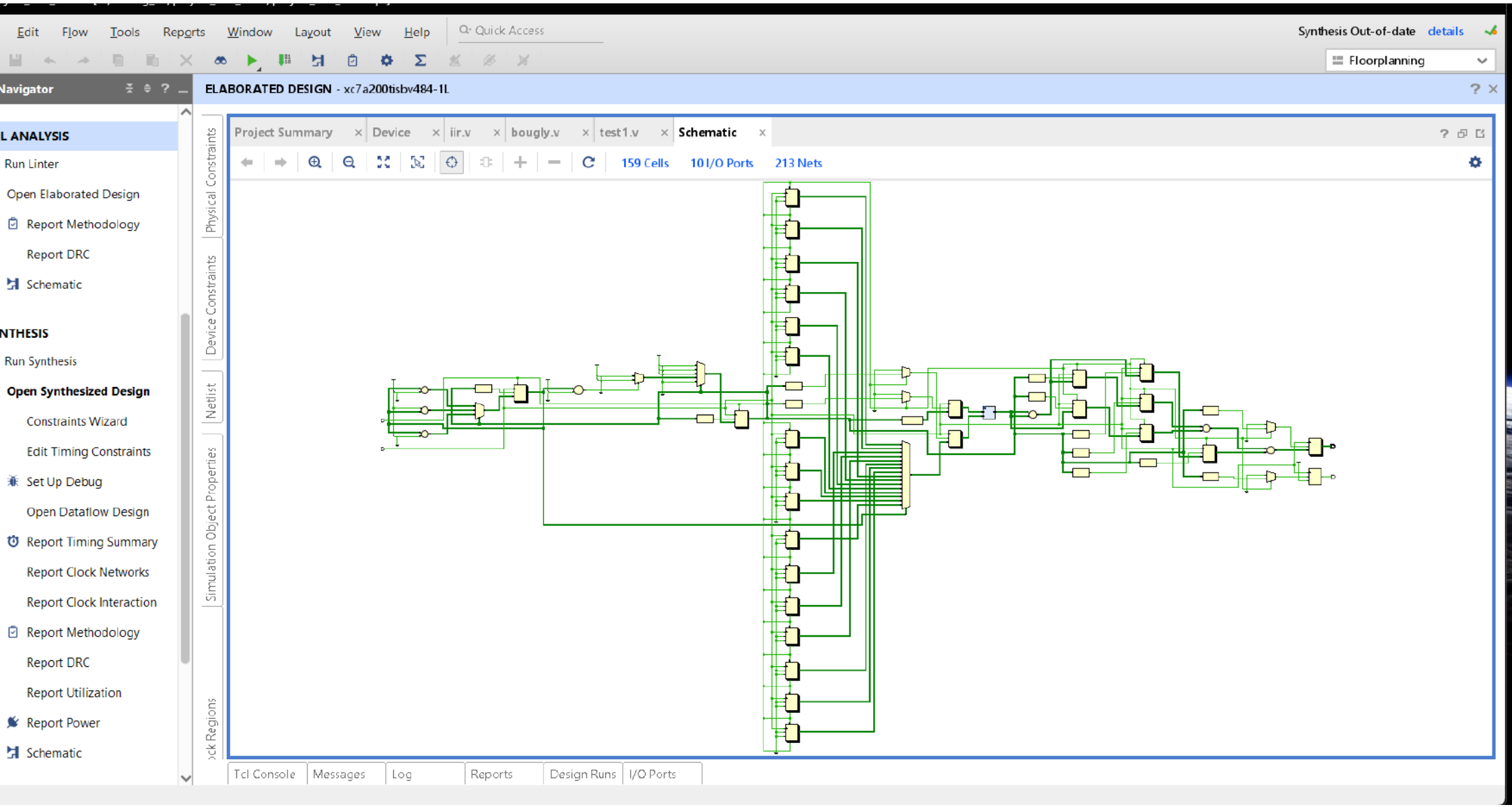
On-Chip Power



power_1


t_2IIR_Filter - [D:/verilog_11/project_2IIR_Filter/project_2IIR_Filter.xpr] - Vivado 2024.2
Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Out-of-date details
Timing Analysis
SYNTHESIZED DESIGN * - xc7a200tisbv484-1L
Tcl Console Messages Log Reports Design Runs Power Timing Utilization
Hierarchy
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Slice Registers (<1%)
Register as Flip Flop (<1%
Memory
DSP
IO and GT Specific
Bonded IOB (4%)
Clocking
BUFGCTRL (3%)
Specific Feature
Primitives
Black Boxes
Instantiated Netlists
Name
Slice LUTs (134600)
Slice Registers (269200)
Bonded IOB (285)
BUFGCTRL (32)
iir
24
60
10
1
utilization_1
NALYSIS
n Linter
pen Elaborated Design
HESIS
n Synthesis
pen Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Open Dataflow Design
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
MENTATION
n Implementation
pen Implemented Design


ect_2IIR_Filter - [D:/verilog_11/project_2IIR_Filter/project_2IIR_Filter.xpr] - Vivado 2024.2
Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Out-of-date details
Timing Analysis
SYNTHESIZED DESIGN * - xc7a200tisbv484-1L
Tcl Console Messages Log Reports Design Runs Power Timing Utilization
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Methodology Summary
Check Timing (8)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
Setup
Worst Negative Slack (WNS): 6.899 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 120
Hold
Worst Hold Slack (WHS): 0.139 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 120
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 61
All user specified timing constraints are met.
Timing Summary - timing_1
ANALYSIS
Run Linter
Open Elaborated Design
THESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Open Dataflow Design
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
LEMENTATION
Run Implementation
Open Implemented Design


Edit
Flow
Tools
Reports
Window
Layout
View
Help
Quick Access
Synthesis Out-of-date
details
Floorplanning
Navigator
ELABORATED DESIGN - xc7a200tisbv484-1L
L ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Schematic
NTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Open Dataflow Design
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
Physical Constraints
Device Constraints
Netlist
Simulation Object Properties
ock Regions
Project Summary
Device
iir.v
bougly.v
test1.v
Schematic
159 Cells
101/O Ports
213 Nets
Tcl Console
Messages
Log
Reports
Design Runs
I/O Ports