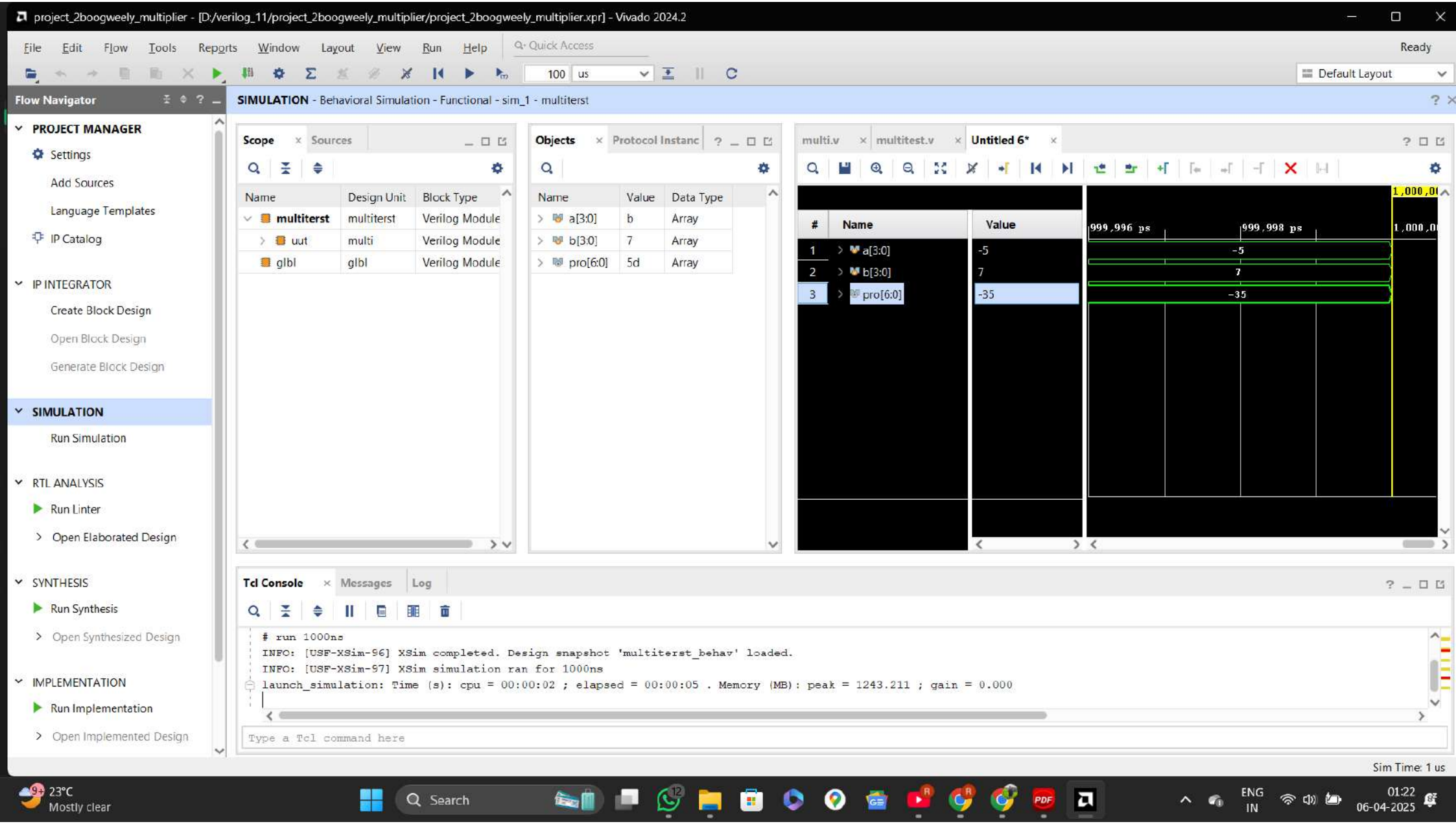
project_2boogweely_multiplier - [D:/verilog_11/project_2boogweely_multiplier/project_2boogweely_multiplier.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
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Add Sources
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IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
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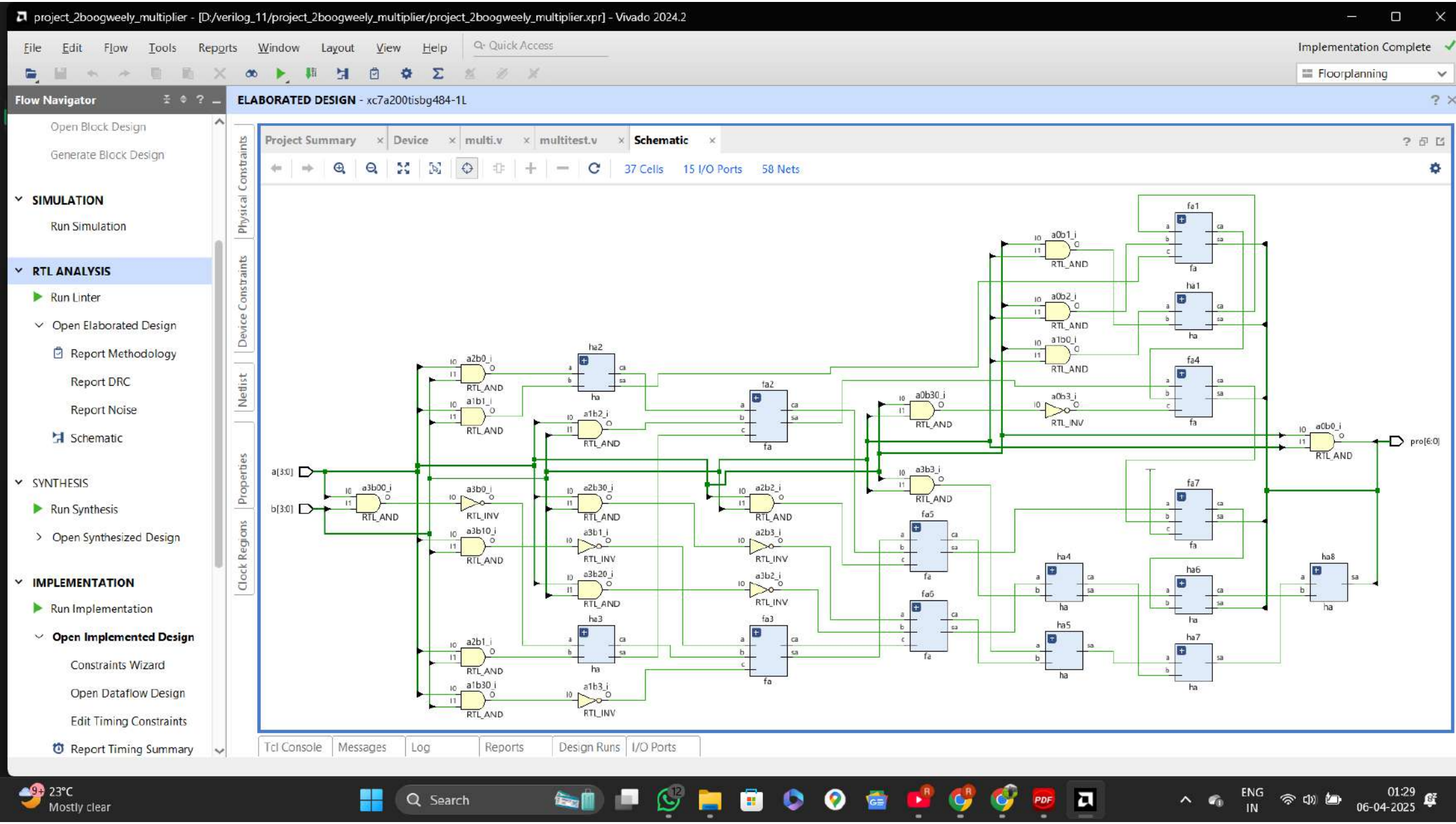
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
SIMULATION - Behavioral Simulation - Functional - sim_1 - multiterst
Scope
Sources
Name
Design Unit
Block Type
multiterst
multiterst
Verilog Module
uut
multi
Verilog Module
glbl
glbl
Verilog Module
Objects
Protocol Instanc
Name
Value
Data Type
a[3:0]
b
Array
b[3:0]
7
Array
pro[6:0]
5d
Array
multi.v
multitest.v
Untitled 6*
#
Name
Value
1
a[3:0]
-5
2
b[3:0]
7
3
pro[6:0]
-35
999,996 ps
999,998 ps
1,000,0
-5
7
-35
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'multiterst_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 . Memory (MB): peak = 1243.211 ; gain = 0.000
Type a Tcl command here
Sim Time: 1 us
23°C
Mostly clear
Search
ENG
IN
01:22
06-04-2025


project_2boogweely_multiplier - [D:/verilog_11/project_2boogweely_multiplier/project_2boogweely_multiplier.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Help
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Floorplanning
Flow Navigator
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Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Open Dataflow Design
Edit Timing Constraints
Report Timing Summary
ELABORATED DESIGN - xc7a200tisbg484-1L
Physical Constraints
Device Constraints
Netlist
Properties
Clock Regions
Project Summary
Device
multi.v
multitest.v
Schematic
37 Cells
15 I/O Ports
58 Nets
a[3:0]
b[3:0]
pro[6:0]
RTL_AND
RTL_INV
ha
fa
Tcl Console
Messages
Log
Reports
Design Runs
I/O Ports
23°C
Mostly clear
Search
ENG
IN
01:29
06-04-2025

project_2boogweely_multiplier - [D:/verilog_11/project_2boogweely_multiplier/project_2boogweely_multiplier.xpr] - Vivado 2024.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

Implementation Complete

I/O Planning

Flow Navigator

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION
- Run Implementation
- Open Implemented Design
  - Constraints Wizard
  - Open Dataflow Design
  - Edit Timing Constraints
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power
  - Schematic

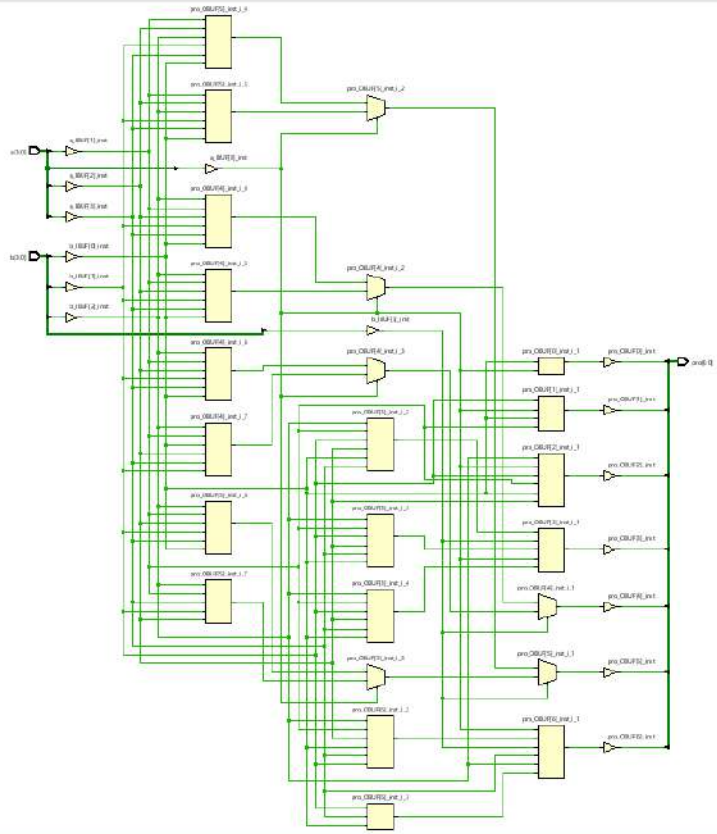
PROGRAM AND DEBUG
- Generate Bitstream
- Open Hardware Manager

IMPLEMENTED DESIGN - xc7a200tisbg484-1L

Sources Netlist Device Constraints Properties Clock Regions

Package Device multi.v multitest.v Schematic Schematic (2)

39 Cells 15 I/O Ports 47 Nets



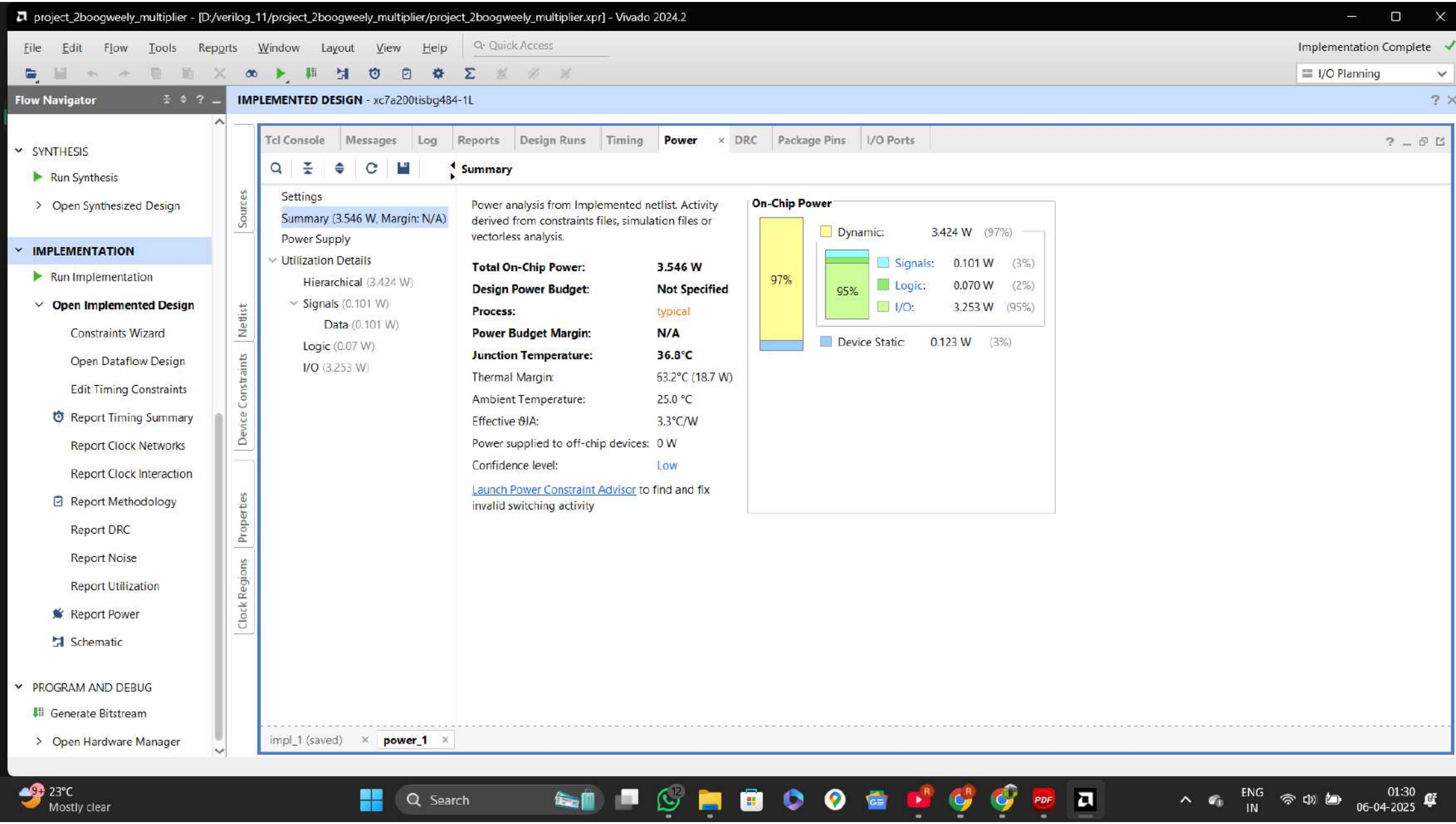
Tcl Console Messages Log Reports Design Runs Timing Power DRC Package Pins I/O Ports

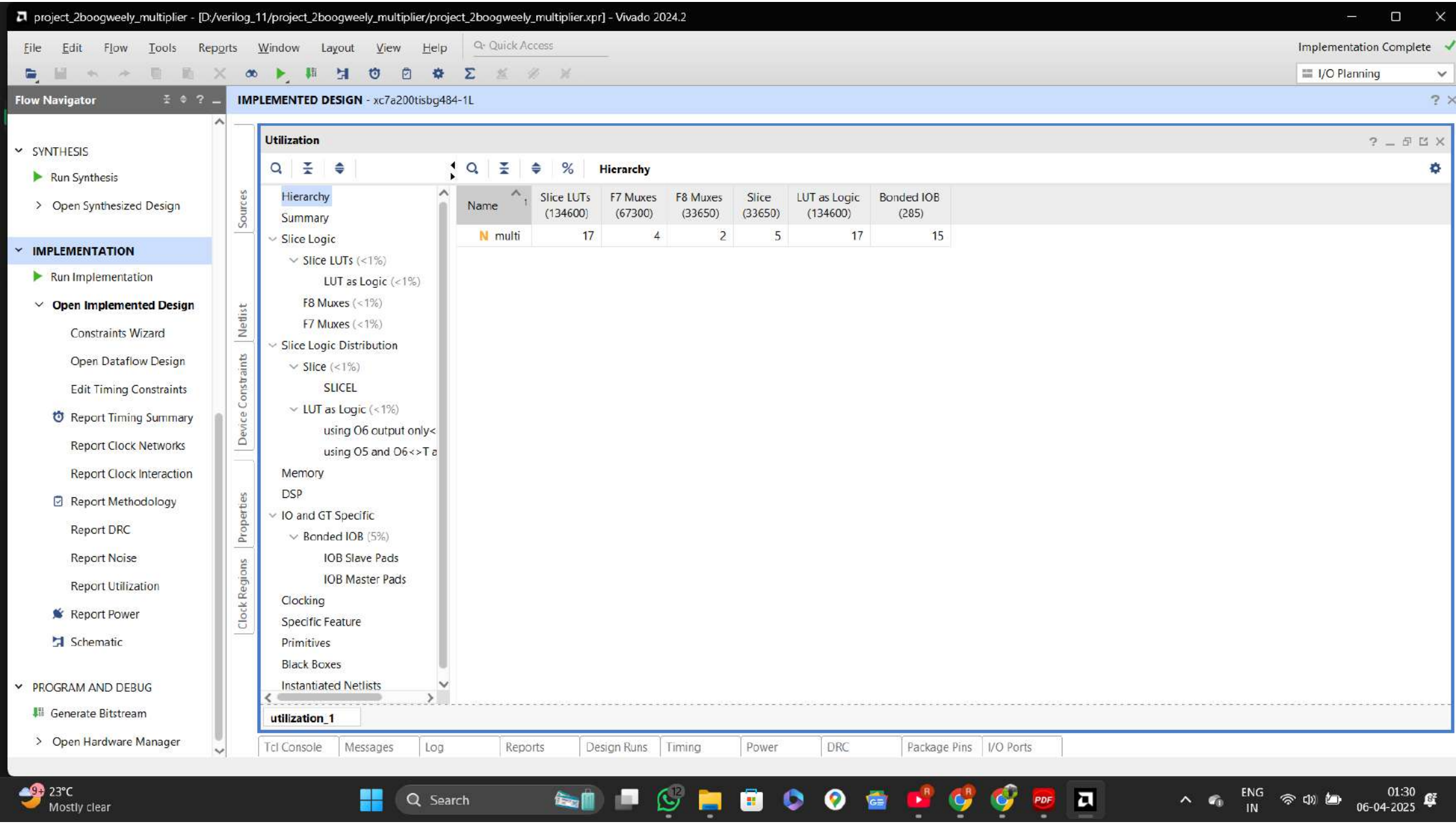
23°C Mostly clear

Search

ENG IN

01:29 06-04-2025


project_2boogweely_multiplier - [D:/verilog_11/project_2boogweely_multiplier/project_2boogweely_multiplier.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
I/O Planning
Flow Navigator
IMPLEMENTED DESIGN - xc7a200tisbg484-1L
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Open Dataflow Design
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Sources
Netlist
Device Constraints
Properties
Clock Regions
Tcl Console Messages Log Reports Design Runs Timing Power DRC Package Pins I/O Ports
Summary
Settings
Summary (3.546 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (3.424 W)
Signals (0.101 W)
Data (0.101 W)
Logic (0.07 W)
I/O (3.253 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 3.546 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 36.8°C
Thermal Margin: 63.2°C (18.7 W)
Ambient Temperature: 25.0 °C
Effective θJA: 3.3°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
97%
Dynamic: 3.424 W (97%)
95%
Signals: 0.101 W (3%)
Logic: 0.070 W (2%)
I/O: 3.253 W (95%)
Device Static: 0.123 W (3%)
impl_1 (saved)
power_1
23°C
Mostly clear
Search
ENG
IN
01:30
06-04-2025


project_2boogweely_multiplier - [D:/verilog_11/project_2boogweely_multiplier/project_2boogweely_multiplier.xpr] - Vivado 2024.2
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Implementation Complete
I/O Planning
Flow Navigator
IMPLEMENTED DESIGN - xc7a200tisbg484-1L
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Open Dataflow Design
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Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
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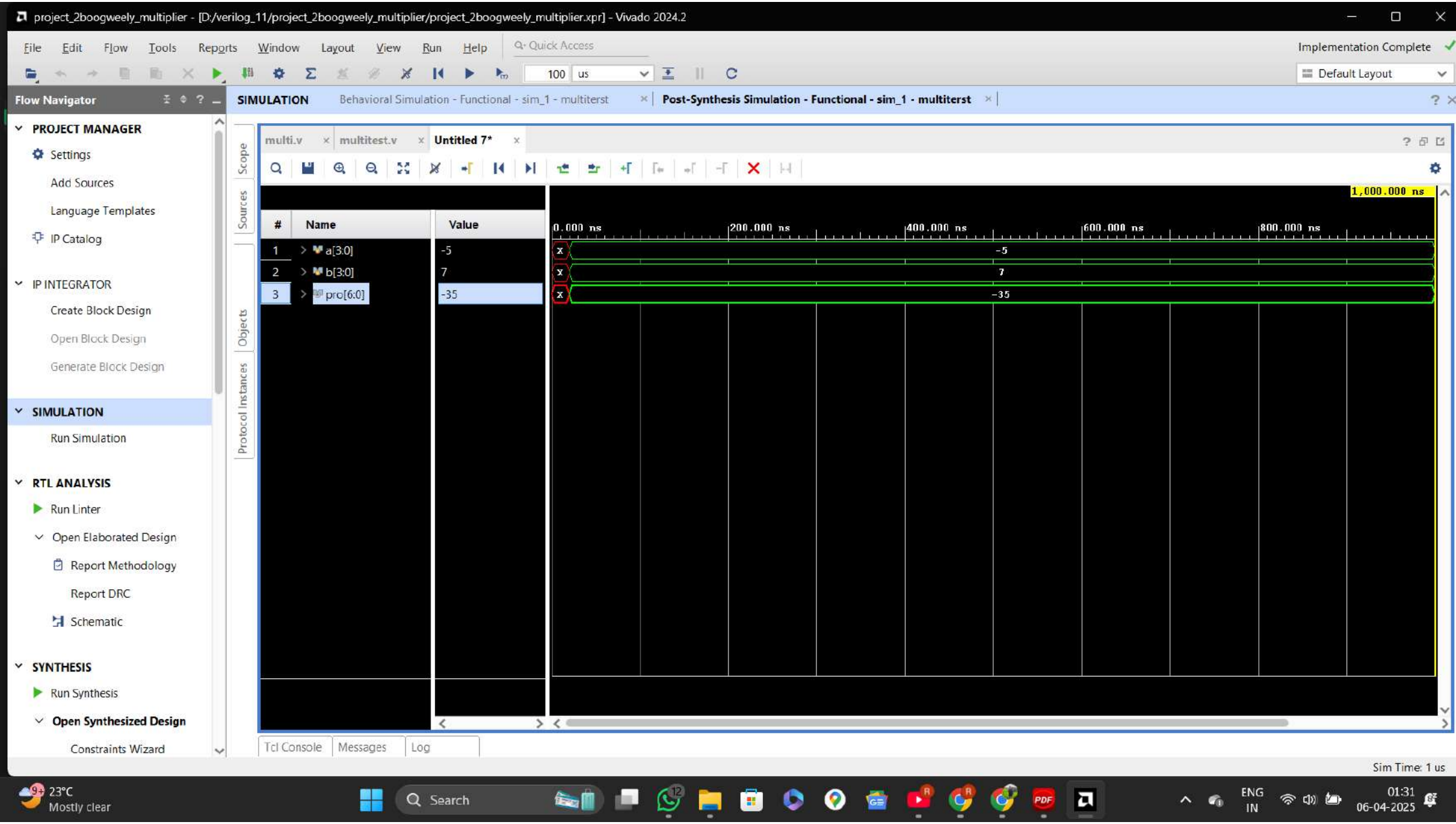
Open Hardware Manager
Sources
Netlist
Device Constraints
Properties
Clock Regions
Utilization
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
F8 Muxes (<1%)
F7 Muxes (<1%)
Slice Logic Distribution
Slice (<1%)
SLICEL
LUT as Logic (<1%)
using O6 output only<
using O5 and O6<>T a
Memory
DSP
IO and GT Specific
Bonded IOB (5%)
IOB Slave Pads
IOB Master Pads
Clocking
Specific Feature
Primitives
Black Boxes
Instantiated Netlists
Hierarchy
Name
Slice LUTs (134600)
F7 Muxes (67300)
F8 Muxes (33650)
Slice (33650)
LUT as Logic (134600)
Bonded IOB (285)
multi 17 4 2 5 17 15
utilization_1
Tcl Console Messages Log Reports Design Runs Timing Power DRC Package Pins I/O Ports
23°C Mostly clear
Search
ENG IN
01:30 06-04-2025


project_2boogweely_multiplier - [D:/verilog_11/project_2boogweely_multiplier/project_2boogweely_multiplier.xpr] - Vivado 2024.2
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Report DRC
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
SIMULATION
Behavioral Simulation - Functional - sim_1 - multiterst
Post-Synthesis Simulation - Functional - sim_1 - multiterst
multi.v
multitest.v
Untitled 7*
Scope
Sources
Objects
Protocol Instances
Name Value
1 a[3:0] -5
2 b[3:0] 7
3 pro[6:0] -35
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
-5
7
-35
Tcl Console
Messages
Log
Sim Time: 1 us
23°C
Mostly clear
Search
ENG
IN
01:31
06-04-2025