EC6101D Digital System Design using HDL

Lab Assignment - 1

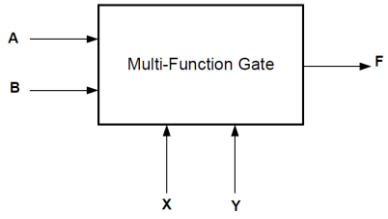
Guidelines for preparing report:

1. Start preparing your report well in advance instead of doing everything close to the dead line.
2. Report should contain Question, Gate level Circuit diagram and/or Truth Table, Verilog Code including testbench and Simulation Waveform.
3. Circuit Diagrams may be copied from any source. But make sure that all signals both at the interface and internal signals are named properly and use the same name in the code. Name all the instances as well.
4. Testbench is mandatory for all the designs.
5. Use the font **`Courier New size 10 Bold`** for Verilog code with single line spacing.
6. Use font Times New Roman, size 12 for text, 14 for headings and single line spacing.
7. Do all the simulations and prepare the report on your own. If found to be copied, marks will not be awarded for Lab Assignments.
8. Use the cover page template available in the LMS.
9. Submit the report in pdf format only. File name format should be **"Shortname_RegNo_Lab_Report_1.pdf".**
   Example: Rahul_M210656EC_Lab_report_1.pdf

Lab Exercises

1) Write structural level Verilog code of the following:
   a) 2x1 Mux using logic gates
   b) 4x1 Mux using logic gates
   c) 4x1 Mux using 2x1 Mux
   d) 8x1 Mux using 4x1 and 2x1 Mux
   e) 1x4 Demux using logic gates
   f) 2 to 4 Decoder using logic gates
   g) 4 to 2 Encoder using logic gates
   h) Half Adder using logic gates
   i) Full Adder using Half Adders
   j) 4-bit Ripple Carry Adder using Full Adders

2) Design a Multi-function gate which can work as a two input (A, B) one output (F) logic gate based on the control values placed on two other inputs X and Y. Control input values and the corresponding function is given in the table below. After obtaining the optimized schematic, write structural level verilog code for it.



X	Y	Function
0	0	AND
0	1	OR
1	0	NOR
1	1	NAND

3) Design a four-bit input prime number circuit. The output is logic 1 if the input is a prime number between 0 and 15. Write Structural level Verilog code for the circuit.

4) Write Verilog code using conditional operator for the following:
    a) 2x1 Mux
    b) 4x1 Mux
    c) 2 to 4 Decoder
    d) 4 to 2 Encoder

5) Write one testbench to check if the designs 1.b, 1.c and 4.b are equivalent by applying same set of test vectors simultaneously to all designs and comparing their outputs. At the end display a "PASS" if all outputs match else display a "FAIL".

6) Implement a circuit that performs the following function on a two 4-bit input numbers (X, N):

Input(X)	**Output**
X is odd number	X - N
X is even number	X + N

Design this circuit using minimal logic. The building components of your addition circuit should be composed of a 1-bit full adder and other logic as necessary.

a) Show the design steps including the truth table (Handwritten pages may be included in the report).

b) Circuit schematics and Structural level Verilog code of the design.

c) Results: Include one screen snapshot of the simulator outcome for the following input combinations

X= 8 and N=7

X= 15 and N=8