EC6101D Digital System Design using HDL
Lab Assignment - 2

Guidelines for preparing report:

1. Start preparing your report well in advance instead of doing everything close to the dead line.
2. Report should contain Question, Gate level Circuit diagram and/or Truth Table, Verilog Code including testbench and Simulation Waveform.
3. Circuit Diagrams may be copied from any source. But make sure that all signals both at the interface and internal signals are named properly and use the same name in the code. Name all the instances as well.
4. Testbench is mandatory for all the designs.
5. Use the font **`Courier New size 10 Bold`** for Verilog code with single line spacing.
6. Use font Times New Roman, size 12 for text, 14 for headings and single line spacing.
7. Do all the simulations and prepare the report on your own. If found to be copied, marks will not be awarded for Lab Assignments.
8. Use the cover page template available in the LMS.
9. Submit the report in pdf format only. File name format should be **"Shortname_RegNo_Lab_Report_2.pdf".**
   Example: Rahul_M210656EC_Lab_report_2.pdf

Lab Exercises

All Verilog codes in this assignment are to be written in Behavioral level unless otherwise mentioned.

1) JK Flip-Flop.
2) 8-bit Shift register.
3) 4-bit up-down counter.
4) 8-bit Johnson Counter.
5) Write the hardware description of a 4-bit mod-13 up-down counter.
6) Write Behavioral level Verilog code for the following Universal shift register controlled by {S1,S0} with synchronous reset signal.

S1	S0	Action
0	0	Hold
0	1	Shift right
1	0	Shift left
1	1	Parallel load

7) Write Verilog code for N-bit Ripple Carry Adder (RCA) using **`parameter`** (default value is 6) and **`generate`**. Write two different testbenches one for 4-bit and another for 8-bit RCA by overriding the parameter value and verify it. Show the results of any 3 different input combinations.

8) Use files for providing the inputs and storing the outputs in the testbenches written for Q7 (4-bit RCA). Show the content of the input and output files with atleast 5 entries.

9) Use functions and tasks to provide the inputs and perform self-checking of the outputs in the testbenches written for Q7 (4-bit RCA). Output corresponding to all the possible input combinations are to be checked.

10) Write behavioral level Verilog code for a parallel to serial data converter (16-bit to 8-bit) using the waveform given below.