KANUGOVI HARINI

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Objective

Seeking a challenging position in an esteemed organization where I can explore my skills in developing design and verifying by contributing towards the growth of organization.

Work experience

- Working as Graphics hardware DV engineer in GPU – VPC team.
- Worked as a Design Engineer at Truechip Solutions for a period of 2 months.
- Worked as Associate Engineer at Cerium Systems Pvt. Ltd. (Client – Intel, End Client –Mobiveil) for a period of 10 months.
- Worked as RTL Design Engineer at Semi Design for a period of 1 year, 3 months.

Trainings and certifications

- Professional training: PG Diploma in VLSI (Frontend Developer) from Cranes varsity a Training Division of Cranes Software International Ltd for a period of 5 months.

Academic Credentials

- Bachelor of technology (Electronics and communication engineering) from Vignana Bharathi institute of technology (Affiliated to JNTUH) in 2019 with 74% aggregate.
- Intermediate (MPC) from Sri Gayatri junior college in 2015 with 93% aggregate.
- SSC from Geetanjali Vidhyalaya School in 2013 with 8.0 CGPA.

Technical exposure

- **Hardware Description Languages:** Verilog, System Verilog, UVM (Basics)
- **Automation Tools:** Xilinx ISE, Synopsys Verdi

Key skills

- Good communicator and have strong presentation skills.
- Able to work in multi-disciplinary team environment.
- Self-motivated and a strong team-player.
- Ability to learn new tools and technologies.
- Ready to accept challenges.

Projects

- **Project-1: VPC block verification in GPU**

  Description: This project is to verify VPC block in GPU. Verifying the vector and random tests, along with the performance of the registers that passes through the interfaces of sub-blocks in VPC (FE, BE and US).

  Tool used: Verdi (Synopsys)
  Language: UVM
  Role: Debugging

- **Project-2: Verification of CXL InterOp**

  Description: This project is to verify the host which is integrated with five different devices. Need to check whether link is trained with Gen5 speed and debug the failure test cases for MESI protocol.

  Tool used: Verdi (Synopsys)
  Language: SV
  Role: Debugging

- **Project-3: Verification of Avalon streaming interface (AVST)**

  Description: This project is to develop different test cases to verify packet transfer, it helps to have the communication between source and sink. Need to verify all the tests for the given DUT.

  Tool used: Verdi (Synopsys)
  Language: SV
  Role: programmer

- **Project-4: Design of I2C (Inter Integrated Circuit) Protocol**

  Description: This Project is to develop a bidirectional, half duplex serial communication protocol, it is multi master and multi slave communication protocol. So, this implementation helps to understand how two devices communicate using master and slave technology.

  Tool used: Xilinx ISE, Questa Sim
  Language: Verilog
  Role: Programmer

- **Project-5: Design of SPI (Serial peripheral interface) Protocol**

  Description: This project is to establish the communication between two units such as master and slave in full duplex mode. This is one of the protocols which can provide communication between different peripheral devices with one master and many slave devices.

  Tool used: Xilinx ISE, Questa Sim
  Language: Verilog
  Role: Programmer

- **Project-6: Design of UART (Universal Asynchronous Receiver andTransmitter) Protocol:**

  Description: This Project is to develop a device that has capability to both receive and transmit serial data. For transmission the UART protocol wraps this 8-bit data.

  Tool used: Xilinx ISE, Questa Sim
  Language: Verilog, System Verilog
  Role: Programmer

- **Project-7: Design of Cryptography encryption of 128-bit data using AES**

  Description: This project is to monitor how to protect the data when the data is used for confidential purpose which is stored and exchanged between sender and receiver. In this case security plays very crucial role for data transmission.

  Tool used: Xilinx ISE.
  Language: Verilog
  Role: Programmer

- **Project-8: RF Energy harvesting for Spectrum Management in Cognitive Radio Networks (B. Tech Major project)**

  Description: This project is to harvest the radio frequency energy in cognitive radio networks and to improve the spectrum efficiency. Here, we evaluate the accuracy of the advanced H2BMM and H2BMM based spectrum prediction to achieve better prediction accuracy in a mobile CRN and RF energy is harvested. This integration brings an accuracy prediction on channel status with a relatively low computational complexity. Hence, the mobile frequencies can be dispersed and thus the communication can be further increased.

  Tool used: Matlab
  Language: C
  Role: Programmer

Papers Published

- Participated in **International conference on emerging trends in engineering (ICETE)** conducted by OUCE Alumni association with publishing partner **Spinger** at Osmania University.

  Link - https://link.springer.com/chapter/10.1007%2F978-3-030-24318-0_21

Achievements

- Joint secretary at **IETE – ISF SB** for the tenure 2017-2018.
- Technical coordinator at **IEEE – VBIT SB** for the tenure 2017-2018.
- Document writer at **IETE – VBIT SB** for the tenure 2016-2017.

Declaration

I hereby declare that the above information is true and correct to the best of my knowledge.

(K.HARINI)

Place:
Date: