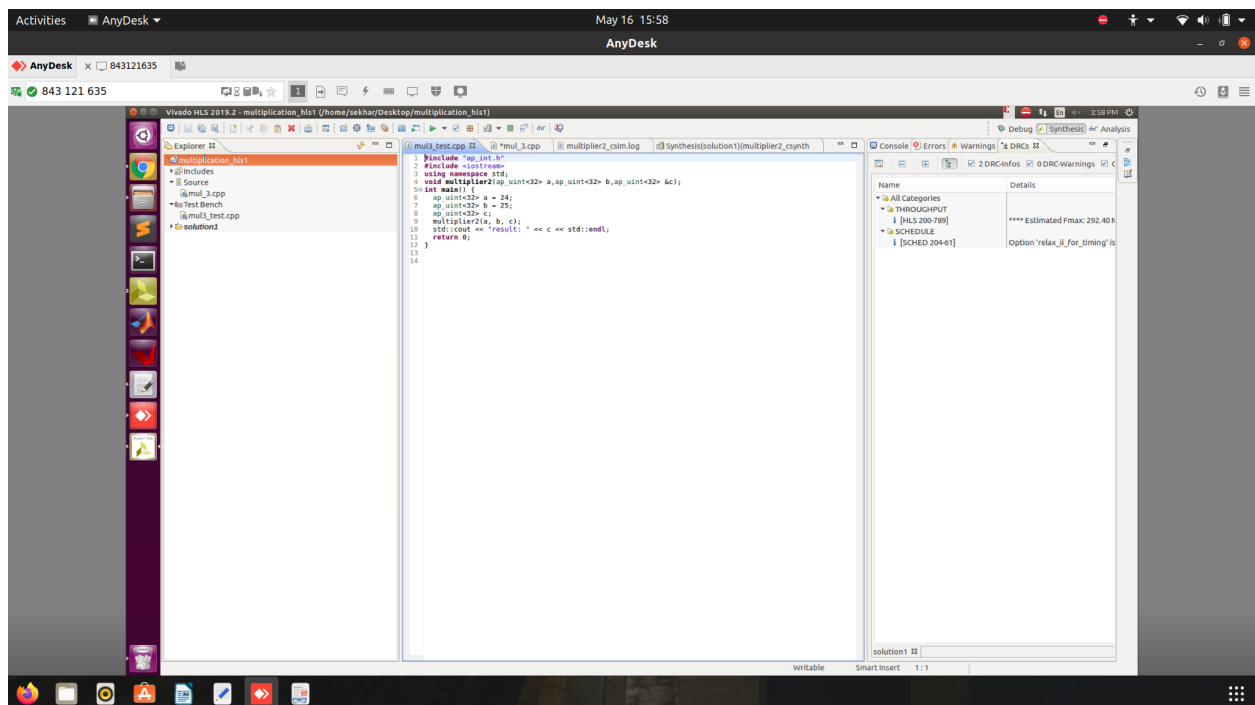
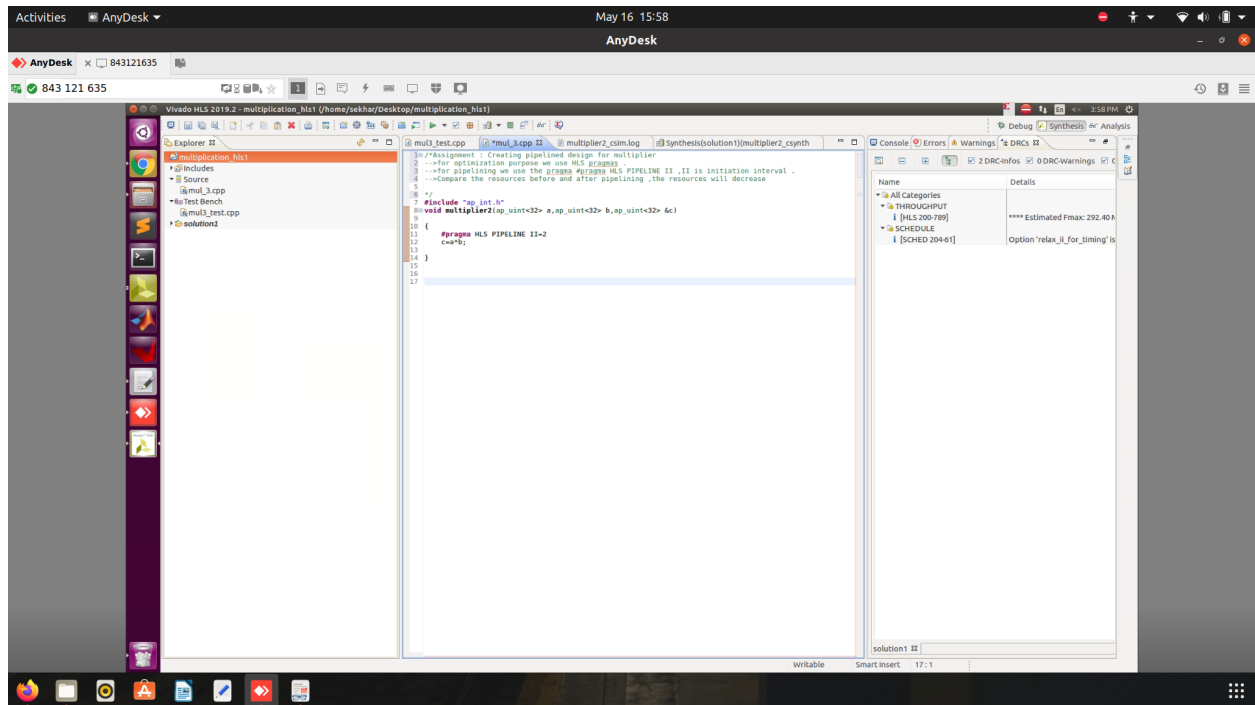


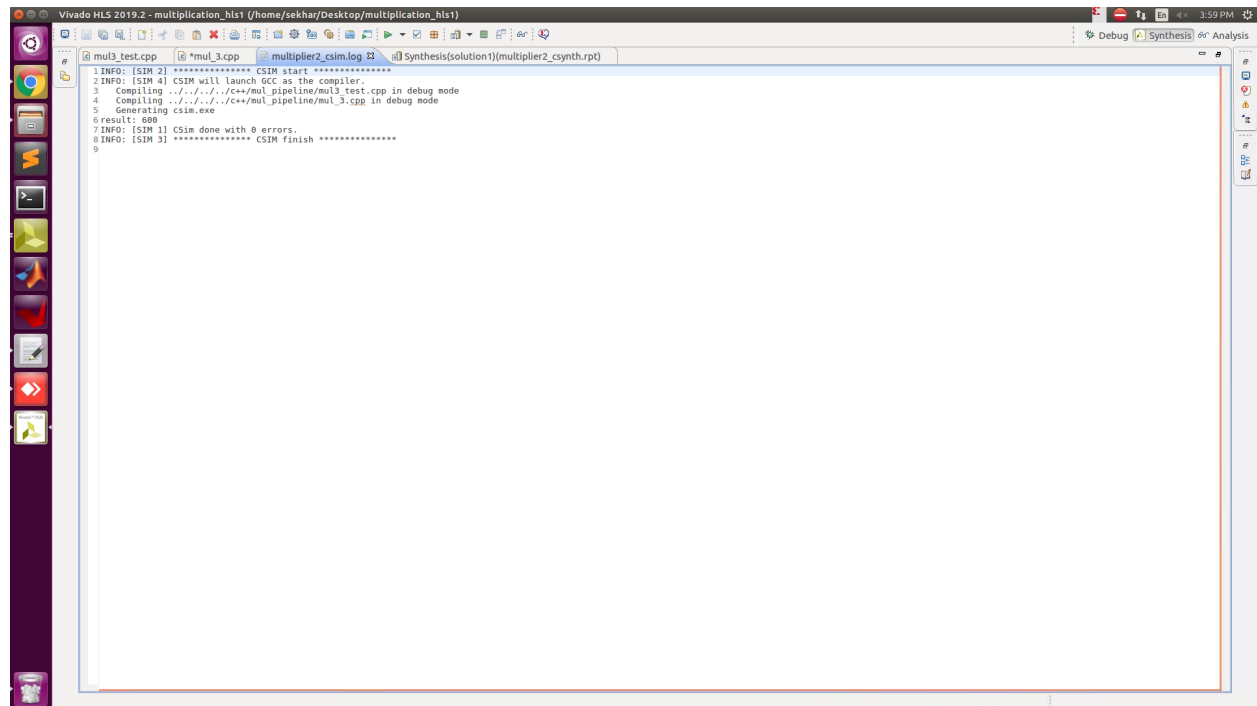
Assignment -2

Create a pipelined design for the multiplier experiment using HLS Pragma

Simulation :

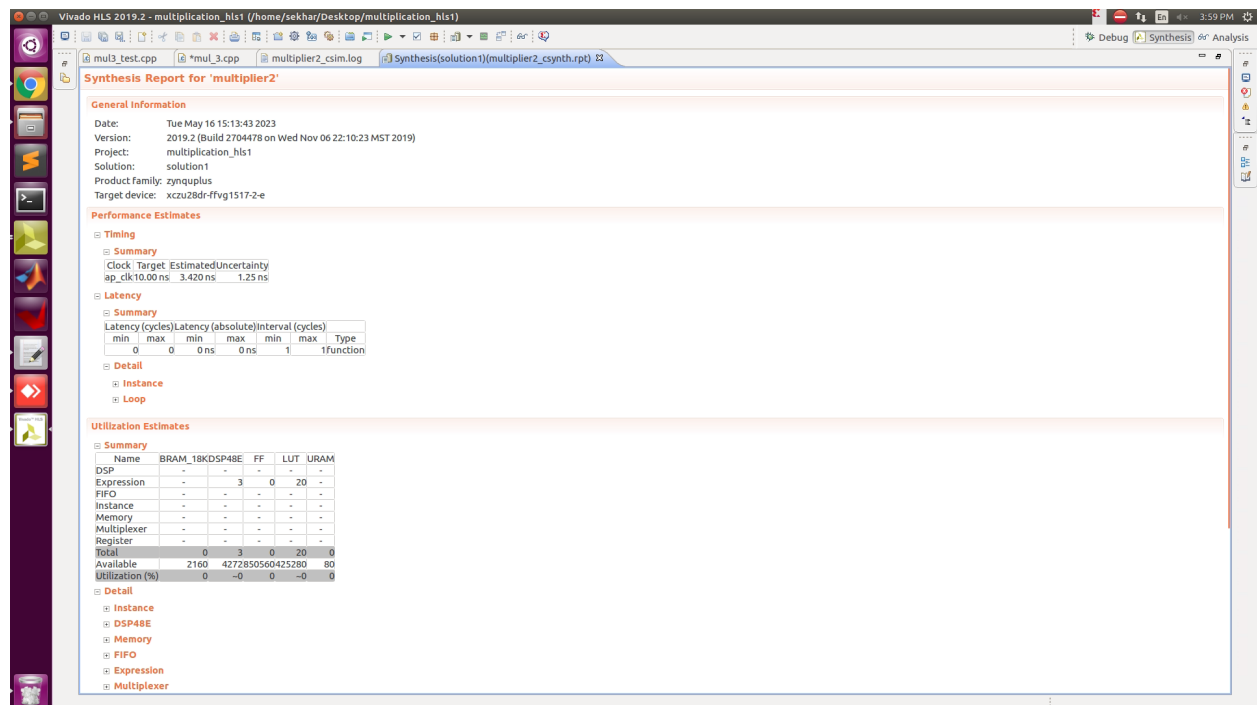


Result :



```
1 INFO: [SIM 2] ***** CSIM start *****
2 INFO: [SIM 4] CSIM will launch GCC as the compiler.
3 Compiling ../../../../../../c++/mul_pipeline/mul3_test.cpp in debug mode
4 Compiling ../../../../../../c++/mul_pipeline/mul3.cpp in debug mode
5 Generating csim.exe
6 result: 600
7 INFO: [SIM 1] CSim done with 0 errors.
8 INFO: [SIM 3] ***** CSIM finish *****
9
```

Synthesis Report :



Synthesis Report for 'multiplier2'

General information

Date: Tue May 16 15:13:43 2023
Version: 2019.2 (Build 2704478 on Wed Nov 06 22:10:23 MST 2019)
Project: multiplication_hls1
Solution: solution1
Product family: zynqplus
Target device: xczu28dt-ffvg1517-2-e

Performance Estimates

Timing

Summary

| Clock | Target | Estimated | Uncertainty |
|--------|----------|-----------|-------------|
| ap_clk | 10.00 ns | 3.420 ns | 1.25 ns |

Latency

Summary

| Latency (cycles) | Latency (absolute) | Interval (cycles) | | |
|------------------|--------------------|-------------------|------|------------|
| min | max | min | max | Type |
| 0 | 0 | 0 ns | 0 ns | 1 function |

Detail

Instance

Loop

Utilization Estimates

Summary

| Name | BRAM | 18KDSP48E | FF | LUT | URAM |
|-----------------|------|------------|--------|-----|------|
| DSP | - | - | - | - | - |
| Expression | - | 3 | 0 | 20 | - |
| FIFO | - | - | - | - | - |
| Instance | - | - | - | - | - |
| Memory | - | - | - | - | - |
| Multiplexer | - | - | - | - | - |
| Register | - | - | - | - | - |
| Total | 0 | 3 | 0 | 20 | 0 |
| Available | 2160 | 4272850560 | 425280 | 80 | 80 |
| Utilization (%) | 0 | -0 | 0 | -0 | 0 |

Detail

Instance

DSP48E

Memory

FIFO

Expression

Multiplexer