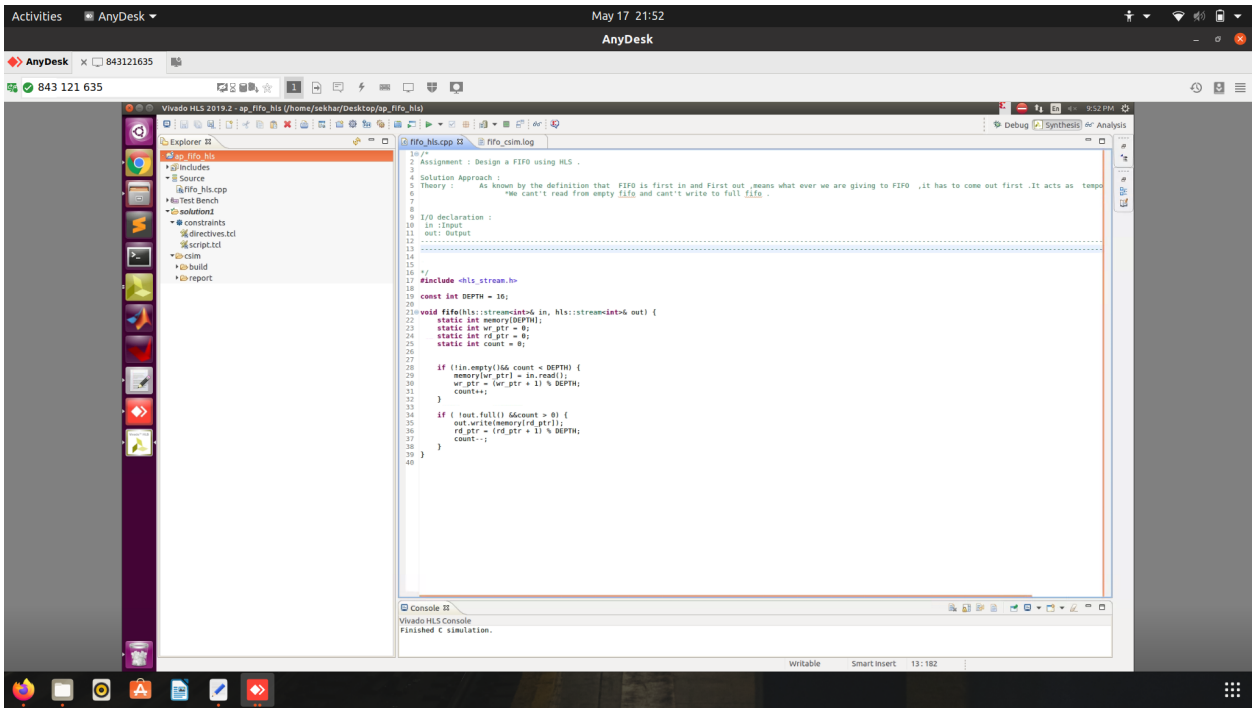
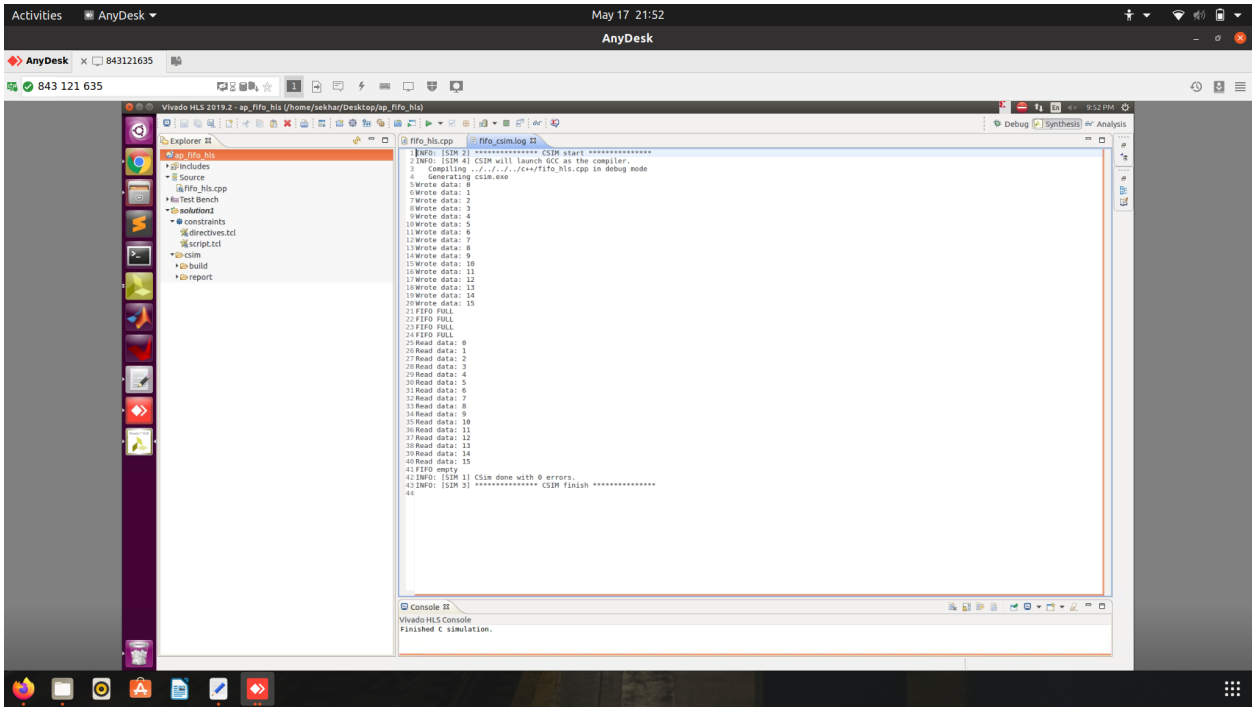
Assignment-8

Implement a FIFO using HLS

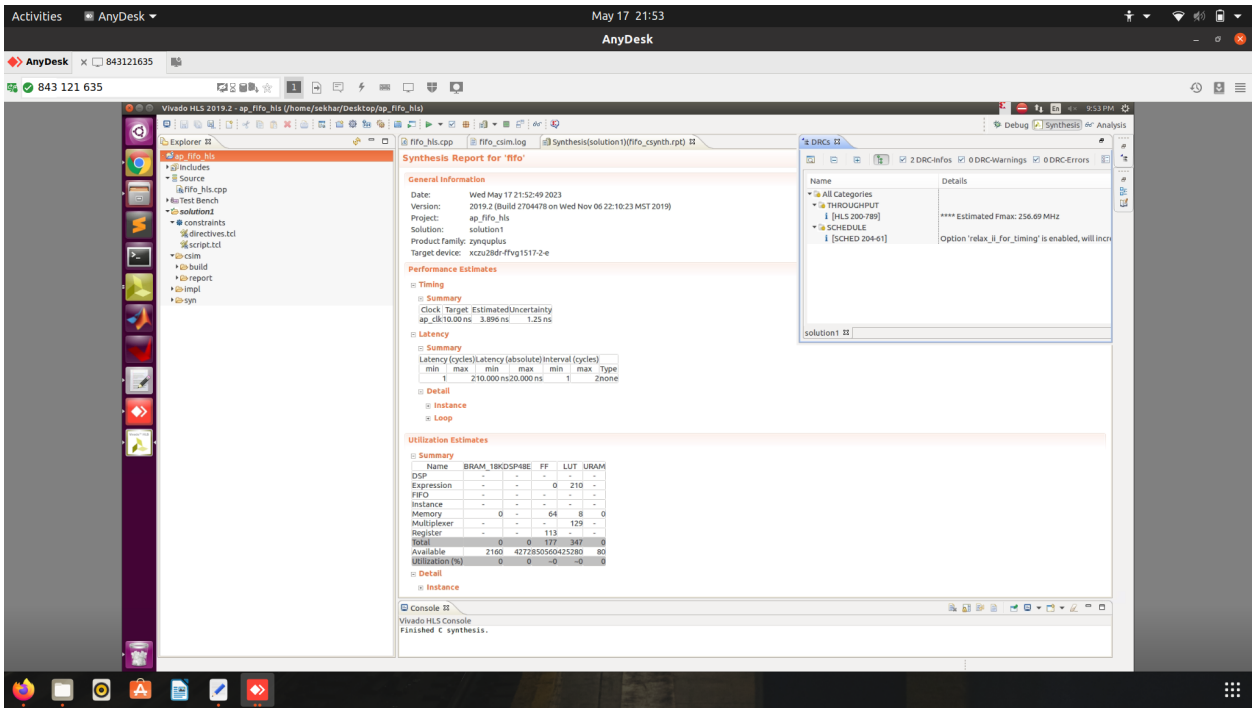
Simulation :



Result :



Synthesis :


Activities
AnyDesk
May 17 21:53
AnyDesk
843 121 635
Vivado HLS 2019.2 - ap_fifo_hls (/home/sekhar/Desktop/ap_fifo_hls)
Explorer
ap_fifo_hls
Includes
Source
fifo_hls.cpp
Test Bench
solution1
constraints
directives.tcl
script.tcl
csim
build
report
impl
syn
fifo_hls.cpp
fifo_csim.log
Synthesis(solution1)(fifo_csynth.rpt)
Synthesis Report for 'fifo'
General Information
Date: Wed May 17 21:52:49 2023
Version: 2019.2 (Build 2704478 on Wed Nov 06 22:10:23 MST 2019)
Project: ap_fifo_hls
Solution: solution1
Product family: zynquplus
Target device: xczu28dr-ffvg1517-2-e
Performance Estimates
Timing
Summary
Clock Target EstimatedUncertainty
ap_clk 10.00 ns 3.896 ns 1.25 ns
Latency
Summary
Latency (cycles) Latency (absolute) Interval (cycles)
min max min max min max Type
1 1 210.000 ns 20.000 ns 1 1 none
Detail
Instance
Loop
Utilization Estimates
Summary
Name BRAM_18K DSP48E FF LUT URAM
DSP - - - - -
Expression - - - 0 210 -
FIFO - - - - - -
Instance - - - - - -
Memory - 0 - 64 8 0
Multiplexer - - - - 129 -
Register - - - 113 - -
Total 0 0 0 177 347 0
Available 2160 4272 850 560 425 280 80
Utilization (%) 0 0 0 0 0 0
Detail
Instance
DRCs
2 DRC-Infos 0 DRC-Warnings 0 DRC-Errors
Name Details
All Categories
THROUGHPUT
[HLS 200-789] **** Estimated Fmax: 256.69 MHz
SCHEDULE
[SCHED 204-61] Option 'relax_ii_for_timing' is enabled, will incr
solution1
Debug Synthesis Analysis
Console
Vivado HLS Console
Finished C synthesis.