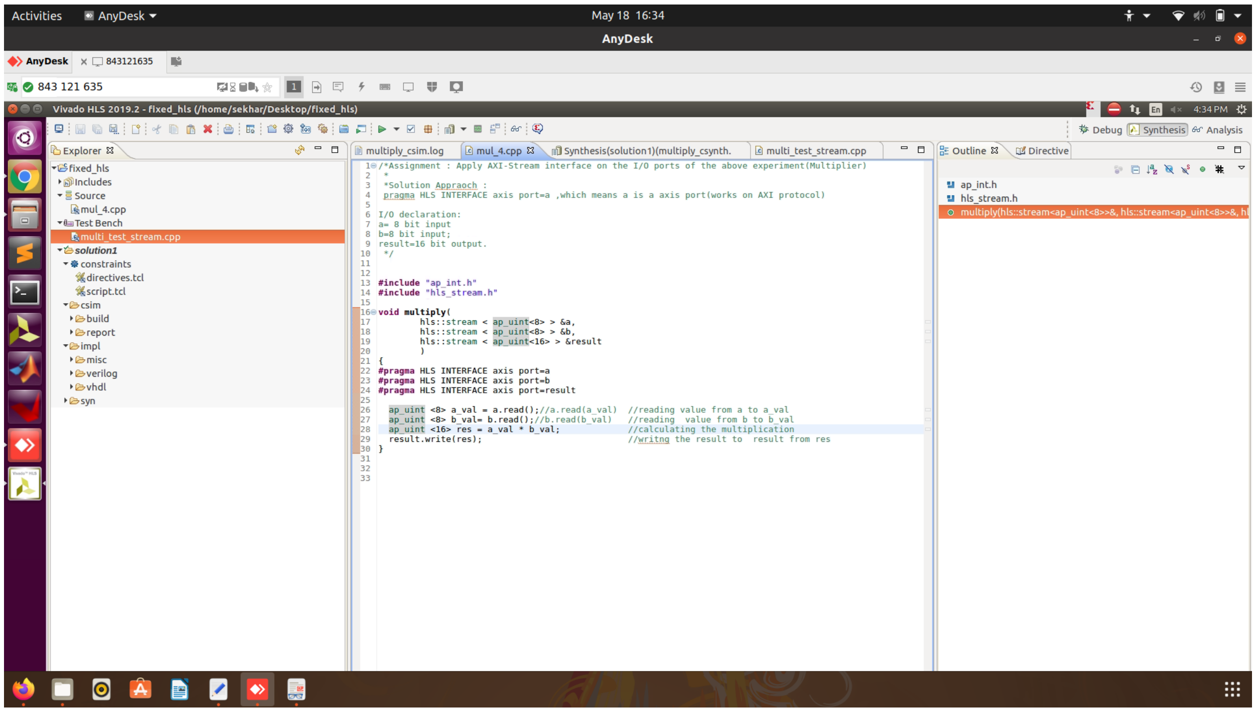
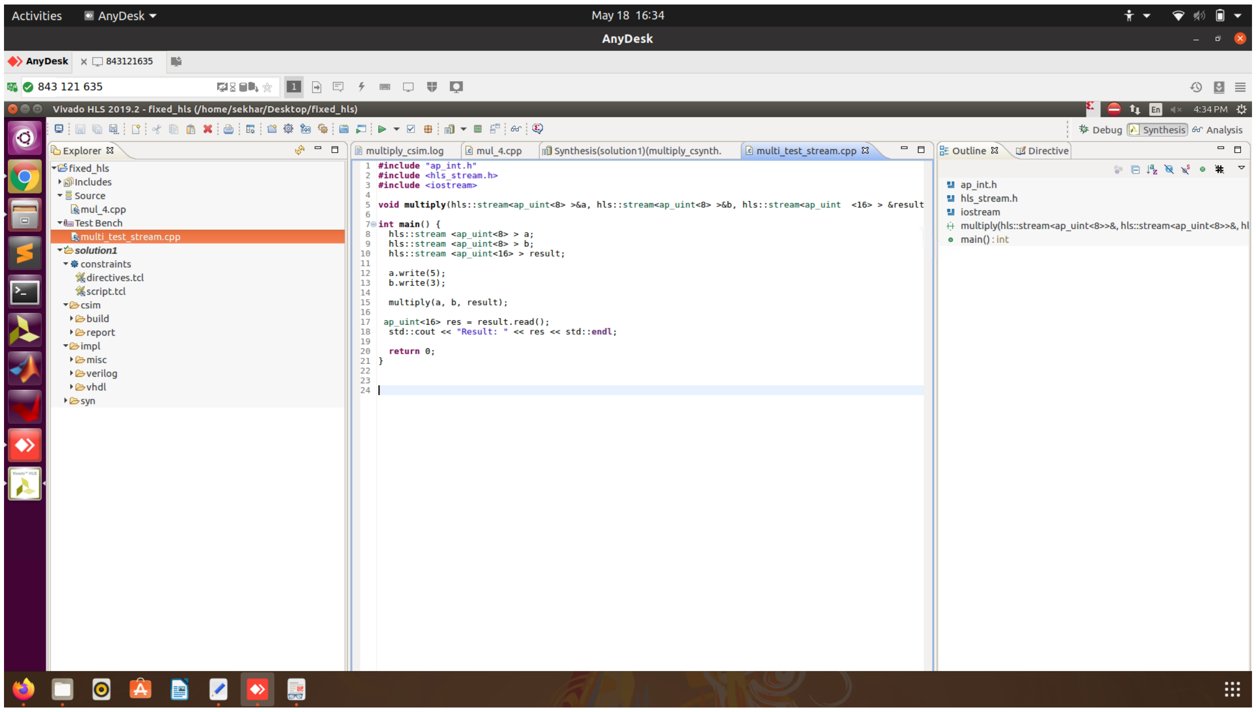
Assignment -3

Apply AXI-Stream interface on the I/O ports of the multiplier experiment

Simulation :

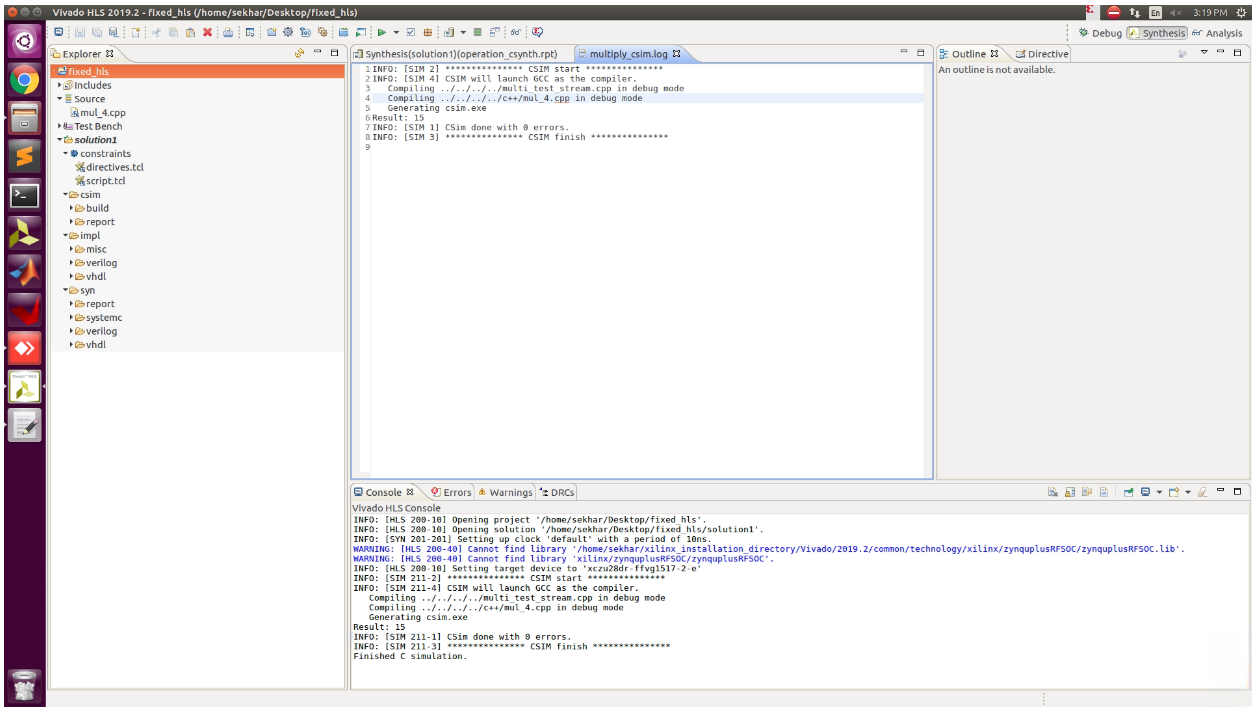


```
/*Assignment : Apply AXI-Stream interface on the I/O ports of the above experiment(Multiplier)
 *
 *Solution Appraoch :
 pragma HLS INTERFACE axis port=a ,which means a is a axis port(works on AXI protocol)

I/O declaration:
a= 8 bit input
b=8 bit input;
result=16 bit output.
 */


#include "ap_int.h"
#include "hls_stream.h"

void multiply(
        hls::stream < ap_uint<8> > &a,
        hls::stream < ap_uint<8> > &b,
        hls::stream < ap_uint<16> > &result
        )
{
#pragma HLS INTERFACE axis port=a
#pragma HLS INTERFACE axis port=b
#pragma HLS INTERFACE axis port=result

  ap_uint <8> a_val = a.read();//a.read(a_val)  //reading value from a to a_val
  ap_uint <8> b_val= b.read();//b.read(b_val)   //reading  value from b to b_val
  ap_uint <16> res = a_val * b_val;             //calculating the multiplication
  result.write(res);                            //writng the result to  result from res
}
```



```
#include "ap_int.h"
#include <hls_stream.h>
#include <iostream>

void multiply(hls::stream<ap_uint<8> >&a, hls::stream<ap_uint<8> >&b, hls::stream<ap_uint  <16> > &result

int main() {
  hls::stream <ap_uint<8> > a;
  hls::stream <ap_uint<8> > b;
  hls::stream <ap_uint<16> > result;

  a.write(5);
  b.write(3);

  multiply(a, b, result);

 ap_uint<16> res = result.read();
  std::cout << "Result: " << res << std::endl;

  return 0;
}
```

Result :

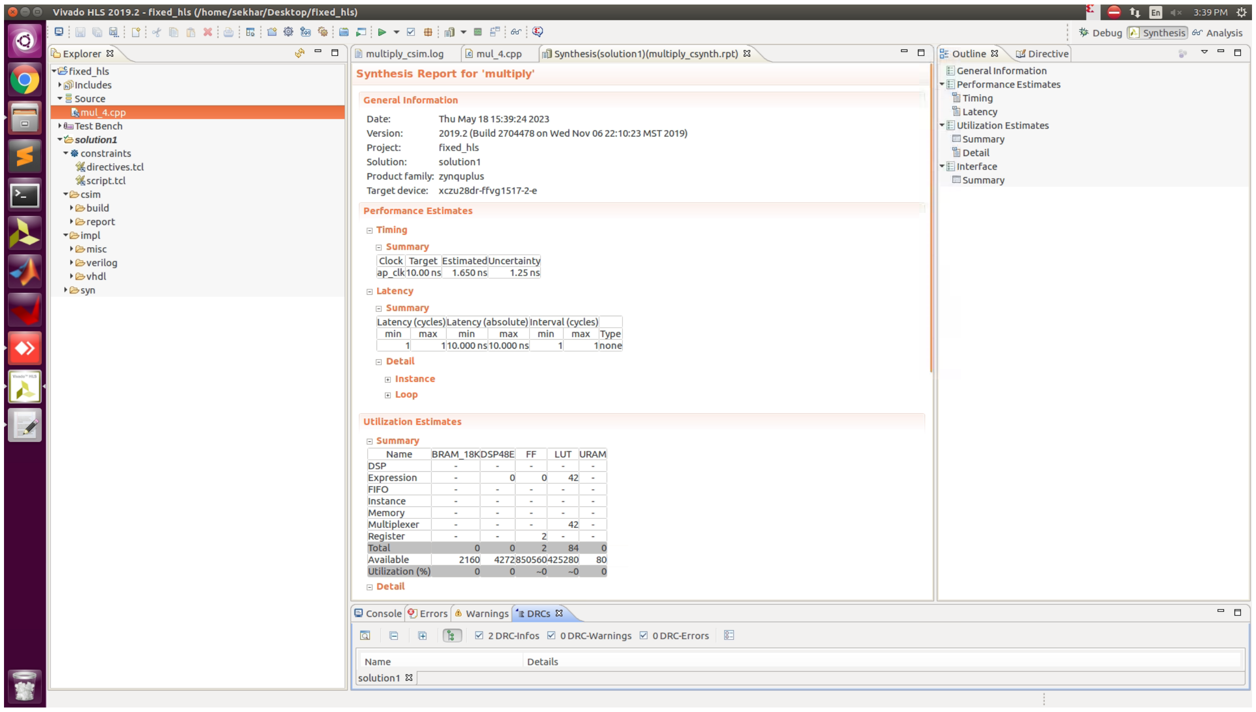

Vivado HLS 2019.2 - fixed_hls (/home/sekhar/Desktop/fixed_hls)
Explorer
Synthesis(solution1)(operation_csynth.rpt)
multiply_csim.log
Outline
Directive
An outline is not available.
Debug
Synthesis
Analysis
Console
Errors
Warnings
DRCs

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../multi_test_stream.cpp in debug mode
   Compiling ../../../../c++/mul_4.cpp in debug mode
   Generating csim.exe
Result: 15
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

Vivado HLS Console

```
INFO: [HLS 200-10] Opening project '/home/sekhar/Desktop/fixed_hls'.
INFO: [HLS 200-10] Opening solution '/home/sekhar/Desktop/fixed_hls/solution1'.
INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.
WARNING: [HLS 200-40] Cannot find library '/home/sekhar/xilinx_installation_directory/Vivado/2019.2/common/technology/xilinx/zynquplusRFSOC/zynquplusRFSOC.lib'.
WARNING: [HLS 200-40] Cannot find library 'xilinx/zynquplusRFSOC/zynquplusRFSOC'.
INFO: [HLS 200-10] Setting target device to 'xczu28dr-ffvg1517-2-e'
INFO: [SIM 211-2] *************** CSIM start ***************
INFO: [SIM 211-4] CSIM will launch GCC as the compiler.
   Compiling ../../../../multi_test_stream.cpp in debug mode
   Compiling ../../../../c++/mul_4.cpp in debug mode
   Generating csim.exe
Result: 15
INFO: [SIM 211-1] CSim done with 0 errors.
INFO: [SIM 211-3] *************** CSIM finish ***************
Finished C simulation.
```

Synthesis Result :



Synthesis Report for 'multiply'

General Information

Date:	Thu May 18 15:39:24 2023
Version:	2019.2 (Build 2704478 on Wed Nov 06 22:10:23 MST 2019)
Project:	fixed_hls
Solution:	solution1
Product family:	zynquplus
Target device:	xczu28dr-ffvg1517-2-e

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	1.650 ns	1.25 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
1	1	10.000 ns	10.000 ns	1	1	none

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	0	0	42	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	42	-
Register	-	-	2	-	-
Total	0	0	2	84	0
Available	2160	4272	850560	425280	80
Utilization (%)	0	0	~0	~0	0

Detail

Console Errors Warnings DRCs

2 DRC-Infos 0 DRC-Warnings 0 DRC-Errors

Name	Details
solution1	