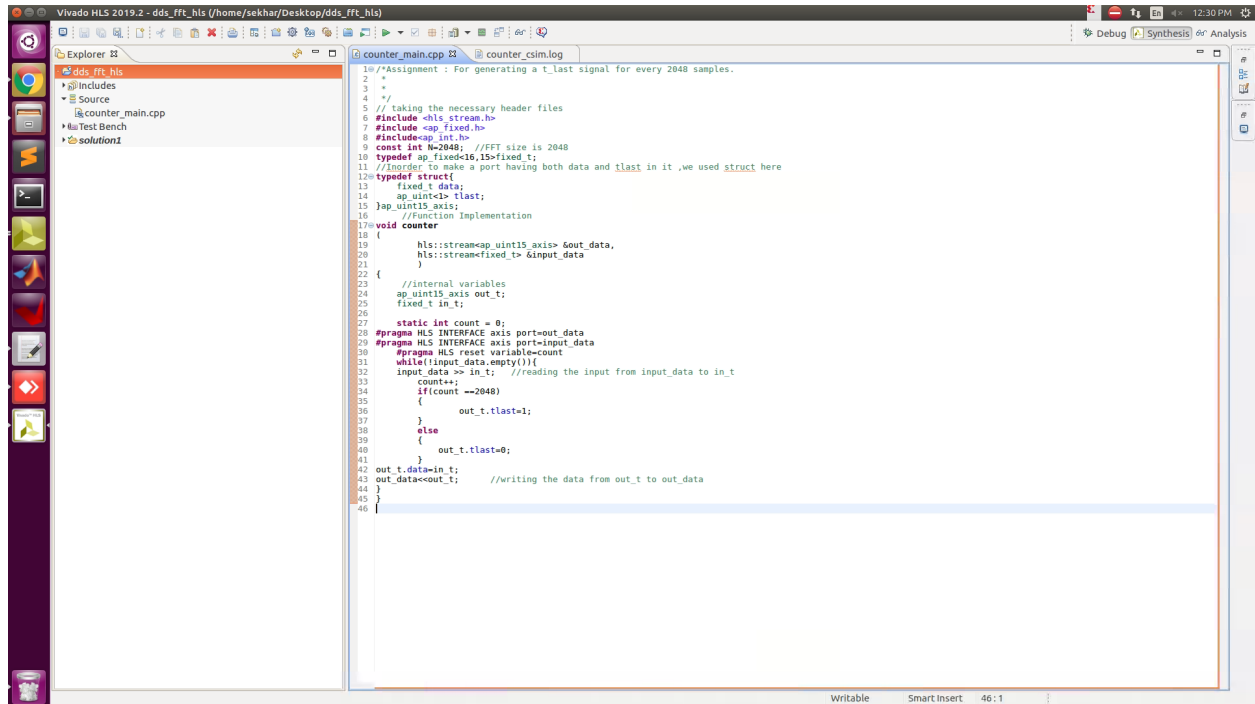


Assignment-10

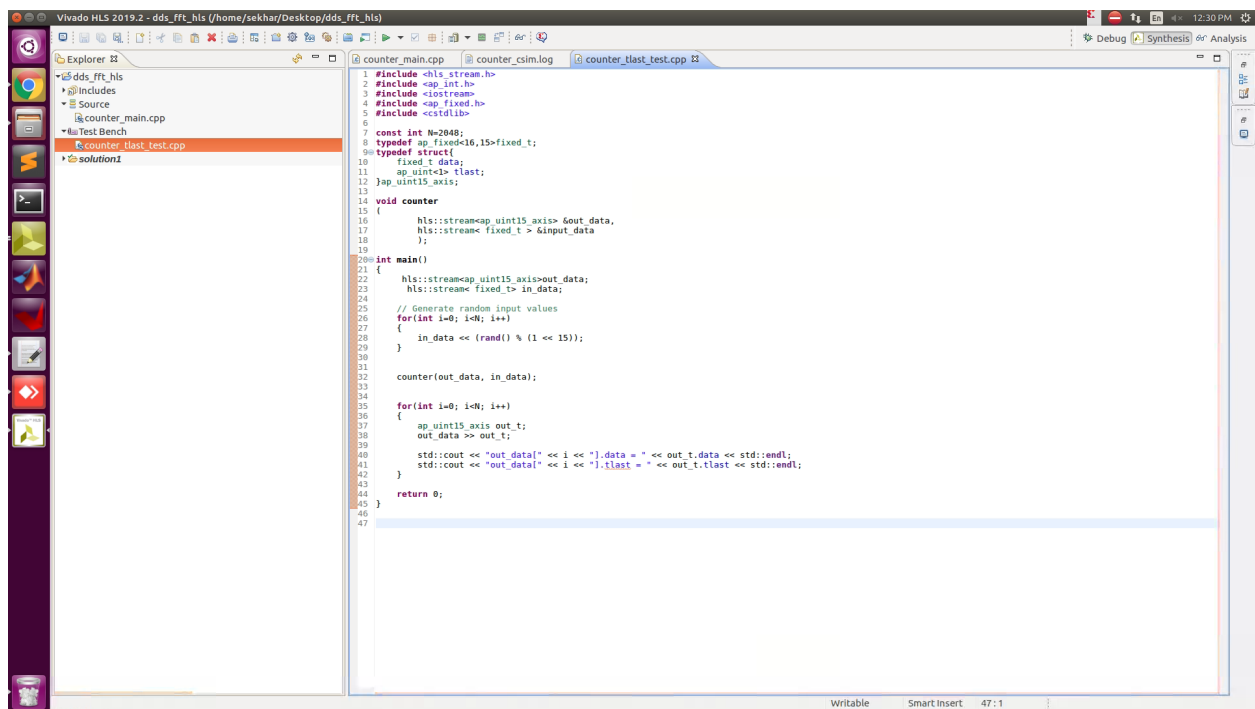
As a part of **Using Xilinx FFT IP in the design**, I implemented this IP for tlast signal .

Simulation :



The screenshot shows the Vivado IDE with the 'counter_main.cpp' file open. The code implements a counter module that generates a 'tlast' signal every 2048 samples. The module has two ports: 'ap_uint15_t tlast' and 'ap_uint15_axis'. The implementation includes a 'void counter' function that reads input data, increments a counter, and updates the 'tlast' signal when the counter reaches 2048.

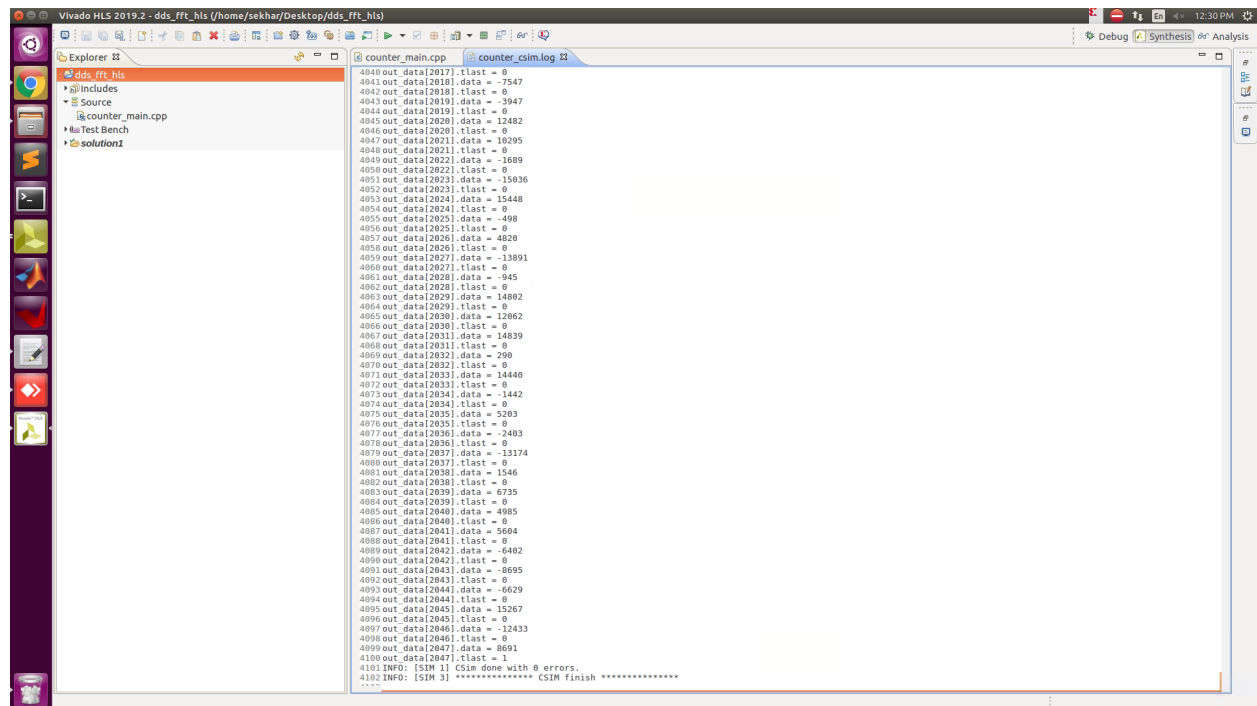
```
10 /*Assignment : For generating a t_last signal for every 2048 samples.
2 *
3 *
4 */
5 // taking the necessary header files
6 #include <hls_stream.h>
7 #include <ap_fixed.h>
8 #include <ap_int.h>
9 const int N=2048; //FFT size is 2048
10 typedef ap_fixed<16,15>fixed_t;
11 //Inorder To make a port having both data and tlast in it ,we used struct here
12 typedef struct{
13     fixed_t data;
14     ap_uint15_t tlast;
15 }ap_uint15_axis;
16 //Function Implementation
17 void counter
18 {
19     hls::stream<ap_uint15_axis> 6out_data,
20     hls::stream<fixed_t> 6input_data
21 }
22 {
23     //Internal variables
24     ap_uint15_axis out_t;
25     fixed_t in_t;
26
27     static int count = 0;
28     #pragma HLS INTERFACE axis port=out_data
29     #pragma HLS INTERFACE axis port=input_data
30     #pragma HLS reset variable=count
31     while(!input_data.empty()){
32         input_data >> in_t; //reading the input from input_data to in_t
33         count++;
34         if(count ==2048)
35         {
36             out_t.tlast=1;
37         }
38         else
39         {
40             out_t.tlast=0;
41         }
42         out_t.data=in_t;
43         out_data<<out_t; //writing the data from out_t to out_data
44     }
45 }
46 }
```



The screenshot shows the Vivado IDE with the 'counter_test.cpp' file open. The code implements a test module that generates random input values and calls the 'counter' function to generate the 'tlast' signal. The module has two ports: 'ap_uint15_axis' and 'ap_uint15_axis'. The implementation includes a 'main' function that generates random input values, calls the 'counter' function, and prints the output data and 'tlast' signal.

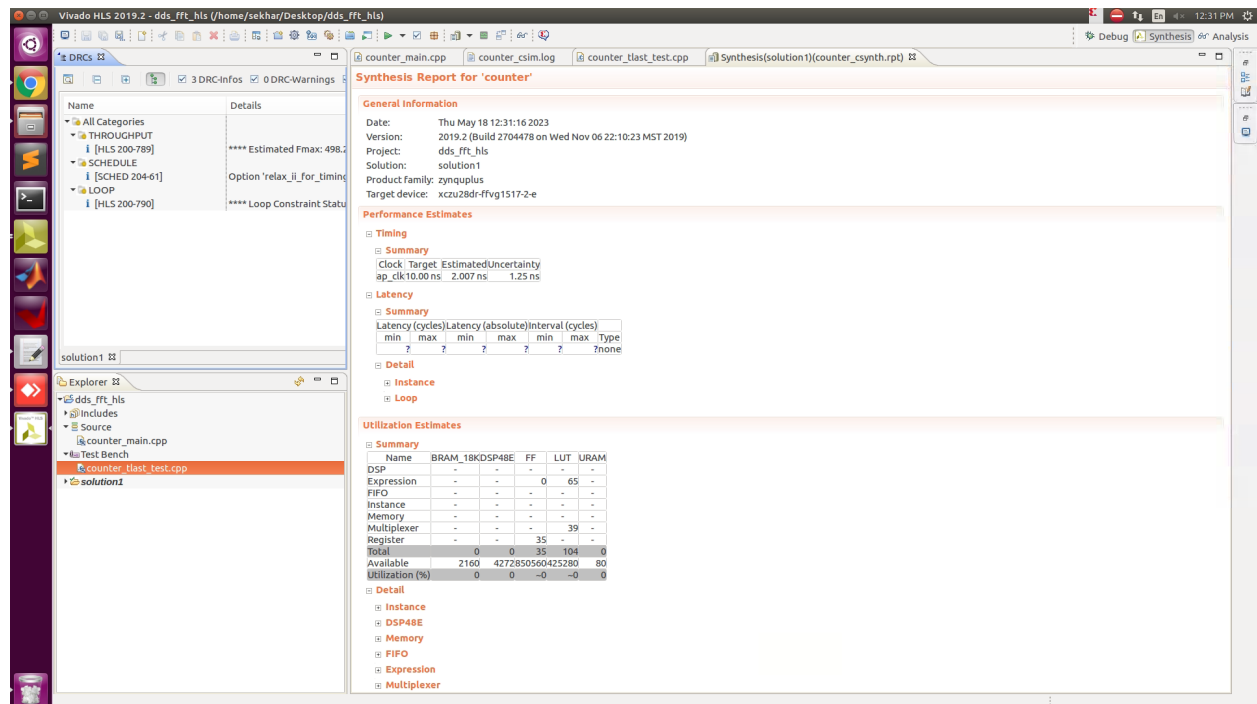
```
1 #include <hls_stream.h>
2 #include <ap_int.h>
3 #include <iostream>
4 #include <ap_fixed.h>
5 #include <cstdlib>
6
7 const int N=2048;
8 typedef ap_fixed<16,15>fixed_t;
9 typedef struct{
10     fixed_t data;
11     ap_uint15_t tlast;
12 }ap_uint15_axis;
13
14 void counter
15 {
16     hls::stream<ap_uint15_axis> 6out_data,
17     hls::stream<fixed_t> 6input_data
18 };
19
20 int main()
21 {
22     hls::stream<ap_uint15_axis>out_data;
23     hls::stream<fixed_t> in_data;
24
25     // Generate random input values
26     for(int i=0; i<N; i++)
27     {
28         in_data << (rand() % (1 << 15));
29     }
30
31     counter(out_data, in_data);
32
33     for(int i=0; i<N; i++)
34     {
35         ap_uint15_axis out_t;
36         out_data >> out_t;
37
38         std::cout << "out_data[" << i << "]data = " << out_t.data << std::endl;
39         std::cout << "out_data[" << i << "].tlast = " << out_t.tlast << std::endl;
40     }
41
42     return 0;
43 }
44
45
46
47 }
```

Result :



```
4040 out_data(2017).tlast = 0
4041 out_data(2018).data = -7547
4042 out_data(2018).tlast = 0
4043 out_data(2019).data = -3947
4044 out_data(2019).tlast = 0
4045 out_data(2020).data = 12482
4046 out_data(2020).tlast = 0
4047 out_data(2021).data = 18295
4048 out_data(2021).tlast = 0
4049 out_data(2022).data = -1689
4050 out_data(2022).tlast = 0
4051 out_data(2023).data = -15836
4052 out_data(2023).tlast = 0
4053 out_data(2024).data = 15448
4054 out_data(2024).tlast = 0
4055 out_data(2025).data = -498
4056 out_data(2025).tlast = 0
4057 out_data(2026).data = 4828
4058 out_data(2026).tlast = 0
4059 out_data(2027).data = -13891
4060 out_data(2027).tlast = 0
4061 out_data(2028).data = -945
4062 out_data(2028).tlast = 0
4063 out_data(2029).data = 14882
4064 out_data(2029).tlast = 0
4065 out_data(2030).data = 12862
4066 out_data(2030).tlast = 0
4067 out_data(2031).data = 14839
4068 out_data(2031).tlast = 0
4069 out_data(2032).data = 290
4070 out_data(2032).tlast = 0
4071 out_data(2033).data = 14440
4072 out_data(2033).tlast = 0
4073 out_data(2034).data = -1442
4074 out_data(2034).tlast = 0
4075 out_data(2035).data = 5283
4076 out_data(2035).tlast = 0
4077 out_data(2036).data = -2483
4078 out_data(2036).tlast = 0
4079 out_data(2037).data = -13174
4080 out_data(2037).tlast = 0
4081 out_data(2038).data = 1546
4082 out_data(2038).tlast = 0
4083 out_data(2039).data = 6735
4084 out_data(2039).tlast = 0
4085 out_data(2040).data = 4885
4086 out_data(2040).tlast = 0
4087 out_data(2041).data = 5684
4088 out_data(2041).tlast = 0
4089 out_data(2042).data = -6482
4090 out_data(2042).tlast = 0
4091 out_data(2043).data = -8695
4092 out_data(2043).tlast = 0
4093 out_data(2044).data = -4629
4094 out_data(2044).tlast = 0
4095 out_data(2045).data = 15267
4096 out_data(2045).tlast = 0
4097 out_data(2046).data = -12433
4098 out_data(2046).tlast = 0
4099 out_data(2047).data = 8691
4100 out_data(2047).tlast = 1
4101 INFO: [SIM 1] CSim done with 0 errors.
4102 INFO: [SIM 1] ***** CSIM Finish *****
```

Synthesis Report :



Synthesis Report for 'counter'

General Information

Date: Thu May 18 12:31:16 2023
Version: 2019.2 (Build 2704478 on Wed Nov 06 22:10:23 MST 2019)
Project: dds_fft_hls
Solution: solution1
Product Family: rynopplus
Target device: xczu28dr-ffvg1517-2-e

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	2.007 ns	1.25 ns

Latency

Summary

Latency (cycles)	Latency (absolute)	Interval (cycles)		
min	max	min	max	Type
?	?	?	?	?none

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM	18KDSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	65	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	39	-
Register	-	-	35	-	-
Total	0	0	35	104	0
Available	2160	4272850560	425280	80	0
Utilization (%)	0	0	-0	-0	0

Detail

Instance

DSP48E

Memory

FIFO

Expression

Multiplexer