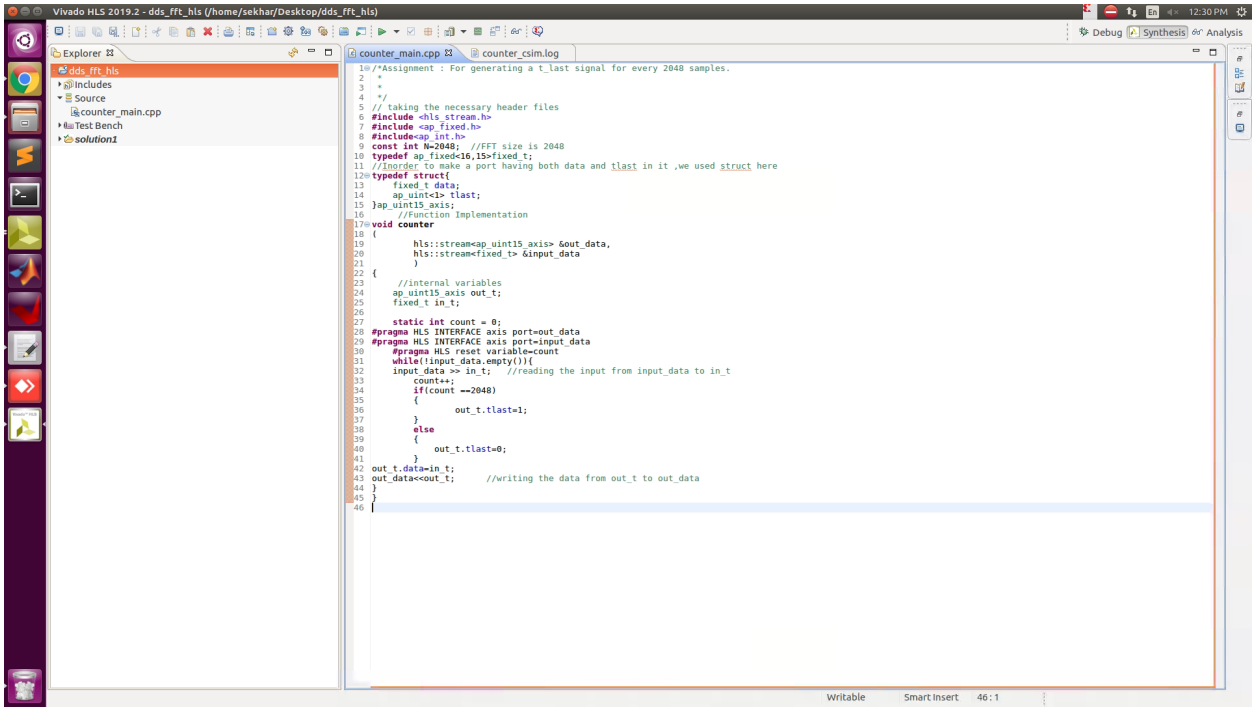
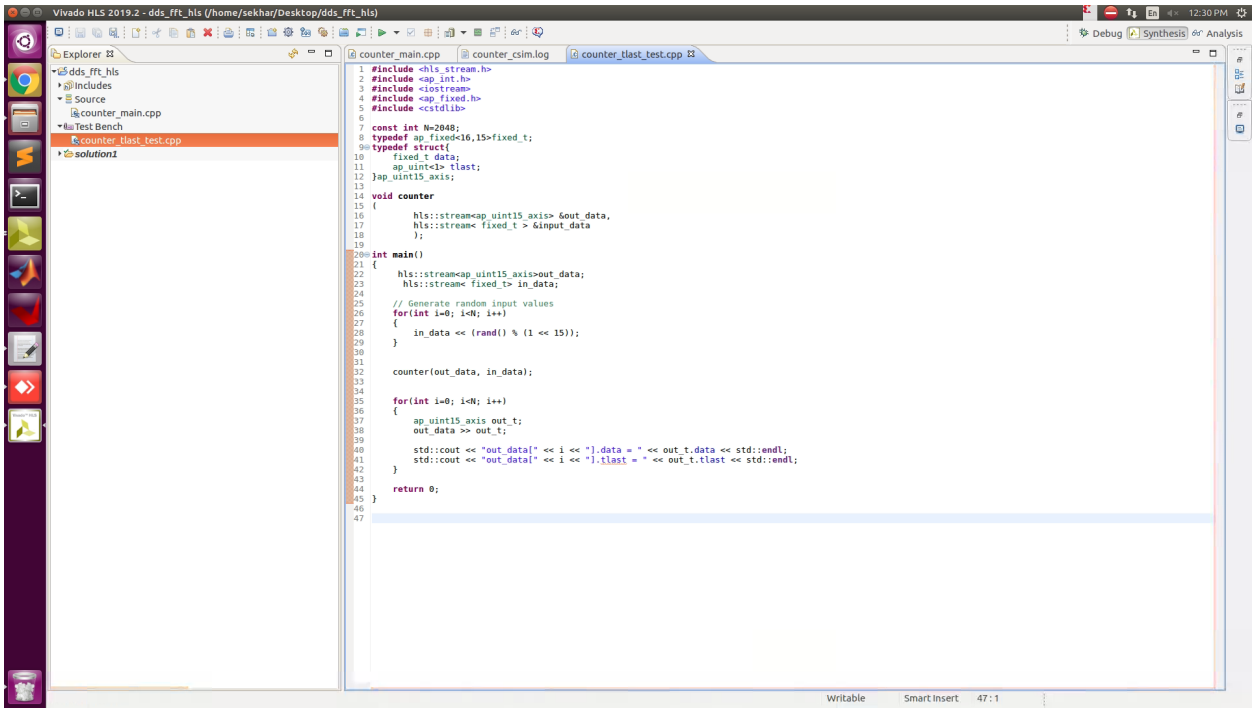
Assignment-10

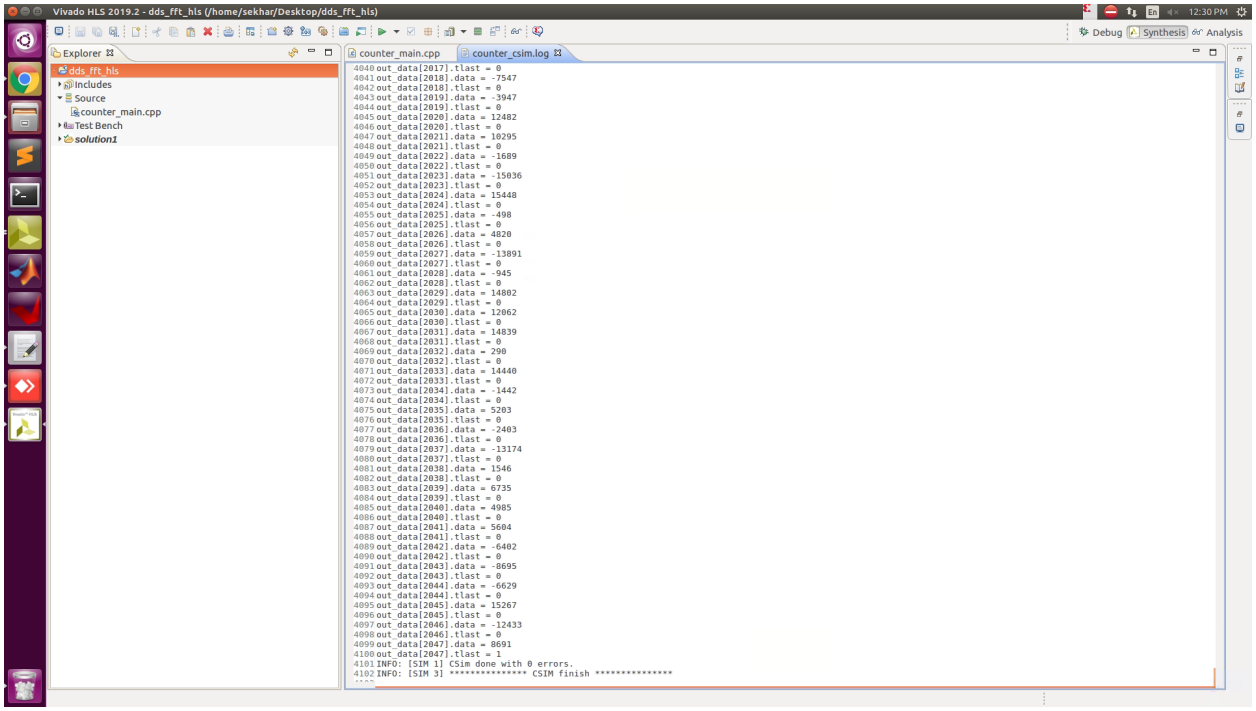
As a part of Using Xilinx FFT IP in the design, I implemented this IP for tlast signal .

Simulation :





Result :



Synthesis Report :