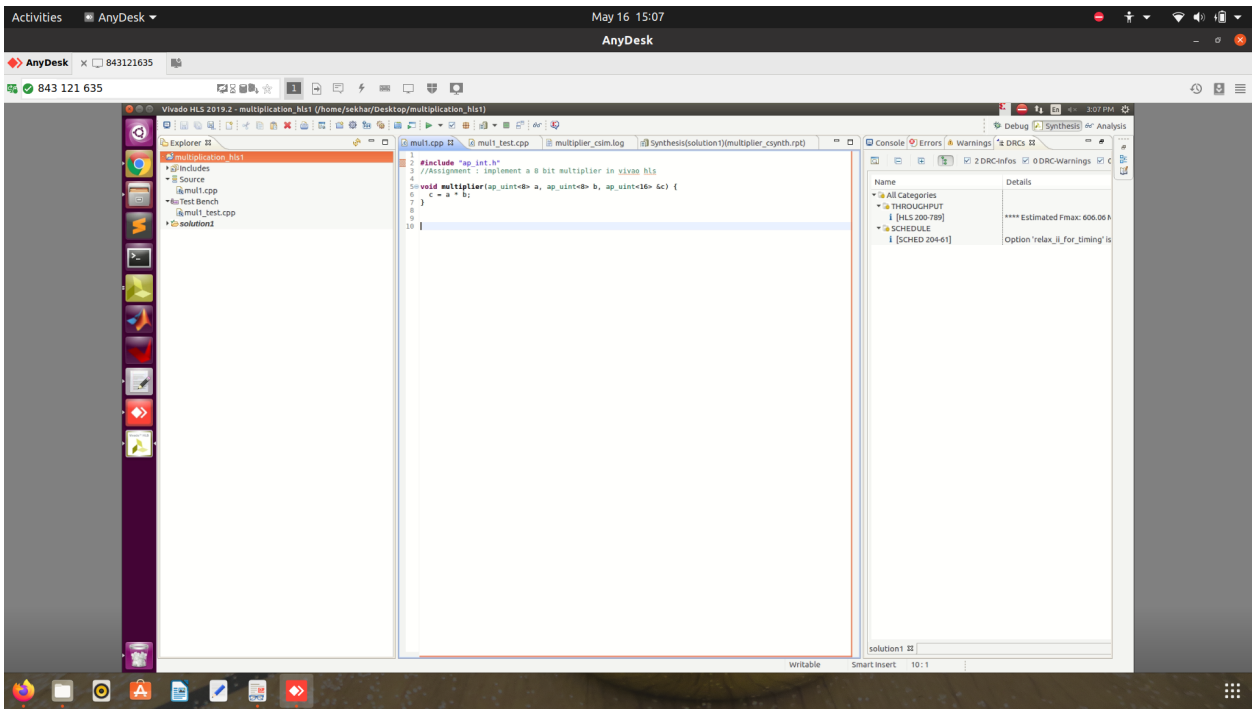
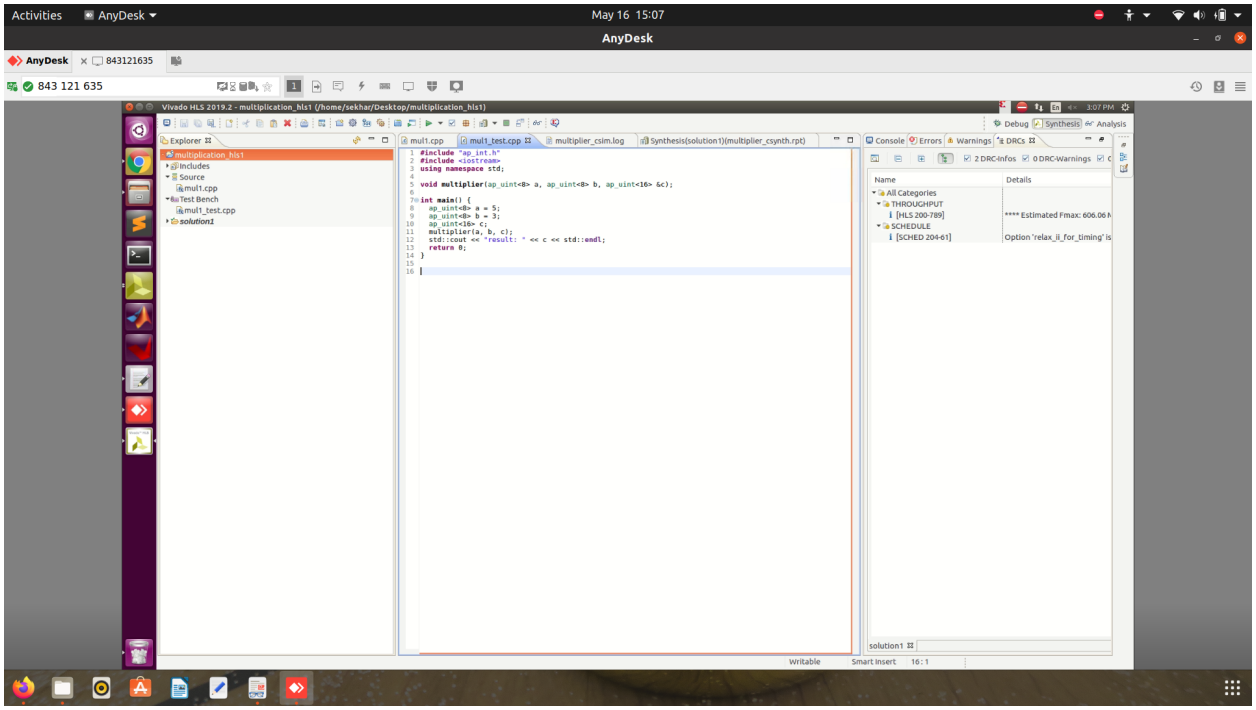
Assignment-1

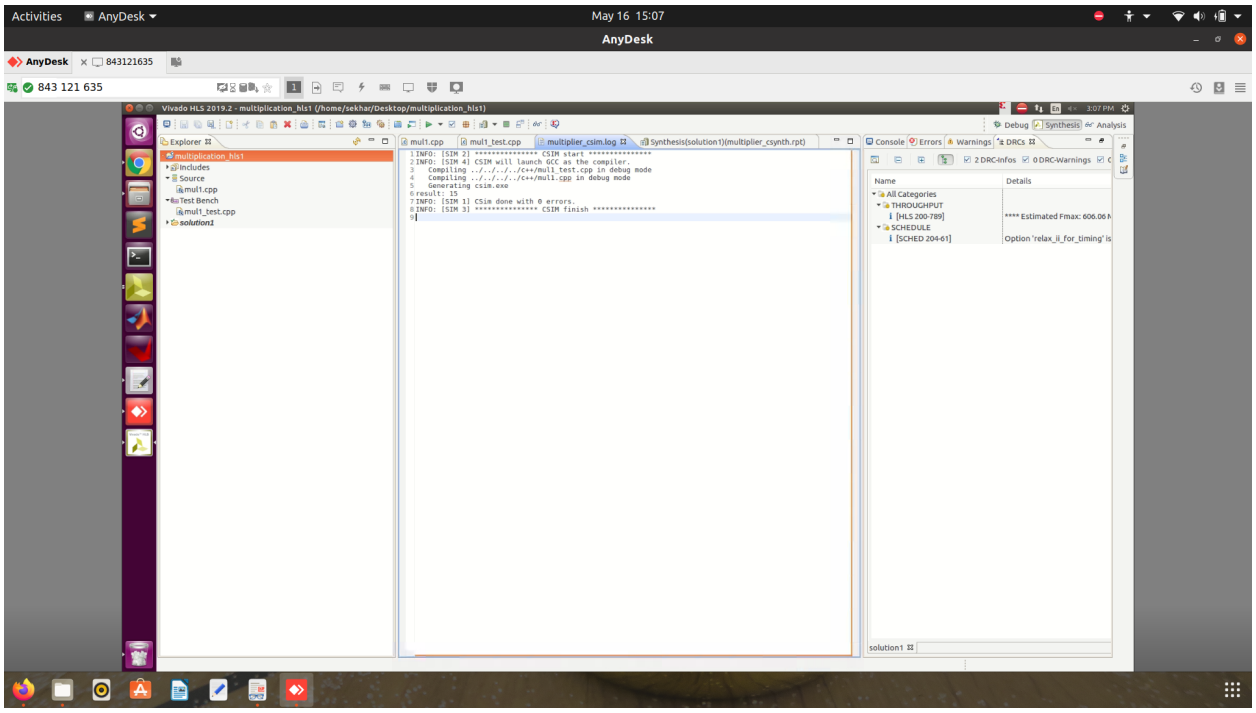
Design an 8X8 multiplier circuit

Simulation :

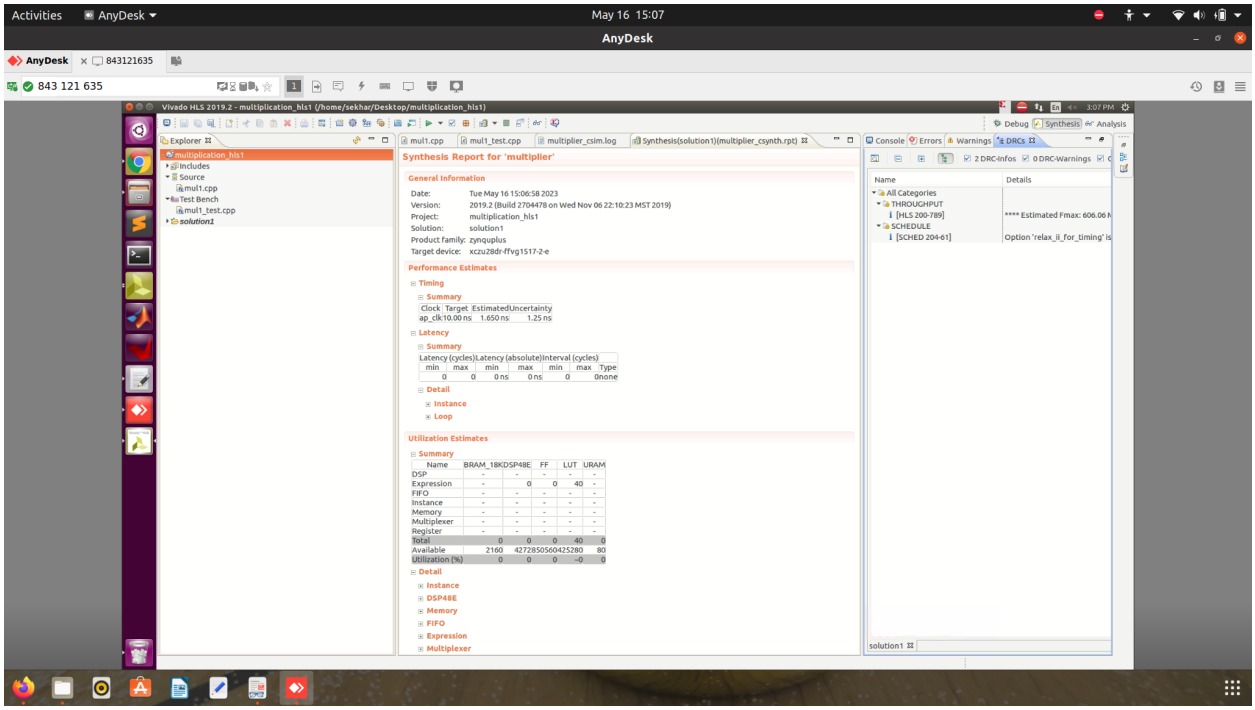




Result :



Synthesis Report :


Activities
AnyDesk
May 16 15:07
AnyDesk
843 121 635
Vivado HLS 2019.2 - multiplication_hls1 (/home/sekhar/Desktop/multiplication_hls1)
Explorer
multiplication_hls1
Includes
Source
mul1.cpp
Test Bench
mul1_test.cpp
solution1
mul1.cpp
mul1_test.cpp
multiplier_csim.log
Synthesis(solution1)(multiplier_csynth.rpt)
Synthesis Report for 'multiplier'
General Information
Date: Tue May 16 15:06:58 2023
Version: 2019.2 (Build 2704478 on Wed Nov 06 22:10:23 MST 2019)
Project: multiplication_hls1
Solution: solution1
Product family: zynquplus
Target device: xczu28dr-ffvg1517-2-e
Performance Estimates
Timing
Summary
Clock Target Estimated Uncertainty
ap_clk 10.00 ns 1.650 ns 1.25 ns
Latency
Summary
Latency (cycles) Latency (absolute) Interval (cycles)
min max min max min max Type
0 0 0 ns 0 ns 0 0 none
Detail
Instance
Loop
Utilization Estimates
Summary
Name BRAM_18K DSP48E FF LUT URAM
DSP - - - - -
Expression - - 0 0 40 -
FIFO - - - - - -
Instance - - - - - -
Memory - - - - - -
Multiplexer - - - - - -
Register - - - - - -
Total 0 0 0 0 40 0
Available 2160 4272850560425280 80
Utilization (%) 0 0 0 0 0 0
Detail
Instance
DSP48E
Memory
FIFO
Expression
Multiplexer
Console
Errors
Warnings
DRCs
2 DRC-Infos
0 DRC-Warnings
Name
Details
All Categories
THROUGHPUT
[HLS 200-789]
**** Estimated Fmax: 606.06 M
SCHEDULE
[SCHED 204-61]
Option 'relax_ii_for_timing' is
solution1