Create a digital circuit for a loadable UP/DOWN counter using Verilog HDL.

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Problem Statement

Create a digital circuit for a loadable UP/DOWN counter with customizable bitwidth using Verilog HDL.

🎯 Requirements

Phase - 1
Use a one-bit signal to control the counter to perform UP or DOWN counting.
Use a one-bit signal to load the counter register with an external input value. Use configurable bitwidth for the ‘load_value’ port.
Use 32 bits as the default bitwidth for the counter register.
Phase - 2
Internally add a maximum and minimum count values for the counter to wrap-around a set of values only.
Phase - 3
Add START, STOP, PAUSE, CONTINUE options to this circuit.

🚚 Deliverables

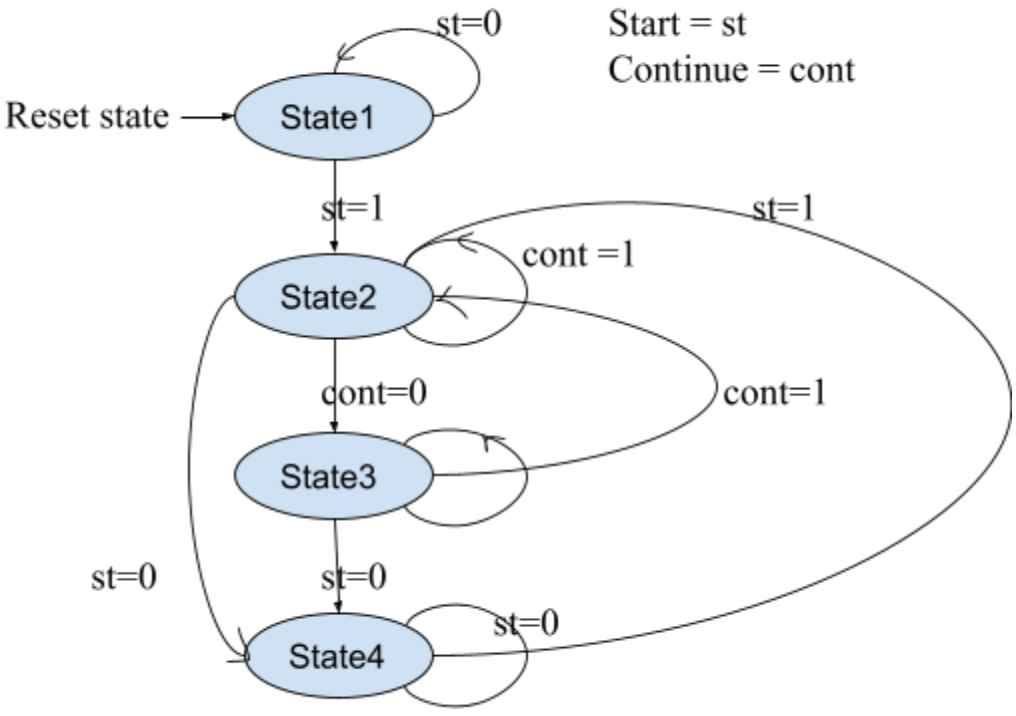
Source and testbench files
Document for the design and user guide
-Explain the implementation part
-Add simulation results
-Add synthesis results

Solution Approach

- As per the given requirements , we need a 1 bit signal to count up or down and another 1 bit signal to load the counter with external input value .
- If the load signal is high the counter is assigned with an external load value .
- Else we can check for up /down signal to count up or down .
- And if the start signal is high we can start the counting, else stop .
- If continue is high , continue to count else pause counting .

Code Implementation

- I implemented the code using FSM that contains one combinational and 2 sequential blocks .
- In the combinational block I used case statements for the state transitions .
- State Diagram



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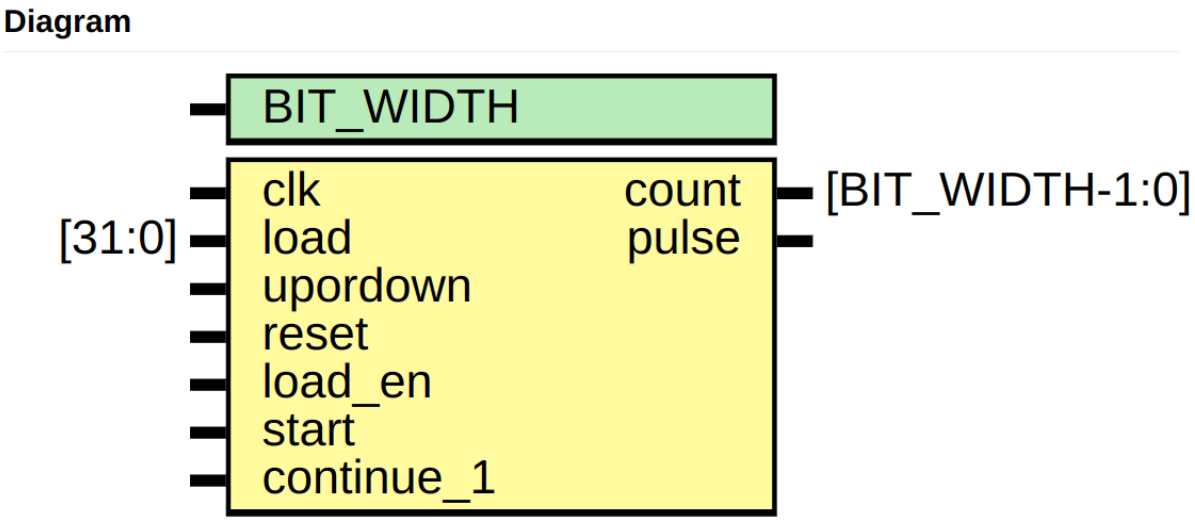
- One sequential block is for next_state transition and reset state .
- One sequential block is for output logic .
- For customizable width used parameters .

RTL simulation

Block Diagram



Test results :

Inputs : reset = active high for 10 clock cycles , load_enable =1 , upordown =1 , load= 32'd100

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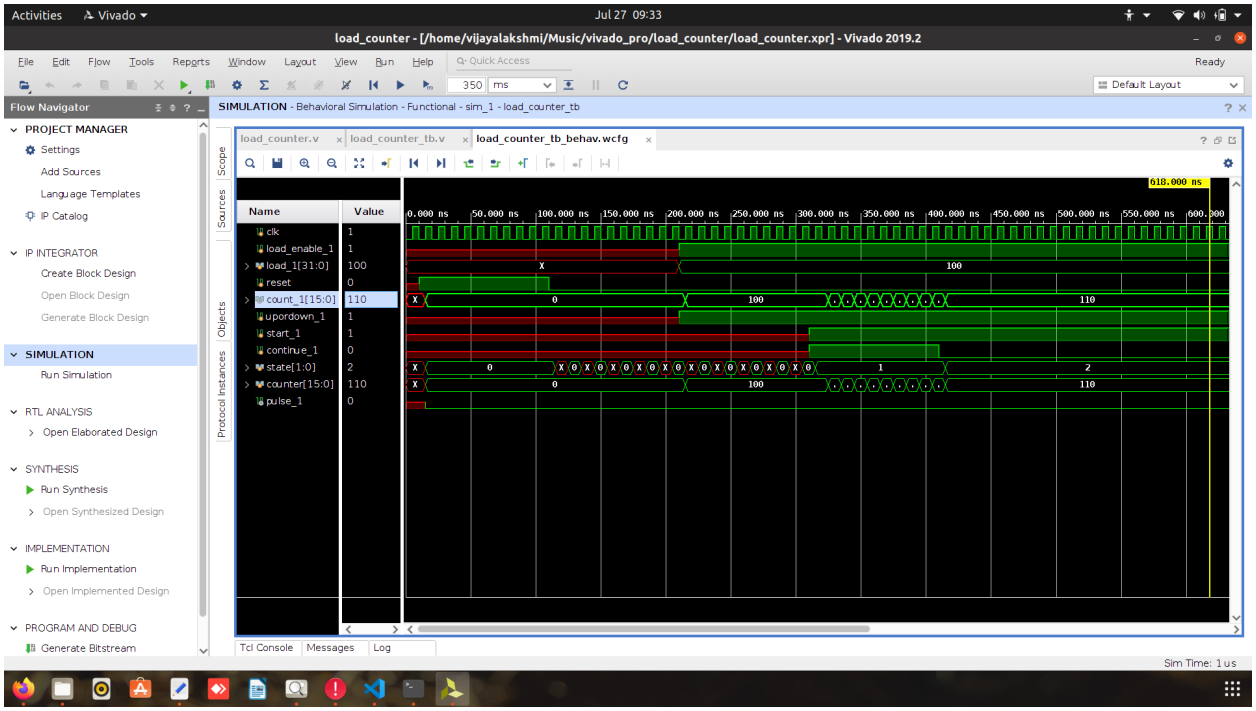

Conclusion

- I designed digital circuit for a loadable UP/DOWN counter with customizable bitwidth using Verilog HDL.