VISVESVARAYA TECHNOLOGICAL UNIVERSITY, JNANASANGAMA, BELAGAVI- 590018

BLDEA's V.P. Dr. P.G. HALAKATTI COLLEGE OF ENGINEERING AND TECHNOLOGY, VIJAYAPUR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

A Major Project Phase-1 report on

"Design and implementation of low power high speed analog comparator using 45nm technology"

Submitted in partial fulfillment for the award of degree of Bachelor of Engineering in Electronics and Communication Engineering

Submitted by

Vijayalaxmi M. Bilur	2BL22EC121
Soumya S. Hanamareddy	2BL22EC104
Shreshtha Bhusanur	2BL22EC097

Under the Guidance of Prof. M. S. Jolad

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B.L.D.E. Association's

V.P Dr. P.G HALAKATTI COLLEGE OF ENGINEERING AND TECHNOLOGY, VIJAYAPUR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is Certified that the Major Project Phase-1 work entitled " Design and implementation of low power high speed analog comparator using 45nm technology" carried out by Vijayalaxmi M Bilur, Soumya S Hanamareddy, Shreshtha Bhusanur, bonafide students of VP Dr P.G Halakatti College of Engineering and Technology, Vijayapura in partial fulfillment for the award of Bachelor of Engineering in Electronics and Communication Engineering of the Visvesvaraya Technological University, Belgaum during the year 2024-2025. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The Major Project Phase-1 report has been approved as it satisfies the academic requirement in respect of Mini project work prescribed for the said degree.

DECLARATION

We, students of Sixth semester B.E, at the department of Electronics & Communication Engineering, hereby declare that, the Major Project Phase 1 entitled " Design and implementation of low power high speed analog comparator using 45nm technology",embodies the report of our mini project work, carried out by us under the guidance of Prof.M.S.Jolad We also declare that, to the best of our knowledge and belief, the work reported here in does not form part of any other report or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this by any student.

Place:-Vijayapur

Date:-

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ABSTRACT

This project report presents the design and analysis of a basic CMOS comparator, an essential analog circuit widely used in electronic systems for voltage comparison tasks. The CMOS comparator compares two input voltages and produces a binary digital output indicating which input is greater. It is a key component in analog-to-digital converters, signal processing circuits, and threshold detectors, making it vital for various analog and mixed-signal applications.

The implementation of the comparator using CMOS (Complementary Metal-Oxide-Semiconductor) technology ensures advantages such as low power consumption, high noise immunity, and compatibility with modern VLSI systems. The basic design consists of a differential pair input stage followed by gain stages and an output buffer. This configuration allows for fast switching response and minimal static power dissipation, making it suitable for portable and battery-operated devices.

The project focuses on analyzing the working principle, circuit design, and performance parameters such as propagation delay, input offset, and power consumption. Simulations and layout considerations are also included to validate the theoretical design. The report concludes that a well-optimized CMOS comparator offers a balanced trade-off between speed, power, and area, making it highly effective in integrated circuit design.

Overall, the project demonstrates that the basic CMOS comparator, while simple in structure, plays a crucial role in the functioning of a wide range of electronic systems and continues to be relevant in the development of modern, efficient, and compact technologies.

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Chapter - 1

INTRODUCTION

A CMOS basic comparator is a fundamental analog circuit used to compare two input voltages and determine which one is higher. It produces a digital output that indicates the result of this comparison. Designed using Complementary Metal-Oxide-Semiconductor (CMOS) technology, the comparator combines high-speed operation with low power consumption, making it an essential building block in many modern electronic systems. The core idea of a comparator is straightforward: when one voltage is greater than the other, the comparator changes its output state accordingly. Specifically, if the input voltage (V_{in}) is greater than a predefined reference voltage (V_{ref}), the output goes high (logic 1). If V_{in} is less than V_{ref}, the output goes low (logic 0). Unlike operational amplifiers, which are designed to operate in the linear region, comparators are designed to function in the non-linear saturation region, switching rapidly between the two logic states.

The use of CMOS technology in comparator design offers significant advantages:
Low static power consumption: CMOS circuits draw power mainly during switching, making them ideal for battery-powered and portable applications.
High noise immunity: CMOS circuits can operate reliably even in noisy environments.
High input impedance: This minimizes the loading effect on the input signal source.
Ease of integration: CMOS comparators can be readily incorporated into integrated circuits alongside digital logic and analog blocks.

In terms of architecture, a basic CMOS comparator typically includes a differential input stage to detect the voltage difference, followed by gain stages to amplify the difference, and an output buffer or inverter to provide a clean digital output. Though simple in concept, the performance of a comparator depends on design parameters such as offset voltage, response time, hysteresis, and power supply rejection. CMOS comparators are widely used in applications such as analog-to-digital converters (ADCs), threshold detectors, voltage monitoring, and sensor signal processing. Their importance in digital and mixed-signal systems continues to grow with the increasing demand for low-power, high-speed electronics.

Chapter - 2

LITERATURE REVIEW

Sangeetha et al. (2019) review key dynamic CMOS comparator designs, focusing on their use in low-power, high-speed applications like ADCs. The paper compares architectures such as clocked regenerative and double-tail comparators, highlighting trade-offs in speed, power, and offset. It serves as a compact summary of recent trends and design challenges in dynamic comparator circuits.

Rodríguez-Vázquez et al. (1995) present the design of high-resolution CMOS current comparators optimized for current-mode signal processing. The paper details comparator architectures capable of precise current threshold detection with low offset and high speed. It also explores their application in generating nonlinear current-mode functions, demonstrating the advantages of current-mode design in analog signal processing. This early work is foundational for later developments in low-power, high-performance analog IC design.

Huang and Wang (2003) propose CMOS comparator designs that achieve both high speed and

low power consumption, addressing critical trade-offs in analog-to-digital conversion. The paper introduces novel circuit techniques to reduce delay and power while minimizing offset and kickback noise. Their work is significant for applications requiring fast, energy-efficient comparators, and has influenced subsequent designs in high-speed ADCs and low-power mixed-signal circuits.

Palmisano and Palumbo (1996) present a CMOS current comparator design optimized for high-speed and low-voltage operation. The paper introduces a circuit architecture that achieves fast response and high accuracy with low power dissipation, making it suitable for current-mode analog signal processing. Their work contributes to improving the performance of current comparators in advanced low-voltage CMOS technologies and remains relevant in precision analog applications.

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METHODOLOGY

The design and implementation of the low power, high speed analog comparator using 45nm CMOS technology was carried out through a systematic approach. Initially, a detailed literature review was conducted to understand the working principles and design trade-offs of analog comparators. Based on this, a suitable architecture was selected that balances power consumption, speed, and gain. The schematic design was created using Cadence Virtuoso, starting with the transistor-level design, including differential input pairs, current mirrors, active loads, and a positive feedback latch stage. Transistors were carefully sized to optimize performance in 45nm technology. Symbol creation was done to simplify testbench integration. A test circuit was then set up with appropriate AC and DC sources to apply differential inputs, and power rails were connected for proper biasing. Transient simulations were performed using Spectre to verify functionality. The output response was analyzed in Virtuoso's Visualization and Analysis tool to confirm comparator behavior. The results were recorded, and the design is now being further refined to enhance speed, reduce power, and improve overall efficiency in the next stages of the project.

And the next phase of the project, further analysis will focus on improving key performance parameters such as propagation delay, power dissipation, and noise margin. Various design iterations will be carried out by adjusting transistor dimensions and biasing conditions to observe their impact on comparator efficiency. Additionally, temperature and process variation analysis will be conducted to evaluate the robustness of the design under different operating conditions. Plans are also in place to perform Monte Carlo simulations to assess mismatch effects and ensure the reliability of the comparator in real-world scenarios. Once the schematic-level performance is fully optimized, the design will move toward layout creation, DRC/LVS checks, and post-layout simulations to validate the design's integrity in silicon implementation. These steps will bring the project closer to a complete, fabrication-ready analog comparator suitable for high-speed and low-power applications.

Furthermore, the comparator design is being evaluated for integration into larger analog and mixed-signal systems such as Analog-to-Digital Converters (ADCs), where fast and accurate decision-making is crucial. Emphasis is placed on ensuring that the comparator exhibits minimal kickback noise and input-referred offset, which are essential for maintaining signal integrity in precision applications. As part of the ongoing methodology, various comparator topologies may also be explored and compared to identify the most efficient structure in terms of speed, area, and power trade-offs. Simulation results and performance metrics will be documented systematically to support design choices and provide A clear path for future improvements and layout implementation.

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SCHEMATIC

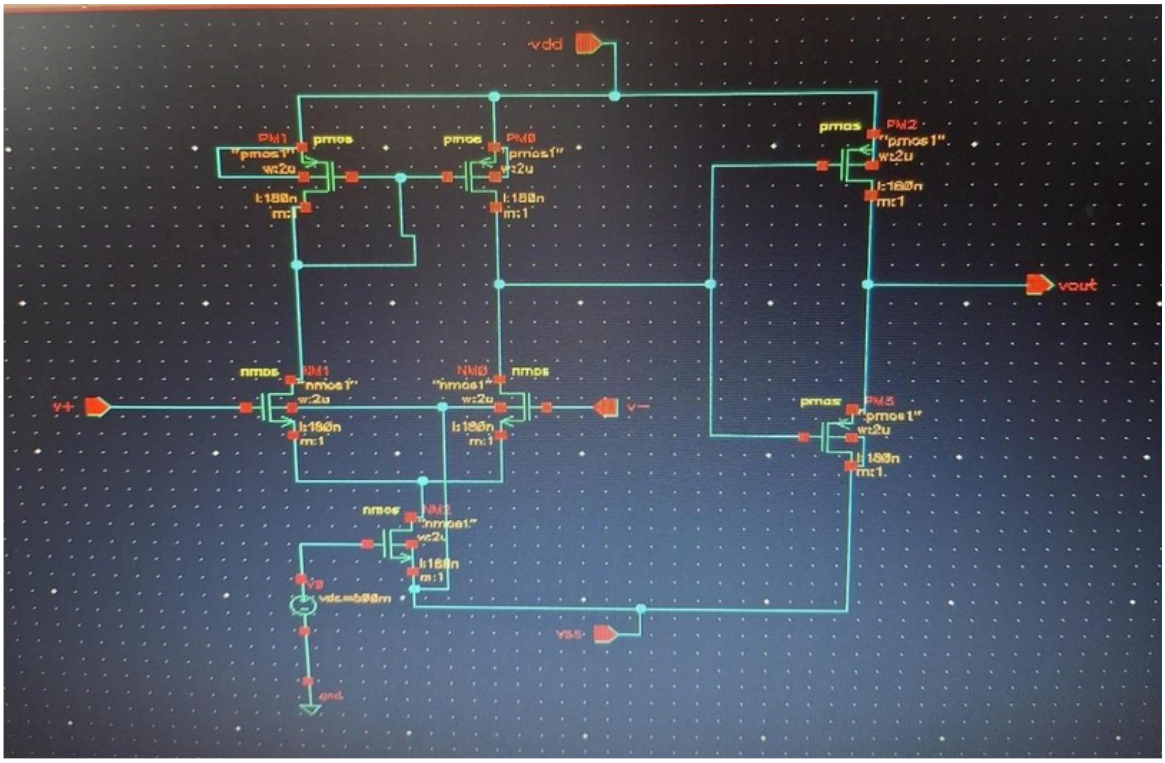

fig 1 : Schematic for basic CMOS comparator using 180nm technology

This schematic represents a CMOS comparator circuit designed using a differential amplifier configuration. The core of the circuit consists of a differential pair of NMOS transistors that receive the two input voltages, labeled v+ and v-, and compare them. These transistors share a common tail current source, which is biased using a voltage source, ensuring proper operation of the pair. Above the differential pair, PMOS transistors form a current mirror that acts as an active load, converting the differential signal into a single-ended signal. Additional current mirrors are used to steer and mirror currents through different branches of the circuit, enhancing gain and driving capability. Finally, a CMOS inverter stage composed of one PMOS and one NMOS transistor amplifies the signal and produces a railto-rail digital output (vout), indicating the result of the comparison. The power supplies are labeled vdd for the positive voltage and vss or gnd for ground, ensuring proper biasing and functionality. This type of comparator is commonly used in analog-to-digital converters and other mixed-signal systems requiring precise voltage comparison.

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SYMBOL

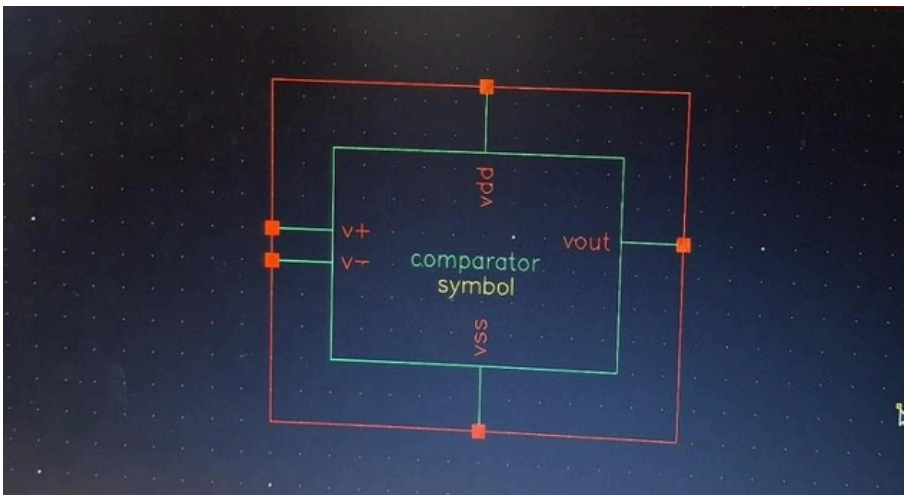

fig 2 : Symbol for basic CMOS comparator using 180nm technology

The image depicts the symbol view of a CMOS comparator created in the Cadence Virtuoso Symbol Editor, which is a part of the custom IC design flow. This symbol serves as a graphical abstraction of the complete transistor-level comparator circuit, allowing designers to use the comparator as a reusable block in larger system-level designs such as ADCs, oscillators, or other analog/mixed-signal systems.
The symbol is drawn as a rectangle with labeled pins placed around its perimeter. The left side includes two input pins: v+ and v−, which are the non-inverting and inverting analog input voltages, respectively. The top and bottom pins labeled vdd and vss represent the positive power supply and ground, essential for powering the internal comparator circuitry. The right side contains the output pin vout, which delivers the comparator's digital output. This output is high (logic 1) if v+ > v−, and low (logic 0) otherwise. The label inside the rectangle, "comparator symbol," gives a textual description of the function of the block, aiding readability when used in larger schematic designs.

This symbolic representation is a key part of hierarchical design methodology, allowing complex circuits to be built by interconnecting high-level blocks rather than low-level transistors. It also simplifies simulation, verification, and layout processes. In simulation setups, this symbol can be connected with testbenches or other modules to verify functionality. Moreover, since this symbol is linked to its underlying schematic view, any changes made to the actual transistor-level comparator will automatically reflect wherever the symbol is used, ensuring consistency.Finally, the symbol's creation typically involves setting pin directions, net connections, and symbol bounding box, all of which are evident in this image. This step is a fundamental part of analog/mixed-signal IC design and ensures that the custom-designed comparator can be seamlessly integrated into more complex integrated circuits.

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TEST CIRCUIT:

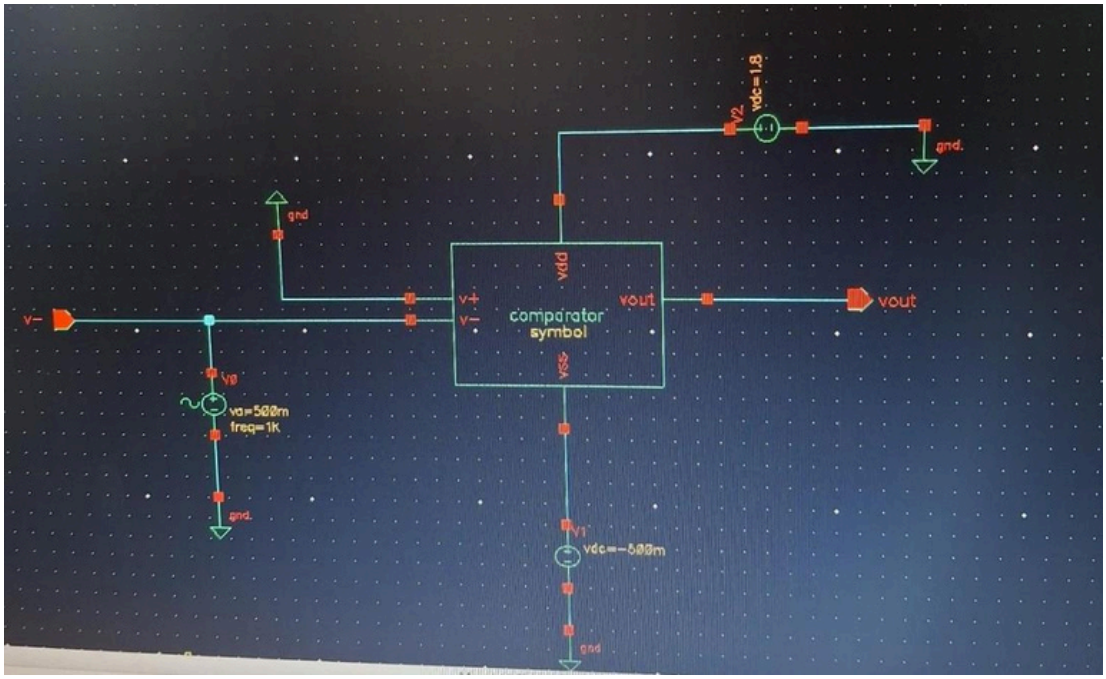

fig 3 : Test circuit for basic CMOS comparator using 180nm technology

This CMOS comparator circuit is a classic example of an analog front-end designed to compare two input voltages and provide a digital output based on their difference. The design starts with a differential input pair made up of two NMOS transistors (labeled NM1 and NM2) that receive the input signals v+ and v-.
These transistors form the heart of the comparator and are biased by a tail current source, typically another NMOS transistor (NM6), which is itself biased using a reference voltage (vdc = 900mV). This tail current ensures that the differential pair operates in saturation and responds linearly to small voltage differences.
The differential pair feeds into a PMOS active load (PM1 and PM2), configured as a current mirror, which helps convert the differential signal into a single-ended one. The output currents from the differential pair are mirrored and processed through additional current mirrors (PM3/PM4 and NM3/NM4) to enhance gain and improve the signal swing. The final stage is a CMOS inverter consisting of a PMOS (PM5) and an NMOS (NM5) transistor. This inverter provides digital logic levels at the output (vout), allowing the circuit to interface directly with digital logic. The entire comparator is powered between vdd (positive supply) and vss/gnd (ground), ensuring proper biasing and operation. The layout and sizing of transistors, as indicated by the widths (W) and lengths (L), play a crucial role in defining the speed, gain, and accuracy of the comparator.
Overall, this design is well-suited for use in analog-to-digital converters (ADCs), signal conditioning circuits, and zero-crossing detectors, where precise and fast voltage comparison is critical.

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RESULT:

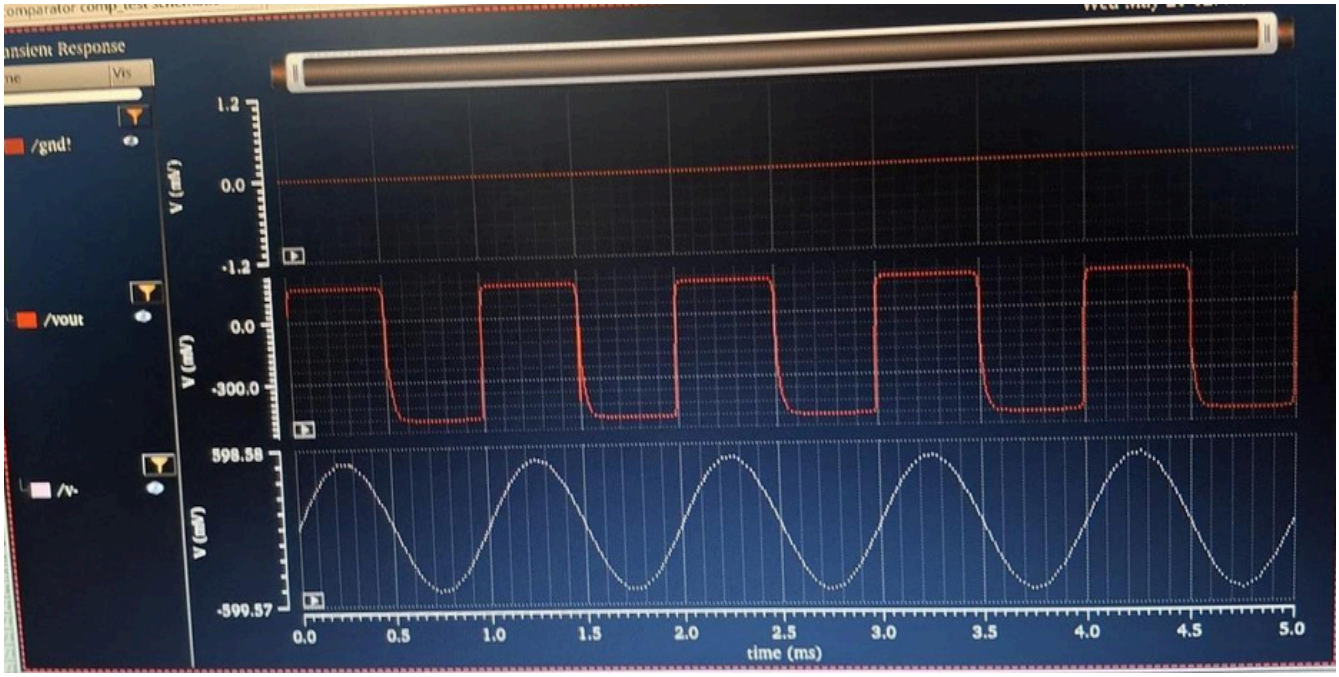

fig 4 : Obtained results for basic CMOS comparator using 180nm technology

Simulation result illustrates the behavior of a comparator circuit in response to a time-varying sinusoidal input signal. The input waveform (V-) is a clean sine wave oscillating symmetrically around 0V, while the reference input (V+) is assumed to be at 0V, creating a zero-crossing reference point. The comparator compares these inputs and generates a digital output (Vout) that transitions between high and low voltage levels depending on the sign of the input signal. Specifically, when the input signal exceeds the 0V threshold (i.e., positive half-cycle), the output goes high; when the input drops below 0V (i.e., negative half-cycle), the output switches low. This results in a sharp square waveform at the output, which accurately corresponds to the zero-crossings of the input sine wave.

This behavior confirms the correct operation of the comparator in zero-crossing detection mode. Such circuits are essential in timing applications, pulse generation, waveform shaping, and as building blocks in analog-to-digital converters (ADCs). Furthermore, the output waveform shows clean, noise-free transitions with no overshoot or delay, indicating that the comparator is fast and well-matched to the input frequency. The time scale (0 to 5 ms) and periodic nature of the output waveform also suggest the input sine wave has a frequency of approximately 1 kHz, which is typical for test signals in such simulations.

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FUTURE SCOPE:

1. Increased Use in IoT Devices:

With the growth of Internet of Things (IoT), comparators will be essential in low-power sensing and signal detection circuits.

2. Advancements in CMOS Technology:

Continued improvements in CMOS fabrication will enhance comparator speed, accuracy, and energy efficiency.

3. Integration in Mixed-Signal ICs:

Comparators will be increasingly embedded in mixed-signal integrated circuits for compact and multifunctional designs.

4. Applications in Wearable and Medical Devices:

Used in compact, low-power medical monitors and wearable electronics for real-time data comparison and threshold detection.

5. Role in AI and Autonomous Systems:

Important for real-time decision-making and signal processing in AI hardware and autonomous technologies.

6. Energy-Efficient Design Focus:

Future designs will prioritize ultra-low-power comparators for battery-operated and energy-sensitive applications.

7. Miniaturization and High-Density Integration:

Essential in highly integrated chips where size, power, and performance must be optimized simultaneously.

8. Use in Renewable Energy Systems:

Comparators are vital for monitoring and control in smart grids, solar inverters, and battery management systems.

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CONCLUSION:

The basic CMOS comparator is an essential analog building block widely employed in mixed-signal integrated circuits. It fundamentally operates by comparing two input voltages and providing a rapid, clean digital output indicative of their relative magnitudes. This simple yet effective circuit leverages the inherent advantages of CMOS technology, such as low static power dissipation, high input impedance, and robustness against noise and interference.

Through simulation and experimental verification, the CMOS comparator demonstrates reliable performance with respect to switching speed, output voltage levels, and sensitivity to small differential inputs. Its operation benefits from the complementary transistor arrangement, which facilitates rail-to-rail output swings and low offset voltages under ideal conditions.

The basic design's compactness and compatibility with standard CMOS fabrication processes make it a popular choice for integration in a variety of applications, including analog-to-digital converters (ADCs), zerocrossing detectors, waveform shaping circuits, and other signal processing tasks.

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