Synchronous Counters.

1. Determine the number of flip-flops needed.
   $2^n >$ number of states.
2. Choose the type of flip-flop.
3. Using the excitation table of selected flip-flop determine the excitation table for the counter.
4. Use k-map for simplification to derive the flip flop inputs.
5. Draw the logic diagram.

1. Design Mod-8 up counter using JK flip flop.

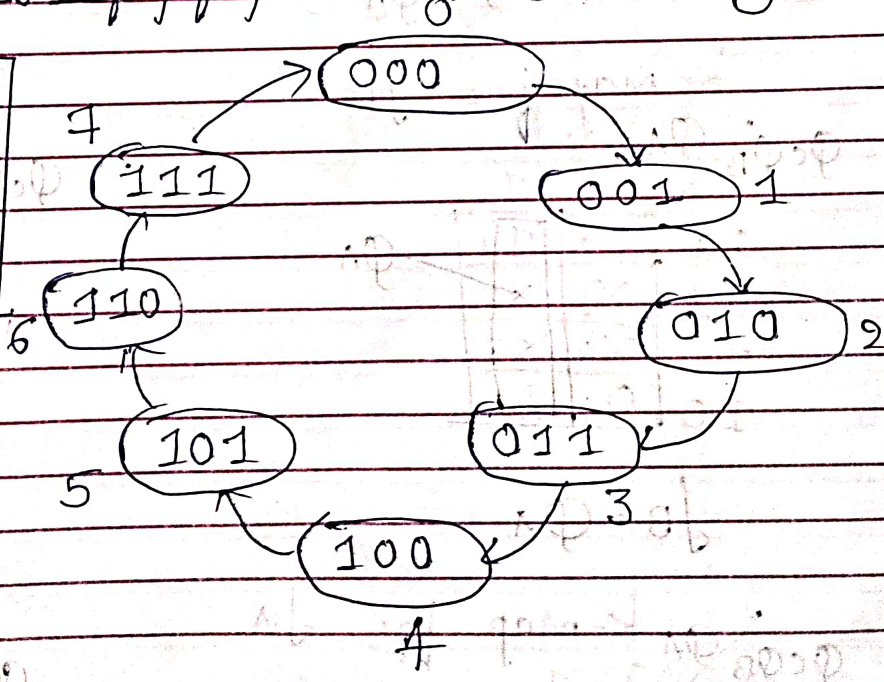
$2^n \geq 8, \quad 2^3 \geq 8, \quad 8 \geq 8$

3 flip-flop's required.

Excitation table for JK flip flop.

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

State diagram.



Excitation table for counter.

Present state MSB Q_C	Q_B	LSB Q_A	Next state Q_C^+	Q_B^+	Q_A^+	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

K-map for J_C

$Q_CQ_B \backslash Q_A$	0	1
00	0_0	0_1
01	0_2	1_3
11	X_6	X_7
10	X_4	X_5

Q_BQ_A

$J_C = Q_BQ_A$

K-map for K_C

$Q_CQ_B \backslash Q_A$	0	1
00	X_0	X_1
01	X_2	X_3
11	0_6	1_7
10	0_4	0_5

Q_BQ_A

$K_C = Q_AQ_B$

K-map for J_B

$Q_CQ_B \backslash Q_A$	0	1
00	0_0	1_1
01	X_2	X_3
11	X_6	X_7
10	0_4	1_5

Q_A

$J_B = Q_A$

K-map for K_B

$Q_CQ_B \backslash Q_A$	0	1
00	X_0	X_1
01	0_2	1_3
11	0_6	1_7
10	X_4	X_5

Q_A

$K_B = Q_A$

K-map for J_A

$Q_CQ_B \backslash Q_A$	0	1
00	1_0	X_1
01	1_2	X_3
11	1_6	X_7
10	1_4	X_5

1

$J_A = 1$

K-map for K_A

$Q_CQ_B \backslash Q_A$	0	1
00	X_0	1_1
01	X_2	1_3
11	X_6	1_7
10	X_4	1_5

1

$K_A = 1$

$J_C = K_C = Q_A Q_B$

$J_B = K_B = Q_A$

$J_A = K_A = 1$

Logic Circuit

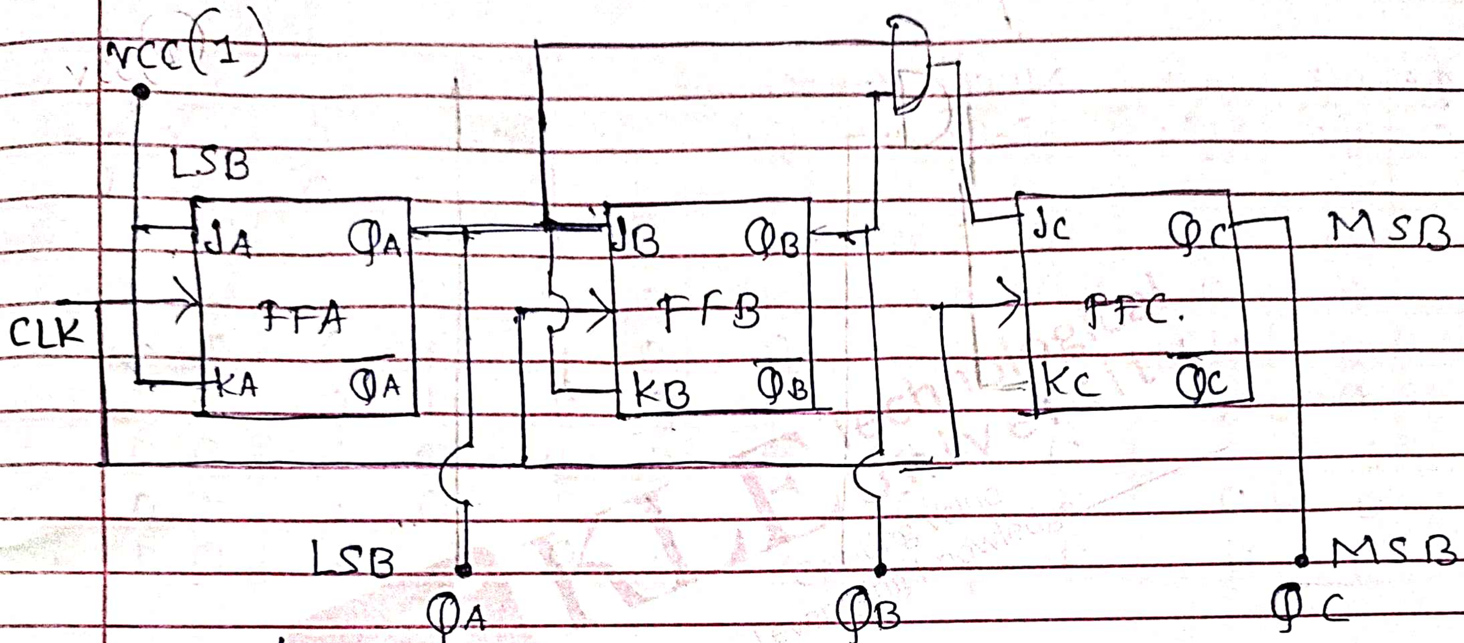


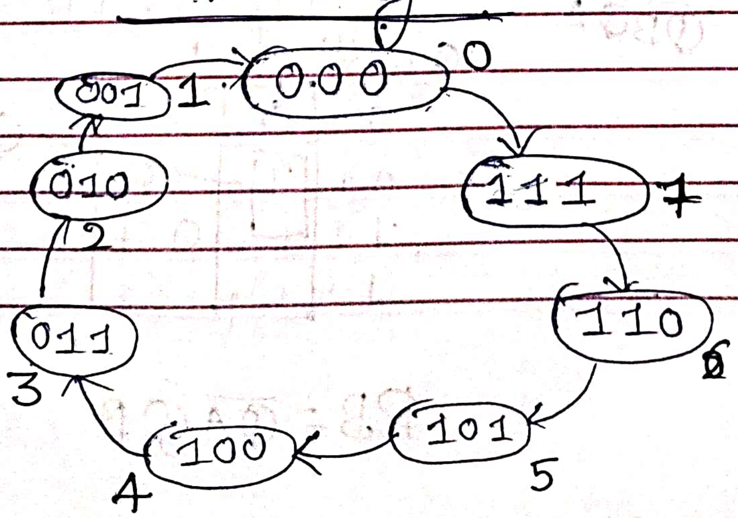
fig :- Mod-8 Sync up counter.

(2) Mod-8 down counter using SR flip flop

$2^n > 8$, $2^3 \geq 8$, $8 \geq 8$

3 SR flip flop's required.

State diagram.



Excitation table for SR flip flop

Q_t	Q_{t+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Excitation table for Counter

present state			Next state.								
Q_C	Q_B	Q_A	Q_C^{+1}	Q_B^{+}	Q_A^{+1}	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	1	1	1	1	0	1	0	1	0
0	0	1	0	0	0	0	X	0	X	0	1
0	1	0	0	0	1	0	X	0	1	1	0
0	1	1	0	1	0	0	X	X	0	0	1
1	0	0	0	1	1	0	1	1	0	1	0
1	0	1	1	0	0	X	0	0	X	0	1
1	1	0	1	0	1	X	0	0	1	1	0
1	1	1	1	1	0	X	0	X	0	0	1

K-map for SC

Q_CQ_B \ Q_A	0	1
00	1_0	0_1
01	0_2	0_3
11	X_6	X_7
10	0_4	X_5

$\overline{Q_A}\,\overline{Q_B}\,\overline{Q_C}$

SC =

K-map for RC

Q_CQ_B \ Q_A	0	1
00	0_0	X_1
01	X_2	X_3
11	0_6	0_7
10	1_4	0_5

$Q_C\overline{Q_B}\,\overline{Q_A}$

$RC = \overline{Q_A}\,\overline{Q_B}\,Q_C$

K-map for SB.

Q_CQ_B \ Q_A	0	1
00	1_0	0_1
01	0_2	X_3
11	0_6	X_7
10	1_4	0_5

$\overline{Q_B}\,\overline{Q_A}$

$SB = \overline{Q_A}\,\overline{Q_B}$

K-map for RB

Q_CQ_B \ Q_A	0	1
00	0_0	X_1
01	1_2	0_3
11	1_6	0_7
10	0_4	X_5

$Q_B\overline{Q_A}$

$RB = \overline{Q_A}\,Q_B$

K-map for SA

$Q_C Q_B$ \ Q_A	0	1
00	1_0	0_1
01	1_2	0_3
11	1_6	0_7
10	1_4	0_5

$\overline{Q_A}$

$S_A = \overline{Q_A}$

K-map for RA

$Q_C Q_B$ \ Q_A	0	1
00	0_0	1_1
01	0_2	1_3
11	0_6	1_7
10	0_4	1_5

Q_A

$R_A = \overline{Q_A}$

$S_C = \overline{Q_A}\,\overline{Q_B}\,Q_C$

$R_C = \overline{Q_A}\,\overline{Q_B}\,Q_C$

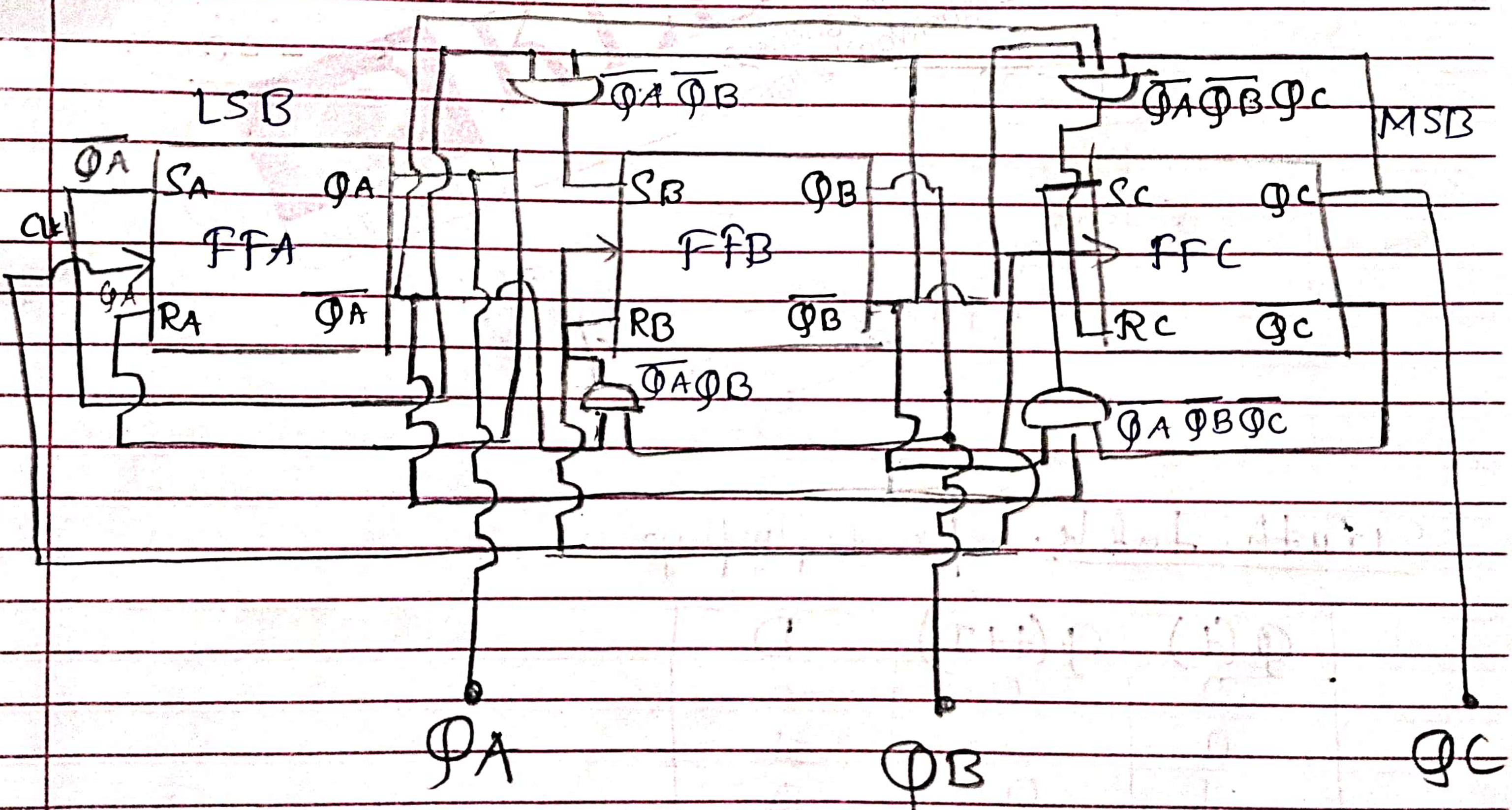
$S_B = \overline{Q_A}\,\overline{Q_B}$

$R_B = \overline{Q_A}\,Q_B$

$S_A = \overline{Q_A}$

$R_A = Q_A$

Logic Circuit



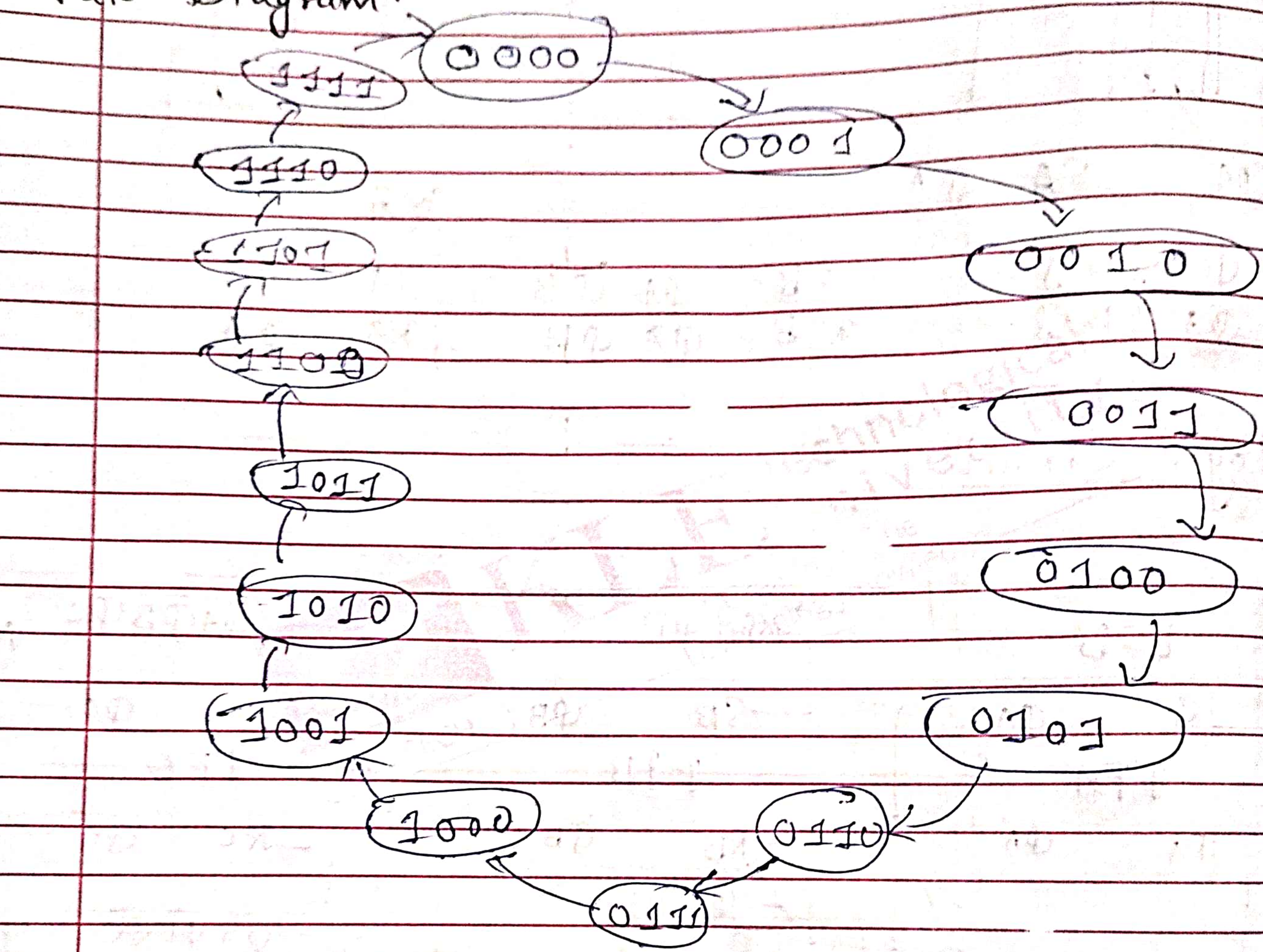
(3)

4-bit up counter using D flipflop

4-bit 4-D f/f's (up-counter 0-15)

Mod-16 counter.

State Diagram.



Excitation table. for D flipflop

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State				Next State							
ϕ_D	ϕ_C	ϕ_B	ϕ_A	ϕ_D^+	ϕ_C^+	ϕ_B^+	ϕ_A^+	D_D	D_C	D_B	D_A
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	1	0	0	1	1	0	0
1	1	0	0	1	1	0	1	1	1	0	1
1	1	0	1	1	1	1	0	1	1	1	0
1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	0	0	0	0	0	0	0	0

K-map for D_D

$\phi_D\phi_C \backslash \phi_B\phi_A$	00	01	11	10
00	0 (0)	0 (1)	0 (3)	0 (2)
01	0 (4)	0 (5)	1 (7)	0 (6)
11	1 (12)	1 (13)	0 (15)	1 (14)
10	1 (8)	1 (9)	1 (11)	1 (10)

$\overline{\phi_A}\phi_B\phi_C\phi_D$

$\phi_D\overline{\phi_A}$

$\phi_D\overline{\phi_C}$

$\phi_D\overline{\phi_B}$

$$= \phi_D\overline{\phi_C} + \phi_D\overline{\phi_B} + \phi_D\overline{\phi_A} + \overline{\phi_D}\phi_C\phi_B\phi_A$$

$$= \phi_D(\overline{\phi_C} + \overline{\phi_B} + \overline{\phi_A}) + \overline{\phi_D}(\phi_C\phi_B\phi_A)$$

$$= \phi_D(\overline{\phi_C\phi_B\phi_A}) + \overline{\phi_D}(\phi_C\phi_B\phi_A)$$

$$\boxed{D_D = \phi_D \oplus (\phi_C\phi_B\phi_A)}$$

K-map for D_C.

Q_DQ_C \ Q_BQ_A	00	01	11	10
00	0_{0}	0_{1}	1_{3}	0_{2}
01	1_{4}	1_{5}	0_{7}	1_{6}
11	1_{12}	1_{13}	0_{15}	1_{14}
10	0_{8}	0_{9}	1_{11}	0_{10}

$Q_C\overline{Q_A}$

$\overline{Q_C}Q_BQ_A$

$Q_C\overline{Q_B}$

$$D_C = Q_C\overline{Q_B} + Q_C\overline{Q_A} + \overline{Q_C}Q_BQ_A$$
$$= Q_C(\overline{Q_B} + \overline{Q_A}) + \overline{Q_C}(Q_BQ_A)$$
$$= Q_C(\overline{Q_BQ_A}) + \overline{Q_C}(Q_BQ_A)$$

$$\boxed{D_C = Q_C \oplus Q_BQ_A}$$

K-map for D_B

Q_DQ_C \ Q_BQ_A	00	01	11	10
00	0_{0}	1_{1}	0_{3}	1_{2}
01	0_{4}	1_{5}	0_{7}	1_{6}
11	0_{12}	1_{13}	0_{15}	1_{14}
10	0_{8}	1_{9}	0_{11}	1_{10}

$Q_B\overline{Q_A}$

$\overline{Q_B}Q_A$

$$D_B = \overline{Q_B}Q_A + Q_B\overline{Q_A}$$

$$\boxed{D_B = Q_A \oplus Q_B}$$

K-map for $D_{\cancel{B}A}$

Q_DQ_C \ Q_BQ_A	00	01	11	10
00	1_{0}	0_{1}	0_{3}	1_{2}
01	1_{4}	0_{5}	0_{7}	1_{6}
11	1_{12}	0_{13}	0_{15}	1_{14}
10	1_{8}	0_{9}	0_{11}	1_{10}

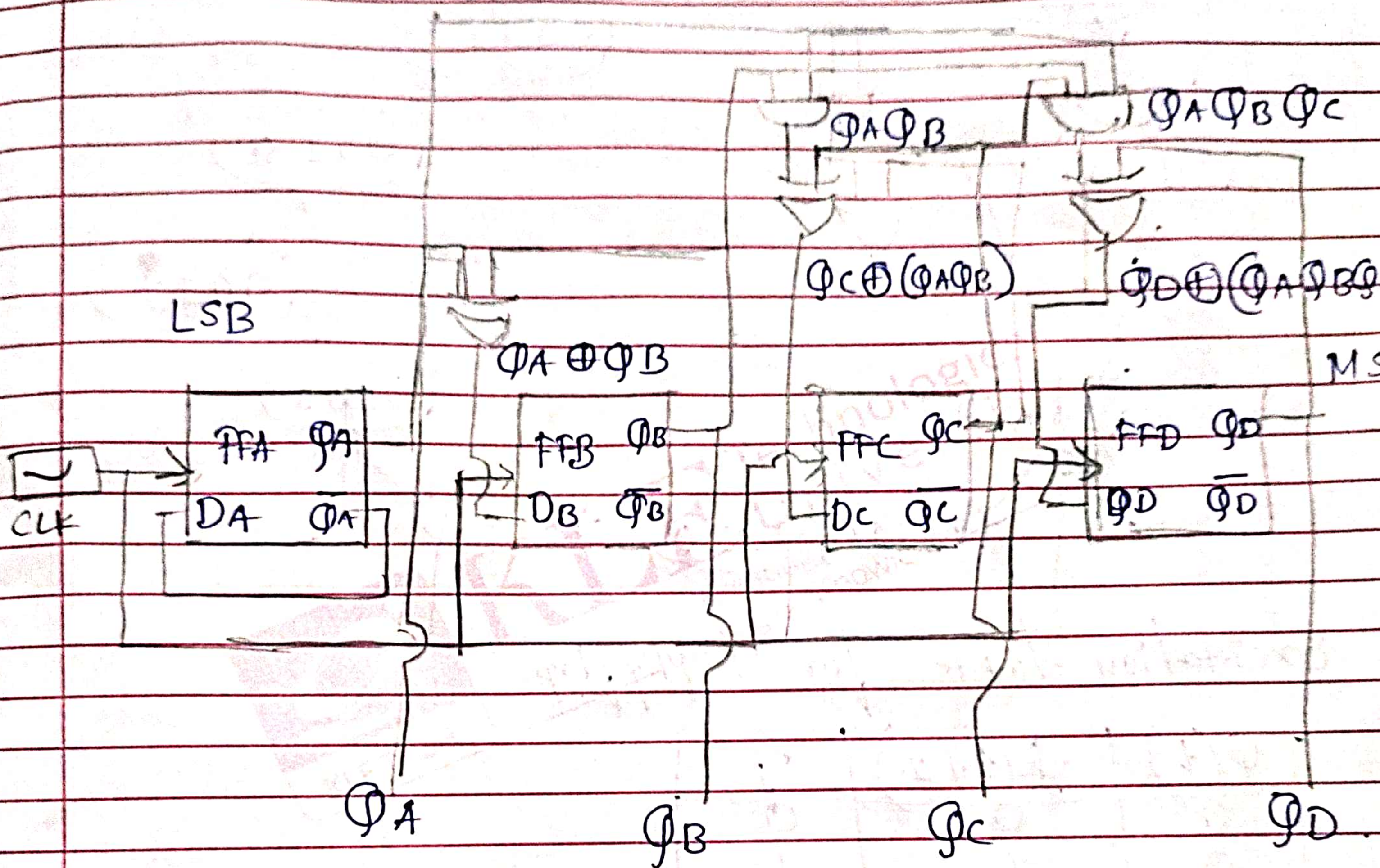
$\overline{Q_A}$

$$\boxed{D_A = \overline{Q_A}}$$

$D_A = \overline{Q_A}$ $D_B = Q_A \oplus Q_B$ $D_C = Q_C \oplus Q_B Q_A$

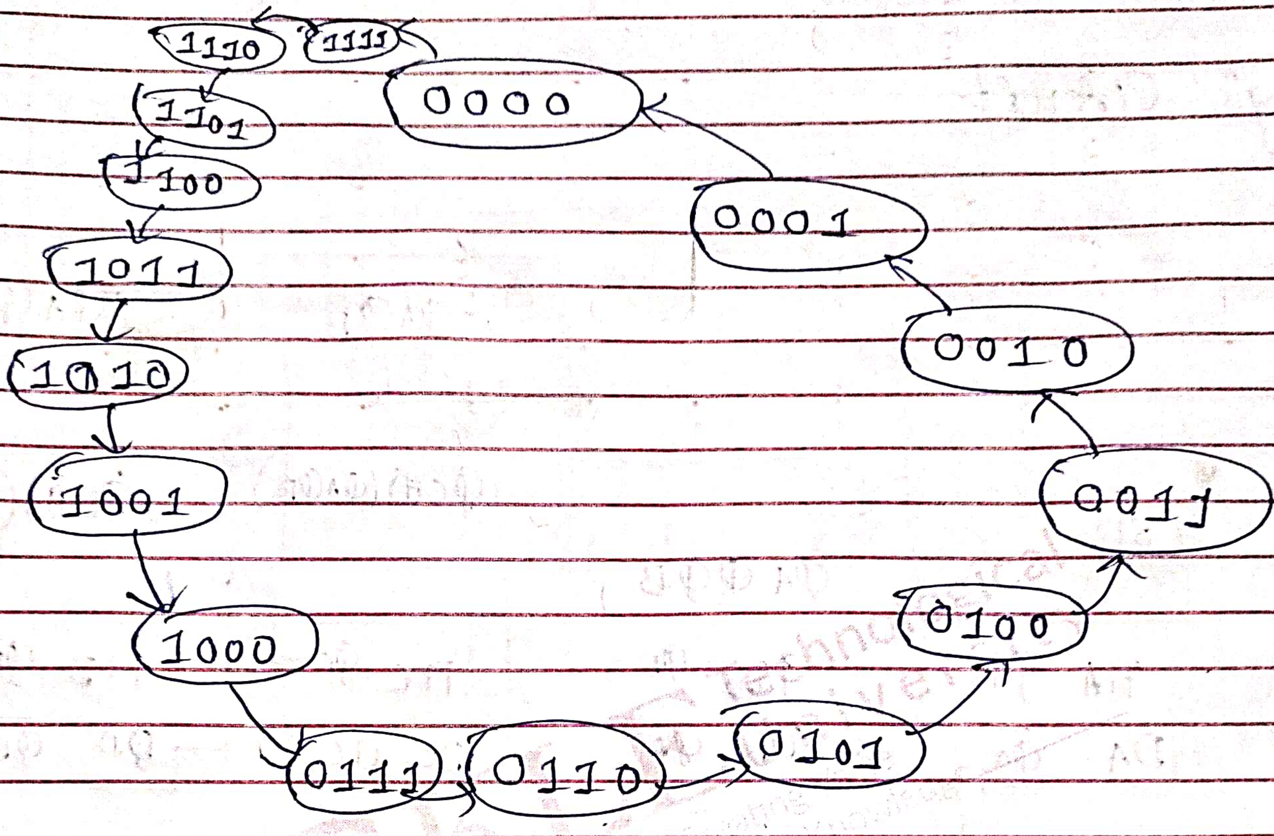
$D_D = Q_D \oplus (Q_C Q_B Q_A)$.

Logic Circuit:



④ 4-bit down counter using T flipflop.

⇒ 4 bit, 4-T flipflops (down counter 15 → 0)



Excitation table for T flipflop.

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table for counter

Present-state				Next-state							
Q_D	Q_C	Q_B	Q_A	Q_D^{+1}	Q_C^{+1}	Q_B^{+1}	Q_A^{+1}	T_D	T_C	T_B	T_A
0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	1	0	0	1	1
0	0	1	1	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	1	1	1
0	1	0	1	0	1	0	0	0	0	0	1
0	1	1	0	0	1	0	1	0	0	1	1
0	1	1	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	0	0	0	0	0	1
1	0	1	0	1	0	0	1	0	0	1	1
1	0	1	1	1	0	1	0	0	0	0	1
1	1	0	0	1	0	1	1	0	1	1	1
1	1	0	1	1	1	0	0	0	0	0	1
1	1	1	0	1	1	0	1	0	0	1	1
1	1	1	1	1	1	1	0	0	0	0	1

K-map for T_D

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	1_0	0_1	0_3	0_2
01	0_4	0_5	0_7	0_6
11	0_{12}	0_{13}	0_{15}	0_{14}
10	1_8	0_9	0_{11}	0_{10}

$T_D = \overline{Q_A}\,\overline{Q_B}\,\overline{Q_C}$

K-map for T_C

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	1_0	0_1	0_3	0_2
01	1_4	0_5	0_7	0_6
11	1_{12}	0_{13}	0_{15}	0_{14}
10	1_8	0_9	0_{11}	0_{10}

$\overline{Q_A}\,\overline{Q_B}$

$T_C = \overline{Q_A}\,\overline{Q_B}$

K-map for T_B

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	1_0	0_1	0_3	1_2
01	1_4	0_5	0_7	1_6
11	1_{12}	0_{13}	0_{15}	1_{14}
10	1_8	0_9	0_{11}	1_{10}

$T_B = \overline{Q_A}$

K-map for T_A

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	1_0	1_1	1_3	1_2
01	1_4	1_5	1_7	1_6
11	1_{12}	1_{13}	1_{15}	1_{14}
10	1_8	1_9	1_{11}	1_{10}

1

$T_A = 1$

$T_A = 1 \quad T_B = \overline{Q_A} \quad T_C = \overline{Q_A}\,\overline{Q_B} \quad T_D = \overline{Q_A}\,\overline{Q_B}\,\overline{Q_C}$

Logic Circuit: