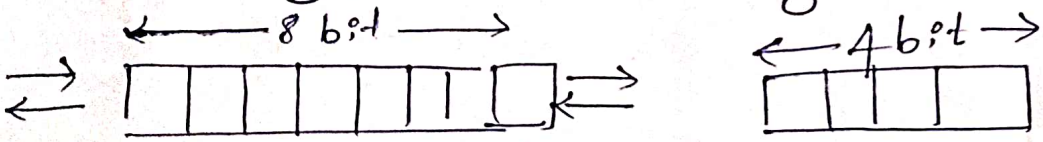
# Registers.

In digital electronics, a register is a temporary storage area built into a CPU that stores & manipulates data during the execution of instructions.

A register is a collⁿ of flip flops. A flip-flop is used to store single bit digital data for storing a large no. of bits, the storage capacity is increased by grouping more than one flip flops.

If we want to store an n-bit word, we have to store an n-bit word, we have to use n-bit register containing 'n' no. of ff's.



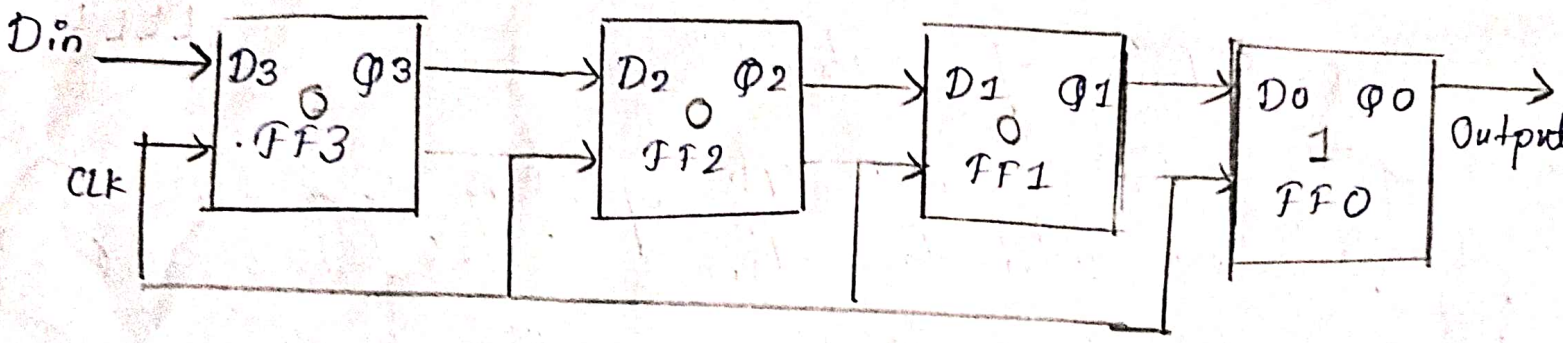

## Shift Register :

The binary data in a register can be moved within the register from one ff to another. The registers that allow such data transfers are called shift register.

There are four mode of operation of a shift Register.

① SISO ② SIPO ③ PISO ④ PIPO.

## ① SISO (Shift Right)




Truth table.

MSB LSB
1 1 1 1

| CLK | Q3 | Q2 | Q1 | Q0 | |
|---|---|---|---|---|---|
| ↓ | 0 | 0 | 0 | 0 | ✓ |
| ↑ | 1 | 0 | 0 | 0 | ✓ |
| ↑ | 1 | 1 | 0 | 0 | ✓ |
| ↑ | 1 | 1 | 1 | 0 | ✓ |
| ↑ | 1 | 1 | 1 | 1 | ✓ |
| ↑ | 0 | 1 | 1 | 1 | ✓ |
| ↑ | 0 | 0 | 1 | 1 | ✓ |
| ↑ | 0 | 0 | 0 | 1 | ✓ |

Initially let all the ff be in reset condition i.e., $Q_3 Q_2 Q_1 Q_0 = 0000$.

If an entry of 4-bit binary number 1111 is made into the register across Din bit, with LSB bit applied first.

The D i/p of FF3 i.e., D3 is connected as Serial Input & FF0 is connected as o/p. O/p of $Q_3$ is given as i/p to D2 & so on.

Operation.

LSB no. to be entered to Din so $Din = D3 = 1$
Apply the clock.

→ On Raising edge of clk, the FF3 is set, & stored word in the register is $Q_3 Q_2 Q_1 Q_0 = 1000$

→ On 2nd Raising edge of clk, FF2 will be set, & stored word in the register is $Q_3 Q_2 Q_1 Q_0 = 1100$

→ On 3rd Raising edge of clk, FF1 will be set & stored word in the register is $Q_3 Q_2 Q_1 Q_0 = 1110$

→ On 4th ~~Raising~~ edge 4th clock pulse, FF0 will be set & stored word in the register is $Q_3 Q_2 Q_1 Q_0 = 1111$.

The bits in ff goes on shifting right with every clock pulse.

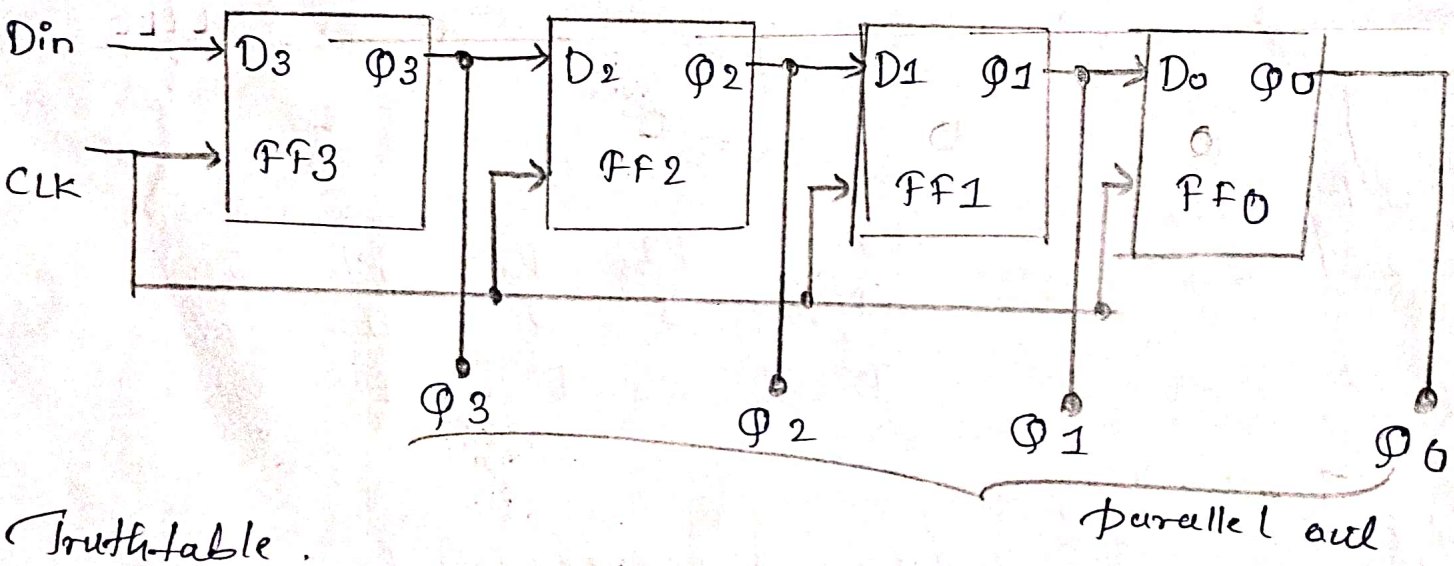
## SIPO shift Register.

In this data entered serially & taken out in parallel fashion.

Data is loaded bit by bit. The o/p's are disabled as long as the data is loading.

As soon as the data loading gets completed, all the ff's contain their required data, the o/p's are enabled so that all the loaded data is made available over all the o/p lines at the same time.

4 clock pulse are required to load a four bit word.

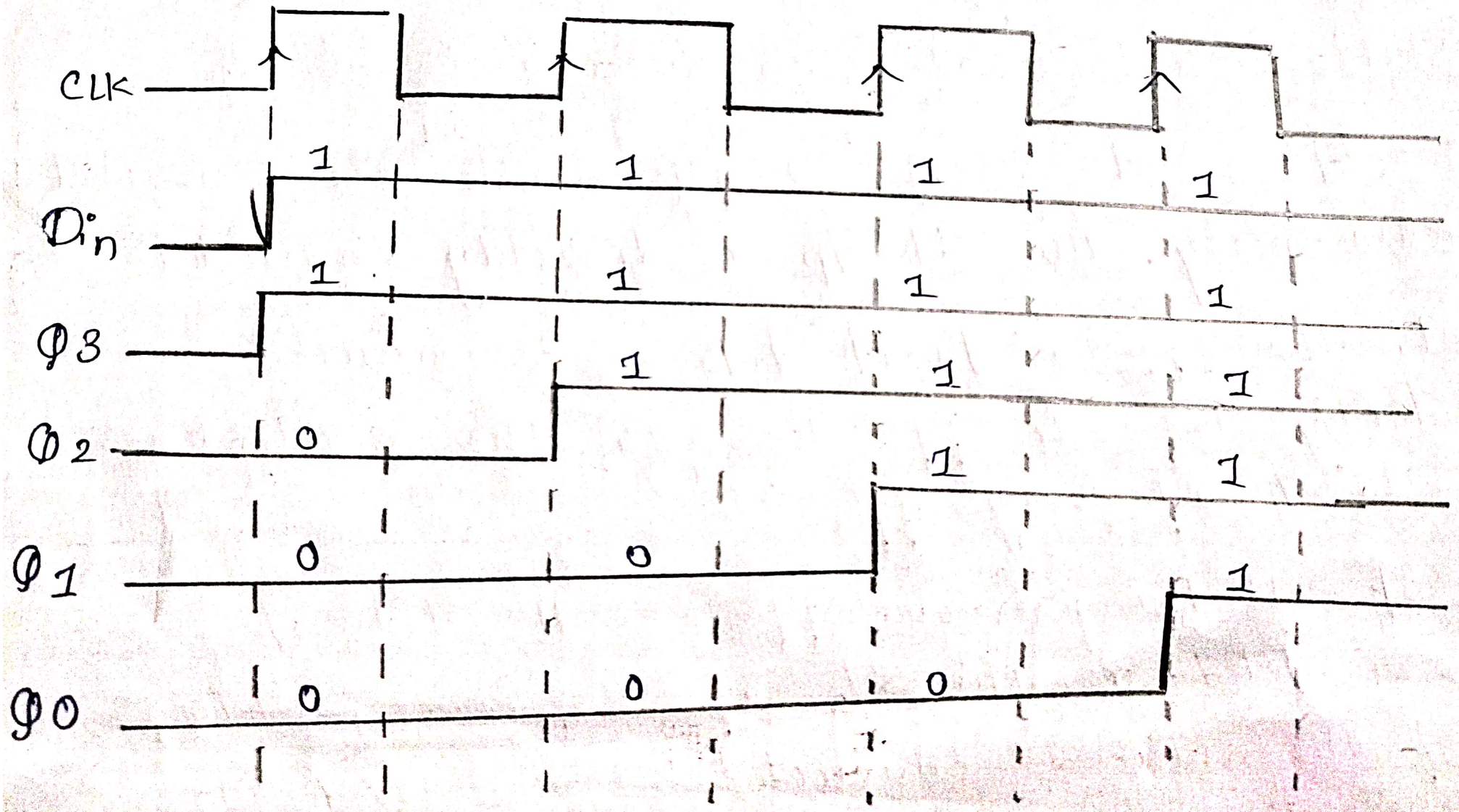



Truth table.

| CLK | Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|---|
| ↓ | 0 | 0 | 0 | 0 |
| ↑ | 1 | 0 | 0 | 0 |
| ↑ | 1 | 1 | 0 | 0 |
| ↑ | 1 | 1 | 1 | 0 |
| ↑ | 1 | 1 | 1 | 1 |

Waveforms.

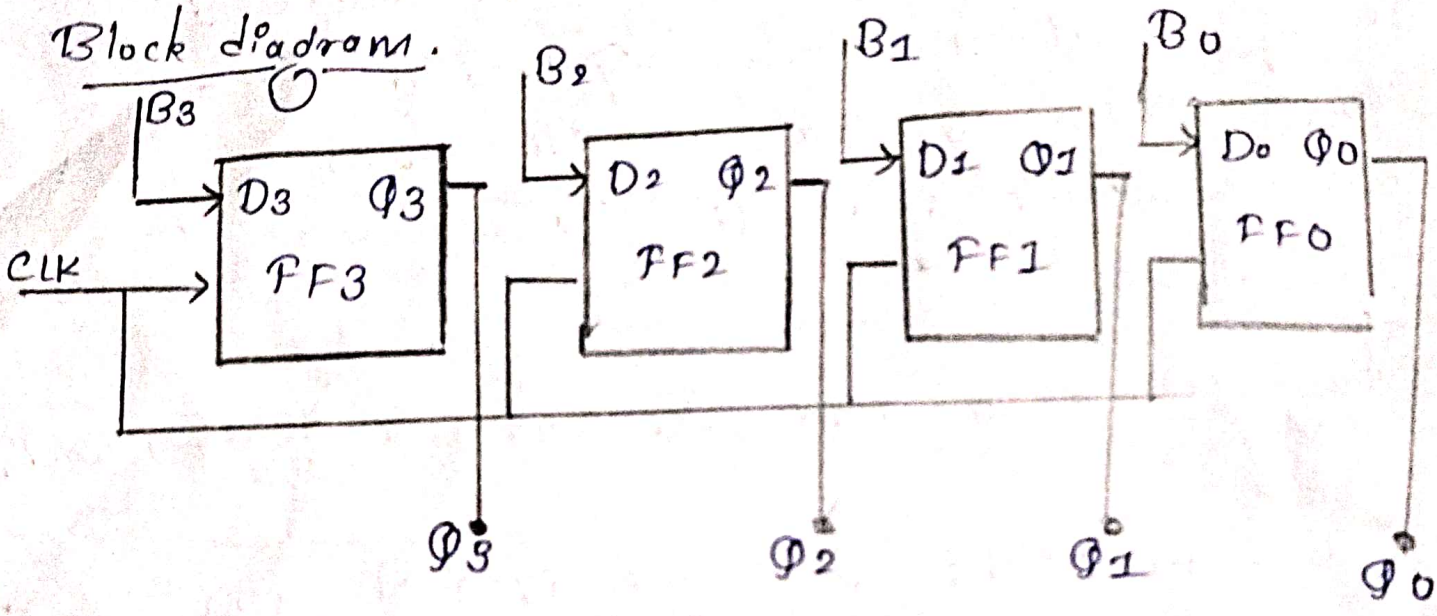
## SIPO



## PIPO shift Registers

When the clk pulse is applied the input binary bits will be loaded into the FF's simultaneously. The loaded bits will appear simultaneously to the o/p side only clock pulse is essential to load all the bits.

Block diagram.

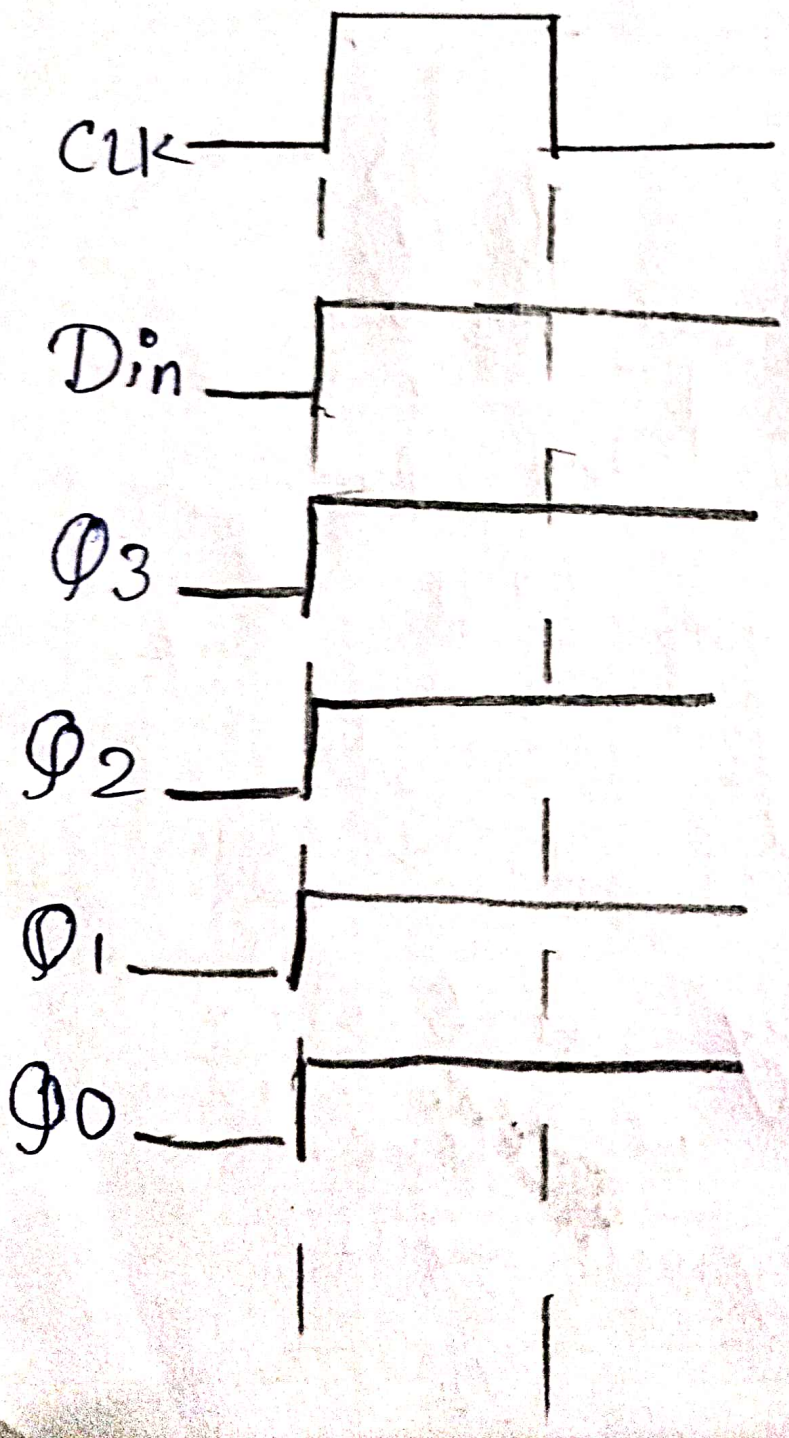



| CLK | B3 | B2 | B1 | B0 | Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|---|---|---|---|---|
| ↓ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ↑ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Only one clock pulse is required to load the data & the o/p is taken.

It's faster compare to SISO & SIPO.

PIPO



## Truth table:

| | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|---|
| ↓ | 0 | 0 | 0 | 0 |
| ↑ | 01 | 10 | 01 | 10 |
| ↑ | 0 | 1 | 0 | 1 |
| ↑ | 0 | 0 | 1 | 0 |
| ↑ | 0 | 0 | 0 | 1 |

## Waveform: