Wafers are the raw material that is used in the preparation of IC chips. Single crystalline silicon is used to produce silicon wafer because of its superior properties as mentioned below.

Physical properties:

1. Si is a semiconductor having the forbidden gap or band gap of 1.125 ev at 25^{o}C
2. At atmospheric pressure Si crystallizes into a diamond cubic structure. Vapour deposition below 500^{o}C, results in amorphous Si and if reheated above this temp., crystallization occurs.
3. Elements, metals and compounds contracts on cooling and expands on heating. But Si contracts on melting (heating) and expands on solidification (cooling), which facilitates doping or incorporation of impurities.
4. Impurities incorporated in the Si lattice, provides either free electrons (-ve charge) or holes (+ve charge).
5. Impurities from V group ('Phosphorus') are 'n' dopants (creating –ve charge) and III group ('Boron') are 'p' dopants (Creating +ve charge).
6. The impurities are expressed in terms of 'Minority carrier life time'. Si doped with 'P' or 'B' has a minority carrier life time of 50 to 300 µs suitable for electrical and electronic devices.

Chemical properties of Silicon:

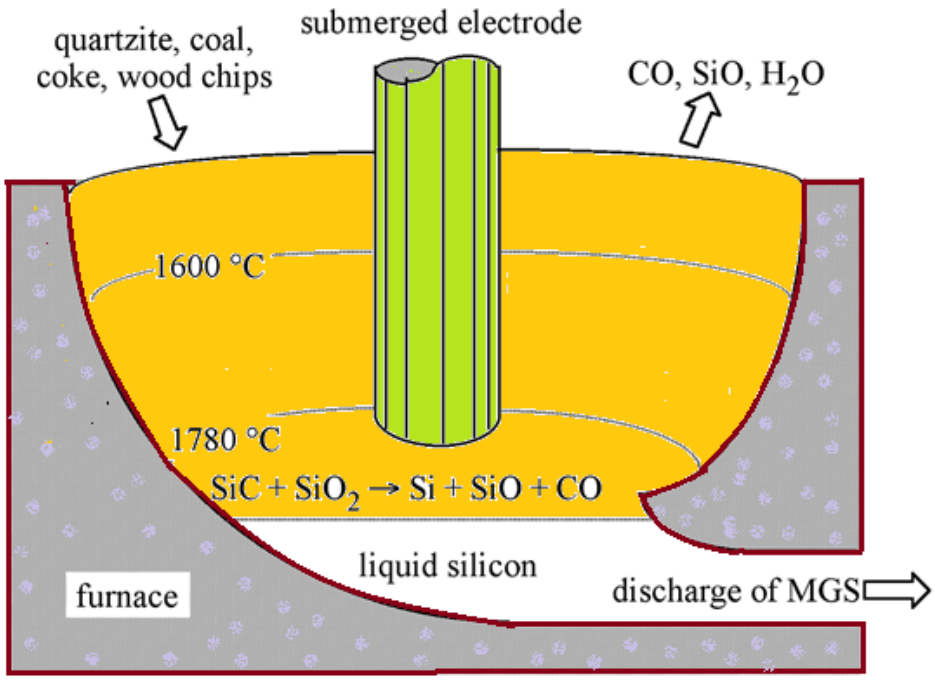
1. Si belongs to Carbon family (IV group). Si^{14} EC: $1s^2 2s^2 2p^6 3s^2 3p^2$
2. Si has a +2 and +4 oxidation states, but +4 is stable (tetravalent state).
3. Silicon combines with Carbon, another tetravalent element, forming Si-C having strong covalent bonds and stable products. Si-C is an abrasive (can be removed in the form of layers) and can be sliced for wafering Si crystals.
4. Si is reactive towards halogens and forms Chlorosilanes such as H_2SiCl_2, $HSiCl_3$ and $SiCl_4$ with 8.3^{0}C, 32^{0}C and 57.6^{0}C boiling points respectively. They are highly volatile and can be decomposed to elemental Si at low temperatures. Hence Chlorosilanes are used in the purification of Si.
5. Si readily combines with H_2 to form hydrides or silanes. The monosilane, SiH_4, is used in the further purification and preparation of electronic grade silicon – EGS.

Single crystal silicon can be obtained from sand or quartz. The process of obtaining single crystal silicon involves three steps.

1. Production of Metallurgical grade silicon – MGS
2. Production of electronic grade silicon – EGS
3. Preparation of single crystal silicon – SCS

PRODUCTION OF METALLURGICAL GRADE SILICON

Metallurgical grade silicon, also called **silicon metal**, with a typical purity of 98.5% Si is produced in submerged electric arc furnaces.



THE CARBOTHERMIC REDUCTION OF SILICA:

The electric arc furnace consists essentially of a vessel filled with quartz and carbon materials.

Electrodes are made of carbon. Liquid silicon metal is tapped from the bottom of the furnace and the thoroughly mixed raw materials are charged on the top.

The reactions taking place in the electric arc furnace are:

At 1600 ^{O}C,

The temperature in the inner zone is in the range of 1600 °C, allowing a high proportion of SiO in this zone, which is vital for further reduction according to the following reactions:

(i) $SiO + CO \longrightarrow SiO_2 + C$

(ii) $SiO + 2C \longrightarrow SiC + CO$

(iii) $SiO_2 + C \longrightarrow SiO + CO$

At 1780 ^{O}C,

In the outer zone, where the temperature is in the range of 1780°C, SiC and SiO_2 coming from the inner zone meet and react with each other forming liquid silicon.

(i) $SiC + SiO_2 \longrightarrow Si + SiO + CO$
MGS

At frequent intervals, liquid silicon is drained out from the bottom of the furnace.

Depending on the quality of the raw materials used and the operational strategy and skills, the silicon yield as metallurgical grade silicon ranges from 80 to 90%.

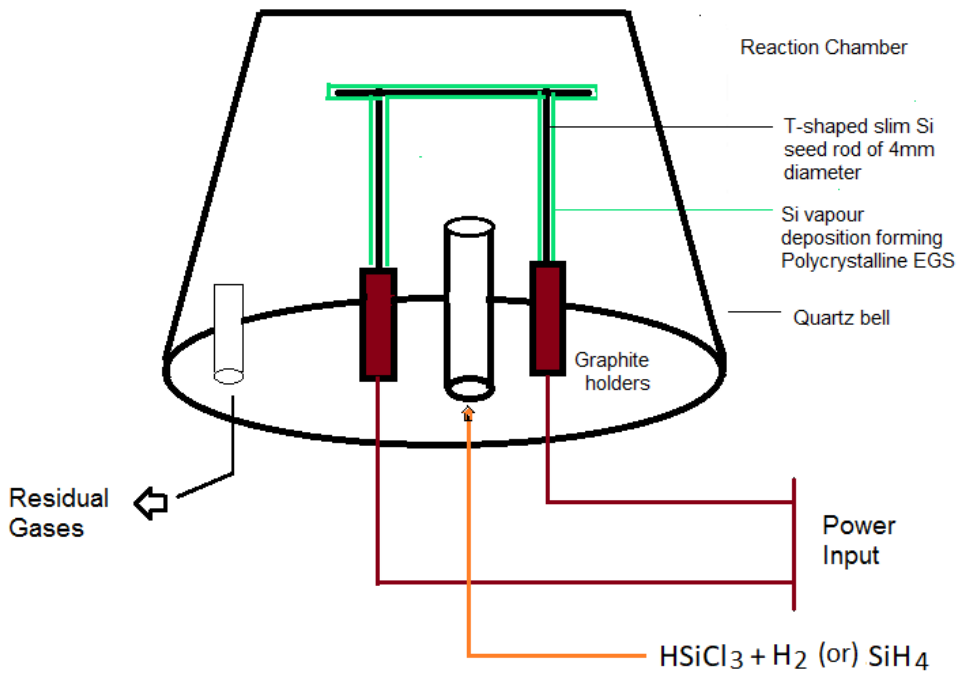
The so obtained **Metallurgical Grade Silicon**, also called **silicon metal** undergoes a double purification through fractional distillation.

PREPARATION OF ELECTRONIC GRADE SILICON BY CVD PROCESS

Trichlorosilane, $HSiCl_3$ is prepared by hydro-chlorination of metallurgical grade silicon in a fluidised bed reactor at 350 ^{O}C.

$$Si\ (s) + 3\ HCl \rightarrow HSiCl_{3\ (g)}$$
Powdered MGS **Trichlorosilane**

The so obtained trichlorosilane undergoes a double purification through fractional distillation and used as raw material for the preparation of Electronic Grade Silicon, EGS.



CVD REACTOR

Reduction Reaction:

- Highly purified trichlorosilane and high-purity hydrogen gas is introduced into the deposition reactor where the temperature is maintained around 1400^{o}C.
- At this temperature, reduction of $HSiCl_3$ to Si occurs and it is deposited over the T-shaped slim Si rod of 4 mm diameter.

$$\mathbf{HSiCl_{3\,(g)} + H_{2\,(g)} \rightarrow Si_{(s)} + 3HCl_{(g)}}$$

- To achieve deposit thickness of 20 cm rod of polycrystalline EGS, the process takes 16-24 hours.
- Polycrystalline Si of EG can be cut from these rods as single chunks.

Pyrolysis:

- Polycrystalline Electronic Grade Silicon can also be prepared by Pyrolysis of Silane at 900^{0}C in the CVD reactor.

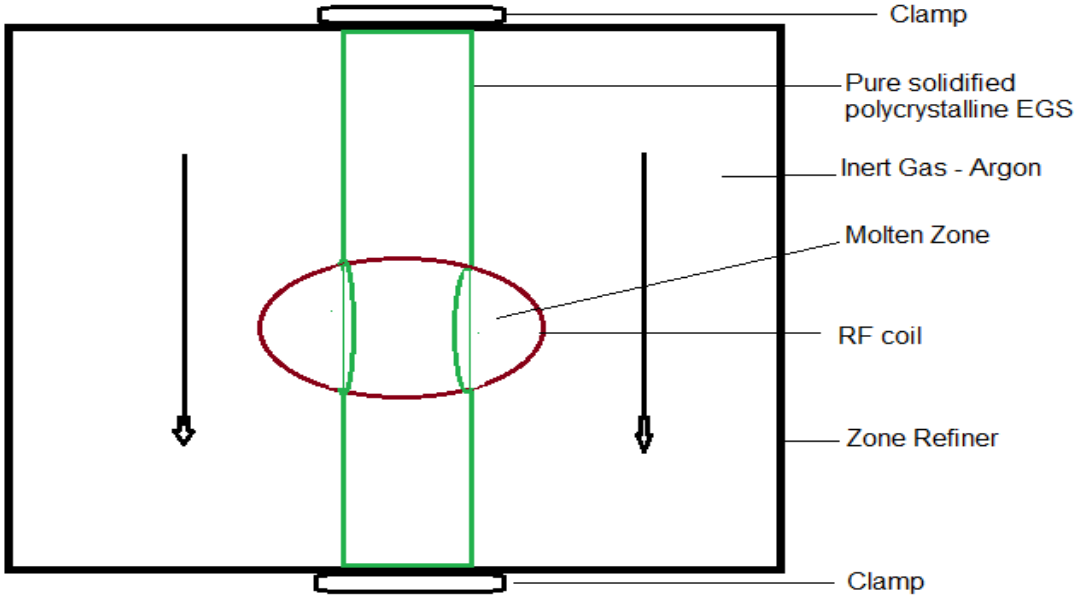
$$\mathbf{SiH_4 \rightarrow Si + 2H_{2\,(g)}}$$

- This process facilitates the potentially low cost production of EGS and less harmful reaction products. Worldwide consumption of EGS is around 5000 tons per year.

PURIFICATION OF SILICON BY ZONE REFINING

Zone Refining is the unique method of obtaining 99.9999% pure polycrystalline Electronic Grade Silicon with perfect and rigorous recrystallization.

Principle: When a solid is melted, the impurities tend to concentrate in the molten zone.



Procedure:

- A vertical zone refiner is used for the purification of EGS.
- A rod of polycrystalline EGS to be purified is clamped vertically in a zone refiner.
- Zone refiner is heated by a RF coil to the melting point of Si (1000^{o}C) in a reducing atmosphere of Ar.
- The heater RF coil is moved very slowly from top towards bottom where the impurities are swept down along with the molten part the material.
- Pure polycrystalline EGS solidifies at upper portion with perfect recrystallization.
- This is said to be one zone pass. Repeated zone pass can reduce the impurity level to one atom in every 10^{12} atoms of silicon in parts per trillion ranges.
- After the process is completed, the bottom portion of the rod where the impurities are concentrated is cut and removed.

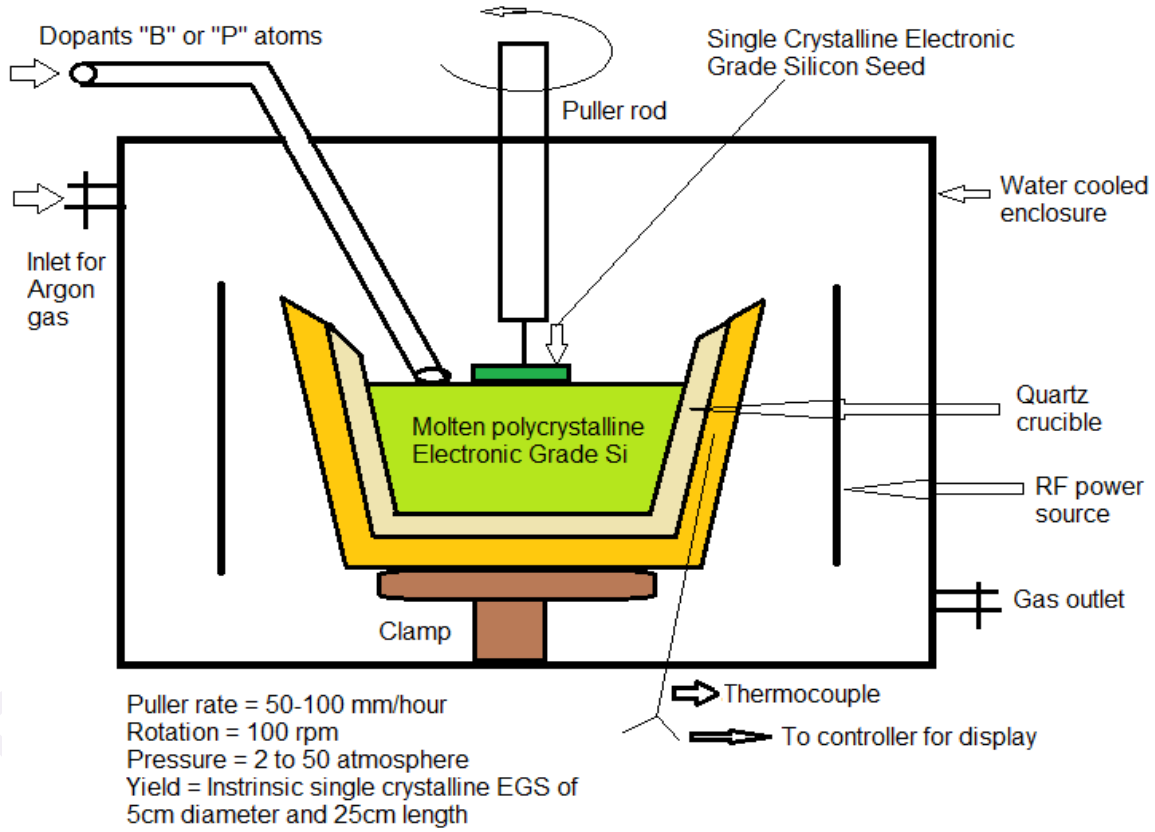
PRODUCTION OF SINGLE CRYSTAL SILICON BY CZHOCHRALSKI

CRYSTAL PULLING TECHNIQUE

Fabrication of most of the semiconductor devices requires single crystalline electronic grade silicon.

- **Czhochralski crystal pulling technique** is a method used for the production of single crystal EGS from polycrystalline EGS.
- **Principle:**

In this technique single crystalline electronic grade silicon is used as a seed to grow single crystal silicon from polycrystalline silicon. When the silicon melt is pulled out, the atoms of polycrystalline silicon solidifies and reproduces the same orientation and crystal structure as that of the single crystalline electronic grade silicon seed.



- **Procedure:**
  - Gas inlet and outlet for inert gas Argon or Krypton which prevents the oxidation of molten silicon.
  - Provision is made to incorporate dopants "Boron" or "Phosphorus" into the molten silicon.
  - Water cooled enclosure is provided to maintain low temperature for growing single crystal silicon.
  - Polycrystalline electronic grade silicon is now taken in a quartz crucible and kept in molten state by RF power source in an inert atmosphere of Argon gas.
  - The temperature of RF power source is regulated by thermocouple and displayed through controller.
  - Calculated amount of dopant atoms either 'B' (p-type) or 'P' (n-type) are added to polycrystalline EGS in the molten state.
  - A single crystalline EG silicon seed is attached to the tip of puller rod and is lowered into a molten material in such a way that it just touches the surface of the molten polycrystalline EGS.
  - The puller rod is slowly rotated and simultaneously pulled out. That is the **puller rate** is maintained at around **50-100 mm/hour** with **rotation** of **100 rpm** at a **pressure** of **2-50 atmospheres**.
  - As the silicon melt is pulled out, the atoms of polycrystalline silicon solidifies and takes the same orientation and crystal structure as that of the single crystalline EG silicon seed.
  - Finally, an intrinsic single crystalline EG silicon of 5cm diameter and 25cm length is obtained as a yield.
- **Segregation Constant, K_0:**

  It is defined as the ratio of concentration of impurities in the solid state (C_s) to the concentration of impurities in the liquid state (C_l).

  $$K_0 = C_s / C_l$$
- **Solid solubility:**

  The maximum concentration of impurities that can be introduced into a semiconductor at a given temperature is known as solid solubility. Solid solubility increases with increase in temperature.

NUMERICAL PROBLEMS ON CZHOCHRALSKI CRYSTAL PULLING TECHNIQUE

Lesson Plan: Q. No: 4

A silicon crystal is to be grown by Czhochralski process and is to contain 5 x 10^{15} boron atoms per cm^3. Given K_o = 0.8 for boron in silicon, atomic weight of boron = 10.81g/mole, density of silicon = 2.33g/$cm^3$and Avogadro number = 6.023 x 10^{23} atoms/mole.

a) Determine the initial concentration of boron atoms in the melt to produce the required density.
b) If initial amount of silicon in the crucible is 50kg, how many grams of boron should be added?

Given:

- Concentration of 'B' atoms in solid state, C_s = 5X10^{15} Boron atoms/cm^3.
- Segregation constant for 'B' in Silicon = K_o = 0.8.
- Initial weight of Silicon in the crucible = 50 kg = 50X10^3 g.
- Density of Silicon = 2.33 g/cm^3.
- Atomic weight of Boron= 10.81 g/mole.
- Avogadro Number = 6.023X10^{23} atoms/mole.

Solution:

(a) Concentration of 'B' atoms in the melt, C_l:

- **Segregation constant, $K_o = C_s / C_l$**

  $C_l = C_s / K_o$ = 5X10^{15} / 0.8 = 6.25X10^{15} atoms/cm^3

❖ **C_l = 6.25X10^{15} atoms/cm^3.**

(b) Weight of Boron atoms to be added for 50X10^3 g of Si, W_B :

- **Volume of Silicon, V_{si}:**

  V_{Si} = Weight of Si / Density of Si = 50X10^3 / 2.33 cm^3

❖ **V_{Si} = 21.46X10^3 cm^3.**

- **Total number of 'B' atoms in the given volume of Si, T_B :**

  $T_B = C_l$ X V_{si} = 6.25X10^{15} X 21.46X10^3 atoms

❖ **T_B = 134.125X10^{18} atoms.**

- **Weight of 'Boron' atoms to be added, W_B :**

  W_B = Atomic weight of Boron X Total number of 'B' atoms grams

  Avogadro Number

  $W_B = (10.81 \times 134.125X10^{18}) / 6.023X10^{23} = 240.73X10^{-5}$ g. = $240.73X10^{-5}$ X 1000 mg

❖ **W_B = 2.4073 mg.**

Lesson Plan: Q. No: 5

A silicon crystal is to be pulled from the melt and doped with phosphorus. If Si weighs 1Kg, how many grams of phosphorus atoms should be introduced to achieve a donor concentration of 2 x 10^{15}atoms / cm^3 during initial growth?
Given: K_o = 0.32 for P in Si; Atomic weight of 'P' = 30.97g/mole, Density of silicon = 2.33g/cm^3, Avogadro number = 6.023 x 10^{23} atoms/mole.

Given:

- Concentration of 'P' atoms in solid state, $C_s = 2X10^{15}$ 'P' atoms/cm^3.
- Segregation constant for 'P' in Silicon = K_o = 0.32.
- Initial weight of Silicon in the crucible = 1 kg = $1X10^3$ g.
- Density of Silicon = 2.33 g/cm^3.
- Atomic weight of Phosphorus = 30.97 g/mole.
- Avogadro Number = $6.023X10^{23}$ atoms/mole.

Solution:

Concentration of 'P' atoms in the melt, C_l:

- **Segregation constant, $K_o = C_s / C_l$**

  $C_l = C_s / K_o = 2X10^{15} / 0.32 = 6.25X10^{15}$ atoms/cm^3

❖ **$C_l = 6.25X10^{15}$ atoms/cm^3 .**

Weight of Phosphorus atoms to be added for $1X10^3$ g of Si, W_P :

- **Volume of Silicon, V_{si}:**

  V_{Si} = Weight of Si / Density of Si = $1X10^3$ / 2.33 cm^3

❖ **$V_{Si} = 0.42918X10^3$ cm^3.**

- **Total number of 'P' atoms in the given volume of Si, T_P :**

  $T_P = C_l \times V_{si} = 6.25X10^{15} \times 0.42918X10^3$ atoms

❖ **$T_P = 2.682375X10^{18}$ atoms.**

- **Weight of 'Phosphorus' atoms to be added, W_P :**

W_P = Atomic weight of Phosphorus X Total number of 'P' atoms g.

Avogadro Number

$W_P = (30.97 \times 2.682375 \times 10^{18}) / 6.023 \times 10^{23} = 13.79265 \times 10^{-5}$ g.

$W_P = 13.79265 \times 10^{-5} \times 1000$ mg

❖ **W_P = 0.1379265 mg.**

Additional Problems:

1) A semiconductor crystal with acceptor concentration, N_A with 2×10^{16} atoms/cm^3 must be obtained by Czhochralski crystal pulling technique. What weight of Boron must be added to the melt if it contains 10 Kg of Si?

Given: $K_0 = 0.8$ for 'B' in Si; Atomic weight of 'B' = 10.81g/mole, Density of Si = 2.33 g/cm^3, Avogadro number = 6.023×10^{23} atoms/mole.

2) A Silicon crystal is to be pulled from the melt and doped with phosphorous . If silicon weighs 7 kg, how many grams of phosphorous should be introduced to achieve a donor concentration of 2×10^{15}/cm^3 during initial growth.

Given: K_0 for 'P' in Silicon is 0.32; Atomic weight of 'P' = 30.97 g/mole;

Density of Si is 2.33 g/cm^3; Avogadro number = 6.023×10^{23} atoms/mole

CRYSTAL SLICING

- The crystal ingot which has 20cm diameter and 100cm length is ground to have cylindrical shape with flat ends.
- A sample slice is cut and the crystal orientation is determined by X-ray diffraction method.
- Further slicing is done at different angles until the desired crystal orientation of the surface is obtained.
- Now the flat ended crystal ingot is cut into slices called **wafers** using diamond tipped saw with respect to the desired crystal orientation of the surface.
- The thickness of the wafers varies from 0.4mm to 1.0mm and $1/3^{rd}$ of the material is lost as dust.

WAFER PREPARATION

- The so obtained single crystalline electronic grade silicon wafers as a result of crystal slicing are subjected to:
  - **Lapping** under pressure using a mixture of Al_2O_3 and glycerine to remove any cracked surface on silicon wafer.
  - **Chemical etching** using a mixture of HF, HNO_3 and CH_3COOH to remove any damages on the surface of silicon wafers.
  - Lapping and chemical etching processes produce flat surface on silicon wafers which are further sorted out on an automated basis according to thickness.

One side of the silicon wafer is polished to a mirror finish over which fabrication process is carried out.

FABRICATION PROCESS

Fabrication is the process of making or manufacturing something from raw or semi-finished materials instead of being assembled from readymade components or parts.

For many electrical and electronic applications the quality of polished wafer is not sufficient. This is mainly due to the defects generated during crystal growth in the bulk of the silicon wafer. These defects, when they are within a few microns to the surface, can deteriorate the performance of devices built on it.

Currently, this problem has been overcome by depositing an additional layer of high purity Si on the top of the polished Si wafer substrate.

The important unit processes involved in the fabrication of devices are:

- **Thermal oxidation**
- **Diffusion**
- **Ion implantation**
- **Epitaxial Growth**
- **Masking**
- **Photo Lithography**
- **Etching**

The basic integrated circuit fabrication process is known as 'planar process' in which introduction of impurities and metallic connections are carried out from the top surface of the wafer.

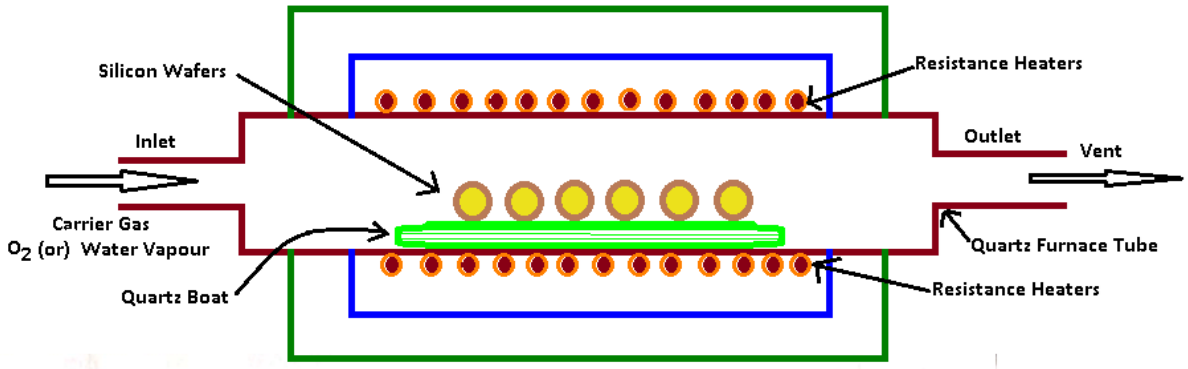
In planar process several wafers consisting of similar devices or circuits can be processed simultaneously. Precise control of temperature; humidity and extremely clean environment are required for fabrication of devices.

THERMAL OXIDATION

Thermal Oxidation is a method of growing a film of SiO_2 from a single crystal silicon wafer.

Thermal oxidation is required

- For masking the material
- For surface modification
- For biocompatibility and
- to act as a sacrificial layer



THERMAL OXIDATION SYSTEM

Procedure:

- Thermal oxidation is carried out in a thermal oxidation furnace.
- It consists of a quartz furnace tube.
- One end of the tube is provided with a vent and the other end of the tube is having an inlet for sending carrier gas such as oxygen (dry oxidation) or oxygen and water vapour (wet oxidation) which is required for oxidation.
- Quartz boat is placed inside the quartz furnace tube.
- Silicon wafers are placed vertically in the quartz boat.
- The quartz furnace tube is heated to a temperature of 900^{o}C to 1200^{o}C using resistance heaters.
- Thermal oxidation proceeds in two ways depending on the nature of oxidizing agent used.

Dry Oxidation:

- This process takes place when dry oxygen is used as an oxidizing agent.
- In this process dry oxygen in molecular form is diffused into the Si wafer at high temperature of **900 °C to 1200 °C** and made to react with it.
- The chemical reaction at the Si surface is

$$Si + O_2 \rightarrow SiO_2$$

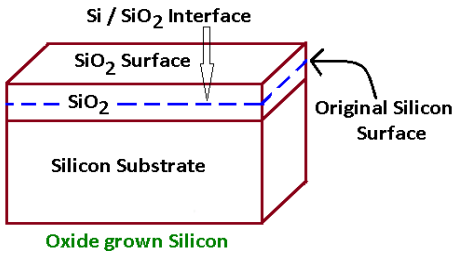
- Here one molecule of oxygen results in the formation of one molecule of SiO_2.
- The oxide growth rate is very low in dry oxidation. But its electrical properties are excellent.

Wet Oxidation:

- Here water vapour is used as an oxidizing agent in presence of oxygen.
- This process takes place at a temperature of **900 °C to1000 °C**.
- The following chemical reaction takes place

$$Si + 2H_2O_{(g)} \rightarrow SiO_2 + 2H_{2(g)}\uparrow$$

- Here, two molecules of water vapours are used to form one molecule of SiO_2.
- H_2 gas evolved by this reaction diffuses rapidly through the growing oxide and leaves the system at the gas oxide interface.
- Wet oxidation is much faster than dry oxidation. It is suitable for making thick oxide exceeding 1μm.



- When SiO_2 is grown on Si wafer, thickness of Si decreases as Si is consumed during oxidation.
- In the beginning, O_2 and Si react to form SiO_2. Once oxide layer is formed, further oxidation occurs at Si-SiO_2 interface, but not on the top of oxide.
- Oxide growth rate slows down with increase in oxide thickness because the oxidizing agent should move through the growing oxide layer in order to reach the Si surface.
- The oxide films thus formed are used in making both simple and complex semiconductor devices and in integrated circuits.

Prove that the ratio of thickness of Si Consumed to thickness of SiO_2 formed is 0.44:

Given:

- Atomic weight of Si = 28.09 g/mol
- Density of Si = 2.33 g/cm^3
- Molecular weight of SiO_2 = 60.08 g/mol
- Density of SiO_2 = 2.20 g/cm^3

Solution:

$$\frac{\text{Thickness of Silicon consumed X Area}}{\text{Thickness of } SiO_2 \text{ grown X Area}} = \frac{\text{Volume of 1 mole of Silicon}}{\text{Volume of 1 mole of } SiO_2}$$

$$\text{Volume of 1 mole of Silicon} = \frac{\text{Atomic weight of Silicon}}{\text{Density of Silicon}} = \frac{28.09\ g}{2.33\ g/cm^3} = \mathbf{12.056\ cm^3}$$

$$\text{Volume of 1 mole of } SiO_2 = \frac{\text{Molecular weight of } SiO_2}{\text{Density of } SiO_2} = \frac{60.08\ g}{2.20\ g/cm^3} = \mathbf{27.31 cm^3}$$

$$\frac{\text{Thickness of Silicon consumed}}{\text{Thickness of } SiO_2 \text{ grown}} = \frac{12.056}{27.31}$$

Therefore,

$$\mathbf{\frac{\text{Thickness of Silicon consumed}}{\text{Thickness of } SiO_2 \text{ grown}} = 0.44}$$

NUMERICAL PROBLEMS ON THERMAL OXIDATION

Lesson Plan: Q. No: 9

Determine the ratio of silicon consumed to the thickness of grown SiO_2 layer over the wafer. If SiO_2 layer of 1000Å is to be grown, what would be the thickness of used silicon.
Given: Atomic weight of silicon = 28.09 g./mol. Density of silicon = 2.33 g./cm^3.Molecular weight of SiO_2 = 60.08g./mol. Density of SiO_2 = 2.20g./cm^3.

Given:

- Atomic weight of Si = 28.09 g/mol
- Density of Si = 2.33 g/cm^3
- Molecular weight of SiO_2 = 60.08 g/mol
- Density of SiO_2 = 2.20 g/cm^3
- Thickness of SiO_2 grown = 1000 Å

Solution:

$$\frac{\text{Thickness of Silicon consumed X Area}}{\text{Thickness of } SiO_2 \text{ grown X Area}} = \frac{\text{Volume of 1 mole of Silicon}}{\text{Volume of 1 mole of } SiO_2}$$

$$\text{Volume of 1 mole of Silicon} = \frac{\text{Atomic weight of Silicon}}{\text{Density of Silicon}} = \frac{28.09\ g}{2.33\ g/cm^3} = \mathbf{12.056\ cm^3}$$

$$\text{Volume of 1 mole of } SiO_2 = \frac{\text{Molecular weight of } SiO_2}{\text{Density of } SiO_2} = \frac{60.08\ g}{2.20\ g/cm^3} = \mathbf{27.31 cm^3}$$

$$\frac{\text{Thickness of Silicon consumed}}{\text{Thickness of } SiO_2 \text{ grown}} = \frac{12.056}{27.31}$$

Therefore,

$$\mathbf{\frac{\text{Thickness of Silicon consumed}}{\text{Thickness of } SiO_2 \text{ grown}} = 0.44}$$

Thickness of Silicon consumed = 0.44 X Thickness of SiO_2 grown = 0.44 X 1000 Å

- **Thickness of Silicon consumed = 440Å**

Lesson Plan: Q. No: 10

Determine the ratio of silicon consumed to the thickness of grown SiO_2 layer over the wafer. If 100Å thick silicon is used for the process, what would be the thickness of SiO_2 grown?
Given: Atomic weight of silicon = 28.09 g./mol. Density of silicon = 2.33 g./cm^3. Molecular weight of SiO_2 = 60.08g./mol. Density of SiO_2 = 2.20g./cm^3.

Given:

- Atomic weight of Si = 28.09 g/mol
- Density of Si = 2.33 g/cm^3
- Molecular weight of SiO_2 = 60.08 g/mol
- Density of SiO_2 = 2.20 g/cm^3
- Thickness of Si = 100 Å

Solution:

$$\frac{\text{Thickness of Silicon consumed X Area}}{\text{Thickness of } SiO_2 \text{ grown X Area}} = \frac{\text{Volume of 1 mole of Silicon}}{\text{Volume of 1 mole of } SiO_2}$$

$$\text{Volume of 1 mole of Silicon} = \frac{\text{Atomic weight of Silicon}}{\text{Density of Silicon}} = \frac{28.09 \text{ g}}{2.33 \text{ g/cm}^3} = \mathbf{12.056\ cm^3}$$

$$\text{Volume of 1 mole of } SiO_2 = \frac{\text{Molecular weight of } SiO_2}{\text{Density of } SiO_2} = \frac{60.08 \text{ g}}{2.20 \text{ g/cm}^3} = \mathbf{27.31 cm^3}$$

$$\frac{\text{Thickness of Silicon consumed}}{\text{Thickness of } SiO_2 \text{ grown}} = \frac{12.056}{27.31}$$

Therefore,

$$\frac{\textbf{Thickness of Silicon consumed}}{\textbf{Thickness of } SiO_2 \textbf{ grown}} = \mathbf{0.44}$$

$$\text{Thickness of } SiO_2 \text{ grown} = \frac{\text{Thickness of Silicon consumed}}{0.44} = \frac{100}{0.44} \text{ Å}$$

❖ **Thickness of SiO_2 grown = 227.273 Å**

Lesson Plan: Q. No: 11

Calculate the increase in thickness of Si wafer during the process of oxidation, if 50Å thick silicon is used for the process. Given: Atomic weight of Si = 28.09 g./mol. Density of Si = 2.33 g./cm^3. Molecular weight of SiO_2 = 60.08g./mol. Density of SiO_2 = 2.20g./cm^3.

Given:

- Atomic weight of Si = 28.09 g/mol
- Density of Si = 2.33 g/cm^3
- Molecular weight of SiO_2 = 60.08 g/mol
- Density of SiO_2 = 2.20 g/cm^3
- Thickness of Si = 50 Å

Solution:

$$\frac{\text{Thickness of Silicon consumed X Area}}{\text{Thickness of } SiO_2 \text{ grown X Area}} = \frac{\text{Volume of 1 mole of Silicon}}{\text{Volume of 1 mole of } SiO_2}$$

$$\text{Volume of 1 mole of Silicon} = \frac{\text{Atomic weight of Silicon}}{\text{Density of Silicon}} = \frac{28.09\ g}{2.33\ g/cm^3} = \mathbf{12.056\ cm^3}$$

$$\text{Volume of 1 mole of } SiO_2 = \frac{\text{Molecular weight of } SiO_2}{\text{Density of } SiO_2} = \frac{60.08\ g}{2.20\ g/cm^3} = \mathbf{27.31 cm^3}$$

Therefore,

$$\frac{\textbf{Thickness of Silicon consumed}}{\textbf{Thickness of } SiO_2 \textbf{ grown}} = \frac{\textbf{12.056}}{\textbf{27.31}} = \mathbf{0.44}$$

$$\text{Thickness of } SiO_2 \text{ grown} = \frac{\text{Thickness of Silicon consumed}}{0.44} = \frac{50}{0.44}\ Å$$

- **Thickness of SiO_2 grown = 113.636 Å**

  Increase in thickness of Si wafer = Thickness of SiO_2 grown - Thickness of Si consumed

  Increase in thickness of Si wafer = 113.636 – 50 = 63.636 Å

- **Increase in thickness of Si wafer = 63.636 Å**

Additional Problem:

1) Calculate the increase in thickness of Si wafer during the process of oxidation, if 75 Å thick silicon is used for the process. Given: Atomic weight of Si = 28.09 g/mol. Density of Si = 2.33 g/cm^3. Molecular weight of SiO_2 =60.08 g/mol. Density of SiO_2 = 2.20 g/cm^3.

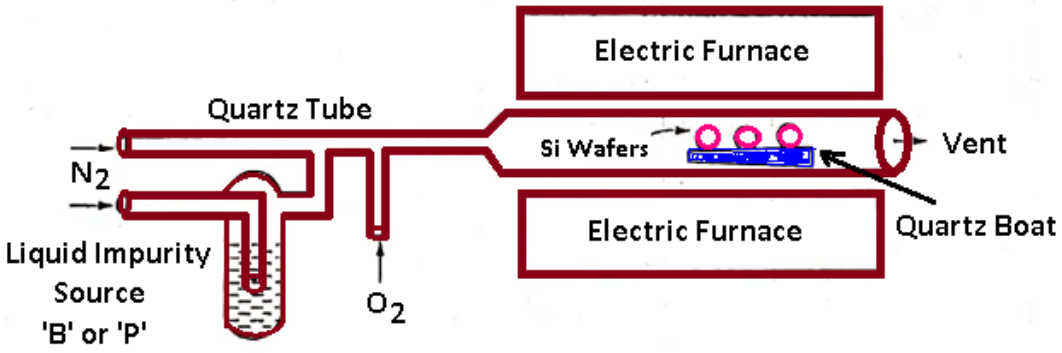
DIFFUSION

Diffusion is a process of selective doping of 'B' or 'P' atoms into semiconductor Si wafer.

Doping means the introduction of impurities such as 'B' or 'P' atoms into the semiconductor silicon wafer to change its conductivity.

Doping can be done selectively into Si wafer by using SiO_2 as masking layer. This can conveniently be carried out by relative etching of SiO_2 layer obtained on a Si wafer by Thermal Oxidation process.

The diffusion process is carried out in an open tube diffusion reactor/furnace.



Open Tube Diffusion System

- Open tube diffusion reactor consists of a quartz tube inside of which movable quartz boat is present.
- Silicon wafers are inserted into the movable quartz boat in series in order to have uniform doping on all silicon wafers.
- Diffusion process is carried out in two steps: **Pre deposition** and **Drive in**.

Pre deposition:

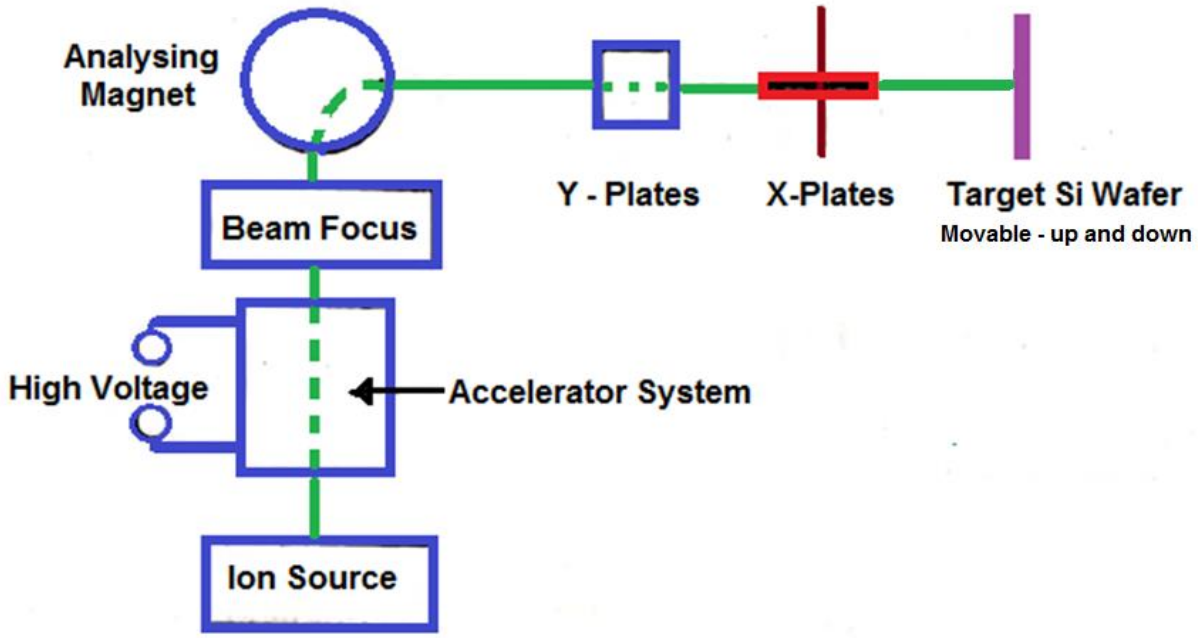
- In Pre-deposition process, a high concentration of dopant atoms such as Boron or Phosphorous are introduced into the furnace in vapour form using Nitrogen and Oxygen as carrier gases at $1000^{O}C$ on Si surface.
- Quartz boat is heated by means of electric furnace to a temperature of $1000^{O}C$ and pre-deposition process takes place on Si wafers.
- At this high temperature, the bonds in Si are broken and facilitate the diffusion of dopant atoms into the Si wafer.
- This process produces a shallow, heavily doped layer.
- This is also known as **constant source diffusion**.

Drive in:

- After the desired amount of dopant atoms are deposited on Si wafer during pre-deposition, the dopant source is removed.
- Now, the temperature is increased to $1100^{O}C$ to $1250^{O}C$ and the drive in process begins and driving the impurities deeply into the semiconductor silicon wafer.
- As the source of dopants is removed after pre-deposition, the total amount of impurities in the wafer remains constant during drive in process.
- This reduces the surface concentration and increases the junction depth.
- This is also called as **constant dose diffusion**.
- The diffusion depth is decided by the precise control of the temperature and time of diffusion.

ION IMPLANTATION

- **Ion Implantation** is a method of doping in which the selected area of the surface of silicon wafer is bombarded with high energy (10,000ev) impurity ions. These high energy dopant ions can penetrate deeply into the Si semiconductor.
- The faster the dopant ions 'shot' at the silicon wafer, the deeper they penetrate. On entering the silicon wafer, due to collision with electrons and nuclei of silicon atoms, they lose their energy and stops penetration.
- A simplified setup for ion implantation process is shown in the figure.



Procedure:

- Ion source consists of the dopant material such as 'B' or 'P' within a strong electric field.
- This electric field is strong enough to separate the dopant atoms into constituent ions forming charged gaseous plasma.
- These charged ions are then accelerated to the desired velocity by the control of high voltage in the accelerator system.
- Then, these charged high velocity ions are focused into a narrow beam of high velocity ions having current of the order of 1 mA.
- The beam is turned through 90^0 by using an analysing magnet. The unwanted impurities in the beam are removed in analysing magnet.

- The magnetic field in the analysing magnet is set up in such a way that only the desired dopant turns through right angle (90^O) and the unwanted impurities having different mass from that of the desired material are turned by different angle and are screened out by 'Y' plates.
- The focused beam of dopant ions is then passed through 'X' scanning plates which helps in proper implantation of ion beam over the target silicon wafer.
- The ion beam is moved over the target wafer up and down, as the implantation has to be done bit by bit.
- The depth of penetration of any particular type of ion will increase with increasing accelerating voltage.
- After the ion implantation process, the silicon wafer is subjected to annealing process at a temperature of 800-1000^{o}C for period of 20 to 30 minutes to restore any mechanical damage on silicon wafer.

Annealing is done mainly to achieve the following:

- The semi-conductor Si wafer can regain its crystal structure back to single crystal which is important for efficient device operation.
- It allows the dopant material to fit substantially into the silicon crystal lattice.

Though ion implantation is more expensive process than conventional diffusion, it offers the following **advantages**.

- The depth of the doping levels can be precisely controlled, because both the accelerating voltage and the ion beam current are electrically controlled outside the apparatus.
- Extreme purity of dopants can be added.
- Uniform doping over the silicon surface is possible.
- Doping area can be precisely defined since the spread of the directed ion beam is very little.
- As it is a low temperature process, the movement of impurities is less within the Si wafer.

IMPLANTATION DOSE (Q_0).

- The total **Implantation Dose (Q_0)** over the targeted silicon wafer can be calculated by using the expression

$$\mathbf{Q_0 = Jt/q\ cm^{-2}}$$

where '**J**' is **ion beam current density**; '**t**' is implantation time and '**q**' is **electric charge**.

NUMERICAL PROBLEMS ON ION IMPLANTATION

Lesson Plan: Q. No: 12

Phosphorus is implanted in a n-type silicon sample with a uniform doping concentration of $5X10^{16}$atoms/cm^3. If the beam current density is 2.5µA/cm^2 and the implantation time is 8 minutes, calculate the implantation dose.

Given:

- Concentration of dopant atoms 'P' on silicon wafer = $5X10^{16}$ atoms/cm^3
- Ion beam current density = J = 2.5µA/cm^2 = $2.5X10^{-6}$ A/cm^2
- Implantation time = t = 8 minutes = 8X60 = 480 seconds
- Electric charge = q = $1.6X10^{-19}$ A-Sec

Solution:

- **Implantation Dose = Q_0 = Jt/q cm^{-2}.**

  Q_0 = ($2.5X10^{-6}$ X 480) / $1.6X10^{-19}$cm^{-2}

❖ **Implantation Dose = Q_0 = $7.50X10^{15}$ cm^{-2}.**

Lesson Plan: Q. No: 13

Boron is implanted in a p-type silicon sample with a uniform doping concentration of $2X10^{15}$atoms/cm^3. If the beam current density is 1mA/cm^2, calculate the time required to realize the implantation dose of 5 x10^{15} per cm^3.

Given:

- Concentration of dopant atoms 'B' on silicon wafer = $2X10^{15}$ atoms/cm^3
- Ion beam current density = J = 1mA/cm^2 = $1X10^{-3}$ A/cm^2
- Electric charge = q = $1.6X10^{-19}$ A-Sec
- Implantation dose = Q_0 = $5X10^{15}$cm^{-2}

Solution:

- **Implantation Time = t = Q_0 q /J seconds.**

  t= ($5X10^{15}$ X $1.6X10^{-19}$) / $1X10^{-3}$ seconds

❖ **Implantation Time = t = 0.8 seconds.**

Additional Problems:

1) Phosphorus is implanted in n-type silicon sample with a uniform doping concentration of $5x10^{16}$ atoms/cm^3. If the beam current density is 5μA/cm^2 and the implantation time is 6 min., calculate the implantation dose. Given: Electric charge, q = $1.6X10^{-19}$ A-Sec.

2) Boron is implanted in p-type silicon sample with a uniform doping concentration of 2 x 10^{15} atoms/cm^3. If the beam current density is $3X10^{-4}$ A/cm^2, what is the time required to realize the implantation dose of 6 $x10^{15}$ per cm^{-2}. Given: Electric charge, q = $1.6X10^{-19}$ A-Sec.

EPITAXIAL GROWTH

- **Epitaxy** is the process of growing a crystalline layer over a crystalline substrate.

  In the epitaxial process, the substrate wafer acts as a seed crystal, thus preserving the overall single crystal structure. Hence, epitaxially grown layer has the same crystal structure as that of the substrate.

- **Homoepitaxy**: When the grown layer and the substrate are of same material, then the process is known as homoepitaxy or autoepitaxy. Example - Si grown on Si and GaAs grown on GaAs.

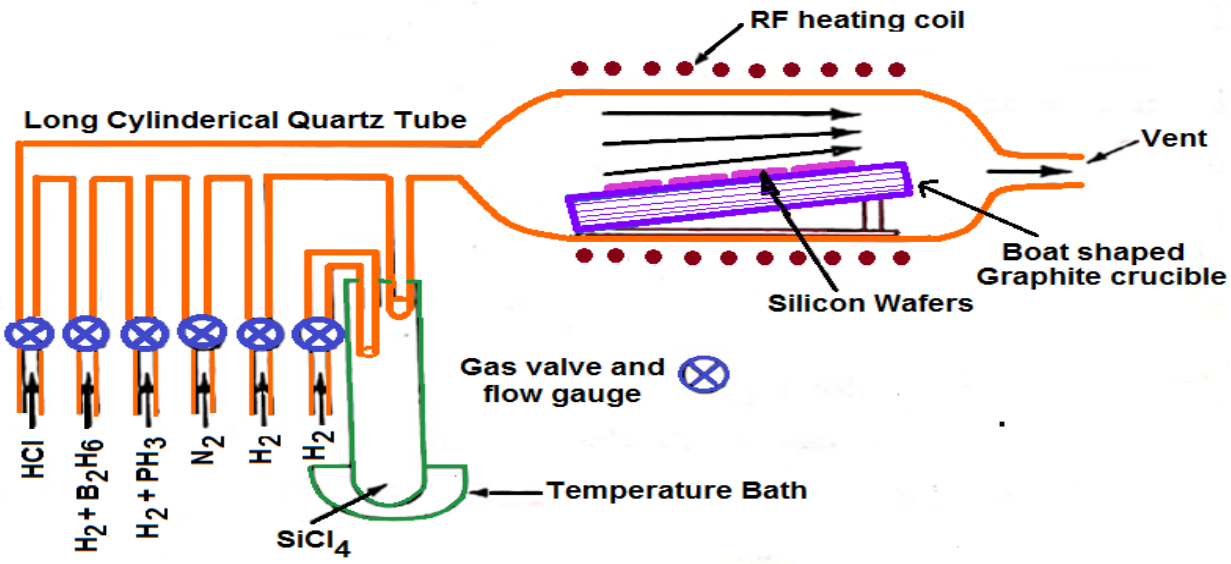
  In homoepitaxy, no problems of compatibility occurs because of similarity in orientation, chemical properties, lattice parameters and crystal structure of the epitaxial layer and the substrate on which it is grown.

- **Heteroepitaxy**: When the grown layer and the substrate are of different material, then the process is known as heteroepitaxy. Example - Si (diamond lattice) grown on sapphire (hexagonal) and GaAs on Si.

  In heteroepitaxy, the crystal structures of the layer and the substrate should be similar if crystalline growth is to be obtained. The substrate must be chemically and physically inert to the growth environment. There must be chemical compatibility between the materials.

- By diffusion or ion-implantation process, impurities such as ‘B’ or ‘P’ are driven into the silicon semiconductor wafer. But **in epitaxial growth, a layer of doped semiconductor is grown over the existing semiconductor which may be of any doping**.

- A simplified setup for growing epitaxial layer is shown in the fig.



Epitaxial Growth System

Procedure

- The silicon wafers are placed in a boat shaped graphite crucible and kept in a long cylindrical quartz tube with inlets and outlet for gases.
- The reactive gases are introduced into the reaction chamber based on the selection of semiconductor material and the dopant atoms.
- The system is heated by RF coil to a temperature of 1200^{o}C. At this temperature, semiconductor formation takes place and grows on the silicon semiconductor substrate.
- The by product gases like H_2 and HCl are vented away from the quartz tube.
- The thickness of the layer varies from 3 to 30 microns. This type of epitaxial growth is called as vapour phase epitaxial growth.

Steps involved in vapour phase epitaxial growth:

- Hydrogen gas is passed to purge the reactor of any impurities.
- HCl gas is passed for vapour phase etching of silicon semiconductor wafer surface at a temperature of 1150^{O}C to 1250^{O}C for 3 minutes. Thin region of damaged Si is removed from the silicon wafer surface by means of HCl etching.

$$Si_{(S)} + 4HCl_{(g)} \rightarrow SiCl_{4\,(g)} + 2H_{2\,(g)}.$$

- Vapours of H_2 and $SiCl_4$ are passed into the reaction chamber for producing **silicon on silicon** epitaxial layer. This process of epitaxial growth is known as **chemical vapour deposition** as all the chemicals introduced and that take part in the reactions are in the form of gaseous state.

$$\mathbf{SiCl_{4\,(g)} + 2H_{2\,(g)} \rightarrow Si_{(S)} + 4HCl_{\,(g)}.}$$

- H_2 and Diborane (B_2H_6) are supplied for p-type epitaxial layer growth on silicon wafer.
- H_2 and Phosphene (PH_3) are supplied for n-type epitaxial layer growth on silicon wafer.
- Once the growth is completed, the dopant atoms and silicon flows are eliminated and temperature is reduced by shutting the power off.
- Hydrogen gas is passed to purge the reactor of any impurities left out in the reactor.
- As the reactor cools down to ambient temperature, the H_2 flow is replaced by N_2 flow so that the reactor may be opened up safely.

Advantages of using $SiCl_4$ as source:

- $SiCl_4$ is non-toxic, inexpensive and easy to purify.
- The reaction of $SiCl_4$ and the formation of Si takes place only on the Si surface and not on boat or reaction chamber walls.