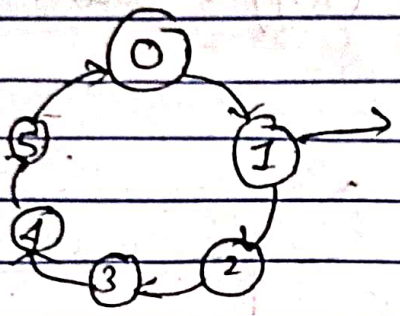
Counter.

A counter is a cascade of flipflop's configured to output a specific sequence on application of a clock. Each output of the sequence is dependent on the contents of the flipflops & is called a state of the counter.

The modulus of a counter is the total no. of states of the counter.



6 - states
modulo 6 / mod 6

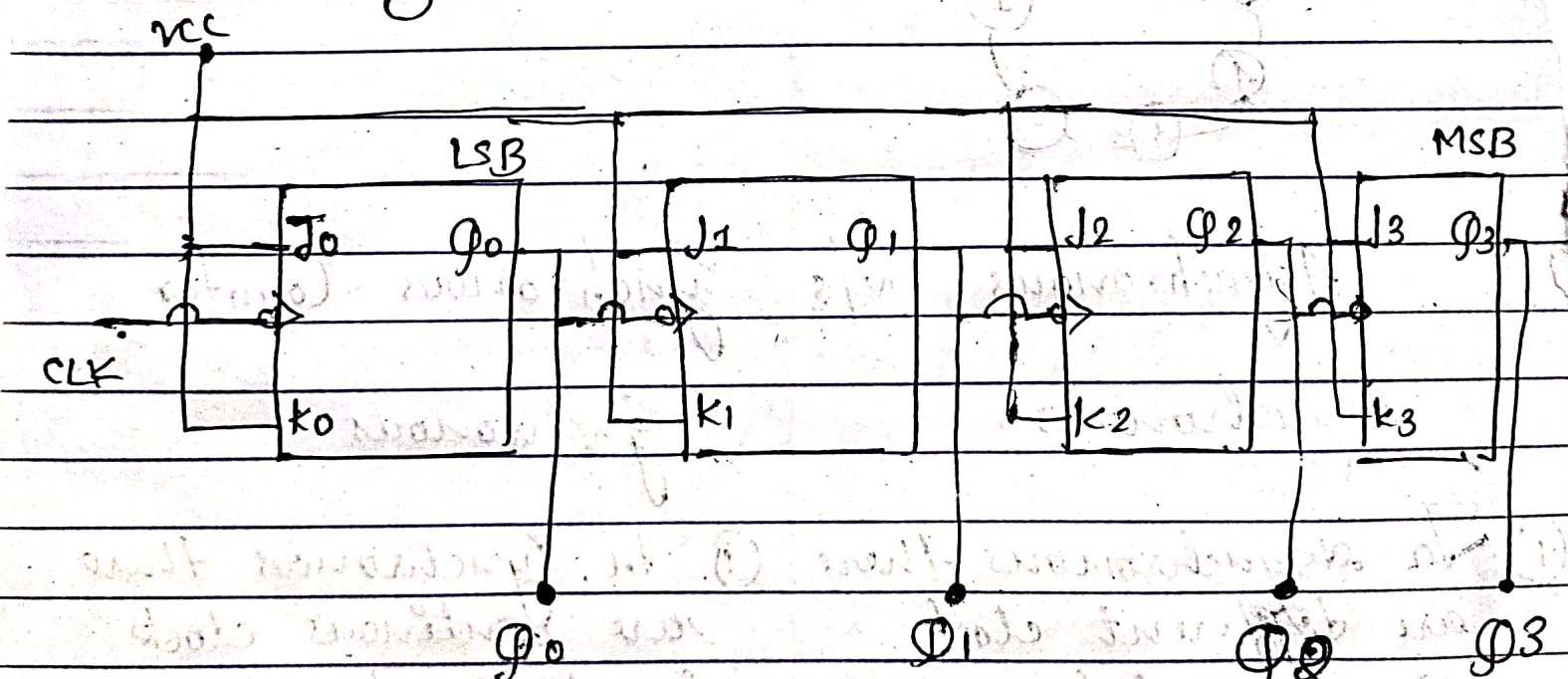
Asynchronous v/s Synchronous Counter

Asynchronous	Synchronous
(1) In Asynchronous there are different clock signals used to produce the output.	(1) In Synchronous there are continuous clock input signals or same clock pulse to produce the output.
(2) Operation is low	(2) Operation is faster
(3) Also known as serial counter.	(3) Also known as parallel counter
(4) produces more errors than Synchronous counter	(4) produces lesser error than asynchronous counter.

Asynchronous Counter	Synchronous Counter
(5) Design of the counter is simple	(5) Design of the counter is complex
(6) Can work with a fixed number of count sequences	(6) Can work with a flexible number of count sequences.

(1) 4-bit binary ripple-up counter using Asynchronous Counters (Ripple Counter).

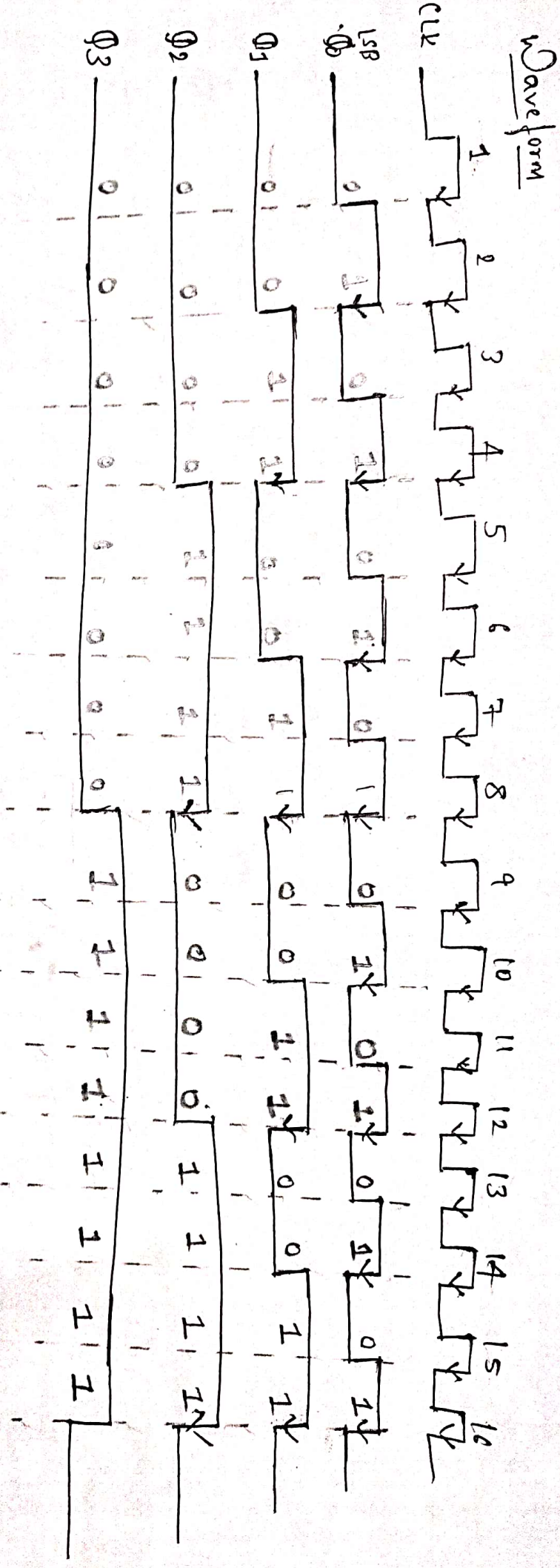
Block diagram



Truth table

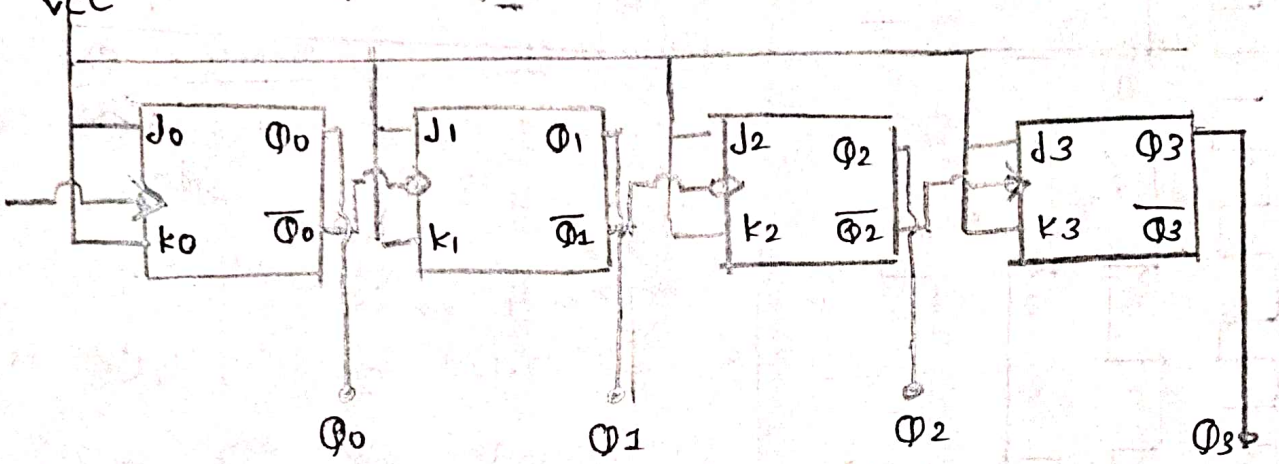
CLK	Q_3	Q_2	Q_1	Q_0	
↓	0	0	0	0	0
↑	0	0	0	1	1
↑	0	0	1	0	2
↑	0	0	1	1	3
↑	0	1	0	0	4
↑	0	1	0	1	5
↑	0	1	1	0	6
↑	0	1	1	1	7
↑	1	0	0	0	8
↑	1	0	0	1	9
↑	1	0	1	0	10
↑	1	0	1	1	11
↑	1	1	0	0	12
↑	1	1	0	1	13
↑	1	1	1	0	14
↑	1	1	1	1	15

Waveform



② 4-bit binary ripple-down counter using negative edge triggered JK flip flop.

⇒ Block diagram



Q_0 triggers at -ve edge of clock pulse

Q_1 triggers at -ve edge $\overline{Q_0}$ (+ve edge of Q_0)

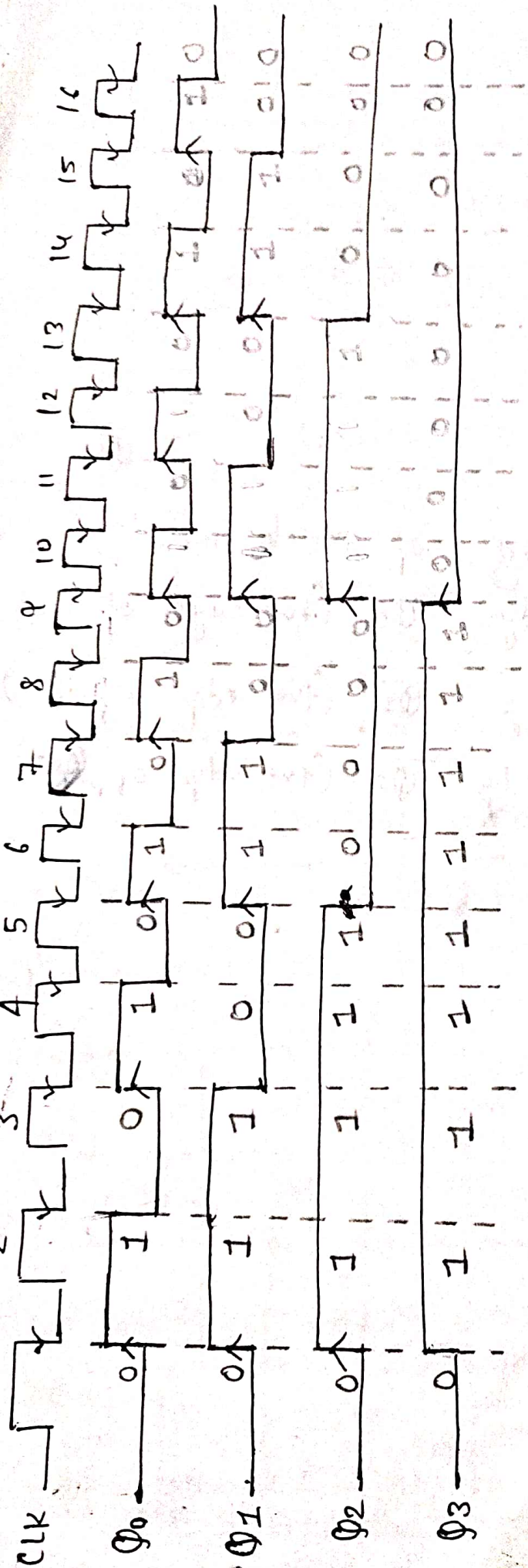
Q_2 triggers at -ve edge $\overline{Q_1}$ (+ve edge of Q_1)

Q_3 triggers at -ve edge $\overline{Q_2}$ (+ve edge of Q_2).

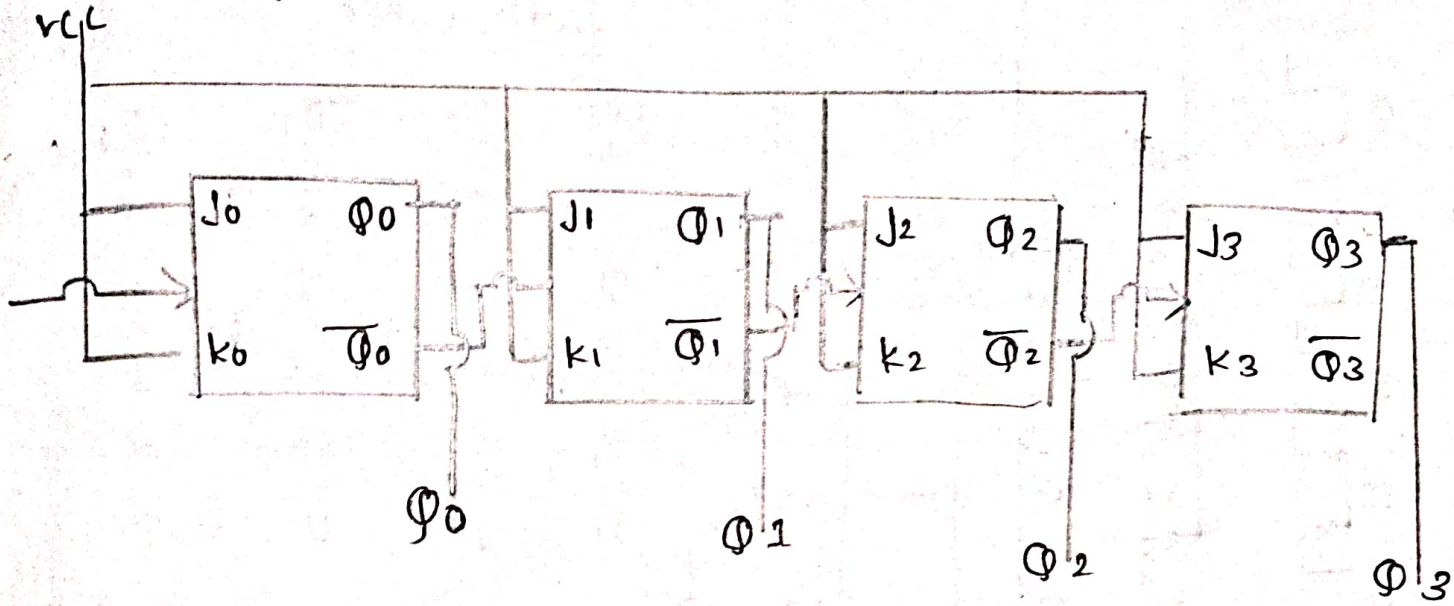
Truth table

Q_3	Q_2	Q_1	Q_0	
1	1	1	1	-15
1	1	1	0	-14
1	1	0	1	-13
1	1	0	0	-12
1	0	1	1	-11
1	0	1	0	-10
1	0	0	1	-9
0	0	0	1	-8
1	1	1	0	-7
0	1	1	0	-6
0	1	0	1	-5
0	1	0	0	-4
1	1	0	0	-3
0	1	0	0	-2
1	0	0	0	-1
0	0	0	0	-0

Waveform.



③ 4-bit binary ripple up counter using +ve edge triggered JK ff



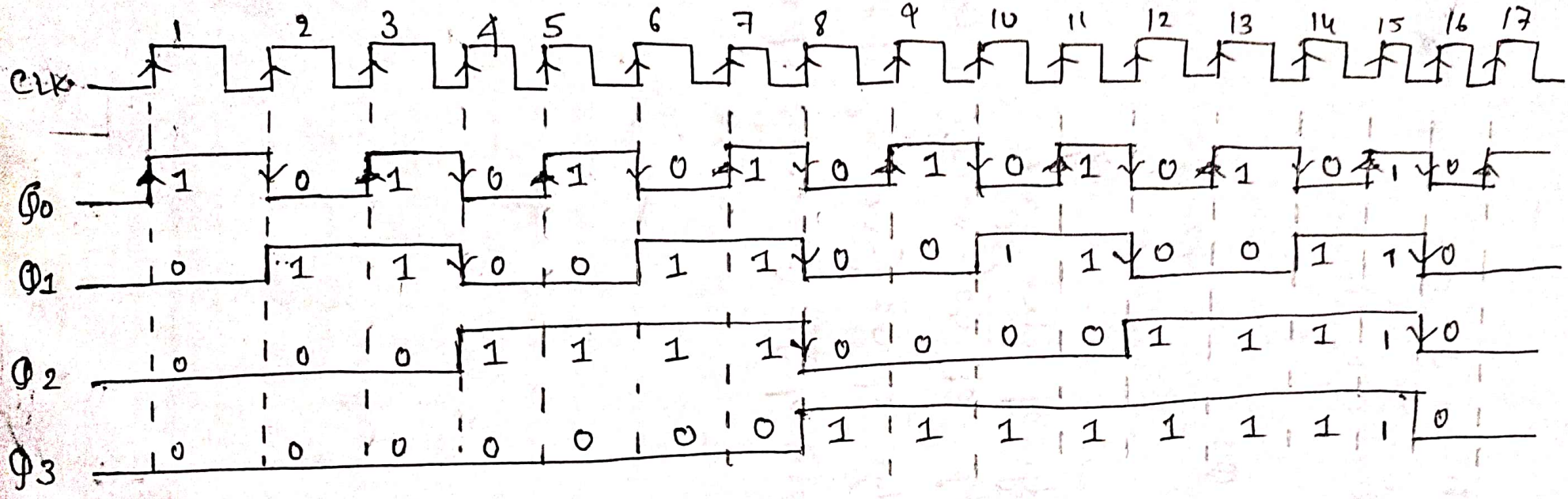
Q_0 toggles at +ve edge of clock pulse

Q_1 triggers at +ve edge of $\overline{Q_0}$ (-ve edge of Q_0)

Q_2 triggers at +ve edge of $\overline{Q_1}$ (-ve edge of Q_1)

Q_3 triggers at +ve edge of $\overline{Q_2}$ (-ve edge of Q_2).

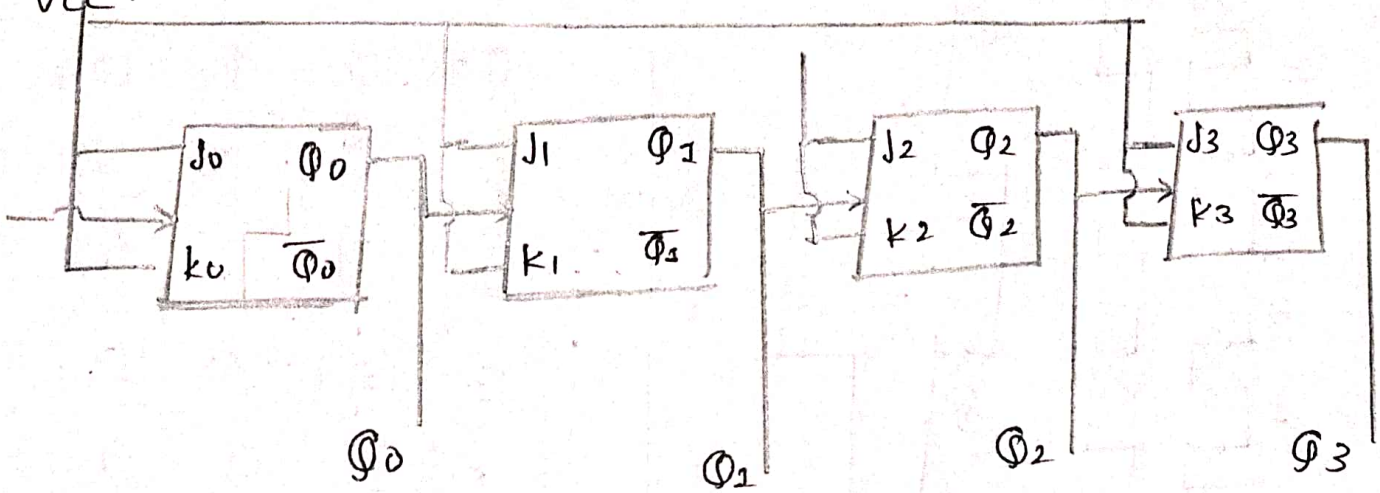
Waveform.



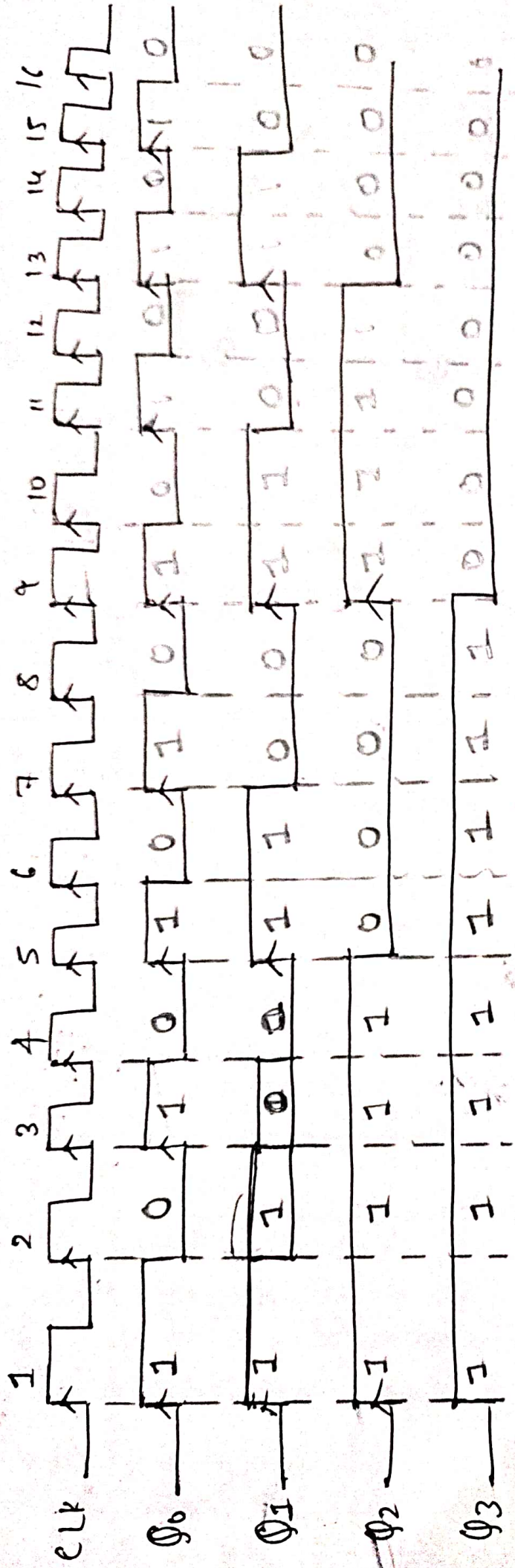
Truth table

S	Q_0	Q_1	Q_2	Q_3
0	1	0	0	0
1	0	1	0	0
2	1	1	0	0
3	0	0	1	0
4	1	0	1	0
5	0	1	1	0
6	1	1	1	0
7	0	0	0	1
8	1	0	0	1
9	0	1	0	1
10	1	1	0	1
11	0	0	1	1
12	1	0	1	1
13	0	1	1	1
14	1	1	1	1
15	0	0	0	0

④ 4-bit binary ripple-down counter using +ve edge triggered JK flip flop



Waveform.



Truth table.

Q_3	Q_2	Q_1	Q_0	
1	1	1	1	- 15
1	1	1	0	- 14
1	1	0	1	- 13
1	1	0	0	- 12
1	0	1	1	- 11
1	0	1	0	- 10
1	0	0	1	- 9
1	0	0	0	- 8
0	1	1	1	- 7
0	1	1	0	- 6
0	1	0	1	- 5
0	1	0	0	- 4
0	0	1	1	- 3
0	0	1	0	- 2
0	0	0	1	- 1
0	0	0	0	- 0