DEPARTMENT OF ELECTRICAL ENGINEERING

IIT BOMBAY

Project Report on

Comparison of Wallace and Dadda Multiplier

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Master of Technology, Electronic Systems

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Objective: Comparative study of 16*16-bit unsigned Wallace & Dadda multiplier based on worst case delay.

Theory:

Dadda Multiplier: Dadda multiplier involves the generation of partial product, collect all partial products bits with the same place value in bunches of wires and reduce these in several layers of adders till each weight has no more than two wires. Then use a fast adder of appropriate size at the end. The reduction of wires in Dadda should be as late as possible.

Reduction of wire:

1) Wires in every layer can't exceed from layer capacity. The capacity of each layer is an integer part of 1.5 times the next layer capacity (from the end).

2) We know final adder can take no more than two wire. So end layer capacity will be 2. The layer previous to this will have capacity 3. Similarly going above the capacity will be 4,6,9,13.... and so on.

3) While reducing the wires at each weight we will use HA or FA only when passing the wires from one layer to next layer exceeds its capacity.

Dot diagram of 16*16 Dadda multiplier

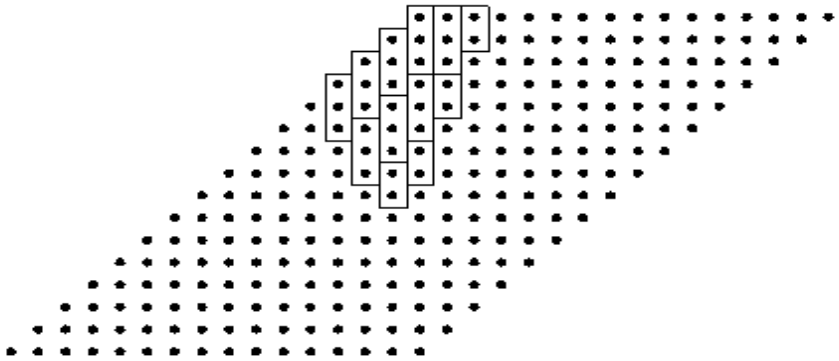
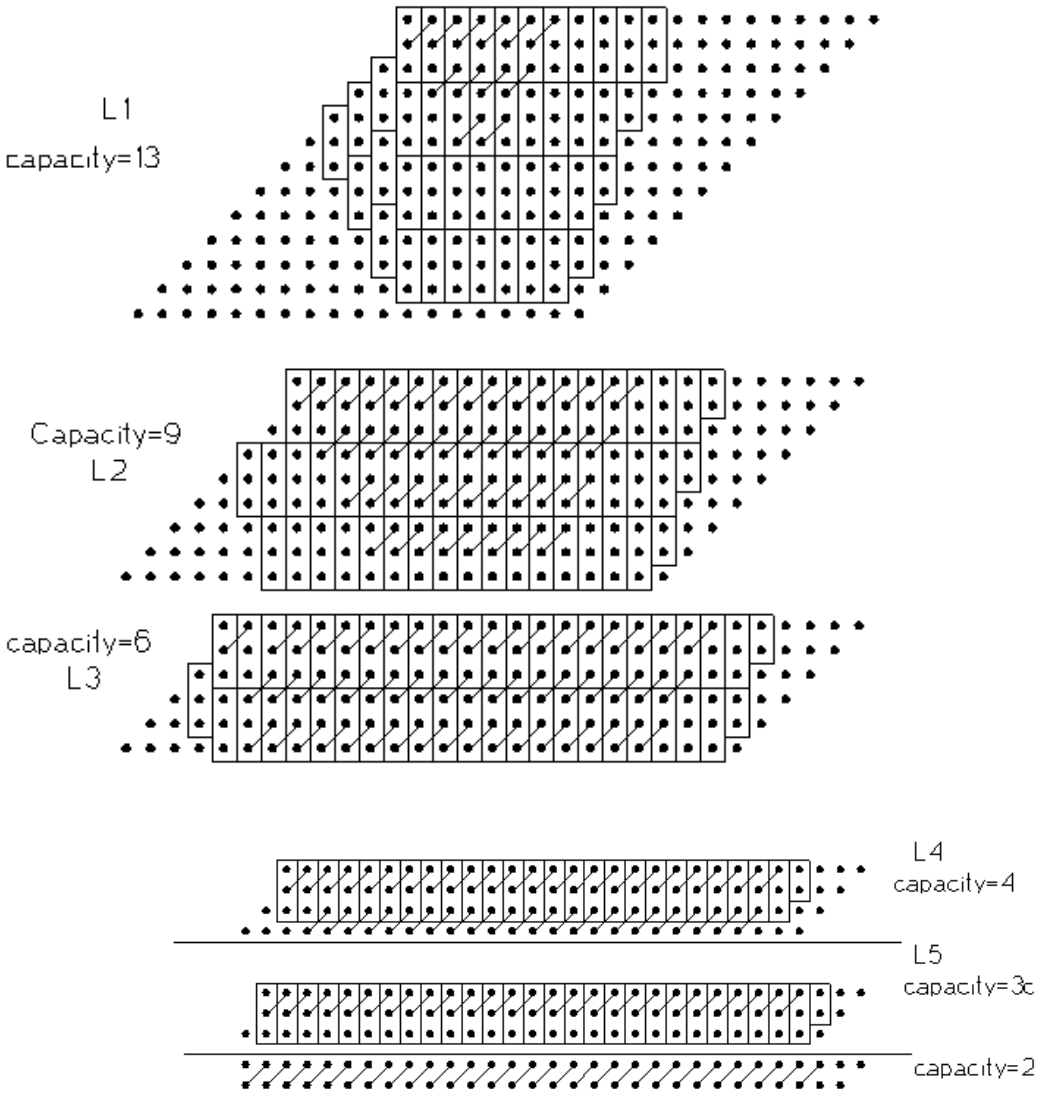


Fig: partial product (16*16)

Maximum wire at any weight is 16. So the capacity of the next layer would be 13. Wires at weight 14 exceeds the capacity 13 of the next layer. So HA is used to reduce one wire. At weight 15 total wire will be 16(15 partial product & 1 carry of the previous HA). So to reduce wires to 13 FA & HA is used. Similar approach is done for others weight.



In last layer 6 all the weight does not have wire more than 2. So there will be no further reduction. To get the result of multiplication we will use 32-bit Brent-Kung adder.

Wallace Multiplier: The reduction of wires in Wallace should be as early as possible.

Reduction of wire:

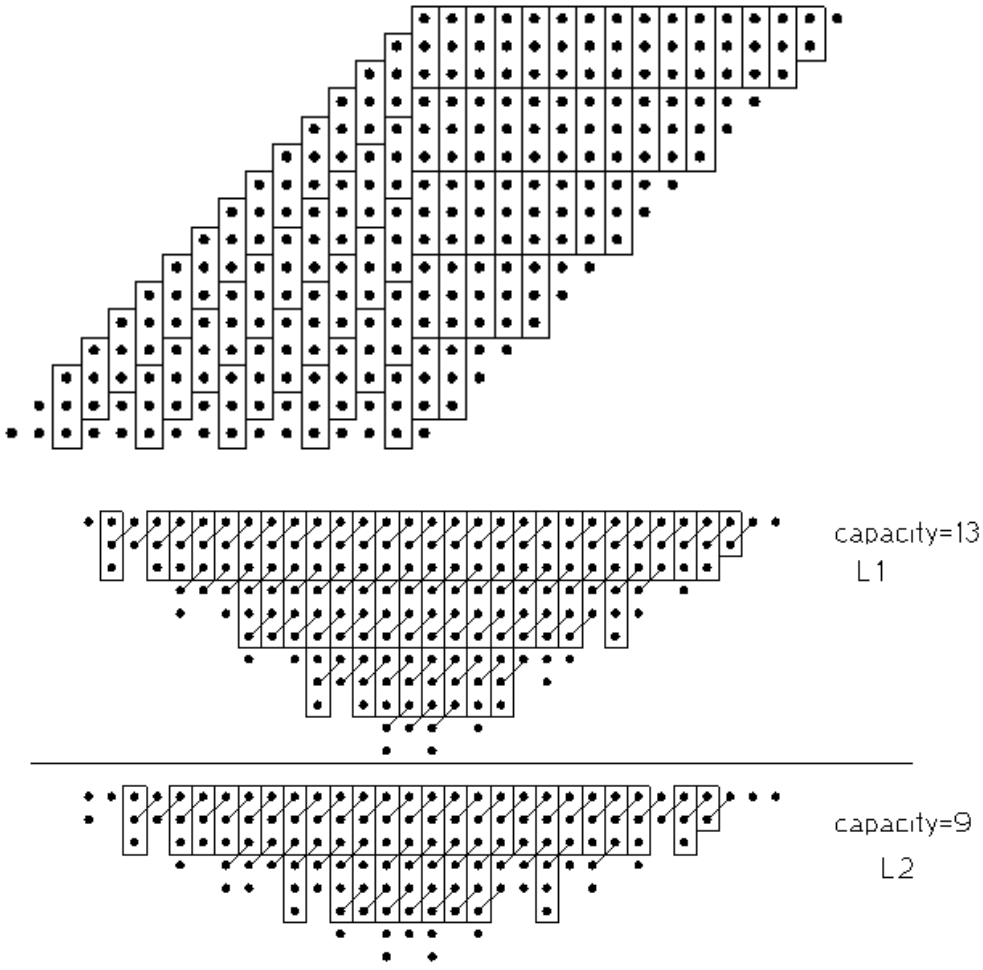
1) Wires in every layer can't exceeds from layer capacity. The capacity of each layer is integer part of 1.5 times of the next layer capacity (from the end).

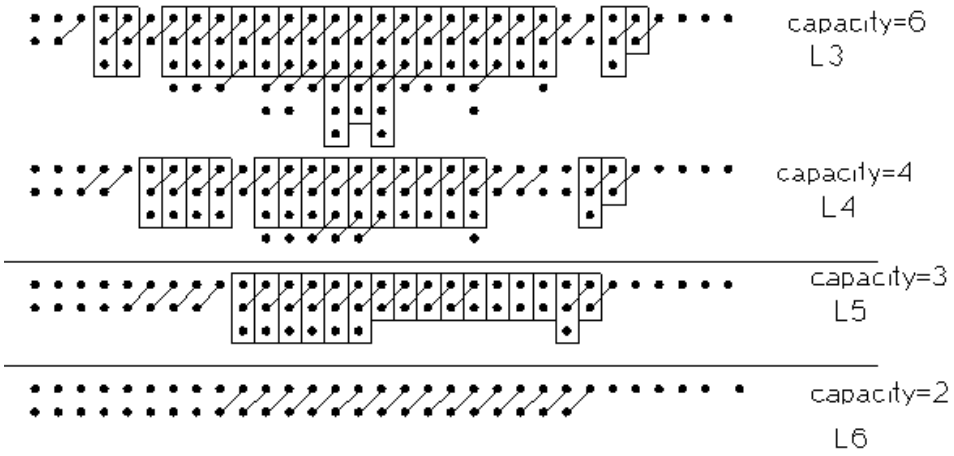
2) Pass the single wire to the next layer directly.

3) Pass the bunch of 3 wire to FA.

4) We have to take the decision for the 2 wire. if all columns at the right have a single wire, we reduce the two wires using a half adder. If there is a column to the right with more than one wire, we pass through the two wires to the next layer if it can accommodate these. (That is, the total number of wires do not exceed the capacity of that layer). If passing through the two wires would exceed the capacity of next layer, we reduce these with a half adder.

Dot diagram of 16*16 Wallace multiplier:





Results & Resources for 16*16 Dadda Multiplier:

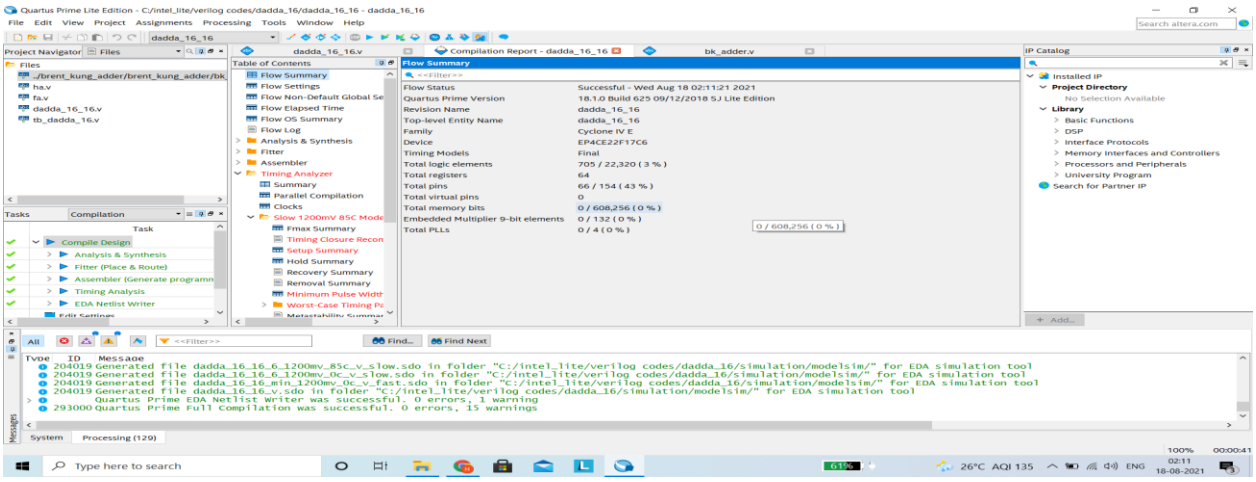


Fig: Resources Used

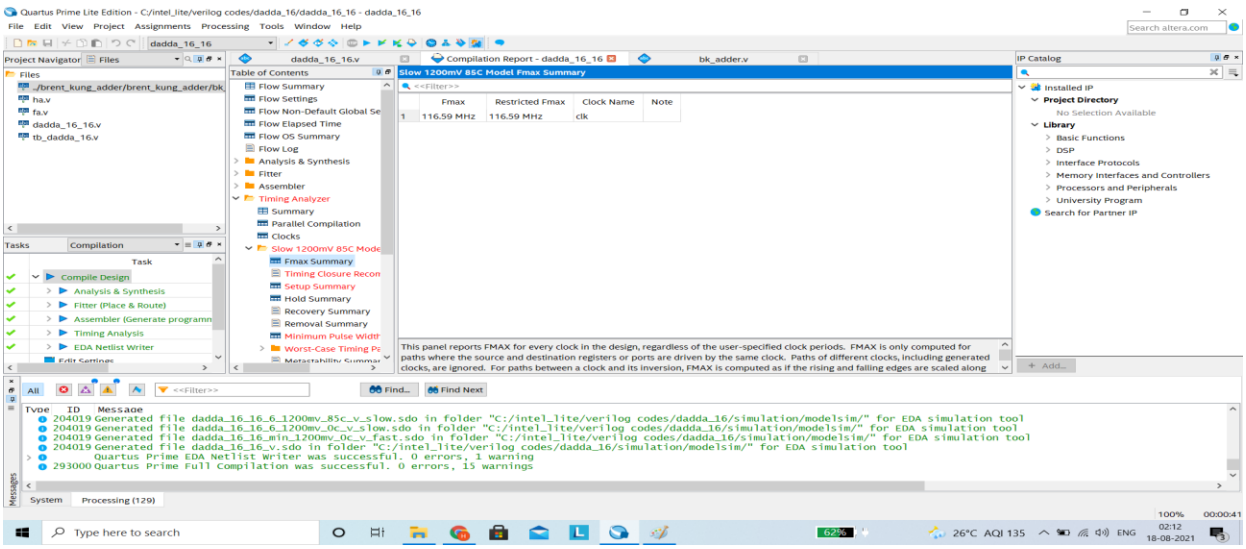


Fig: Frequency required

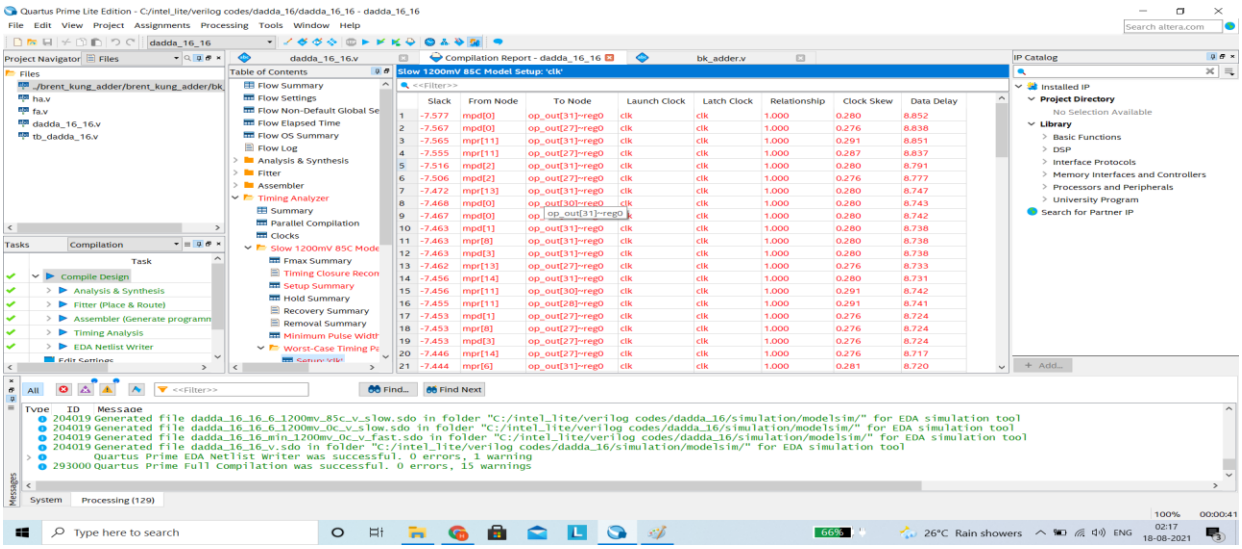


Fig: Slack for this design

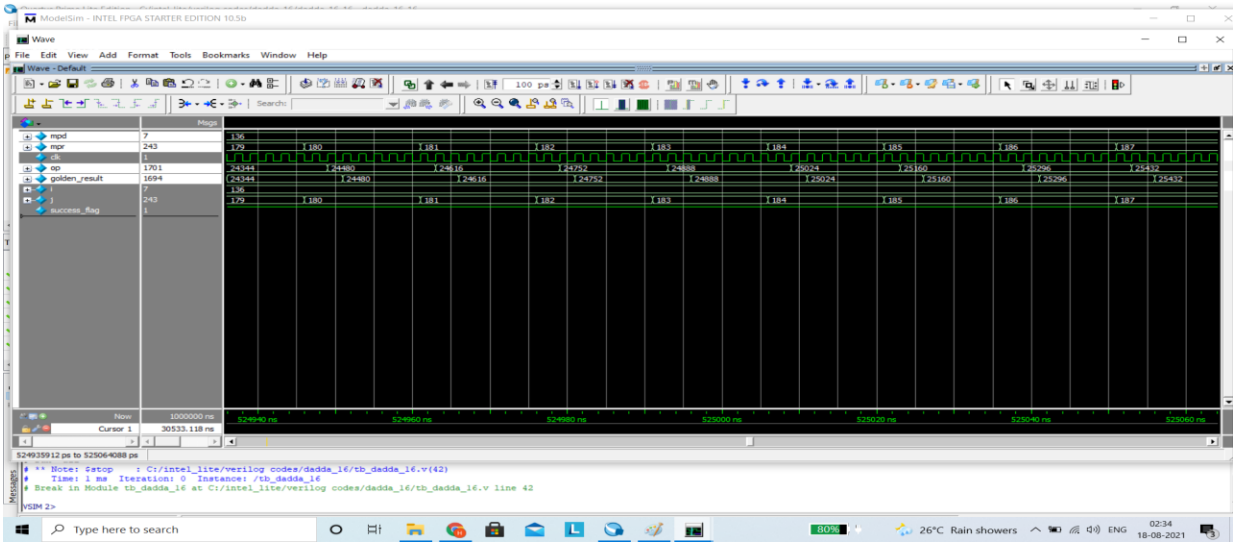


Fig: Simulation Result

Results & Simulation for 16*16 Walace Multiplier:

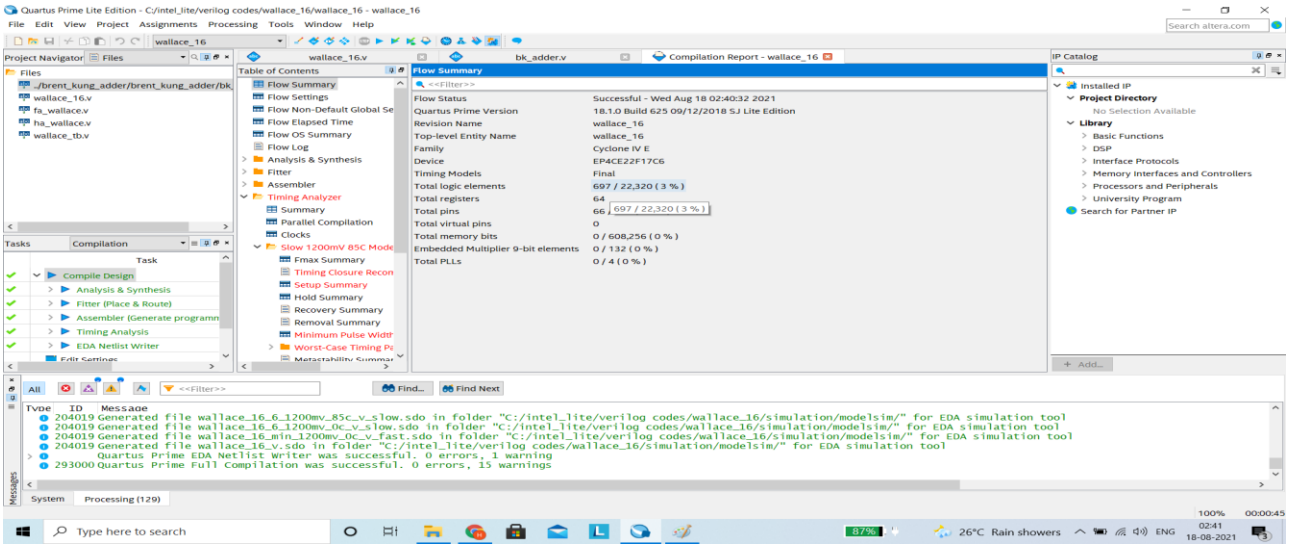


Fig: Resources Used

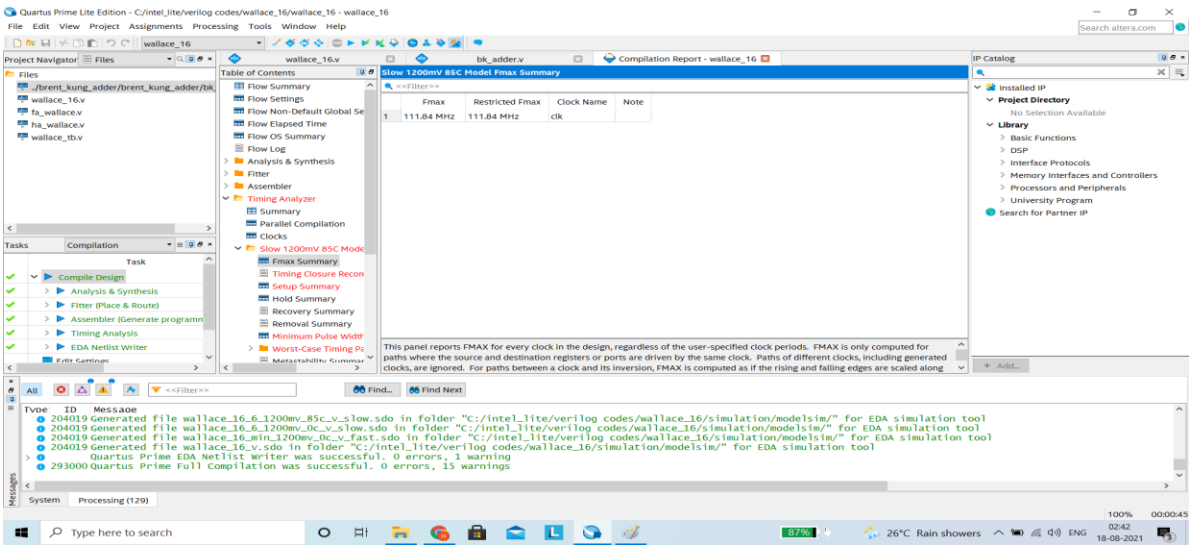


Fig: frequency Required

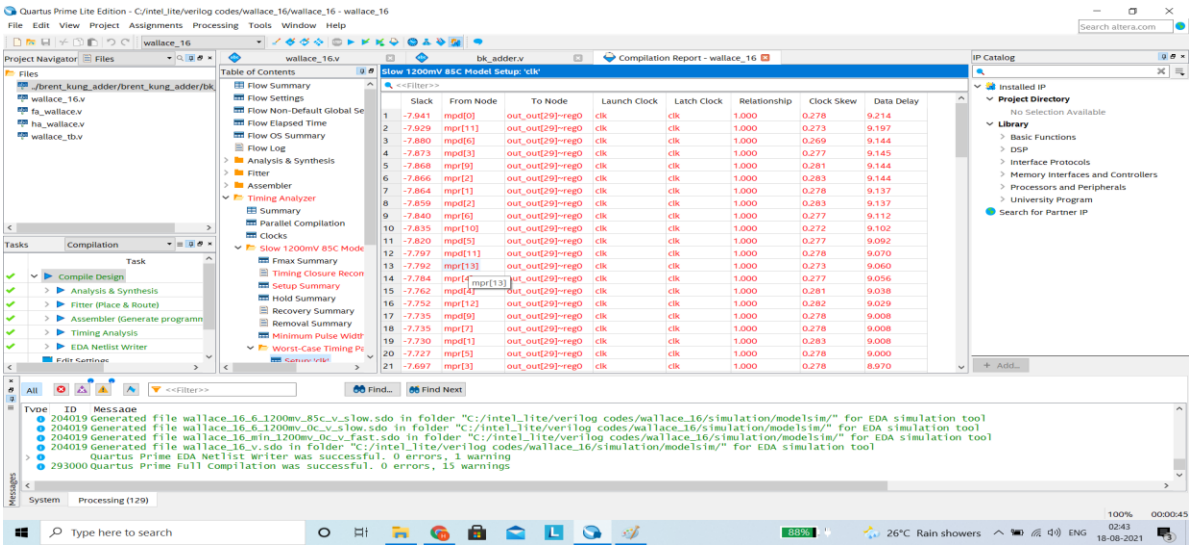


Fig: Slack of design

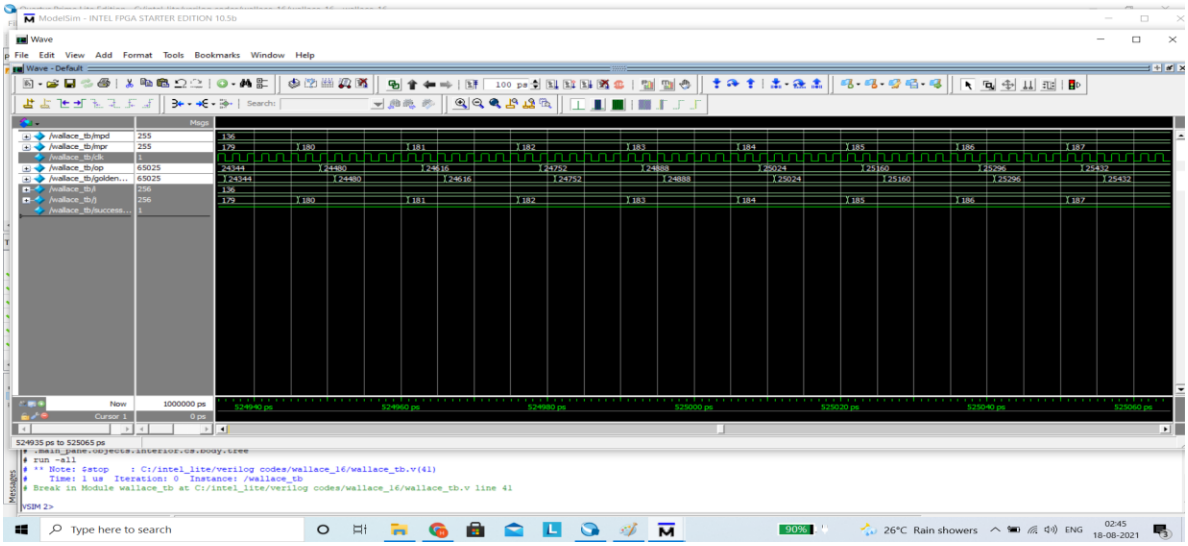


Fig: Simulation & Result

Conclusion: Frequency of dadda is high. So Dadda is faster than Wallace.