BhadaleIT - QAI R&D LAB — OPERATING MANUAL v1.1 (Full Expanded Edition) Hybrid Executive + Engineering Edition (2025–2030)

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SECTION 1 — Executive Summary

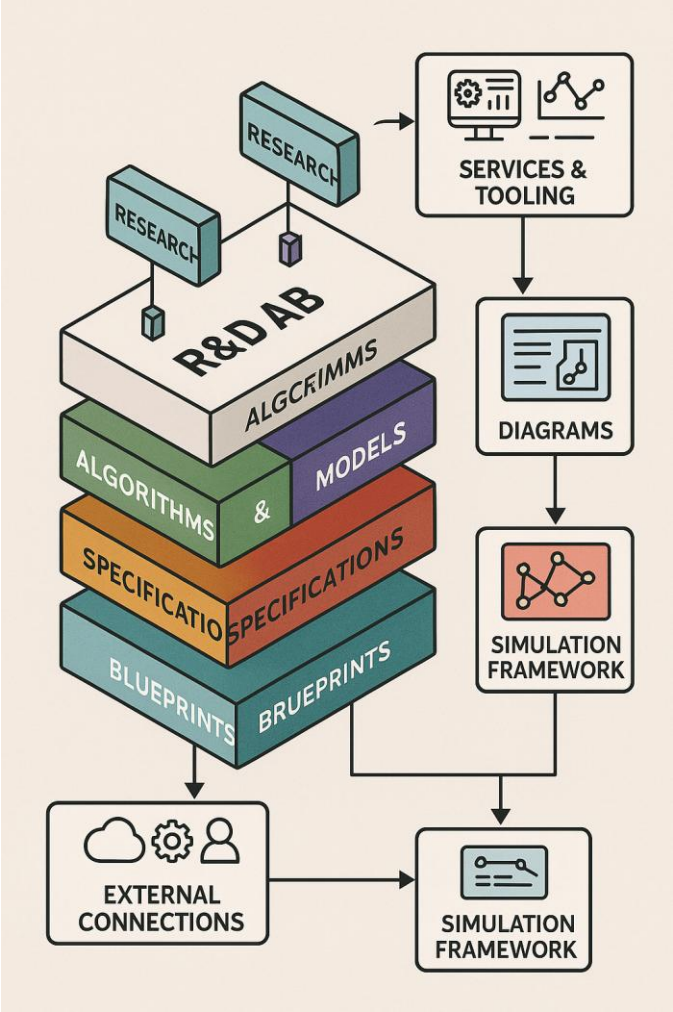
The Quantum AI (QAI) R&D Lab serves as the central research engine enabling foundational quantum mechanics exploration, quantum AI model development, compiler work, advanced control systems, and frontier theoretical directions including QQM, Categorical QI, and relativistic communication.

This manual integrates:
- US_QAI_Unified_Roadmap_v1.5
- QAI Product Foundry Framework
- QAI RnD Lab Blueprint
- QAI TTO Suite & IP Protection Models
- Rolling PCT & Secure Commercialization Program

The objective: create a scalable, federally aligned R&D ecosystem capable of accelerated innovation, robust IP generation, and high- value acquisition readiness.

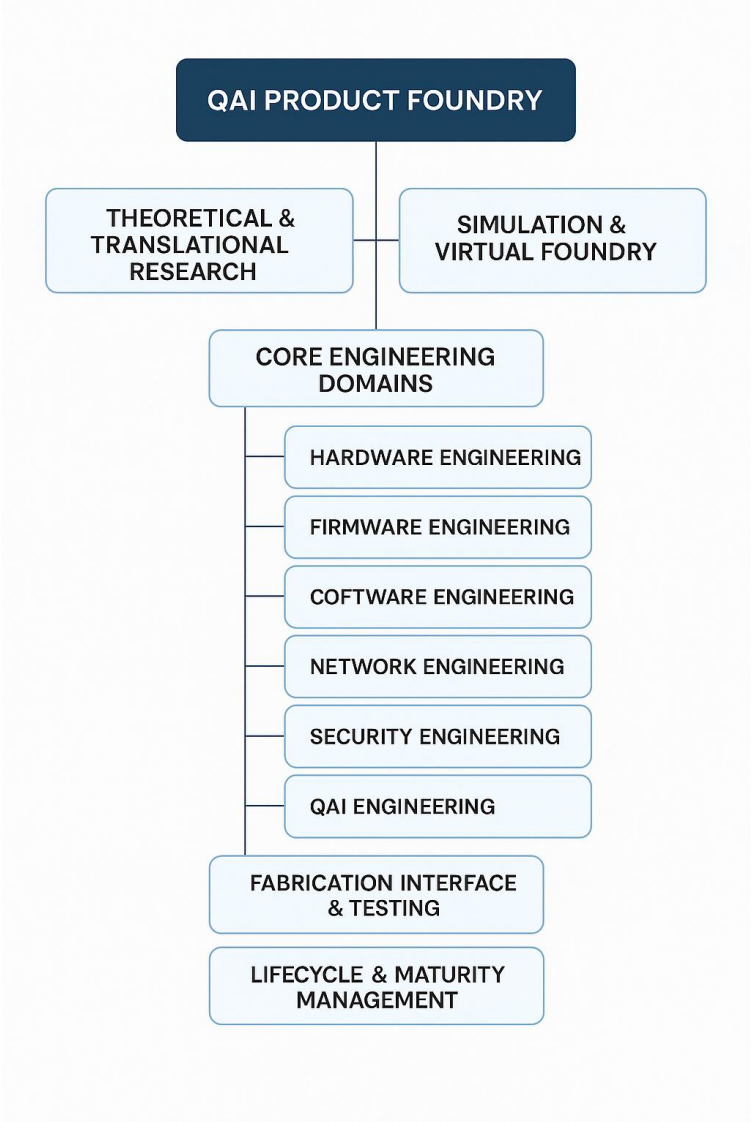
SECTION 2 — Organizational Structure

The R&D Lab operates using Divisions → Tracks → Working Groups.



The 12 Tracks from the Roadmap form the core execution engine. Each WG executes sprint cycles, simulation experiments, prototype development, or theoretical tasks feeding downstream engineering.

SECTION 3 — Research Operating Model



The research-to-product pipeline:
1. Fundamental Research (Math, Physics, Algorithms)
2. Model Development (QAI, QNNs, QEC, QQM frameworks)
3. Specifications (Interface definitions, compiler IRs, control systems)
4. Blueprints (Hardware, firmware, and architectural designs)
5. Simulation (Virtual testing, logical verification, benchmarking)
6. Prototype & PoC (Engineering validation)
7. Product Foundry Handoff

SECTION 4 — Simulation & Tooling Framework

Simulation is central to all R&D activities. Approved tools include:

Quantum Simulators:
- Qiskit Aer
- PennyLane
- AWS Braket Local Simulator
- Xanadu Strawberry Fields
- QAI custom simulators (internal)

Classical Tooling:
- GitLab private runners
- Local Colab notebooks with encryption
- FPGA/ASIC simulation suites
- Microwave/RF simulators

Every simulation generates:
- Hypothesis Report
- Simulation Log
- Verification Summary
- WG Review Notes

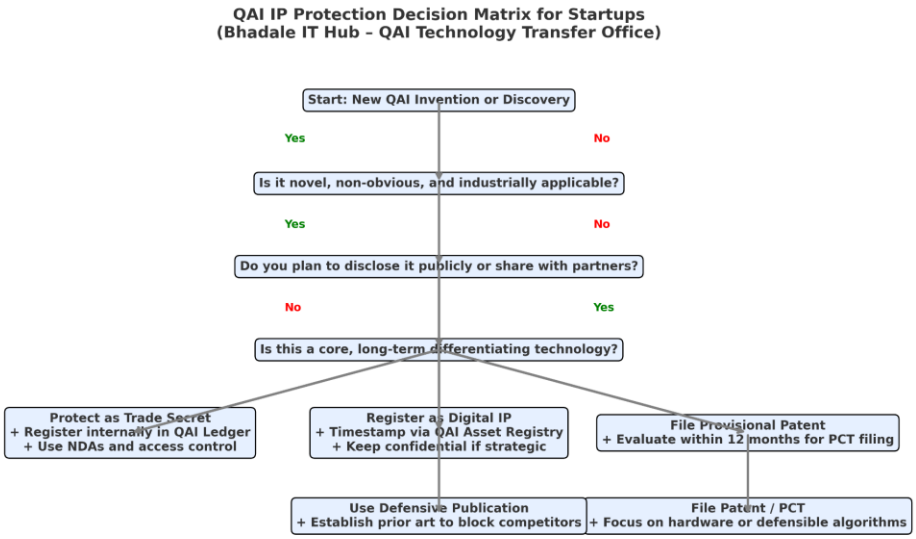
SECTION 5 — Prototype, PoC & Product Engineering Flow

The Product Foundry receives validated research outputs. R&D Lab produces:

- Qubit control algorithms
- Compiler modules
- Mathematical proofs
- System architecture blueprints
- Communication protocol PoCs
- Firmware blocks
- Error correction modules

Each output must pass:
1. WG Review
2. Simulation Validation
3. Engineering Integration
4. TTO IP Pre- screen

SECTION 6 — IP, Patents & Commercialization



All discoveries follow the TTO workflow:
• Novelty screening
• Prior art mapping
• Decision path (Patent / PCT / Trade Secret / Defensive Publication / Digital IP)
• Filing preparation
• Rolling PCT & Secure Commercialization Program alignment

Joint IP projects follow the Collaborative IP Framework with:
• Universities
• Federal labs
• Industrial partners (under NDA)

SECTION 7 — Compliance, Security & Export Control

Mandatory frameworks:
• ITAR / EAR export control
• NIST 800-53 & PQC migration standards
• Internal data classification (Confidential / Restricted / Public Abstract Only)

Security includes:
• Access-controlled GitLab
• Encrypted vaults for IP
• Simulation sandbox isolation

• Partner identity verification
• Document watermarking

SECTION 8 — Operational Procedures & Sprint Cadence

Every WG operates in 2–4 week sprints:
1. Hypothesis Selection
2. Simulation & Experimentation
3. WG Integration Review
4. Filing Ready Output
5. Handoff to Product Foundry

Sprint outputs include:
• Hypothesis document
• Simulation results
• WG alignment notes
• IP-ready abstract
• Decision: Publish / File / Internal hold

SECTION 9 — Templates & Appendices

Included Templates:
• Hypothesis Template
• Simulation Report Template
• Specification Template
• Blueprint Template
• R&D → Foundry Handoff Checklist
• WG Charter Template
• Internal IP Log Sheet

Appendix A – Confidentiality & Intellectual Property Disclaimer

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