



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.

Jimson Mathew  
Priyadarsan Patra  
Dhiraj K. Pradhan  
A.J. Kuttyamma (Eds.)

Communications in Computer and Information Science

305

# Eco-friendly Computing and Communication Systems

International Conference, ICECCS 2012  
Kochi, India, August 2012  
Proceedings

**Volume Editors**

**Jimson Mathew**  
University of Bristol, UK  
E-mail: [jimson@cs.bris.ac.uk](mailto:jimson@cs.bris.ac.uk)

**Priyadarsan Patra**  
Intel Corporation, Hillsbro, OR, USA  
E-mail: [priyadarsan.patra@intel.com](mailto:priyadarsan.patra@intel.com)

**Dhiraj K. Pradhan**  
University of Bristol, UK  
E-mail: [pradhan@cs.bris.ac.uk](mailto:pradhan@cs.bris.ac.uk)

**A. J. Kuttyamma**  
Rajagiri School of Engineering and Technology  
Kochi, Kerala, India  
E-mail: [kuttyamma\\_aj@rajagiritech.ac.in](mailto:kuttyamma_aj@rajagiritech.ac.in)

ISSN 1865-0929  
ISBN 978-3-642-32111-5  
DOI 10.1007/978-3-642-32112-2  
Springer Heidelberg Dordrecht London New York

e-ISSN 1865-0937  
e-ISBN 978-3-642-32112-2

Library of Congress Control Number: 2012942857

CR Subject Classification (1998): I.4, I.2.4, C.2.1, E.3, I.6, J.3, H.3

© Springer-Verlag Berlin Heidelberg 2012

This work is subject to copyright. All rights are reserved, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, re-use of illustrations, recitation, broadcasting, reproduction on microfilms or in any other way, and storage in data banks. Duplication of this publication or parts thereof is permitted only under the provisions of the German Copyright Law of September 9, 1965, in its current version, and permission for use must always be obtained from Springer. Violations are liable to prosecution under the German Copyright Law.

The use of general descriptive names, registered names, trademarks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

*Typesetting:* Camera-ready by author, data conversion by Scientific Publishing Services, Chennai, India

Printed on acid-free paper

Springer is part of Springer Science+Business Media ([www.springer.com](http://www.springer.com))

# Table of Contents

## Energy Efficient Software System and Applications

- Energy-Aware Mobile Application Development by Optimizing GCC for the ARM Architecture ..... 1  
*Mahalingam P.R. and Shimmi Asokan*

- Compiler Efficient and Power Aware Instruction Level Parallelism for Multicore Architecture ..... 9  
*D.C. Kiran, S. Gurunarayanan, Faizan Khaliq, and Abhijeet Nawal*

- MotherOnt: A Global Grid Environment for Interconnecting the Ontologies Semantically to Enable the Effective Semantic Search ..... 18  
*Rohit Rathore, Rayan Goudar, Sreenivasa Rao, Priyamvada Singh, and Rashmi Chauhan*

## Wireless Communication Systems

- FFMS: Fuzzy Based Fault Management Scheme in Wireless Sensor Networks ..... 30  
*Prasenjit Chanak, Indrajit Banerjee, Tuhina Samanta, and Hafizur Rahaman*

- Evaluation of WSN Protocols on a Novel PSoC-Based Sensor Network ..... 39  
*Rakhee, P. Sai Phaneendra, and M.B. Srinivas*

- Improving Lifetime of Structured Deployed Wireless Sensor Network Using Sleepy Algorithm ..... 47  
*Jis Mary Jacob and Anita John*

- Cellular Automata Approach for Spectrum Sensing in Energy Efficient Sensor Network Aided Cognitive Radio ..... 54  
*Jaison Jacob, Babita R. Jose, and Jimson Mathew*

## Green Energy Technologies

- Economic Analysis of a Biomass/PV/Diesel Autonomous Power Plant ..... 62  
*Subhadeep Bhattacharjee and Anindita Dey*

- A Slope Compensated Current Mode Controlled Boost Converter ..... 69  
*K.G. Remya, Chikku Abraham, and Babita R. Jose*

Minimizing Energy of Scalable Distributed Least Squares Localization .....	77
<i>Diana Olivia, Ramakrishna M., and Divya S.</i>	
Multiple Fault Diagnosis and Test Power Reduction Using Genetic Algorithms .....	84
<i>J.P. Anita and P.T. Vanathi</i>	
A Novel Design of Reduced Order Controllers Using Exponential Observers for Large-Scale Linear Discrete-Time Control Systems .....	93
<i>Kavitha Madhavan and Sundarapandian Vaidyanathan</i>	
Adiabatic Technique for Designing Energy Efficient Logic Circuits .....	100
<i>Shari Jahan C.S. and N. Kayalvizhi</i>	

## Image and Signal Processing

Comparative Study of Recent Compressed Sensing Methodologies in Astronomical Images .....	108
<i>Nidhin Prabhakar T.V., Hemanth V.K., Sachin Kumar S., K.P. Soman, and Arun Soman</i>	
Speaker Recognition in Emotional Environment .....	117
<i>Shashidhar G. Koolagudi, Kritika Sharma, and K. Sreenivasa Rao</i>	
CBMIR: Content Based Medical Image Retrieval System Using Texture and Intensity for Dental Images .....	125
<i>B. Ramamurthy, K.R. Chandran, V.R. Meenakshi, and V. Shilpa</i>	
A Ridgelet Based Symmetric Multiple Image Encryption in Wavelet Domain Using Chaotic Key Image .....	135
<i>Arpit Jain, Musheer Ahmad, and Vipul Khare</i>	
Investigation of Quality of Metric in H.323 (VoIP) Protocol Coexisting of WLAN with WiMax Technologies of Different Network Loaded Conditions .....	145
<i>K. Sakthisudhan, G. DeepaPrabha, A.L. Karthika, P. Thangaraj, and C. MariMuthu</i>	
Kernel Based Automatic Traffic Sign Detection and Recognition Using SVM .....	153
<i>Anjan Gudigar, B.N. Jagadale, Mahesh P.K., and Raghavendra U.</i>	
Color Segmentation of 2D Images with Thresholding .....	162
<i>Hepzibah A. Christinal, Daniel Díaz-Pernil, Pedro Real Jurado, and S. Easter Selvan</i>	

Vowel Recognition from Telephonic Speech Using MFCCs and Gaussian Mixture Models . . . . .	170
<i>Shashidhar G. Koolagudi, Sujata Negi Thakur, Anurag Barthwal, Manoj Kumar Singh, Ramesh Rawat, and K. Sreenivasa Rao</i>	
A Robust Binary Watermarking Scheme Using BTC-PF Technique . . . . .	178
<i>Chinmay Maiti and Bibhas Chandra Dhara</i>	
Uniform Based Approach for Image Fusion . . . . .	186
<i>Radhika Vadhi, Veeraswamy Kilari, and Srinivaskumar Samayamantula</i>	
A Fast Image Reconstruction Algorithm Using Adaptive R-Tree Segmentation and B-Splines . . . . .	195
<i>Ravikant Verma and Rajesh Siddavatam</i>	

## Bioinformatics and Emerging Technologies

A Novel Algorithm for Hub Protein Identification in Prokaryotic Proteome Using Di-Peptide Composition and Hydrophobicity Ratio . . . . .	204
<i>Aswathi B.L., Baharak Goli, Renganayaki Govindarajan, and Achuthsankar S. Nair</i>	
Synchronization of Hyperchaotic Liu System via Backstepping Control with Recursive Feedback . . . . .	212
<i>Suresh Rasappan and Sundarapandian Vaidyanathan</i>	
New Feature Vector for Recognition of Short Microbial Genes . . . . .	222
<i>Baharak Goli, Aswathi B.L., Chinu Joy, and Achuthsankar S. Nair</i>	
Fault Resilient Galois Field Multiplier Design in Emerging Technologies . . . . .	230
<i>Mahesh Poolakkaparambil, Jimson Mathew, and Abusaleh Jabir</i>	

## Secure and Reliable Systems

A Novel Security Architecture for Biometric Templates Using Visual Cryptography and Chaotic Image Encryption . . . . .	239
<i>Divya James and Mintu Philip</i>	
A New Fault-Tolerant Routing Algorithm for MALN-2 . . . . .	247
<i>Nitin and Durg Singh Chauhan</i>	
Multilanguage Block Ciphering Using 3D Array . . . . .	255
<i>C. Nelson Kennedy Babu, M. Rajendiran, B. Syed Ibrahim, and R. Pratheesh</i>	

A Novel Invisible Watermarking Based on Cascaded PVD Integrated LSB Technique .....	262
<i>J.K. Mandal and Debashis Das</i>	

Fault Tolerant High Performance Galois Field Arithmetic Processor ....	269
<i>Vinu K. Narayanan, Rishad A. Shafik, Jimson Mathew, and Dhiraj K. Pradhan</i>	

## Mathematical Modeling and Scientific Computing

Numerical Study on Separation of Analytes through Isotachophoresis ...	282
<i>S. Bhattacharyya and Partha P. Gopmandal</i>	

Finite Dimensional Realization of a Guass-Newton Method for Ill-Posed Hammerstein Type Operator Equations .....	293
<i>Monnanda Erappa Shobha and Santhosh George</i>	

Projection Scheme for Newton-Type Iterative Method for Lavrentiev Regularization .....	302
<i>Suresan Pareth and Santhosh George</i>	

Modelling the Wind Speed Oscillation Dynamics .....	311
<i>K. Asokan and K. Satheesh Kumar</i>	

Some Modelling Aspects of Aggregation Kernels and the Aggregation Population Balance Equations .....	319
<i>Nageswara Rao Narni, Gerald Warnecke, Jitendra Kumar, Mirko Peglow, and Stefan Heinrich</i>	

Mixed Covering Arrays on Hypergraphs.....	327
<i>Yasmeen and Soumen Maity</i>	

Kalman Filter and Financial Time Series Analysis.....	339
<i>M.P. Rajan and Jimson Mathew</i>	

Fuzzy Properties on Finite Type of Kac-Moody Algebras .....	352
<i>A. Uma Maheswari and V. Gayathri</i>	

## Pervasive Computing and Applications

Enabling Location Privacy in Pervasive Computing by Fragmenting Location Information of Users .....	364
<i>Jeeva Susan Jacob and Preetha K.G.</i>	

<i>R</i> -norm Intuitionistic Fuzzy Information Measures and Its Computational Applications .....	372
<i>Rakesh Kumar Bajaj, Tanuj Kumar, and Nitin Gupta</i>	

Soft Computing Techniques for Distillation Column Composition Control .....	381
<i>Subhadeep Bhattacharjee and Bhaswati Medhi</i>	
Efficient Segmentation of Characters in Printed Bengali Texts .....	389
<i>Ayan Chaudhury and Ujjwal Bhattacharya</i>	
A GIS Based Approach of Clustering for New Facility Areas in a Digitized Map .....	398
<i>J.K. Mandal, Anirban Chakraborty, and Arun Kumar Chakrabarti</i>	
Enhanced Rule Accuracy Algorithm for Validating Software Metrics ....	406
<i>Abdul Jabbar and Sarala Subramani</i>	
Ontology Based Retrieval for Medical Images Using Low Level Feature Extraction .....	413
<i>Priyamvada Singh, Rohit Rathore, Rashmi Chauhan, Rayan Goudar, and Sreenivasa Rao</i>	
Ontology Based Automatic Query Expansion for Semantic Information Retrieval in Sports Domain .....	422
<i>Rashmi Chauhan, Rayan Goudar, Rohit Rathore, Priyamvada Singh, and Sreenivasa Rao</i>	
Privacy Preserving Technique in Data Mining by Using Chinese Remainder Theorem .....	434
<i>P. Rajesh, G. Narasimha, and Ch. Rupa</i>	
<b>Author Index .....</b>	443

# Energy-Aware Mobile Application Development by Optimizing GCC for the ARM Architecture

Mahalingam P.R. and Shimmi Asokan

Department of Computer Science,  
Rajagiri School of Engineering & Technology, Rajagiri Valley, Cochin, India  
`{prmahalingam, shimmideepak}@gmail.com`

**Abstract.** Nowadays, mobile domain is growing much faster than the desktop domain. This is since people are obsessed with the concept of “portable devices”, which is catered to by handheld devices. Even if small in size, portable devices are responsible for a considerable share of power consumption, primarily due to their abundance. So, ample attention has to be provided in optimizing the applications in this field also. Some of the power consumption is reduced by the ARM core, which is well-known for its power-efficient working. If the applications running on the mobile can also be optimized, the end result will be a considerably efficient and low-power mobile device. We tweak the existing optimizations in such a way that they provide the best possible performance. To increase the level of optimization, we perform optimization reordering, instruction selection, and so on. The end result is projected to give around 32% improvement, which translates to a considerable change in power consumption (up to 35,000 MW per year), and ultimately forms a big step forward in green computing. We take the instance of GCC, which is one of the major contributors to application development.

**Keywords:** ARM core, GNU Compiler Collection, RISC architectures, Machine Idioms, Instruction selection, Optimization, Architecture dependency, Green applications.

## 1 Introduction

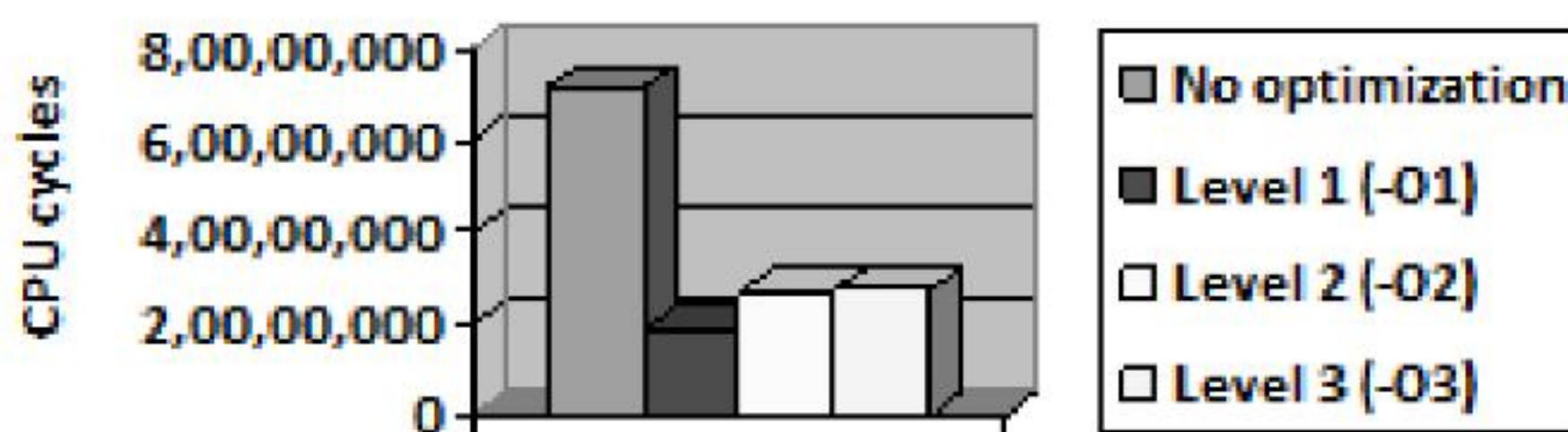
Mobile domain is one of the most booming fields in technology. When we depend heavily on mobiles for our daily processes, their performance also matters a lot. To satisfy this need, the programs that create the applications have to be tuned for performance. Almost all mobile devices (phones, PDAs, etc.) that arrive in the market rely on the processing power provided by the ARM core[7]. ARM is a RISC-based processor core that is famous for its low power usage. So, any performance tuning should be adapted to the ARM core so that they can be used directly on the applications.

**Importance of Optimization:** Optimization[8] in compilers[9] refers to improving the efficiency of the code such that the semantics remains unchanged. This phase performs processes like unwanted code elimination, redundancy removal, code reordering, etc. We can also perform pipeline-dependent operations that will be of advantage in the ARM point of view.

Even in a non-pipelined system, the optimizer can bring about a lot of improvement. Consider a program to sort an array of 100,000 elements using selection sort. The GNU Compiler Collection provides 3 levels of optimization, in addition to an unoptimized level. The number of cycles taken up by the program will be as below.

**Table 1.** Comparison of optimization levels

Level	Number of CPU Cycles
No optimization	71,280,000
Level 1 (-O1)	18,910,000
Level 2 (-O2)	26,410,000
Level 3 (-O3)	27,160,000



**Fig. 1.** Performance of different optimization levels

## 2 GNU Compiler Collection

GNU Compiler Collection (GCC) consists of a group of compiler packages, and is designed to be a generic, flexible compilation unit. Originally called *GNU C Compiler*, it was later expanded to accommodate other languages. Right now, 17 language front-ends are supported by GCC. Also, it has the back-ends for 63 architectures, divided into 3 categories: Standard release (20 architectures), Additional release (23 architectures), FSF releases (20 architectures)

**General Features:** GCC is a complete language processing system[12] made up of 4 components: Preprocessor (cpp), Compiler (cc), Assembler (as), Linker & Loader (ld).

It uses a variety of intermediate formats during the translation from the high-level source program to the assembly code. They are GENERIC, GIMPLE and RTL[11][18]. When we improve the performance at the architecture level, we have to work on RTL, which is attached to the code generation phase. GCC performs a variety of optimizations[3] on the intermediate code.

It is also a portable compiler package[3], allows cross-compilation and is modular. It is distributed as a free software under GNU GPL. The presence of a multitude of front-end and back-ends has made it nearly impossible to make GCC specific for a particular architecture[14]. The only option is to selectively invoke certain optimizations. But if that is stressed upon too much, it might indirectly cause issues to

other architectures. All this has led GCC to be built as a “generic” package. So, there is a lot of scope for improving GCC from the ARM point of view.

### 3 RISC Architectures and ARM Core

ARM stands for Advanced RISC Machine. It is currently used in a variety of embedded system applications like mobile phones, PDAs, handheld organizers, etc. ARM is not a single core, but a whole family of designs sharing similar design principles and a common instruction set. ARM is not a 100% RISC architecture[4], due to the limitations posed by the embedded systems[7] themselves.

RISC Features: ARM core uses RISC architecture[7]. RISC is a design philosophy aimed at delivering simple, but powerful instructions that execute within a single cycle. The complexity of instructions is reduced. The main RISC design rules are given as: Instructions, Pipelines, Registers and Load-store architecture.

Application Domains of ARM Core: ARM cores were primarily aimed at the mobile domain. Nowadays, every handheld device (including smartphone breeds) is powered by an ARM-based processor. The attractive feature that pulls mobile devices to use this core is the power-efficient operation. ARM consumes very little power compared to the desktop processors. This core is now being tested on server systems, for which, a more robust core has been developed. Once that is completely successful, any ARM-based enhancement will have far-reaching applications.

### 4 Machine-Dependent Operations in GCC

GCC supports some machine-dependent operations, mainly in the code generation phase (and in the code optimization phase, as selective optimizations).

Code Support for Architectures: The modularity of GCC ensures that all the architecture-level operations are clearly laid out as individual modules, allowing addition of new architectures, and modification of existing ones. They are put in the configuration folders of each architecture, and they have their own set of *Machine Descriptions*[16] that describe the appropriate RTL processes[11][17] required. The RTL supports two operations[13]: Direct translation[13] and Conversion[13]. The RTL conversion adds more architecture-specific code generation.

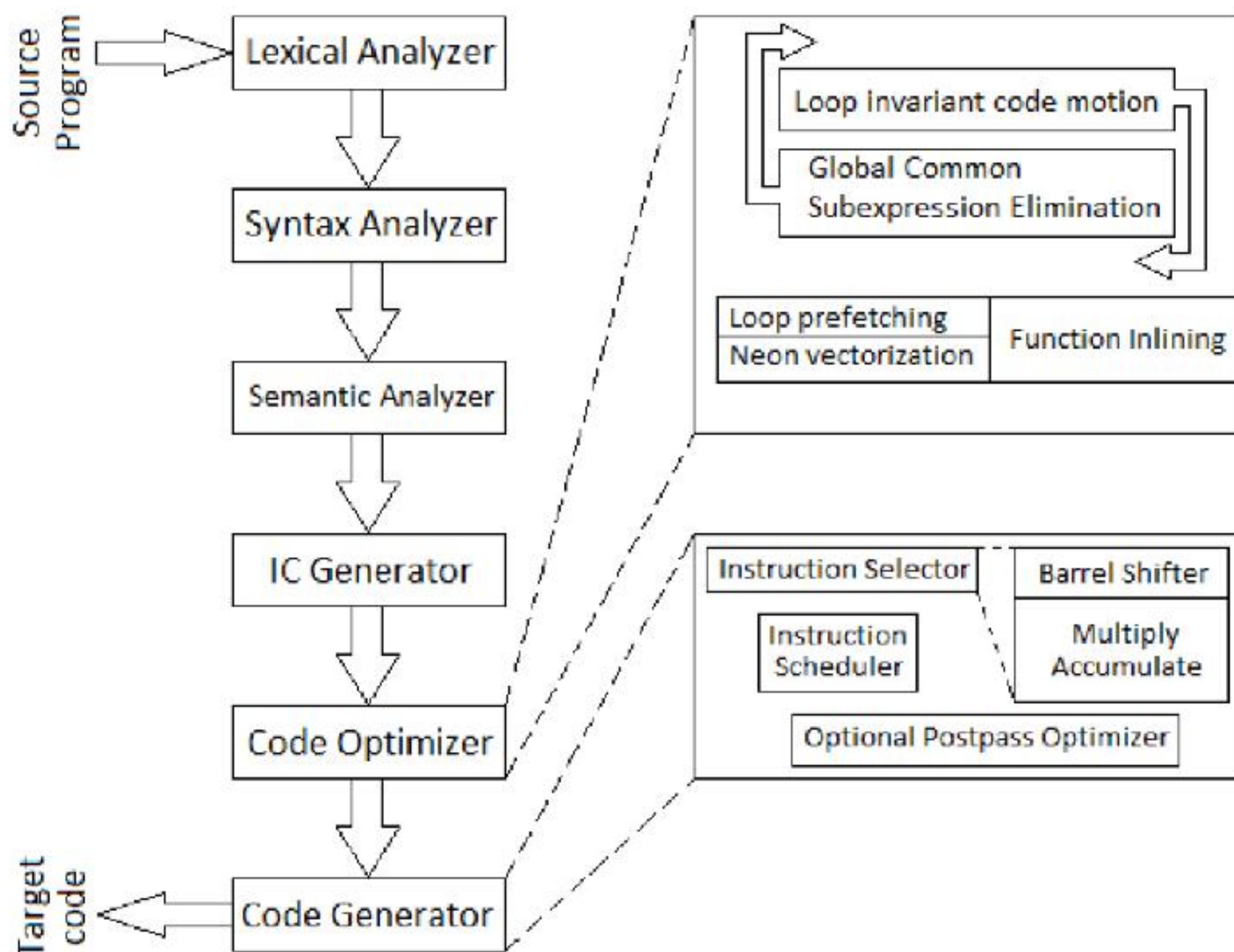
Adding Specific Operations: To modify the architecture-level features, we can work at different levels. Initially, we can modify the command line options for the architecture. These options are used while building GCC from the source, to add or remove features from the final compiler. Another option is to modify the machine descriptions[13], which are defined in the file `arm.md`. The machine descriptions govern the code generation module by outputting assembly segments specific to the architecture. If any code template can improve the performance over some other, they can be explicitly defined in the RTL conversion options, as an expand option. In that case, the operation will be automatically cast to the required template, and we can perform any optional further processing on them.

## 5 Proposed Methodology

The proposed methodology enhances the existing performance by adding pipeline-friendly instruction templates, and removing non-performing features. We have to first analyze the performance of the existing optimization functions and determine whether they can improve the code in any way. Since the GCC structure is generic, an optimizer module might be placed, keeping a specific architecture in view. But the same operation might worsen the performance in a different architecture. We can also add new optimizations in the machine level, as *postpass optimizer*[2]. Here, we stress on some basic modifications that can be done.

Reordering of Optimizations: Many optimizations remove unwanted code from the program. But at the same time, they might render some additional code useless. To remove that, we have to repeat some optimizations later in the process, and remove the code rendered useless by other optimizers. The same is done in GCC by using multiple passes for an optimization[1].

The default ordering of optimizations and their configuration is suited for most architecture. But in the case of ARM, some changes can be made in the optimizers, both in order and configuration.



**Fig. 2.** Scope for modifications to the existing framework

Some of the configurational are:

- Swap the usages of loop-invariant code motion and global common subexpression elimination[1][8]
- Configure loop prefetching[1] to avoid excessive cache misses, and at the same time, avoid unnecessary re-fetching during branch statements.
- Selectively invoke neon vectoriation[1] so that any underperforming scenario is avoided.

**Machine Idioms:** They refer to the machine-specific operations[2] that can replace the conventional instruction templates and bring an improvement in performance. They are commonly combined with *instruction combining*[8] so that a complete template is replaced. It has been observed that some idioms can replace entire loops.

Here, we consider two main idioms that can improve the performance to a good degree – Barrel Shifter and Multiply Accumulate.

**Barrel Shifter:** It performs the *shift* operation[10] in ARM. By default, barrel shifter shifts the bits to the left or right, adding zeroes as necessary. This operation can benefit in some cases. Multiplications can be done indirectly by the barrel shifter. Consider the example:

$$5 \times 6 = 30$$

In binary,  $101 \times 110 = 11110$

We can perform the process indirectly as:  $5 \times (2+4) = 30$

It can now be distributed to separate operations in the following way.

$$5 \times 2 + 5 \times 4 = 30$$

Now, we can split the multiplication in such a way that it is the sum of multiplications, with powers of 2. ie, we now split the operation as:

$5 \times 2^1 = t1$	(shift one bit left)
$5 \times 2^2 = t2$	(shift two bits left)
$t1 + t2 = 30$	(conventional addition)

So, the composite multiplication is now converted to a set of two shifts, followed by an addition. This will be beneficial in cases of small decompositions. But if it is a large number, the summations will outweigh the improvement provided by the shifter.

**Multiply Accumulate:** Multiply accumulate[7] is an option that can eliminate a lot of memory transfers that occur during RISC operations[10], by maintaining intermediate results in the accumulator. This is an option that makes extensive advantage out of pipelining, by maintaining the results, and directly executing subsequent instructions. This is a heavily used process in RISC architectures, especially in fields like Image Processing. They use special architecture that implements integer multiplication with early termination.

**Instruction Selection and Ordering:** Even if we use idioms, there are still other instructions that can be manipulated for efficiency. The pipelined architecture enables the instructions to be ordered in such a way that the dependencies are minimized. Also, proper scheduling ensures that loops and sequences are selected and executed efficiently.

## 6 Challenges in Implementation

Even if the methodology seems straightforward, there are a lot of issues that cause difficulties while implementing. Some of them are as follows.

- Size of code<sup>1</sup> is one of the main factors that affect the implementation.
- ARM-specific optimization is a less explored domain[15]. Many efforts have been limited to simply tuning the performance of the compiler and optimizers, but not much effort had been introduced in adding features.
- Performance estimate of existing optimizations has to be analyzed in depth to decide what all to remove. An example is in the case of vectoriation, where we have to identify the cases in which the optimization should be enabled.
- ARM provides no support for threads[6]. It uses a method called Simultaneous MultiThreading that uses rapid switching. So, even separate, and independently executable functions should be scheduled sequentially.

## 7 Evaluation

Considering machine idioms, each idiom takes a different number of cycles to execute compared to the original. On average, if we consider the possible templates which get replaced, we can see the improvements as follows.

**Table 2.** Improvement by machine idioms

Instruction	Improvement
Barrel shifter	30%
Multiply accumulate	25%
Both	32%

When we consider the reordering of optimizations, we have varying improvements, since they depend on the entire program to adjust the code. The same applies for instruction selection and reordering, since the performance depends on the dependencies imposed by all the instructions.

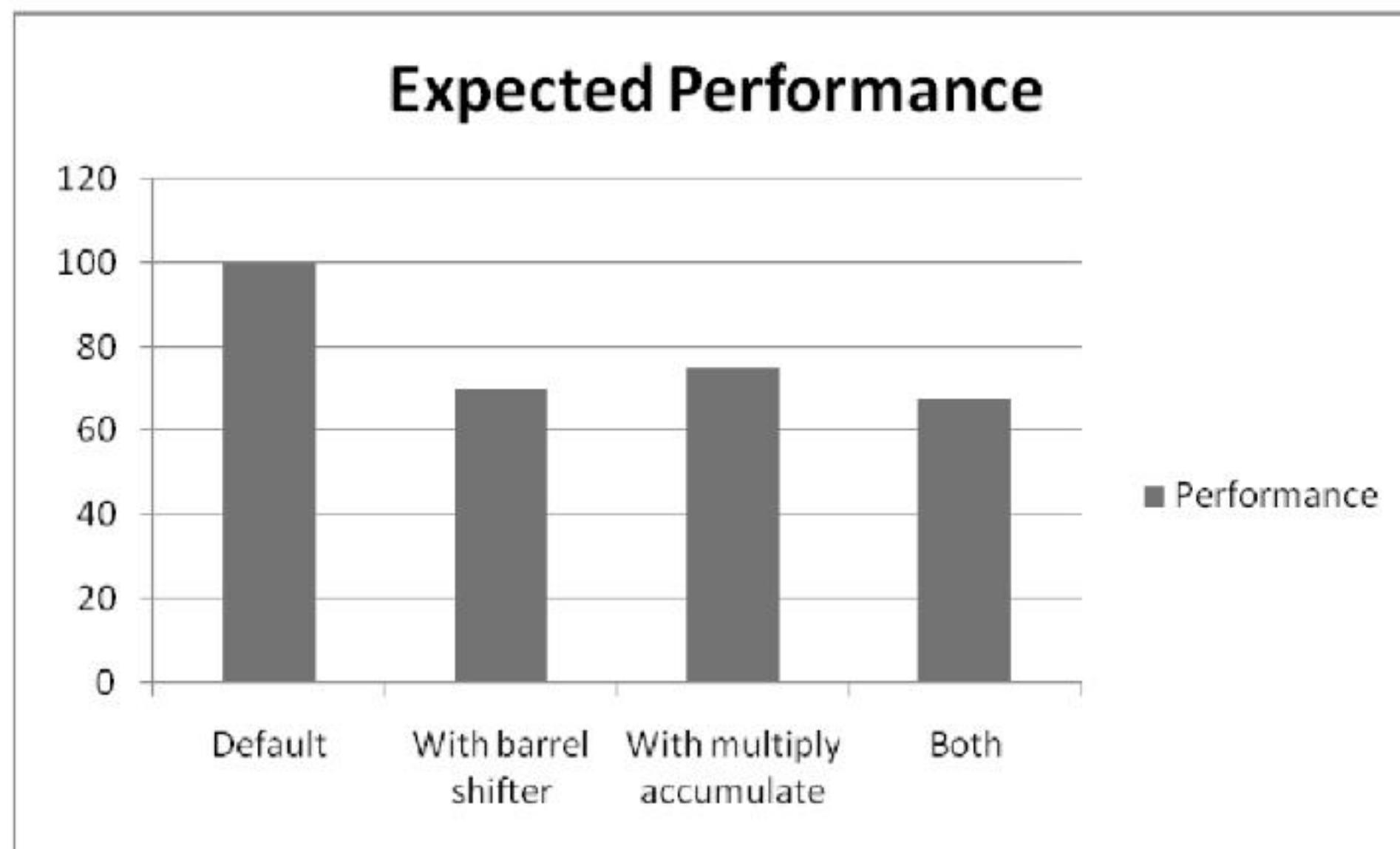
But when we consider the performance as a whole, considering typical embedded system programs<sup>2</sup>, we can expect a performance improvement of around 20%-30%.

Consider a program running in ARM that takes 1,000,000 cycles to execute. This scenario is normally encountered during the execution of simple applications. An improvement of 32% will translate to savings of 320,000 cycles. If we consider an average clock rate of 300 MHz, the difference in 320,000 cycles is shown as 0.1% improvement in the execution time. So, if we take a complex application, or even the case of mobile operating systems, the performance improvement can be safely scaled up to around 10%.

---

<sup>1</sup> GCC is more than 70,000 files in size, and reaches over 500 MB in size. There are nearly 2 million lines of code to be analyzed.

<sup>2</sup> We consider cases like image rendering and manipulation, which involves a lot of complex multiplications and other mathematical operations.



**Fig. 3.** Expected performance of proposed optimizations (on a scale of 1-100)

If we estimate the power consumption at 0.1milliwatts per MHz, a difference of 10% will translate to 0.01 milliwatts (or 10 microwatts) saved per second. An improvement of 10 microwatts per second may sound very small, but over a day, this will translate to 864,000 microwatts, which is equivalent to 0.864 watts (or can be approximated to 0.1 watts). Now, with nearly 5 billion mobile devices in the world, this improvement translates to atleast 5 million watts, or 5 MW.

So, even the smallest improvement has translated to 5 MW of reduced consumption per day. Once Calxeda project, which uses ARM cores in its servers, takes off, the same improvement will get multiplied by a factor of nearly 20, which is nearly 100 MW. So, per year, we save up to 36,500 MW.

## 8 Conclusion

With the advent of the mobile domain, more stress has been placed on application development for mobile users. But the stress on application optimization hasn't increased to that degree. When we consider the ARM core, which is at the heart of mobile devices, and try to optimize the applications, we are getting a considerable improvement (more than 35,000 MW per year).

This shows the power of optimization, which has an impact even in the mobile domain. Taking the case of GCC, some optimizations were proposed, and taking typical examples, the improvement is estimated at 32%. If we consider other packages, it might get better. But even if we don't achieve this large an improvement, we would have a minimum of 5% improvement, translating to around 6000 MW per year.

## 9 Future Work

The current work has been done on the mobile domain. But the same optimization can apply to desktop computing itself. It will further improve by nearly 50%, and in the end, the savings will be quite considerable, which is a great step in green computing. If we can add some level of improvement in hardware, we can exploit all possible opportunities in green computing at the application level.

## References

1. Melnik, D., Belevantsev, A., Plotnikov, D., Lee, S.: A case study: optimizing GCC on ARM for performance of libevas rasterization library. In: Proceedings of GROW 2010 (2010)
2. Wang, L., Lu, B., Zhang, L.: The Study and Implementation of Architecture-dependent Optimization in GCC. IEEE (2010)
3. Stallman, R.M.: Using and Porting the GNU Compiler Collection. GNU Press (2001)
4. Sloss, A.N., Symes, D., Wright, C.: ARM System Developer's Guide—Designing and Optimizing System Software, pp. 1–5. Morgan Kaufmann Publishers (2006)
5. Stallman, R.M.: GCC Developer Community, Using the GNU Compiler Collection for GCC version 4.4.2. GNU Press (2008)
6. Dong, L., Ji, Z., Suixufeng, Hu, M., Cui, G.: A SMT-ARM Simulator and Performance Evaluation. In: Proceedings of the 5th WSEAS Int. Conf. on Software Engineering, Parallel and Distributed Systems, pp. 208–210 (2006)
7. Furber, S.: ARM System-on-Chip Architecture, pp. 47–52. Pearson Education (2007)
8. Muchnik, S.S.: Advanced Compiler Design and Implementation, pp. 319–704. Morgan Kaufmann Publishers
9. Aho, A.V., Lam, M.S., Sethi, R., Ullman, J.D.: Compilers—Principles, Techniques and Tools, pp. 769–902. Pearson Education (2008)
10. ARM DDI 0100 E, ARM Architecture Reference Manual, ARM Limited
11. Novillo, D.: GCC Internals—Internal Representations. In: GCC IR-2 (2007)
12. Gough, G.: An Introduction to GCC for the GNU compilers gcc and g++. Network Theory Limited (2004)
13. Novillo, D.: GCC Internals—Code Generation. In: GCC IR-2 (2007)
14. Wirth, N.: Compiler Construction. Addison-Wesley (2005)
15. Den, W.: ARM7TDMI Optimization Based on GCC, pp. 639–642. IEEE (2010)
16. Khedker, U.: GCC Translation Sequence and Gimple IR. GCC Resource Center, Department of Computer Science and Engineering. Indian Institute of Technology, Bombay (2010)
17. Stallman, R.: GCC Internals—GCC 4.7.0 pre-release. GNU Press (2010)
18. Merrill, J.: GENERIC and GIMPLE: A New Tree Representation for Entire Functions. GCC Developers Summit (2007)

# Compiler Efficient and Power Aware Instruction Level Parallelism for Multicore Architecture

D.C. Kiran, S. Gurunarayanan, Faizan Khaliq, and Abhijeet Nawal

Department of Computer Science and Information Systems,  
Birla Institute of Technology and Science-Pilani,  
Pilani, 333031, Rajasthan, India

{dck, sguru, h2010137, h2010198}@bits-pilani.ac.in

**Abstract.** The paradigm shift to multicore processors for better performance has added a new dimension for research in compiler driven instruction level parallelism. The work in this paper proposes an algorithm to group dependent instructions of a basic block of control flow graph into disjoint sub-blocks during the SSA form translation. Following this an algorithm is presented which constructs a graph tracking dependencies among the sub-blocks spread all over the program. A global scheduler of the compiler is presented which selectively maps sub-blocks in the dependency graph on to multiple cores, taking care of the dependencies among them. The proposed approach conforms to spatial locality, aims for minimized cache coherence problems, communication latency among the cores and overhead of hardware level instruction re-ordering while extracting parallelism and saving power. The results observed are indicative of better and balanced speedup per watt consumed.

**Keywords:** Control Flow Graph (CFG), Static Single Assignment (SSA), Data Dependency, Multicore Processors, Instruction Level Parallelism, Global Scheduler, Local Scheduler, Energy Efficiency, Performance per watt, Sub-block Dependency Graph (SDG).

## 1 Introduction

Increasing demand for speed up in processors has resulted in many revolutions over the past years. Multicore processors are one of them in which a single chip has two or more independent cores which read and execute program instructions. Finding an effective way to exploit the parallelism or concurrency inherent in an application is one of the most daunting challenges in multicore environment. This parallelism can be achieved in two ways, first is scheduling different tasks on different cores. Second is scheduling portions of same tasks on different cores, Intra process parallelism or Instruction level parallelism. In first approach the scheduler of the operating system picks up a task and schedules it on the free core. In second approach compiler has to analyze the program for the possibilities of parallelism and suitable scheduler should

map the parallel constructs on to multiple cores. By analyzing the dependencies between instructions, the compiler can identify the independent instructions that can run in parallel. There are three types of dependencies to look for [1], Write after Write dependency (WAW), Write after Read dependency (WAR), and Read after Write dependency (RAW). Converting program to static single assignment (SSA) form will remove WAW and WAR dependencies and hence compiler has just to look for RAW dependencies. SSA form is an intermediate representation of a program in which each variable is defined only once [2].

ILP can be achieved by existing scheduling techniques, where one instruction at a time is scheduled on to multiple execution units [3][4]. To perform this, critical path of instructions is created by analyzing the dependencies. The instruction with longest critical path was scheduled first to enable other instruction to get scheduled. This approach was well suited for parallel architectures which were available before multicore era. But this technique cannot be applied on multi-core environments because two dependent instructions may get scheduled on different cores (may not be in the same time) resulting in increased communication latency.

A technique was proposed to overcome these limitations [5], in which a set of dependent instructions within a basic block which are in SSA form were grouped. This set is disjoint and is referred as sub-block. The intra block scheduler is used to schedule these sub-blocks on to multiple cores.

The creation of sub-blocks can be done at two levels. In the first approach [5] a SSA form program is taken as input. These SSA form instructions are then analyzed for dependencies in a separate pass so as to form the sub-blocks. In the second approach [6], dependency analysis and sub-block creation is done along with variable renaming step in the generation of SSA form program. This avoids the need for an extra pass done in the first approach. The proposed work is an extension of the second approach. In this work a technique is proposed which considers extracting parallelism among the sub-blocks created across the program referred thereafter as inter-block parallelism. This technique facilitates global scheduling. This technique also conforms to the principle of spatial locality as the closely related or dependent instructions are grouped together in sub-blocks. This also minimizes the cache coherence problems as the instruction stream of a sub-block scheduled to a core is not dependent on what is scheduled on the other cores at a time. This in turn reduces the communication latency among the cores. The task of instruction stream reordering in the processor hardware consumes power. Since as per this technique the dependency analysis in the instruction stream is done in the compilation phase itself, the overhead of hardware level reordering is reduced. This makes the technique power aware. The scheduler being presented takes the granularity of instruction stream to be presented to a core as sub-block and so it is possible to selectively utilize the cores. This makes it more energy efficient.

The rest of the paper is organized as follows. Section 2 gives a brief overview of the architecture and compiler used in the work. Section 3 gives details of creating

sub-block dependency graph (SDG). Section 4 gives the detail of the inter block scheduling technique. Analysis and discussion of results are given in section 5. Finally, the paper concludes with Section 6.

## 2 Realm

The framework for the proposed work has two parts, the target architecture and the compiler. The target architecture will expose the low level details of hardware to compiler. They implement minimal set of mechanisms in the hardware and these mechanisms are fully exposed to software, where software includes both runtime system and compiler. Here runtime system manages mechanisms historically managed by hardware, and compiler has responsibility of managing issues like resource allocation, extracting parallel constructs for different cores, configurable logic, and scheduling. These types of architectures can be seen in some network processors and RAW architecture [7][8].

The multicore environment has multiple interconnected tiles and on each tile there can be one RISC like processor or core. Each core has instruction memory, data memory, PC, functional units, register files, and source clock. FIFO is used for communication. Here the register files are distributed, eliminating the small register name space problem, thus allows exploiting ILP at greater level.

The proposed work uses Jackcc Compiler [9]. This is an open source compiler developed at university of Virginia. The basic block in CFG of Jackcc is called *Arena*, and instruction inside the block is called *Quad*. The DAG generated by front end of the compiler is converted into *quad* intermediate representation, and then these quads are used to construct the basic blocks of CFG. Instructions are in SSA form. The process of converting a Non-SSA form program to SSA form program has two steps.

Step 1: Placing Phi ( $\Phi$ ) statements by computing iterated dominance frontier.

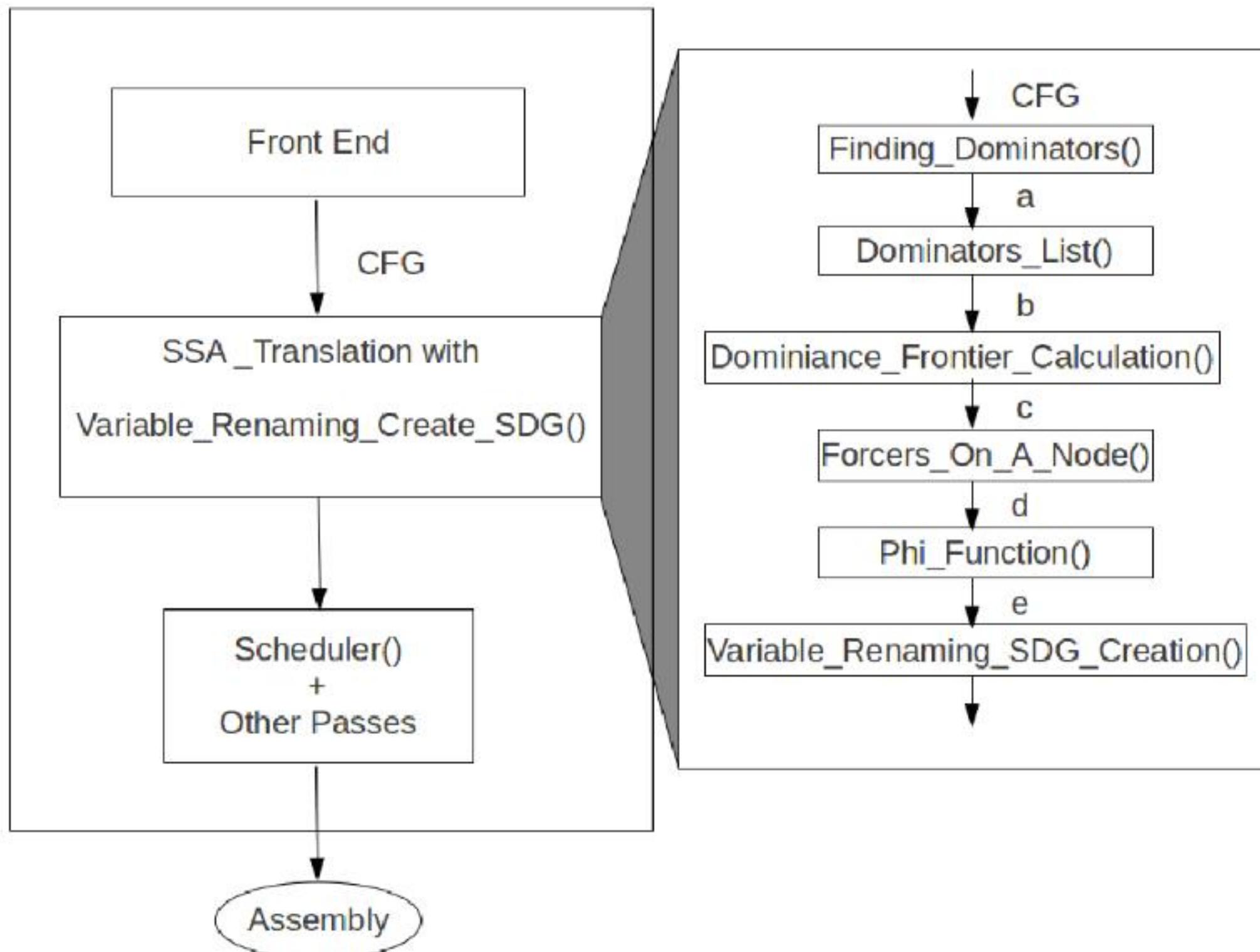
Step2: Renaming variables in original program and Phi ( $\Phi$ ) functions, using dominator tree and rename stack to keep track of the current names.

## 3 Inter Block Parallelism

The proposed work is an extension of intra block technique where sub-blocks within the basic blocks of CFG were considered for scheduling [5]. Extracting inter block parallelism will facilitate global scheduling. In this approach the sub-blocks across the program are considered for scheduling. The sub-blocks are disjoint within a basic block of CFG, but the sub-blocks across the basic blocks need not be disjoint. The non-disjoint sub-blocks should be executed one after the other.

Inter block parallelism is a process of finding the non-disjoint sub-blocks across the basic blocks. The process of extracting inter block parallelism involves two steps, one creating sub-block and second creating sub-block dependency graph.

The technique discussed here to create sub-block and sub-block dependency graph is compiler efficient, because it is done during SSA translation itself as shown in Figure1.



**Fig. 1.** Modified flow or Jackcc to create disjoint sub-blocks and SDG

Disjoint sub-blocks were created by modifying variable renaming step of SSA translation function [6]. There are two tasks which need to be done simultaneously during translation. First is variable renaming and second is creating disjoint sub-blocks.

Its first role is accomplished by traversing each node of the CFG which has now Phi ( $\Phi$ ) functions inserted and rename every variable in such a way that each use corresponds to exactly one definition. Each definition is renamed with a new version of that variable. Second job is accomplished by updating the use of the renamed variable, there by anti dependency (RAW) of the current statement is gathered to forms the disjoint sub-blocks.

### 3.1 Sub Block Dependency Graph (SDG)

This section explains the process of creating of a sub block dependency graph along with variable renaming and creating disjoint sub-blocks during SSA translation. The dependencies among the sub blocks from different basic blocks will be analyzed by the compiler to form the sub block dependency graph.

The SDG is graph  $G(V, E)$ , where vertex  $v_i \in V$  is sub-block  $B_p SB_i$  of basic block  $B_p$  and the edge  $e \in E$ , is drawn between vertex  $SB_i \in B_p$  and  $SB_j \in B_q$  where  $p \neq q$ , and instruction in the sub-block  $SB_j$  is dependent on one or more instructions in  $SB_i$ .

SDG is represented as dependency matrix. In dependency matrix all sub-blocks are arranged in first column. If the sub-block  $B_p SB_i$  is dependent on sub-block  $B_q SB_j$ , then  $B_q SB_j$  is added in the dependency list of  $B_p SB_i$ , meaning  $B_p SB_i$  should be scheduled only after  $B_q SB_j$  completes its execution. The sub-block  $B_p SB_i$  can be scheduled only if the list is empty otherwise it should wait till the list becomes empty.

### 3.2 Algorithm for Sub Block Dependency Graph Creation

Algorithm for creation of Sub block Dependency Graph is given below

```

Scan the current statement
if(variables on right hand side==0)
    if statement has phi function
        for each predecessor of this block do
            find_sub_block_and_block
            add_sub_block_to_dependency_list
        endfor
    endif
endif
else if(number of variables on right hand side==1)
    find where this variable is defined
    if(variable is not defined in the current block)
        find_sub_block_and_block
        add_sub_block_to_dependency_list
    endif
endelseif
else if(number of variables on right hand side==2)
    find where these variables are defined
    if(one variable is not defined in current block)
        find_sub_block_and_block
        add_sub_block_to_dependency_list
    endif
    else if(no variable is defined here)
        find_sub_block_and_block_for_both_variables
        add_sub_blocks_to_dependency_list
    endelseif
endelseif

```

Here each statement is scanned for inter block dependencies. If statement has got phi function as it's R value then there would be inter dependencies coming from the predecessors of given basic block as per definition of phi function. While observing every predecessor, dependency edges are created between the sub blocks and those sub blocks are added to the dependency matrix. Second case could be presence of one variable in R value of statement such that this variable is not defined in current basic block. Hence inter block dependency exist and the graph is traversed upwards covering its predecessor to look for the dependency. Hence one edge would be added and the sub block is added to the dependency matrix. Similar action would be taken for the case when R value consists of two variables, both of which are defined in predecessors of the given basic block.

### 3.3 Complexity Analysis

Let number of nodes in CFG=N

Let average number of statements per block=S

Let total number of variables definitions in program (before conversion to SSA) =D

Let average number of variables defined per block (after conversion to SSA) =d

Let average number of sub blocks formed in a basic block after processing s statements = B

Let average number of statements in each sub block = S'

Let average number of predecessors of a basic block= P

Then complexity of the algorithm turns out to be

$$O(\max(N*S*(\max(D,d,B*S',N))), (N*S*(\max(D,P*\max(N,d)))))) \quad (1)$$

This complexity is of variable renaming plus intra block plus sub block dependency graph creation since all are being done in the same pass. Two conditions contributing to the worst scenario can be observed. First one is when statement doesn't have a phi function and there are two variables in the R value and both of them cause intra block dependency. In that case complexity would be given by  $N*S*\max(D,B*S',N,d)$ . In second condition, there is a phi function in the statement and complexity is given by  $N*S*\max(D,P*\max(N,d))$ . So the final complexity would be maximum of these two values.

If the formation of sub blocks and formation of sub block dependency graph takes place in the separate pass then complexity would be given by

$$O(N*S*\max(D,d))+O(\max(N*S*\max(B*S',N,d)), N*S*(\max(D,P*\max(N,d)))) \quad (2)$$

In equation the Big O notation gives the worst case complexity of variable renaming phase and Big O notation on the right gives the worst case complexity of creating sub block and forming sub block dependency graph. It can be observed that compared to equation 1 at least  $O(N*S)$  time is more in equation 2 and hence complexity in equation 2 is greater than equation 1.

## 4 Scheduler

In the proposed compiler framework, the scheduling phase follows the SSA translation phase. The scheduler takes SDG as input and maps the sub-blocks on to multiple cores. To schedule sub-blocks on multiple cores scheduler needs information like height of each sub-block, number of instructions in each sub-block, schedule time of each core, and ready-time of sub-block. This information is stored in a structure along with respective sub-block. This structure is an element in priority queue.

The information required by Scheduler is calculated as:

- I. Scheduling time of core

$$\text{Schedule time of core I} = \text{current schedule time of core I} + \text{no. of instructions in currently scheduled sub-block.} \quad (3)$$



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



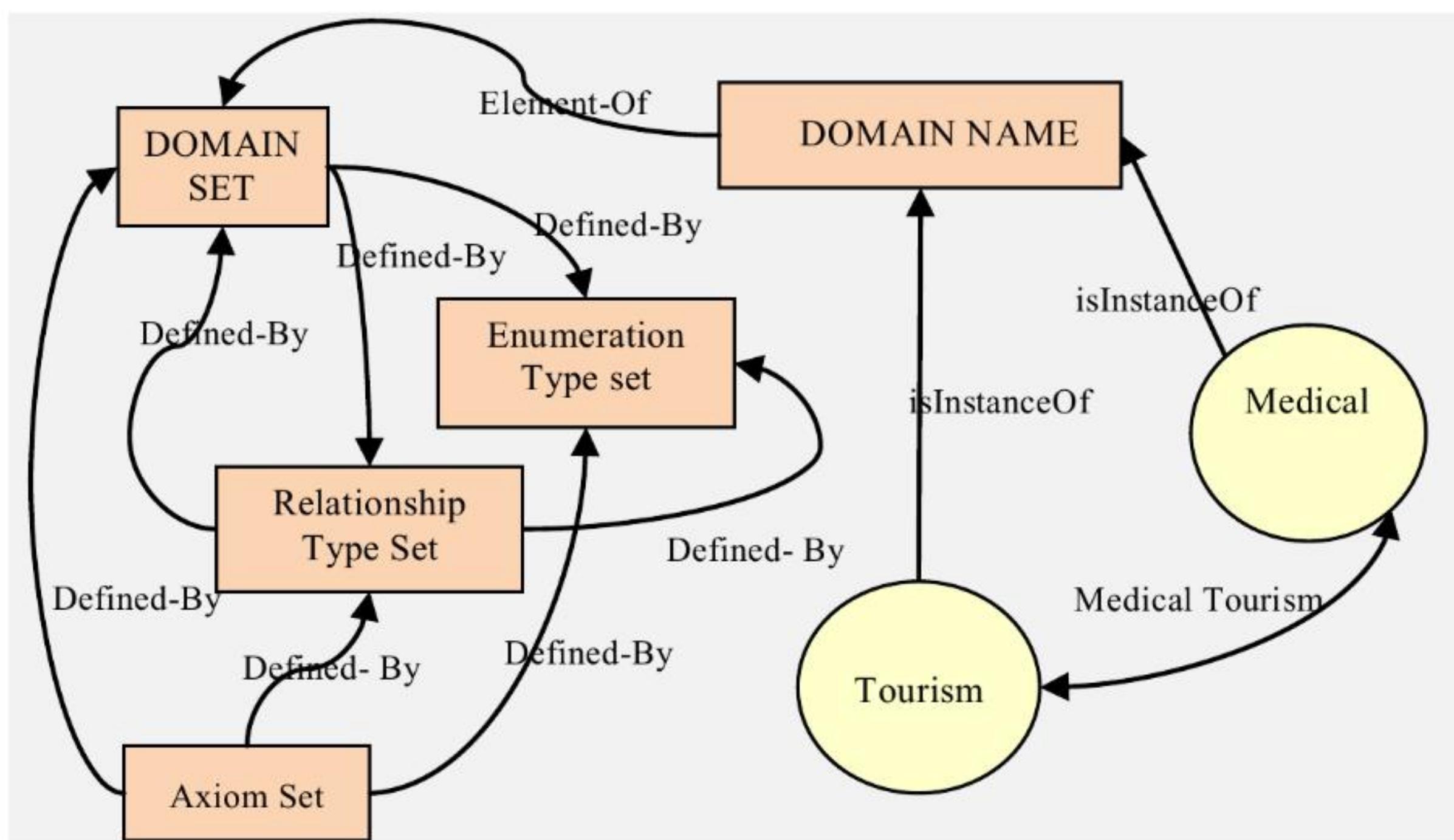
You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.

- The information that exists today on the Web is mostly semi-structured or unstructured in nature. Semantic web is a vision for future, for the time when almost all the available knowledge on the web will have a semantic structure. So any effective, modern day web search architecture should combine both the traditional keyword based search technique with semantic search approach [16]. In order to decide what search to perform on a particular user query, the search engine needs to determine whether enough ontologies are available for the key terms or not. This can be established by the use of OKB.

## 3 Proposed Idea

### 3.1 Need for Creating a Global Ontology or MotherOnt

Ontologies are used to provide semantic structuring or meaning to the web documents in their particular domains so as to offer a number of advantages including enabling the context-based or semantic search for web documents. We realize that there is a need to add semantic markup or annotations to the ontologies of various domains so as to offer the same advantages in searching for existing ontologies on web, as are offered by semantically annotating the documents while performing the document search.



**Fig. 1.** Conceptual Model of Global Ontology “MotherOnt”

Some sorts of standardization efforts are required for interconnecting all the ontologies semantically to produce a global grid environment for enabling the effective Semantic Search. For achieving such an interconnection, a global ontology, we call it MotherOnt in our model, can be created and maintained by a central governing body



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.

# FFMS: Fuzzy Based Fault Management Scheme in Wireless Sensor Networks\*

Prasenjit Chanak, Indrajit Banerjee, Tuhina Samanta, and Hafizur Rahaman

Department of Information Technology  
Bengal Engineering and Science University, Shibpur,  
Howrah, India

prasenjit.chanak@gmail.com,  
{ibanerjee, t\_samanta, rahaman\_h}@it.becs.ac.in

**Abstract.** Fault detection and fault management in wireless sensor network is a major challenge in its performance analysis. In this paper we propose a fuzzy logic based fault detection and fault management scheme (FFMS). Fuzzy rules are proposed for efficient detection of different types of nodes named as normal node, traffic node, end node, and dead node. Fuzzy interface engine categorizes the different nodes according to the chosen membership function and the defuzzifier generates a non-fuzzy control to retrieve the various types of nodes. Next, active nodes' performance analyses are done using five traditional metrics. Experimental results manifest that the proposed FFMS scheme is more effective for fault management in WSN.

**Keywords:** Wireless sensor networks (WSNs), fault detection, fuzzy logic, power efficiency.

## 1 Introduction

Wireless sensor network is a collection of hundreds and thousands of low-cost, low power miniaturized electronic programmable devices, which are deployed in a monitoring area [1], [2]. These devices are capable for data sensing of monitoring environment, data processing and communicating between each other. Low cost and effortlessly deployable nodes makes sensor network an attractive solution for a plethora of applications in various filed, such as military tracking, fire monitoring etc. Low power, low computation capability of the node is the main obstacle in augmentation of sensor networks application [3]. Due to distant deployment of sensor nodes, the probability of fault in sensor network is very high [4]. Consequently, node failure degrades the life time and quality of service of the networks [2]. In addition, many WSN applications requires harsh node deployment, which makes difficult to control and monitor individual nodes manually [5]. Such networks demand automatic fault management technique in WSN.

---

\* This work is partially supported by the grant from the Council of Scientific and Industrial Research (CSIR), human resource development group (Extramural research division), Govt. of India.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.

## 5 Conclusion and Future Work

In this paper, authors explored the utility of PSoC to build a sensor network. PSoC, with its programmable analog, digital and microcontroller blocks, coupled with CYFi RF module, can function as a sensor node. Integration of all signals processing functionality in a single chip results in a small footprint for the node several of which have been combined to set up a sensor network. Well known WSN protocols such as LEACH and SPIN have been tested on the network and found to be functioning correctly. A model is created in NS-2 simulator to scale the network for larger nodes. More experiments are under way to scale up the network as well as test other routing protocols, to quantify the performance of the network in terms of latency, energy consumption and other important parameters.

## References

1. Cypress Semiconductor website, <http://www.cypress.com>
2. Wang, G., Wang, Y., Tao, X.: An Ant colony Clustering Routing Algorithm for Wireless Sensor Networks. In: Third International Conference on Genetic and Evolutionary Computing (2009)
3. Li, L., Wu, H., Chen, P.: Discuss in Round Rotation Policy of Hierarchical Route in Wireless Sensor Networks. Digital Engineering Research Center, China
4. Abd-El-Barr, M.I., Youssef, M.A.M., Al-Otaibi, M.M.: Wireless sensor networks - part I: topology and design issues. In: Canadian Conference on Electrical and Computer Engineering, May 1-4, pp. 1165–1168 (2005)
5. Rehena, Z., Roy, S.: A Modified SPIN for Wireless Sensor Networks. In: International Conference on Communication Systems and Networks, pp. 1–4 (January 2011)
6. SPI-based CyFi™ Transceiver Data Sheet. Cypress (2009)
7. CYRF7936 2.4 GHz CyFi™ Transceiver Data Sheet. Cypress (2008)
8. CY8C27443 Datasheet. Cypress (2007)



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.

given linear discrete-time control system, *i.e.* we derive the reduced-order model for a given discrete-time linear control system keeping only the dominant state of the given discrete-time linear control system. Using the reduced-order model obtained, we characterize the existence of a reduced-order exponential observer that tracks the state of the reduced-order model, *i.e.* the dominant state of the original linear plant. We note that the reduced-order observer design detailed in this paper is a discrete-time analogue of the results of Aldeen and Trinh [8] for the observer design of the dominant state of continuous-time linear control systems.

## 2 Reduced Order Model and Observer for Discrete-Time Linear Systems

In this section, we consider a large scale linear discrete-time control system  $\mathbf{S}_1$  given by

$$\begin{aligned} x(k+1) &= Ax(k) + Bu(k) \\ y(k) &= Cx(k) \end{aligned} \quad (1)$$

where  $x \in R^n$  is the state,  $u \in R^m$  is the control or input and  $y \in R^p$  is the system output. We assume that  $A, B$  and  $C$  are constant matrices with real entries having dimensions  $n \times n$ ,  $n \times m$ ,  $p \times n$  respectively.

First, we suppose that we have made an identification of the *dominant (slow)* and *non-dominant (fast)* states of the original linear system (1) using the modal approach as described in [9].

Without loss of generality, we may assume that  $x = \begin{bmatrix} x_s \\ x_f \end{bmatrix}$ , where  $x_s \in R^r$  represents the *dominant* state and  $x_f \in R^{n-r}$  represents the *non-dominant* state of the system.

Then the linear system (1) becomes

$$\begin{aligned} \begin{bmatrix} x_s(k+1) \\ x_f(k+1) \end{bmatrix} &= \begin{bmatrix} A_{ss} & A_{sf} \\ A_{fs} & A_{ff} \end{bmatrix} \begin{bmatrix} x_s(k) \\ x_f(k) \end{bmatrix} + \begin{bmatrix} B_s \\ B_f \end{bmatrix} u(k) \\ y(k) &= \begin{bmatrix} C_s & C_f \end{bmatrix} \begin{bmatrix} x_s(k) \\ x_f(k) \end{bmatrix} \end{aligned} \quad (2)$$

From (2), we can write the plant equations as

$$\begin{aligned} x_s(k+1) &= A_{ss}x_s(k) + A_{sf}x_f(k) + B_s u(k) \\ x_f(k+1) &= A_{fs}x_s(k) + A_{ff}x_f(k) + B_f u(k) \\ y(k) &= C_s x_s(k) + C_f x_f(k) \end{aligned} \quad (3)$$

Next, we shall assume that the matrix  $A$  has a set of  $n$  linearly independent eigenvectors. In most practical situations, the matrix  $A$  has distinct eigenvalues and this condition is immediately satisfied. Thus, it follows that  $A$  is diagonalizable. Thus, we can find a non-singular (*modal*) matrix  $P$  consisting of  $n$  linearly independent eigenvectors of  $A$  such that  $P^{-1}AP = \Lambda$ , where  $\Lambda$  is a diagonal matrix consisting of the  $n$  eigenvalues of  $A$ .

Now, we introduce a new set of coordinates on the state space given by

$$\xi = P^{-1}x \quad (4)$$

In the new coordinates, the plant (1) becomes

$$\begin{aligned} \begin{bmatrix} \xi_s(k+1) \\ \xi_f(k+1) \end{bmatrix} &= \begin{bmatrix} \Lambda_s & 0 \\ 0 & \Lambda_f \end{bmatrix} \begin{bmatrix} \xi_s(k) \\ \xi_f(k) \end{bmatrix} + P^{-1}Bu(k) \\ y(k) &= CP \begin{bmatrix} \xi_s(k) \\ \xi_f(k) \end{bmatrix} \end{aligned} \quad (5)$$

where  $\Lambda_s$  and  $\Lambda_f$  are  $r \times r$  and  $(n-r) \times (n-r)$  diagonal matrices respectively, consisting of the dominant and non-dominant eigenvalues of  $A$ .

Define matrices  $\Gamma_s, \Gamma_f, \Psi_s$  and  $\Psi_f$  by

$$P^{-1}B = \begin{bmatrix} \Gamma_s \\ \Gamma_f \end{bmatrix} \text{ and } CP = \begin{bmatrix} \Psi_s & \Psi_f \end{bmatrix} \quad (6)$$

where  $\Gamma_s, \Gamma_f, \Psi_s$  and  $\Psi_f$  are  $r \times m$ ,  $(n-r) \times m$ ,  $p \times r$  and  $p \times (n-r)$  matrices respectively.

From (5) and (6), we see that the plant (3) has the following simple form in the new coordinates (4).

$$\begin{aligned} \xi_s(k+1) &= \Lambda_s \xi_s(k) + \Gamma_s u(k) \\ \xi_f(k+1) &= \Lambda_f \xi_f(k) + \Gamma_f u(k) \\ y(k) &= \Psi_s \xi_s(k) + \Psi_f \xi_f(k) \end{aligned} \quad (7)$$

Next, we make the following assumptions:

**(H1)** As  $k \rightarrow \infty$ ,  $\xi_f(k+1) \approx \xi_f(k)$ , i.e.  $\xi_f$  takes a constant value in the steady-state.

**(H2)** The matrix  $I - \Lambda_f$  is invertible.

Then it follows from (7) that for large values of  $k$ , we have

$$\xi_f(k) \approx (I - \Lambda_f)^{-1} \Gamma_f u(k) \quad (8)$$

Substituting (8) into (7), we obtain the reduced-order model as

$$\begin{aligned} \xi_s(k+1) &= \Lambda_s \xi_s(k) + \Gamma_s u(k) \\ y(k) &= \Psi_s \xi_s(k) + \Psi_f (I - \Lambda_f)^{-1} \Gamma_f u(k) \end{aligned} \quad (9)$$

To obtain the reduced-order model of the linear plant (1) in the  $x$  coordinates, we proceed as follows. By the linear change of coordinates (4), it follows that

$$\xi = P^{-1}x = Qx.$$

Thus, we have

$$\begin{bmatrix} \xi_s(k) \\ \xi_f(k) \end{bmatrix} = Q \begin{bmatrix} x_s(k) \\ x_f(k) \end{bmatrix} = \begin{bmatrix} Q_{ss} & Q_{sf} \\ Q_{fs} & Q_{ff} \end{bmatrix} \begin{bmatrix} x_s(k) \\ x_f(k) \end{bmatrix} \quad (10)$$

Using (9) and (10), it follows that

$$Q_{ff} x_f(k) = -Q_{fs} x_s(k) + (I - \Lambda_f)^{-1} \Gamma_f u(k) \quad (11)$$

Next, we assume the following:

**(H3)** The matrix  $Q_{ff}$  is invertible.

Using the assumption (H3), the equation (11) becomes

$$x_f(k) = -Q_{ff}^{-1} Q_{fs} x_s(k) + Q_{ff}^{-1} (I - \Lambda_f)^{-1} \Gamma_f u(k) \quad (12)$$

To simplify the notation, we define the matrices

$$R = -Q_{ff}^{-1} Q_{fs} \text{ and } S = Q_{ff}^{-1} (I - \Lambda_f)^{-1} \Gamma_f \quad (13)$$

Using (13), the equation (12) can be simplified as

$$x_f(k) = Rx_s(k) + Su(k) \quad (14)$$

Substituting (14) into (3), we obtain the reduced-order model  $\mathbf{S}_2$  as

$$\begin{aligned} x_s(k+1) &= A_s^* x_s(k) + B_s^* u(k) \\ y(k) &= C_s^* x_s(k) + D_s^* u(k) \end{aligned} \quad (15)$$

where the matrices  $A_s^*$ ,  $B_s^*$ ,  $C_s^*$  and  $D_s^*$  are defined by

$$A_s^* = A_{ss} + A_{sf} R, \quad B_s^* = B_s + A_{sf} S, \quad C_s^* = C_s + C_f R, \quad D_s^* = C_f S \quad (16)$$

where  $A_s^*$ ,  $B_s^*$ ,  $C_s^*$  and  $D_s^*$  are defined as in (16).



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.

## 5 Conclusions

In this paper, using the dominant state analysis of the given large-scale linear plant, we obtained the reduced-order model of the linear plant. Then we derived sufficient conditions for the design of observer-based reduced-order controllers. The observer-based reduced order controllers are constructed by combining the reduced order controllers for the original linear system which require the dominant state of the original system and reduced order observers for the original linear system which provide an exponential estimate of the dominant state of the original linear system. We also established a separation principle in this paper which shows that the pole placement problem and observer problem are independent of each other.

## References

- [1] Cumming, S.D.: Design of observers of reduced dynamics. *Electronics Letters* 5, 213–214 (1969)
- [2] Fortman, T.E., Williamson, D.: Design of low-order observers for linear feedback control laws. *IEEE Trans. Automat. Control* 17, 301–308 (1972)
- [3] Litz, L., Roth, H.: State decomposition for singular perturbation order reduction – a modal approach. *International J. Control* 34, 937–954 (1981)
- [4] Lastman, G.J., Sinha, N.K., Rozsa, P.: On the selection of states to be retained in a reduced-order model. *IEEE Proceedings – Control Theory* 131, 15–24 (1984)
- [5] Anderson, B.D.O., Liu, Y.: Controller reduction: concepts and approaches. *IEEE Trans. Automat. Control* 34, 802–812 (1989)
- [6] Mustafa, D., Glover, K.: Controller reduction by  $H_\infty$  balanced truncation. *IEEE Trans. Automat. Control* 36, 668–692 (1991)
- [7] Aldeen, M.: Interaction modelling approach to distributed control with application to power systems. *International J. Control* 53, 1035–1044 (1991)
- [8] Aldeen, M., Trinh, H.: Observing a subset of the states of linear systems. *IEE Proceedings – Control Theory* 141, 137–144 (1994)
- [9] Sundarapandian, V.: Distributed control schemes for large-scale interconnected discrete-time linear systems. *Mathematical and Computer Modelling* 41, 313–319 (2005)
- [10] Ogata, K.: *Discrete-Time Control System*. Prentice Hall, New Jersey (2010)

# Adiabatic Technique for Designing Energy Efficient Logic Circuits

Shari Jahan C.S. and N. Kayalvizhi

Department of Electronics and Communication Engineering, Amrita Vishwa Vidyapeetham University, Coimbatore, India  
shari\_jahan@yahoo.co.in, n\_kayalvizhi@cb.amrita.edu

**Abstract.** Energy minimization is an important factor in designing digital circuits which are portable and battery operated. Irreversible logic operation causes the minimum dissipation of  $KT \ln 2$  joules of heat energy when each bit is erased. Reversible logic that employs adiabatic switching principles can be used to minimize dynamic power , which is the major contributor to total power dissipation. Reversible Energy Recovery Logic (RERL) belongs to fully adiabatic logic family and it eliminates non adiabatic energy loss by making use of reversible logic. RERL NAND/AND gate and RERL SR latch is proposed in this work using eight phase clocking scheme. This RERL circuits consume less energy compared with static CMOS logic circuits at low speed operation. The simulation result using HSPICE shows that RERL circuits consume less power compared with the static CMOS circuits.

**Keywords:** Adiabatic circuit, RERL, Reversible logic.

## 1 Introduction

By Moore's law the power dissipation will double for constant cost roughly once every two years. Also in conventional logic operation the flipping of bits cause energy dissipation. This will be accompanied by a decrease in the entropy of the system which results in the dissipation of heat. According to Landauer's research erasing of each bit in an irreversible operation causes heat dissipation of  $KT \ln 2$  joules. This energy dissipation can be reduced by employing reversible logic since it is physically and logically reversible. Physically reversible means there is no heat dissipation and by logical reversibility the inputs can be retrieved from the output. The reversible operation can be performed only with the support of reversible gates. The reversible logic is implemented by adiabatic logic family by using adiabatic switching principle.

Adiabatic logic family includes fully adiabatic logic and quasi static adiabatic logic. Fully adiabatic logic includes Split Level Charge Recovery Logic (SCRL) and Reversible Energy Recovery Logic (RERL). Adiabatic circuits have adiabatic, non-adiabatic and adiabatic losses.

The adiabatic loss is inversely proportional to the transition time  $T$  of the trapezoidal clock [1, 3]. The adiabatic loss in adiabatic circuits is given by

$$E_{\text{ADIABATIC}} = \frac{R_{\text{ON}} C_L}{T} C_L V_{\text{DD}}^2 \quad (1)$$

where  $R_{\text{ON}}$  is the on-resistance of the switch and  $C_L$  is the load capacitance. By making the transition time very much greater than  $R_{\text{ON}}C_L$ , adiabatic loss can be reduced. The non-adiabatic losses are due to the potential difference across the terminals of a switch when the switch is turned on. It does not depend on the frequency. At low frequency the non-adiabatic loss becomes prominent.

$$E_{\text{NON\_ADIABATIC}} = \frac{1}{2} \frac{C_1 C_2}{(C_1 + C_2)} (V_1 - V_2)^2 \quad (2)$$

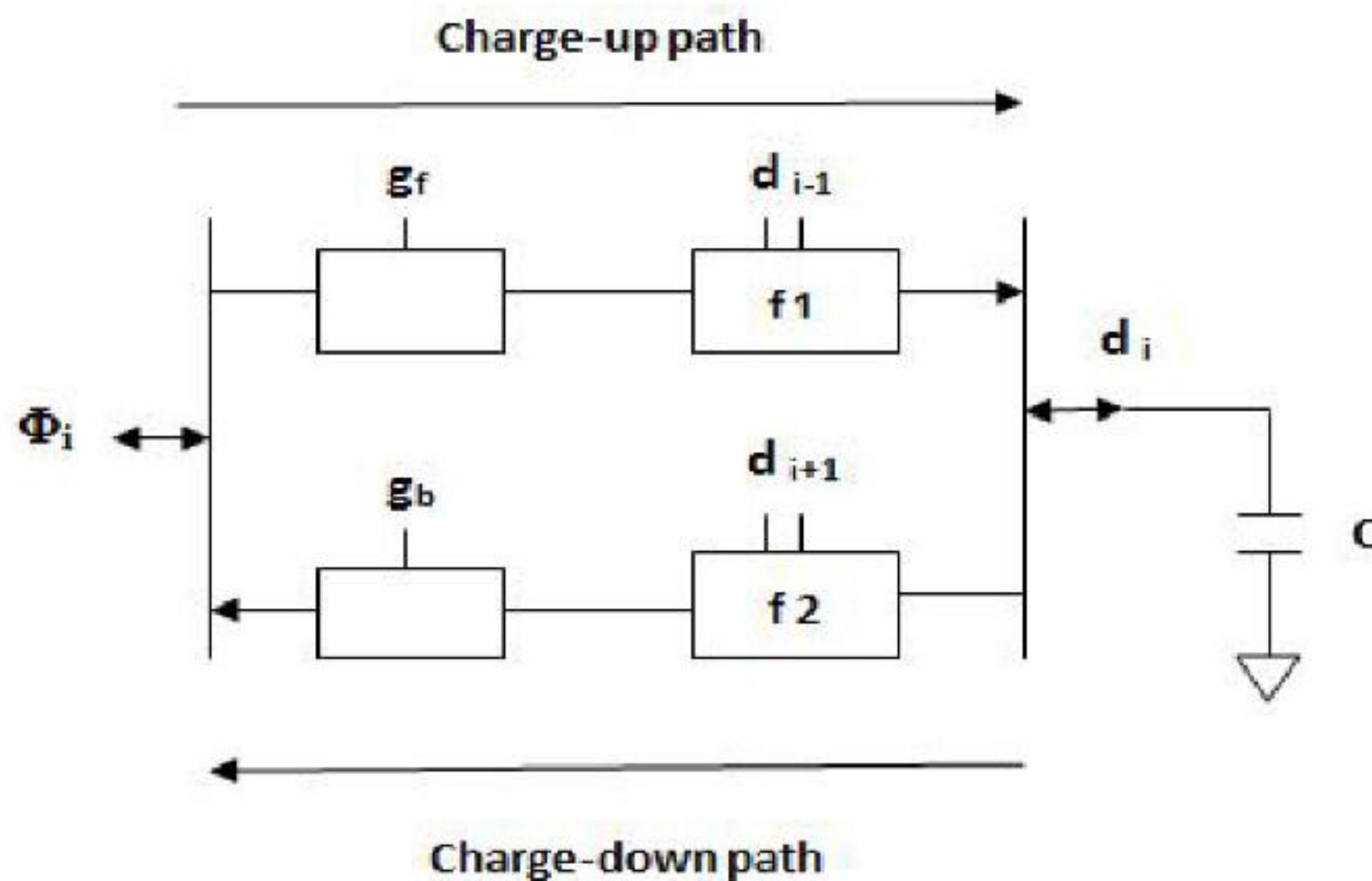
where  $C_1$  and  $C_2$  are the capacitance across the terminals of the switch and  $V_1$  and  $V_2$  are their voltages. When there is a difference in voltage across the switch it causes non adiabatic losses as it is proportional to the square of the voltage difference. So zero voltage switching should be satisfied that is the transistor should not be turned on when there is a potential difference between the drain and source to eliminate non-adiabatic losses. In the case of adiabatic circuits with non-adiabatic losses, reversible logic can be used to recycle the energy. To recycle the energy, separate charge recovering path is required and the input has to be constructed from the output which is possible only with reversible logic. Even though SCRL uses reversible logic, RERL is preferred as RERL requires less clock rails compared to SCRL [2].

The rest of the paper is organized as follows: section 2 describes the switching scheme in adiabatic logic. The Reversible Energy Recovery Logic (RERL) and RERL inverter/buffer is explained in section 3. Section 4 explains the proposed RERL NAND/AND gate and RERL SR latch. Section 5 shows the simulation results using HSPICE and the conclusion is given in section 6.

## 2 Switching Scheme in Adiabatic Logic

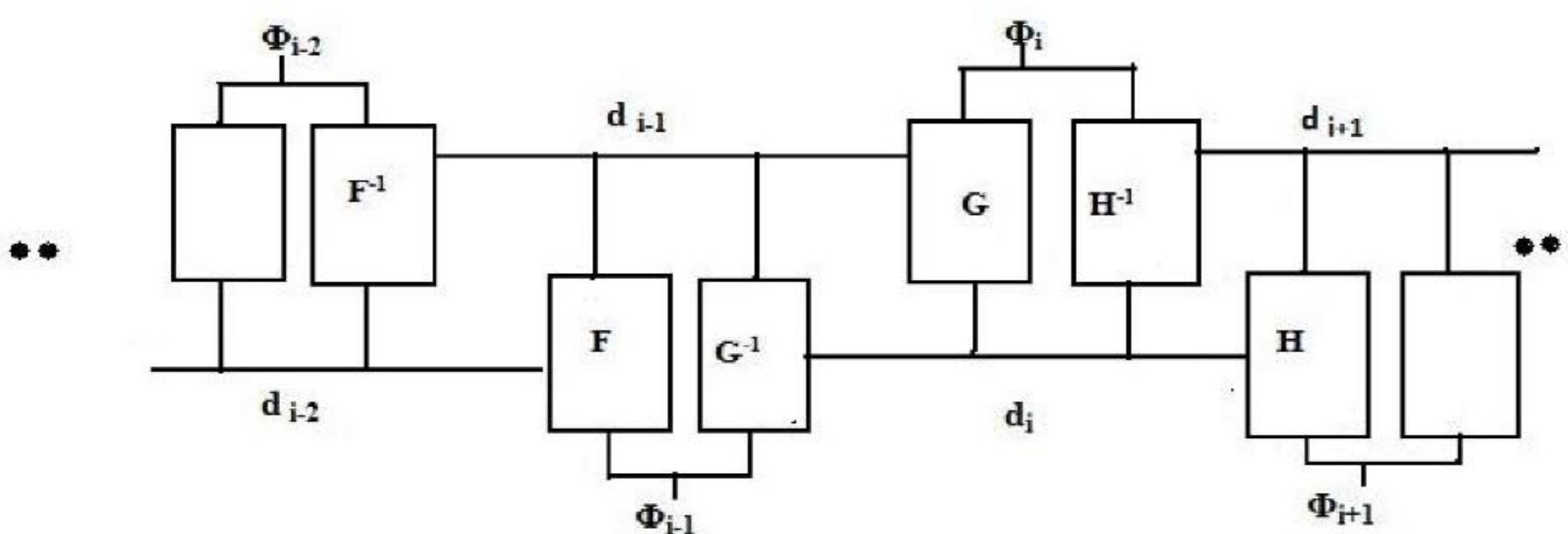
The adiabatic switching scheme is shown in Fig.1. It consists of a charge up and a charge down path with a clock signal  $\Phi_i$  to power the circuit. The unlabelled boxes are single transmission gate which is provided with input signals  $g_f$  and  $g_b$  to guard against the non-adiabatic loss. The labeled boxes indicate a network of transmission gates which are connected in series or parallel to implement Boolean functions [5].

The reversible operation can be achieved by ramping up and ramping down the clock signal  $\Phi_i$  and by providing inputs to the labeled and unlabelled transmission gates. When  $\Phi_i$  ramps up, the load capacitor will be charged to  $d_i$  via charge-up path and then the operation of the circuit is reversed by ramping down  $\Phi_i$ . Thus the energy is recycled back to the power supply by using the charge down path. The logic functions are computed by making use of charge up path. The output of one stage is given as the input to the next stage in a cascading fashion. This becomes impractical when the number of cascaded stages is high and hence pipelining is used.



**Fig. 1.** A gate structure suitable for reversible logic [5]

By using pipelining, inputs of the earlier stages can be changed before the final output is ready. It can be done by computing the inverse of each function as data passes from one stage to another. The function is performed by the transmission gates and its inputs in the charge down path. The inputs to the transmission gates  $f_2$  is obtained from the output of the next stage. The energy is recycled through the charge down path when the clock signal  $\Phi_i$  ramps down. The pipelining connection is shown in Fig.2.



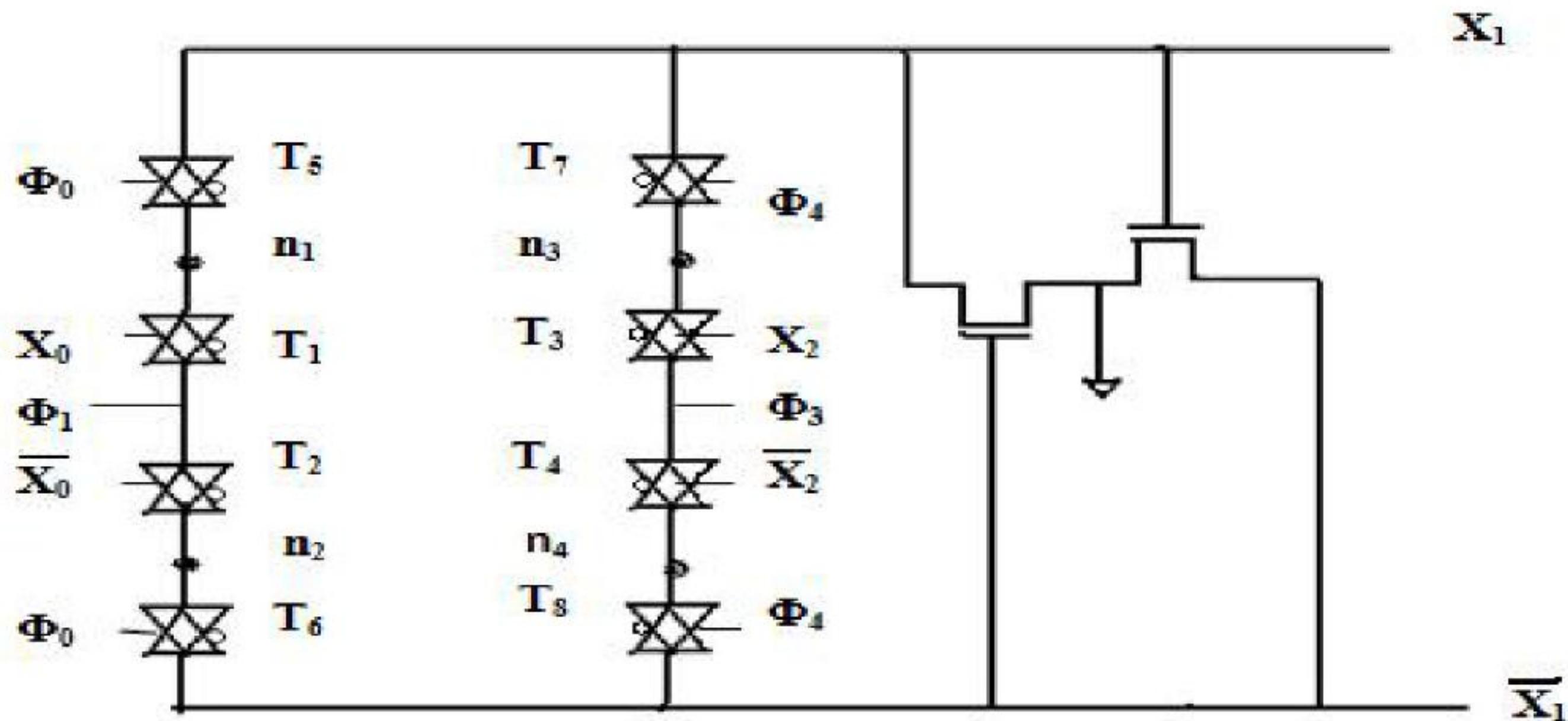
**Fig. 2.** Interconnection of logic gates in a pipeline [5]

### 3 Reversible Energy Recovery Logic

RERL is a dual rail adiabatic logic circuit that uses the concept of reversible logic to eliminate non-adiabatic energy loss by satisfying Zero-Voltage Switching (ZVS). Due to inherent micropipelining RERL computes one logic level per clock phase. So in RERL a long pipelined stage is there to implement a logic circuit.

The RERL buffer or inverter [1,7] is shown in Fig.3 and its pipeline connection is shown in Fig 4. The circuit is implemented using 18 transistors to reduce the power

dissipation. Therefore the area overhead is higher in reversible logic as compared with static CMOS logic. The transmission gates are used in the circuit design to avoid non-adiabatic losses due to signal degradation [8].



**Fig. 3.** RERL inverter or buffer [1]

RERL inverter or buffer uses 8 phase clocking scheme for its operation.  $X_0$  is the input signal and  $X_1$  is the pipelined output signal.  $X_2$  is the output of the next stage whose input is  $X_1$ . The transmission gates  $T_1$  and  $T_2$  implement forward logic function and will determine the charging path of output node whereas  $T_3$  and  $T_4$  implement backward logic function and determine the discharging path of output node.  $T_5$  and  $T_6$  are the forward isolation switch which isolate the charging path and  $T_7$  and  $T_8$  are backward isolation switch which isolate the discharging path.

The operation of the circuit is as follows [1]:

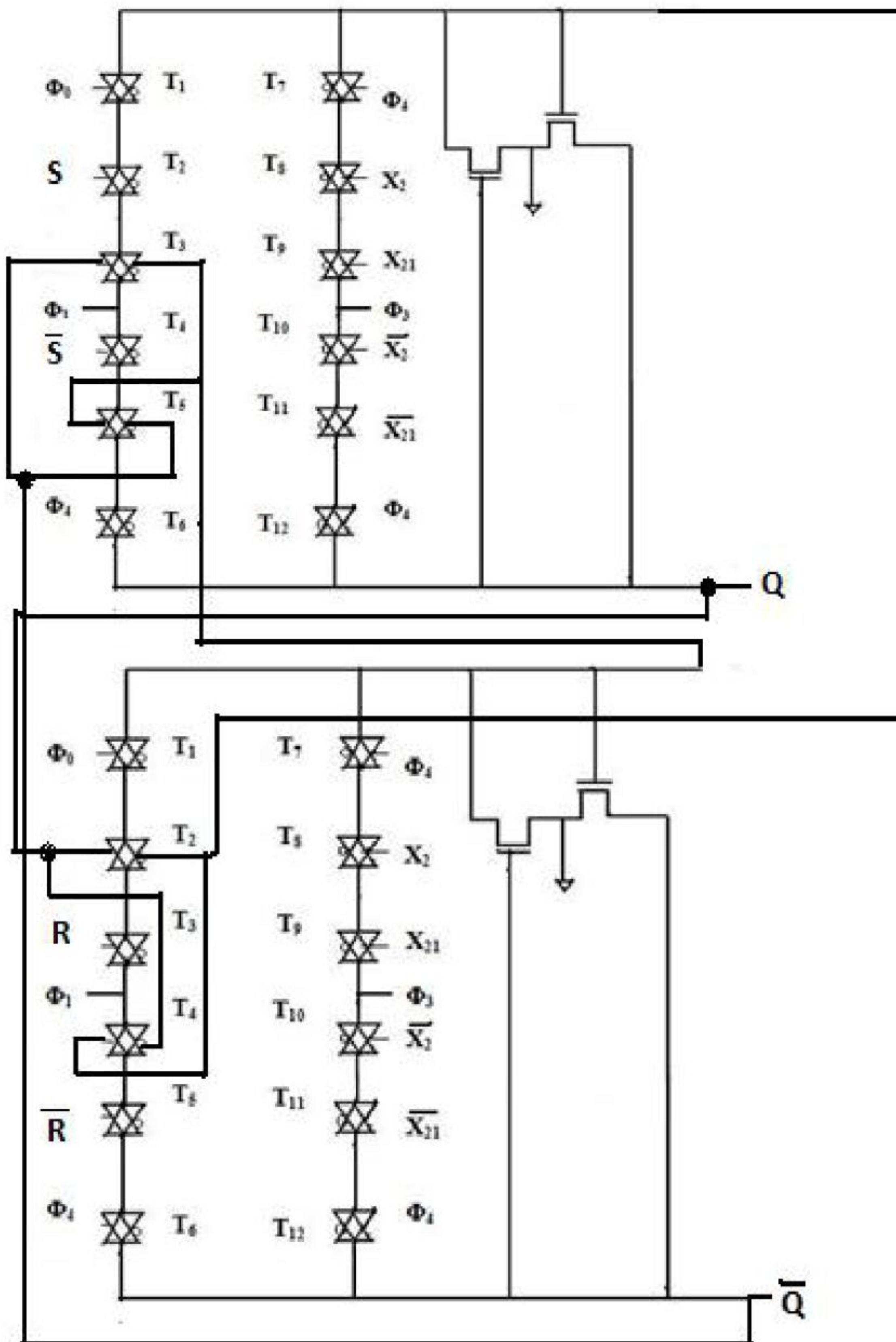
In RERL inverter all the internal nodes are initially grounded and they do not have any abrupt voltage change to satisfy ZVS condition. During the time interval  $t_0$ , when the input  $X_0$  goes high and the clock signal  $\Phi_0$  ramps up, the forward isolation switch  $T_5$  and  $T_6$  are turned on. At  $t_1$  the clock signal  $\Phi_1$  goes high,  $X_1$  and internal node  $n_1$  follows it. During this time interval  $n_2$  remains low as the transmission gate  $T_2$  is off. As  $X_1$  goes high during  $t_1$  it will become the input of the next stage and the output  $X_2$  of the next stage goes high during  $t_2$ . During  $t_3$  transmission gate  $T_3$  will be turned on as  $X_2$  is high and thereby  $n_3$  goes high. Forward isolation switches  $T_5$  and  $T_6$  are turned off during the time interval  $t_4$  as  $\Phi_0$  ramps down. But  $\Phi_4$  goes high and hence the backward isolation switches  $T_7$  and  $T_8$  are turned on. During  $t_5$ ,  $\Phi_1$  falls and discharges  $n_1$  and at  $t_6$  falling  $\Phi_2$  in the previous stage discharges  $X_0$ . During  $t_7$  falling  $\Phi_3$  discharges  $X_1$  and  $n_1$ . Transmission gates  $T_7$  and  $T_8$  are turned off during  $t_8$  to repeat the operation.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.

**Fig. 6.** RERL SR Latch

## 6 Conclusion

In this paper, circuits based on RERL is discussed. RERL is dual rail adiabatic logic circuit. The non-adiabatic energy loss in RERL is removed by using the concept of reversible logic. The simulation done using HSPICE proved that the energy dissipation in RERL circuits is less compared with the static CMOS circuits. In conclusion, RERL is suitable for ultra low power application where high performance is not required.

## References

1. Lim, J., Kim, D.-G., Chae, S.-I.: Reversible energy recovery logic circuits and its 8 phase clocked power generator for ultra low power application. *EICE Trans. Electron* E82-C(4) (1999)
2. Khatir, M., Ejlali, A., Moradi, A.: Improving the energy efficiency of reversible logic circuits by the combined use of adiabatic styles. *Integration, The VLSI Journal* 44 (2010)
3. Sunil Gavaskar Reddy, Y., Rajendra Prasad, V.V.G.S.: Comparison of CMOS and Adiabatic Full Adder Circuits. *International Journal of Scientific & Engineering Research* 2 (2011)
4. Athas, W.C., Svensson, L.J., Koller, J.G., Tzartzanis, N., Chou, Y.: Low-power digital systems based on adiabatic-switching principles. *IEEE Trans. VLSI Systems* 2(4), 398–406 (1994)
5. Athas, W.C., Svensson, L.J.: Reversible Logic Issues in Adiabatic CMOS. In: *IEEE Conf. on Physics and Computation* (1994)
6. Kim, S., Ziesler, C.H., Papaefthymiou, M.C.: Charge recovery computing on silicon. *IEEE Trans. on Computers* 54 (2005)
7. Lim, J., Kim, D.G., Chae, S.-I.: A 16-bit carry-lookahead adder using reversible energy recovery logic for ultra-low-energy systems. *IEEE J. Solid-State Circuits* 34(6), 898–903 (1999)
8. Lim, J., Kim, D.-G., Chae, S.-I.: nMOS Reversible Energy Recovery Logic for Ultra-Low-Energy Applications. *IEEE J. Solid-State Circuits* 35(6) (2000)

# Comparative Study of Recent Compressed Sensing Methodologies in Astronomical Images

Nidhin Prabhakar T.V.<sup>1</sup>, Hemanth V.K.<sup>1</sup>, Sachin Kumar S.<sup>1</sup>,  
K.P. Soman<sup>1</sup>, and Arun Soman<sup>2</sup>

<sup>1</sup> Centre for Excellence in Computational Engineering and Networking  
Amrita University, Coimbatore-641112, India

<sup>2</sup> Department of Information Technology,  
Rajagiri School of Engineering & Technology

**Abstract.** Compressed sensing(CS) which serves as an alternative to Nyquist sampling theory, is being used in many areas of applications. In this paper, we applied recent compressed sensing algorithm such as DALM, FISTA and Split-Bregman on astronomical images. In astronomy, physical prior information is very crucial for devising effective signal processing methods. We particularly point out that CS-based compression scheme is flexible enough to account for such information. We try to compare these algorithms using objective measures like PSNR, MSE et al. With these measures we intend to verify the image quality of reconstructed and original images.

## Introduction

Compressed Sensing(CS) also known as compressive sensing, is a new field of interest based on sparsity that has emerged and rapidly attracted much attention in recent years. CS created a complete paradigm shift to the area of sampling. The theory of compressed sensing, or compressive sampling [4], [5], [6] states that signals which are sparse in some basis may be perfectly reconstructed when under-sampled at more than Nyquist rate, subject to a specific constraint. The solution i.e. the image reconstruction can be obtained by using  $\ell_1$ -norm minimization methods like DALM, FISTA, Split-Bregman reconstruction etc.

Here we are dealing with astronomical images which are of very large size and the advantage of applying CS on astronomical images are:1.One can use a single sensor to capture astronomical images(Research is still going on for developing a single-pixel camera, though RICE university has proposed a design for one.)2.Imaging time and power consumption can be reduced.3.Only less data required to recover the super-resolution photos and thus the storage space for acquired image reduces.4.The highly compressed data can be taken by CS cameras and can be easily transmitted back to earth[2].

Application of compressed sensing in astronomy Bobin et al. in [1] was very recently proposed in which on board data compression for the future Herschel space observatory was discussed. It was required by ESA to obtain a compression ratio of atleast 2.5 which can be easily achieved using CS. The versatility of



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



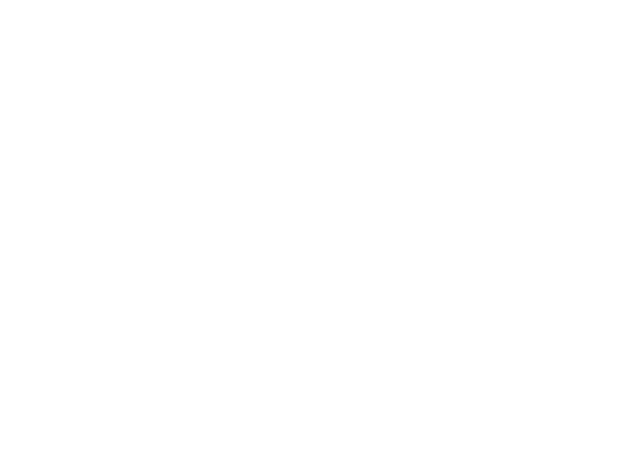
You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



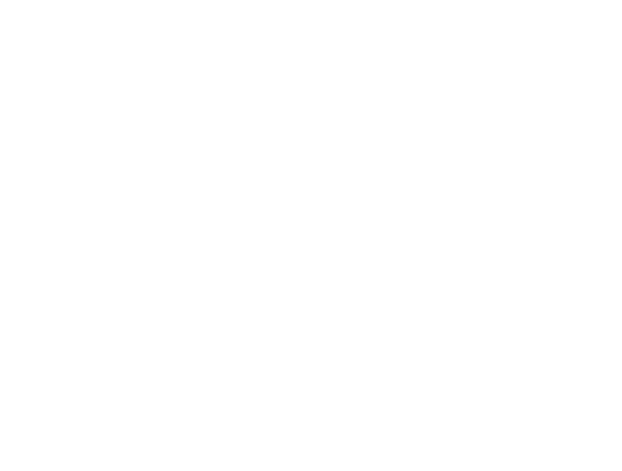
You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.

8. Dinur, L., Nissm, K.: Revealing Information while Preserving Privacy. In: Proceedings of 22nd ACM Symposium on Principles of Database Systems, pp. 202–210 (2003)
9. Andrew, Y.: Making Privacy Preserving Data mining Protical with Smartcards (2009)
10. Canetti, R.: Security and Composition of multiparty Cryptographic Protocols. *Journal of Cryptology*, 143–202 (2000)
11. Canetti, R., Ishai, Y., Kumar, R., Reiter, M.K.: Selective Private Function Evaluation with Application to Private Statistics. In: 20th PODC, pp. 243–304 (2001)
12. Lindell, Y., Pintas, B.: Preserving Data mining. *Journal of Cryptology*, 177–206 (2002)
13. Witreman, M.: Advances in Smartcard Security. *Information Security Bultrin*, 11–22 (2002)
14. Bayardo, R.J., Agrawal, R.: Data Privacy through Optimal k-anonymization. In: Proceedings of the 21st International Conference on Data Engineering (ICDE 2005), pp. 217–228 (2005)
15. <http://Research.microsoft.com/en-us/projects/Databaseprivacy>
16. <http://www.nextgenerationdatabasesystems.com>
17. <http://www.privacypreservingbiblography.com>
18. Recent IEEE Papers on Privacy Preserving datamining
19. Kolitz, N.: A Course in Number theory and Cryptography. In: Proceedings of Springer-verlay (1994)
20. Nuiven, I., Herbertz, S., Zuckerman: An Introduction to theory of Numbers. Wiley Easte-ren limited
21. Edpegg, J.R.: Chinese Remainder theorem. In: Wolfram Demonstrations Project (2007)
22. Ding, C., Dingwipei, Salomaa, A.: CRT Applications in Computing, Cooling, Cryptogra-phy, pp. 1–213. World Scientific Publishing (1996)
23. Weisstein, Eric, W.: CRT, from mathworld
24. Asmuth, L.A., Bloom, J.: A modular approach to key safe guarding. *IEEE Transactions on Information Theory* (1983)
25. Ifrene, S.: General Packett sharing Based on the CRT with Applications in E-voting. ENTCS, pp. 67–84 (2007)
26. Behrouz, Forouzan, A.: Cryptography and network security, pp. 20–40. The MC Graw Hill Companies (2005)
27. Borodin, A.B., Muhro, I.: For an interesting collection of papers that deal with evaluation, interpolation and modular arithmetic See. *The Computational Complexity of Algebraic and Numeric Problems*

## Author Index

- Abraham, Chikku 69  
Ahmad, Musheer 135  
Anita, J.P. 84  
Asokan, K. 311  
Aswathi, B.L. 204, 222
- Babu, C. Nelson Kennedy 255  
Bajaj, Rakesh Kumar 372  
Banerjee, Indrajit [30](#)  
Barthwal, Anurag 170  
Bhattacharjee, Subhadeep 62, 381  
Bhattacharya, Ujjwal 389  
Bhattacharyya, S. 282
- Chakrabarti, Arun Kumar 398  
Chakraborty, Anirban 398  
Chanak, Prasenjit [30](#)  
Chandran, K.R. 125  
Chaudhury, Ayan 389  
Chauhan, Durg Singh 247  
Chauhan, Rashmi 18, 413, 422  
Christinal, Hepzibah A. 162
- Das, Debashis 262  
DeepaPrabha, G. 145  
Dey, Anindita 62  
Dhara, Bibhas Chandra 178  
Díaz-Pernil, Daniel 162  
Divya, S. 77
- Gayathri, V. 352  
George, Santhosh 293, 302  
Goli, Baharak 204, 222  
Gopmandal, Partha P. 282  
Goudar, Rayan 18, 413, 422  
Govindarajan, Renganayaki 204  
Gudigar, Anjan 153  
Gupta, Nitin 372  
Gurunarayanan, S. [9](#)
- Heinrich, Stefan 319  
Hemanth, V.K. [108](#)
- Jabbar, Abdul 406  
Jabir, Abusaleh 230  
Jacob, Jaison 54
- Jacob, Jeeva Susan 364  
Jacob, Jis Mary 47  
Jagadale, B.N. 153  
Jain, Arpit 135  
James, Divya 239  
John, Anita 47  
Jose, Babita R. 54, 69  
Joy, Chinu 222  
Jurado, Pedro Real 162
- Karthika, A.L. 145  
Kayalvizhi, N. [100](#)  
Khaliq, Faizan [9](#)  
Khare, Vipul 135  
Kilari, Veeraswamy 186  
Kiran, D.C. [9](#)  
Koolagudi, Shashidhar G. 117, 170  
Kumar, Jitendra 319  
Kumar, Tanuj 372
- Madhavan, Kavitha 93  
Mahalingam, P.R. [1](#)  
Mahesh, P.K. 153  
Maiti, Chinmay 178  
Maity, Soumen 327  
Mandal, J.K. 262, 398  
MariMuthu, C. 145  
Mathew, Jimson 54, 230, 269, 339  
Medhi, Bhaswati 381  
Meenakshi, V.R. 125
- Nair, Achuthsankar S. 204, 222  
Narasimha, G. 434  
Narayanan, Vinu K. 269  
Narni, Nageswara Rao 319  
Nawal, Abhijeet [9](#)  
Nidhin Prabhakar, T.V. [108](#)  
Nitin 247
- Olivia, Diana 77
- Pareth, Suresan 302  
Peglow, Mirko 319  
Phaneendra, P. Sai 39  
Philip, Mintu 239



You have either reached a page that is unavailable for viewing or reached your viewing limit for this book.