-> Concurrent Datastructures

Harburgs -> Concurrent
Synchronised

-> How memory to stored for process

-> fragmentation

-> MMU -> memory management wait

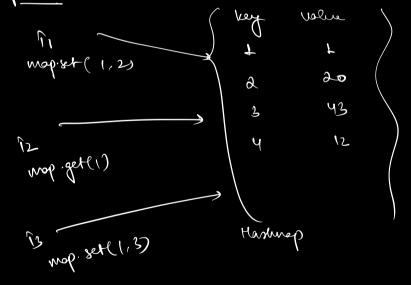
-> Paging

-> Page Replacement algo

-> Page fower

-> Deadlocks

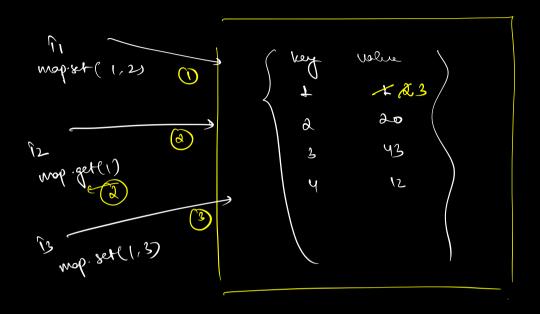
=) Hashmaps:

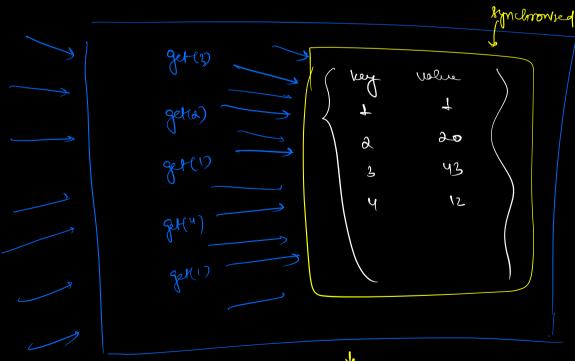


Chances of race coroly

· making it synchronised to make it thread safe:

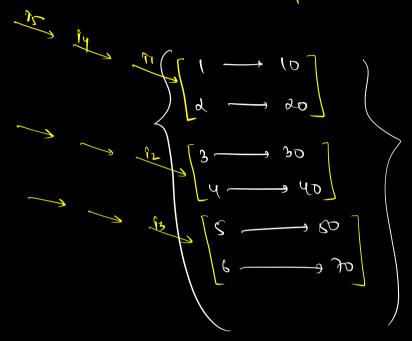
Lynchronised Hashmap]





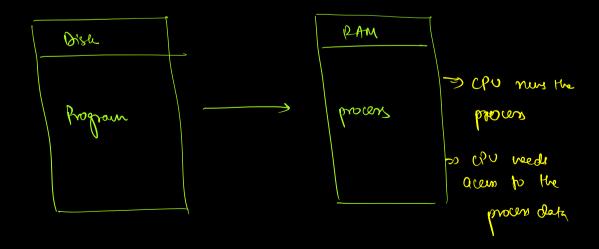
since only I thread can execute at a time this is not fast enough

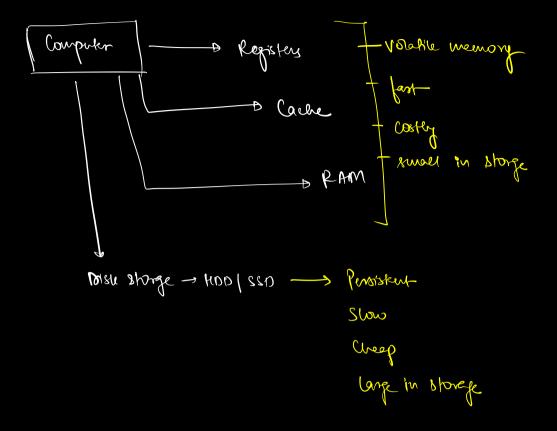
Concurrent Hashmap: "It allows muchiple threads to operate on the map but synchronises buckets—
in side the map.



: Memory Management

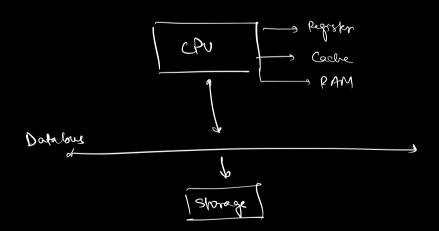
-> How exactly data is stored in a process ?





: CPV cant directly table to storage devices

(because of speed differences)



=> Some programs appres can be huge in size

There can be scenarios where complete process may

RAM = Y LB.

en on 1) homes

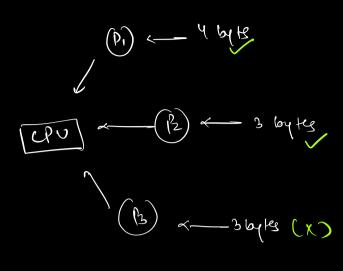
- 11) Too way talks on chrome
- us video editing
- W) IDES (Android Studio)
- V) highly dota intentive algo

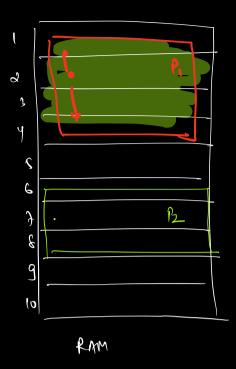
- How does it work?

- -> team process to shored on memory;
- & CPV alwestes memory for process in RAM, then starts executing.

4 CONTIGUOS MEMORY ALLOCATION;

CPU allocates a part of the free PAM to complete for comprete execution





=> faster

=> complete data of the process 19

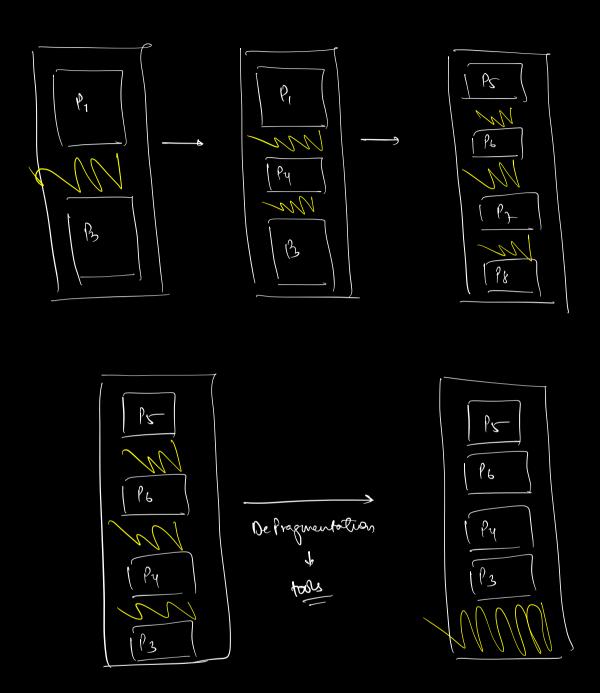
always or memory

=> wastage

rode vearly data, and stores it in

when a CPV K

fragmentation (pieces, parts) > memory divided into smaller churches leads to wastage of memory



how do we actually execute it?

Pahneh - reality. RAM - YUB } extra 2WB Stored Pu a dish
Req - 6UB HOD SID / flash arriver privaple > -> store wholever is possible in RAM - everything close to be stored in he disk 2 a B 4 WB COH 6 MB

so whenever CPV needs to accens something, from the obst., it is first brought but memory, then accensed by CPV.

An

Who does all this work?

MMV (memory management with

=> Deep dine on Paging !

There are a type of addresses!

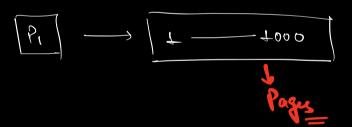
1) bejæl addrers - conceptral addrers

1) Physial address - real address.

=> Appre will only know or "logical addresses"

=> At soon as a process starts, MMU allocates a huge no. of conceptual address (logical address to it.

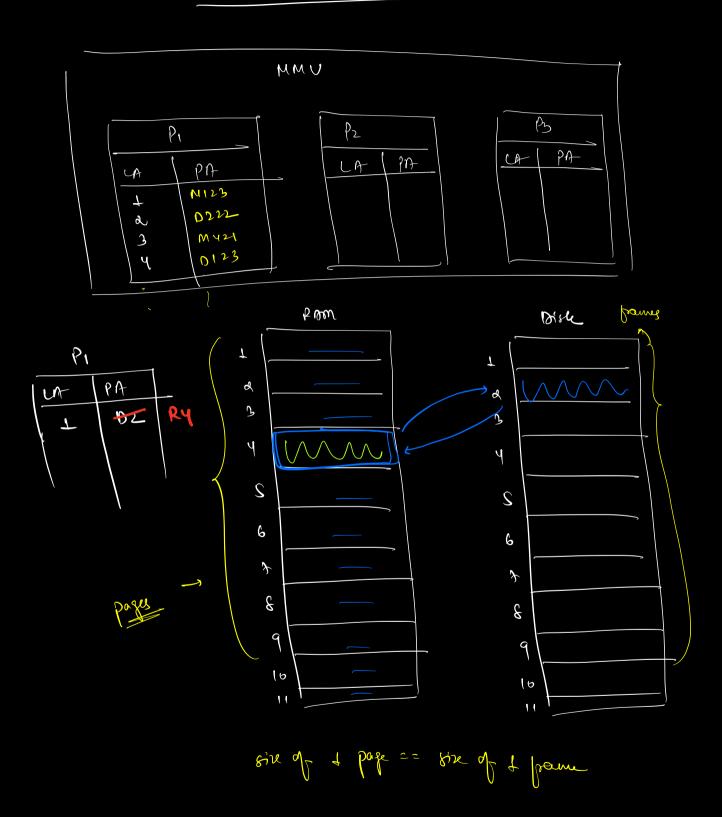
Those Passe)



=) MMV Enternally maintains a table to map the cogical address to scal purplear address.

PAM or disk

table = Process Page table



=> [Page Replacement]

Page replacement algo - decides which

page to remove from RAM, when a new

from from Disk has to be brought in RAM.

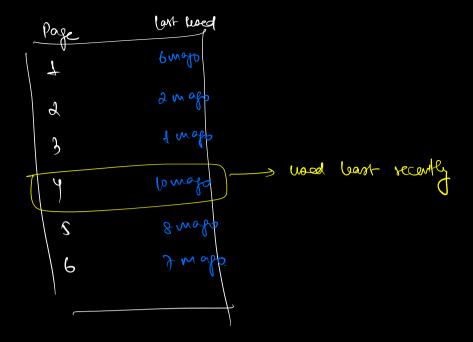
=> 1. FIFO -> Perst for First out

	Pages	dureton	
bru	(M	
) a	6M	
	3	6M	
	4	MO)	Older page (fist fu)
	S	(2 M	
	6	161	
	7	24	

11) IRV -> least recently word

replace the page which was least—

recently word



111) LIFO - last in first out

PAGING!-

PRO

- 4 no memory think
- 4 no memory wastage

CONS

- a complex to design
- d flower
- * oppn doesn't know where exactly the data is prosent

accen the data; How process PU 5 to ogecute needs the data CPU CU usu get the logical adriken. CNI CPU MMU with logical addr. MMU matines (logical -> physical) こ process table address present en diste proent in RAM 1) sur a page seplacement

algo

11) explace the page

in setur to Cho

proces place

octum to CPU

Page Fault: when CPU asks MMV for data but data is present in disk of instead of RAM.

-> reigner no. of page four

-> long. slowners