Design of 6T CMOS SRAM

Abstract:

Semiconductor devices should have low power consumption and high speed operation when it comes to deploying them in applications where computation speed matters. If we go into transistor level , power consumption and area will depend on transistor operating voltage and its W/L ratio.

Reference Circuit details:

Low power SRAM Cell design can be designed by the back to back connection of two CMOS inverters.. With this analogy , low static power dissipation can be achieved due to less leakage current in the cell. For designing W/L ratio , two aspects need to consider (i) information present in the cell should be retained during read operation. (ii) cell should allow modification of data during write operation.

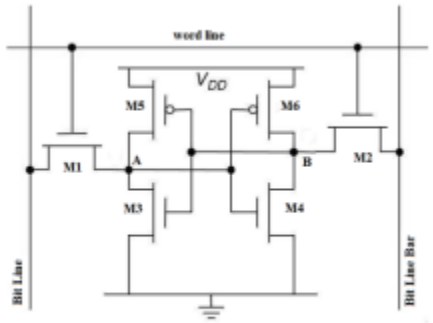


Fig.4.2 6-Transistor SRAM Memory cell[1]

In this design , SRAM is operated in 3 modes

(I) Latch mode

(ii) Write mode

(iii) Read mode

(I) Latch mode: In this mode, word line is off due to which M1 and M2 transistors are off. During this mode, memory cell retains its previous data as long as power supply is given. Here Column capacitances are the charges to supply voltage through M5 and M6. In this mode , cell consumes less power

(ii) Write mode: if the logic 0 has to be written to the cell , assuming initial data present in the cell is logic 1. voltages present at node A and B are VDD and 0 respectively. Hence M3 and M6 are off, M4 and M5 will operate in linear region. Now BL is set to logic 0 , M1 and M2 are set to activate by using word line. inorderto achieve this, we should have

$$\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_1} < \frac{\mu_n}{\mu_p} \frac{2(V_{DD}-1.5V_{T,n})V_{T,n}}{(V_{DD}+V_{T,p})^2} \quad \text{---------- (A)}$$

(iii) Read mode: The prerequisites for read mode will be the bit line voltages should be VDD(with help of precharge circuit). If the read 0 operation need to perform , assuming data stored is logic 0 and initial voltages present at nodes A and B are 0v and VDD. So M4 and M5 will be off , whereas M3 and M6 will be in linear region. Pass transistors M1 and M2 are turned on by using word line. Now , there is no current flown through M2, Since voltage at node B and BL Voltage are equal to VDD. M1 and M3 transistors will exhibit a non zero current due to BL voltage discharge from VDD to Gnd. Now if both the bit line voltages are given to the input of sense amplifier[17] and it will produce logic 0 as output.

$$\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_3} < \frac{2(V_{DD}-1.5V_{T,n})V_{T,n}}{(V_{DD}-2V_{T,n})^2} \quad ----------(B)$$

Sense Amplifier- A sense amplifier is part of the read operation that is used when data is to be read from the SRAM cell, it senses the low power signals from the bit lines that represents data bit 1or 0 stored in memory cell.

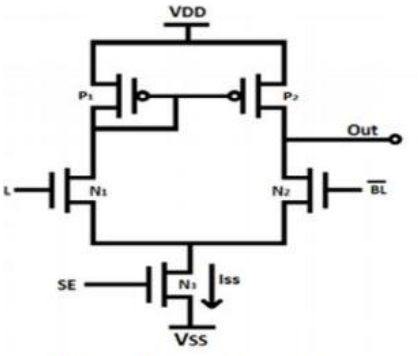


Figure.2. Sense Amplifier

Precharge- This circuit helps in charging both the bit lines to supply voltages Vdd.

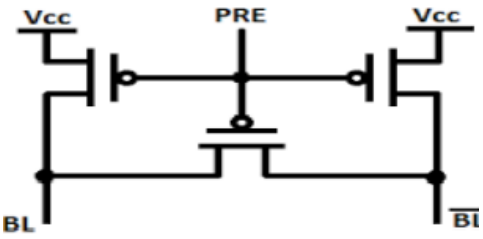
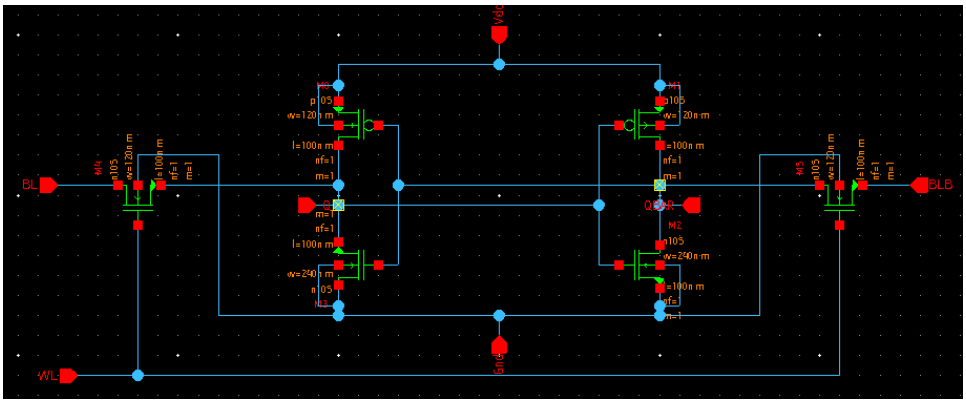


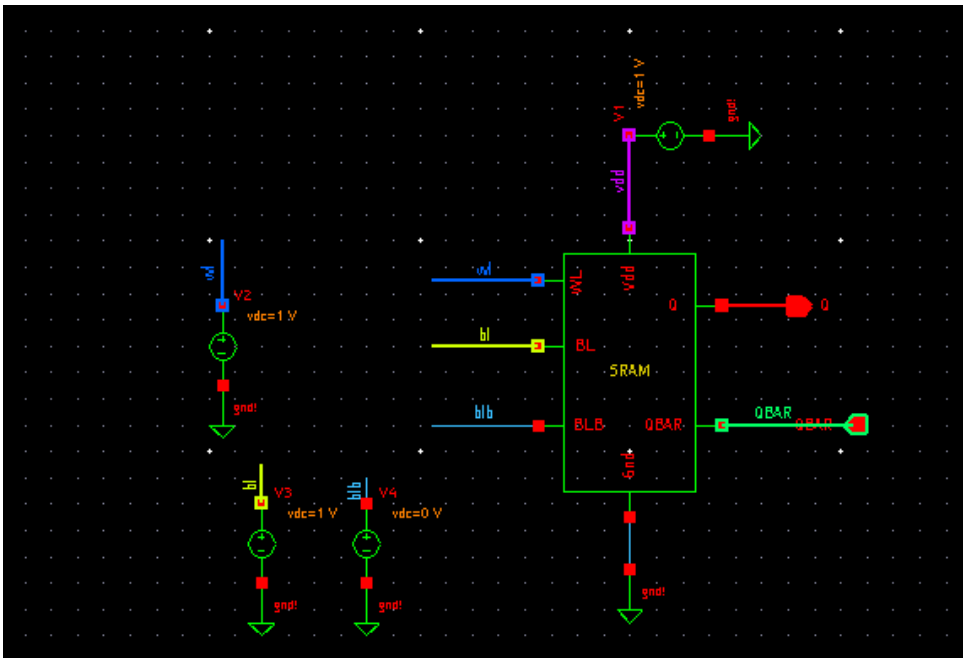
Figure.3. Precharge circuit

Reference circuit design:

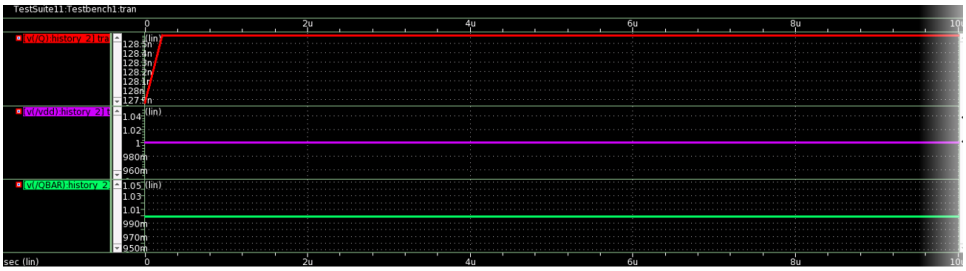
Schematic for 6T SRAM :



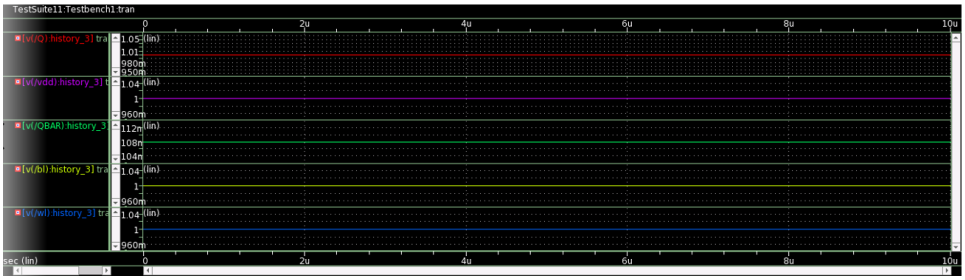
Testbench schematic for latch and write mode:



Waveform for standby:



Waveform for write:



Note:

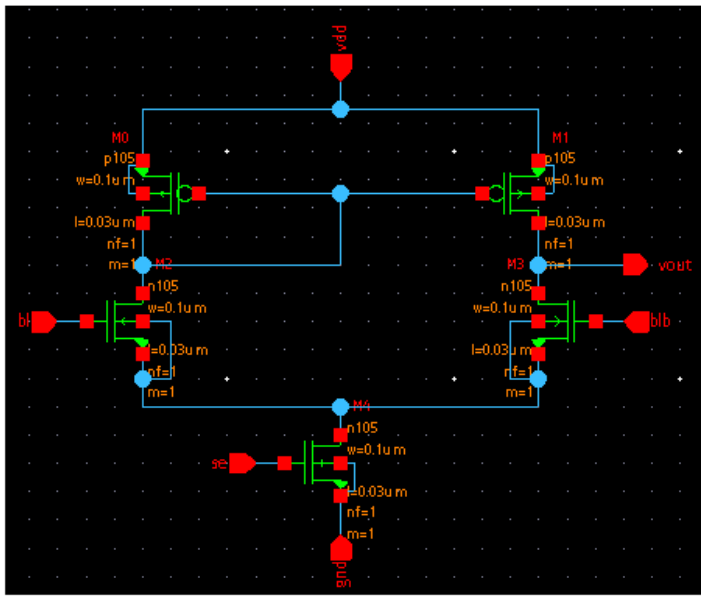
During latch mode -

I)WL lines are made as off.

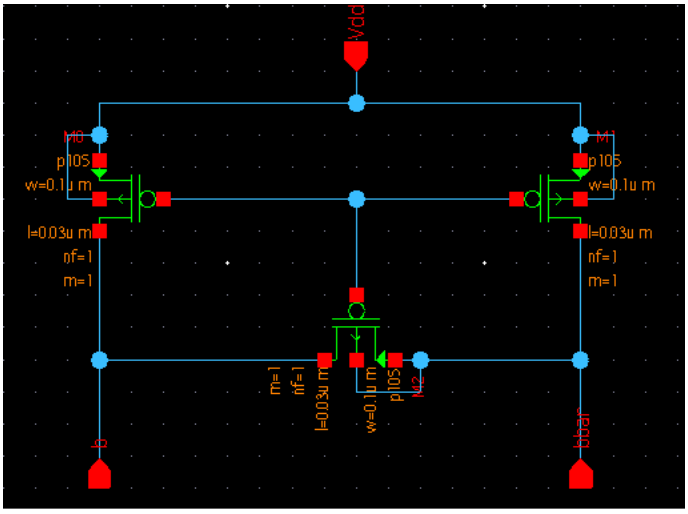
During write mode -

I) WL lines are made as high and BL line is made as high.

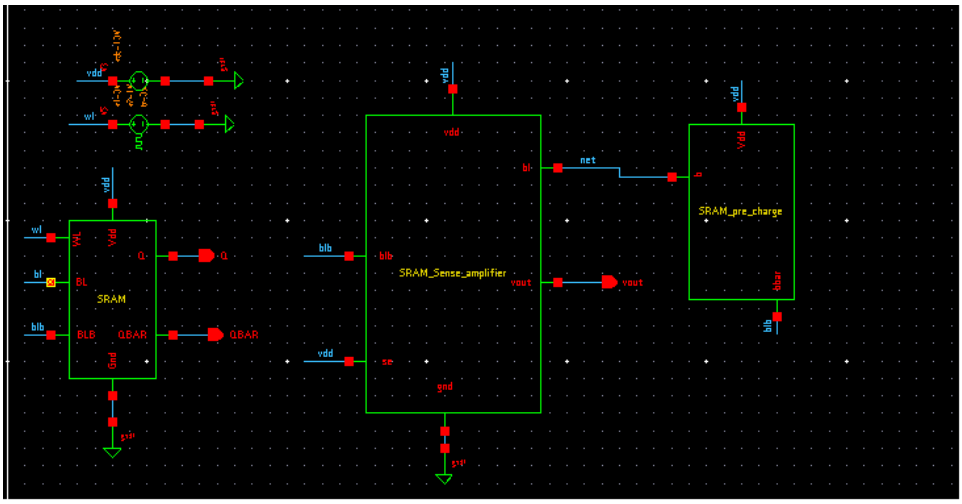
Schematic for Sense amplifier :



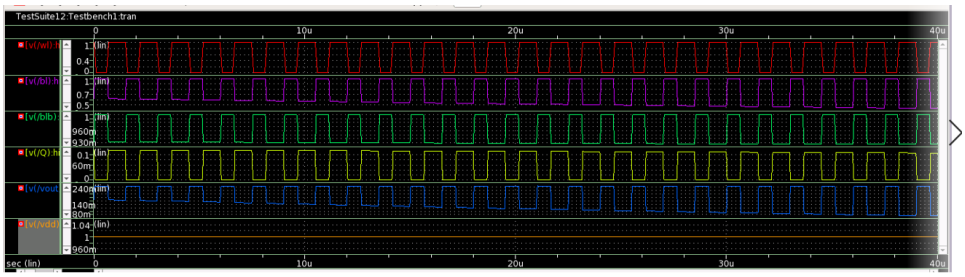
Schematic for Precharge :



Test bench schematic for Read operation:



Waveform for read operation:



Reference papers/journals - [1]CMOS VLSI Design A Circuits and Systems Perspective Fourth Edition Neil H. E. Weste ,David Money Harris

[2] Debasis Mukherjee,Hemanta Kr.Mondal,‖Static Noise Margin Analysis of SRAM Cell For High Speed Application‖, IJCSI International Journal of Computer Science Issues, Vol. 7,Issue 5,September 2010.

[3] Performance Analysis of SRAM at Different Technologies using Cadence, Manoj Padmanabha Murthy. T1 , Nithin. N 2 , Pallavi. N 3 , V. Rajashekar4 , Sharanagouda. V Patil5 Student. Volume 10 Issue 6, June 2020