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Single CCTA based high frequency floating and grounded type of incremental/decremental memristor emulator and its application

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ABSTRACT

This paper reports a new charge controlled practical memristor emulator circuit based on single current conveyor transconductance amplifier (CCTA). The proposed grounded and floating type memristor emulator circuit can be configured as both incremental and decremental types. Both the floating and grounded memristors are obtained simultaneously from the same circuit without any alteration. The circuit is very simple as compared to existing circuits and avoids the utilization of ADC, DAC, analog multiplier and multiple sub-circuits. It exploits the controllability of transconductance of CCTA for multiplication. It performs well up to a few MHz. Experimental verification of this circuit has been performed using the commercially available integrated circuits, CFOA (AD844AN) and OTA (CA3080). It has been tested at a frequency range from 5 kHz to 30 kHz. Moreover, as an application, amplitude modulation (AM) of frequency modulated (FM) signal and demodulation using the proposed memristor emulator circuit has been discussed. It confirms the functionality of the proposed circuit. The PSPICE simulation results and experimentally obtained results are included.

1. Introduction

Memristor is a fourth basic circuit element after the resistor, capacitor and inductor, postulated in 1971 by Leon O. Chua [1]. It is a two terminal resistive device, which retains its resistance value, hence its name. A memristor can be used in sensors, cellular networks, chaotic circuits, analog circuits, digital logic neuromorphic systems [2,3] and also has a numerous other exciting prospects. The basic principle of flux and charge controlled memristor is that, when current flows in one direction its resistance increases, similarly when current flows in the opposite direction, its resistance decreases and when the current flow stops, it keeps the same resistance till the time current flow starts again. The article entitled 'Memristive devices and Systems' in 1976 explains the theory of memristor and memristive systems [4]. After thirty-seven years of the Leon Chua's proposal, first solid state memristor using platinum (Pt) and titanium dioxide (TiO_2) was fabricated by Hewlett-Packard (HP) Labs in May 2008 [5], which shows the behaviour of hypothetical memristor. TiO_2 memristor was a milestone for realm of memristor. However study of this device was a little bit complex and hard itself for its designers. It took them about six years from 2002 to 2008 to formulate its model and finally they presented their model in [5]. It opened doorway for new researchers to work with memristor. However, TiO_2 based memristor is not commercially available due to cost and many complications in fabrication at the nanoscale level. In [6–15] a variety of circuits have been reported in the literature and each one has its own advantages and disadvantages. The flux controlled memristor circuit [6] can be used to verify the memristor properties experimentally, but it cannot be used to emulate a memristor in practical circuits. Piecewise linear model [5], SPICE macromodels [7–14] and cubic nonlinear functions [15] have been used to imitate the memristor properties. Some of them used model presented by HP Labs [5]. The macro models are advantageous for simulating memristor, but cannot be used to build hardware for real applications. Due to these reasons some memristor emulator circuits, which resembles the actual memristor, have been developed [16–31] for real application devices.

Several operational amplifier and analog multiplier based emulators were used to built complex and bulky circuits with hysteresis loop operating at low frequency due to various parameters of active devices. Some topologies offer high speed being less dependent on parasitics due to simple circuitry [15–18], however, at high frequencies the parasitic effect increases which limit the maximum operating frequency of the circuit. The programmable analog circuit based memristor emulator [19] contains a microprocessor, an ADC and a digital potentiometer, but its performance is limited by the ADC sampling frequency and stepping resolution. Although incremental and decremental memristor emulators are proposed in [20,21] using several solid-state devices to match the real properties of TiO_2 memristor but pinched hysteresis loops of memristors have a low working frequency. Among [14,22–24] CMOS based memristor structure in [22] has a mismatch error on the layout, in [14] excessive resistors have been used, in [23] no practical

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evidence has been found and in [24] low linearity voltage controlled resistors have been found. Some circuits based on varactors, diodes and inductors [25] have been found, which are bulky and costly. In addition, due to the use of varactors and inductors, the circuit cannot store data when power is shut down. In [26] current conveyor (CCII+) and a voltage controlled resistance based simple circuit topology has been used, but the linear range of the transistor is narrow. The light dependent resistance (LDR) based simple circuit proposed in [27] has a low-frequency range and upper limit can vary a few hundred hertz by adjusting discrete components, but it is limited by the physical properties of LDR. The second generation current conveyor based emulator circuits in [28–31] use a large number of active and passive elements. Major drawback reported in [28] is that the emulator cannot work as floating memristor and hence not suitable for complex circuits. The large input impedance is reported in [30,31], which limits its use in current driven circuits. Current feedback operational amplifier (CFOA) and operational transconductance amplifier (OTA) based memristor emulator circuit in [32] contains three active elements and five passive elements. It uses the nonlinear transfer characteristics of OTA. Recently, published article [33] is built from four CFOAs, four capacitors, two diodes, two resistances and one potentiometer. In all the previously discussed literatures, the frequency performance has not been reported except [34,35]. In [34] frequency performance has been discussed, but the number of active and passive devices is more and also has low operating frequency (i.e. 20.2 kHz). The active and passive components used in [35] are less than [34]. It is an incremental or decremental type.

In this paper, a very simple memristor emulator using single CMOS-based current conveyor transconductance amplifier (CCTA), three resistors (one floating, two grounded) and one grounded capacitor is presented. The proposed grounded and floating type memristor emulator circuit can be configured as an incremental and decremental memristor according to the applications. The literature survey reveals that both the grounded and floating type of memristor is not present in the same topology except proposed one. The emulator structure has been tested at different frequencies. The frequency performance analysis of the proposed circuit at different frequencies confirms that the pinched hysteresis loop in voltage (V) versus current (I) plane not only depends on the operating frequency and amplitude but also depends on the value of the passive components used in emulator circuit. To further demonstrate the property of the emulator, the proposed circuit has been tested on printed circuit board using commercially available integrated circuits (CFOA and OTA). An FM to AM convertor has been realized using the proposed memristor emulator circuit as its application.

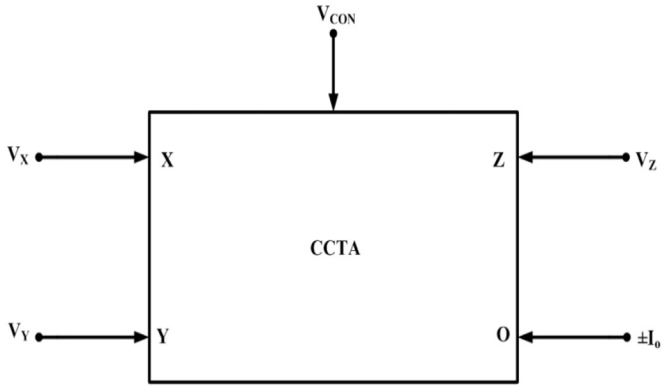

Fig. 1. CCTA symbol.

2. Subcircuit properties

A new building block, namely CCTA is an active element introduced by Prokop and Musil in 2005 [36], which can be used in current mode as well as in voltage mode configuration. Fig. 1 shows the circuit symbol of CCTA, which has low input impedance current mode terminal (X), high input impedance voltage-mode terminal (Y), high impedance auxiliary port (Z) and high output impedance terminal (± O) along with electronically tunable transconductance gain (g_m).

It contains a second generation current conveyor and an operational transconductance amplifier, with the combined advantages of both the circuits. CCTA properties can be described by following equations:

$$I_Y = 0,\ V_X = V_Y,\quad I_Z = I_X,\quad I_{\pm O} = \pm g_m V_Z, \tag{1}$$

where, g_m is transconductance of CCTA, which can be controlled by biasing current I_S generated by V_{Con}. Fig. 2 shows the CMOS implementation of modified CCTA [37], where transconductance (g_m) of the CCTA has been controlled by biasing voltage (V_{con}) and can be expressed as

$$g_m = 2k(V_{con} + V_{SS} - V_T), \tag{2}$$

where k is device parameter and is given by

$$k = \mu_n C_{OX} \frac{W}{L}, \tag{3}$$

where, W and L are respectively channel width and channel length, μ_n, C_{ox} and V_T are respectively mobility of carrier, oxide thickness and threshold voltage of MOS.

The functionality of modified CCTA shown in Fig. 2 is verified

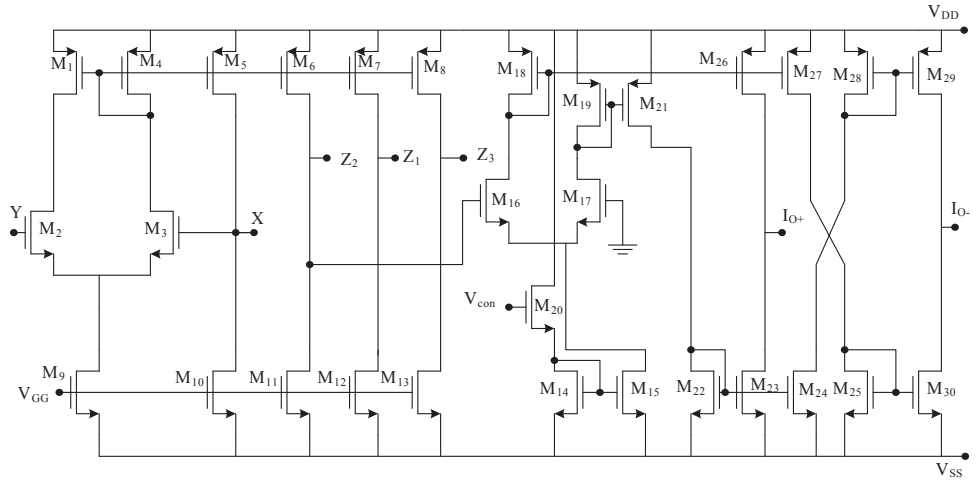

Fig. 2. Internal structure of modified CCTA.

Table 1
Dimension of MOS transistors.

Transistors	W(μm)/L(μm)
M1,M4	5/0.5
M5,M6,M7,M8	8.5/0.5
M2, M9	10/0.5
M14,M15,M16,M17,M18,M19,M20,M21,M22, M23,M24,M25,M26,M27,M28,M29,M30	15/0.5
M3	27.25/0.5
M10,M11,M012,M13	44/0.5

through PSPICE simulation using 0.25 μm TSMC CMOS parameter. The circuit is biased with voltages of $V_{DD}=1.5$ V, $V_{SS}=-1.5$ V and $V_{GG}=-1$V. Aspect ratio of MOS transistors is shown in Table 1. All the MOS transistors are operating in the saturation region. Fig. 3 depicts the simulated transconductance of CCTA, when V_{con} varied from −2 to 2 V and Fig. 4 shows the frequency response (i.e −3 dB bandwidth of I_Z/I_X, V_X/V_Y and I_O/V_{Z2} as shown in Table 2) at the output terminals.

2.1. Proposed emulator circuit

Fig. 5 demonstrates the circuit schematic of proposed grounded and floating memristor emulator circuit, which consists of only one CCTA as an active element, three resistors and one capacitor. It may be noted that incremental/decremental type of floating memristance will be obtained between port 1 and port 2, whereas the incremental/decremental type of ground memristance is available between port 1 and ground.

The input voltage $V_{in}(t)$ is obtained as

$$V_{in}(t)=I_{in}(t)R_1 + V_x \tag{4}$$

Using the characteristic equation of CCTA, we get

$$V_x = V_y = \pm 2k.(V_{con} + V_{SS} - V_T).\ Vz_2.\ R_2 \tag{5}$$

where

$$Vz_2 = I_{in}R_3,\ k = \mu C_{ox}\frac{W}{L} \text{ and } V_{con} = \frac{q_c(t)}{C} \tag{6}$$

Substituting (5) and (6) into (4), it is obtained as

$$V_{in}(t) = I_{in}(t)R_1 \pm 2k.\left(\frac{q_c(t)}{C} + V_{SS} - V_T\right)I_{in}(t)R_2R_3 \tag{7}$$

Then the memristance equation of the proposed grounded/floating incremental and decremental memristor emulator is obtained as

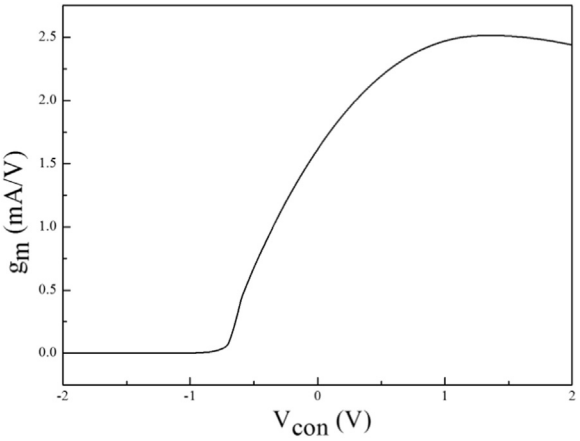

Fig. 3. Transconductance (g_m) versus V_{con}.

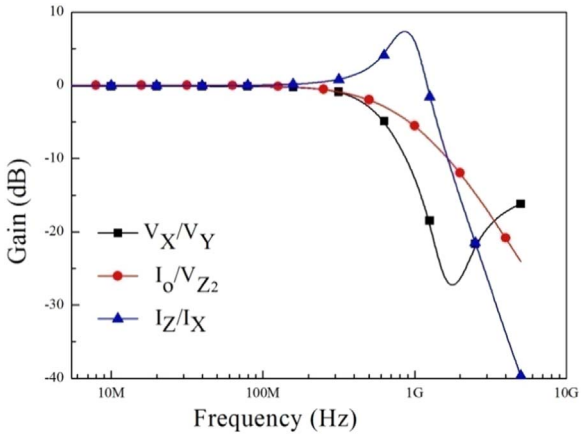

Fig. 4. Frequency responses at output terminal.

$$M(q_c(t)) = \frac{V_{in}(t)}{I_{in}(t)} = R_1 \pm 2kR_2R_3(V_{SS} - V_T) \pm 2k\frac{q_c(t)}{C}R_2R_3 \tag{8}$$

It is important to note that the values of both memristances (grounded and floating type) can be controlled by input signal (V_{in}) and the values of the passive components, but the incremental or decremental behaviour is dependent on the direction of output current at the ± O port (i.e. when +O port is connected to port Y it will act as incremental memristor and when -O port is connected to port Y it will act as decremental memristor) of CCTA as shown in Fig. 5.

To analyze memristive nature of TiO_2 memristor, linear boundary drift model was presented by team of HP Lab [5]. This model as given below was also followed by other researchers [38].

$$v(t) = \left(R_{on}\frac{p(t)}{D} + R_{off}\left(1 - \frac{p(t)}{D}\right)\right)i(t);\ \frac{dp(t)}{dt} = \frac{\mu_v R_{on}}{D}i(t), \tag{9}$$

where R_{on} and R_{off} are minimum and maximum resistances of device. p

Table 2
CCTA parameters.

Parameters	Values
Power Supply	± 1.5 V, −1 V
Power consumption	7.5 mV
−3 dB Bandwidth	1.31 GHz (I_Z/I_X) 511.28 MHz (V_X/V_Y) 612.91 MHz (I_O/V_{Z2})
Transconductance Range	(0–2.4) mA/V
V_{con} Range for controlling g_m	−0.7 to +1 V

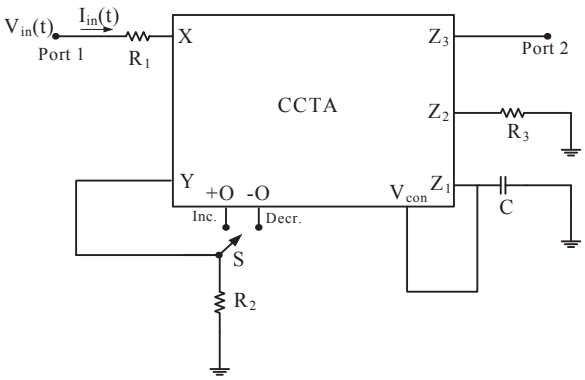

Fig. 5. Proposed memristor emulator circuit.

is length of doped region, μ_v is dopant mobility and D is device full length of TiO_2 thin film. This model is known as linear boundary drift model. The name linear boundary drift comes from the fact that memristance observed in TiO_2 thin film device originates from drift of oxygen vacancies whenever external bias is applied. A more generalized model [39] is

$$M(q) = R_0 - \frac{\eta \Delta R}{Q_0} q(t) \tag{10}$$

where,

$$R_0 = R_{on}\frac{p_0}{D} + R_{off}\left(1 - \frac{p_0}{D}\right)$$

$$Q_0 = \frac{D^2}{\mu_v R_0}$$

$$\Delta R = R_{off} - R_{on}$$

Comparing (8) with (10), following results are obtained.

$$R_0 = R_1 \pm 2kR_2R_3(V_{SS} - V_T);\ \frac{\eta \Delta R}{Q_0} = \frac{2kR_2R_3}{C} \tag{11}$$

Presented memristor emulator shows analogy with linear drift model and it can be controlled by varying value of resistances and capacitance.

2.2. Non-ideal analysis

The non-ideal effects in CMOS implementation of CCTA due to mismatch of transistors are discussed in this section. Taking into consideration of active non-ideal effects of CCTA, the modified port relationships of CCTA can be written as

$$I_y = 0,\quad V_x = \alpha V y,\quad I_{Z_i} = \beta_i I_x,\quad I_O = \pm \gamma g_m V_z,$$
$$I_{Z_i} = \mu_{ij} I_{Z_j},\quad \mu_{ij} = \frac{\beta_i}{\beta_j} \tag{12}$$

where α, β, γ and μ denotes the tracking errors of CCTA and ideally taken to be unity. β_i denotes the tracking error of ith Z-terminal. μ_{ij} denotes tracking error from jth Z-terminal to ith Z-terminal. Considering the non-idealities of CCTA and re-analyzing the circuit of CCTA as shown in Fig. 5, the memristance expression for grounded type incremental and decremental memristor is modified as

$$M'(q_c(t)) \approx R_1 \pm 2k\alpha\beta_2\gamma R_2R_3(V_{SS} - V_T) \pm 2k\alpha\beta_1\beta_2\gamma R_2R_3\frac{q_c(t)}{C} \tag{13}$$

Similarly, for floating type incremental and decremental memristor the memristance expression is obtained as

$$M''(q_c(t)) \approx R_1 \pm 2k\alpha\beta_3\gamma\mu_{23}R_2R_3(V_{SS} - V_T) \pm 2k\alpha\beta_1\beta_3\gamma\mu_{23}R_2R_3\frac{q_c(t)}{C} \tag{14}$$

It clearly indicates that the tracking errors developed due to non-ideality of CCTA effects memristance value.

2.3. Frequency response analysis

In this section, we will study the frequency response of the memristor emulator circuit by assuming an input voltage $V_{in}(t) = A_m \sin(\omega t)$, where A_m is the amplitude of the voltage signal and ω is the frequency of the signal in radian. Average input current can be determined by substituting the time varying part to be zero in (7) and therefore, it is obtained as

$$I_{in}(t) = \frac{V_{in}(t)}{R_1 \pm 2kR_2R_3(V_{SS} - V_T)} \tag{15}$$

As a result, one may obtain,

$$q_c(t) = \frac{A_m}{\omega(R_1 \pm 2kR_2R_3(V_{SS} - V_T))}\cos(\omega t - \pi) \tag{16}$$

Substituting (13) in (8), memristance of the circuit is obtained as

$$M(q_c(t)) = \frac{V_{in}(t)}{I_{in}(t)} = R_1 \pm 2kR_2R_3(V_{SS} - V_T) \pm \frac{2kR_2R_3A_m}{\omega C(R_1 \pm 2kR_2R_3(V_{SS} - V_T))} \cos(\omega t - \pi) \tag{17}$$

It can be seen from the above equation that memristance contains a linear time-variant and a linear time-invariant part. As the frequency of the input signal approaches to infinity, the time varying part in (17) approaches to zero and the resultant memristance will act as the time independent resistor, whose value is constant irrespective of time. Hence, the ratio of their amplitudes is arranged as

$$\varnothing = \frac{2kR_2R_3A_m}{\omega C(R_1 \pm 2kR_2R_3(V_{SS} - V_T))^2} = \frac{1}{f\tau} = \frac{T}{\tau} \tag{18}$$

where τ is the time constant of the emulator circuit given as

$$\tau = \frac{\pi C(R_1 \pm 2kR_2R_3(V_{SS} - V_T))^2}{kR_2R_3A_m} \tag{19}$$

and T is the period of the input voltage signal given by

$$T = \frac{1}{f} = \frac{\pi C \varnothing (R_1 \pm 2kR_2R_3(V_{SS} - V_T))^2}{kR_2R_3A_m} \tag{20}$$

Additionally, if we consider non-ideal effects of the emulator, then for grounded type of memristor emulator, memristance is obtained as

$$M'(qc(t)) \approx R_1 \pm 2k\alpha\beta_2\gamma R_2R_3(V_{SS} - V_T) \pm \frac{2k\alpha\beta_1\beta_2\gamma R_2R_3A_m}{\omega C(R_1 \pm 2k\alpha\beta_2\gamma R_2R_3(V_{SS} - V_T))} \cos(\omega t - \pi) \tag{21}$$

and ø, τ and T are modified respectively as

$$\varnothing' = \frac{2k\alpha\beta_1\beta_2\gamma R_2R_3A_m}{\omega C(R_1 \pm 2k\alpha\beta_2\gamma R_2R_3(V_{SS} - V_T))^2}, \tag{22}$$

where

$$\tau' = \frac{\pi C(R_1 \pm 2k\alpha\beta_2\gamma R_2R_3(V_{SS} - V_T))^2}{k\alpha\beta_1\beta_2\gamma R_2R_3A_m} \text{ and}$$
$$T' = \frac{\pi C \varnothing (R_1 \pm 2k\alpha\beta_2\gamma R_2R_3(V_{SS} - V_T))^2}{k\alpha\beta_1\beta_2\gamma R_2R_3A_m} \tag{23}$$

Similarly the memristance for the floating type of memristor emulator, is obtained as

$$M''(qc(t)) \approx R_1 \pm 2k\alpha\beta_3\gamma\mu_{23}R_2R_3(V_{SS} - V_T) \pm \frac{2k\alpha\beta_1\beta_3\gamma\mu_{23}R_2R_3A_m}{\omega C(R_1 \pm 2k\alpha\beta_1\gamma R_2R_3(V_{SS} - V_T))} \cos(\omega t - \pi) \tag{24}$$

and ø, τ and T are modified respectively as

$$\varnothing'' = \frac{2k\alpha\beta_1\beta_3\gamma\mu_{23}R_2R_3A_m}{\omega C(R_1 \pm 2k\alpha\beta_3\gamma\mu_{23}R_2R_3(V_{SS} - V_T))^2}, \tag{25}$$

$$\tau'' = \frac{\pi C(R_1 \pm 2k\alpha\beta_3\gamma\mu_{23}R_2R_3(V_{SS} - V_T))^2}{k\alpha\beta_1\beta_3\gamma\mu_{23}R_2R_3A_m} \text{ and}$$
$$T'' = \frac{\pi C \varnothing (R_1 \pm 2k\alpha\beta_3\gamma\mu_{23}R_2R_3(V_{SS} - V_T))^2}{k\alpha\beta_1\beta_3\gamma\mu_{23}R_2R_3A_m} \tag{26}$$

3. Simulation results

In order to show the fundamental characteristics of memristor, PSPICE simulation of the proposed emulator circuit has been performed. The simulation has been performed using 0.25 μm TSMC CMOS technology with an aspect ratio of various transistors as shown in

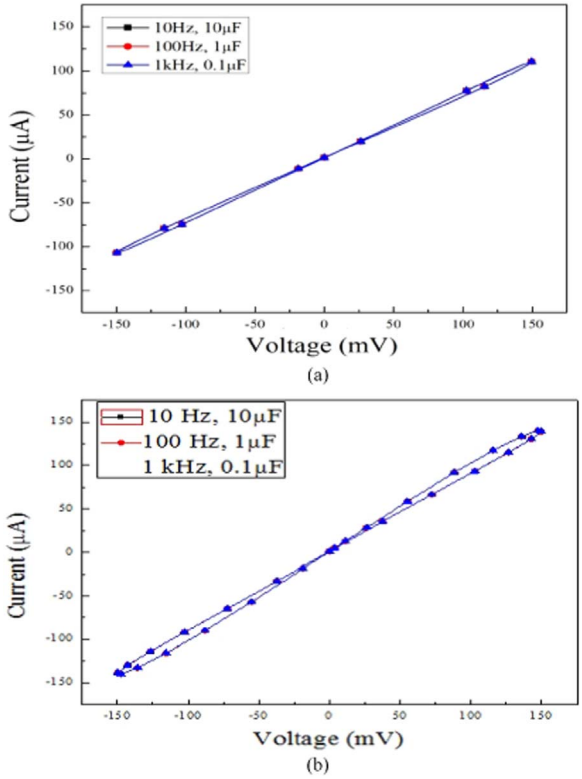

Fig. 6. Comparing Frequency dependent pinched hysteresis loop operating at low frequencies 10 Hz, 100 Hz and 1 kHz with constant ωC and $A_m = 150$ mV: (a) Incremental topology: (b) decremental topology.

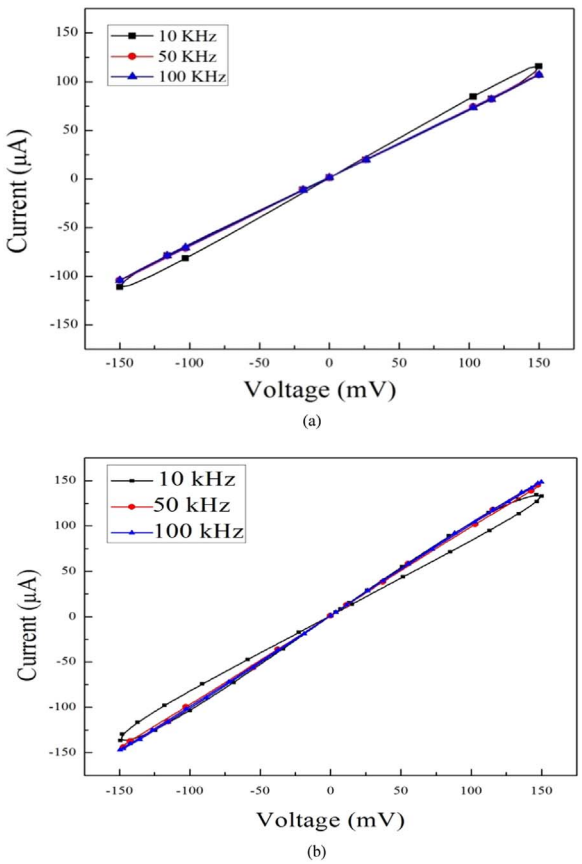

Fig. 7. Comparing frequency dependent pinched hysteresis loop operating at different frequencies (10 kHz, 50 kHz and 100 kHz) for C = 5 nF, $A_m = 150$ mV (a) incremental topology: (b) decremental topology.

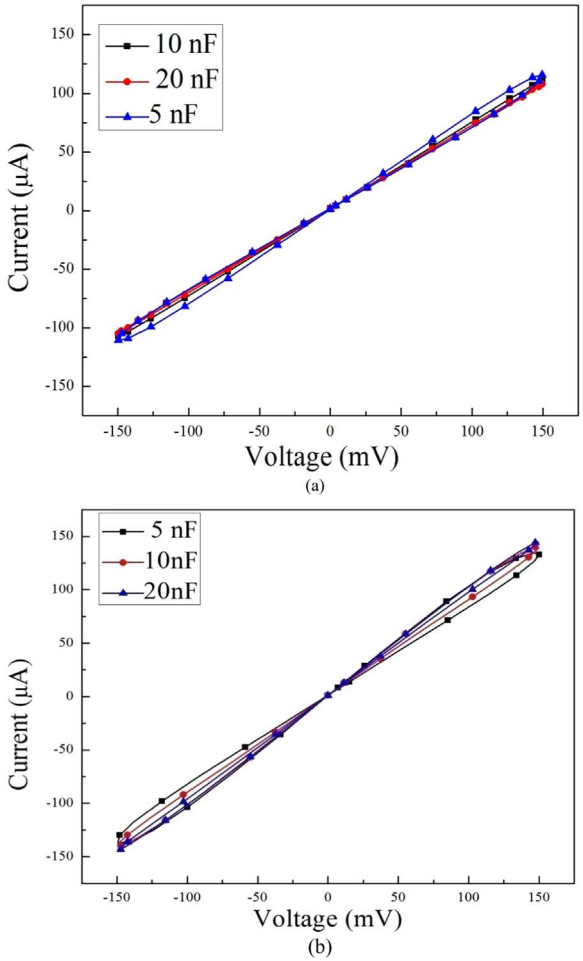

Fig. 8. Comparing Frequency dependent pinched hysteresis loop operating at a frequency of 10 kHz with different capacitor values (5 nF,10 nF and 20 nF) for: (a) incremental topology: (b) decremental topology.

Table 1. It is seen in (17) that if the amplitude of applied signal as well as the product of frequency and capacitor value are constant, then there should be no change in the memristance value. Fig. 6(a) and Fig. 6(b) show respectively the pinched hysteresis loops for incremental and decremental type of memristor keeping the product of frequency and capacitor value to be constant with $A_m = 150$ mV, $R_1 = 1.2$ kΩ, $R_2 = 100$ Ω and $R_3 = 2$ kΩ and operates at different frequencies of 10 Hz, 100 Hz and 1 kHz. The overlapping of pinched hysteresis loops validates the theory.

Fig. 7(a) and Fig. 7(b) show pinched hysteresis loops for incremental and decremental type of memristor at different frequencies (i.e. 10 kHz, 50 kHz and 100 kHz), while keeping capacitance C = 5 nF and amplitude of the applied signal $A_m = 150$ mV constant. The value of resistances are chosen as $R_1 = 1.2$ kΩ, $R_2 = 100$ Ω and $R_3 = 2$kΩ. As with an increment of frequency, the time varying part of (17) will decrease and consequently memristance will convert to linear resistance at higher operating frequency. It can be seen in Fig. 7(a) and Fig. 7(b) that, by increasing the operating frequency up to f = 100 kHz, memristance is dominated by linear time –invariant part.

It is clearly seen in (17) that by scaling down the capacitor value, the pinched hysteresis loop behaviour of both topologies can be pushed for operating at higher frequencies. Fig. 8(a) and Fig. 8(b) show the pinched hysteresis loop behaviour of both topologies for operating signal of amplitude $A_m = 150$ mV at 10 kHz frequency, which is built with components of $R_1 = 1.2$ kΩ, $R_2 = 100$ Ω, $R_3 = 2$ kΩ and different capacitor values (5 nF, 10 nF and 20 nF). By increasing the capacitor

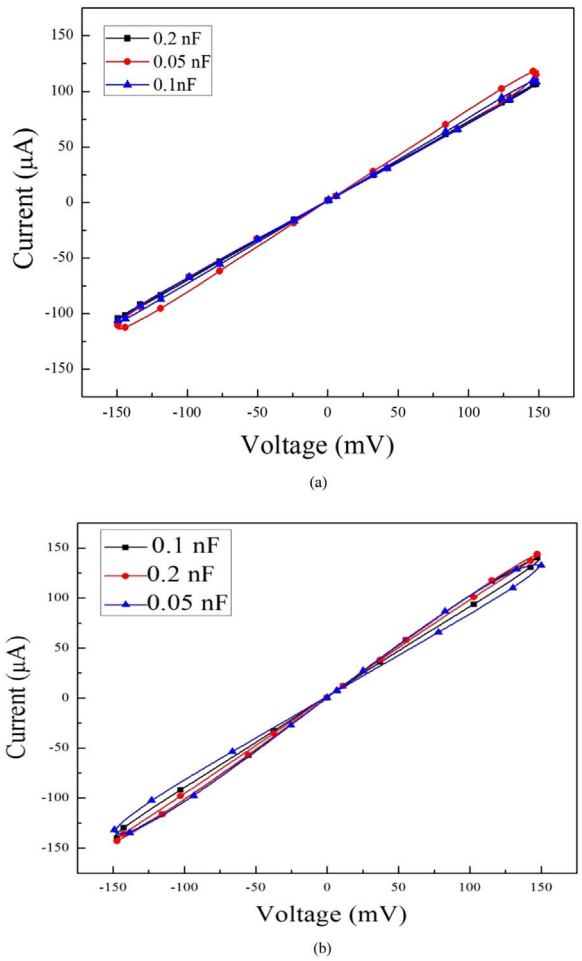

Fig. 9. Comparing Frequency dependent pinched hysteresis loop operating at a frequency of 1 MHz and amplitude (A_m) of 150 mV with different capacitor values (0.05 nF,0.1 nF and 0.2 nF) for: (a) incremental topology: (b) decremental topology.

value until C = 20 nF, the pinched hysteresis loops for both topologies due to linear time-variant resistor are obtained. Hence, the memristor behaviour becomes that of a linear time-invariant resistor when the capacitor value is monotonically increased. Similarly, Fig. 9(a) and Fig. 9(b) show the pinched hysteresis loop behaviour of both topologies for signal of amplitude $A_m = 150$ mV operating at 1 MHz frequency, which is built with components as $R_1 = 1.2$ kΩ, $R_2 = 100$ Ω, $R_3 = 2$ kΩ and with different capacitor values (0.1 nF, 0.2 nF and 0.05 nF).

Further to show digital behaviour, circuit is simulated with $A_m = 150$ mV, $R_1 = 100$ Ω, $R_2 = 5$ kΩ, $R_3 = 2$ kΩ, C = 1 nF; $A_m = 150$ mV $R_1 = 130$ Ω, $R_2 = 4$ kΩ, $R_3 = 2.5$ kΩ, C = 1 nF and $A_m = 200$ mV, $R_1 = 100$ Ω, $R_2 = 5$ kΩ, $R_3 = 2$ kΩ, C = 1 nF for 10 kHz frequency. Simulation results are shown in Fig. 10. Two sharp lines in pinched hysteresis loop correspond to minimum (R_{on}) and maximum (R_{off}) resistance values provided by memristor emulator. Resistance ratios of maximum and minimum values obtained from Fig. 10(a), (b) and (c) are 62, 50 and 59 respectively. These values are incidentally found to be close to thin film TiO_2 memristor [5].

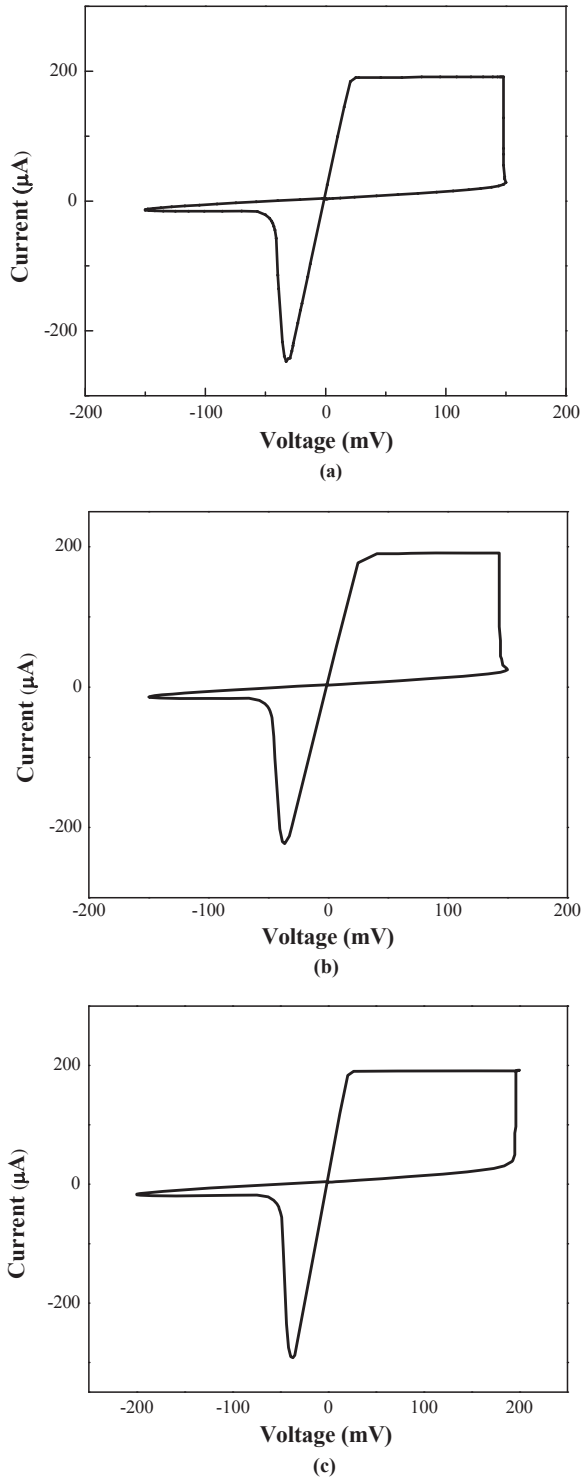

Fig. 10. Pinched hysteresis loop showing bi-stable nature of resistance of memristor at 10 kHz frequency with (a) $A_m = 150$ mV, $R_1 = 100$ Ω, $R_2 = 5$ kΩ, $R_3 = 2$ kΩ, C = 1 nF (b) $A_m = 150$ mV $R_1 = 130$ Ω, $R_2 = 4$ kΩ, $R_3 = 2.5$ kΩ, C = 1 nF (c) $A_m = 200$ mV, $R_1 = 100$ Ω, $R_2 = 5$ kΩ, $R_3 =$ kΩ, C = 1 nF.

4. Comparison

The performance of the proposed memristor emulator circuit has been compared with the existing literature in Table 3. It may be noticed that.

- [20,23,28–35] use excessive number of active building blocks in comparison to the proposed work.
- [28–31,33,34] use excessive number of passive elements.
- Both grounded and floating types of memristor are not available together in any circuit except proposed one.
- Both incremental and decremental types of memristors are available in the proposed one as that of [20,23,28,29,31,34,35].
- Proposed memristor uses only one type of active building block;

Table 3
Comparison of memristor emulator circuit.

Ref.	No.and type of active components used	No. of passive Elements	One kind of Active element	SIM/Exp	Tech. used	Floating/ Grounded Type	Incremental/ decremental Type	Max. Frequency of operation
[20]	10 MOS 1 multiplier 2 op-amp	1 capacitor, 2 resistors, 1 switch	No	Both	CMOS	Floating	Both	few kHz
[23]	1 DDCC, 1 multiplier	1capacitor, 2 resistors	No	SIM	CMOS	Floating	Both	1 MHz
[28]	3 CCII, 1 diode	2 capacitors, 4 resistors	No	Exp	BJT	Grounded	Both	few kHz
[29]	3 CCII, 1 multiplier 1 buffer	1 capacitor, 5 resistors	No	Both	BJT	Grounded	Both	few kHz
[30]	2 CCII, 1 multiplier 2 op-amp	1 capacitor, 7 resistors	No	Both	BJT	Floating	–	few Hz
[31]	4 CCII, 1 multiplier, 1 op-amp	1 capacitor, 8 resistors	No	Both	BJT	Floating	Both	few Hz
[32]	2 CFOA, 1 OTA	1 capacitor, 3 resistors	No	Both	BJT	Grounded	Incremental	2 kHz
[33]	4 CCII 2 diodes	4 capacitors, 4 resistors	No	Exp	BJT	Floating	Incremental	In KHz
[34]	4 ADD844 1 multiplier	1capacitor, 5 resistors	No	Both	BJT	Floating	Both	20.2 kHz
[35]	2 CCII, 1 multiplier	1 capacitor 2 resistors	No	Both	BJT	Floating	Both	160 kHz
Proposed Circuit	1 CCTA	1 capacitor, 3 resistors	Yes	Both	Both	Both	Both	10 MHz

hence suitable for implementation.

- Highest frequency of operation is few Hz range in [30,31], few KHz range in [20,28,29,32–35] and few MHz range in [23, proposed work].

5. Experimental observations

In order to verify the performance of the proposed memristor emulator experimentally, a prototype of the circuit is constructed using commercially available ICs; CFOA (AD 844AN) and OTA (CA 3080). Fig. 11 shows schematic of the circuit. Fig. 11(a) shows the implementation of CCTA while Fig. 11(b) is the proposed memristor. The implementation of terminals ± O is achieved by a scheme of connection of switches (S_1 and S_2) to ± terminals of CA 3080. When S_1 is connected to + and S_2 to -, then output terminal of CA 3080 functions as +O and we get incremental memristor. However, when switches are reversed then the output terminal of CA 3080 functions as –O and the memristor behaves as decremental type. Fig. 12(a) and (b) are the prototype of emulator circuit and its layout using commercially available ICs; AD844 AN and CA 3080. Table 4 shows the parameters and components used. The pinched hysteresis loops obtained for the operating frequencies (5.16 kHz and 30.4 kHz) are shown in Fig. 13. It is clearly seen that hysteresis loops show not only asymmetrical behaviour, but also the area enclosed in the second and fourth quadrant are unequal at two frequencies. It is found in (17), Fig. 8 and Fig. 9 that by down scaling the capacitor value, the operation of the emulator may be pushed to higher frequencies. However, because of limitations on the bandwidth and slew rate of BJT based ICs (AD844 AN and CA 3080) the operating frequencies of the memristor emulator circuit on printed circuit board is in the range of few hundreds of kHz only.

6. Application

6.1. Amplitude modulation of FM signal and demodulation

An important application of proposed memristor emulator circuit is the conversion of Frequency modulation (FM) to Amplitude modulation (AM) [33]. The frequency dependent memristance can be used here to convert FM to AM as shown in Fig. 14(a). The resistance (R_M) of the memristor is dependent on frequency and amplitude of the signal and capacitor value, therefore the gain of the circuit will be dependent on the frequency and amplitude of the input signal and value of the capacitor. At the input an FM signal is applied, and expected that an AM signal will be at the output (V_{AFM}). An inverting amplifier has been used to take the advantage of amplification of output signal. The gain of the inverting amplifier may be written as

$$G = -\frac{R_1}{R_M} \tag{27}$$

Fig. 14(b) shows the circuit for amplitude modulation of FM signal and AM demodulation, which contains envelope detector followed by second order Butterworth low pass filter.

The circuit is simulated using the FM signal, as shown in Fig. 15, of a carrier frequency of 2 kHz, modulating frequency 100 Hz and modulation index 9. The parameters used for the proposed circuit are shown in Table 5. The amplitude modulated FM signal (V_{AFM}) is shown in Fig. 16. Fig. 17 shows the envelope detector output (V_{ED}). Fig. 18 show the extracted modulating signal (V_{out}) of 100 Hz. It verifies that memristor responds to frequency variation as per the theory discussed in Section 2.3.

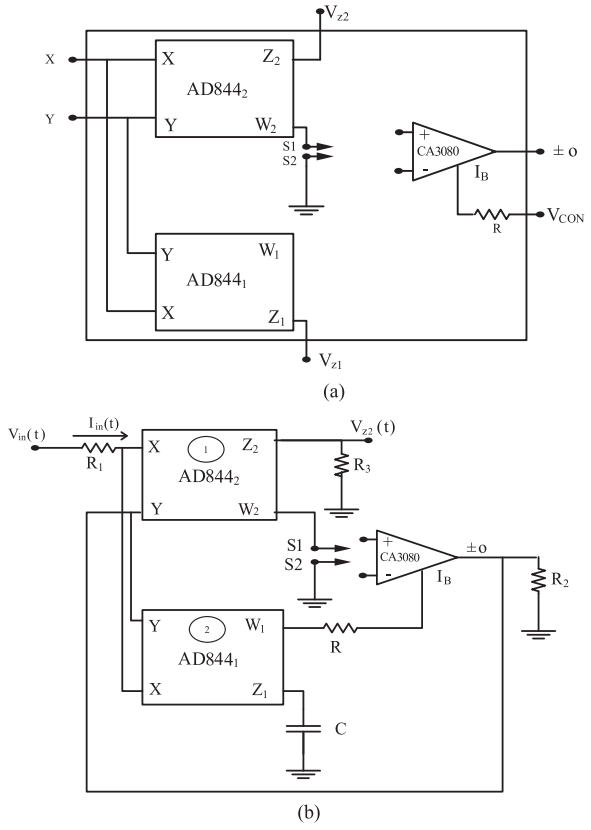

Fig. 11. Practical circuit implementation using commercially available ICs; AD844 and CA 3080 (a) CCTA (b) Incremental/decremental type memristor emulator.

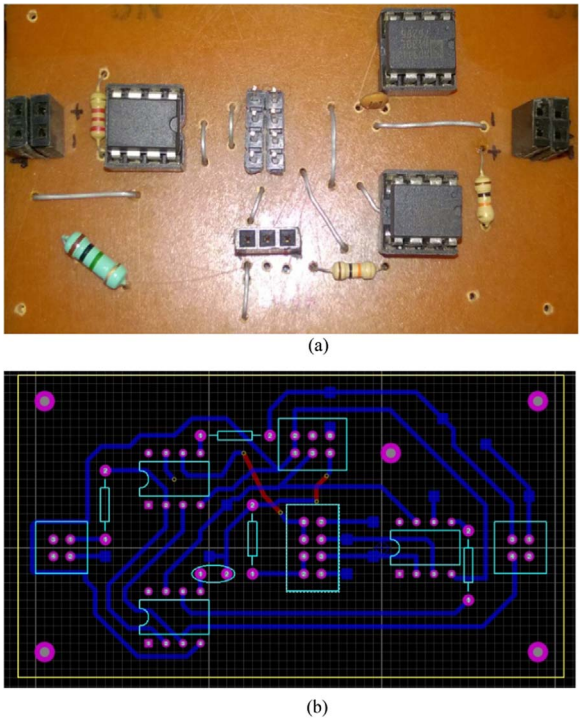

Fig. 12. Prototype of memristor emulator using AD844 and CA3080 (a) Top view of PCB showing components (b) Bottom view (Layout) of PCB.

7. Conclusion

The proposed memristor emulator circuit acting as a real memristor device has simple circuitry built with a single active element and four passive elements (for incremental or decremental type). The proposed emulator circuit can operate at high frequency up to several MHz range. The results of PSPICE simulation are obtained, which is in well agreement with the theoretical expectation. The PSPICE simulation results indicate that the pinched hysteresis loop can be controlled by amplitude and frequency of the input signal and the value of passive components. The experimental verification has also been done using commercially avail-

Table 4
Parameters and components used.

Element	Values
Power Supply	± 10 V
Amplitude (A_m) of input signal	4 V
OTA	CA3080
CCII +	AD844AN
R1,R2	10 kΩ ± 5%
R3	2.2 kΩ ± 5%
R4	1 MΩ ± 5%
C	10 nF ± 20% (for 5.16 kHz) 10 pF ± 20% (for 30.4 kHz)

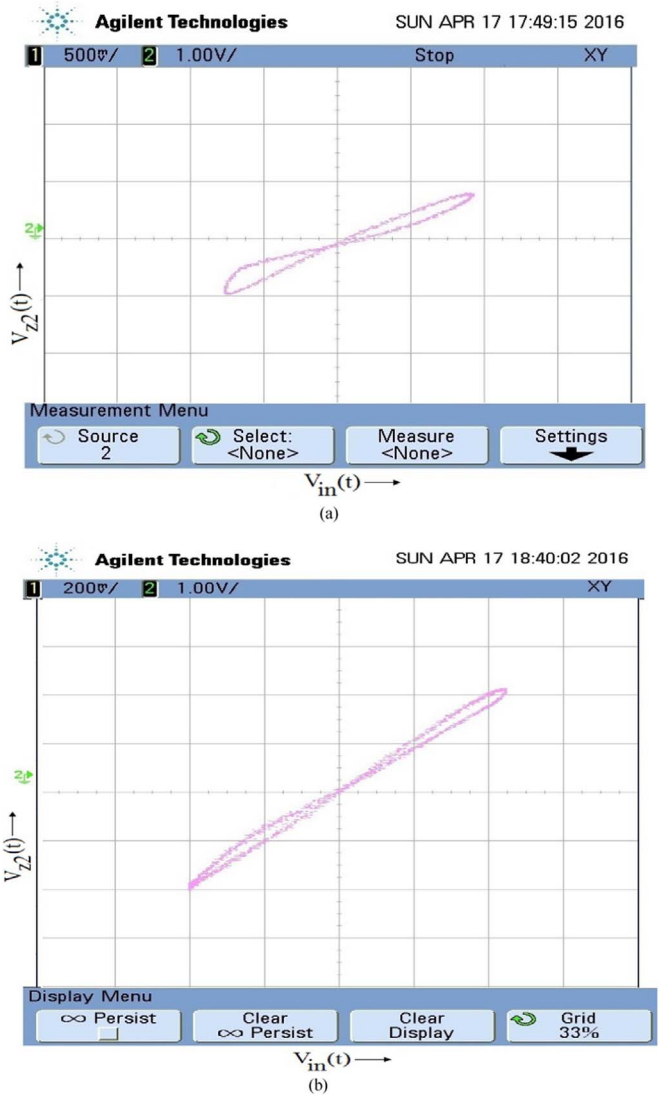

Fig. 13. Experimental results of the frequency-dependent pinched hysteresis loop for the incremental emulator topology operating at: (a) 5.16 kHz, (b) 30.4 kHz.

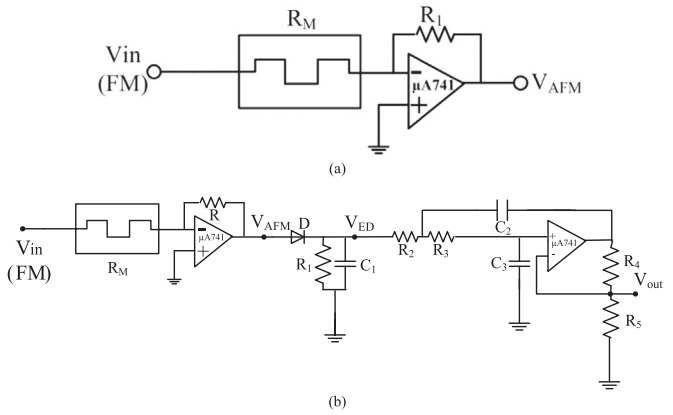

Fig. 14. (a) Amplitude modulation of FM (b) FM to AM and demodulation using a floating memristor emulator.

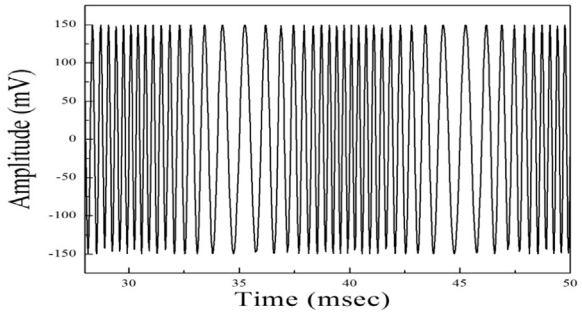

Fig. 15. The FM input signal.

Table 5
Parameters used for AM to FM and demodulation.

Parameters	Values
Power Supply	± 15 V
R, R_1, R_2, R_3, R_4, R_5	10 k, 10 k,10 k, 10 k, 1 k,1 k
C_1, C_2, C_3	500 nF, 100 nF, 100 nF
D	Germinum diode

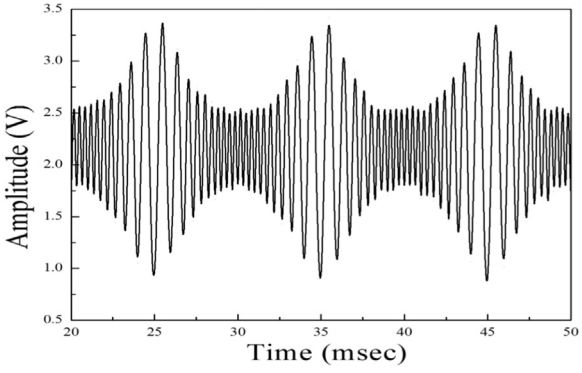

Fig. 16. The amplitude modulated FM signal (V_{AFM}).

able ICs. The test result shows that the proposed memristor emulator circuit works properly. Moreover, as an application, an FM to AM convertor has been realized using the proposed memristor emulator circuit. It confirms the functionality of the circuit. The simulation and experimental results matched nicely with the theoretical proposition.

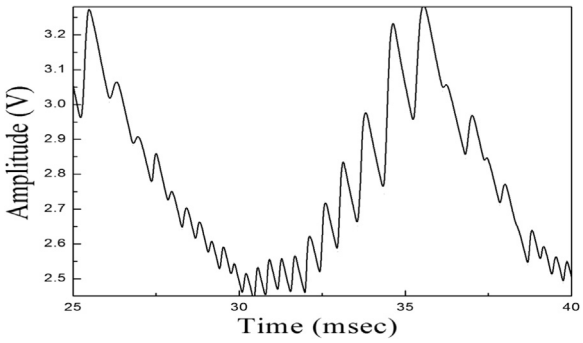

Fig. 17. The envelope detector output signal (V_{ED}).

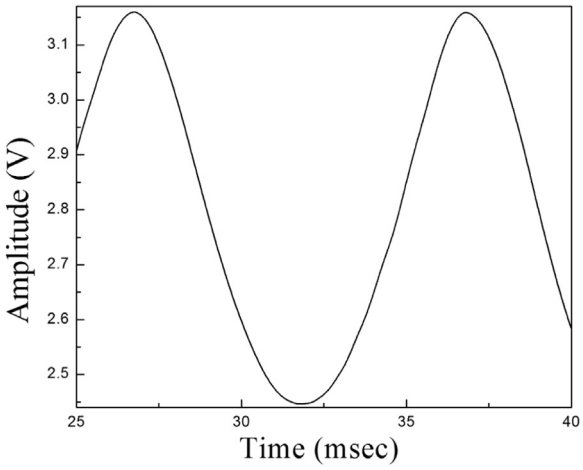

Fig. 18. The recovered modulating signal at the output of low pass filter.

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