

High-frequency floating memristor emulator and its experimental results

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Abstract: In this study, a high-frequency floating-type memristor emulator has been presented. The proposed emulator circuit uses a current conveyor transconductance amplifier, second generation current conveyor, three resistors and a grounded capacitor. The presented floating-type memristor can be configured in both incremental and decremental configurations and performs well up to 5 MHz. The equivalent memristor equation is verified by theoretical analysis of the proposed circuit which also includes non-ideal analysis. The theoretical proposition has been verified through personal simulation program with integrated circuit emphasis simulations using TSMC 0.25 μm complementary metal oxide semiconductor technology parameters. Moreover, non-volatility and Monte Carlo simulation have been performed to check the robustness of the circuit. The effectiveness of the presented memristor emulator design has been verified by printed circuit board prototype using commonly available integrated circuits AD844 and CA3080. The experimental results are included, which show good agreement with the theoretical and simulation results. To test the functionalities of the proposed designs, their applications as parallel and serial combinations, high-pass filter and Chua's oscillator have been presented.

1 Introduction

In 1971, Chua [1] suggested the theoretical missing fundamental element which defines the relationship between magnetic flux and charge on the basis of symmetry. After five years, Chua and Kang [2] published a paper which defined a broader class called memristive systems to introduce four basic elements of a circuit. In [3], the basic characteristics of a circuit to mimic like a memristor are explained. In 2008, Williams and co-authors [4] fabricated the first working solid-state nanoscale memristor in HP Laboratory. It consists of a thin film of titanium dioxide (TiO_2) having two different layers, grown in between platinum electrodes. One of the layers has missing oxygen called oxygen-deficient layer which behaves as a conductor while the other is undoped or pure TiO_2 which acts as an insulator. Its resistance keeps increasing or decreasing according to the magnitude and polarity of the voltage applied across the terminal, this exhibits memristive behaviour and thus cemented its place as the fourth circuit element.

Memristive systems are nonlinear passive elements with memory. Modification of its resistance depends upon the charge flowing through the circuit. Its value is retained when there is no flow of charge or no input is applied, which makes like a nonlinear resistor with memory. This two-port passive element shows the characteristic of a pinched hysteresis loop between the current and voltage plane under periodic sinusoidal input. The area under pinched hysteresis loop is inversely proportional to the applied input frequency. It acts as a linear resistor at high frequency, which is an important fingerprint of the memristor. The memristive systems and generalised mathematical model have been discussed in [5, 6]. Owing to its unique properties, such as nonlinear, non-volatility, high-data storage, low power and endurance, it is suitable for many applications such as oscillator design [7–9], Chua's oscillator circuits [10, 11], neuromorphic networks [12–14], image processing [15], analogue and digital programmable circuits [16, 17]. Its compatibility with conventional complementary metal oxide semiconductor (CMOS) technology has attracted the attention of many researchers to further explore its application.

Nanoscale memristors have high-fabrication cost and technical difficulties in production, however, memristor emulators are simple to design and their properties can be controlled. Several simple simulation program with integrated circuit emphasis models/emulators [18–21] have been proposed to mimic the behaviour of the memristor but they are only for simulation purpose and several memristor emulator circuits have been proposed for the real-world application [11–17]. The circuits presented in [9, 22–27] are floating-type memristors having various active elements such as second generation current conveyor (CCII) [9, 22], operational amplifier (Op-amp) [23], multiplier and Op-amp [24], operational transconductance amplifier (OTA) in [25], all the above proposed design consists of more number of active and passive components. In [26], the memristance value is electronically controllable but it consists of three OTAs and four CCIs. In [27], four CCIs (AD844) and two diodes have been used to design a memristor. Series and parallel combinations of memristor circuits and their application are given in [28]. In [16, 29–33], grounded-type memristor emulator circuits having a large number of passive components have been designed. The proposed circuits [29] have the advantage of high speed but these circuits cannot perform well at higher frequencies. In [30], a current control memristor emulator is designed with two CCIs, one buffer, and one multiplier. The circuit proposed in [16] utilises a microprocessor, an analogue-to-digital converter, and a potentiometer but its performance is restricted to finite resolution. The models proposed in [31, 32] have a current feedback operational amplifier as the basic active elements and are not electronically controllable. CMOS-based charge control grounded memristor emulator design using a single differential voltage current conveyor transconductance amplifier (DVCCTA) block is presented in [33]. Grounded type circuits are complex, more effects of stray currents and parasitic than the floating-type design. In [34], the memristance and operating frequency can be adjusted by selecting corresponding values of passive elements. In [35], the incremental floating emulator is proposed having four CCIs, one multiplier, three resistances, and one capacitor. In [36], the memristor emulator circuit operates up to 150 kHz but requires ten active blocks and 14 passive elements.

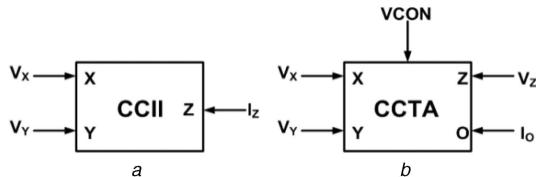


Fig. 1 Symbols of
(a) CCII, (b) CCTA

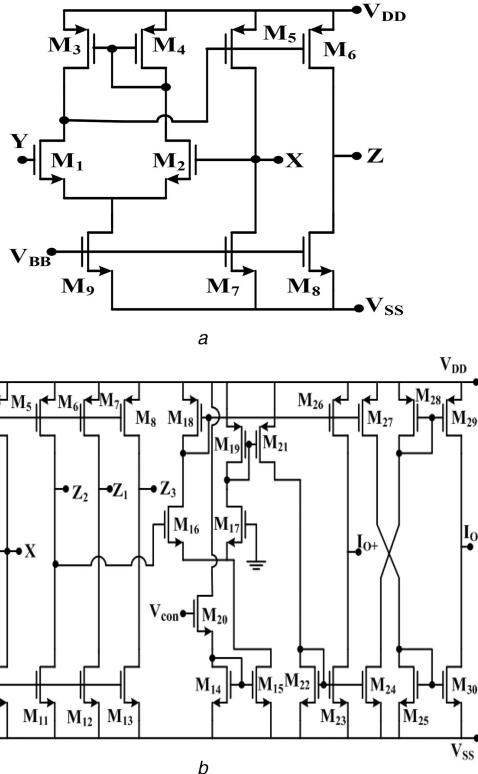


Fig. 2 CMOS implementation of
(a)CCII, (b) CCTA

Table 1 Aspect ratio of MOSFETs

	W/L, μm
CCTA	
M_1, M_4	5/0.5
M_2, M_9	10/0.5
M_3	28/0.5
M_5-M_8	8.5/0.5
$M_{10}-M_{13}$	44/0.5
$M_{14}-M_{30}$	15/0.5
CCII	
M_1, M_9	10/0.5
M_2	27/0.5
M_3, M_4	5/0.5
M_5, M_6	8.5/0.5
M_7, M_8	44/0.5

In [37], a single differential difference current conveyor (DDCC) and a multiplier as an active block have been used. It performs well up to 1 MHz in both incremental and decremental configurations. Recently, a floating/grounded-type memristor emulator [38] has been designed using CCTA as an active element along with a few passive elements.

In this study, a charge control floating-type memristor emulator is designed using one CCTA, one CCII, three resistors, and one grounded capacitor. Since the design is a floating type, it can be

used for complex circuits and has less effect of parasitic. The frequency and amplitude of the applied voltage across emulator can be used as control parameters in order to adjust memristance. It performs well up to 5 MHz, so it can be used in a high-frequency oscillator, Chua's circuits, neuromorphic networks, high speed of logical circuits etc. Two active elements (CMOS-based CCII and CCTA) make the design a bit complex when compared to the nano-scale memristor. However, the proposed emulator design is simple and has wide application. The circuit can also be practically implemented and tested using commercially available bipolar junction transistor (BJT)-based ICs AD844 and CA3080.

2 Building blocks and their properties

Current mode circuits have many advantages over voltage mode circuits such as higher bandwidth, more dynamic range, less power consumption, less chip area, and more linearity. In this design, CCII and CCTA are used as an active building block.

The CCII is the second version of the current conveyor in which no current flows into the Y terminal. The block diagram of the CCII is shown in Fig. 1a. The port relationships of the CCII are defined as

$$I_Y = 0, V_X = V_Y, I_Z = I_X. \quad (1)$$

The circuit symbol of the CCTA is shown in Fig. 1b, which is a combination of a CCII and an OTA, and contains all the advantages of both the circuits. Here, transconductance (g_m) is controlled by a control voltage (V_{con}) instead of biasing current (I_B). The port relationships of the CCII are expressed as

$$I_Y = 0, V_X = V_Y, I_Z = I_X, I_0 = \pm g_m V_Z. \quad (2)$$

The internal CMOS implementation of CCII and CCTA is shown in Fig. 2a and b, respectively. The relationship between transconductance (g_m) and (V_{con}) is given as

$$g_m = k \{(V_{con} - V_{ss})/2 - V_{th}\}, \quad (3)$$

where k is a constant and given by

$$k = \mu C_{ox} \frac{W}{L}, \quad (4)$$

Here, W/L is the aspect ratio of the metal oxide semiconductor field effect transistors (MOSFETs), μ is the mobility of the carrier in the channel, $C_{ox} = 6.16 \times 10^{-3} \text{ F/m}^2$ is oxide capacitance. Threshold voltages of N-type MOS and P-type MOS are 0.423 and -0.553 V , respectively. The functionality of CCII and CCTA is verified through PSpice simulation, using TSMC 0.25 μm CMOS technology. Biasing voltages of the proposed circuit are $V_{DD} = 1.5 \text{ V}$ and $V_{ss} = -1.5 \text{ V}$. The aspect ratio of all the MOSFETs used in CCII and CCTA are shown in Table 1.

3 Proposed floating memristor emulator circuit

In this section, a floating-type charge controlled memristor emulator circuit is proposed. It consists of one CCII, one CCTA, one capacitor, and three resistors as shown in Fig. 3. The transconductance (g_m) parameter of CCTA is utilised for multiplication purpose. The frequency (f) and peak amplitude (V_m) of the sinusoidal input voltage can be used to change the memristance characteristics.

Ideally, the Y terminal of the CCTA is grounded so that the voltage at the X terminal of CCTA will be zero. Hence, the voltage at the input point A is given as

$$V_A(t) = I_{in}(t)R_1, \quad (5)$$

Using the property of CCII and CCTA given in (1) and (2), current at the Z terminal of CCTA and X terminal of CCII is equal to the current through the X terminal of the CCTA given by

$$I_{in}(t) = I_{Z3}(t) = I_S(t) = I_O(t). \quad (6)$$

Using the property of the CCTA given in (2), V_{Z2} can be written as

$$V_{Z2} = I_{in}(t)R_2. \quad (7)$$

Substituting the value of g_m from (3) and V_{Z2} from (7), output current I_{O-} can be obtained as

$$I_O(t) = \pm k \left(\frac{q_c(t)}{2C} - \frac{V_{SS}}{2} - V_t \right) I_{in}(t) R_2. \quad (8)$$

Using the building block property, the following equation can be obtained

$$V_i(t) = V_2(t) = V_B(t) = \pm k \left(\frac{q_c(t)}{2C} - \frac{V_{SS}}{2} - V_t \right) I_{in}(t) R_2 R_3. \quad (9)$$

Substituting $V_A(t)$ and $V_B(t)$ from (5) and (9), the voltage across the circuit can be obtained as

$$V_A(t) - V_B(t) = I_{in}(t)R_1 \mp k \left(\frac{q_c(t)}{2C} - \frac{V_{SS}}{2} - V_t \right) I_{in}(t) R_2 R_3. \quad (10)$$

Equation (10) can be written as

$$\frac{V_{AB}(t)}{I_{in}(t)} = R_1 \pm k R_2 R_3 \left(\frac{V_{SS}}{2} + V_t \right) \mp k R_2 R_3 \frac{q_c(t)}{2C}. \quad (11)$$

So, the expression of memristance for the presented memristor emulator circuit is given as

$$M_{AB}(q) = R_1 \pm k R_2 R_3 \left(\frac{V_{SS}}{2} + V_t \right) \mp k R_2 R_3 \frac{q_c(t)}{2C}. \quad (12)$$

From (12), it can be seen that memristance of the emulator circuit is dependent upon charge flowing through the circuit. So, it is the charge-controlled memristor emulator. The equation obtained for memristance is similar to the equations mentioned in Kim *et al.* [24], which is similar to the linear ion drift model proposed by HP laboratories.

3.1 Frequency response analysis

The memristance expression in (12) contains linear time invariant and linear time variant resistor. Assuming a sinusoidal voltage, $V_{AB}(t) = V_m \sin 2\pi f t$ is applied across the terminals A and B, where V_m is peak amplitude value and f is the frequency of applied voltage signal across terminal A and B. The average input current can be obtained by equating time varying part of (12) equal to zero, so it can be written as

$$I_{in}(t) = \frac{V_{in}(t)}{R_1 \pm k R_2 R_3 ((V_{SS}/2) + V_t)}. \quad (13)$$

As a result, $q_c(t)$ can be written as

$$q_c(t) = \frac{V_m \cos(2\pi f t - \pi)}{2\pi f (R_1 \pm k R_2 R_3 ((V_{SS}/2) + V_t))}. \quad (14)$$

Substituting (14) into (12), memristance can be calculated as

$$M(q) = \frac{V_{in}(t)}{I_{in}(t)} = R_1 \pm k R_2 R_3 \left(\frac{V_{SS}}{2} + V_t \right) \mp k R_2 R_3 \frac{V_m \cos(2\pi f t - \pi)}{2\pi f C (R_1 \pm k R_2 R_3 ((V_{SS}/2) + V_t))}. \quad (15)$$

From (15), it can be observed that the linear time-variant part of the memristance expression becomes negligible with the increment in

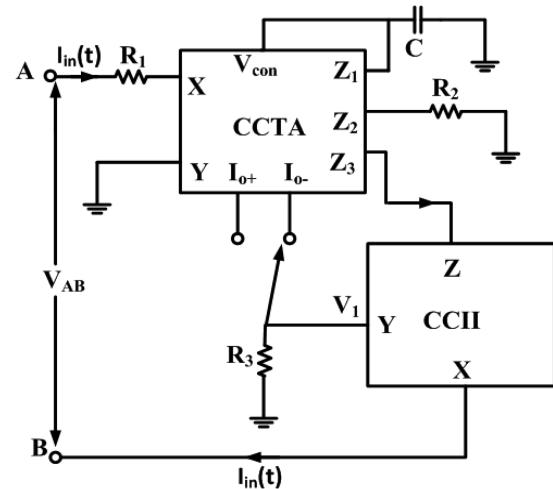


Fig. 3 Proposed floating memristor emulator circuit

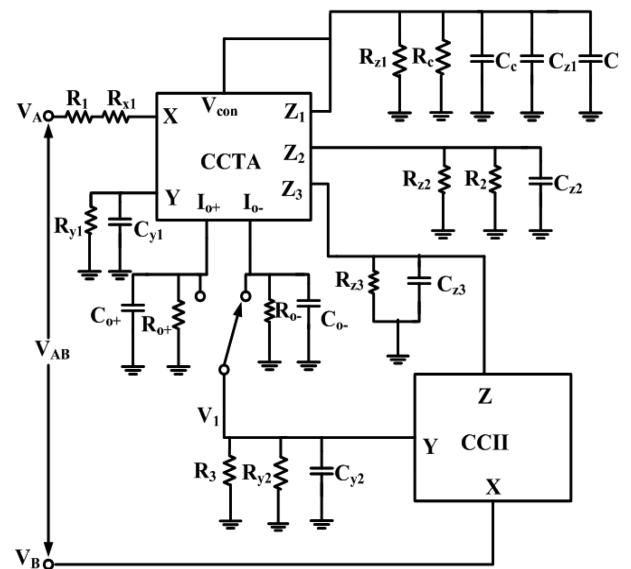


Fig. 4 Proposed memristor emulator circuit with parasitic

frequency. So, a memristor can be considered as a linear resistor independent of time. Hence, the ratio of the linear time variant to the linear time invariant part is given as

$$\phi = \frac{k R_2 R_3 V_m \cos(2\pi f t - \pi)}{2\pi f C (R_1 \pm k R_2 R_3 ((V_{SS}/2) + V_t))^2} = \frac{T}{\tau}, \quad (16)$$

where ' τ ' represents time constant and can be written as

$$\tau = \frac{2\pi C (R_1 \pm k R_2 R_3 ((V_{SS}/2) + V_t))^2}{k R_2 R_3 V_m \cos(2\pi f t - \pi)}. \quad (17)$$

It can be observed that time constant ' τ ' depends upon parameters such as capacitor value and amplitude of applied voltages. The time period (T) of the applied voltage signal is given by

$$T = \frac{1}{f} = \frac{2\pi C \phi (R_1 \pm k R_2 R_3 ((V_{SS}/2) + V_t))^2}{k R_2 R_3 V_m \cos(2\pi f t - \pi)}. \quad (18)$$

From (16), it can be observed that the value of ϕ decreases with an increase in the frequency. To hold pinched hysteresis which is frequency dependent, the time constant τ should be updated as per applied frequency.

3.2 Non-ideal analysis with parasitic

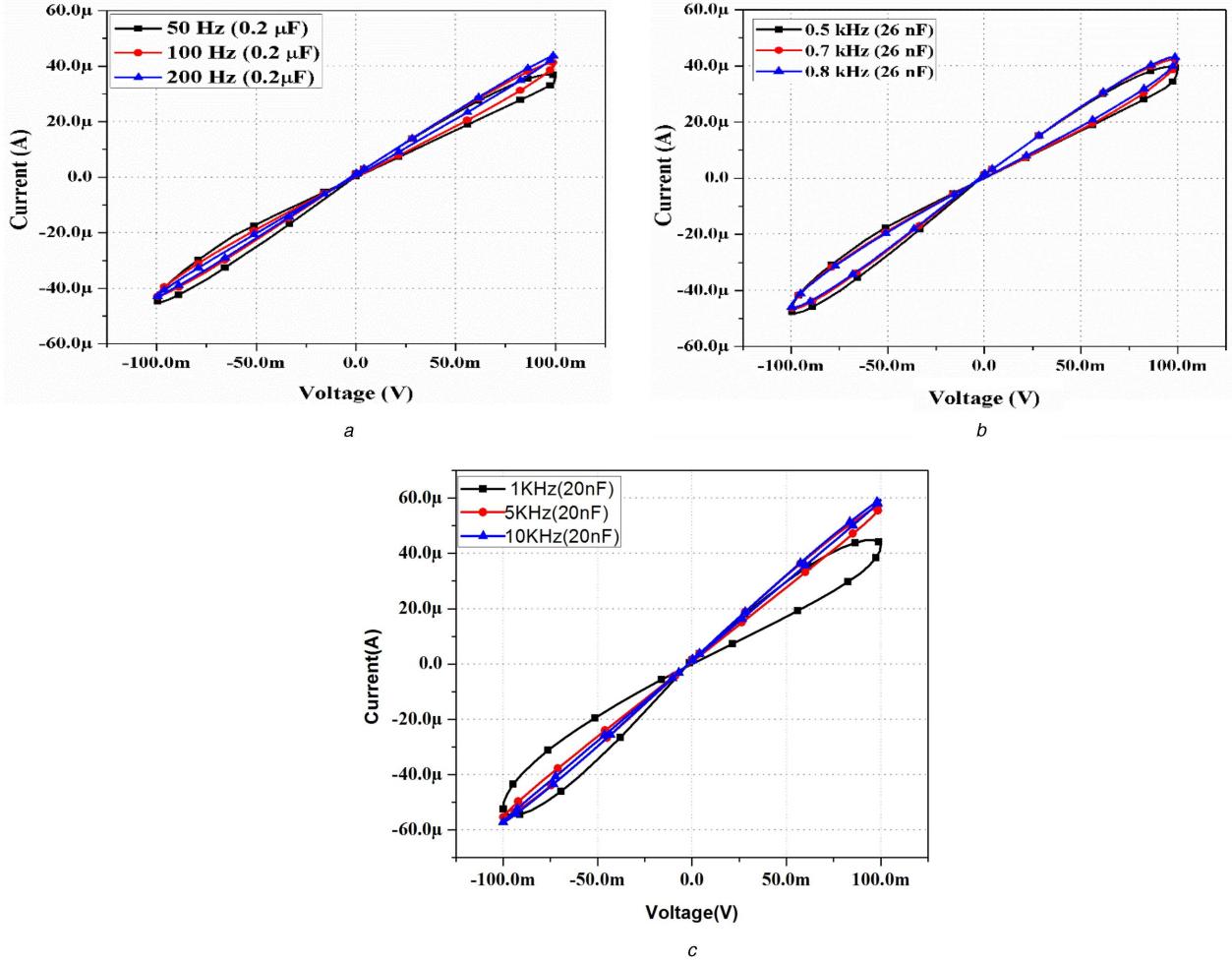


Fig. 5 Comparison of the pinched hysteresis loop in the current voltage plane for

(a) frequencies 50, 100 and 200 Hz at a capacitor value of $0.2 \mu\text{F}$, (b) frequencies 0.5, 0.7 and 0.8 kHz at a capacitor value of 26 nF , (c) frequencies 1, 5 and 10 kHz at a capacitor value of 20 nF

In this section, the effect of non-ideal analysis of the proposed memristor emulator circuit has been discussed which occurs due to a mismatch in the transistors and the effect of parasitic presence in the proposed design is shown in Fig. 4. The modified relationship of voltage and current terminals of CCTA and CCII can be written as

$$I_y = 0, V_x = \alpha V_y, I_{z_i} = \beta_i I_x, I_{0-} = \pm \gamma g_m V_z, \quad (19)$$

where α, β, γ represent the tracking errors of CCTA and CCII. Its ideal value is unity. β_i represents the tracking error of the i th Z-terminal. Also, considering non-ideal effects, the proposed memristor emulator circuit shown in Fig. 3 can be re-analysed as follows:

$$I_{Z_1} = \beta_1 I_x, I_{Z_2} = \beta_2 I_x, I_{Z_3} = \beta_3 I_x, I_{\text{in}} = I_x. \quad (20)$$

$R_{x1}, R_{y1}, R_{y2}, R_{z1}, R_{z2}, R_{z3}, R_{0-}, R_{0+}$ are parasitic resistances and $C_c, C_{y1}, C_{y2}, C_{z1}, C_{z2}, C_{z3}, C_{0-}, C_{0+}$ are parasitic capacitances, shown in Fig. 4. These parasitics will influence the transconductance (g_m), which is expressed as

$$g_m = k \left(\beta_1 \frac{q_c(t)}{2(C + C_c + C_{z1})} - \frac{V_{SS}}{2} - V_t \right). \quad (21)$$

The voltage at point A can be written as

$$V_A(t) = I_{\text{in}}(t)(R_i + R_{xi}). \quad (22)$$

The voltage across Z_2 can be written as

$$V_{z2} = I_{z2}(R_2//R_{z2}//C_{z2}) = \beta_2(R_2//R_{z2}//C_{z2})I_{\text{in}}(t). \quad (23)$$

The output current of CCTA is given as

$$I_O = \pm \gamma g_m \beta_2(R_2//R_{z2}//C_{z2})I_{\text{in}}(t). \quad (24)$$

Using the property of the current building block and considering the non-ideal effect, V_B and V_1 are given as

$$\begin{aligned} V_B(t) &= V_2(t) = \alpha V_1(t), \\ \alpha V_1(t) &= -\gamma \alpha \beta_2 g_m (R_2//R_{z2}//C_{z2})(R_3//R_{y2}//C_{y2})I_{\text{in}}(t). \end{aligned} \quad (25)$$

Substituting the values of g_m , $V_A(t)$ and $V_B(t)$ from (21), (22) and (25), respectively, memristance equation can be obtained as

$$\begin{aligned} M(q) &= R_i + R_x \pm k \alpha \beta_2 \gamma (R_2//R_{z2}//C_{z2})(R_3//R_{y2}//C_{y2}) \left(\frac{V_{SS}}{2} + V_t \right) \\ &\mp k \alpha \beta_1 \beta_2 \gamma (R_2//R_{z2}//C_{z2})(R_3//R_{y2}//C_{y2}) \frac{q_c(t)}{2(C + C_{z1} + C_c)}. \end{aligned} \quad (26)$$

It can be observed that with an increment of frequency, the linear time-variant part of memristance expression becomes negligible. The memristance of the circuit depends upon the tracking errors developed due to non-idealities and parasitic components of the building blocks.

4 Simulation results

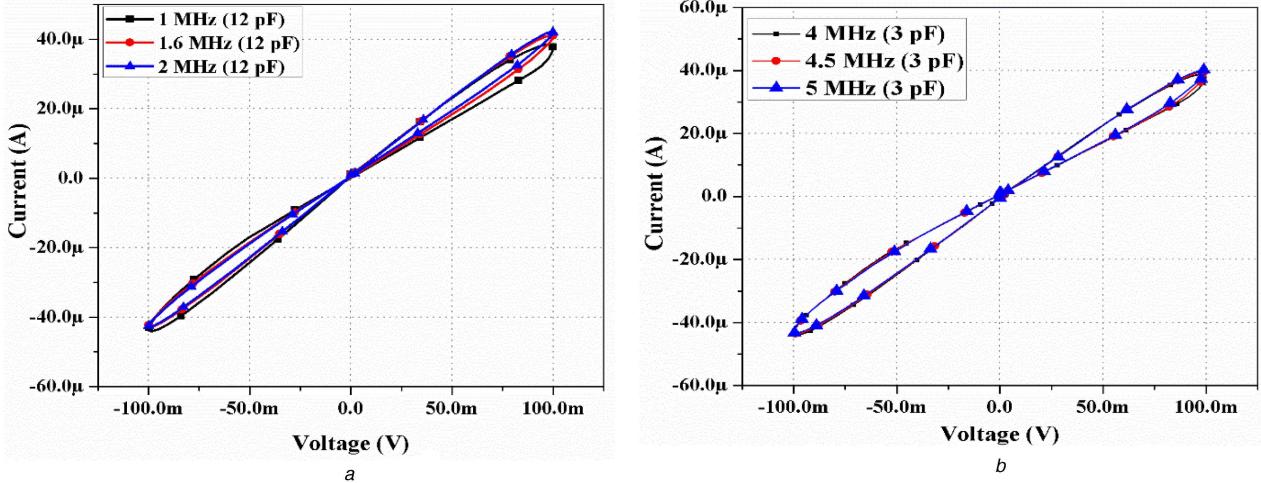


Fig. 6 Comparison of the pinched hysteresis loop in the current voltage plane for

(a) Frequencies 1, 1.6 and 2 MHz at a constant capacitor value of 12 pF, (b) frequencies 4, 4.5, and 5 MHz at a constant capacitor value of 3 pF

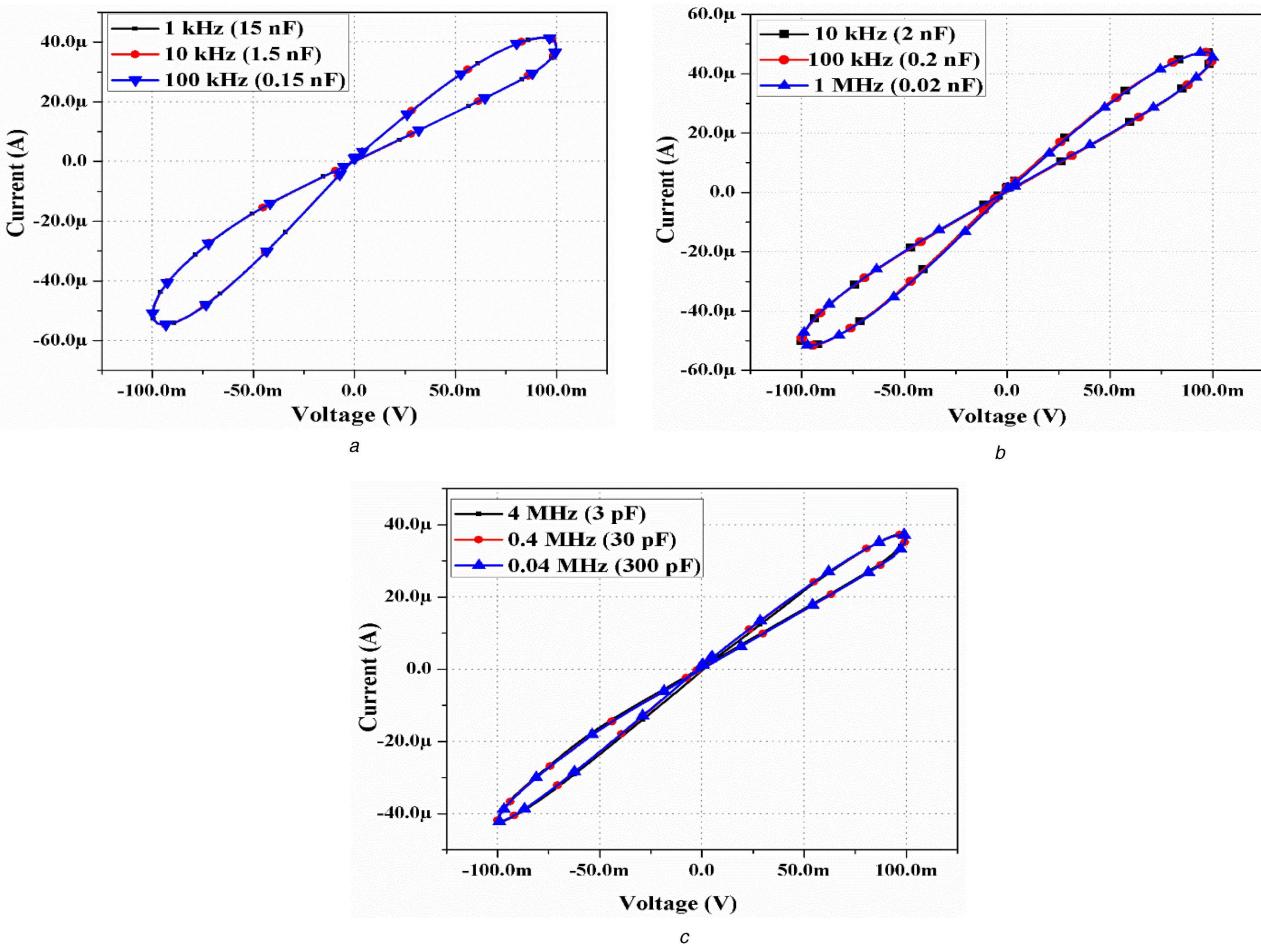


Fig. 7 Hysteresis loop comparison of constant frequency and capacitor product at

(a) 1, 10 and 100 kHz, (b) 10, 100 and 1 MHz, (c) 0.04, 0.4 and 4 MHz

To validate the working of the proposed emulator circuit, which is shown in Fig. 3, the PSPICE simulation has been performed. The CMOS-based CCII and CCTA internal structures have been discussed in Section 2. The values of R_1 , R_2 , and R_3 are frequency dependent and are taken as 2.9, 1.2, and 0.6 k Ω , respectively. It can be observed from Figs. 5 and 6 that if we increase the frequency by taking the value of the capacitor as a constant then the loop area of pinched hysteresis decreases and validates the (15) for decremental configuration. As the value of frequency increases, ϕ reduces, and thus memristor starts to acts as a linear resistor.

Fig. 7 shows the pinched hysteresis loops at different frequencies by keeping frequency and capacitance product

constant. It can be observed that for a constant value of the frequency capacitor product, all the hysteresis curves coincide and look alike because the value of ϕ remains unaltered. This validates the theoretical analysis as stated in (15).

From (16), it can be observed that the area under pinched hysteresis loop decreases as the value of the capacitor increases, thus an increase in the value of the capacitor causes decrease in ϕ , keeping the frequency constant and altering the value of the capacitor as shown in Figs. 8a and b.

For checking the uncertainty and robustness, Monte-Carlo simulation has been carried out for 20 samples at a frequency of 500 kHz as shown in Figs. 9a and b. In Fig. 9a, the tolerance band

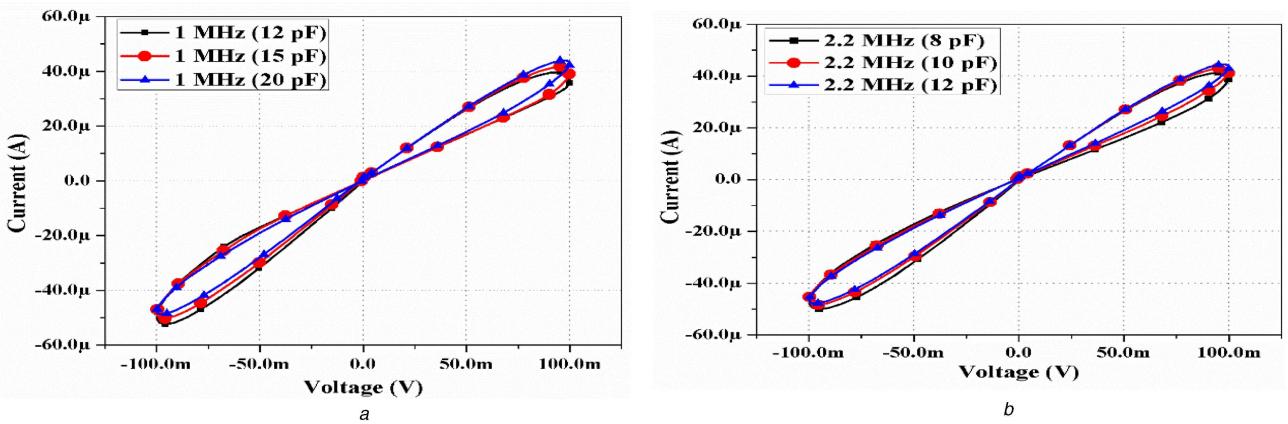


Fig. 8 Hysteresis loop comparison for different values of capacitors at
(a) frequency 1 MHz, (b) frequency 2.2 MHz

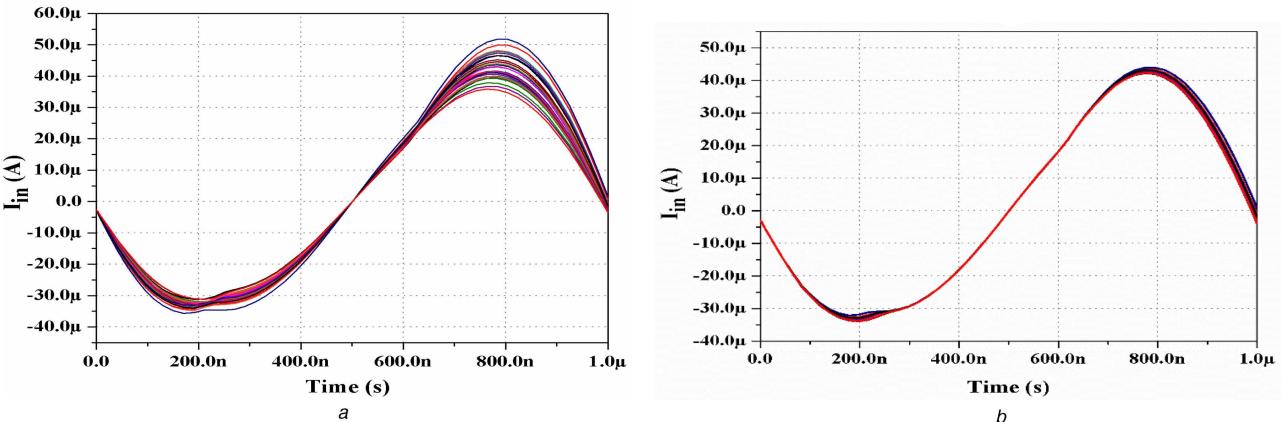


Fig. 9 Monte-Carlo analysis for current through resistance R_1

(a) By varying resistance R_1 , (b) By varying capacitance C_1

of R_1 is taken as 2% and in Fig. 9a tolerance for the capacitor (C_1) is taken as 2%. In Fig. 9a, the amplitude of the current through R_1 varies more while in Fig. 9b it is less due to the fact that the parasitic effect of resistance is more than that of capacitor validating (26).

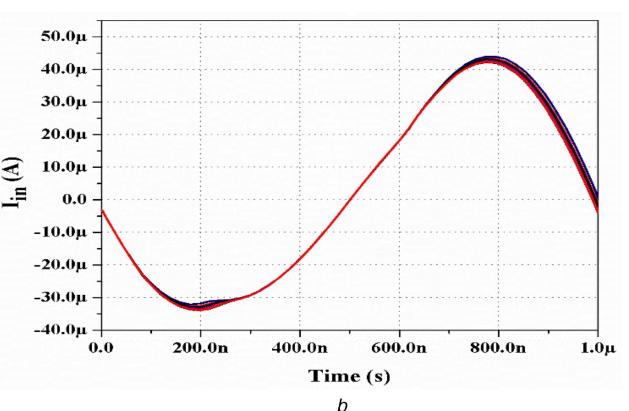
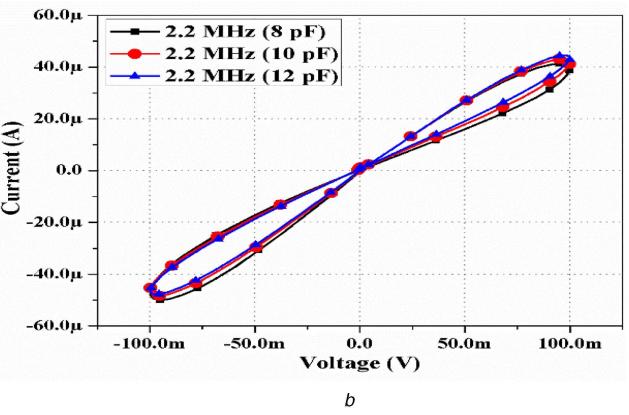
Non-volatility is an important characteristic of the memristor circuit. This characteristic of the memristor can be tested by applying a train of pulses at the input terminal. A pulse signal having a time period of 1 ms, pulse width 1 μ s and amplitude of 1 V is applied in order to verify the non-volatility feature of the presented circuit. Other component values are taken as $R_1 = 2.9$ k Ω , $R_2 = 1.5$ k Ω , $R_3 = 0.6$ k Ω and the capacitance value of $C = 15$ pF. PSpice simulations of both incremental and decremental configurations have been performed. The applied input pulse is shown in Fig. 10a and its corresponding results have been shown in Figs. 10b and c, respectively.

The proposed design shows non-volatility due to the fact that its value remains unaltered in both the topologies when no signal is applied at the input. Since memristance depends on the linear time invariant part as mentioned in (15), the initial values of memristance in both the configurations incremental as well as decremental are different.

5 Comparison

Table 2 shows the comparison between the proposed emulator circuit and the existing literature and it can be observed that

- Maximum frequencies attained by [9, 22–24] are in the range of the Hz range, whereas [25–27, 34–36] are in the kHz range, [37] is up to 1 MHz and proposed design can operate up to 5 MHz.
- The proposed circuit is a floating type. So it can be used between any complex circuits as in [26, 27, 34–37].



- CMOS and BJT technologies are used only in the proposed circuit.
- The authors of [9, 22, 23, 25, 26, 34–36] use more passive elements than the proposed memristor emulator circuit.

6 Integrated circuit (IC)-based floating-type memristor emulator

The IC-based implementation of the proposed memristor emulator circuit is bit complex due to the unavailability of monolithic IC for CCTA and CCII. It restrains us to realise the design using commonly available IC AD844 and CA3080. The IC-based implementation of the circuit is shown in Fig. 11. In this design, four CCIIIs (AD844) and one OTA (CA3080) IC have been used. Since these commercially available ICs (AD844) have only one output for the current, therefore three more CCIIIs (AD844) are required for the proposed circuit. Due to the difference in technology (i.e. BJT and metal oxide semiconductor (MOS)) values such as transconductance (g_m), supply voltages and other parameters such as temperature dependence, slew rate are different for both the technologies. Numerical values of parameter and components required for macromodel implementation are mentioned in Table 3. It has been observed from the macromodel implementation of the emulator circuit that the pinched hysteresis loop has been dominated by the time-invariant part which henceforth confirms the theory.

7 Simulation results of the IC-based circuit

The PSpice simulation of the IC-based proposed emulator circuit as shown in Fig. 11 was performed to validate its theoretical analysis. For a circuit to behave like a memristor, it must satisfy its fingerprint characteristics. Fig. 12 shows the pinched hysteresis loop obtained for an applied periodic signal at frequencies 1 and

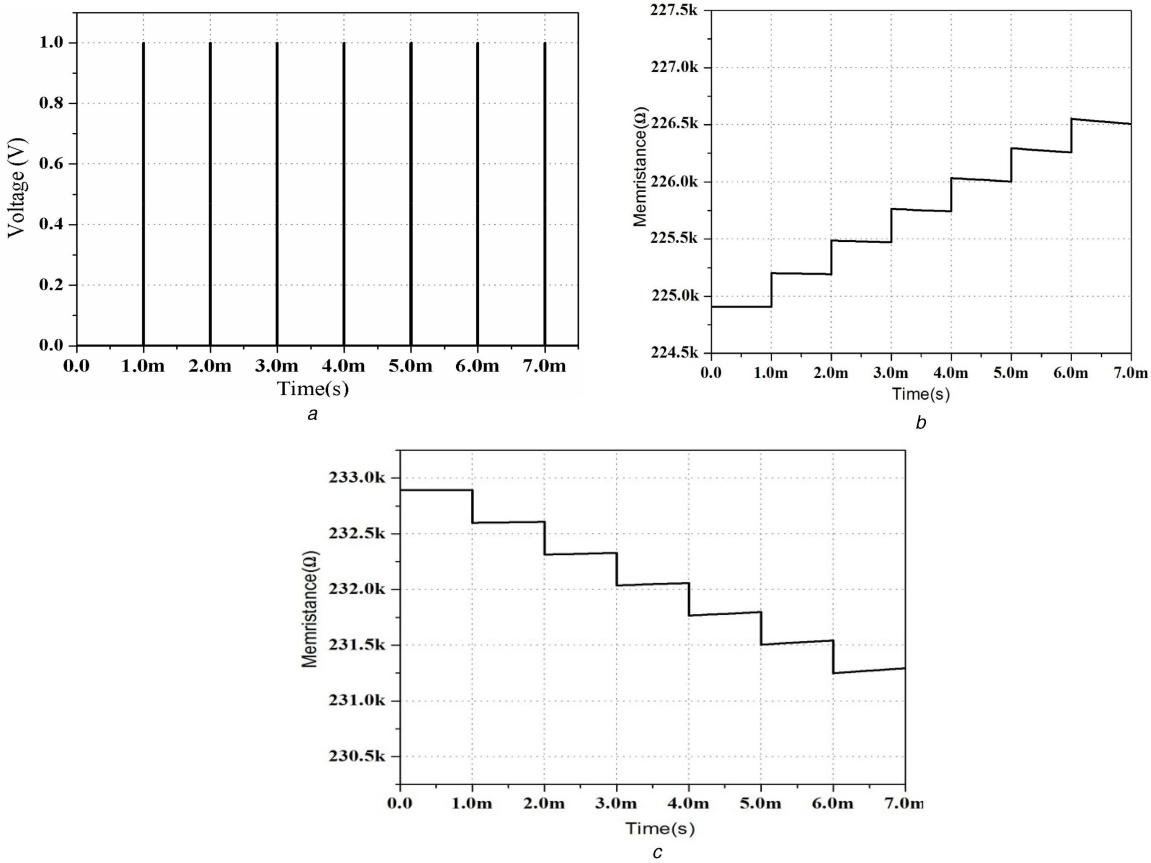


Fig. 10 Test for non-volatility

(a) Applied input pulse of 1 V with a period of 1 ms, (b) Memristance variation in incremental configuration, (c) Memristance variation in decremental configuration

Table 2 Comparison between proposed emulator design and other existing floating-type designs

Reference	No. of active components	No. of passive components	Incremental/decremental	Sim./Exp.	Technology	No. of MOSFETs	Power supply	Max. operating frequency
[22]	2 CCILs, 1 multiplier, 2 op-amps	1 capacitor, 7 resistors	decremental	both	BJT	--	--	Few Hz
[9]	4 CCILs, 1 multiplier, 1 op-amp	1 capacitor, 8 resistors	both	Exp.	BJT	--	-15 V	120 Hz
[23]	2 op-amps, 1 multiplier, 2 AD844	1 capacitor, 7 resistors	incremental	Sim.	BJT	--	± 15 V	160 Hz
[24]	2 op-amps, 1 multiplier 10 transistors	1 capacitor, 2 resistors	decremental	both	BJT	--	± 5 V	800 Hz
[25]	12 OTAs, 1 multiplier	1 capacitor, 3 resistors	both	Sim.	BJT	--	± 10 V	1 kHz
[26]	4 CCILs, 3 OTAs	1 capacitor, 6 resistors	decremental	both	BJT	--	± 15 V	10 kHz
[27]	4 CCILs, 2 diodes	4 capacitors, 4 resistors	incremental	Exp.	BJT	--	± 15 V	Few kHz
[34]	4 AD844, 1 multiplier	1 capacitor, 5 resistors	both	both	BJT	--	± 10 V	20.2 kHz
[35]	4 CCILs + , 1 multiplier	1 capacitor, 3 resistors	both	both	BJT	--	± 10 V	40 kHz
[36]	8 AD844, 2 op-amps	4 capacitors, 8 resistors, 2 inductors	incremental	both	BJT	--	-5 V	150 kHz
[37] proposed work	1 DDCC, 1 multiplier 4 AD844, 1 CA 3080	1 capacitor, 1 resistor 1 capacitor, 4 resistors	both	Sim. both	CMOS BJT	50 --	± 1.5 V ± 10 V	1 MHz 100 kHz
	1 CCII, 1 CCTA	1 capacitor, 3 resistors	both	Sim.	CMOS	38	± 1.5 V	5 MHz

2 kHz in the current voltage plane. It can be observed from Fig. 12 that as the frequency increases, the time-dependent part of the memristor as expressed in (12) will decrease. As a result, it will act as a linear resistor at higher frequencies. Simulation result of the

pinched hysteresis loop shown in Fig. 13 for different values of the capacitor at a frequency of 1 kHz. It is clear from the output that area under the pinched hysteresis loop decreases as the capacitor value increases. This observation justifies theoretical analysis that

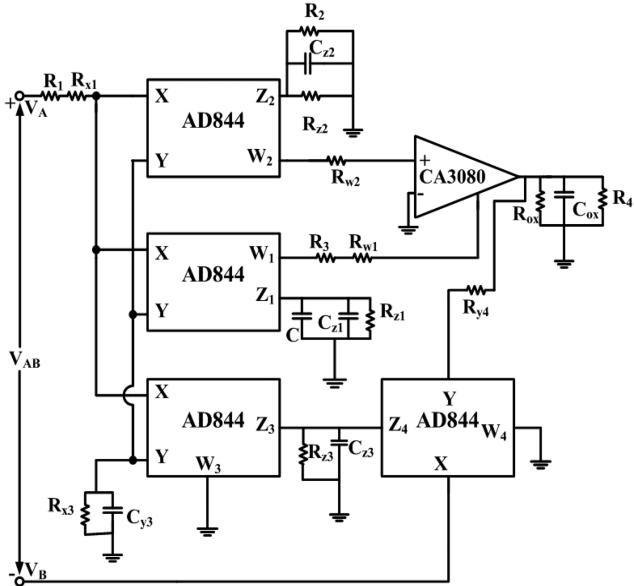


Fig. 11 IC based implementation of memristor emulator circuit using commercially available ICs CA3080 and AD844

Table 3 Parameter and component values used in IC-based design

Element	Value
V _{DD}	±10 V
V _m	4 V
CCII+	AD844
OTA	CA3080
R ₁	10 kΩ
R ₂	2.2 kΩ
R ₃	100 kΩ
R ₄	47 kΩ
C	2 nF (for 1 kΩ)

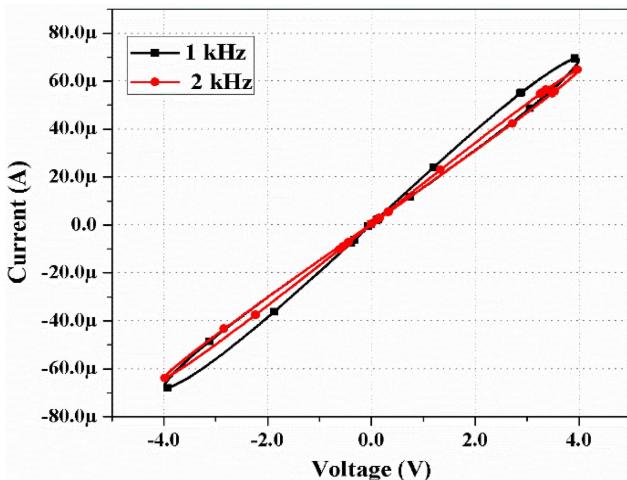


Fig. 12 Voltage-current relationship at frequencies 1 and 2 kHz

the linear time invariant part of memristance equation (12) mentioned in the above section, dominates the linear time-dependent part of higher values of the capacitor. It can be observed from the simulation result that in order to hold pinched hysteresis loop, the value of the capacitor must decrease at higher frequencies.

A non-volatility test for incremental configuration of the IC-based emulator circuit is shown in Fig. 14. It holds the memristance value for the non-pulse period. A similar analysis can be done for decremental configuration. It can operate well up to

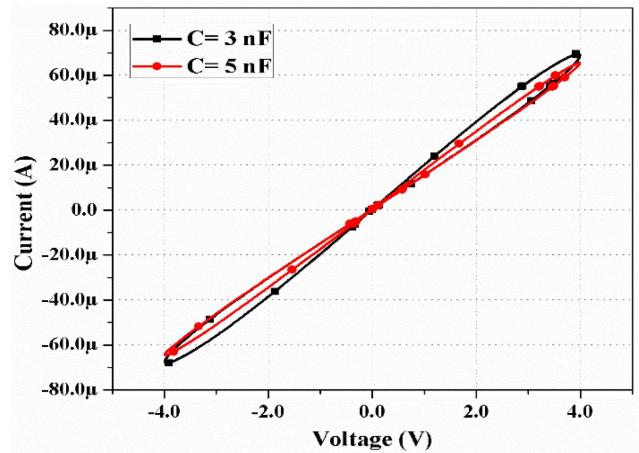


Fig. 13 Voltage-current relationship for capacitor values of 3 and 5 nF at 1 kHz

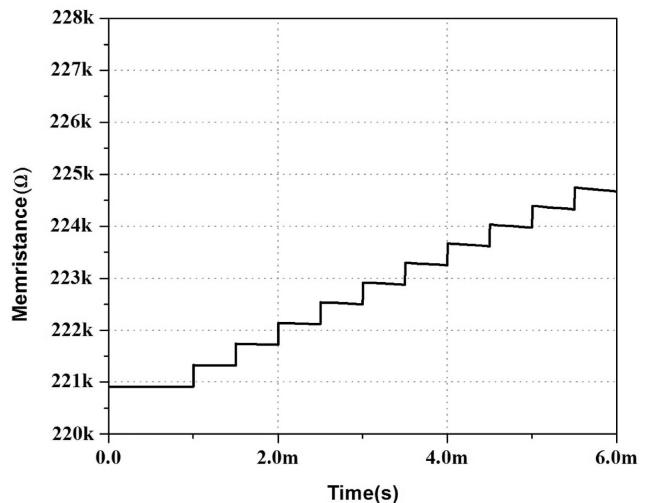
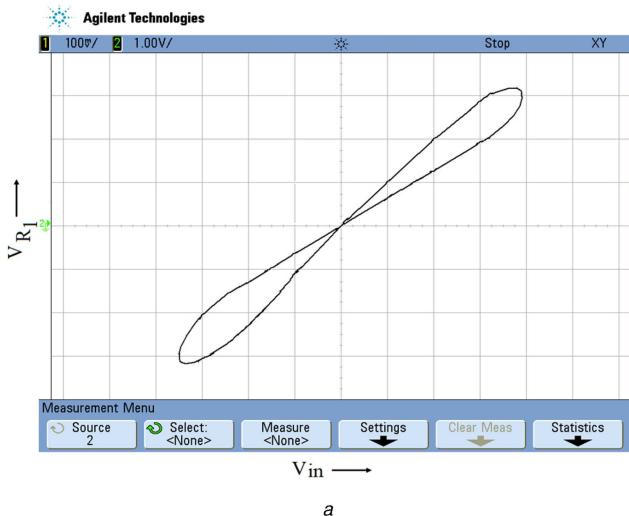


Fig. 14 Non-volatility test of macromodel-based design

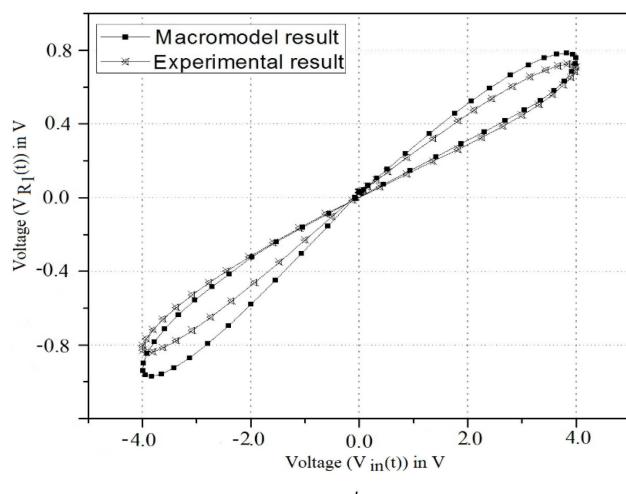
100 kHz without any distortion but on further increasing the frequency, distortion can be noticed. It is observed from Fig. 14 that the memristor holds between non-pulse periods.

8 Experimental results

The performance of the proposed floating memristor emulator is verified experimentally through printed circuit board prototype assembled on a breadboard. Owing to the unavailability of dedicated monolithic IC for CCTA and CCII, the proposed circuit has been realised using four AD844 and a CA3080 as a commonly available IC, shown in Fig. 11. The difference in technology (BJT and CMOS) leads to different values of g_m and supply voltages. It affects the performance of the proposed design. Parameters and component values used for practical implementation have been mentioned in Table 3. The experimentally obtained pinched hysteresis loop in $V_{in}(t)$ versus V_{R1} plane of digital storage oscilloscope (DSO) at an operating frequency of 100 kHz as shown in Fig. 15a proves the time-invariant part is dominated and confirms the theory as discussed in (15). It can be observed from Fig. 15a that the hysteresis loop obtained not only shows asymmetrical behaviour but also offset is observed due to non-idealities in transistor and mismatch in biasing voltage further affecting the practical applications. For the given frequencies, the areas under loop in the first and third quadrant are not alike. The macromodel and experimental results have been shown in Fig. 15b at a frequency of 100 kHz. However, at high frequency, parasitic resistances, parasitic capacitances, non-idealities, loose connections and slew rate of the BJT-based integrated circuit affect the result. The sustaining frequency for the proposed prototype is



a



b

Fig. 15 Experimental result

(a) At a frequency of 100 kHz, (b) Pinched hysteresis loop comparison of Macro-model simulation

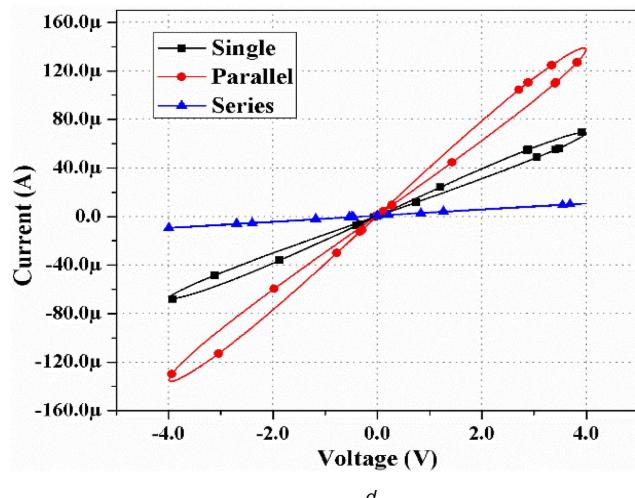
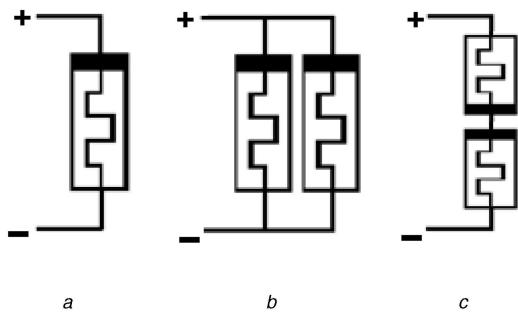


Fig. 16 Circuits of different combinations

(a) Single, (b) Parallel, (c) Series, (d) Comparing pinched hysteresis loop of single, series and parallel memristor combinations

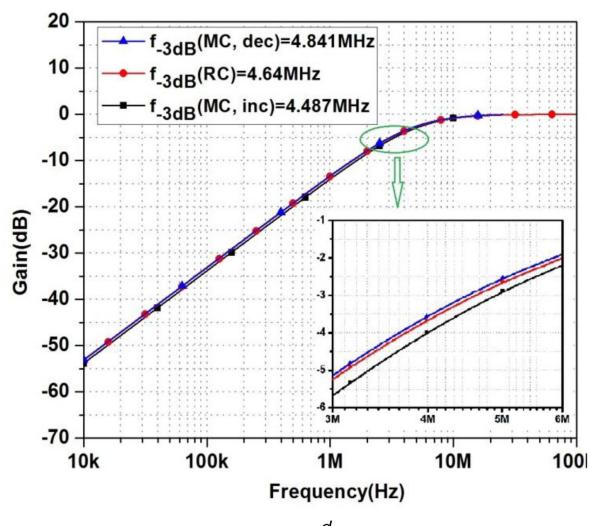
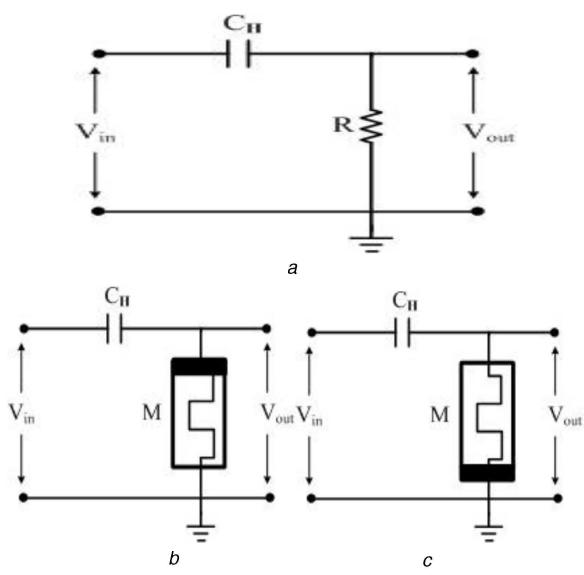


Fig. 17 Circuit implementation of the high-pass filter

(a) Simple RC design, (b) Memristor-capacitor (MC)-based incremental configuration, (c) MC-based decremental configuration, (d) Gain versus frequency plot of high-pass filter in all configurations

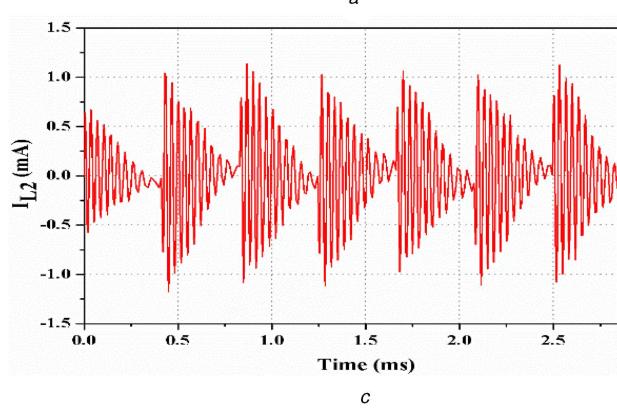
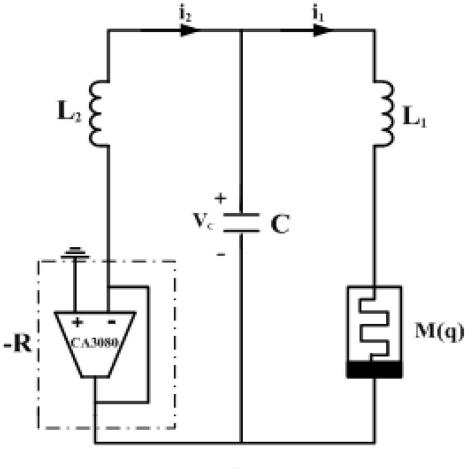


Fig. 18 Canonical Chua's oscillator realization

(a) With proposed memristor emulator, (b) Chaotic output obtained at i_{L1} , (c) Chaotic output obtained at i_{L2} , (d) Double scroll attractor

in the range of few hundred kHz and on further increasing the frequency distortion was observed.

9 Applications

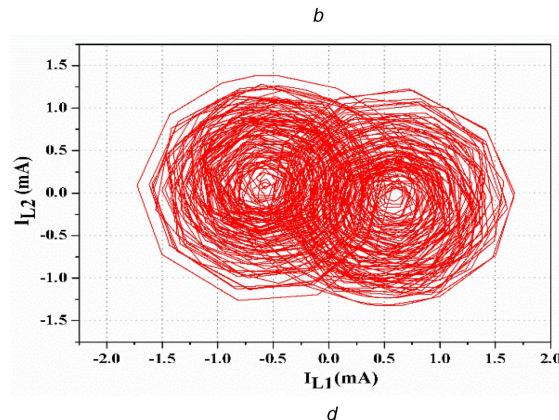
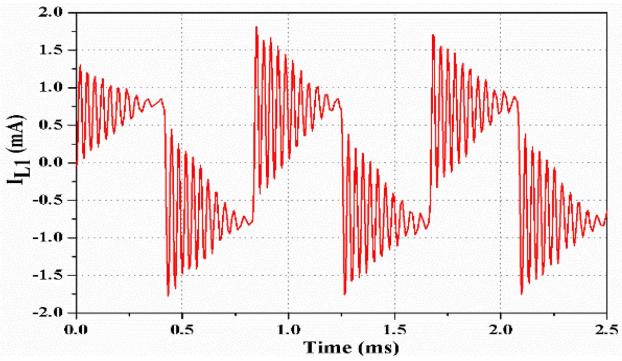
To explore the functionalities of the proposed designs, their applications as parallel and serial combinations, high-pass filter and Chua's oscillator have been presented. The current–voltage relationship of both the combinations has been obtained and compared with that of a single memristor output. Fig. 16a shows an incremental type single memristor, Fig. 16b shows two incremental type memristors connected in parallel combination and Fig. 16c shows one incremental type memristors and one decremental type memristor connected in series combination. In parallel combination, the overall memristance is half of the single one so the area under hysteresis loop increases and for the series combination of one incremental and decremental memristor, the overall memristance remains constant for given input voltage applied across its terminals.

Simulation results obtained for all the three mentioned combinations are shown in Fig. 16d and it can be observed that the area under pinched hysteresis loop for the parallel combination is more than that for a single memristor and the area under pinched hysteresis loop for the series combination is smaller than that for a single memristor which validates the theory as explained in [25].

9.1 High-pass filter

The first-order memristor-based high-pass resistor–capacitor (RC) filter is designed and discussed using the proposed memristor. The filter is designed for both incremental and decremental configurations as shown in Fig. 17. In this filter design, resistance is replaced by the proposed memristor emulator.

A sinusoidal input signal $V_m \sin(2\pi f_m t)$ is applied to the filter. It was observed from (12) that the memristance was varying with the



applied sinusoidal signal and there is variation in R_m around R_{avg} . The (12) can be rewritten as

$$R_m = R_{avg} \pm \Delta R_m \sin(2\pi f_m t + \phi), \quad (27)$$

where ΔR_m is the variation due to the applied signal.

The peak value of R_m is given as

$$R_m = R_{avg} \pm \Delta R_m. \quad (28)$$

The value of ΔR_m can be written as

$$\Delta R_m = \frac{k R_2 R_3 V_m}{2\pi f_m C \left[R_1 \pm k R_2 R_3 \left(\frac{V_{ss}}{2} + V_T \right) \right]}. \quad (29)$$

From (29) [33], it can be observed that ΔR_m will change with the change in amplitude and frequency of the applied sinusoidal signal. Therefore, the memristance value depends upon amplitude, frequency and excitation time of the applied input signal. Thus, the cut-off frequency of the filter can be expressed as

$$f_{-3\text{dB}} = \frac{1}{2\pi C_H [R_{avg} \pm \Delta R_m \sin(2\pi f_m t + \phi)]}. \quad (30)$$

The value of capacitor ' C_H ' and resistance ' R ' of the high-pass filter shown in Fig. 17a is taken as 12 pF and 2.9 k Ω , respectively. In Figs. 17b and c, resistance is replaced by the proposed memristor emulator in both incremental and decremental configurations. The values of capacitors and resistances are taken as $C_H = C = 12$ pF, $R = R_1 = 2.9$ k Ω , $R_2 = 0.5$ k Ω and $R_3 = 1.2$ k Ω , respectively. Pspice simulations for gain versus frequency plot with 3 dB cut-off frequency of the high-pass filter in all the configurations are shown in Fig. 17d.

9.2 Chua's oscillator

The design of Chua's oscillator using the proposed memristor emulator is another important application. The memristor emulator is used to design Chua's oscillator by replacing Chua's diode in Chua's circuit. The proposed memristor emulator is charged control, so a dual canonical circuit [7] is used to design the oscillator where negative resistance is designed using commercially available IC 3080 as shown in Fig. 18a. The dynamic state equation of canonical Chua's oscillator with the proposed memristor emulator can be expressed as

$$\begin{aligned} L_2 \frac{di_2}{dt} &= R i_2 - V_c, \\ L_1 \frac{di_1}{dt} &= V_c - M(q)i_1, \\ C \frac{dV_C}{dt} &= i_2 - i_1. \end{aligned} \quad (31)$$

The values of capacitor C , inductors L_1 and L_2 are taken as 4.5 nF, 21 and 7.2 mH, respectively. Negative resistance is designed using IC CA 3080 with -1250Ω . The chaotic output obtained for i_{Li} and i_{Li} using monolithic IC design are shown in Figs. 18b and c and the simulation response plot of i_{Li} versus i_{Li} is shown in Fig. 18d [10].

10 Conclusion

Floating memristor emulators using one CCTA, one CCII, and few passive elements have been presented. The presented circuit is charge-controlled and works for decremental as well as incremental configurations. IC-based implementation using AD844 and CA3080 has also been done to test the practicability of the circuit. Frequency analysis has been performed to present the behaviour of the voltage-current curve at higher frequencies. Alteration of values of other passive components also affects the lobe area of the pinched hysteresis curve at a particular frequency. It can operate well up to a few MHz. To show the potential of the proposed emulators, high-pass filter and Chua's oscillator have been designed. The simulation and experimental results validate the theory.

11 References

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