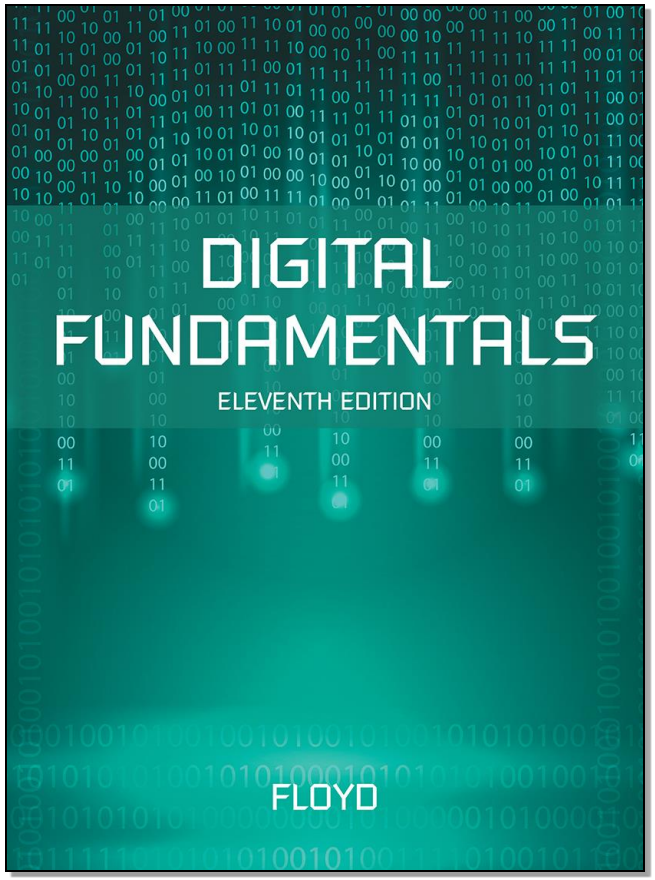
Digital Fundamentals

ELEVENTH EDITION



CHAPTER 10

Programmable Logic

A PAL (programmable array logic) consists of a programmable array of AND gates that connects to a fixed array of OR gates

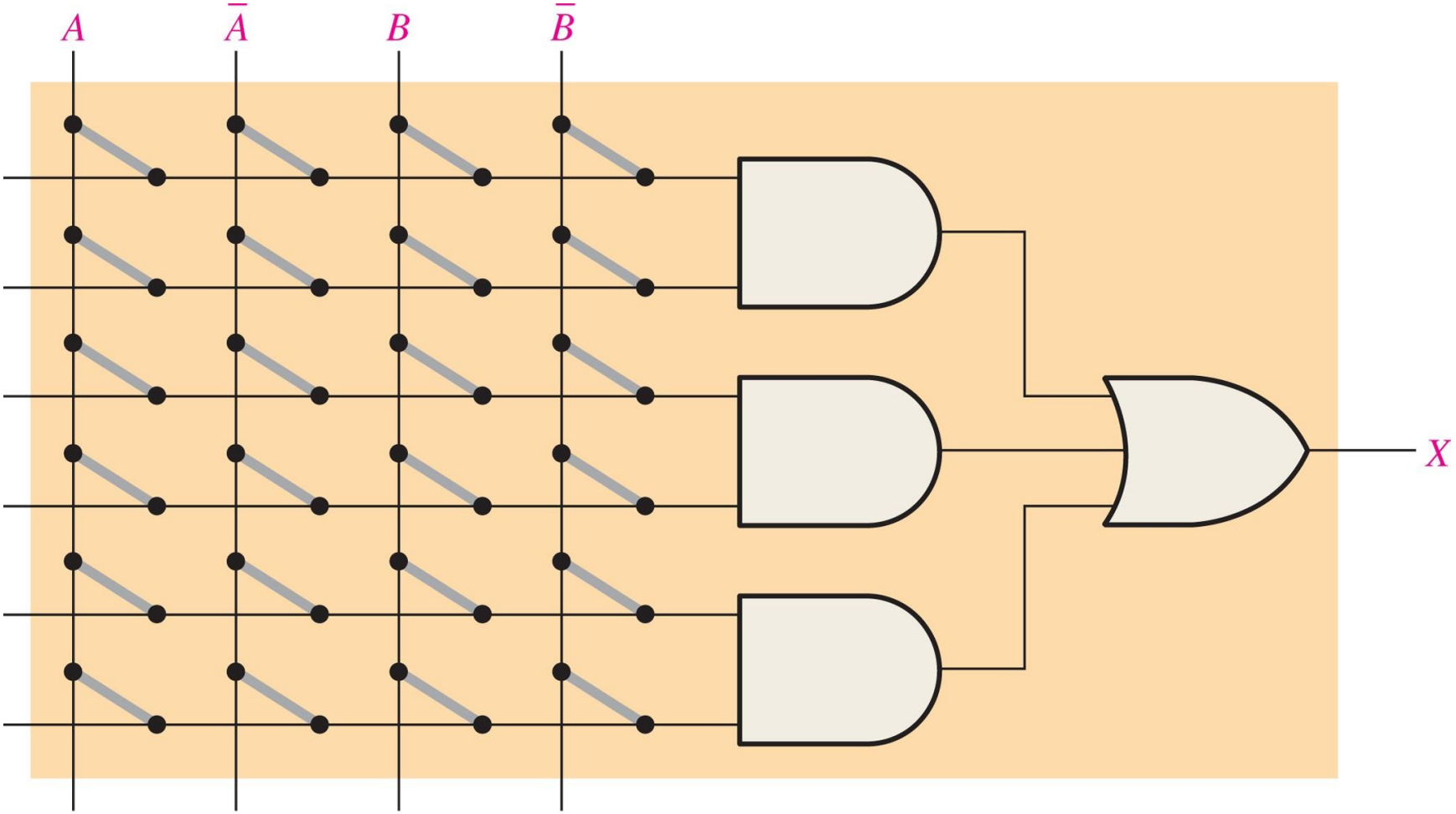


FIGURE 10-2 PAL implementation of a sum-of-products expression.

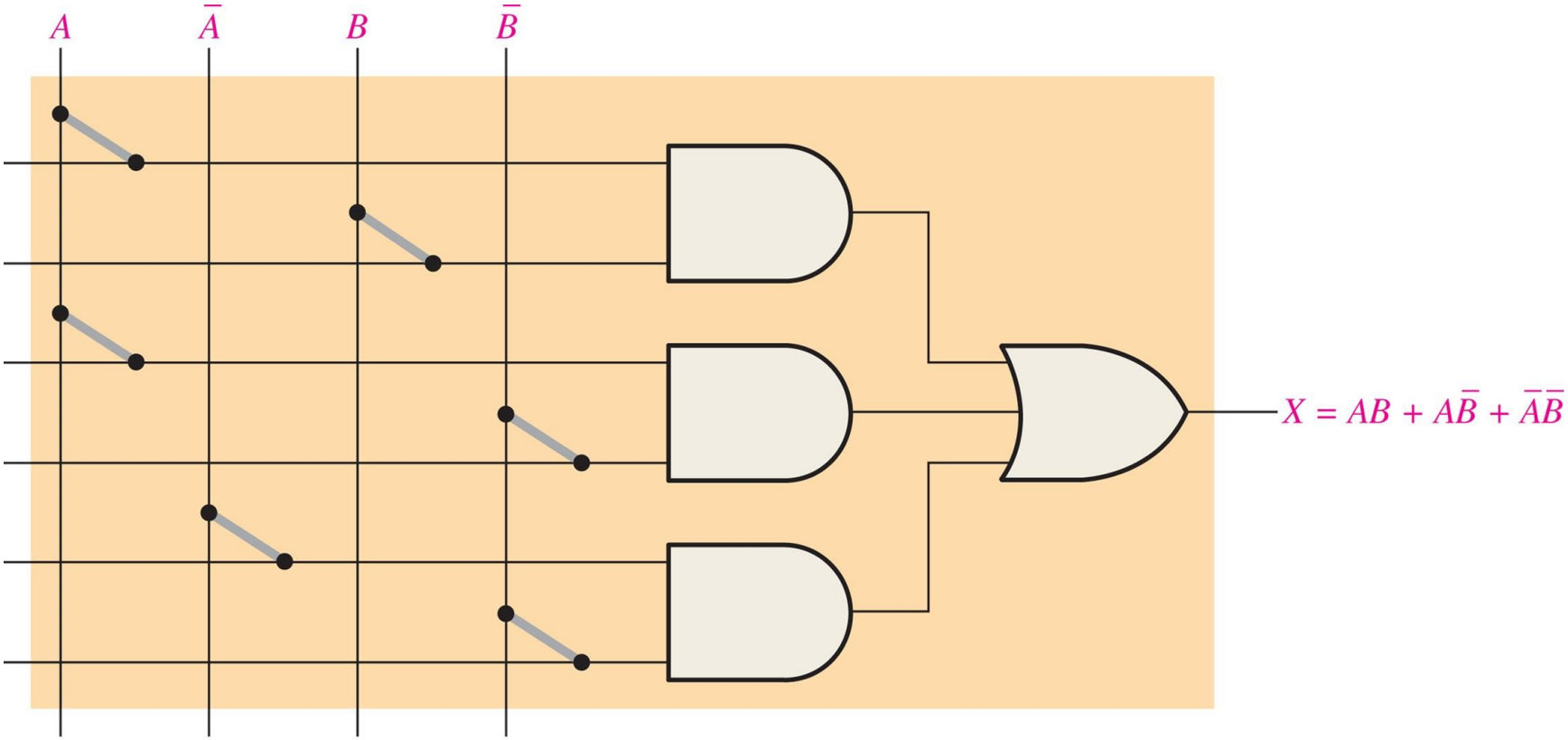


FIGURE 10-3 Simplified GAL array.

SPLD: The GAL The GAL is essentially a PAL that can be reprogrammed. It has the same type of AND/ OR organization that the PAL does. The basic difference is that a GAL uses a reprogrammable process technology, such as EEPROM (E2CMOS), instead of fuses, as shown in Figure 10–3. A A B

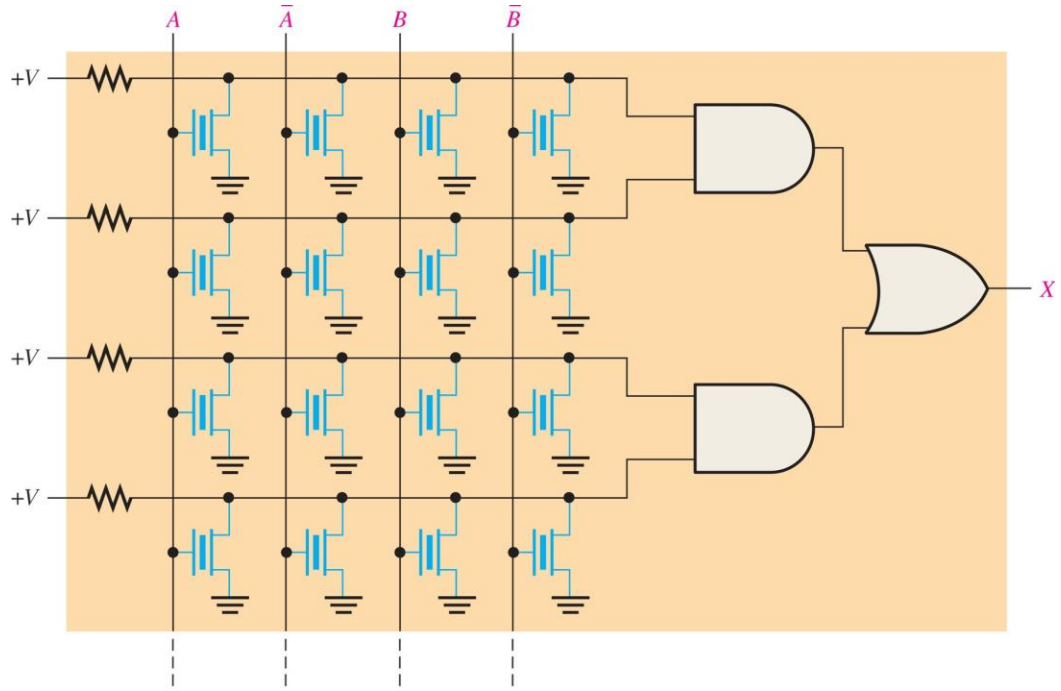


FIGURE 10-4 A portion of a programmed PAL/GAL.

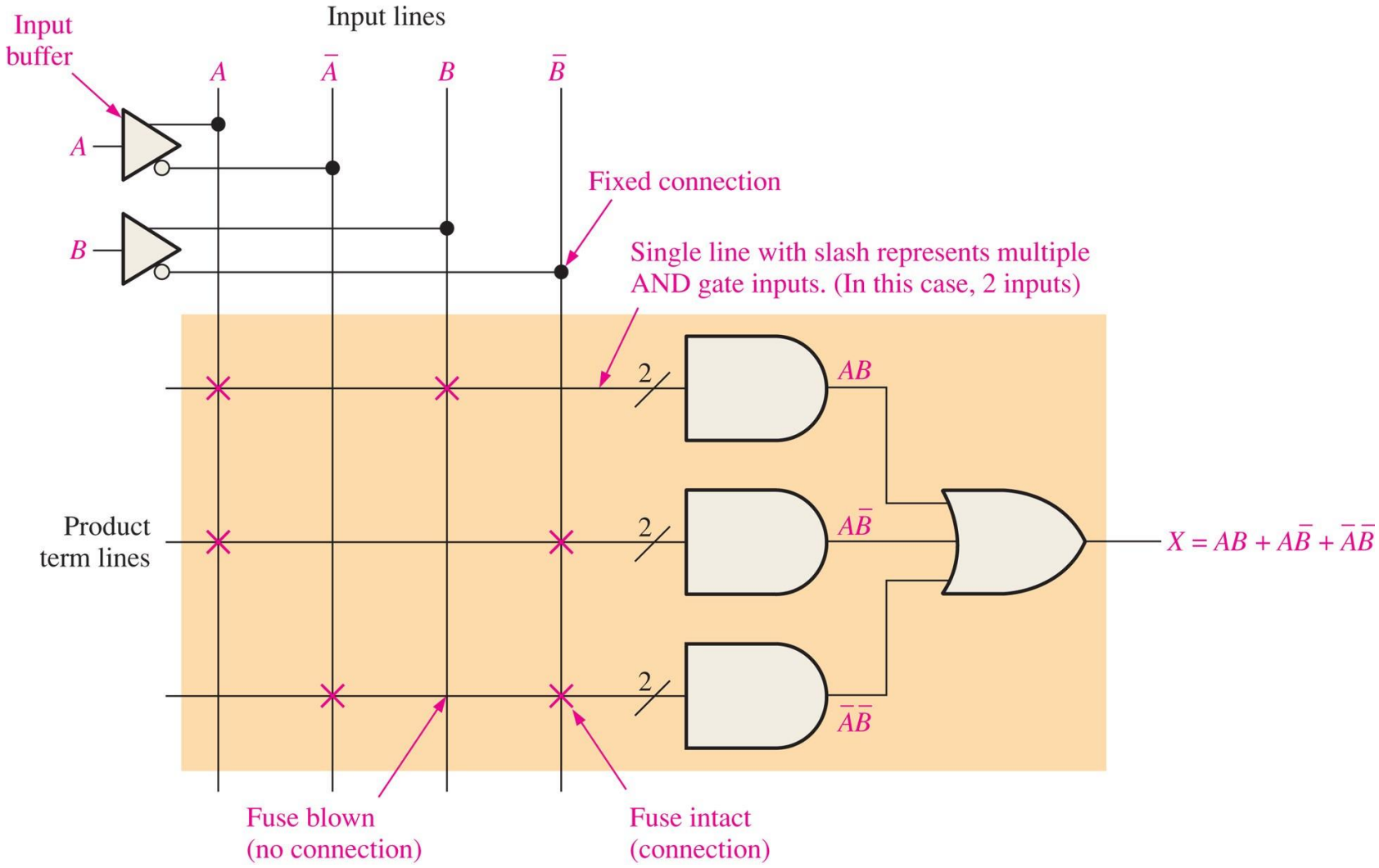


FIGURE 10-5

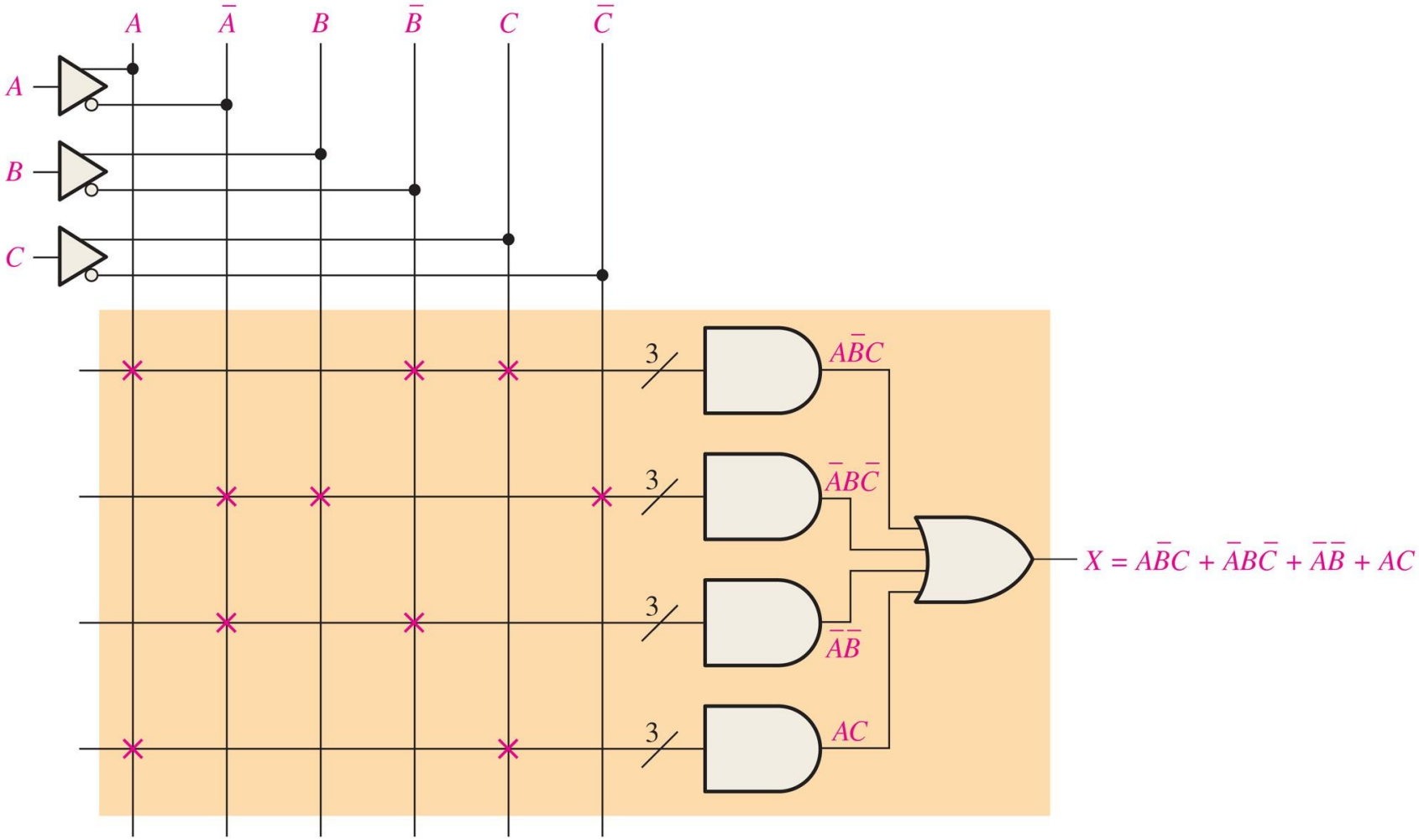


FIGURE 10-6 General block diagram of a PAL or GAL.

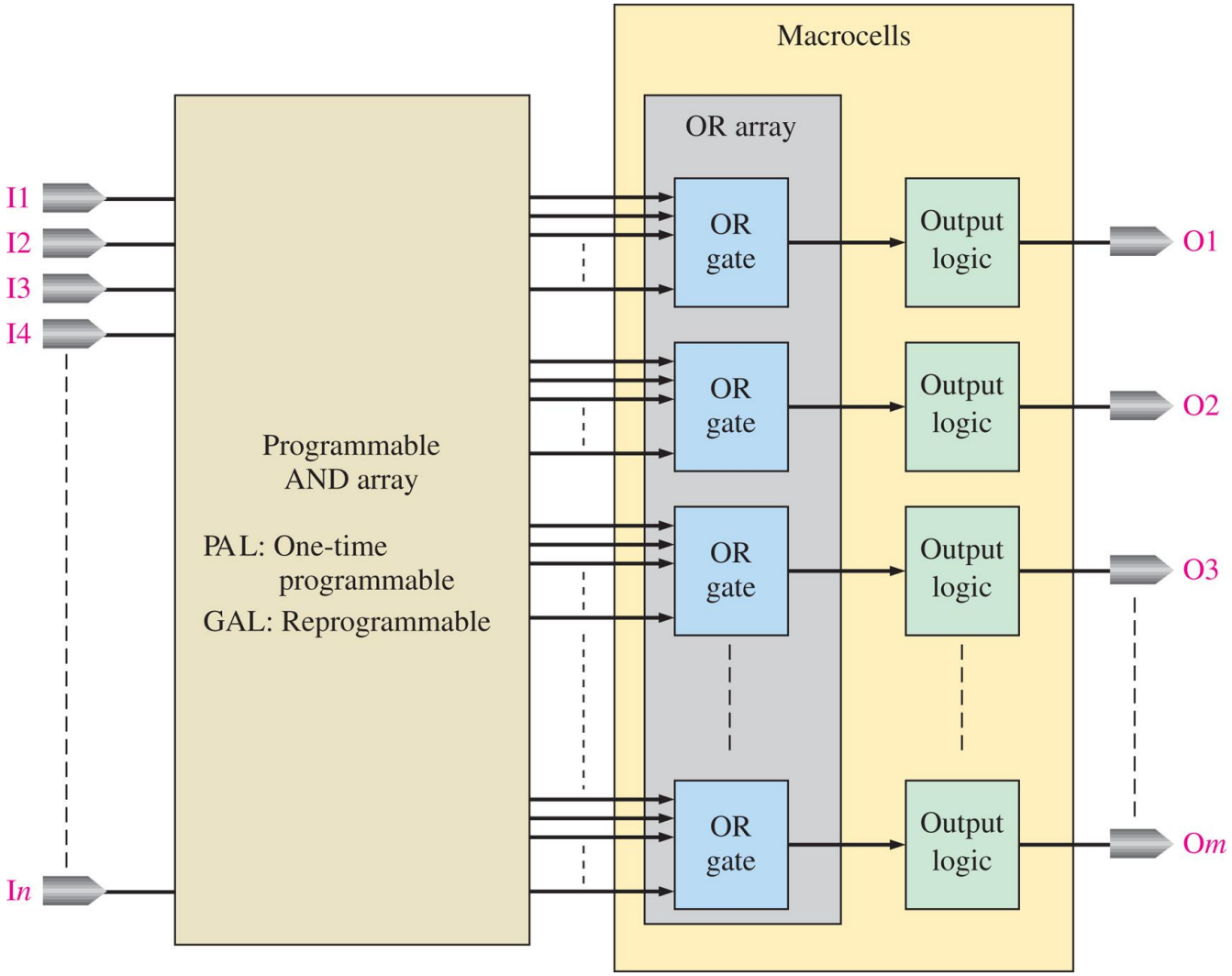
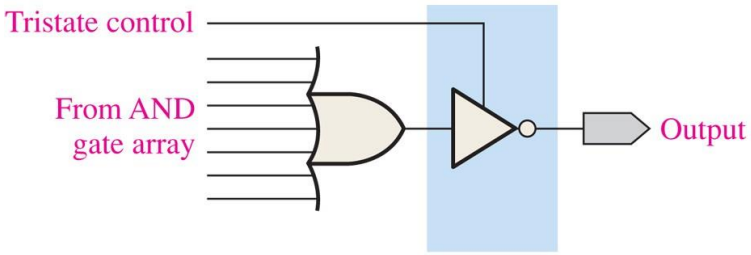
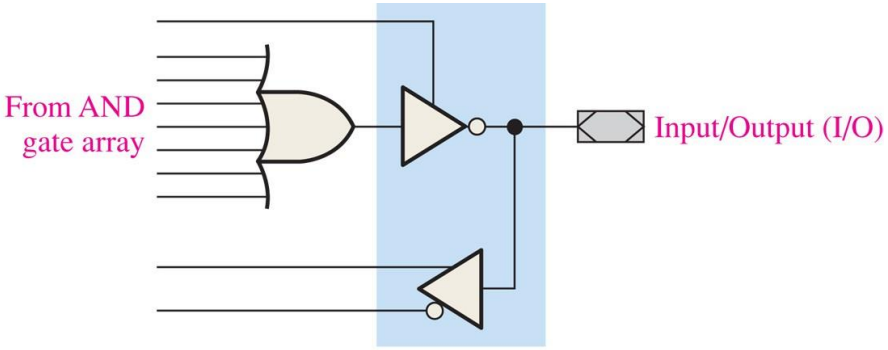


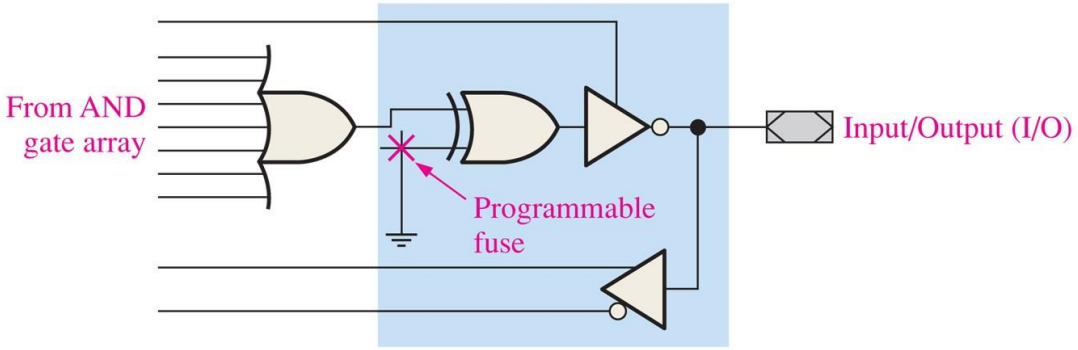
FIGURE 10-7 Basic types of PAL/GAL macrocells for combinational logic.



(a) Combinational output (active-LOW). An active-HIGH output would be shown without the bubble on the tristate gate symbol.



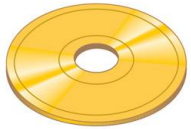
(b) Combinational input/output (active-LOW)



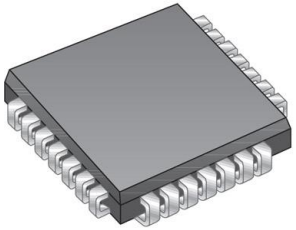
(c) Programmable polarity output

FIGURE 10-35 Essential elements for programming an SPLD, CPLD, or FPGA. (d) photo courtesy of Digilent, Inc.

(a) Computer



(b) Software (CD or Website download)



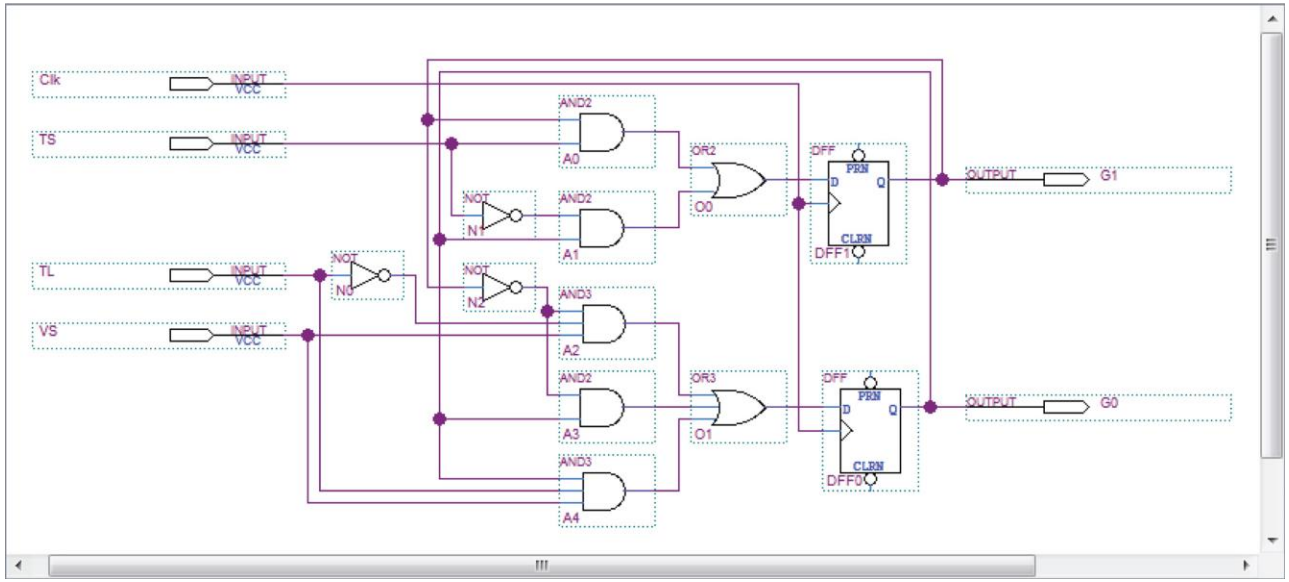
(c) Device

(d) Programming hardware (programming fixture or development board with cable for connection to computer port)

FIGURE 10-37 Text entry with VHDL description of the sequential logic for the traffic signal controller.

```
 1  library ieee;
 2  use ieee.std_logic_1164.all;
 3
 4  entity SequentialLogic is
 5  port(VS, TL, TS, Clk: in std_logic;
 6       G0, G1: inout std_logic);
 7  end entity SequentialLogic;
 8
 9  architecture SequenceBehavior of SequentialLogic is
10  component dff is
11  port(D,Clk: in std_logic;
12       Q: out std_logic);
13  end component dff;
14
15  signal D0, D1: std_logic;
16  begin
17    D1 <= (G0 and not TS) or
18          (G1 and TS);
19
20    D0 <= (not G1 and not TL and VS)  or
21          (not G1 and G0) or
22          (G0 and TL and VS);
23
24  DFF0: dff port map(D => D0, Clk => Clk, Q => G0);
25  DFF1: dff port map(D => D1, Clk => Clk, Q => G1);
26  end architecture SequenceBehavior;
```

FIGURE 10-38 The sequential logic using schematic entry.



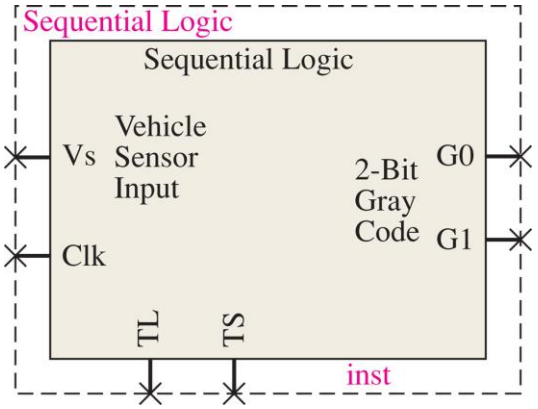


FIGURE 10-44 Downloading a design to the target device.
(Photo courtesy of Digilent, Inc.)