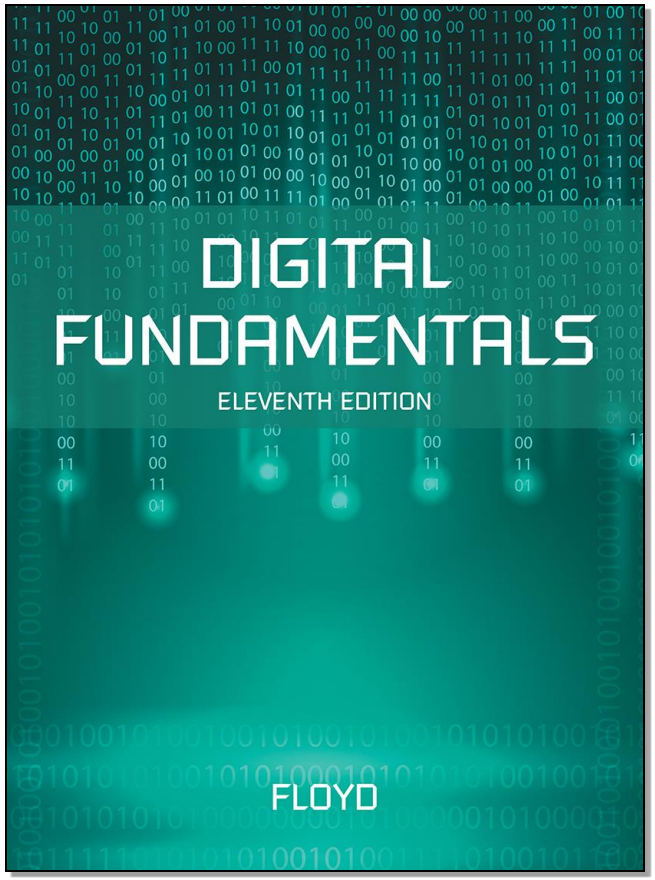
Digital Fundamentals

ELEVENTH EDITION



CHAPTER 8

Shift Registers

FIGURE 8-1 The flip-flop as a storage element.

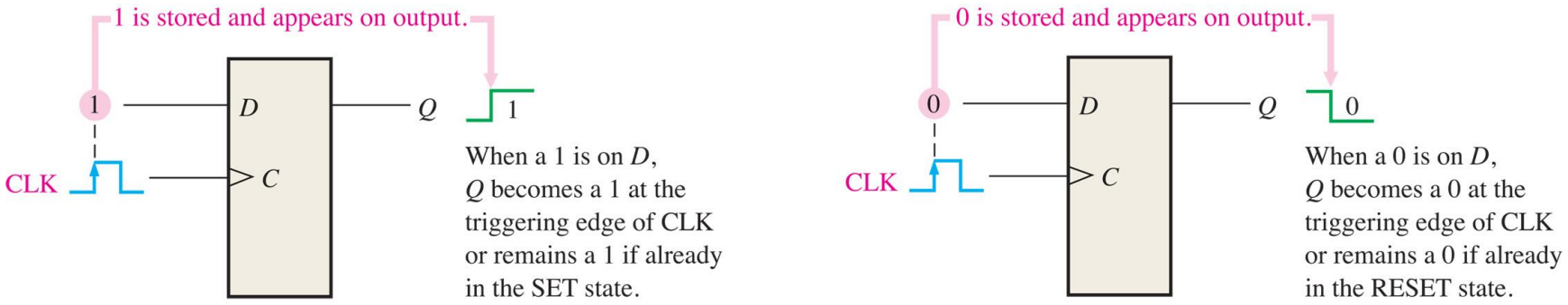


FIGURE 8-2 Basic data movement in shift registers. (Four bits are used for illustration. The bits move in the direction of the arrows.)

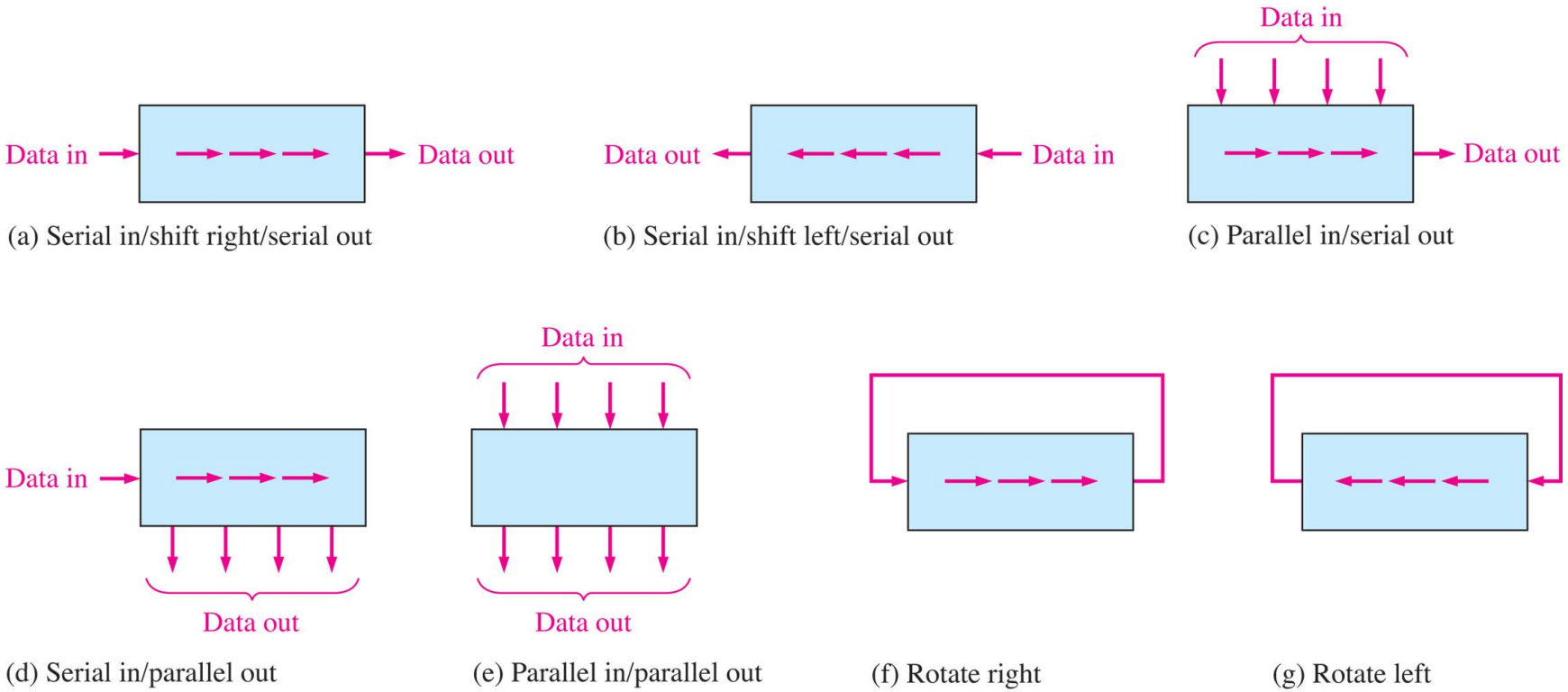


FIGURE 8-3 Serial in/serial out shift register.

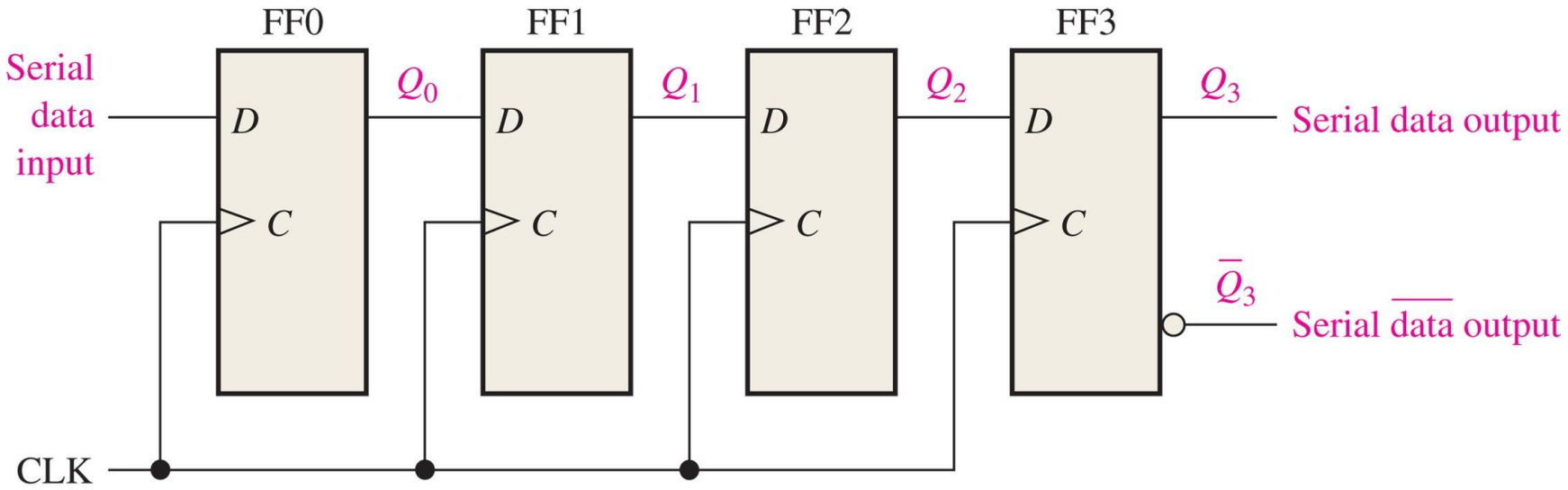


Table 8–1 shows the entry of the four bits 1010 into the register in Figure 8–3

TABLE 8–1

Shifting a 4-bit code into the shift register in Figure 8–3. Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	0	0	0	0
1	**0**	0	0	0
2	**1**	**0**	0	0
3	**0**	**1**	**0**	0
4	**1**	**0**	**1**	**0**

TABLE 8–2

Shifting a 4-bit code out of the shift register in Figure 8–3. Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	**1**	**0**	**1**	**0**
5	0	**1**	**0**	**1**
6	0	0	**1**	**0**
7	0	0	0	**1**
8	0	0	0	0

FIGURE 8-4

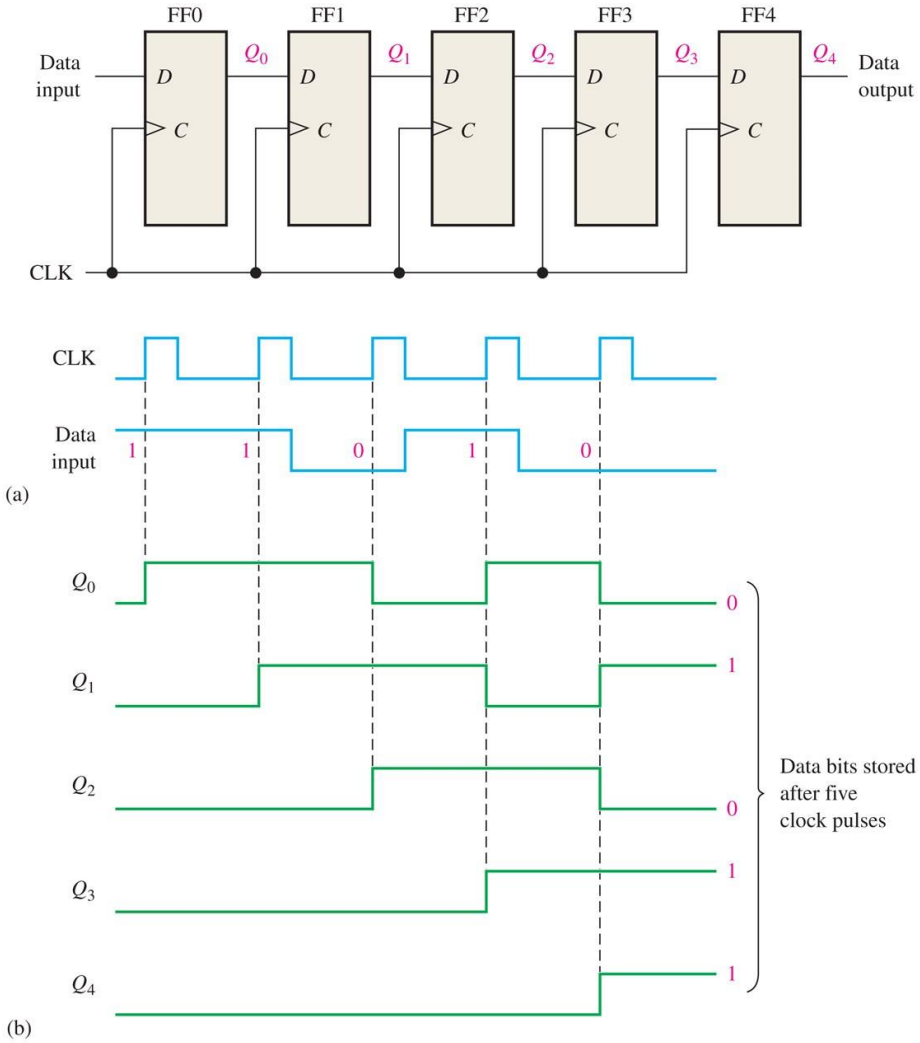


FIGURE 8-5 Logic symbol for an 8-bit serial in/serial out shift register.

FIGURE 8-6 A serial in/parallel out shift register.

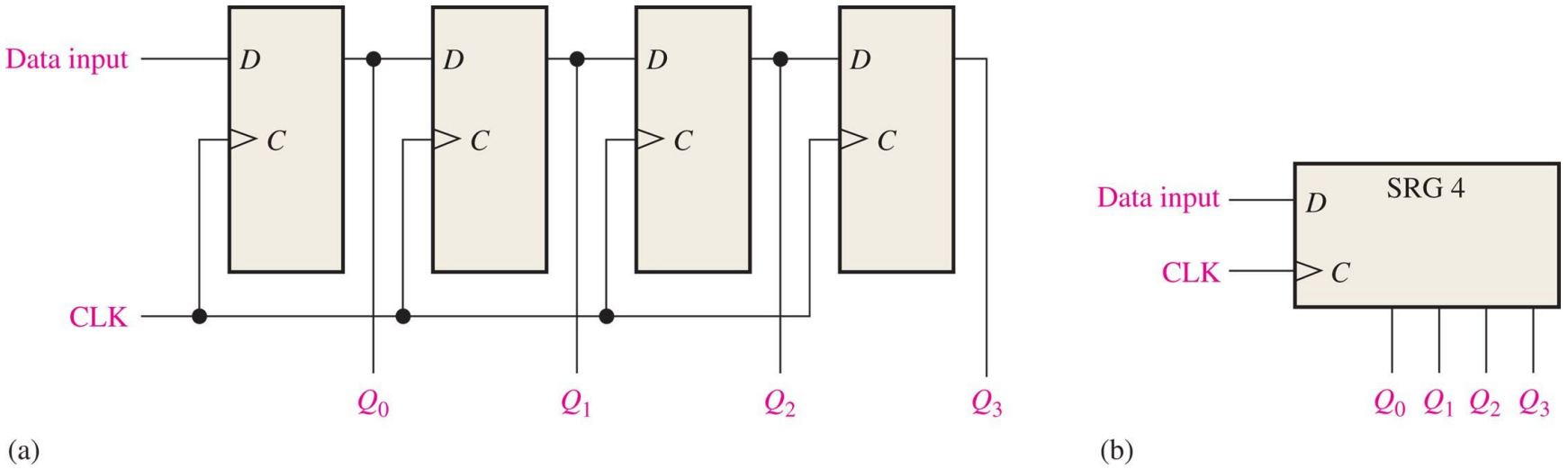
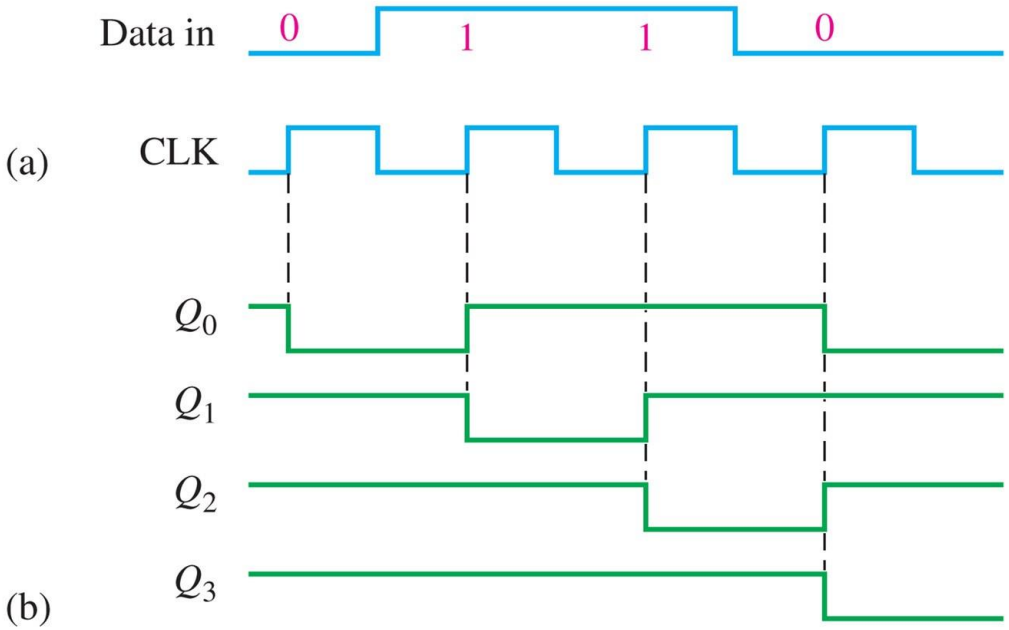
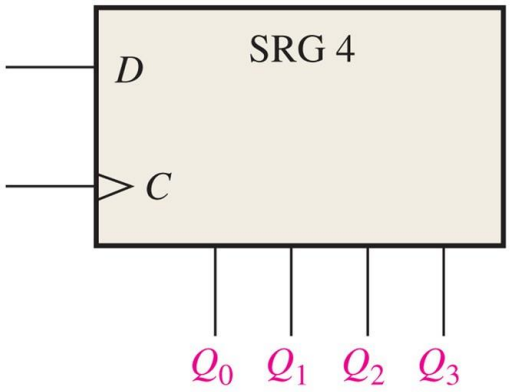


FIGURE 8-7

Show the states of the 4-bit register (SRG 4) for the data input and clock waveforms in Figure 8–7(a). The register initially contains all 1s





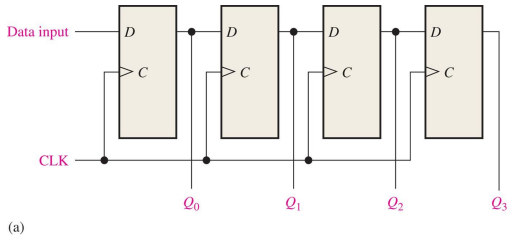


FIGURE 8-8 The 74HC164 8-bit serial in/parallel out shift register.

The 74HC164 is an example of a fixed-function IC shift register having serial in/parallel out operation. The logic block symbol is shown in Figure 8–8. This device has two gated serial inputs, A and B, and an asynchronous clear (CLR) input that is active-LOW. The parallel outputs are Q0 through Q7 .

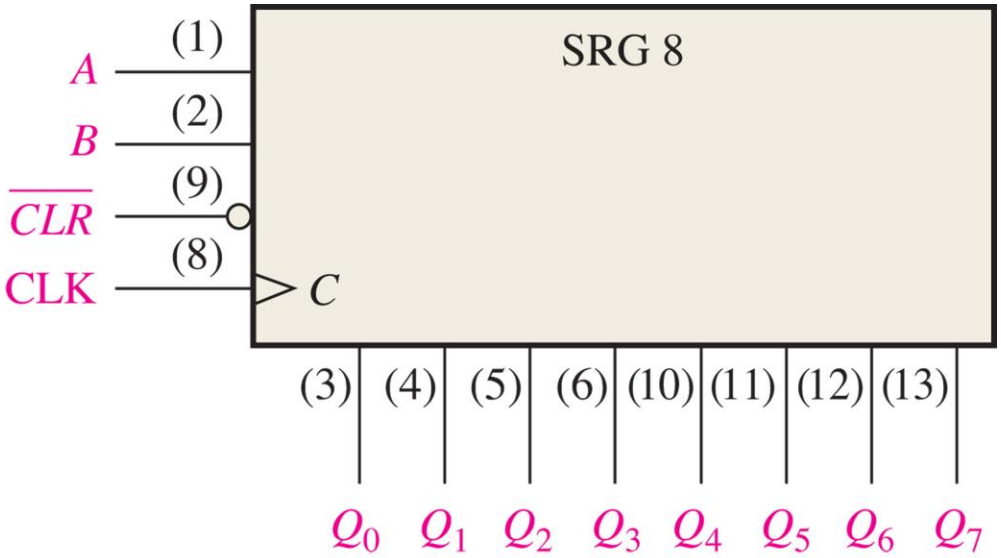


FIGURE 8-9 Sample timing diagram for a 74HC164 shift register.

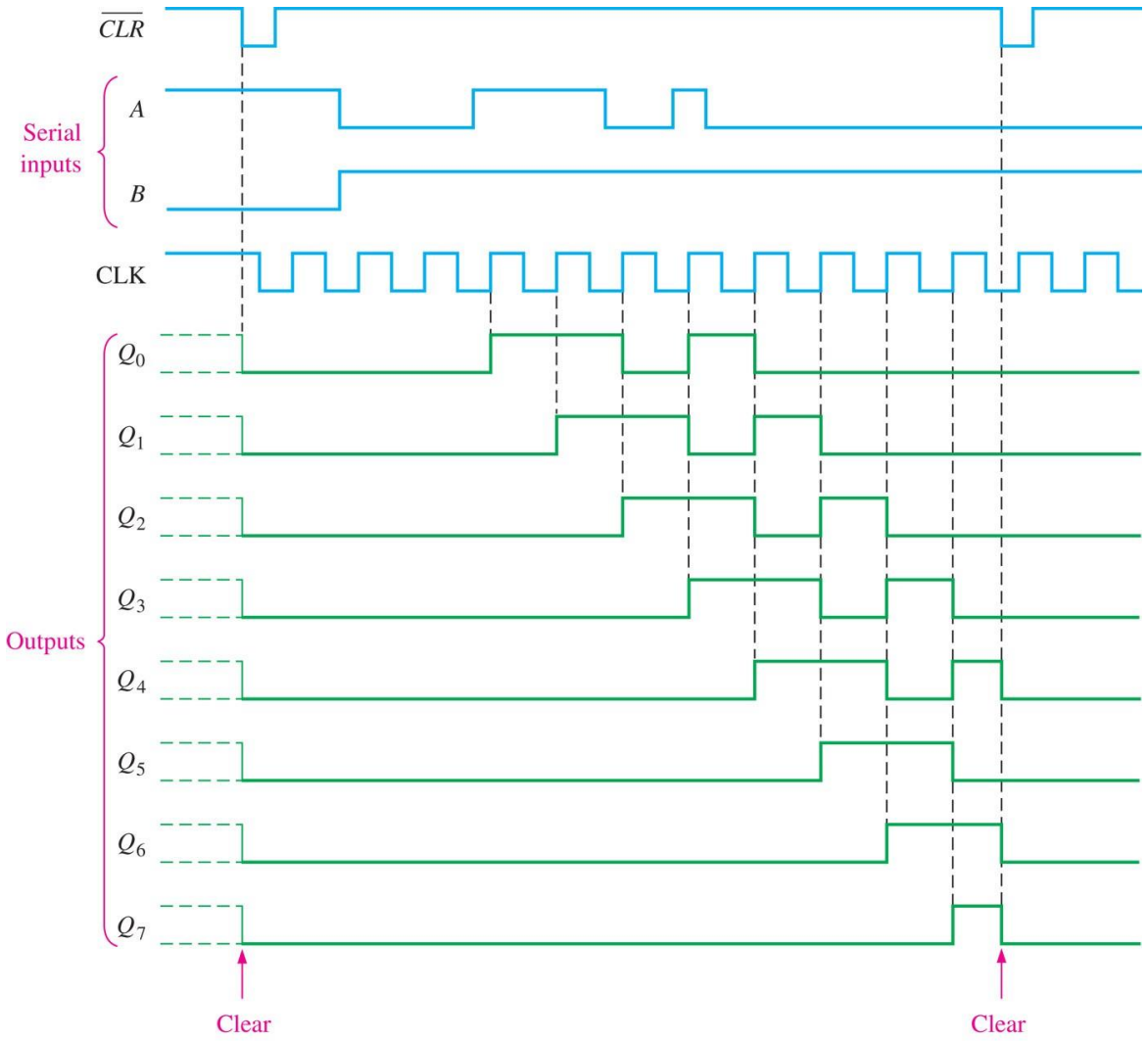
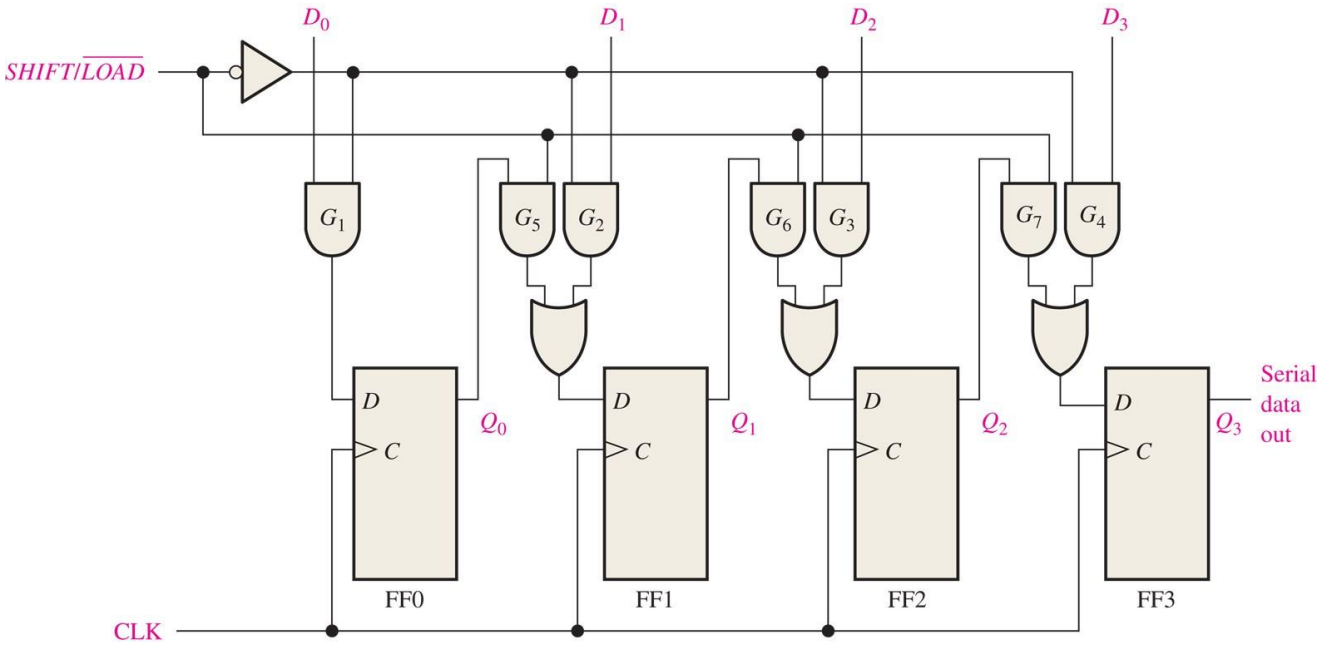
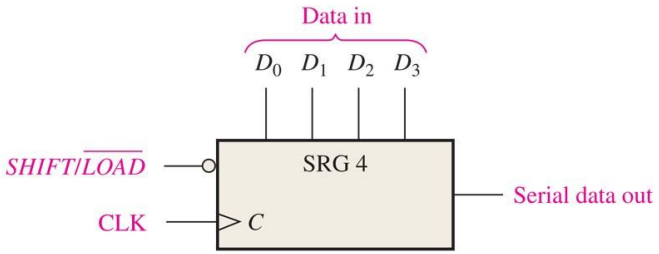


FIGURE 8-10 A 4-bit parallel in/serial out shift register.



(a) Logic diagram



(b) Logic symbol

FIGURE 8-11

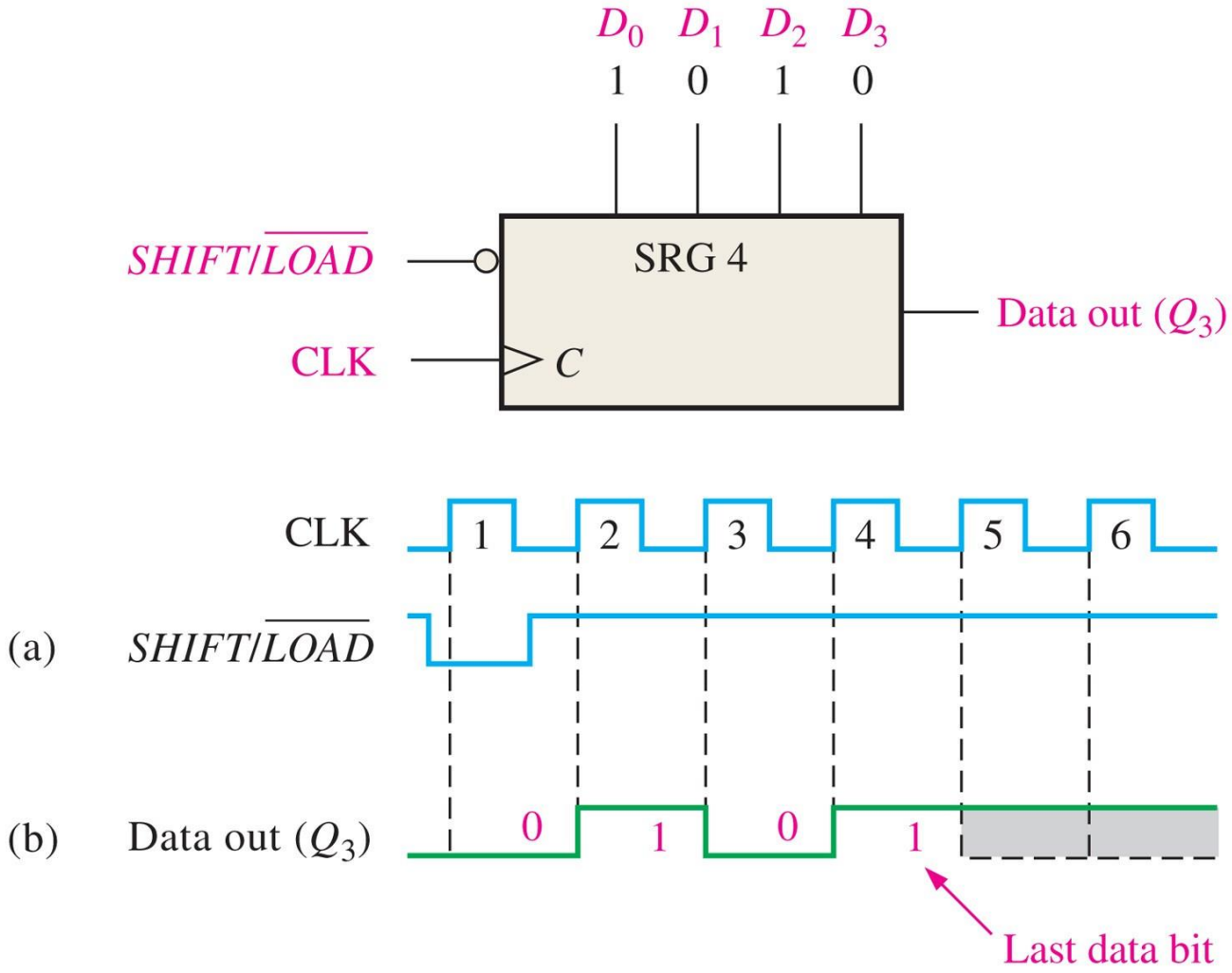


FIGURE 8-12 The 74HC165 8-bit parallel load shift register.

The 74HC165 is an example of a fixed-function IC shift register that has a parallel in/serial out operation (it can also be operated as serial in/serial out). Figure 8–12 shows a typical logic block symbol. A LOW on the SHIFT/LOAD input (SH/LD) enables asynchronous parallel loading. Data can be entered serially on the SER input. Also, the clock can be inhibited anytime with a HIGH on the CLK INH input. The serial data outputs of the register are Q7 and its complement Q7 .

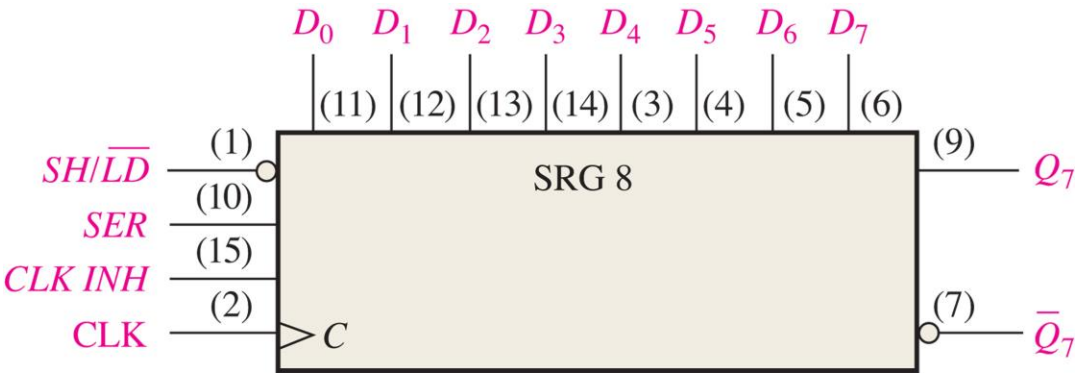


FIGURE 8-13 Sample timing diagram for a 74HC165 shift register.

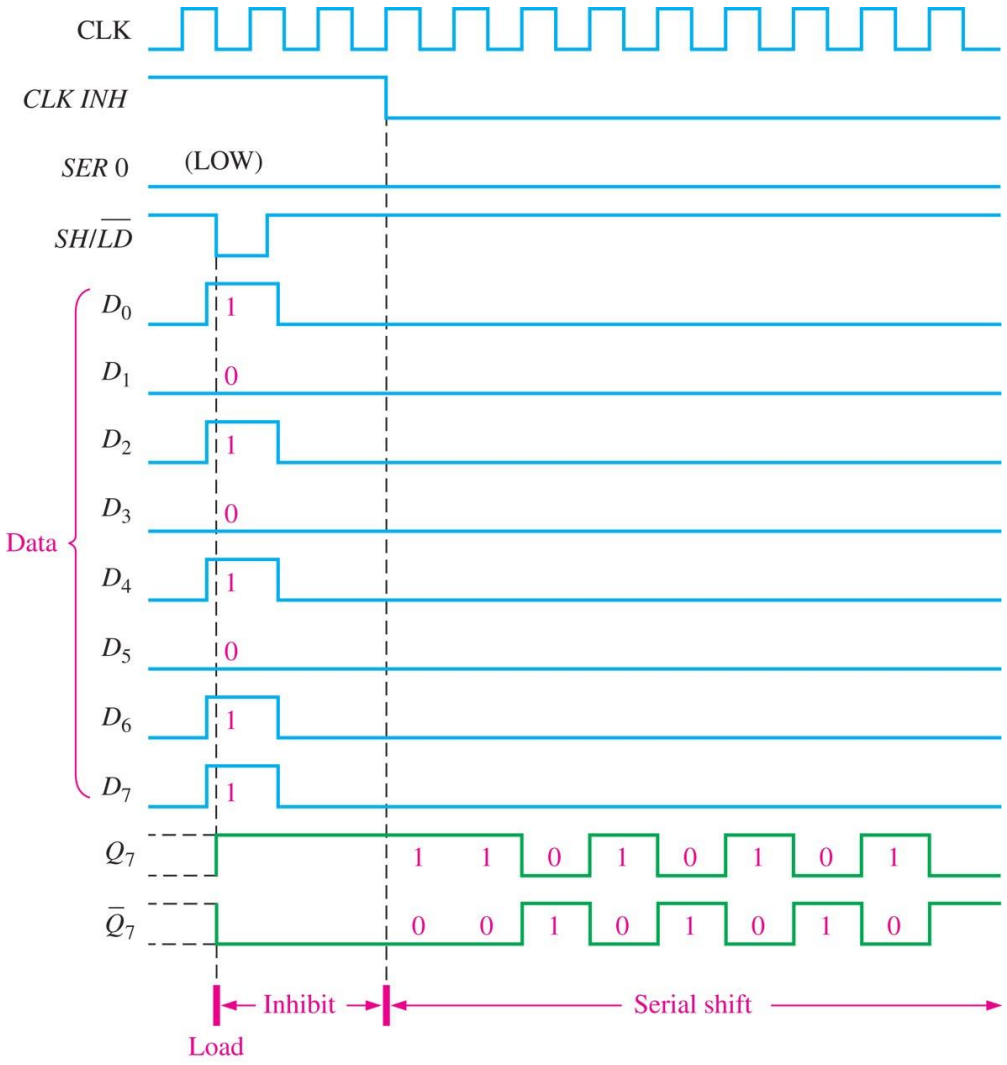


FIGURE 8-14 A parallel in/parallel out register.

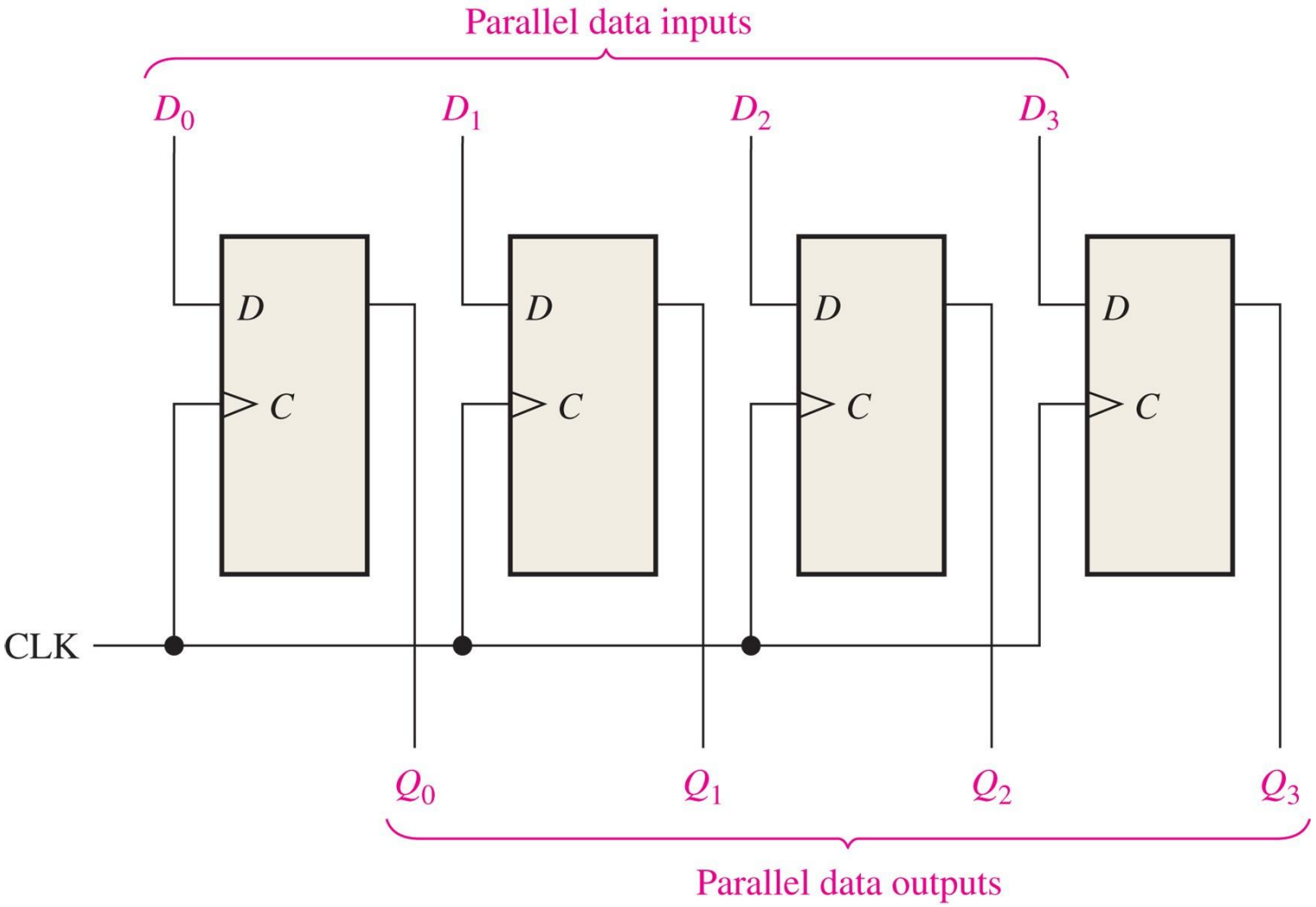
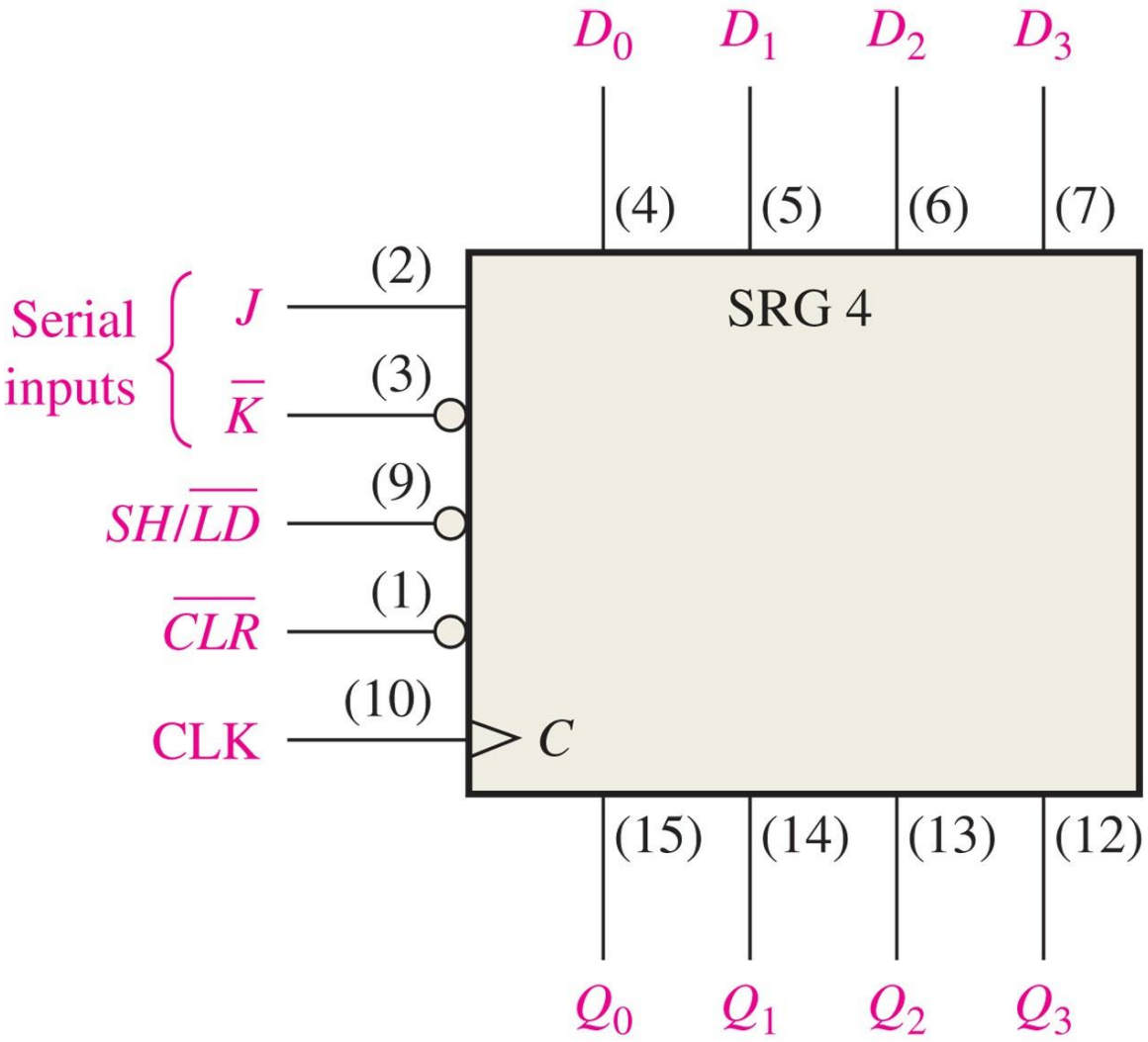


FIGURE 8-15 The 74HC195 4-bit parallel access shift register.



The 74HC195 can be used for parallel in/parallel out operation. Because it also has a serial input, it can be used for serial in/serial out and serial in/parallel out operations. It can be used for parallel in/serial out operation by using Q3 as the output. A typical logic block symbol is shown in Figure 8–15.

When the SHIFT/LOAD input (SH/LD) is LOW, the data on the parallel inputs are entered synchronously on the positive transition of the clock. When (SH/LD) is HIGH, stored data will shift right (Q0 to Q3) synchronously with the clock. Inputs J and K are the serial data inputs to the first stage of the register (Q0); Q3 can be used for serial output data. The active-LOW clear input is asynchronous

FIGURE 8-16 Sample timing diagram for a 74HC195 shift register.

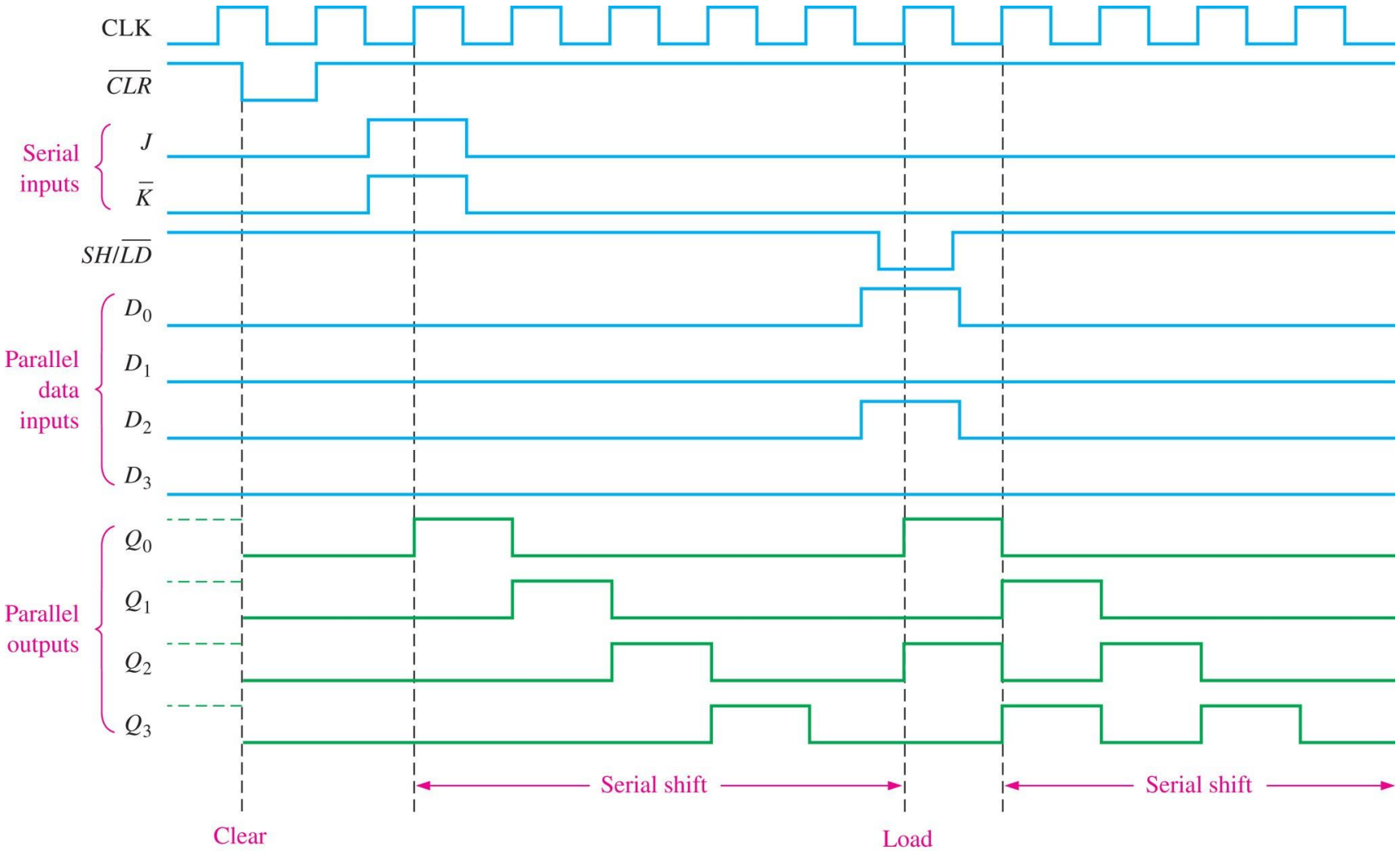


FIGURE 8-17 Four-bit bidirectional shift register.

Determine the state of the shift register of Figure 8–17 after each clock pulse for the given RIGHT/LEFT control input waveform in Figure 8–18(a). Assume that Q0 = 1, Q1 = 1, Q2 = 0, and Q3 = 1 and that the serial data-input line is LOW.

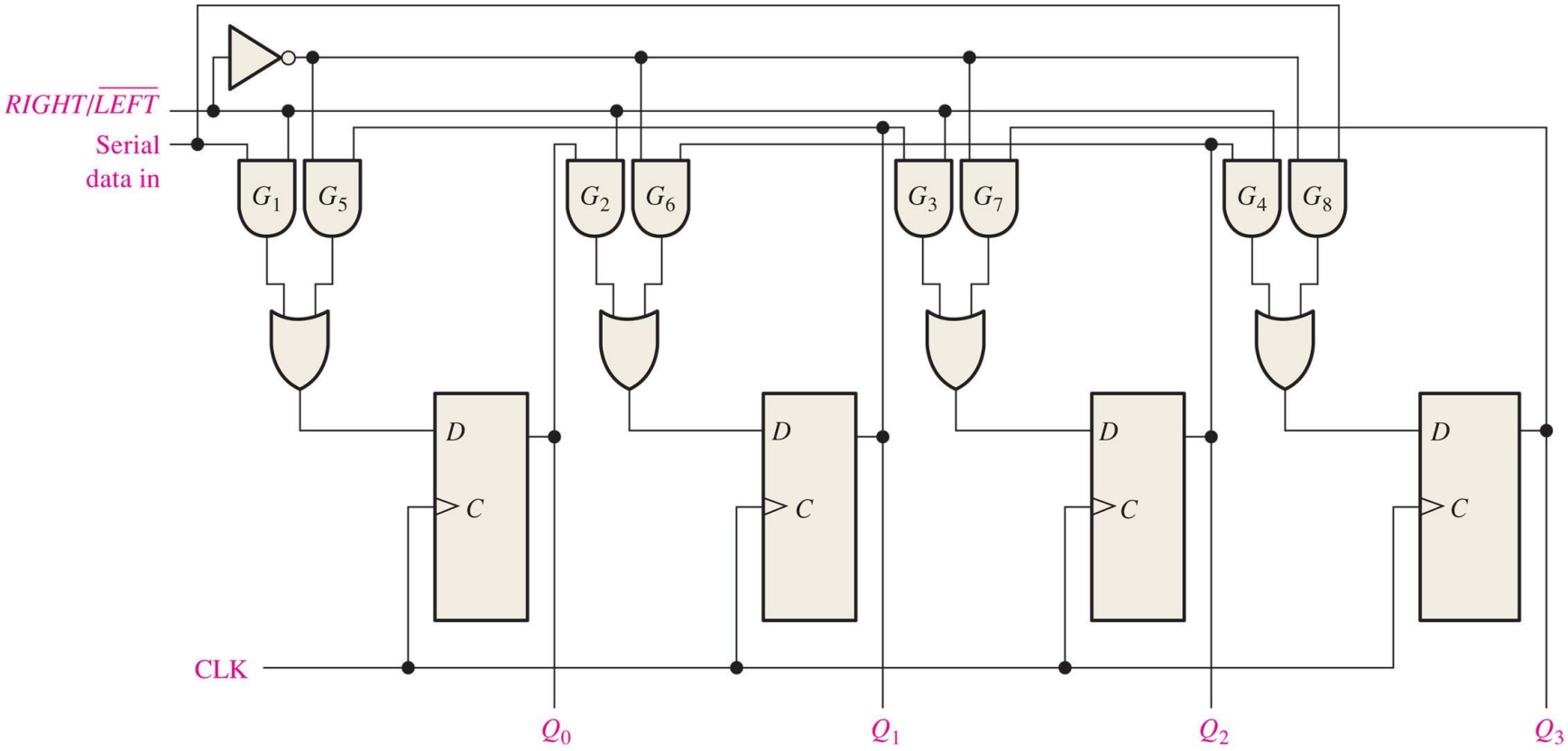


FIGURE 8-18

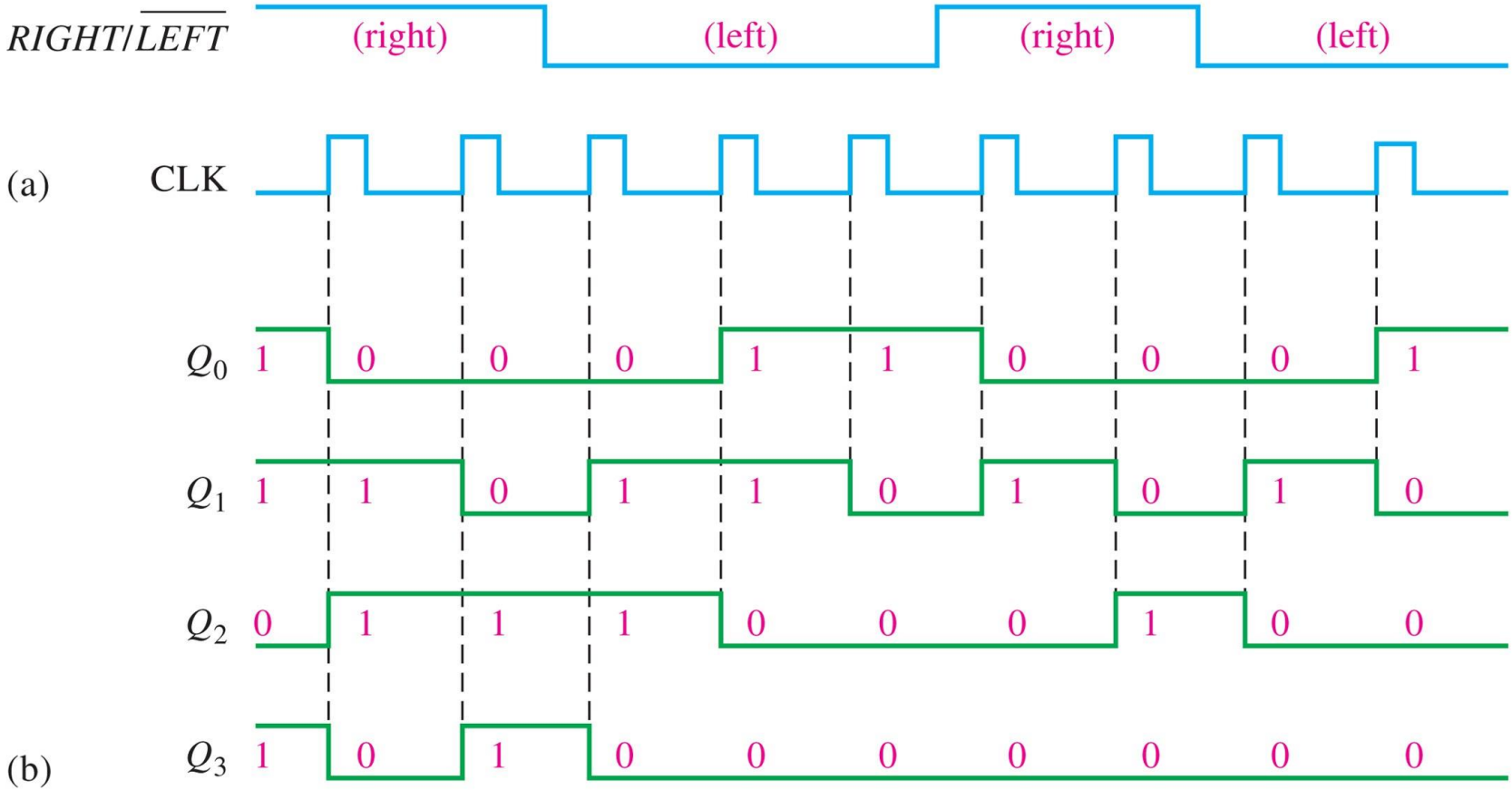
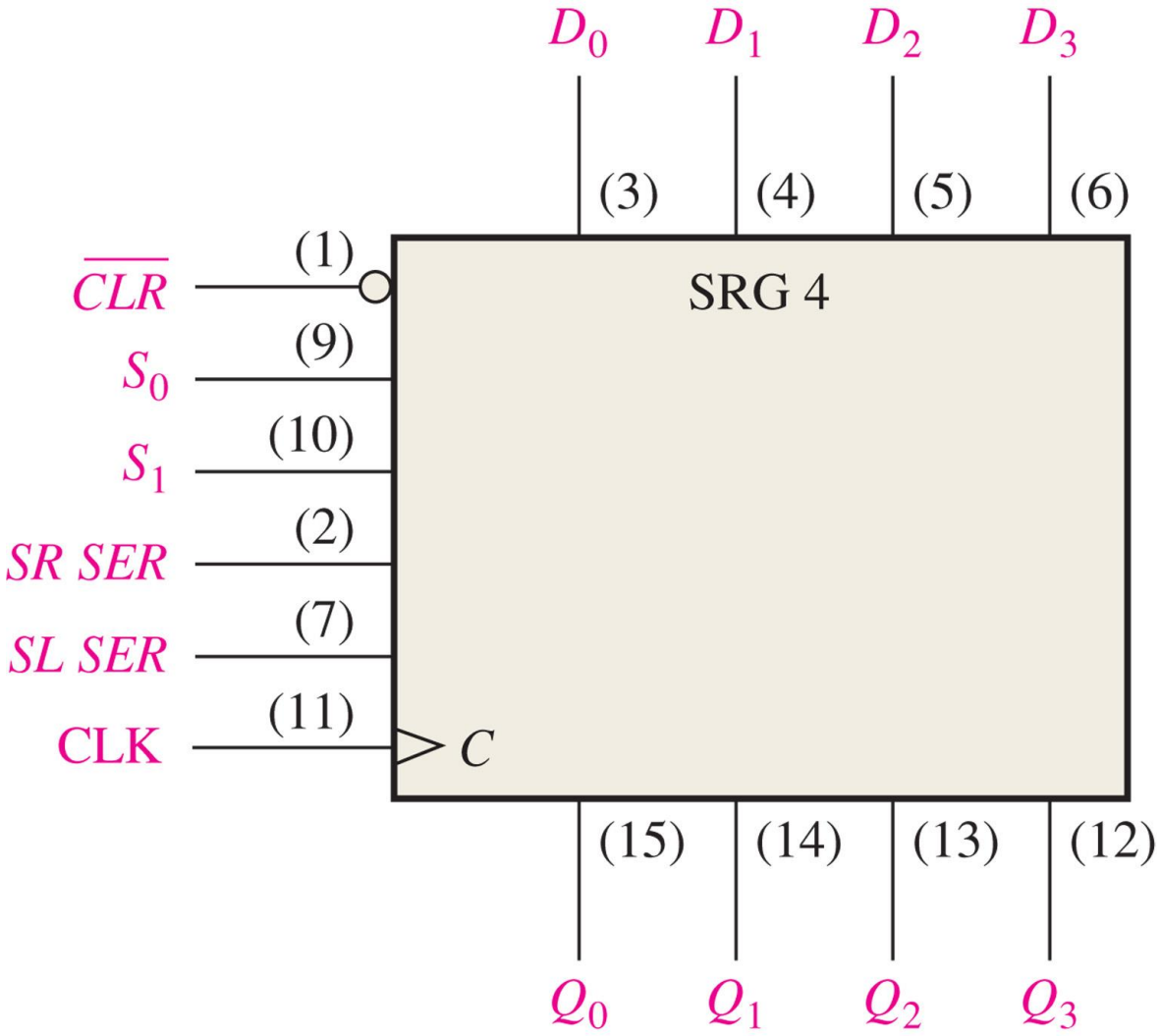


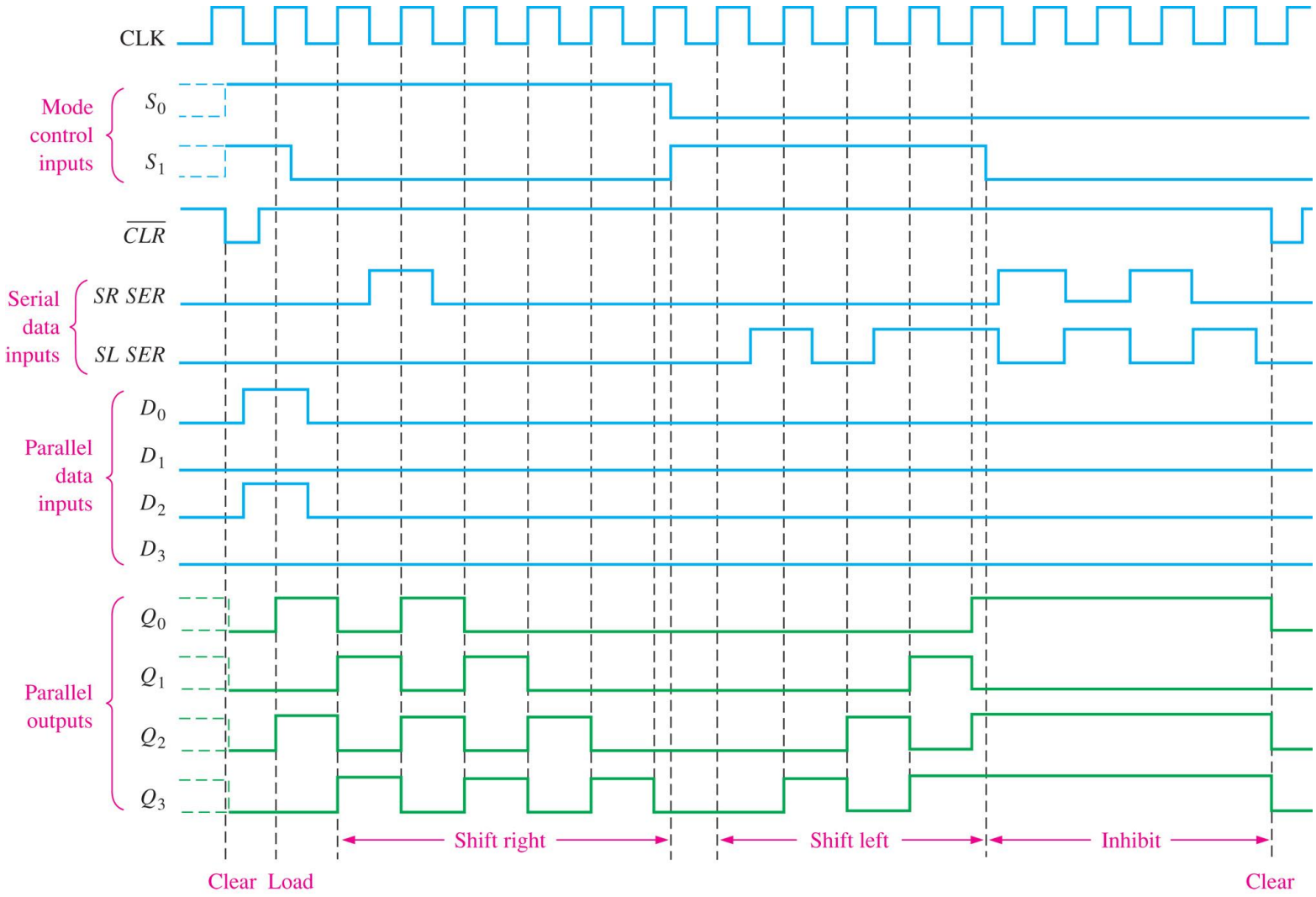
FIGURE 8-19 The 74HC194 4-bit bidirectional universal shift register.



The 74HC194 is an example of a universal bidirectional shift register in integrated circuit form

Parallel loading, which is synchronous with a positive transition of the clock, is accomplished by applying the four bits of data to the parallel inputs and a HIGH to the S0 and S1 inputs. Shift right is accomplished synchronously with the positive edge of the clock when S0 is HIGH and S1 is LOW. Serial data in this mode are entered at the shift-right serial input (SR SER). When S0 is LOW and S1 is HIGH, data bits shift left synchronously with the clock, and new data are entered at the shift-left serial input (SL SER). Input SR SER goes into the Q0 stage, and SL SER goes into the Q3 stage

FIGURE 8-20 Sample timing diagram for a 74HC194 shift register.



A shift register counter is basically a shift register with the serial output connected back to the serial input to produce special sequences.

TABLE 8–3

Four-bit Johnson sequence.

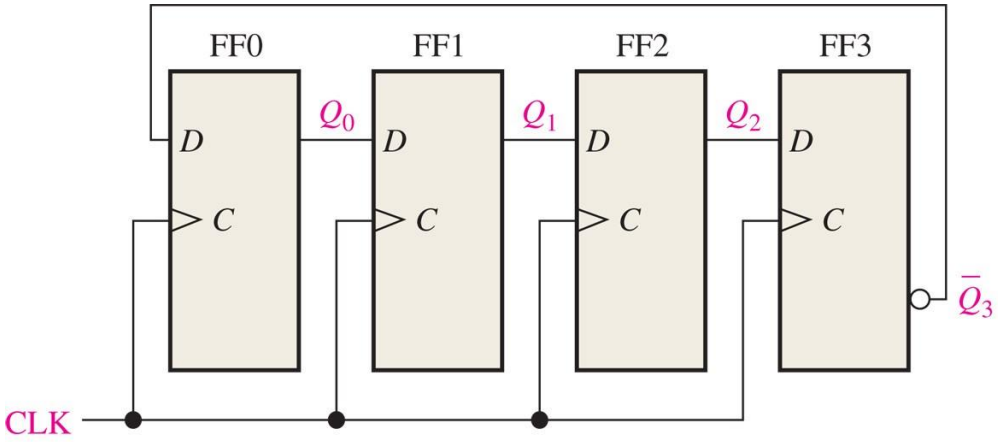
Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

TABLE 8–4

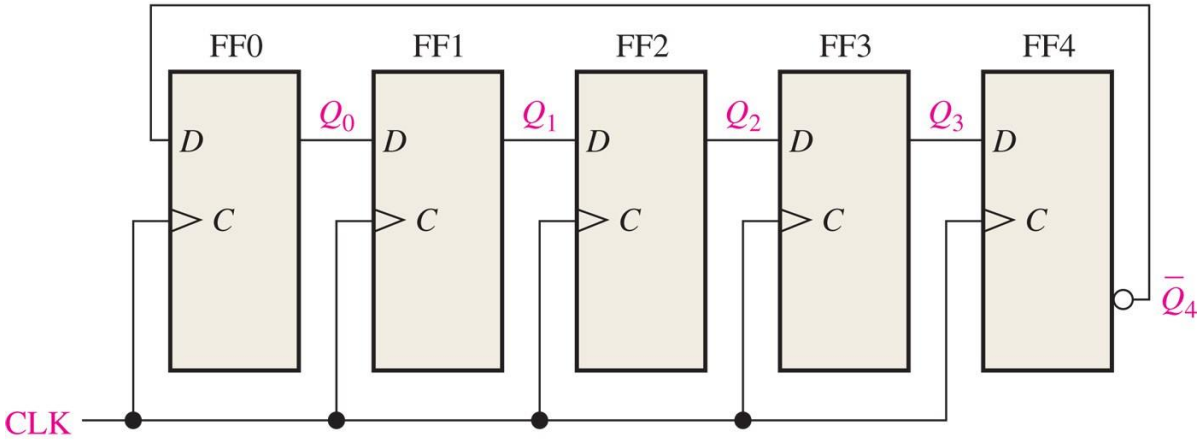
Five-bit Johnson sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

FIGURE 8-21 Four-bit and 5-bit Johnson counters.



(a) Four-bit Johnson counter



(b) Five-bit Johnson counter

FIGURE 8-22 Timing sequence for a 4-bit Johnson counter.

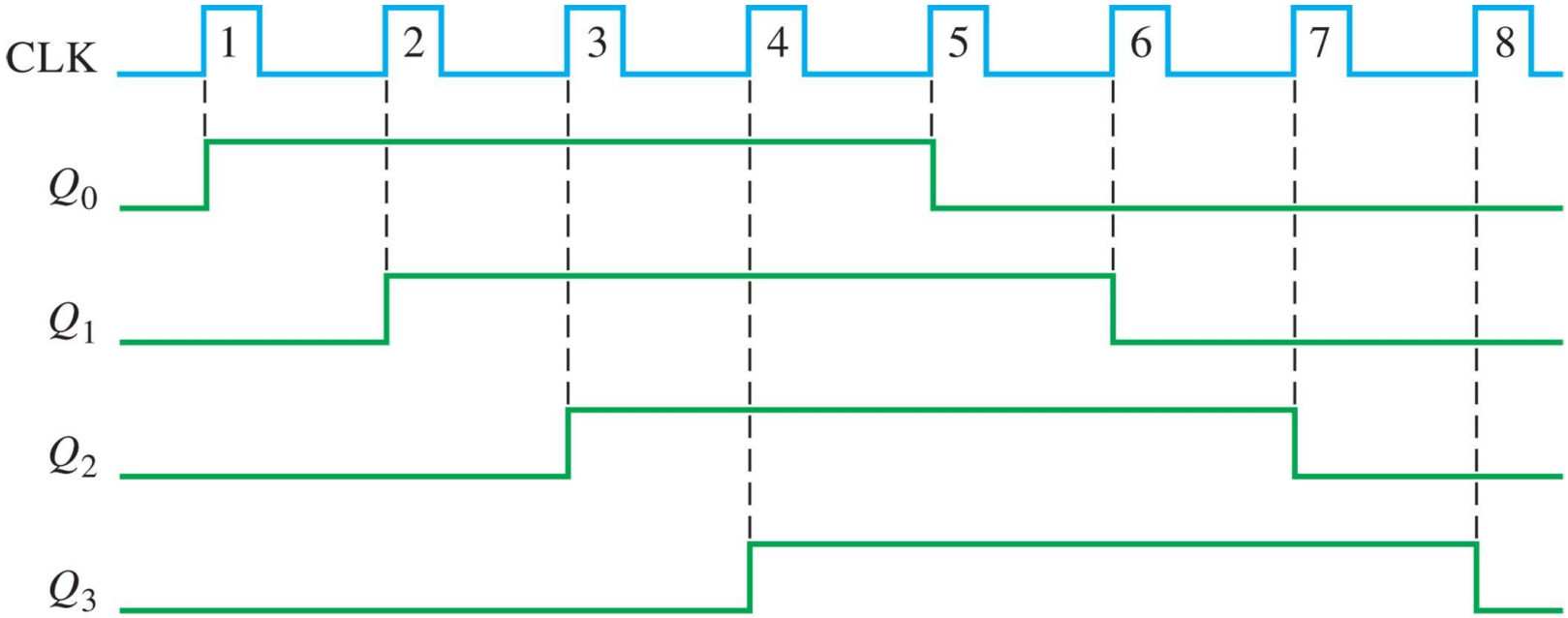


FIGURE 8-23 Timing sequence for a 5-bit Johnson counter.

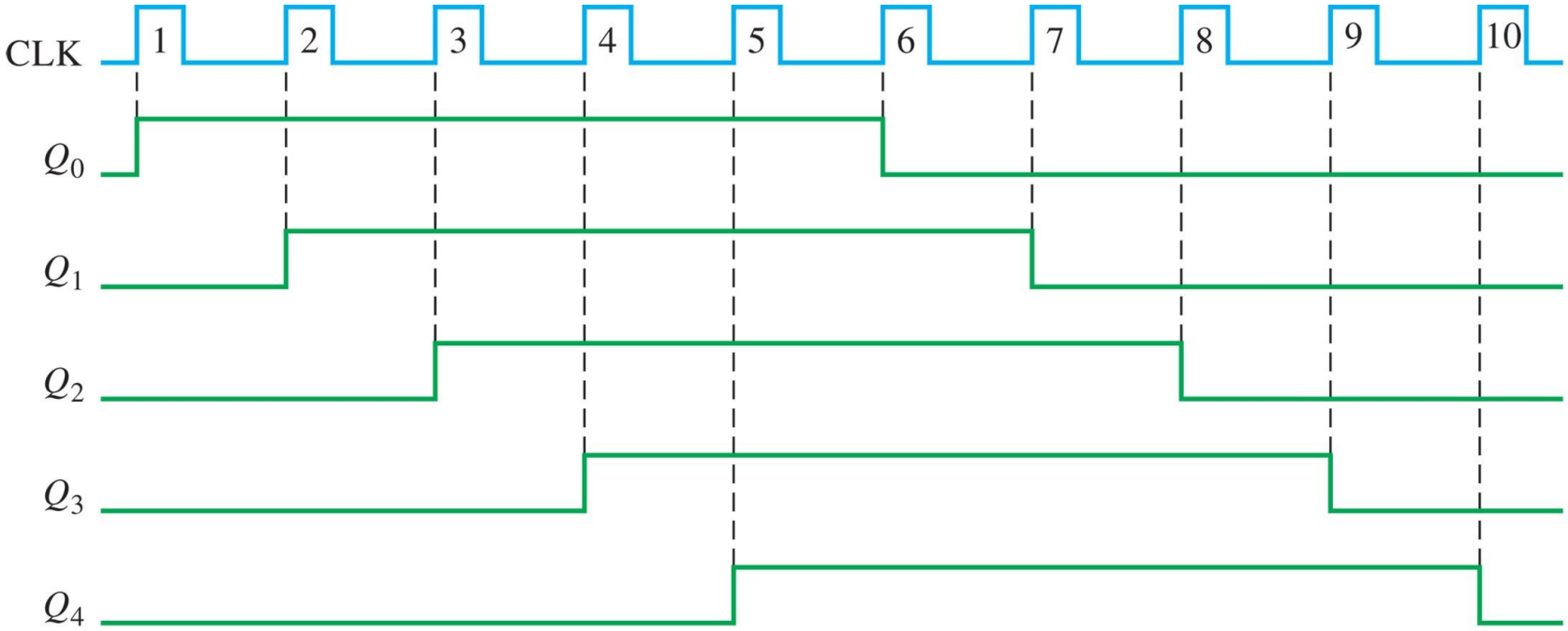


FIGURE 8-24 A 10-bit ring counter.

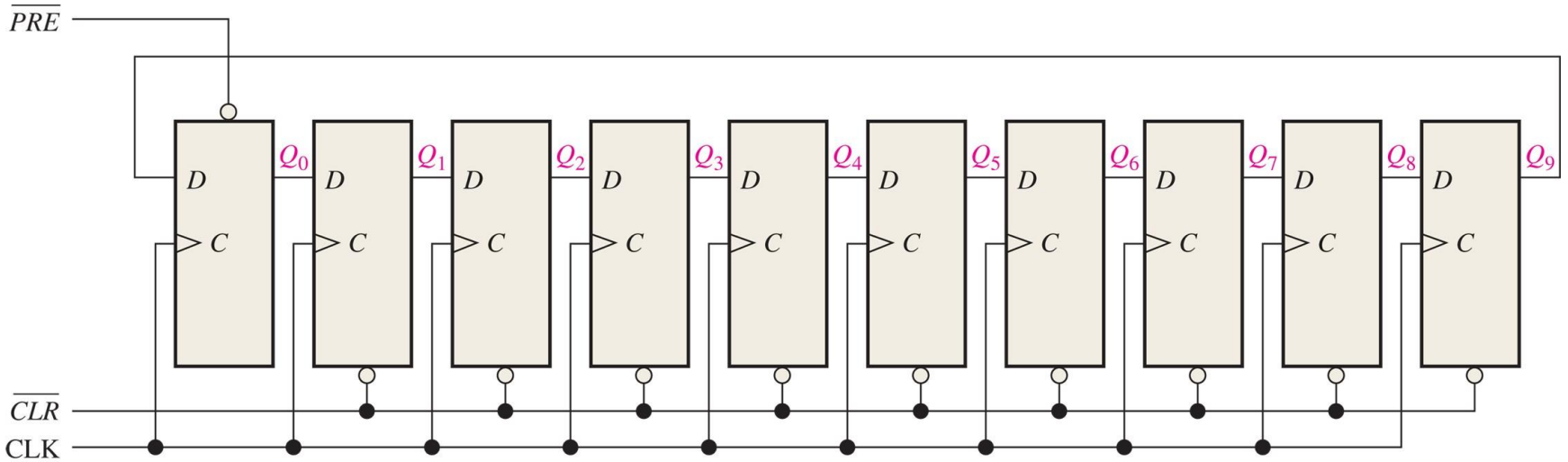


TABLE 8–5

Ten-bit ring counter sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

FIGURE 8-25

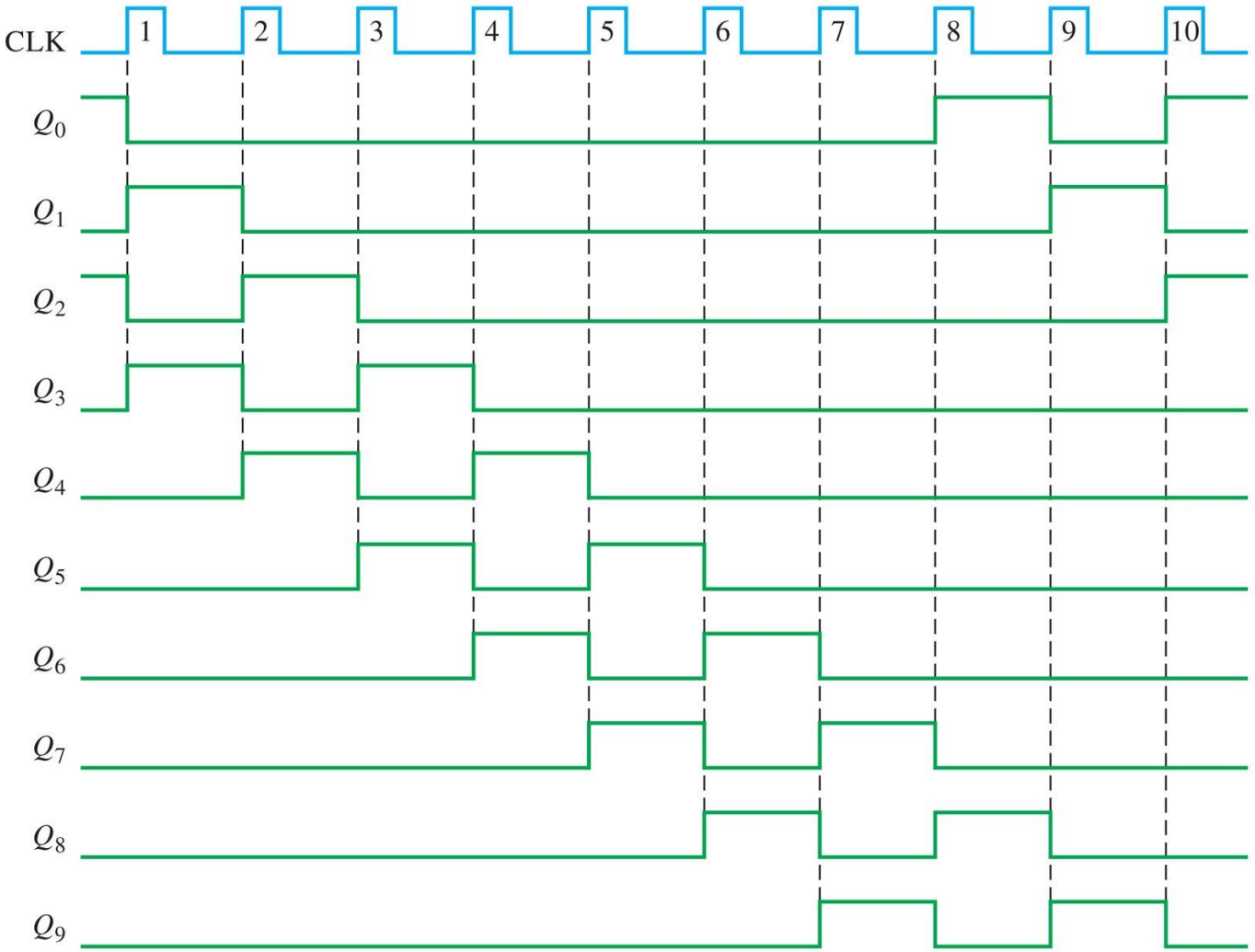


FIGURE 8-26 The shift register as a time-delay device.

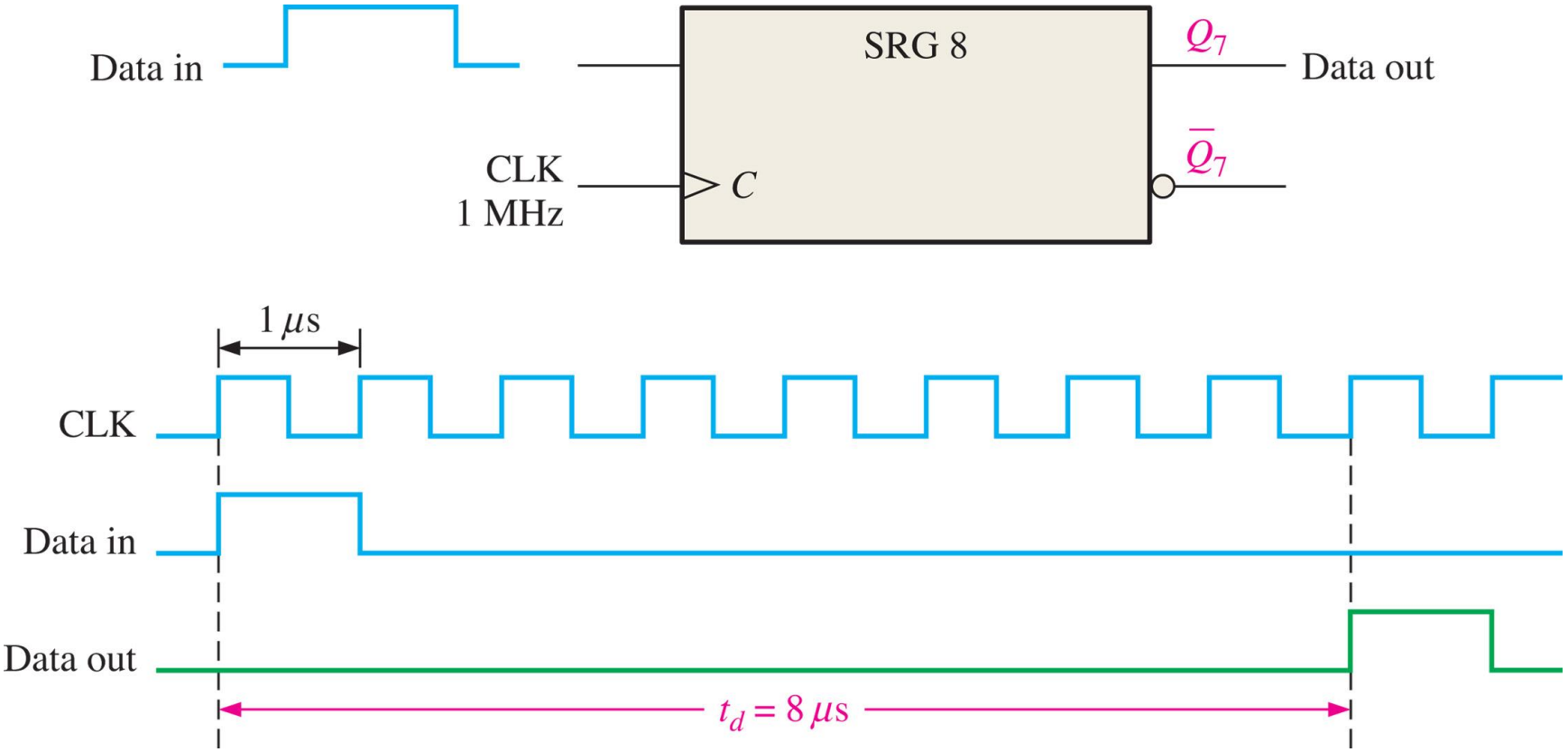
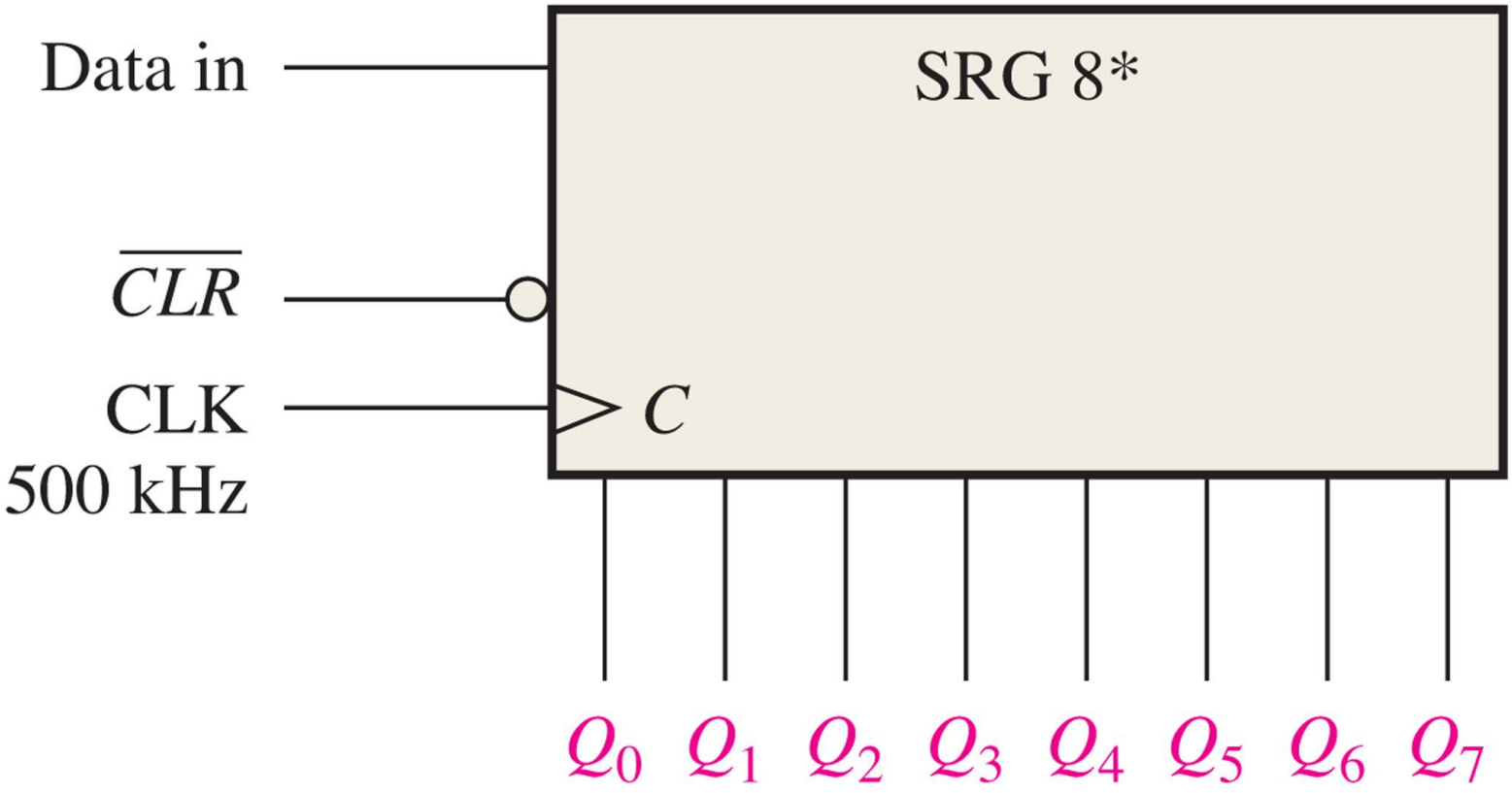


FIGURE 8-27



* Data shifts from Q_0 toward Q_7.

FIGURE 8-28 Timing diagram showing time delays for the register in Figure 8–27.

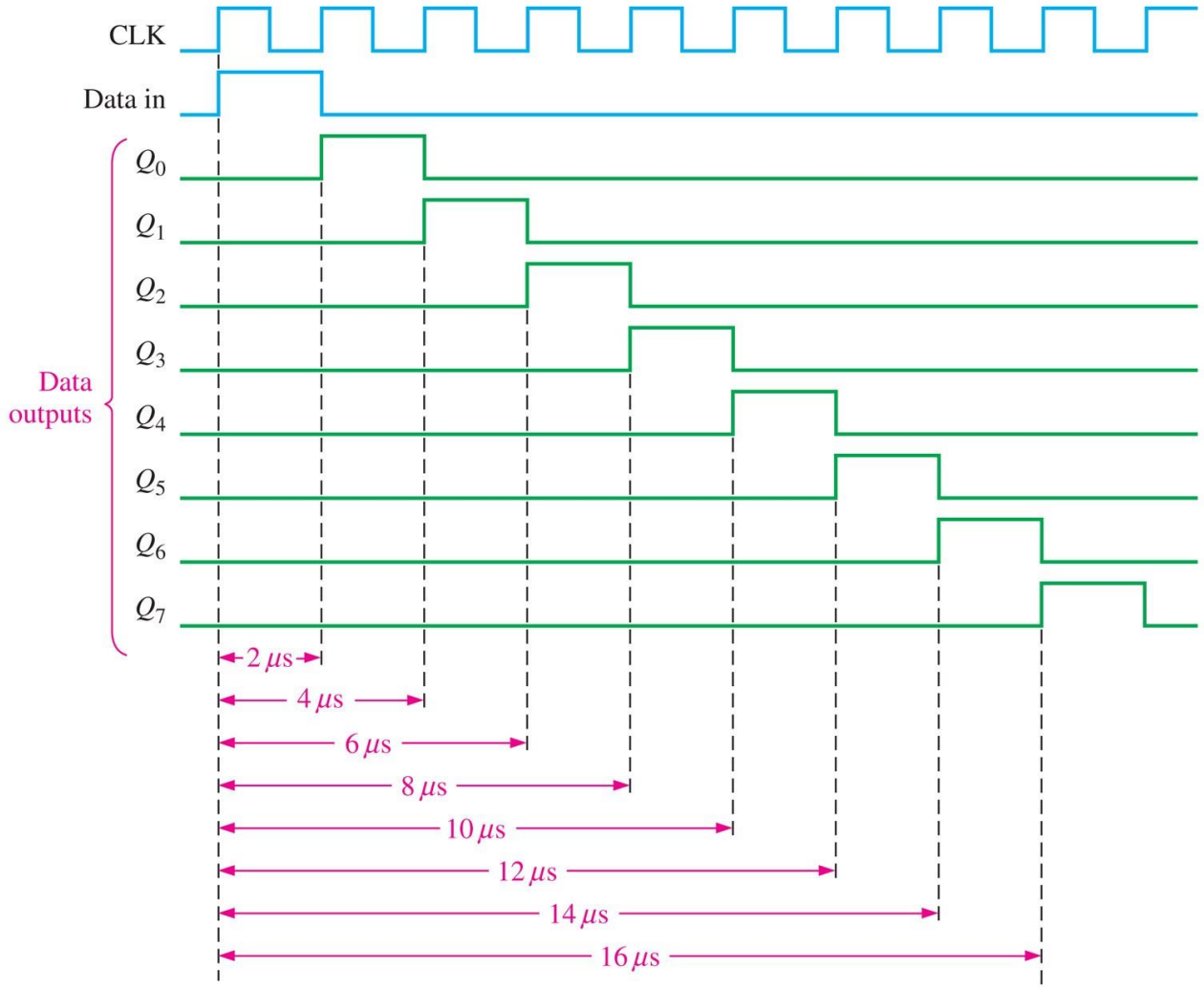


FIGURE 8-29 74HC195 connected as a ring counter.

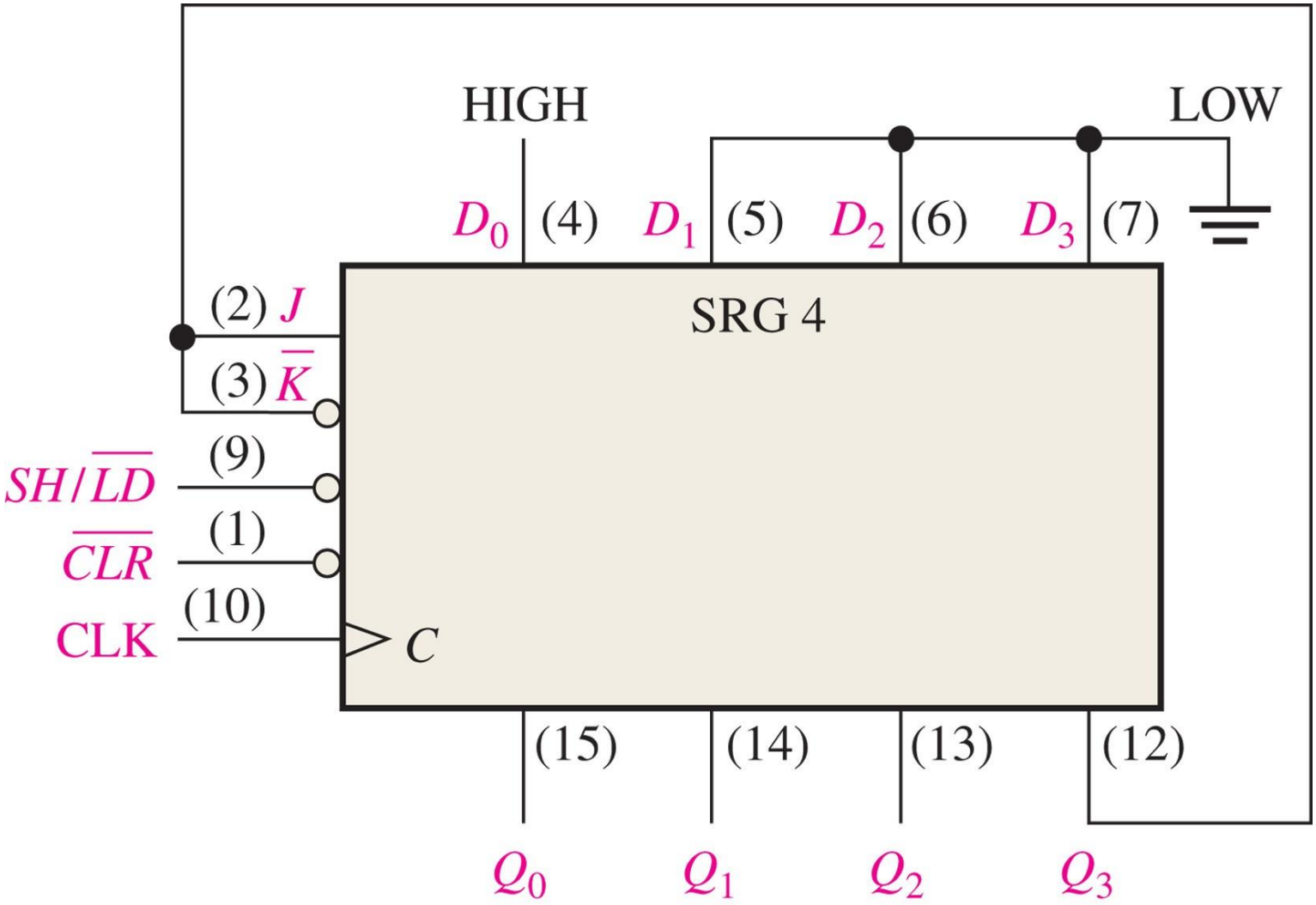


FIGURE 8-30 Timing diagram showing two complete cycles of the ring counter in Figure 8–29 when it is initially preset to 1000.