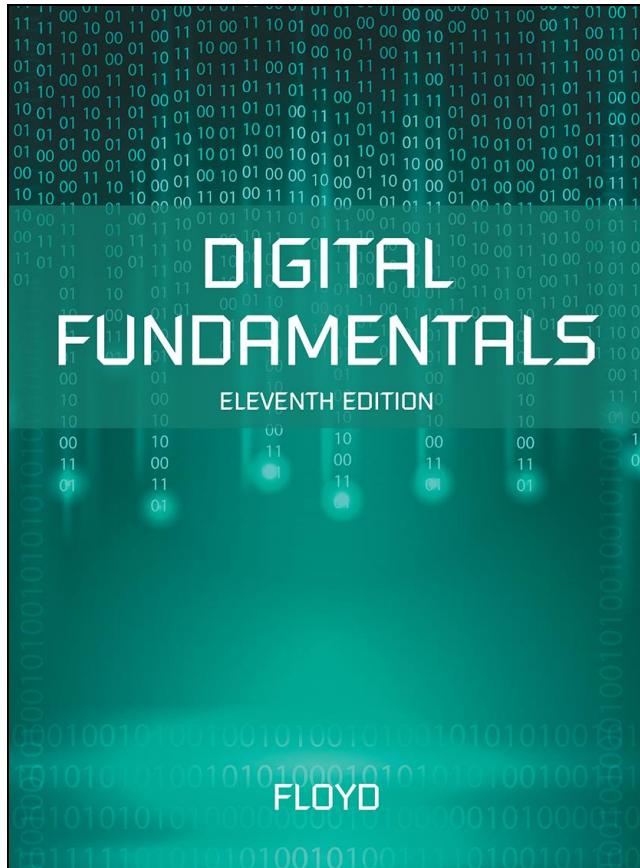


Digital Fundamentals

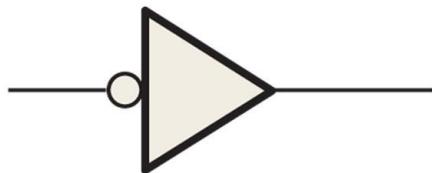
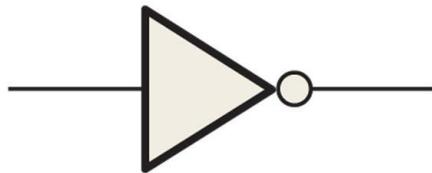
ELEVENTH EDITION



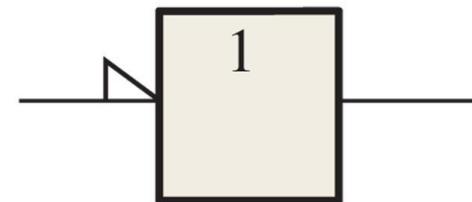
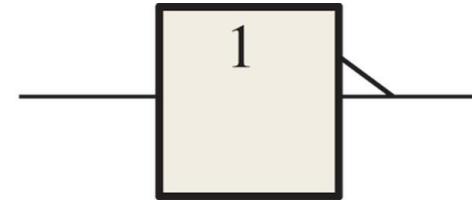
CHAPTER 3

Logic Gates

Standard logic symbols for the inverter (ANSI/IEEE Std. 91-1984/Std. 91a-1991)



(a) Distinctive shape symbols
with negation indicators



(b) Rectangular outline symbols
with polarity indicators

TABLE 3-1

Inverter truth table.

Input	Output
LOW (0)	HIGH (1)
HIGH (1)	LOW (0)

Inverter operation with a pulse input

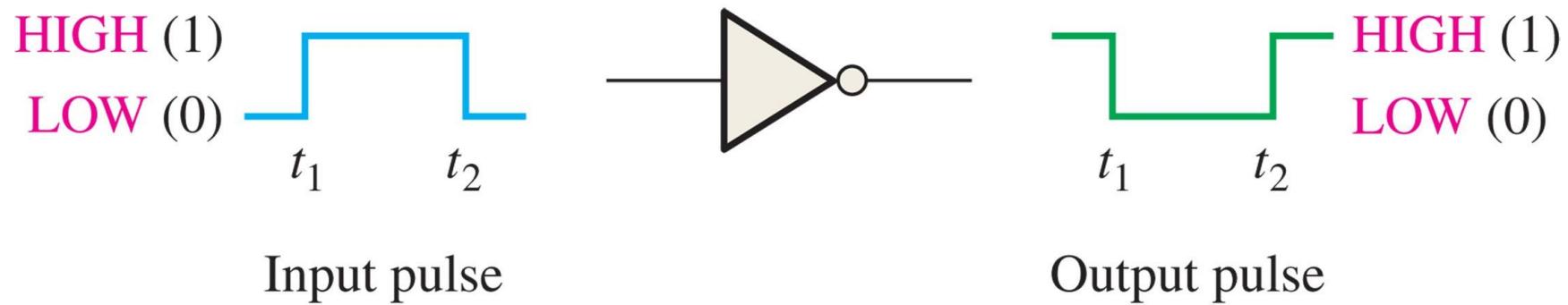
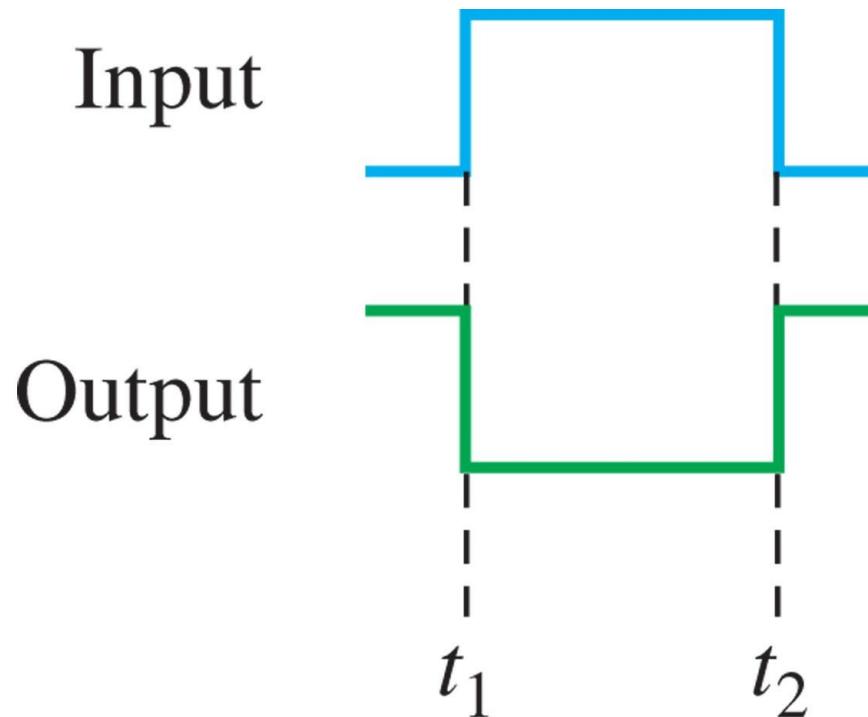


FIGURE 3-3 Timing diagram for the case in Figure 3-2.



Inverter

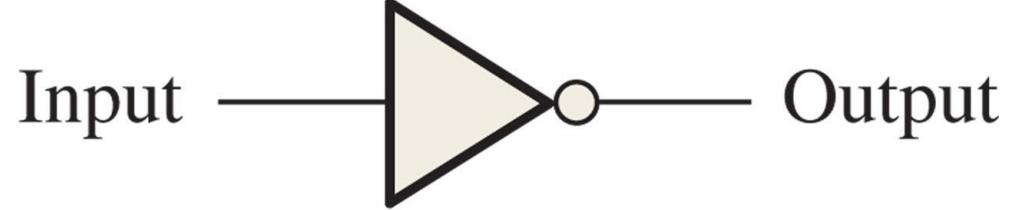
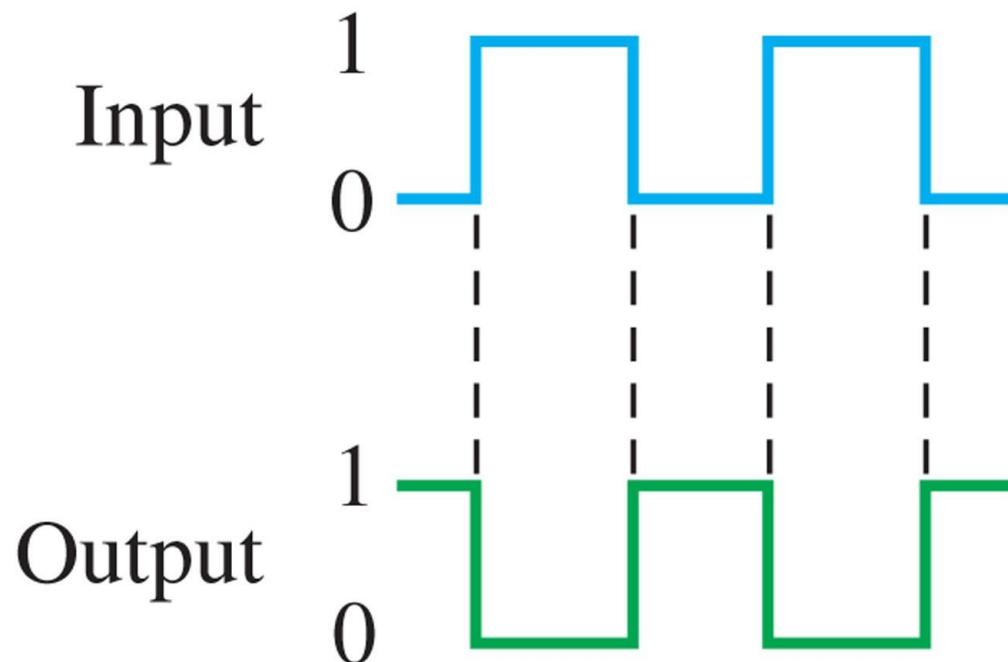
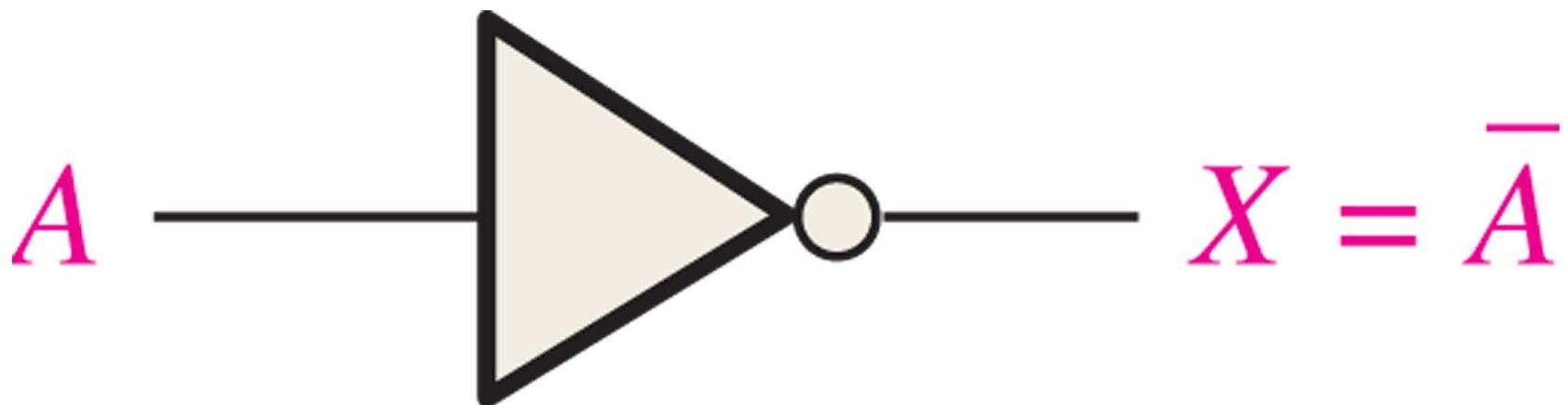


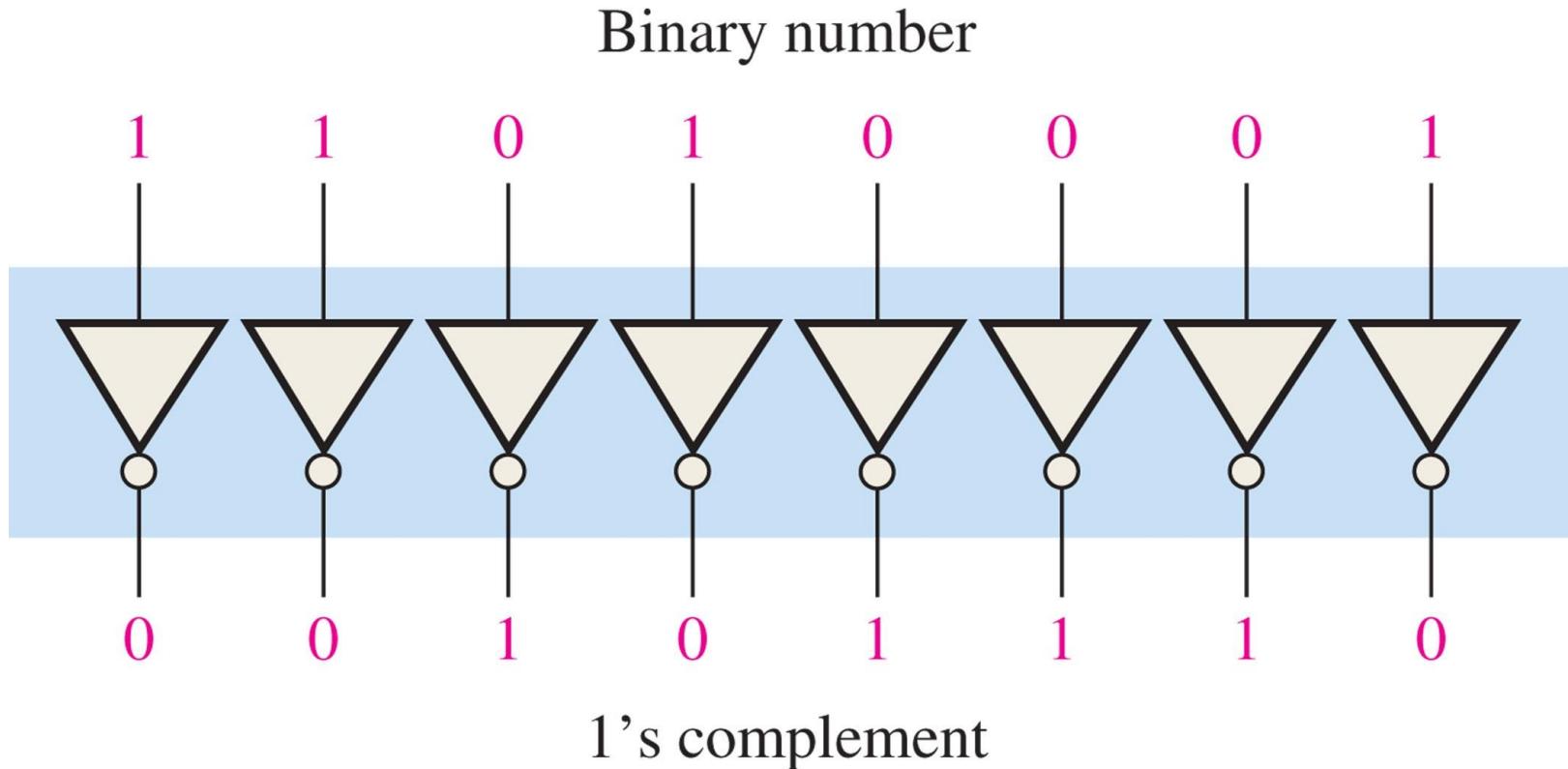
FIGURE 3-5



The inverter complements an input variable



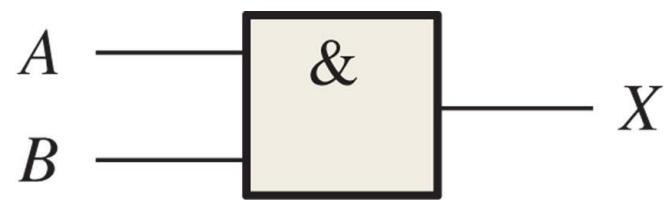
Example of a 1's complement circuit using inverters



Standard logic symbols for the AND gate showing two inputs



(a) Distinctive shape



(b) Rectangular outline with the
AND (&) qualifying symbol

All possible logic levels for a 2-input AND gate

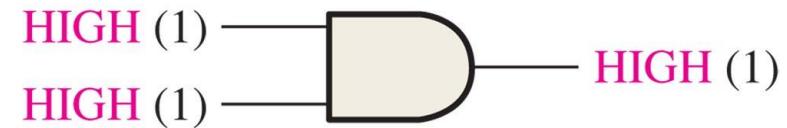
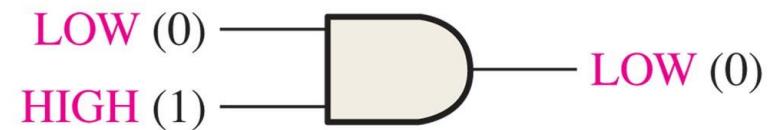
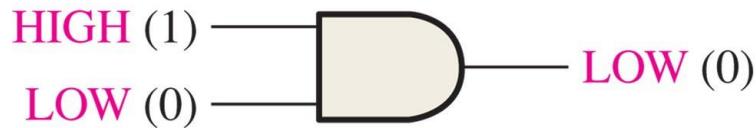
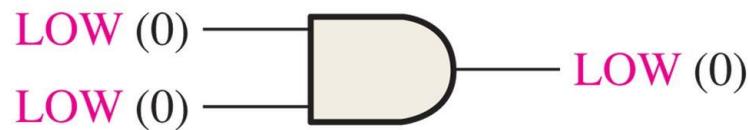


TABLE 3–2

Truth table for a 2-input AND gate.

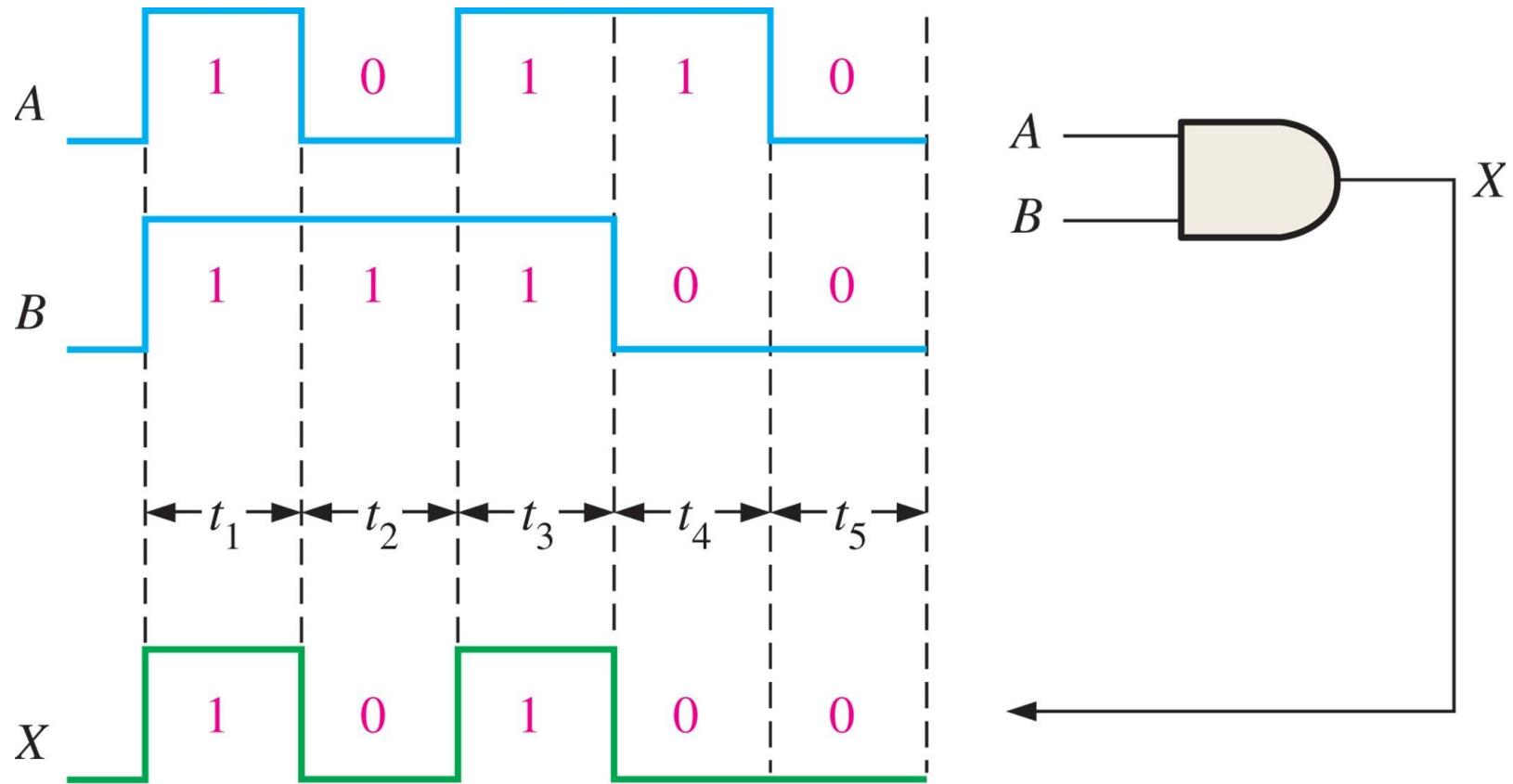
Inputs		Output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

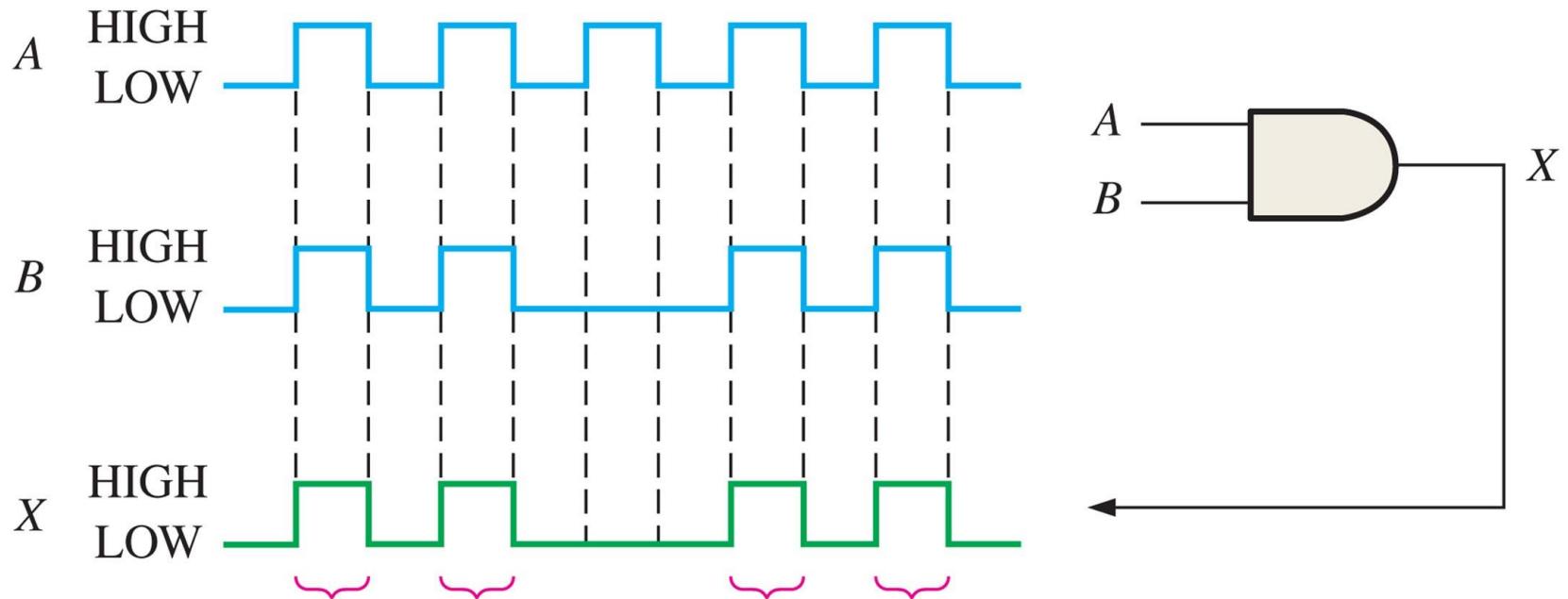
1 = HIGH, 0 = LOW

TABLE 3–3

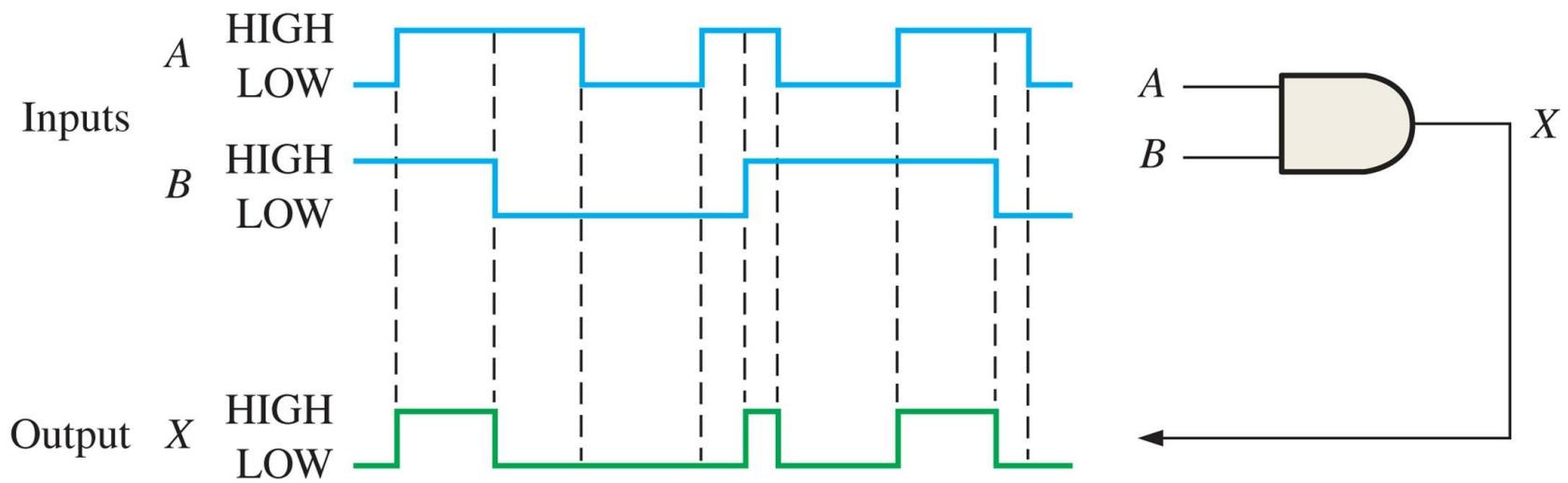
Inputs			Output
<i>A</i>	<i>B</i>	<i>C</i>	<i>X</i>
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

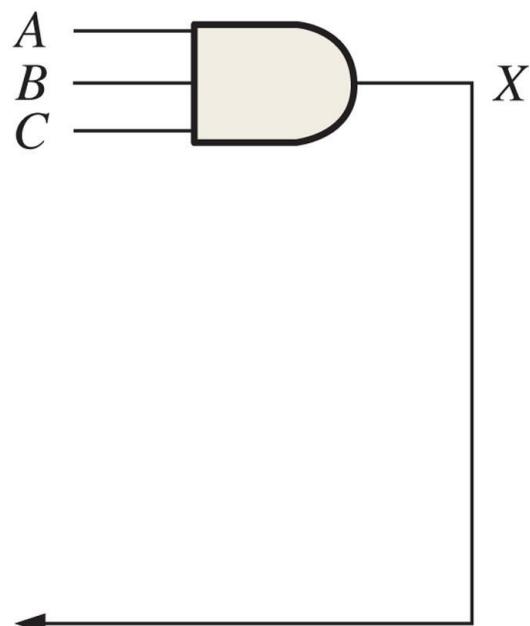
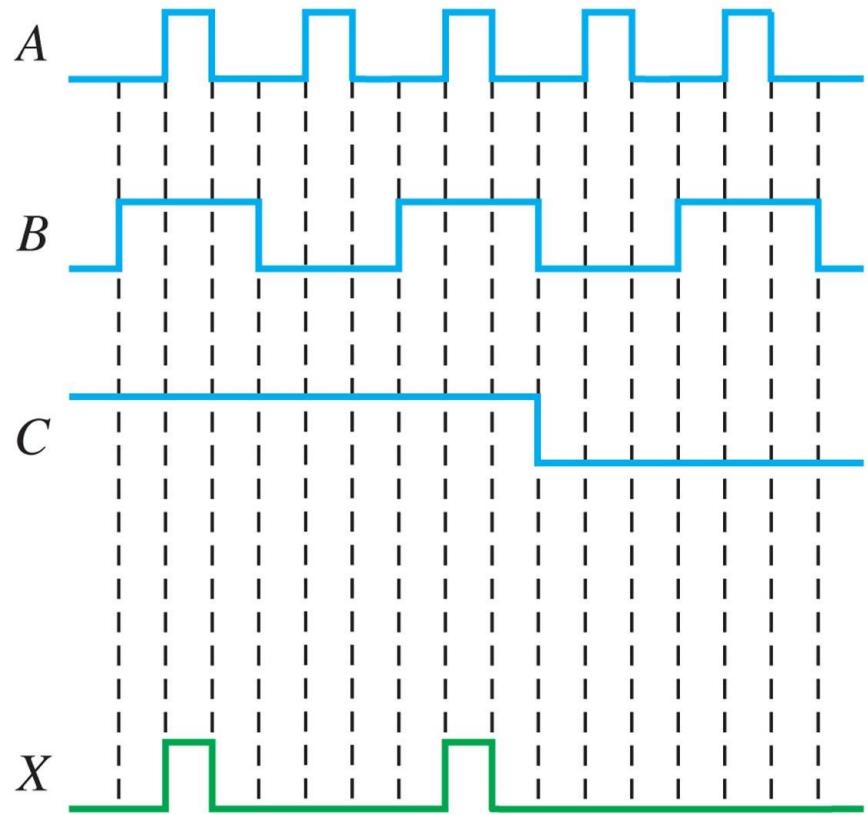
Example of AND gate operation with a timing diagram showing input and output relationships





A and *B* are both HIGH during these four time intervals; therefore, *X* is HIGH.





Boolean expressions for AND gates with two, three, and four inputs

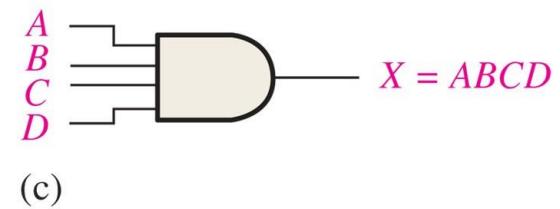
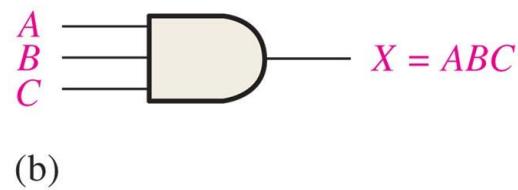
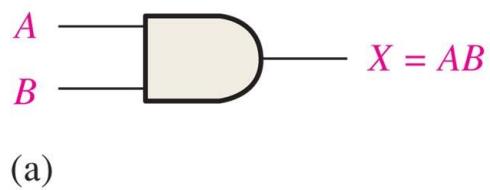
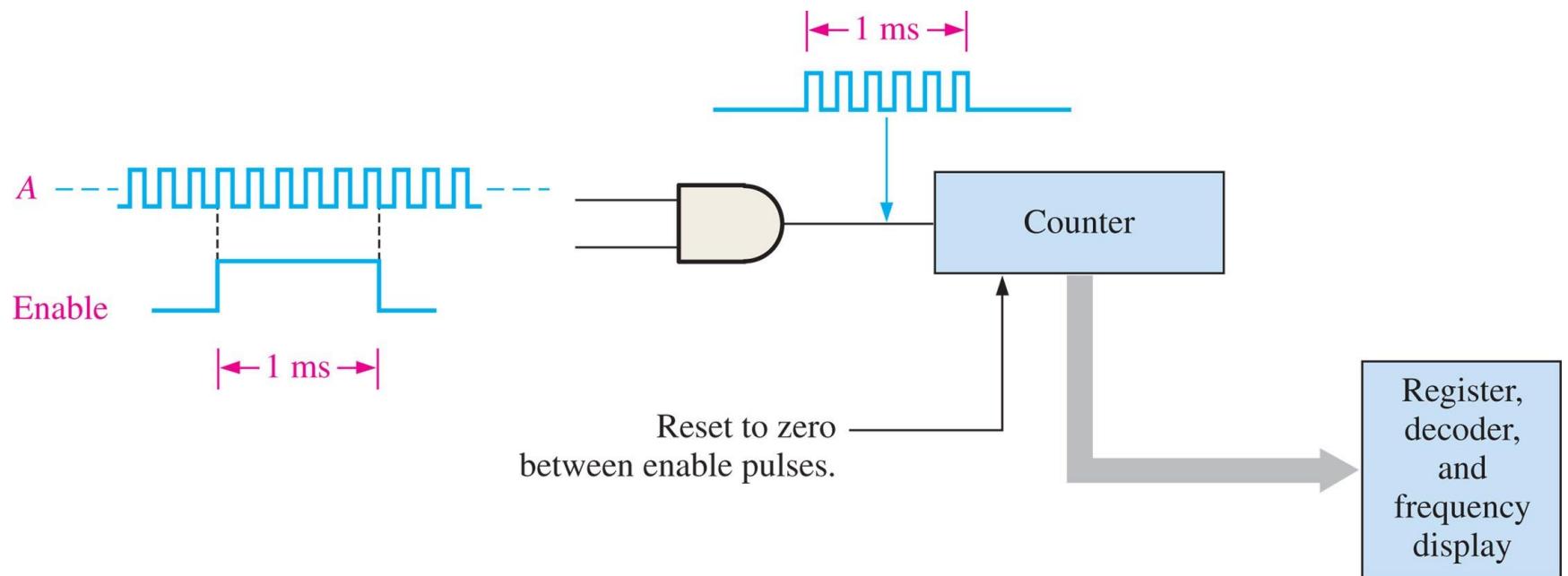


TABLE 3-4

A	B	$AB = X$
0	0	$0 \cdot 0 = 0$
0	1	$0 \cdot 1 = 0$
1	0	$1 \cdot 0 = 0$
1	1	$1 \cdot 1 = 1$

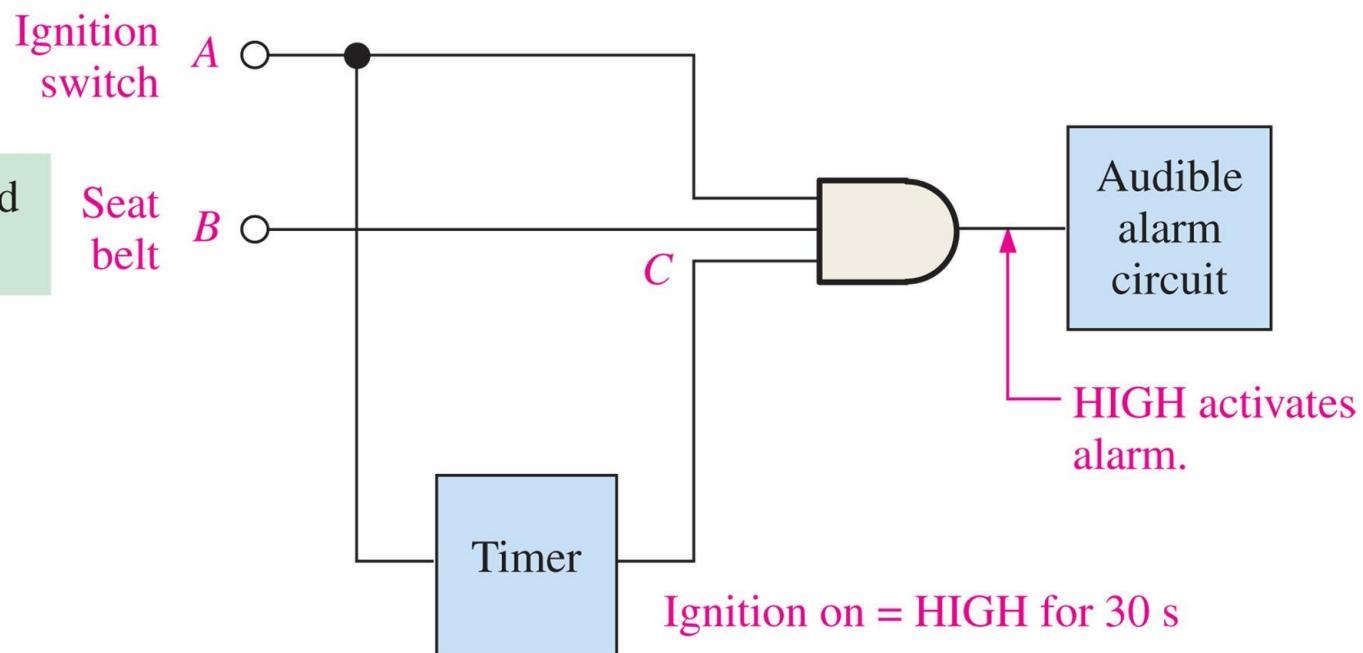
An AND gate performing an enable/inhibit function for a frequency counter



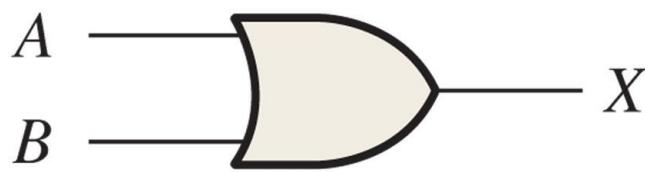
A simple seat belt alarm circuit using an AND gate

HIGH = On
LOW = Off

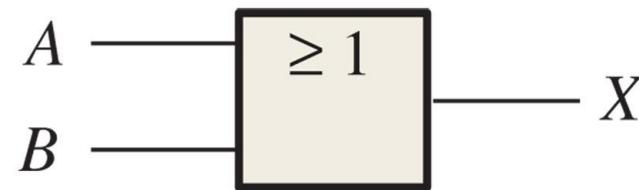
HIGH = Unbuckled
LOW = Buckled



Standard logic symbols for the OR gate showing two inputs



(a) Distinctive shape



(b) Rectangular outline with the OR (≥ 1) qualifying symbol

All possible logic levels for a 2-input OR gate

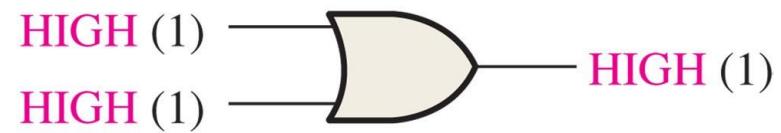
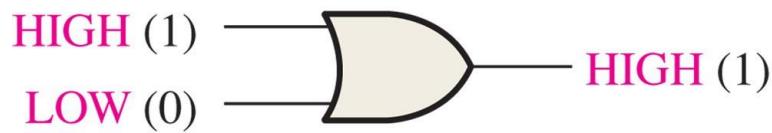
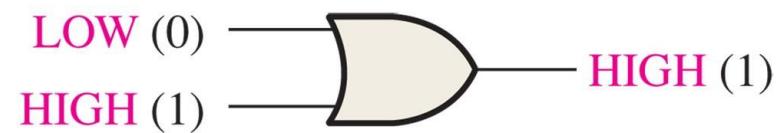
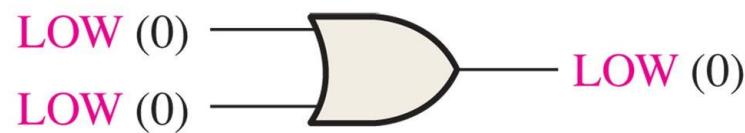


TABLE 3–5

Truth table for a 2-input OR gate.

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

1 = HIGH, 0 = LOW

Example of OR gate operation with a timing diagram showing input and output time relationships

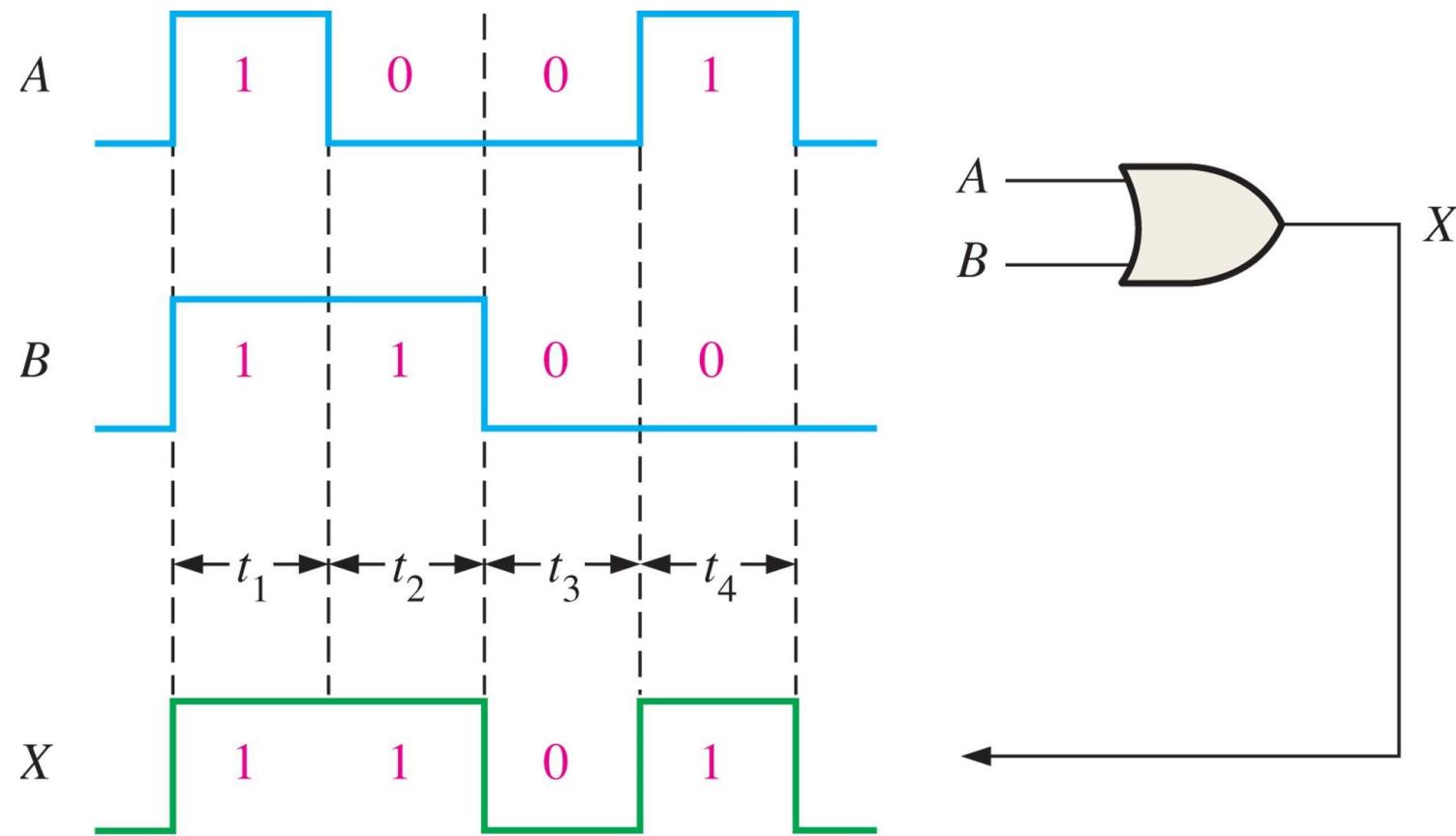
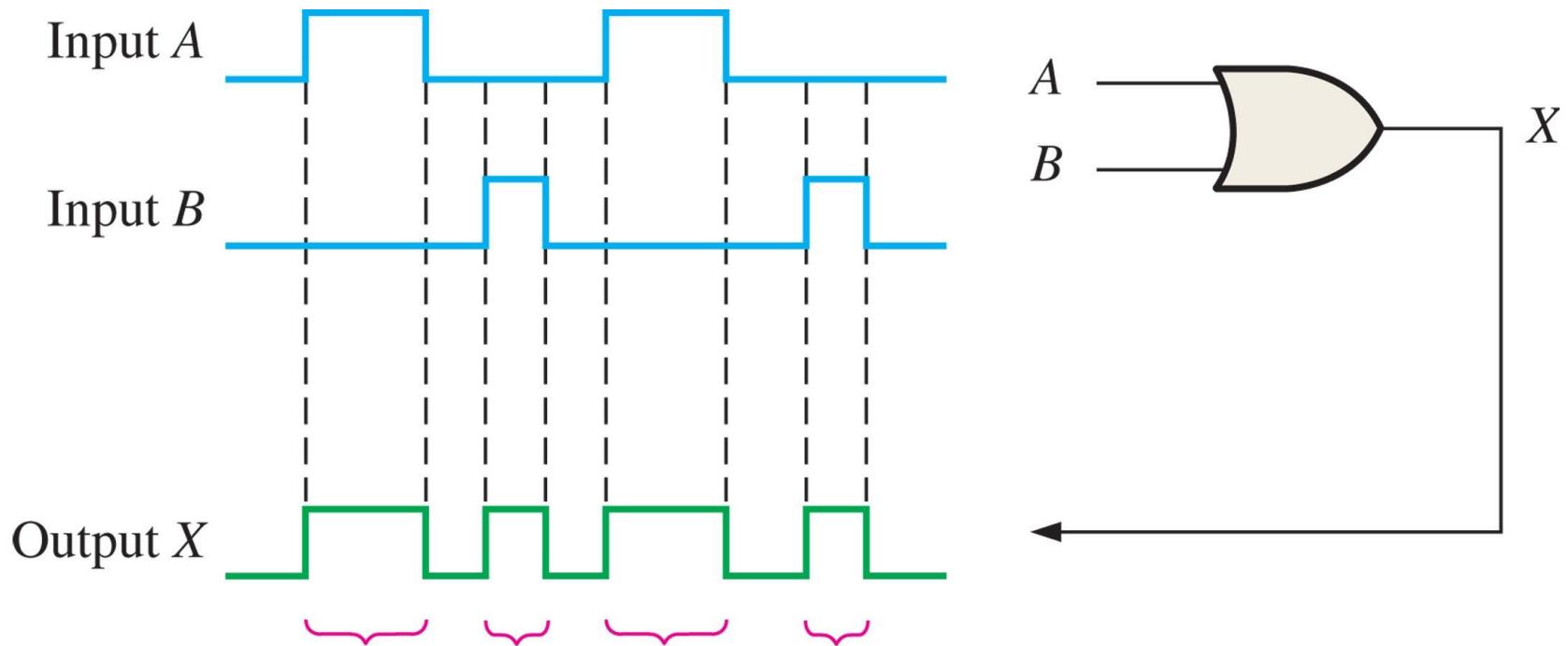


FIGURE 3-21



When either input or both inputs are HIGH,
the output is HIGH.

FIGURE 3-22

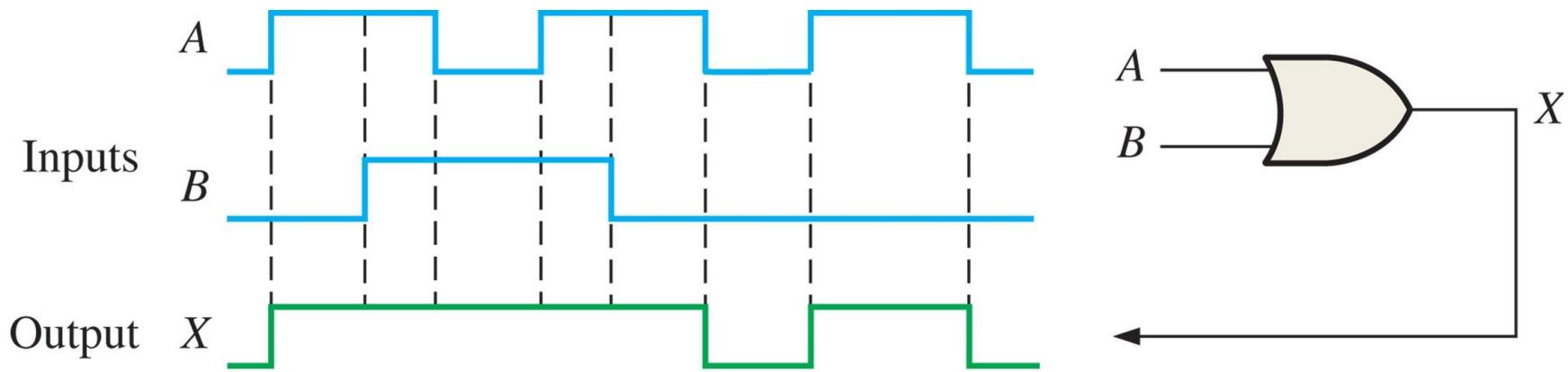
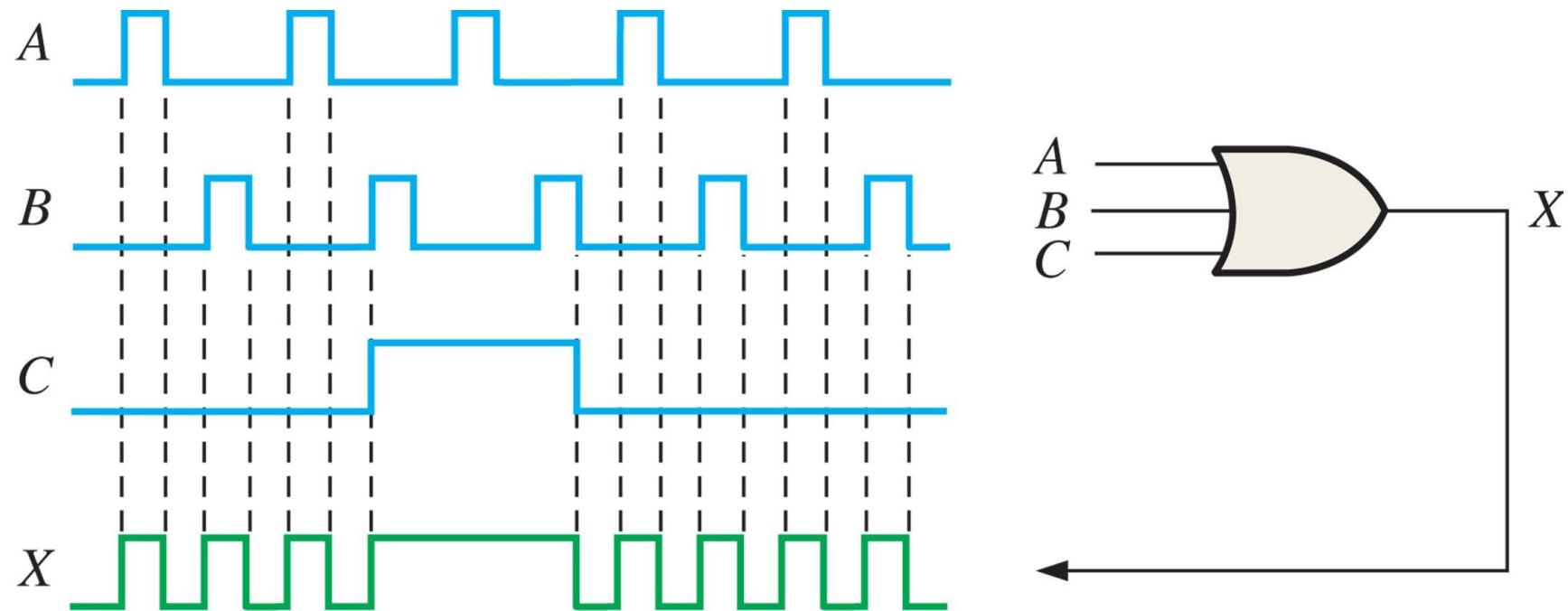
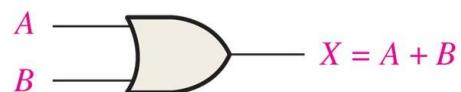


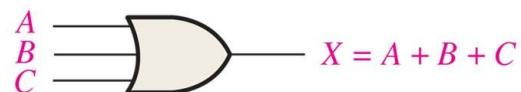
FIGURE 3-23



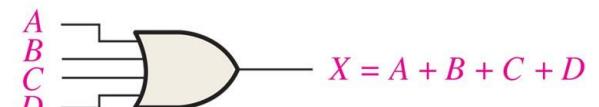
Boolean expressions for OR gates with two, three, and four inputs



(a)



(b)



(c)

TABLE 3–6

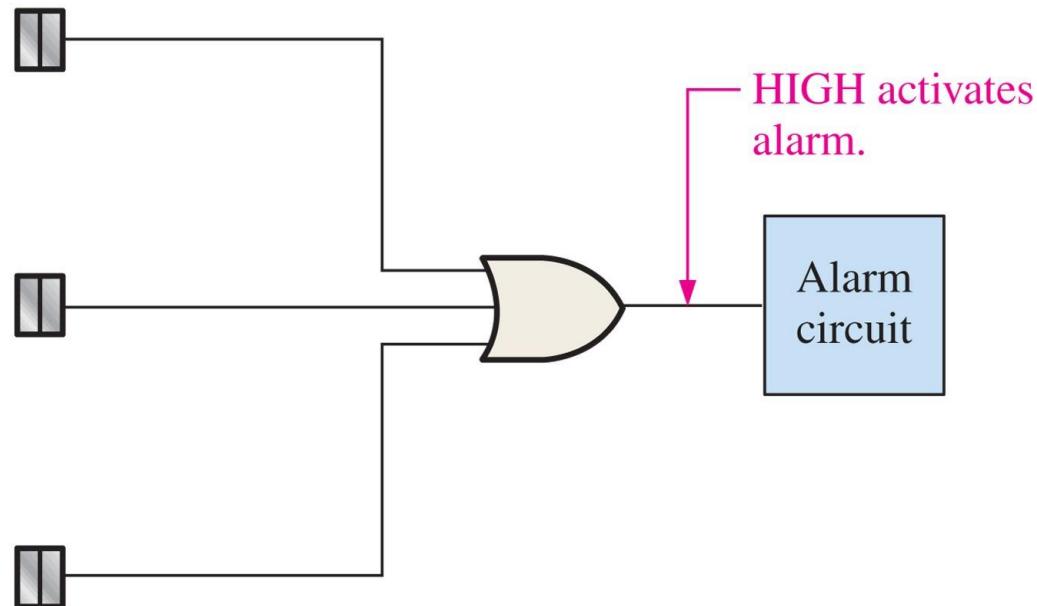
A	B	$A + B = X$
0	0	$0 + 0 = 0$
0	1	$0 + 1 = 1$
1	0	$1 + 0 = 1$
1	1	$1 + 1 = 1$

A simplified intrusion detection system using an OR gate.

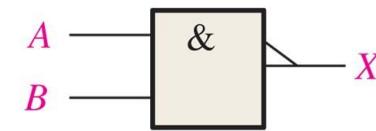
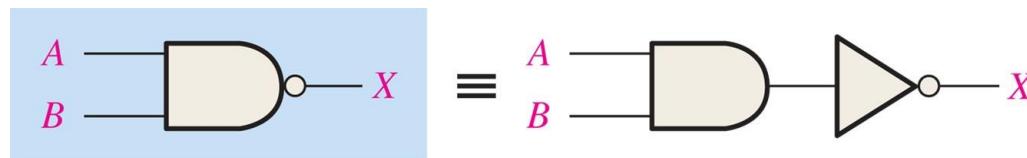
This system could be used for one room in a home—a room with two windows and a door. The sensors are magnetic switches that produce a HIGH output when open and a LOW output when closed. As long as the windows and the door are secured, the switches are closed and all three of the OR gate inputs are LOW. When one of the windows or the door is opened, a HIGH is produced on that input to the OR gate and the gate output goes HIGH. It then activates and latches an alarm circuit to warn of the intrusion.

Open door/window
sensors

HIGH = Open
LOW = Closed



Standard NAND gate logic symbols



(b) Rectangular outline, 2-input NAND gate with polarity indicator

TABLE 3–7

Truth table for a 2-input
NAND gate.

Inputs		Output
<i>A</i>	<i>B</i>	<i>X</i>
<hr/>		
0	0	1
0	1	1
1	0	1
1	1	0
<hr/>		

1 = HIGH, 0 = LOW.

Operation of a 2-input NAND gate

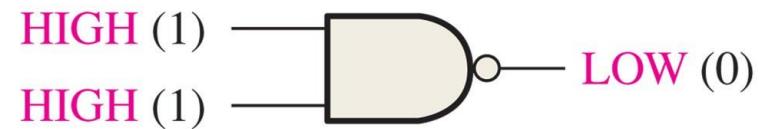
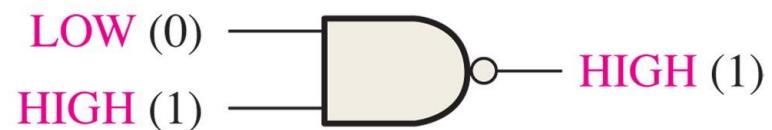
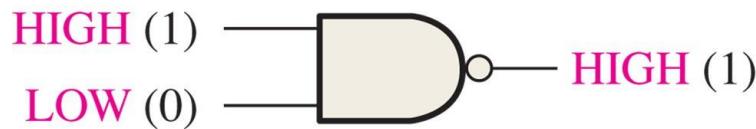
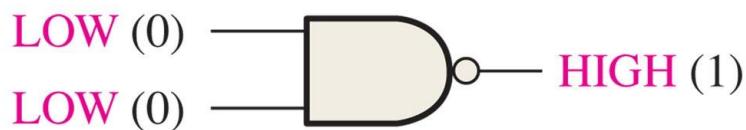
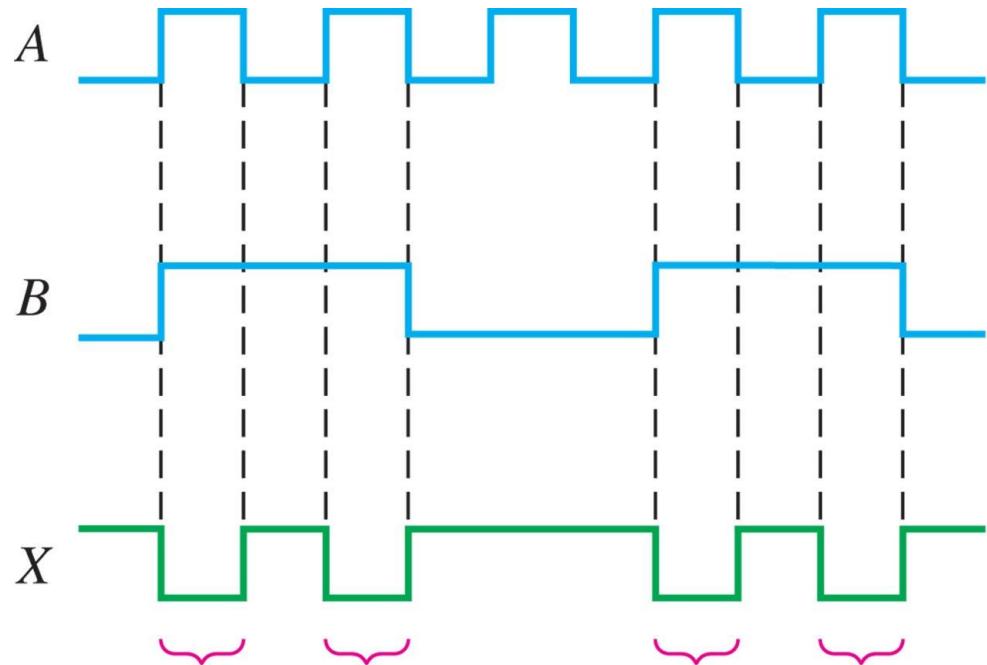
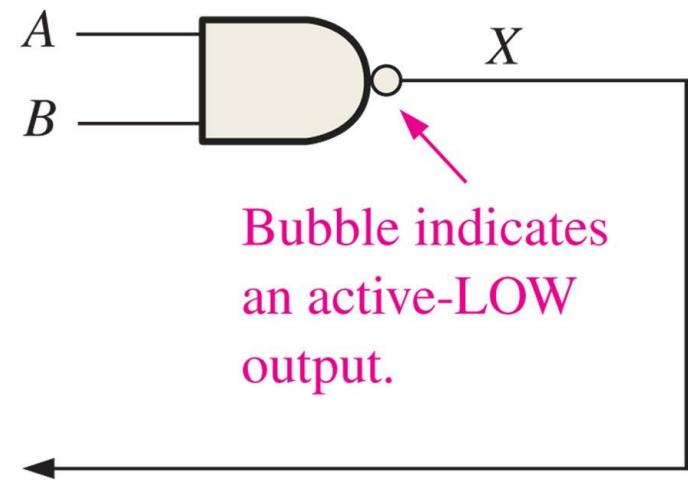


FIGURE 3-28



A and *B* are both HIGH during these four time intervals; therefore, *X* is LOW.



Bubble indicates
an active-LOW
output.

FIGURE 3-29

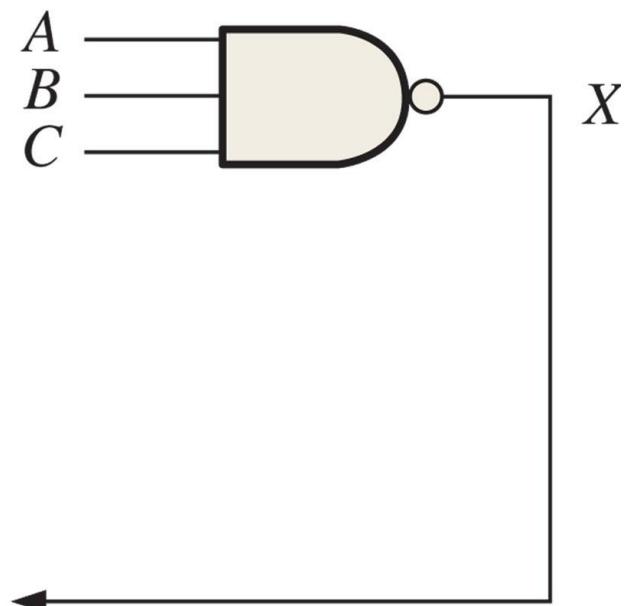
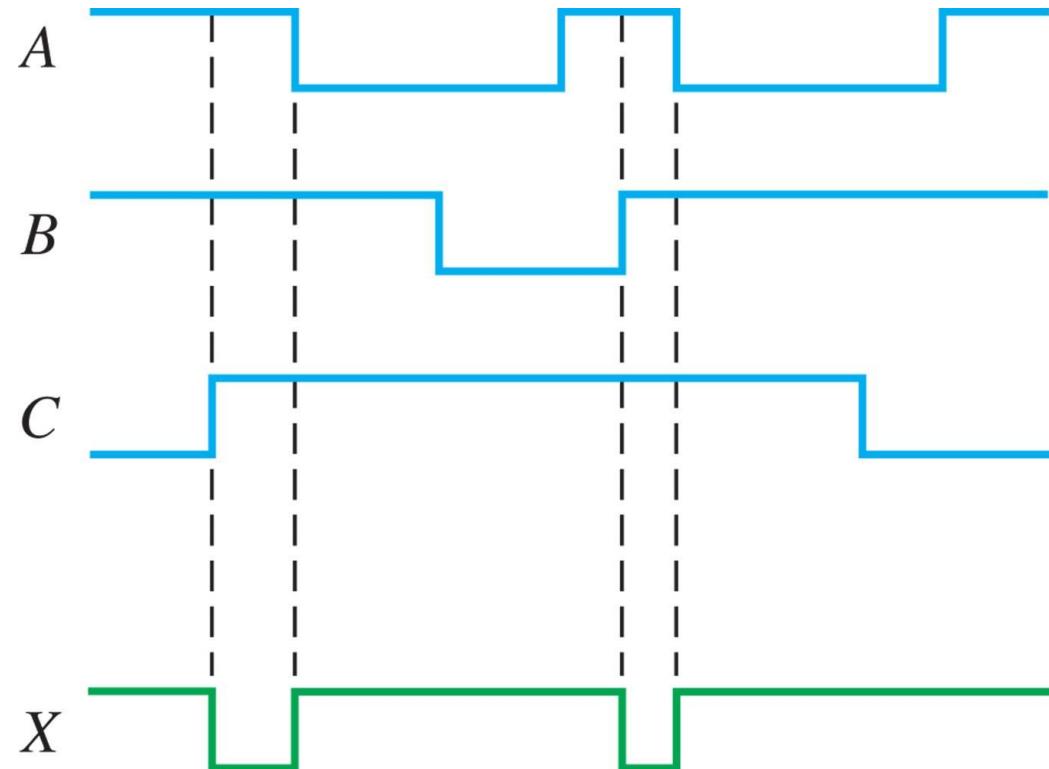
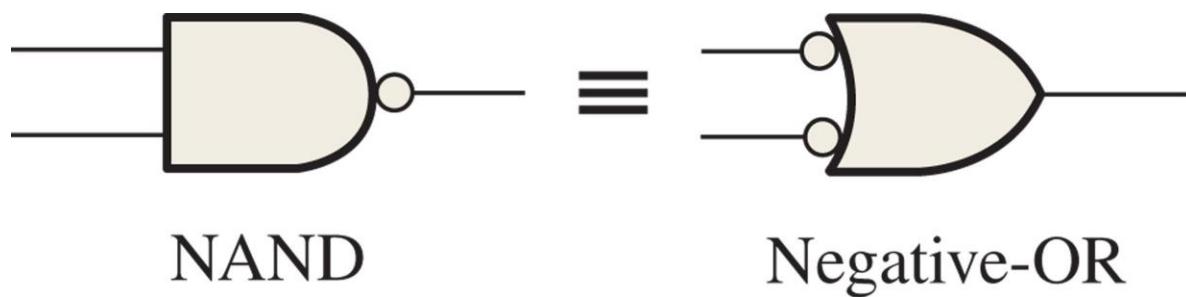
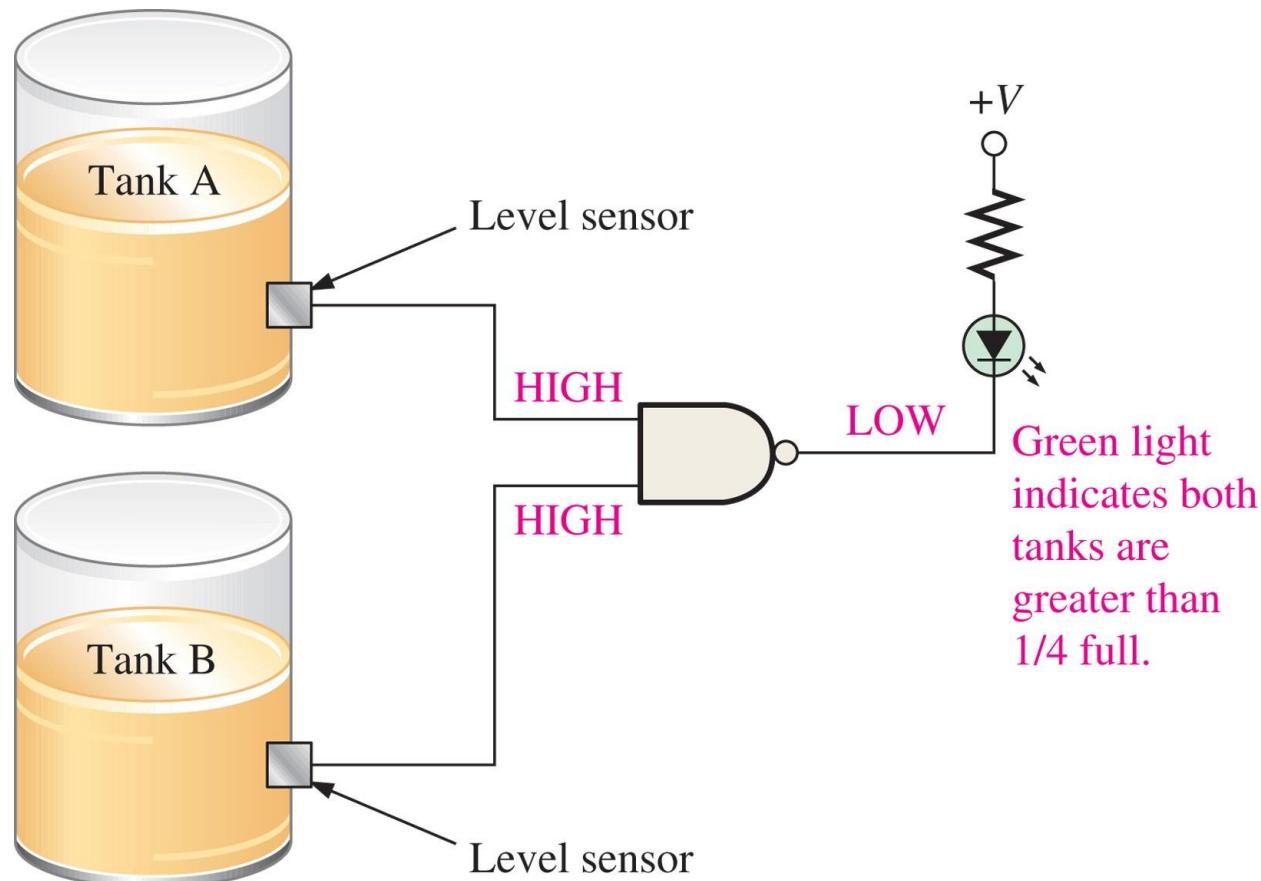


FIGURE 3-30 ANSI/IEEE standard symbols representing the two equivalent operations of a NAND gate.



Two tanks store certain liquid chemicals that are required in a manufacturing process. Each tank has a sensor that detects when the chemical level drops to 25% of full. The sensors produce a HIGH level of 5 V when the tanks are more than one-quarter full. When the volume of chemical in a tank drops to one-quarter full, the sensor puts out a LOW level of 0 V. It is required that a single green light-emitting diode (LED) on an indicator panel show when both tanks are more than one-quarter full. Show how a NAND gate can be used to implement this function.

FIGURE 3-31



it has been decided to have a red LED display come on when at least one of the tanks falls to the quarter-full level rather than have the green LED display indicate when both are above one quarter. Show how this requirement can be implemented

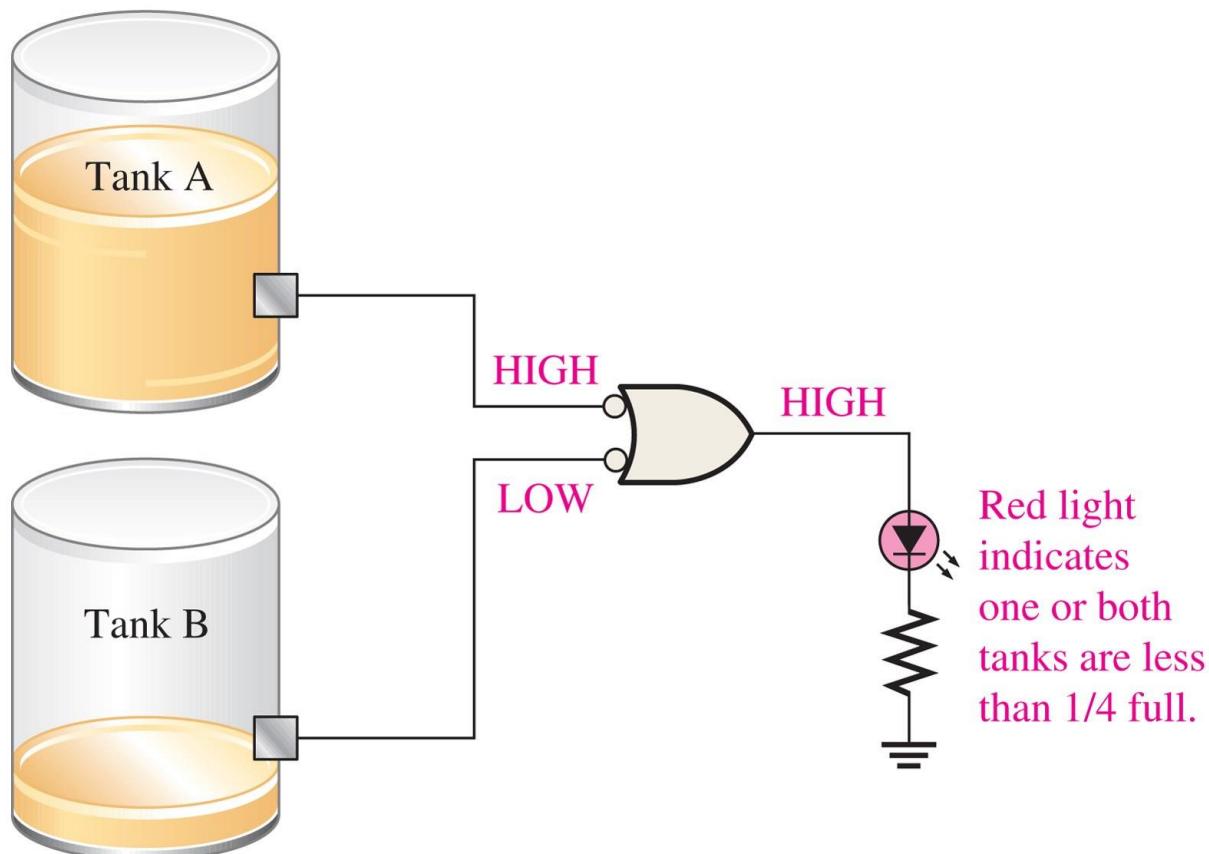
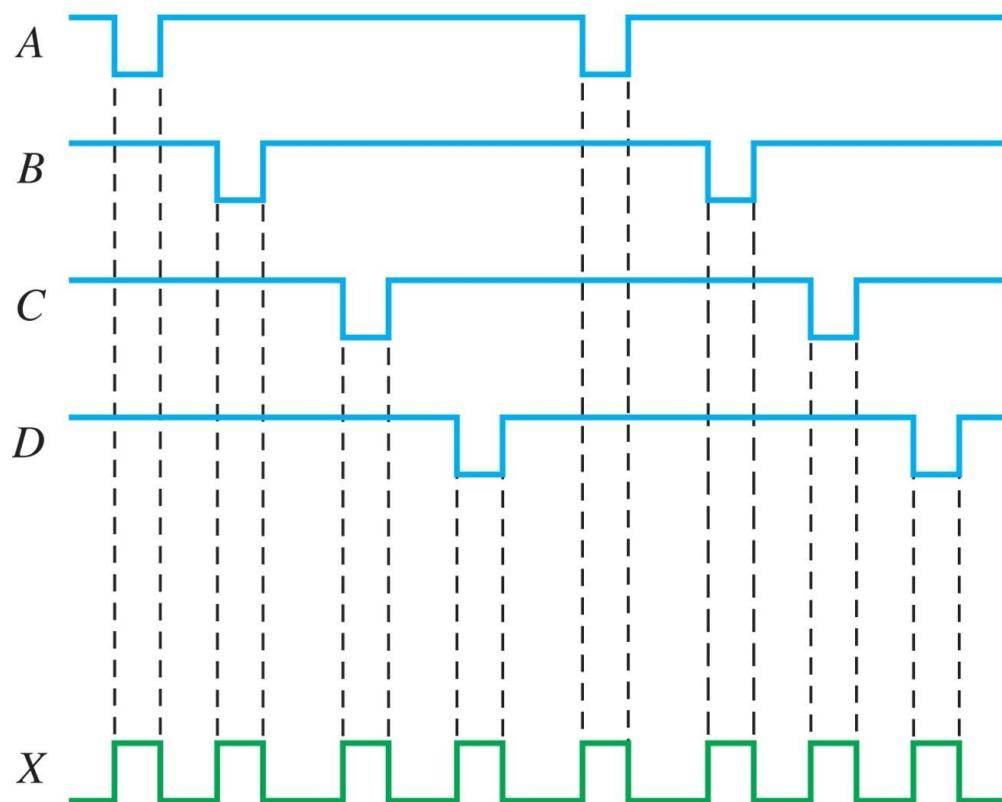


FIGURE 3-33



Bubbles indicate
active-LOW inputs.

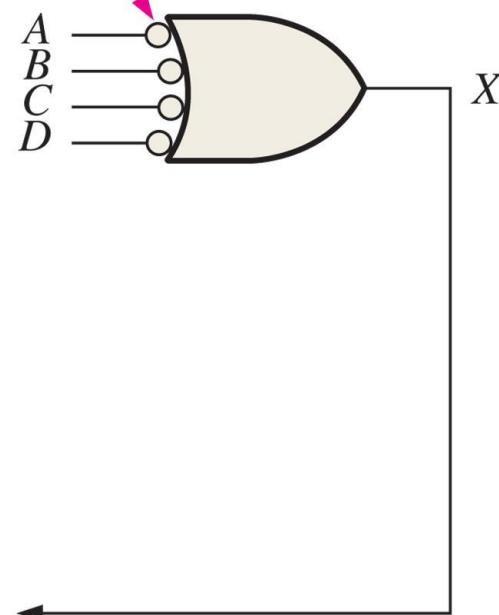
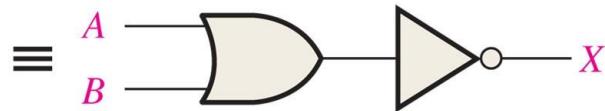
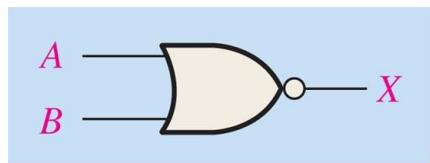


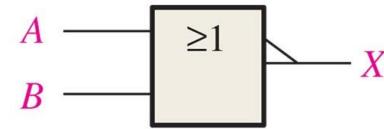
TABLE 3–8

A	B	$\overline{AB} = X$
0	0	$\overline{0 \cdot 0} = \overline{0} = 1$
0	1	$\overline{0 \cdot 1} = \overline{0} = 1$
1	0	$\overline{1 \cdot 0} = \overline{0} = 1$
1	1	$\overline{1 \cdot 1} = \overline{1} = 0$

Standard NOR gate logic symbols



(a) Distinctive shape, 2-input NOR gate and its NOT/OR equivalent



(b) Rectangular outline, 2-input NOR gate with polarity indicator

Operation of a 2-input NOR gate

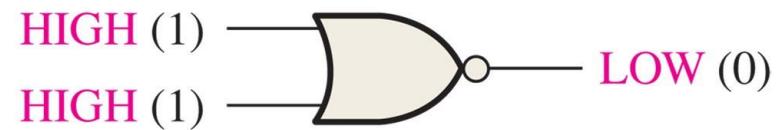
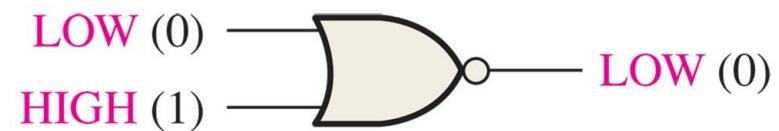
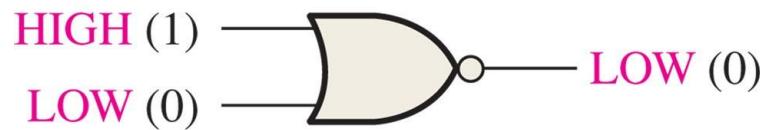
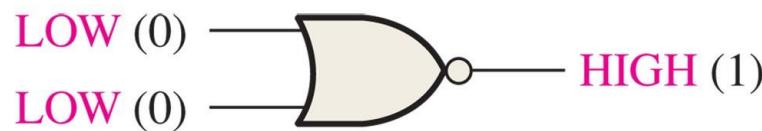


TABLE 3–9

Truth table for a 2-input NOR gate.

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

1 = HIGH, 0 = LOW.

FIGURE 3-36

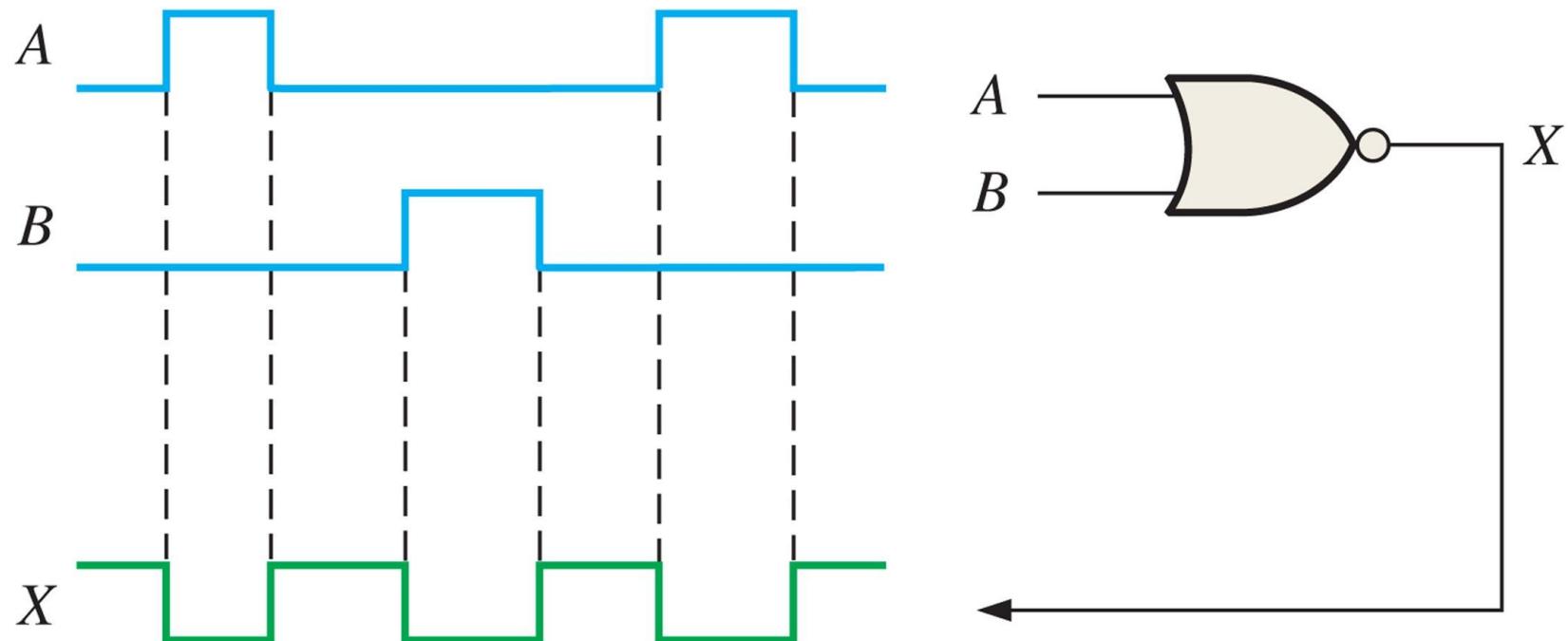
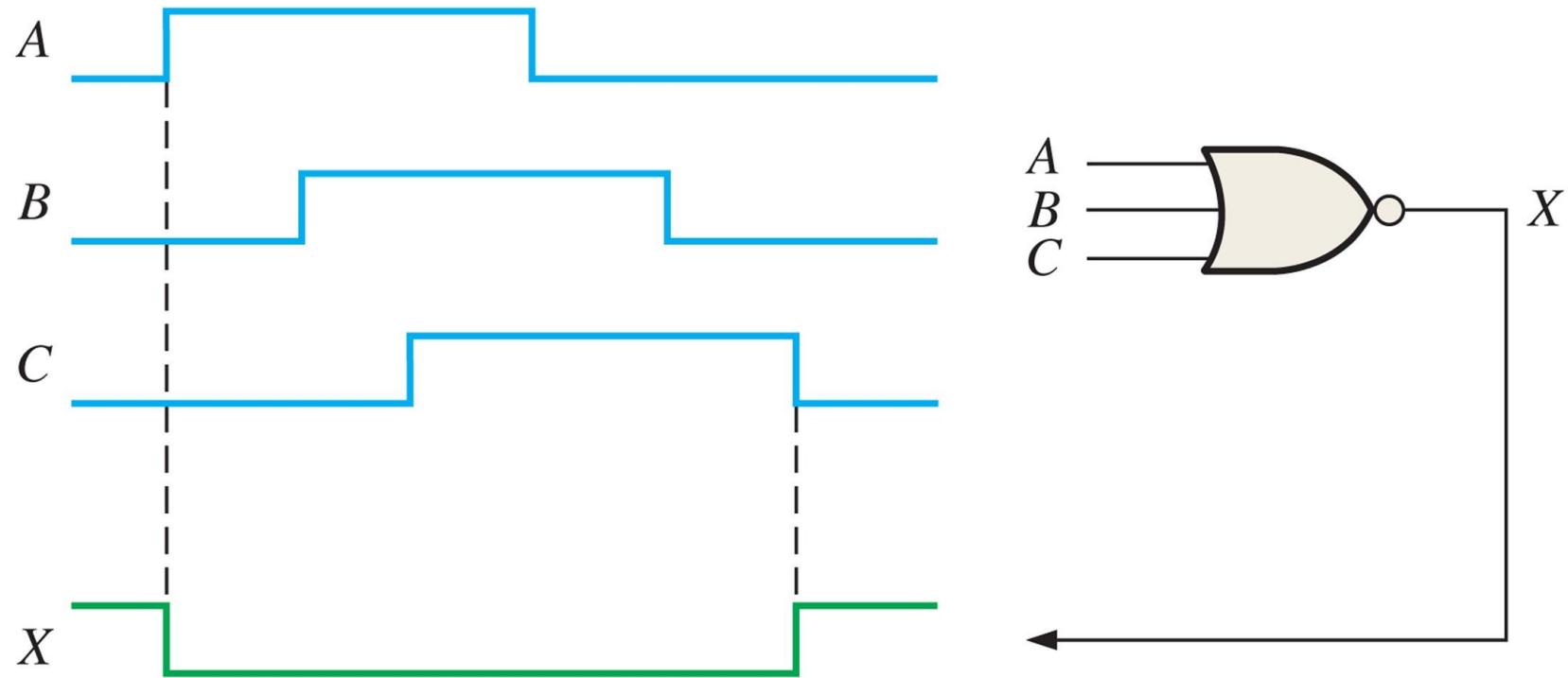


FIGURE 3-37



Standard symbols representing the two equivalent operations of a NOR gate.

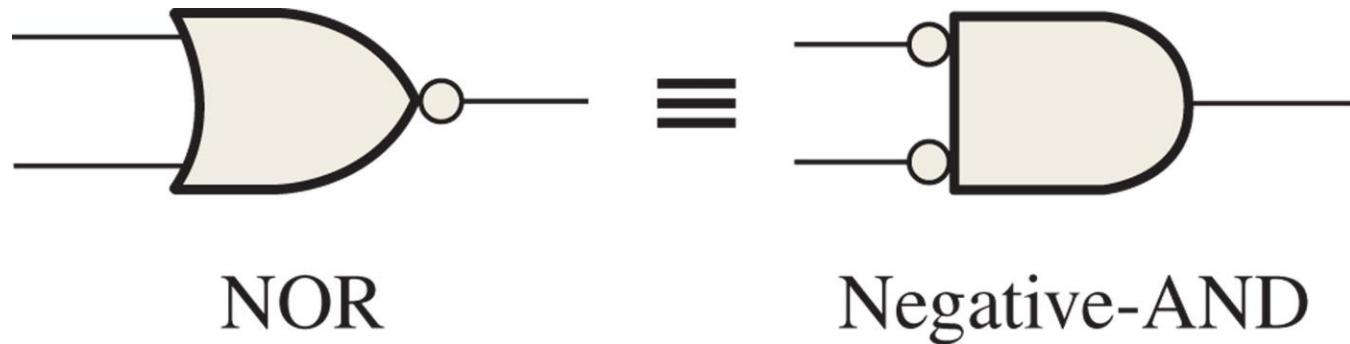
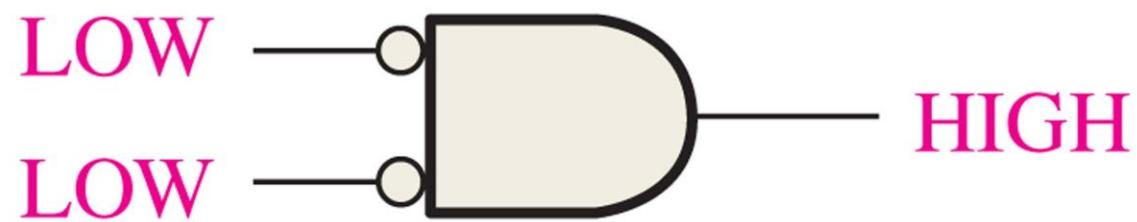


FIGURE 3-39



As part of an aircraft's functional monitoring system, a circuit is required to indicate the status of the landing gears prior to landing. A green LED display turns on if all three gears are properly extended when the "gear down" switch has been activated in preparation for landing. A red LED display turns on if any of the gears fail to extend properly prior to landing. When a landing gear is extended, its sensor produces a LOW voltage. When a landing gear is retracted, its sensor produces a HIGH voltage. Implement a circuit to meet this requirement.

FIGURE 3-40

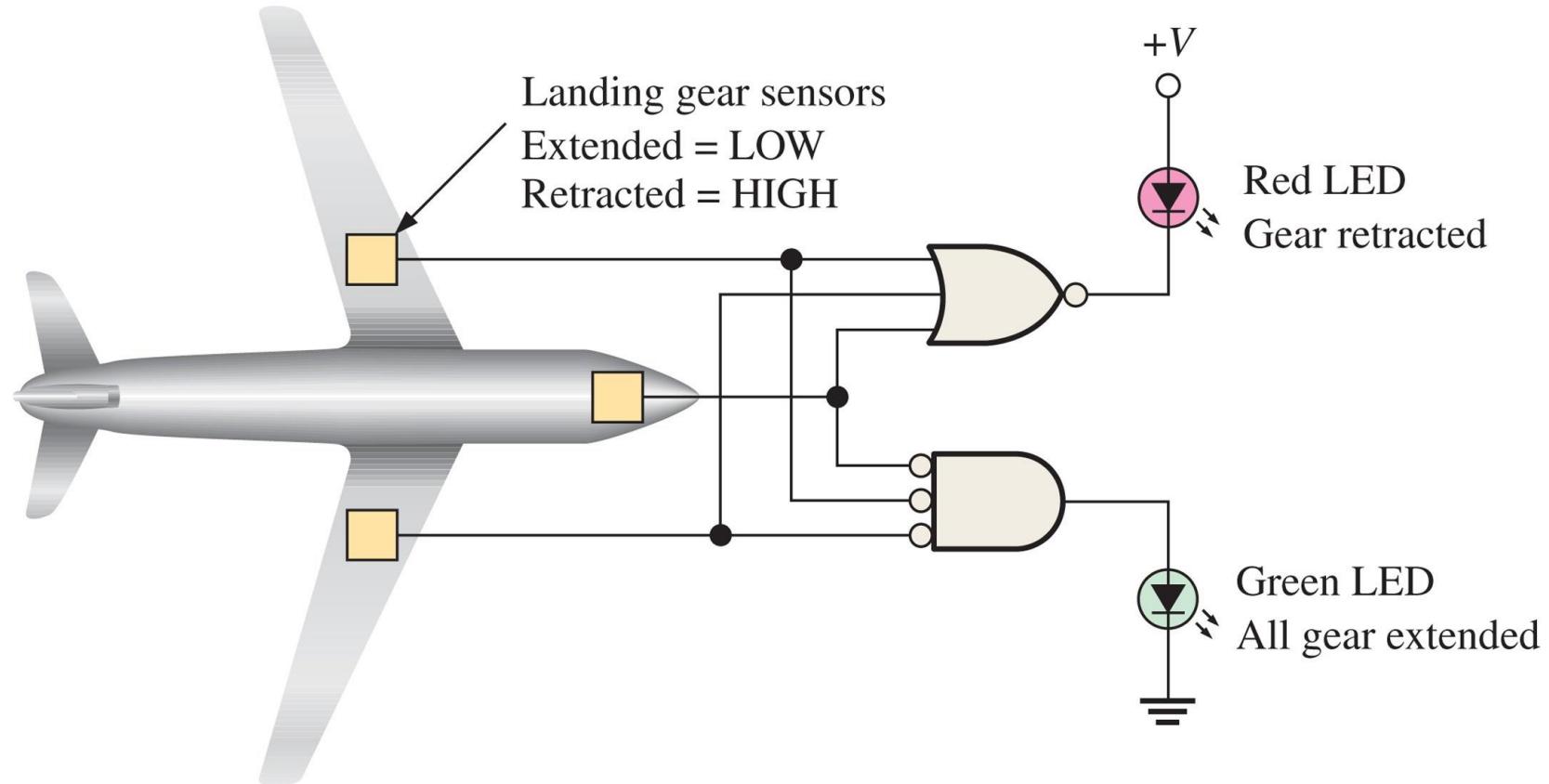


FIGURE 3-41

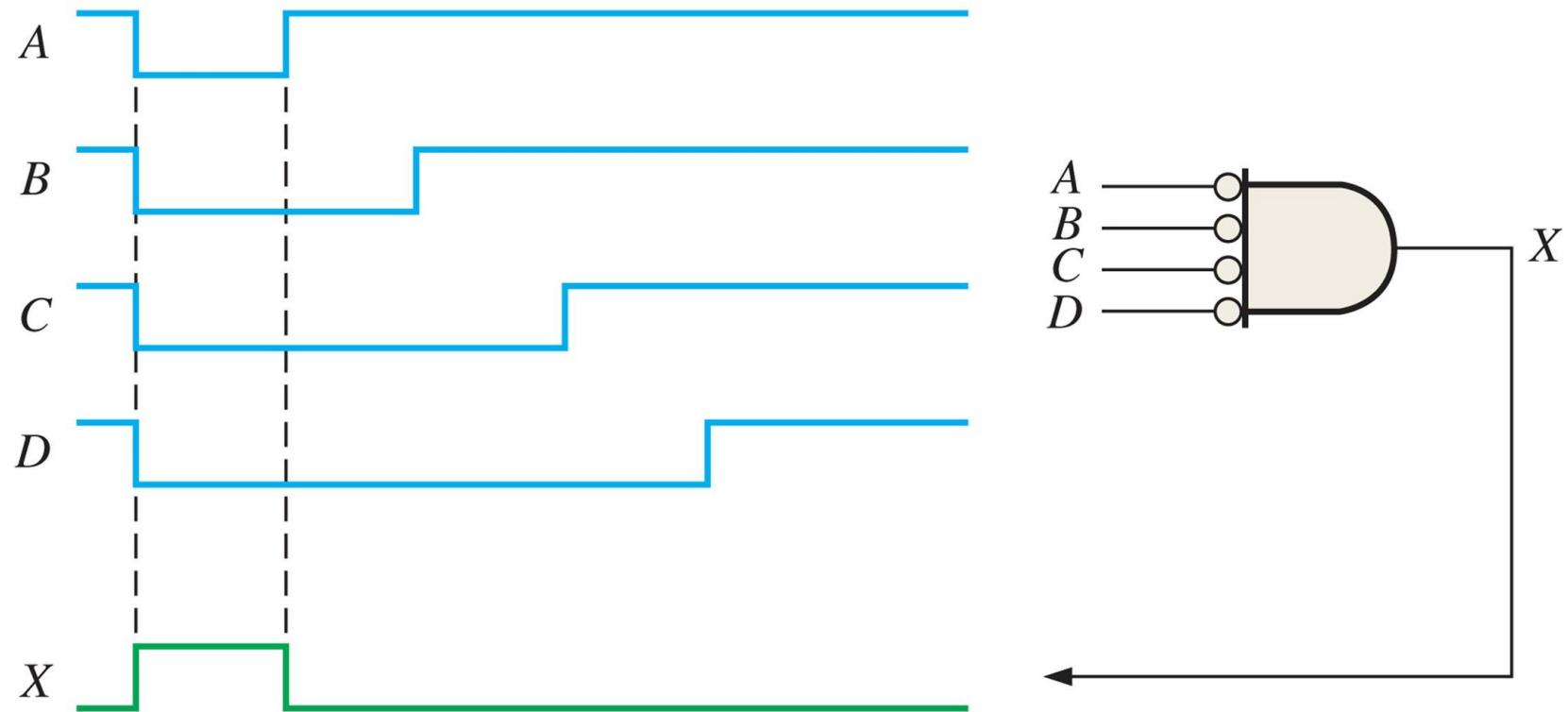
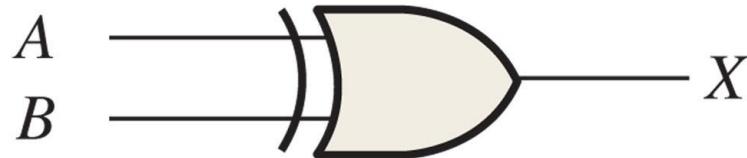


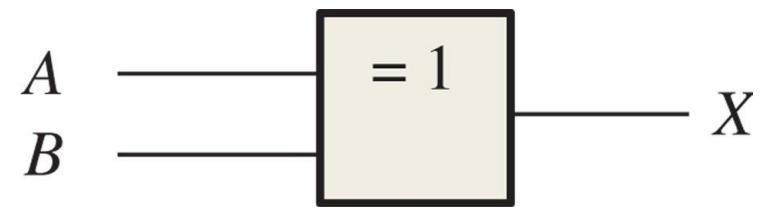
TABLE 3-10

A	B	$\overline{A + B} = X$
0	0	$\overline{0 + 0} = \overline{0} = 1$
0	1	$\overline{0 + 1} = \overline{1} = 0$
1	0	$\overline{1 + 0} = \overline{1} = 0$
1	1	$\overline{1 + 1} = \overline{1} = 0$

Standard logic symbols for the exclusive-OR gate



(a) Distinctive shape



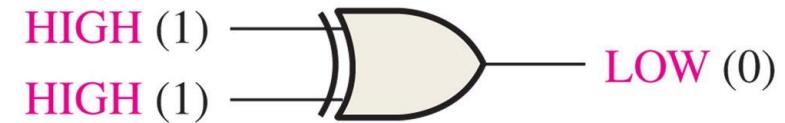
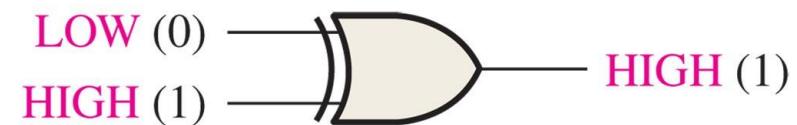
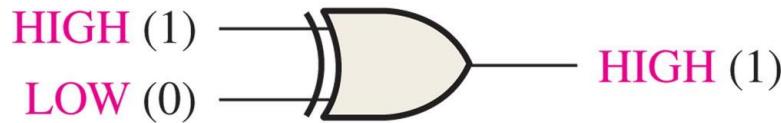
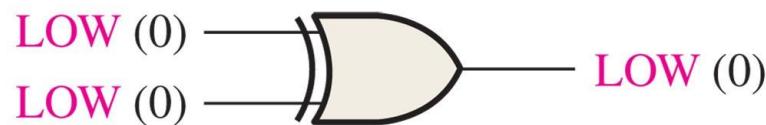
(b) Rectangular outline

TABLE 3-11

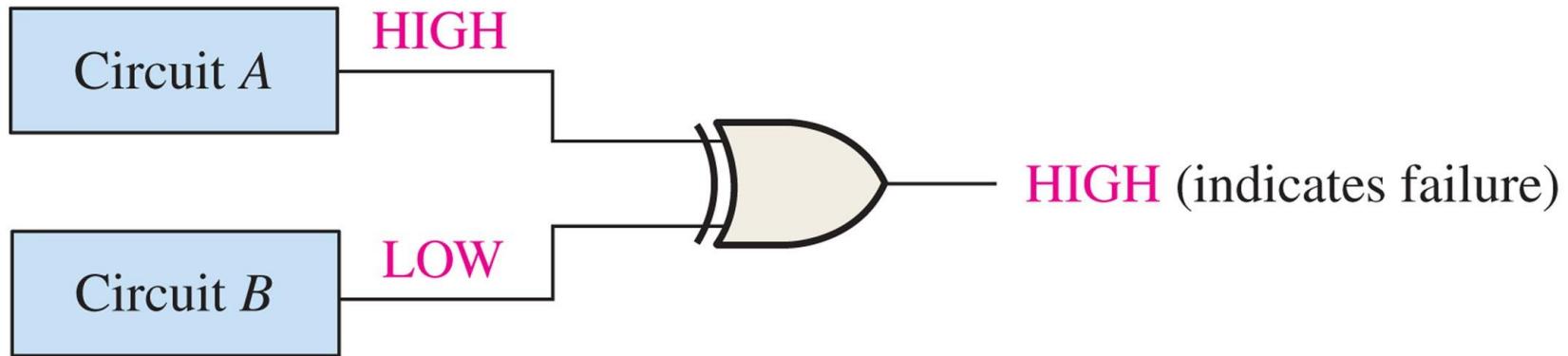
Truth table for an exclusive-OR gate.

Inputs		Output
<i>A</i>	<i>B</i>	<i>X</i>
<hr/>		
0	0	0
0	1	1
1	0	1
1	1	0
<hr/>		

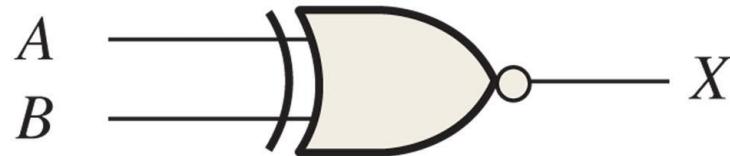
All possible logic levels for an exclusive-OR gate



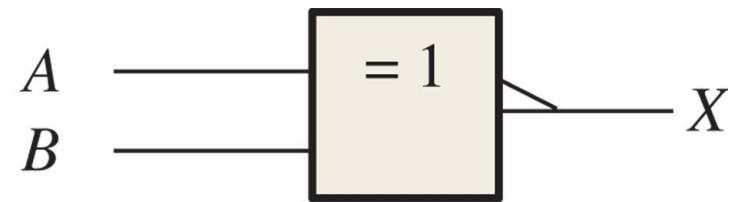
A certain system contains two identical circuits operating in parallel. As long as both are operating properly, the outputs of both circuits are always the same. If one of the circuits fails, the outputs will be at opposite levels at some time. Devise a way to monitor and detect that a failure has occurred in one of the circuits.



Standard logic symbols for the exclusive-NOR gate



(a) Distinctive shape



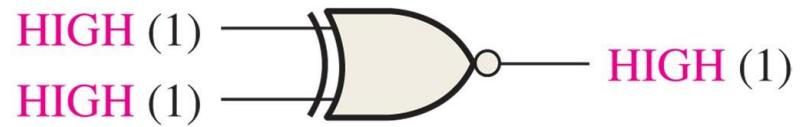
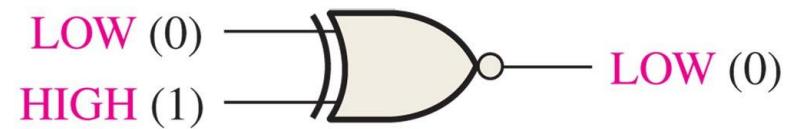
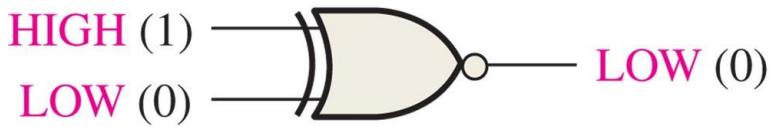
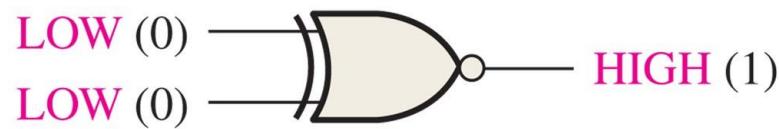
(b) Rectangular outline

TABLE 3-12

Truth table for an exclusive-NOR gate.

Inputs		Output
<i>A</i>	<i>B</i>	<i>X</i>
0	0	1
0	1	0
1	0	0
1	1	1

All possible logic levels for an exclusive-NOR gate



Example of exclusive-OR gate operation with pulse waveform inputs

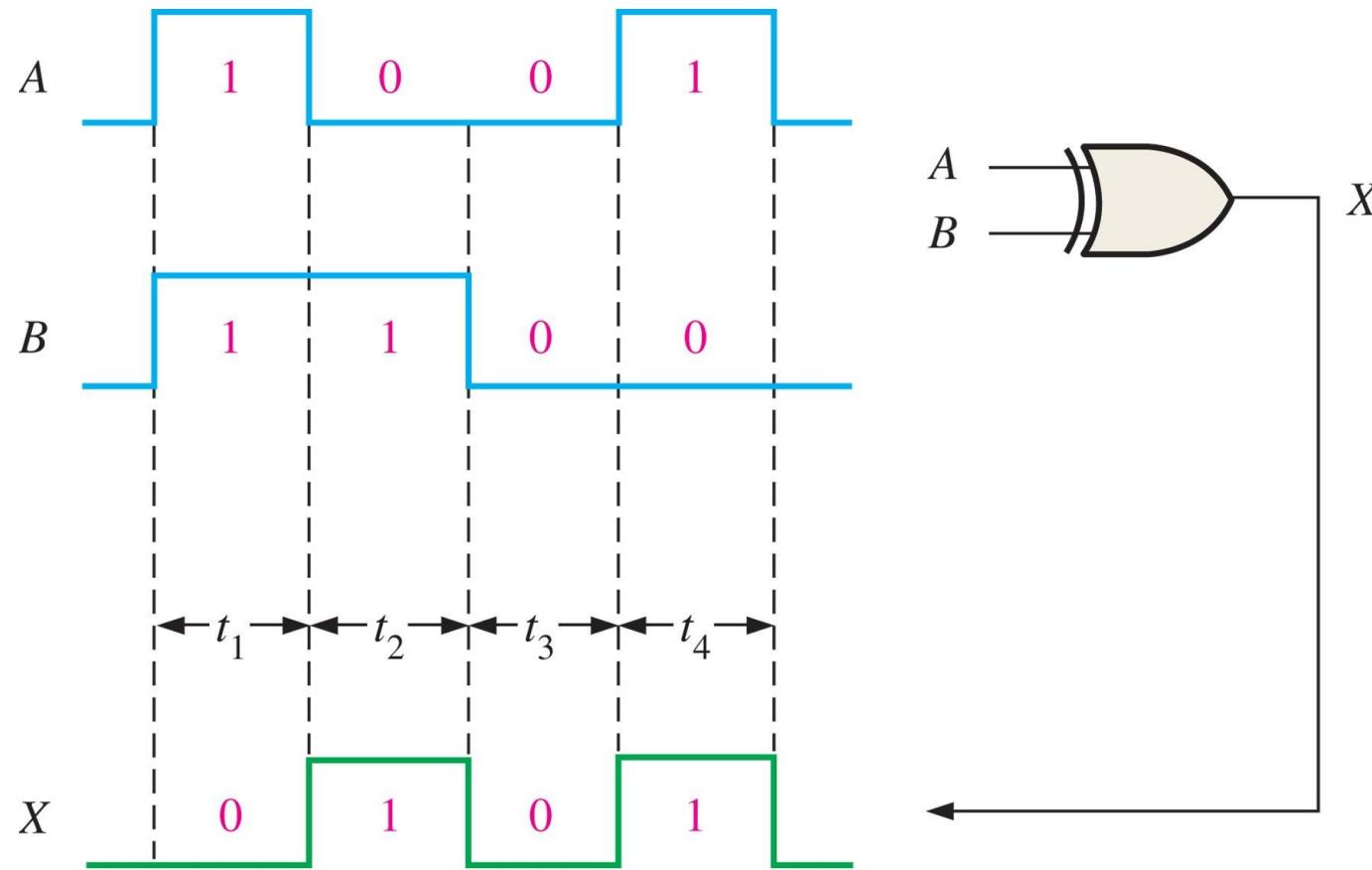


FIGURE 3-48

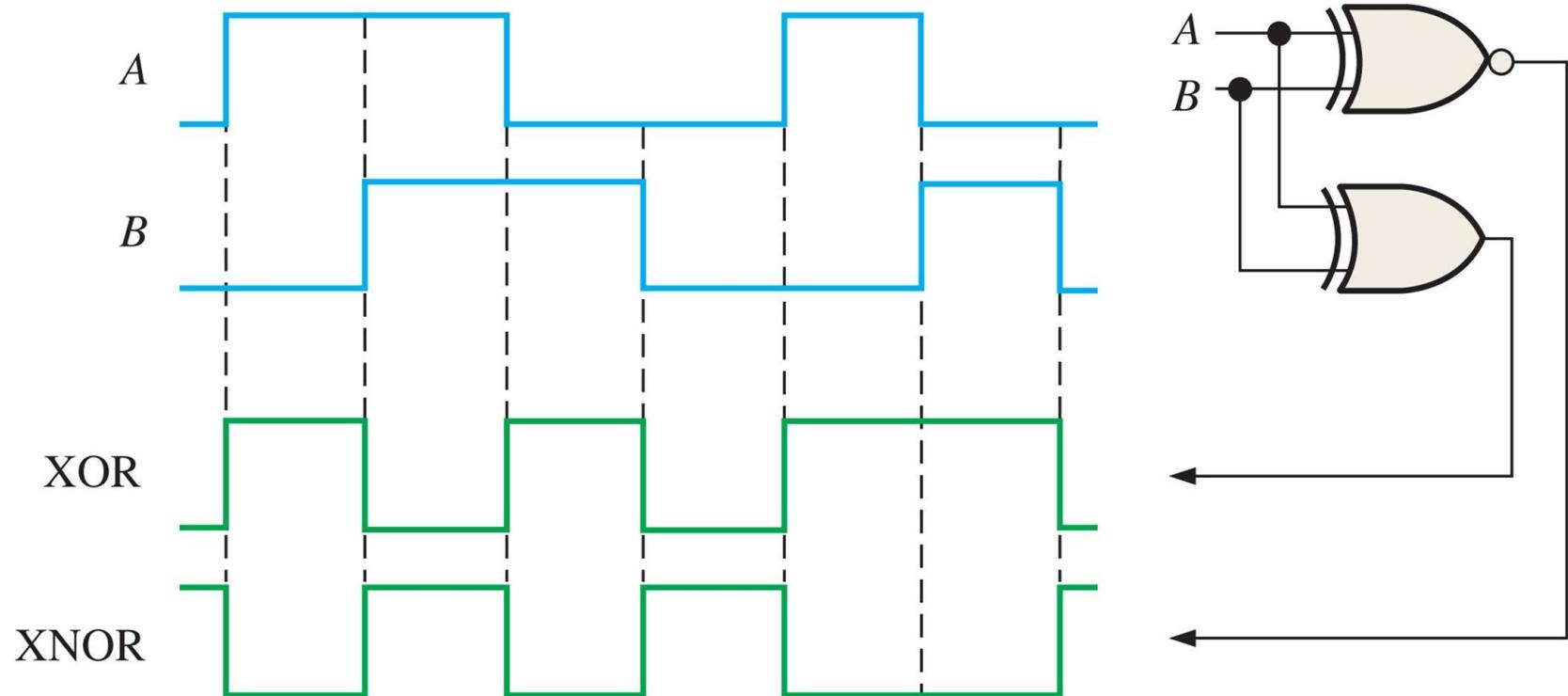
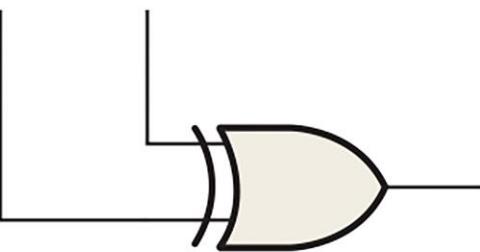


TABLE 3-13

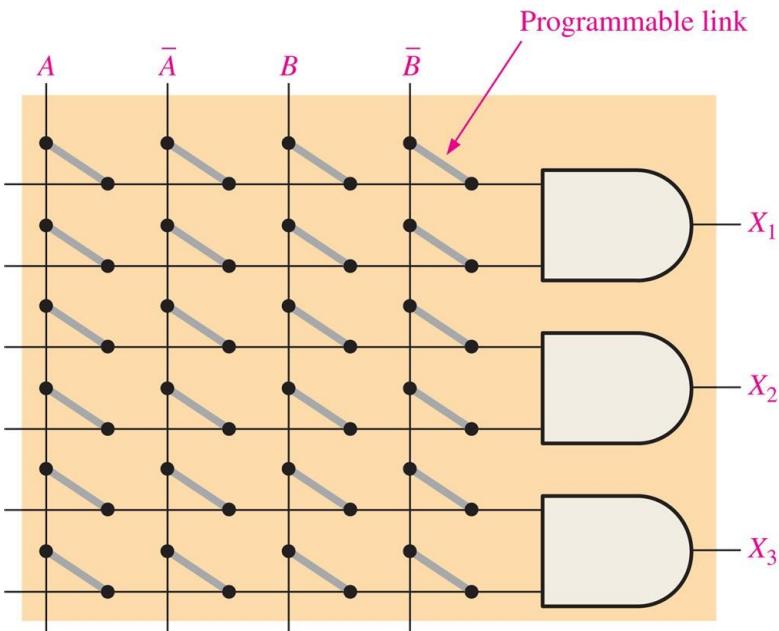
An XOR gate used to add two bits.

Input Bits		Output (Sum)
A	B	Σ
0	0	0
0	1	1
1	0	1
1	1	0 (without the 1 carry bit)

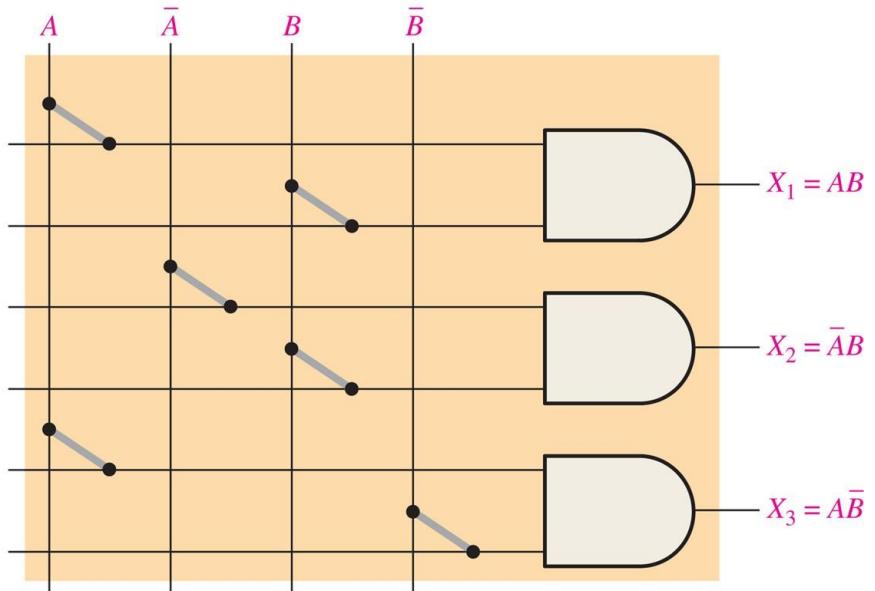


Programmable Logic

Concept of a programmable AND array

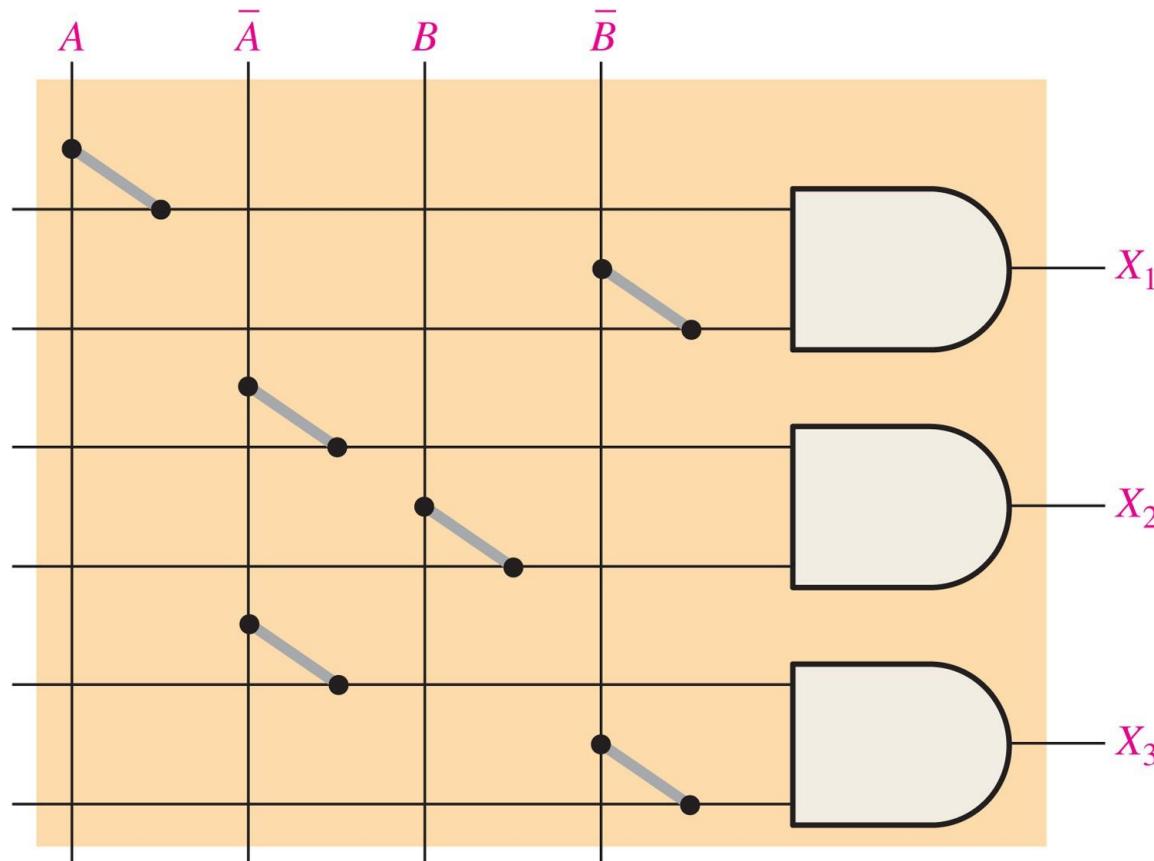


(a) Unprogrammed

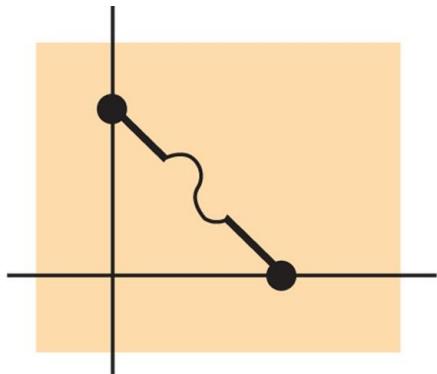


(b) Programmed

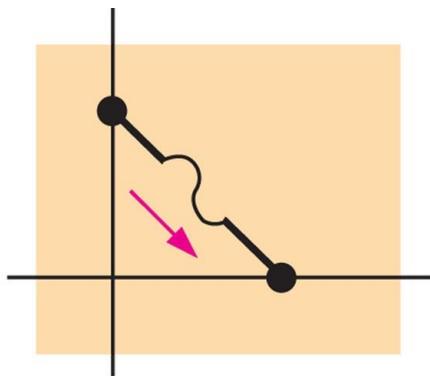
Show the AND array in Figure 3–49(a) programmed for the following outputs:
 $X_1 = A\bar{B}$, $X_2 = \bar{A}B$, and $X_3 = \bar{A}\bar{B}$



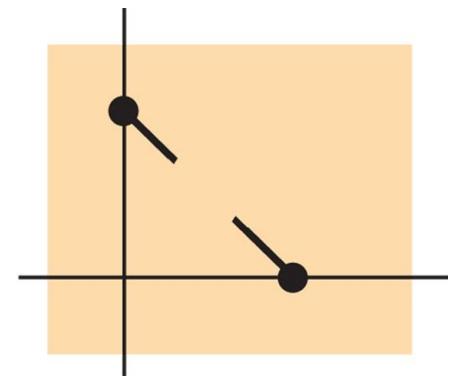
The programmable fuse link



(a) Fuse intact before
programming

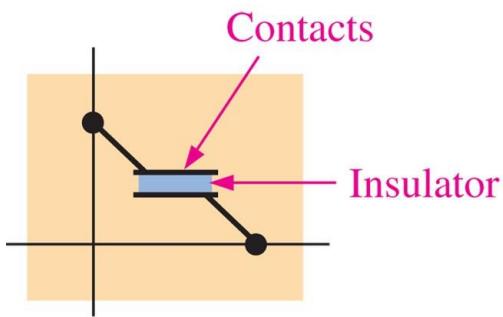


(b) Programming
current

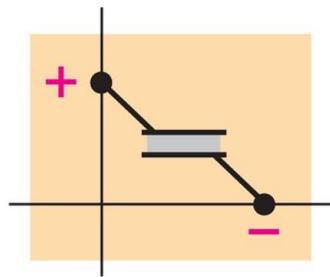


(c) Fuse open after
programming

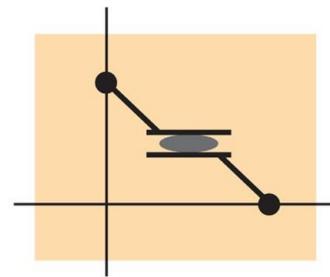
The programmable antifuse link



(a) Antifuse is open before programming.

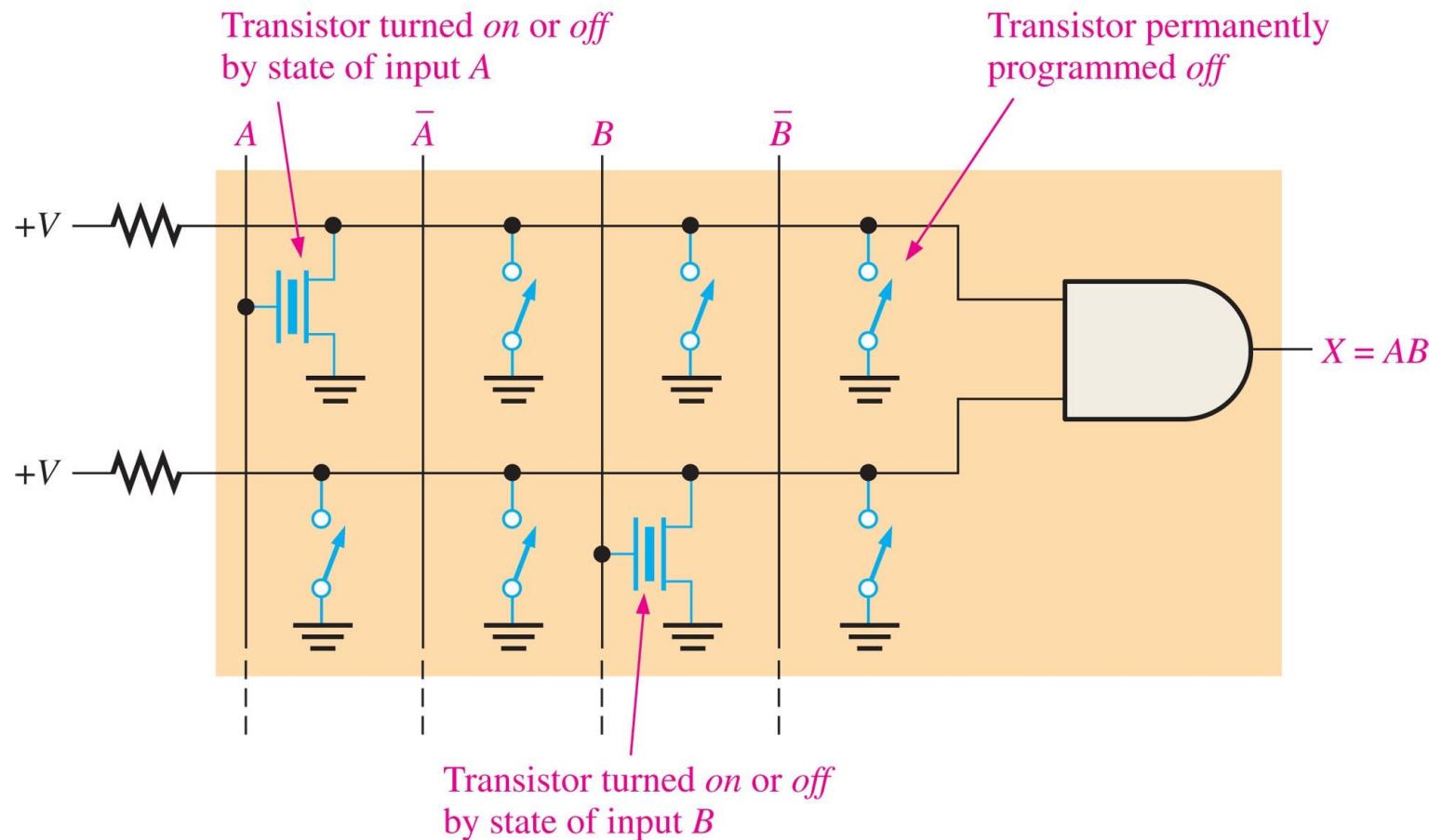


(b) Programming voltage breaks down insulation layer to create contact.



(c) Antifuse is effectively shorted after programming.

Fig 3-53 A simple AND array with EPROM technology
Only one gate in the array is shown for simplicity



EEPROM Technology

Electrically erasable programmable read-only memory technology is similar to EPROM because it also uses a type of floating-gate transistor in E2CMOS cells. The difference is that EEPROM can be erased and reprogrammed electrically without the need for UV light or special fixtures. An E2CMOS device can be programmed after being installed on a printed circuit board (PCB), and many can be reprogrammed while operating in a system. This is called in-system programming (ISP). Fig 3–53 can also be used as an example to represent an AND array with EEPROM technology.

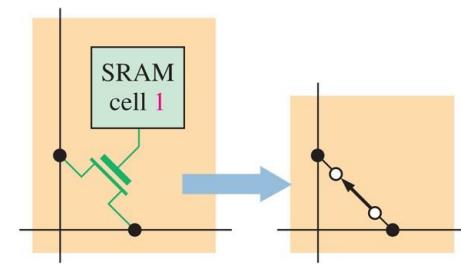
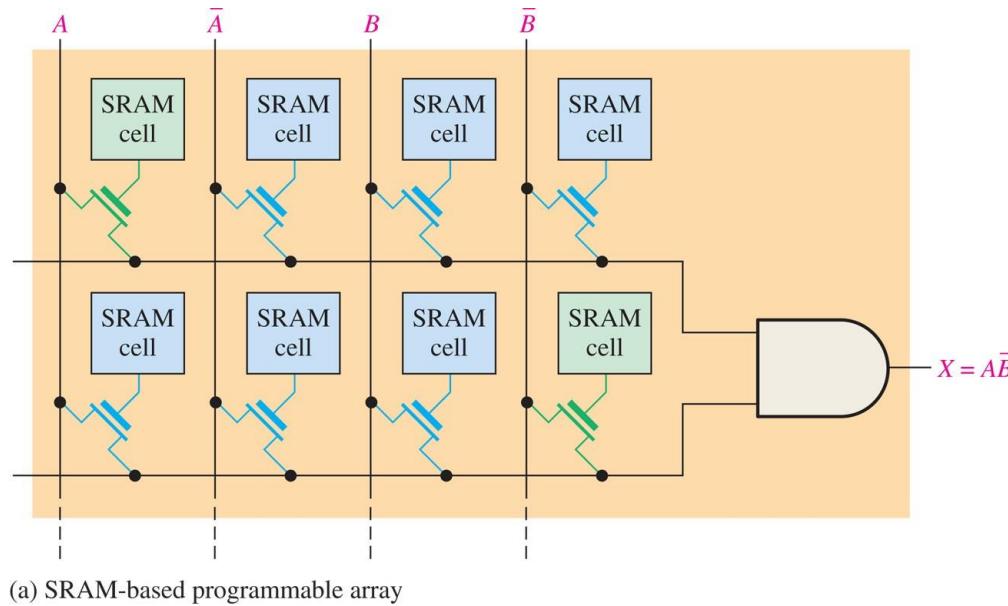
Flash Technology

Flash technology is based on a single transistor link and is both nonvolatile and reprogrammable. Flash elements are a type of EEPROM but are faster and result in higher density devices than the standard EEPROM link.

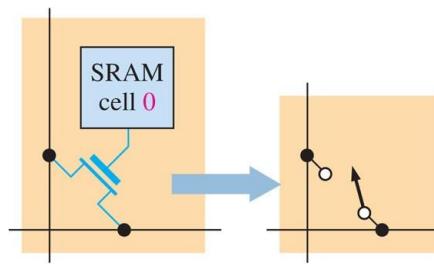
SRAM Technology

Many FPGAs and some CPLDs use a process technology similar to that used in SRAMs (static random-access memories). The basic concept of SRAM-based programmable logic arrays is illustrated in Figure 3–54(a). A SRAM-type memory cell is used to turn a transistor on or off to connect or disconnect rows and columns. For example, when the memory cell contains a 1 (green), the transistor is on and connects the associated row and column lines, as shown in part (b). When the memory cell contains a 0 (blue), the transistor is off so there is no connection between the lines, as shown in part (c).

Fig 3-54 Concept of an AND array with SRAM technology

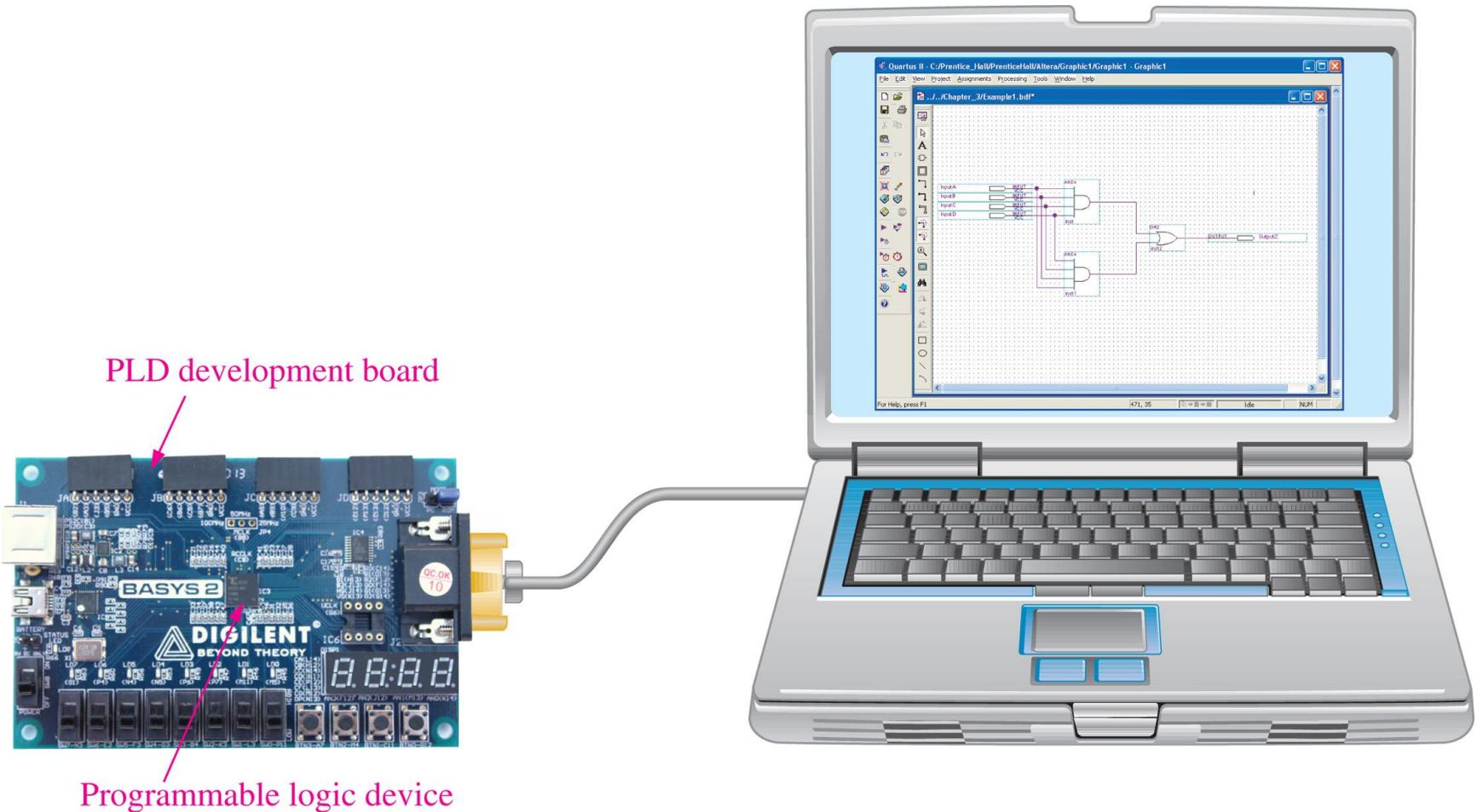


(b) Transistor on



(c) Transistor off

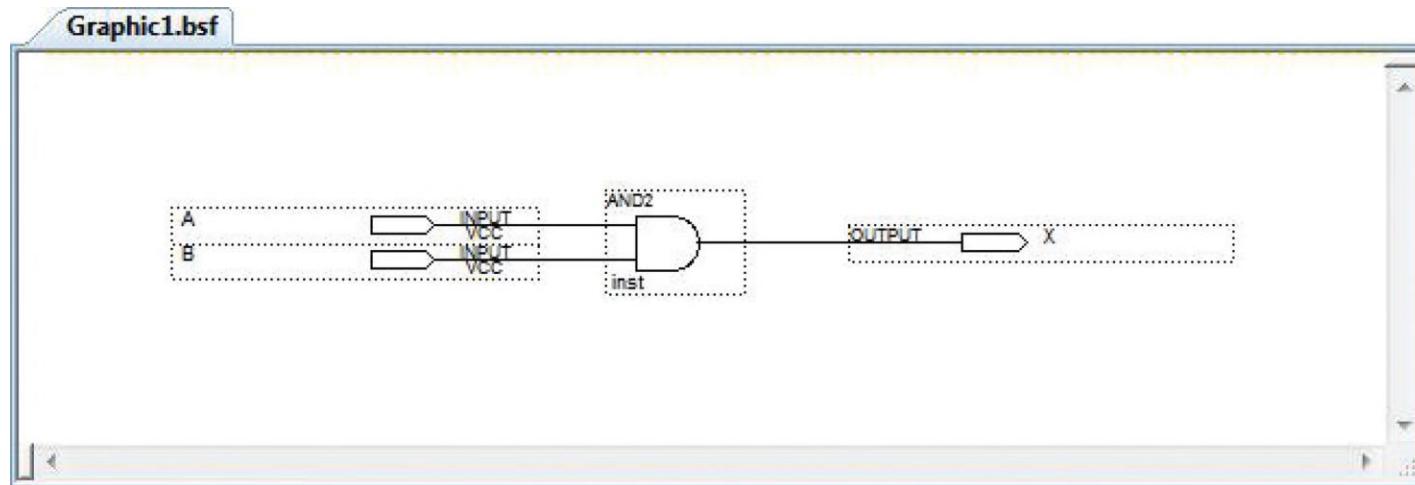
Programming setup for reprogrammable logic devices



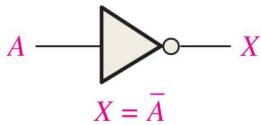
Examples of design entry of an AND gate

Vhdl1.vhd

```
entity VHDL1 is
    port(A, B: in bit; X: out bit);
end entity VHDL1;
architecture ANDfunction of VHDL1 is
begin
    X <= A and B;
end architecture ANDfunction;
```

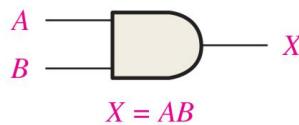


Logic gates described with VHDL



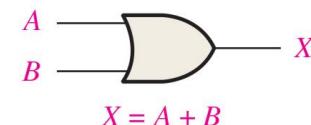
```
entity Inverter is
  port (A: in bit; X: out bit);
end entity Inverter;
architecture NOTfunction of Inverter is
begin
  X <= not A;
end architecture NOTfunction;
```

(a) Inverter



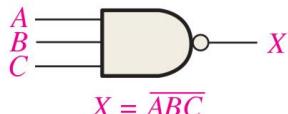
```
entity ANDgate is
  port (A, B: in bit; X: out bit);
end entity ANDgate;
architecture ANDfunction of ANDgate is
begin
  X <= A and B;
end architecture ANDfunction;
```

(b) AND gate



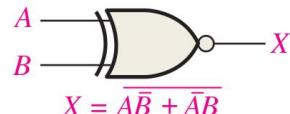
```
entity ORgate is
  port (A, B: in bit; X: out bit);
end entity ORgate;
architecture ORfunction of ORgate is
begin
  X <= A or B;
end architecture ORfunction;
```

(c) OR gate



```
entity NANDgate is
  port (A, B, C: in bit; X: out bit);
end entity NANDgate;
architecture NANDfunction of NANDgate is
begin
  X <= A nand B nand C;
end architecture NANDfunction;
```

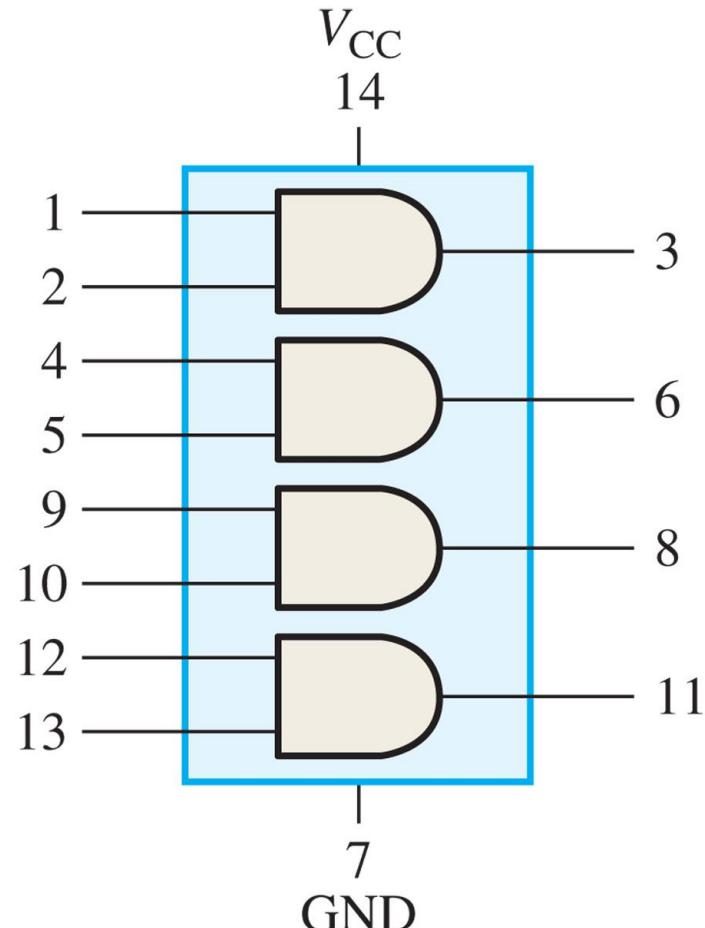
(d) NAND gate



```
entity XNORgate is
  port (A, B: in bit; X: out bit);
end entity XNORgate;
architecture XNORfunction of XNORgate is
begin
  X <= A xnor B;
end architecture XNORfunction;
```

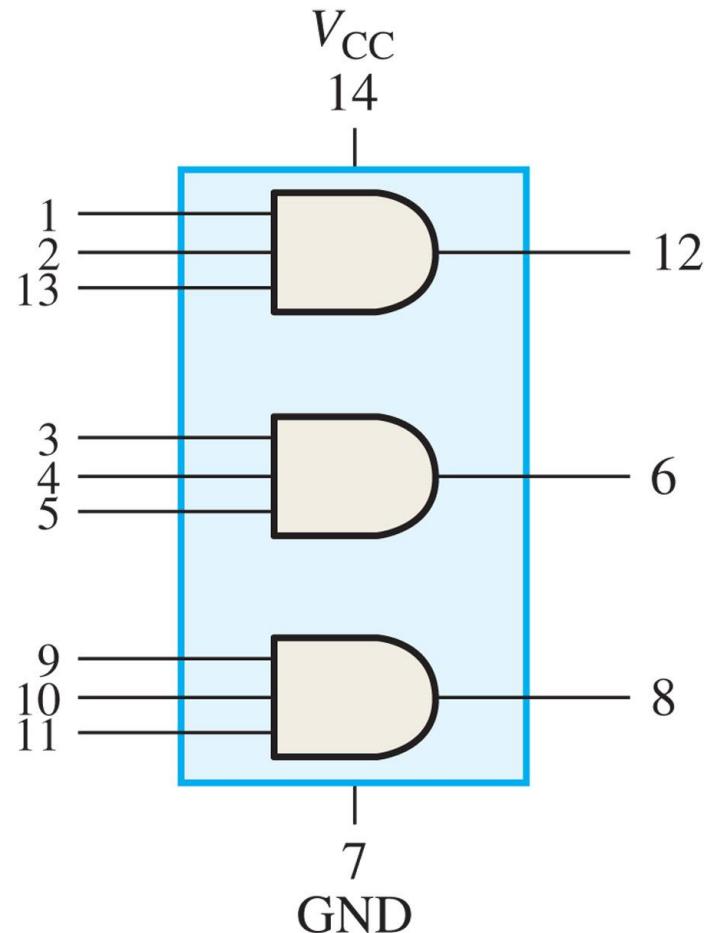
(e) XNOR gate

FIGURE 3-59 74 series AND gate devices with pin numbers.



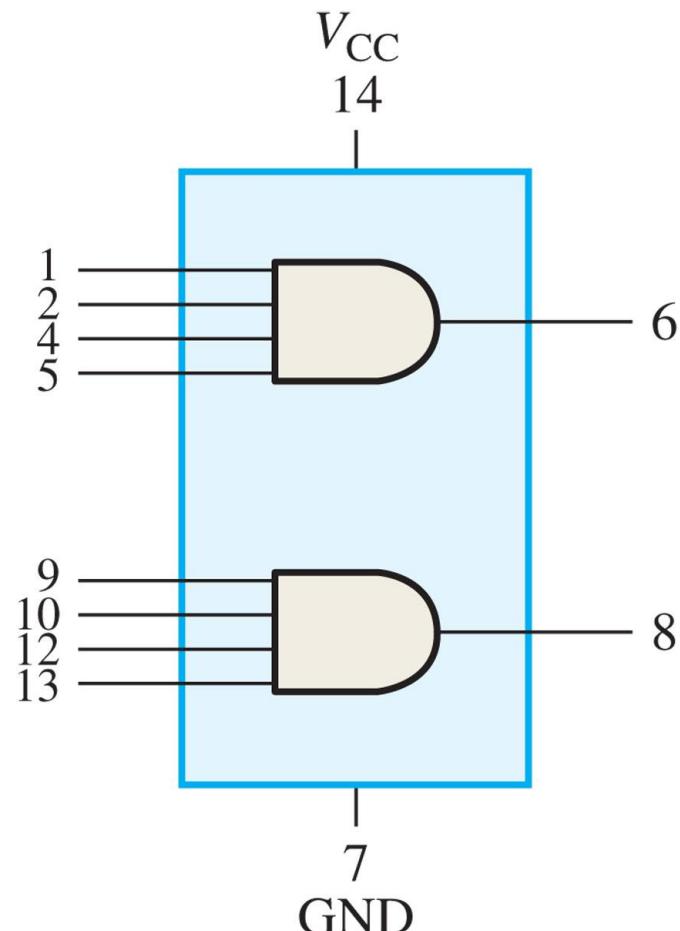
(a) 74xx08

74 series AND gate devices with pin numbers



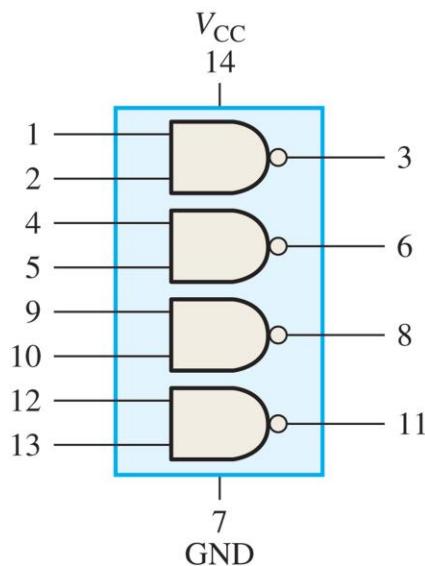
(b) 74xx11

FIGURE 3-59 (continued) 74 series AND gate devices with pin numbers.

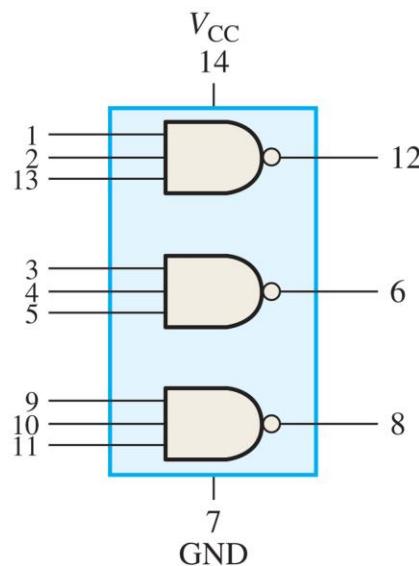


(c) 74xx21

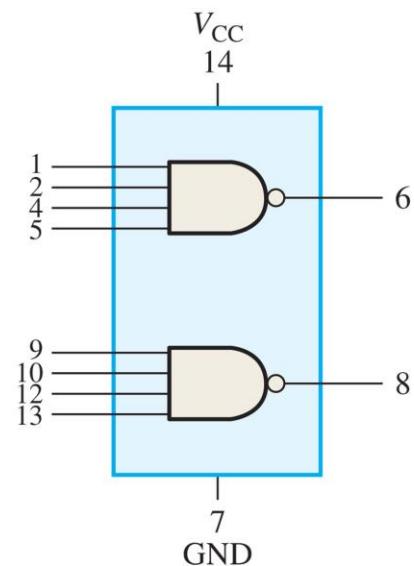
FIGURE 3-60 74 series NAND gate devices with package pin numbers.



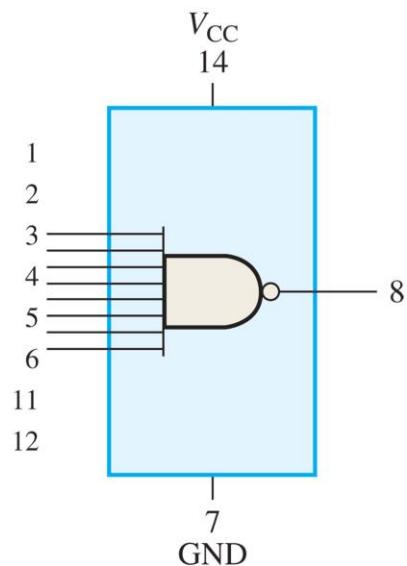
(a) 74xx00



(b) 74xx10

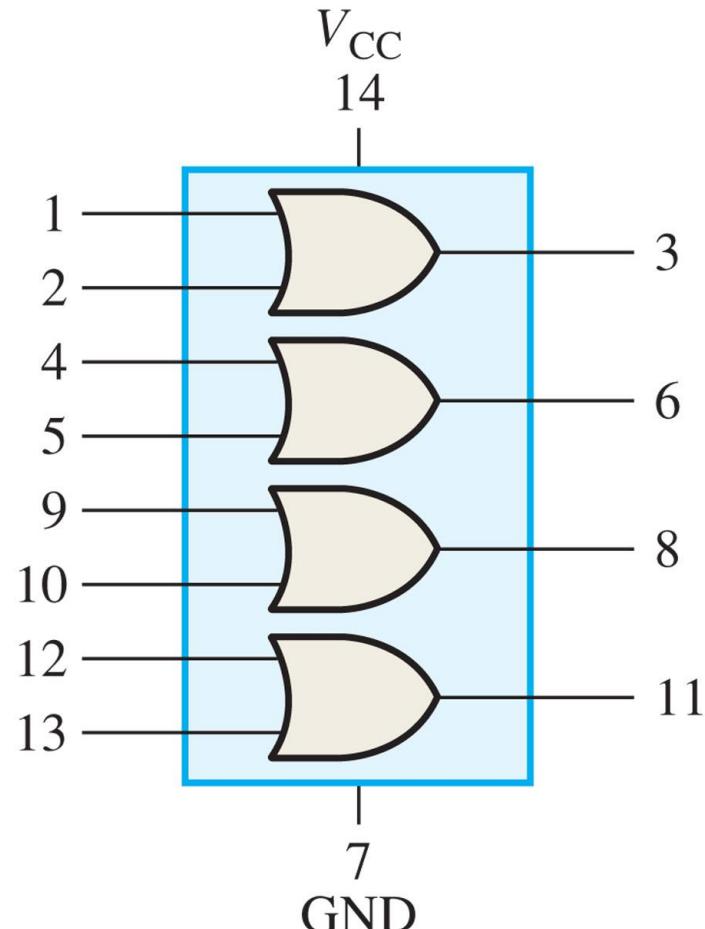


(c) 74xx20



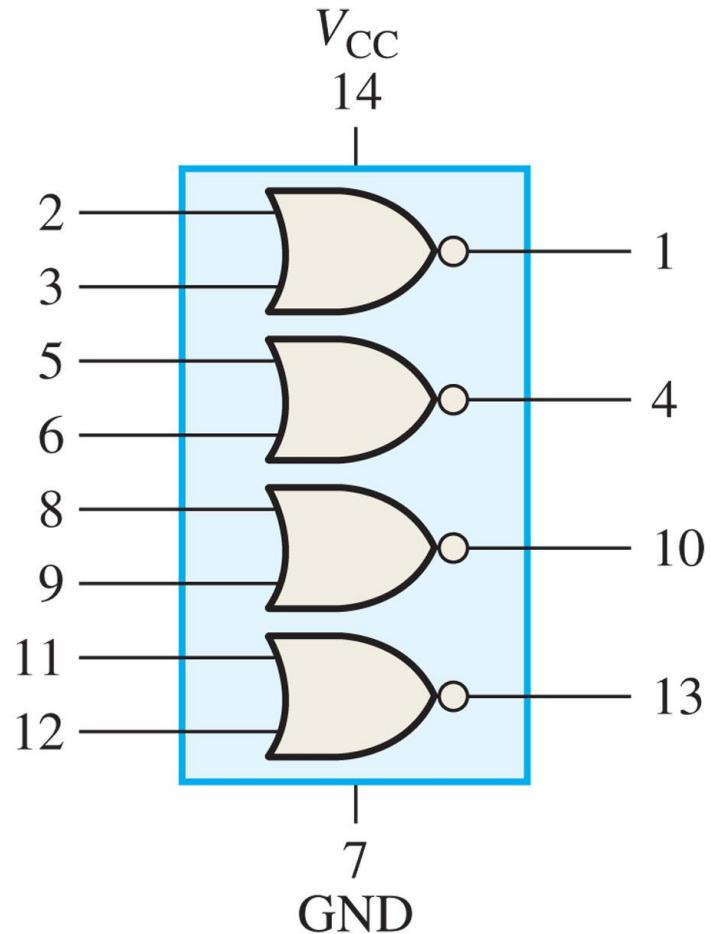
(d) 74xx30

FIGURE 3-61 74 series OR gate device.

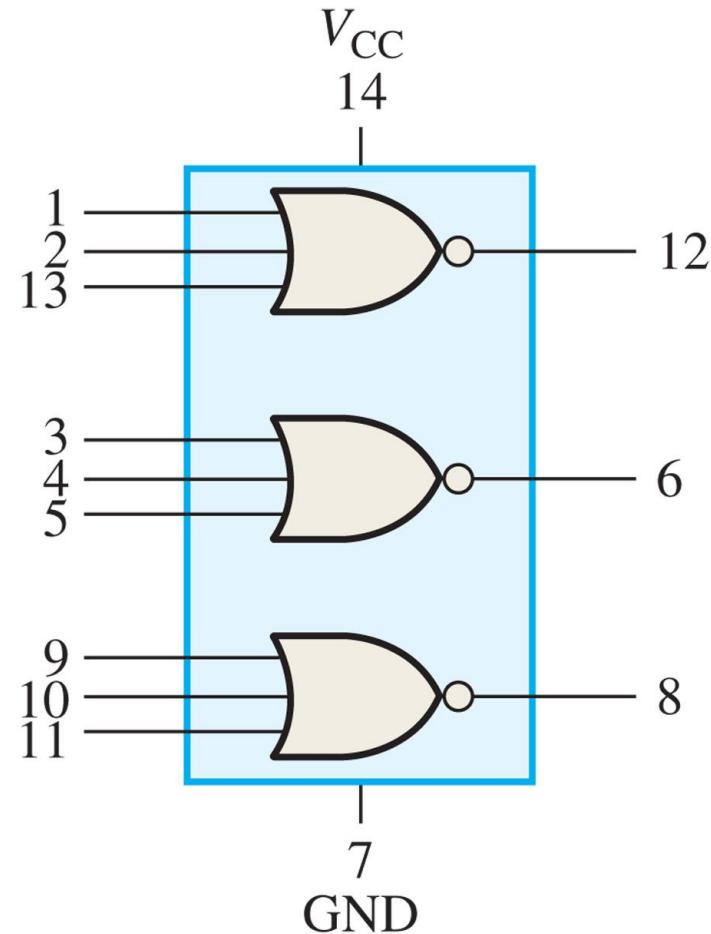


74xx32

FIGURE 3-62 74 series NOR gate devices.

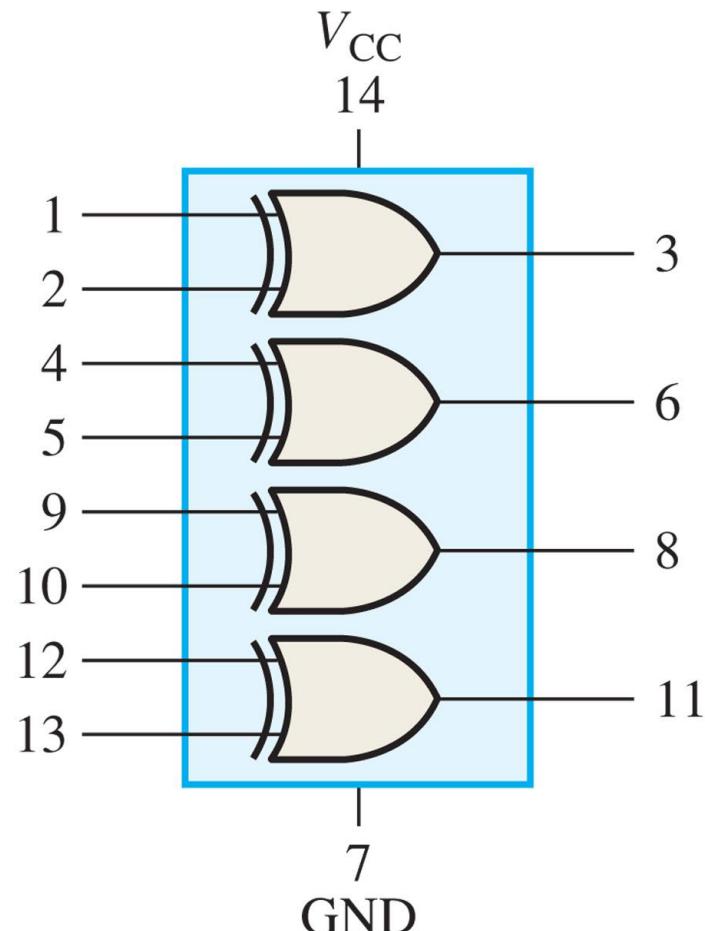


(a) 74xx02



(b) 74xx27

FIGURE 3-63 74 series XOR gate.



74xx86