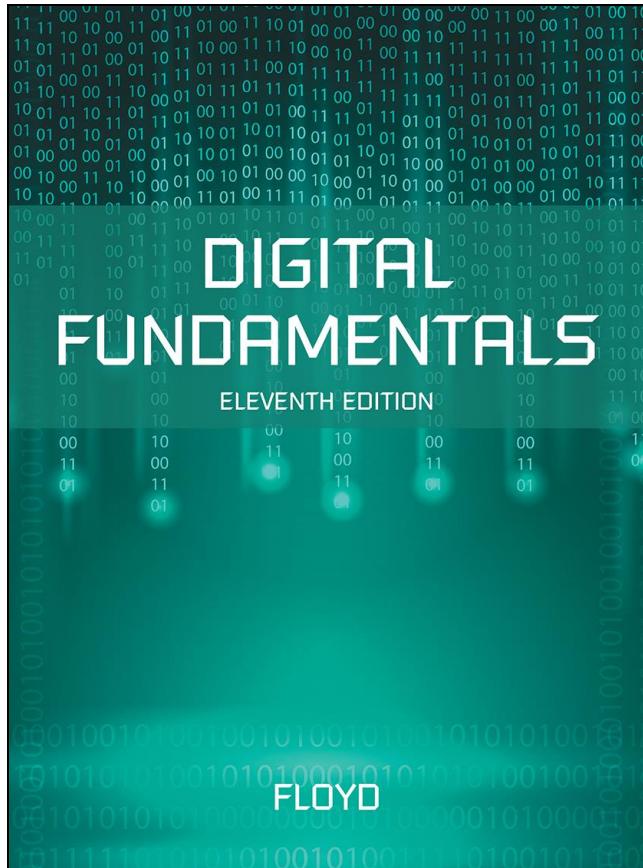


Digital Fundamentals

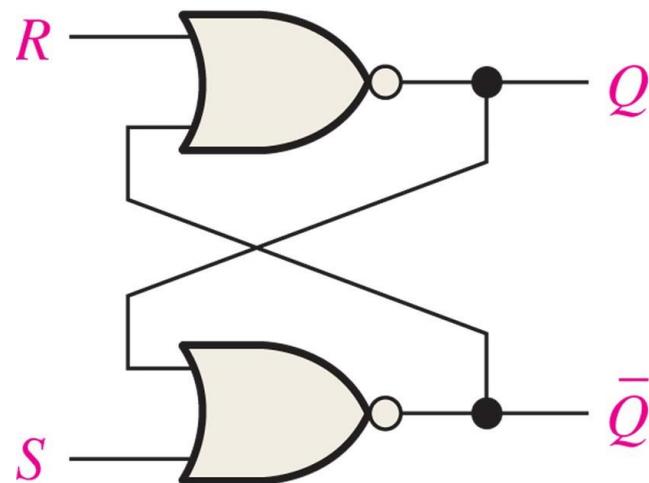
ELEVENTH EDITION



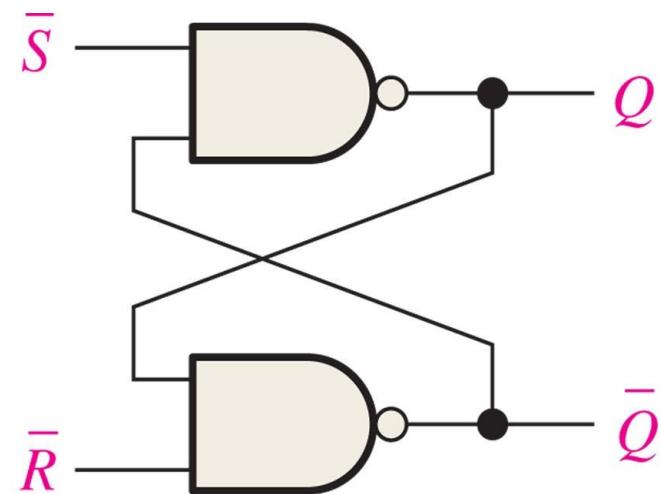
CHAPTER 7

Latches, Flip-Flops, and Timers

FIGURE 7-1 Two versions of SET-RESET (S-R) latches.



(a) Active-HIGH input S-R latch



(b) Active-LOW input \bar{S} - \bar{R} latch

FIGURE 7-2 Negative-OR equivalent of the NAND gate S-R latch in Figure 7-1(b).

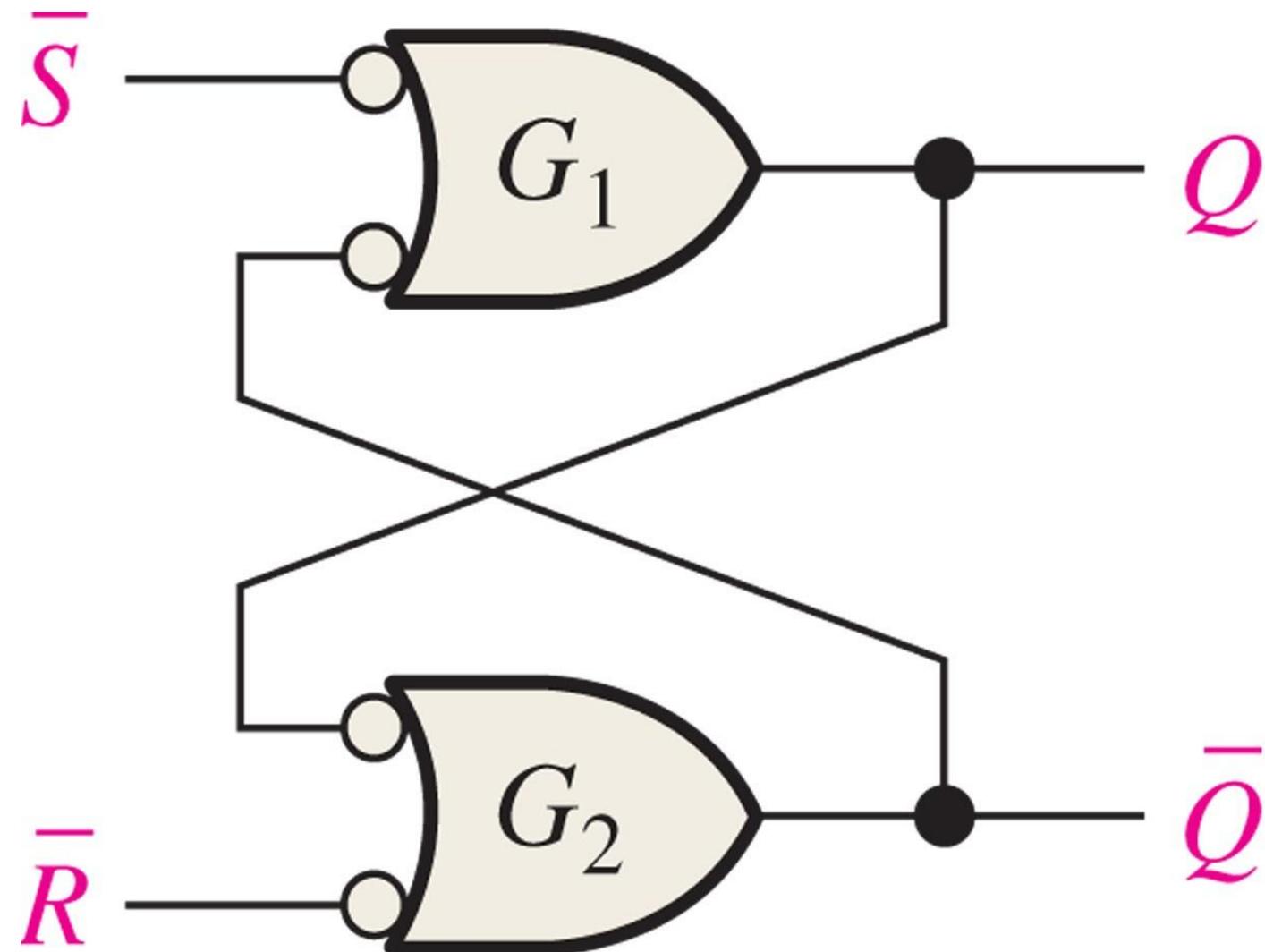
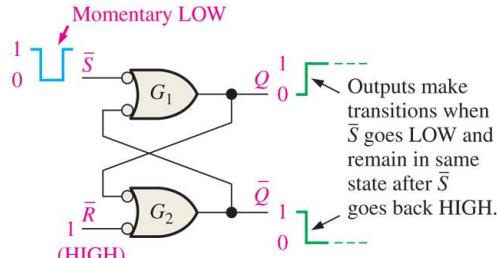


FIGURE 7-3 The three modes of basic \overline{S} - \overline{R} latch operation (SET, RESET, no-change) and the invalid condition.

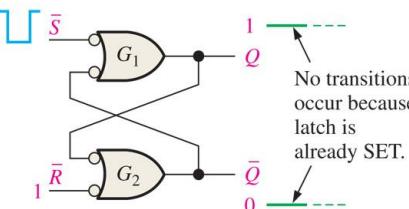
Momentary LOW



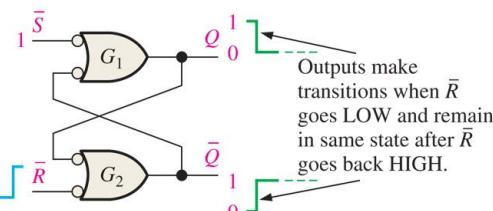
Latch starts out RESET ($Q = 0$).

(a) Two possibilities for the SET operation

Outputs make transitions when \bar{S} goes LOW and remain in same state after \bar{S} goes back HIGH.



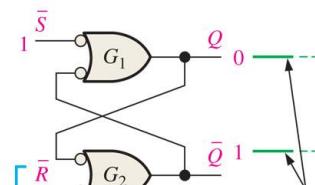
Latch starts out SET ($Q = 1$).



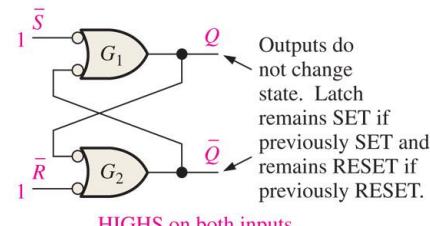
Latch starts out SET ($Q = 1$).

(b) Two possibilities for the RESET operation

Outputs make transitions when \bar{R} goes LOW and remain in same state after \bar{R} goes back HIGH.

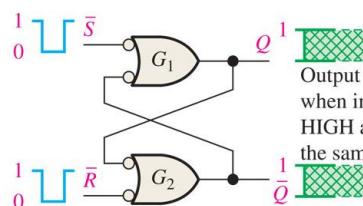


Latch starts out RESET ($Q = 0$).



(c) No-change condition

Outputs do not change state. Latch remains SET if previously SET and remains RESET if previously RESET.



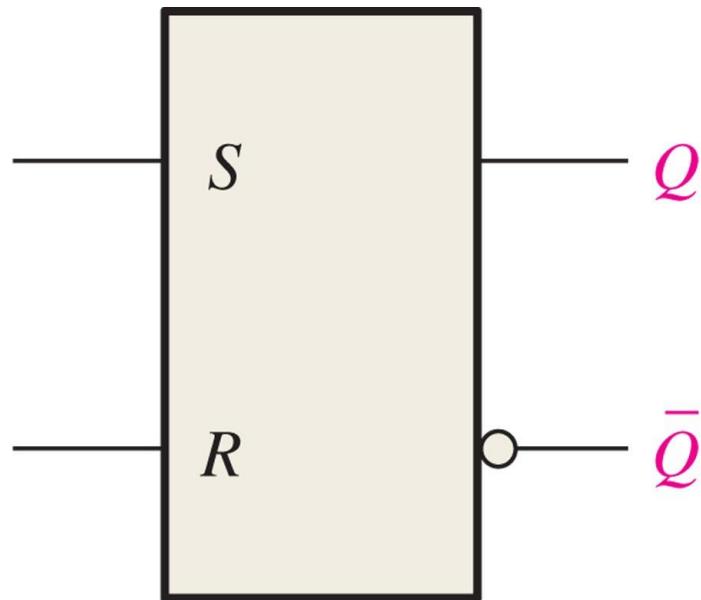
(d) Invalid condition

Output states are uncertain when input LOWs go back HIGH at approximately the same time.

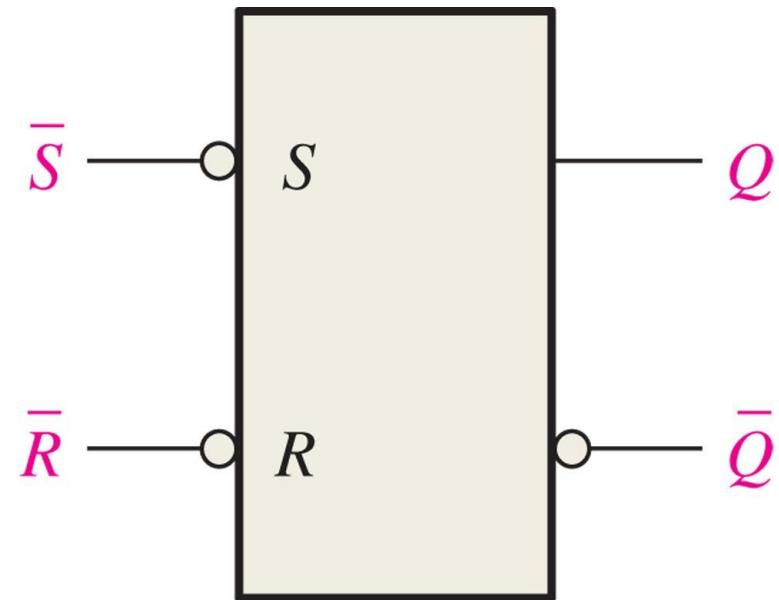
TABLE 7-1Truth table for an active-LOW input \bar{S} - \bar{R} latch.

Inputs		Outputs		Comments
\bar{S}	\bar{R}	Q	\bar{Q}	
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

FIGURE 7-4 Logic symbols for the S-R and \bar{S} - \bar{R} latch.



(a) Active-HIGH input
S-R latch



(b) Active-LOW input
 \bar{S} - \bar{R} latch

FIGURE 7-5

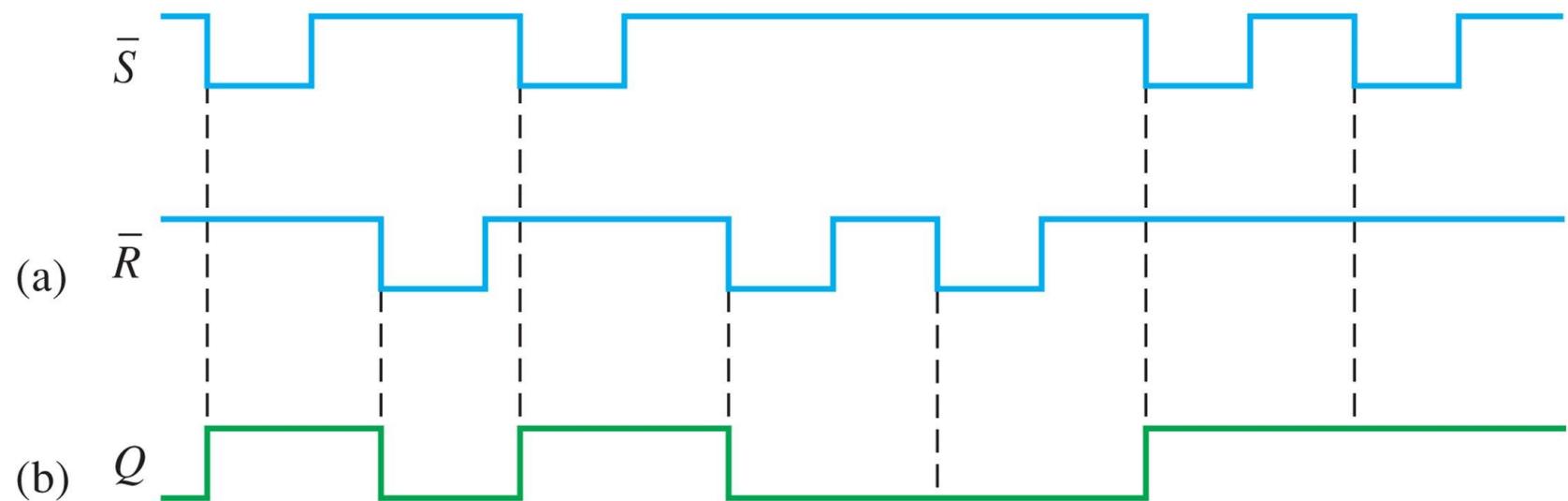
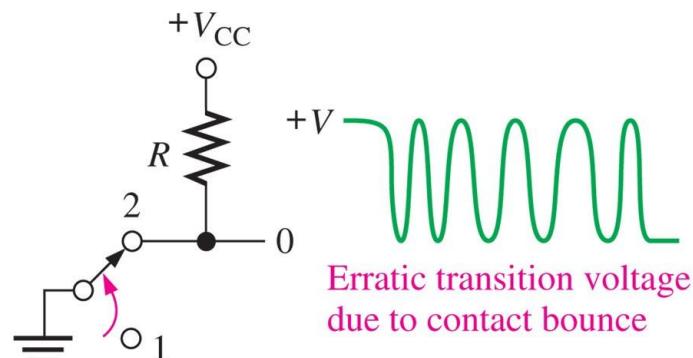
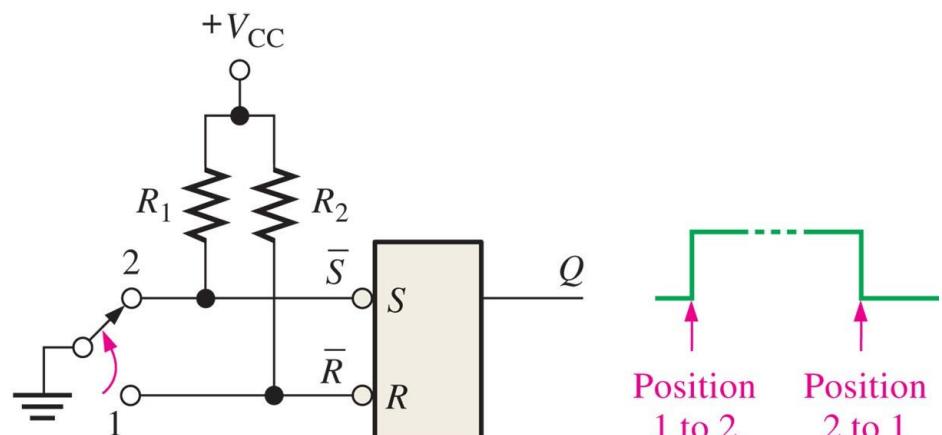


FIGURE 7-6 The \overline{S} - R latch used to eliminate switch contact bounce.

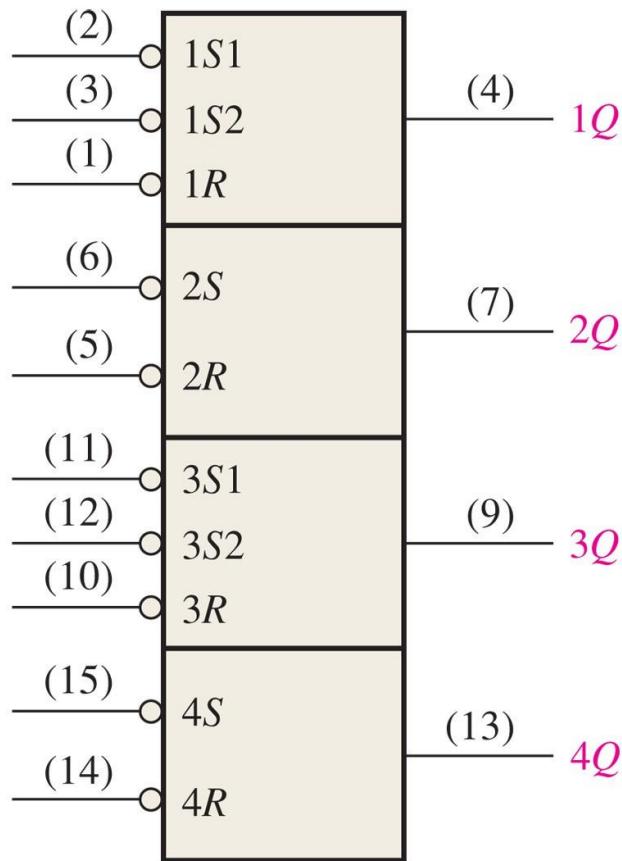


(a) Switch contact bounce

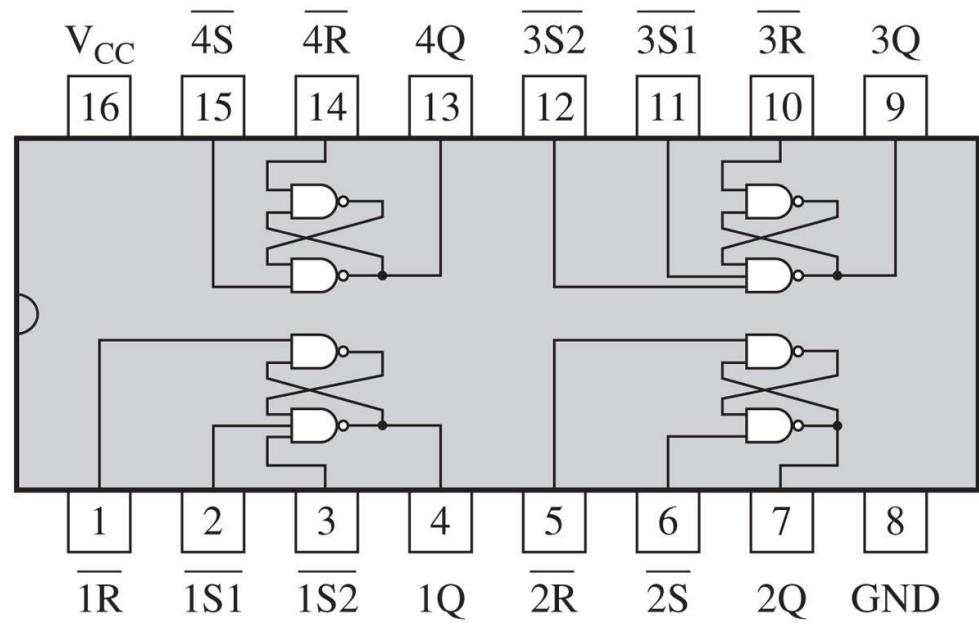


(b) Contact-bounce eliminator circuit

FIGURE 7-7 The 74HC279A quad \overline{S} - \overline{R} latch.

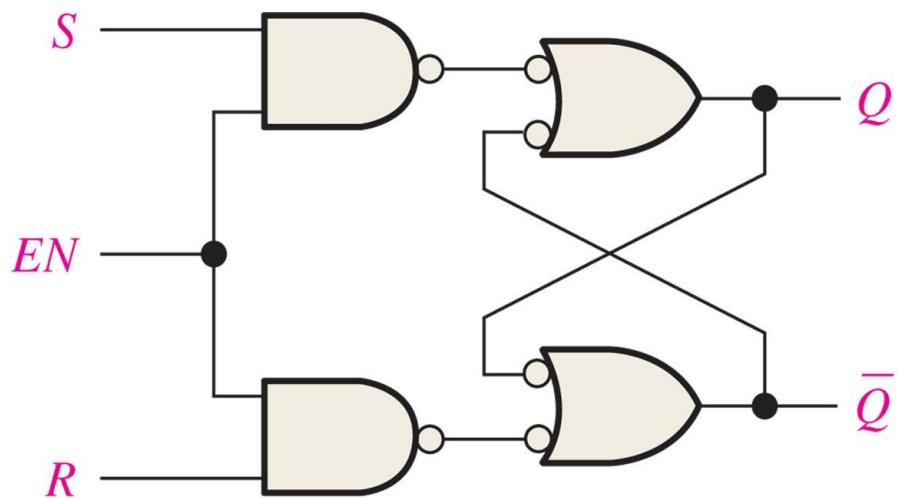


(a) Logic diagram

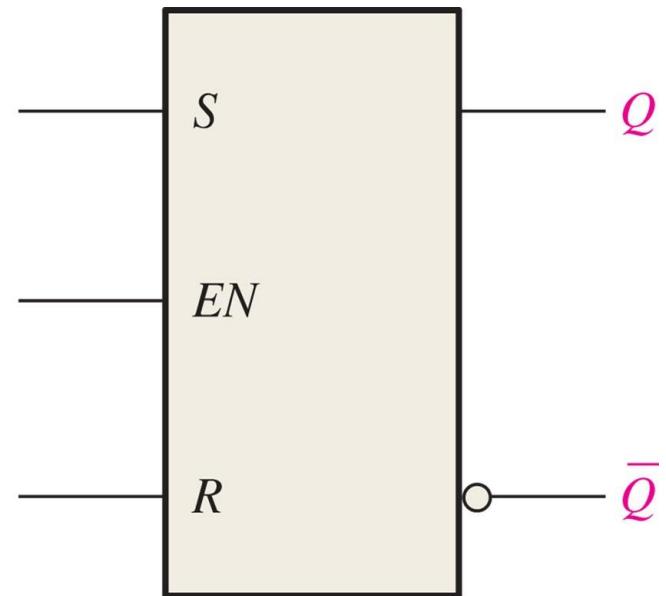


(b) Pin diagram

FIGURE 7-8 A gated S-R latch.



(a) Logic diagram



(b) Logic symbol

FIGURE 7-9

Determine the Q output waveform if the inputs shown in Figure 7–9(a) are applied to a gated S-R latch that is initially RESET.

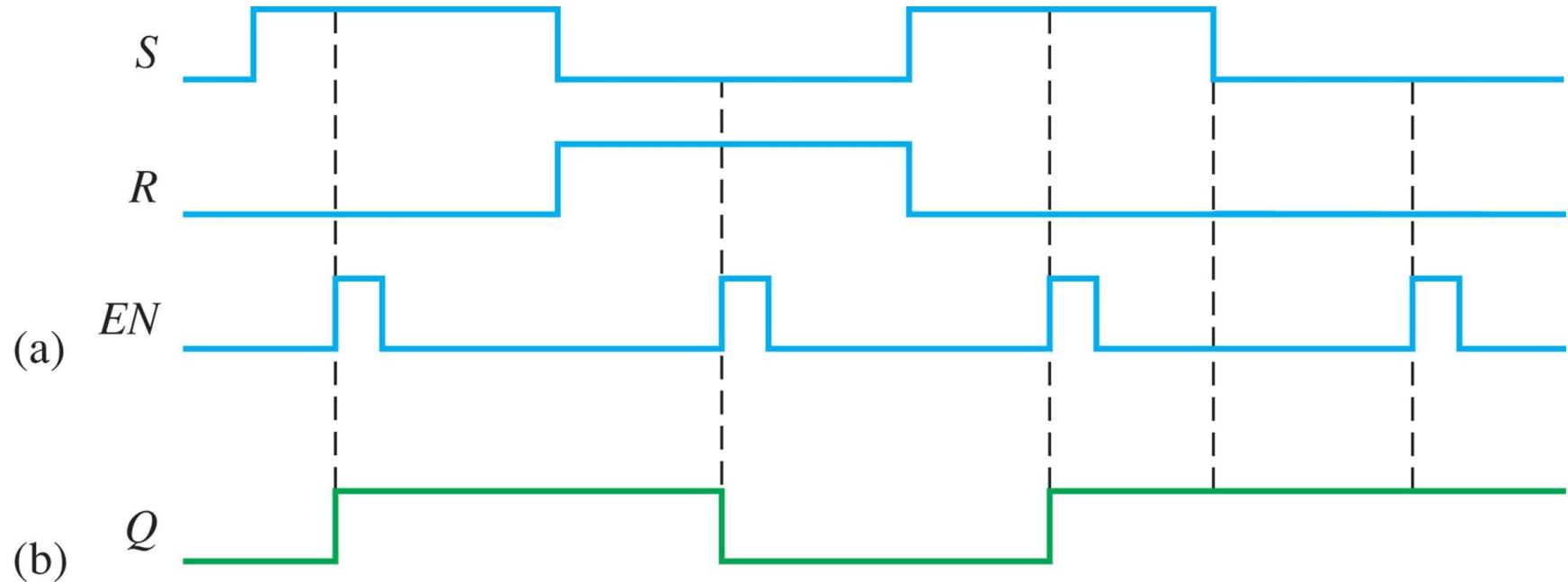
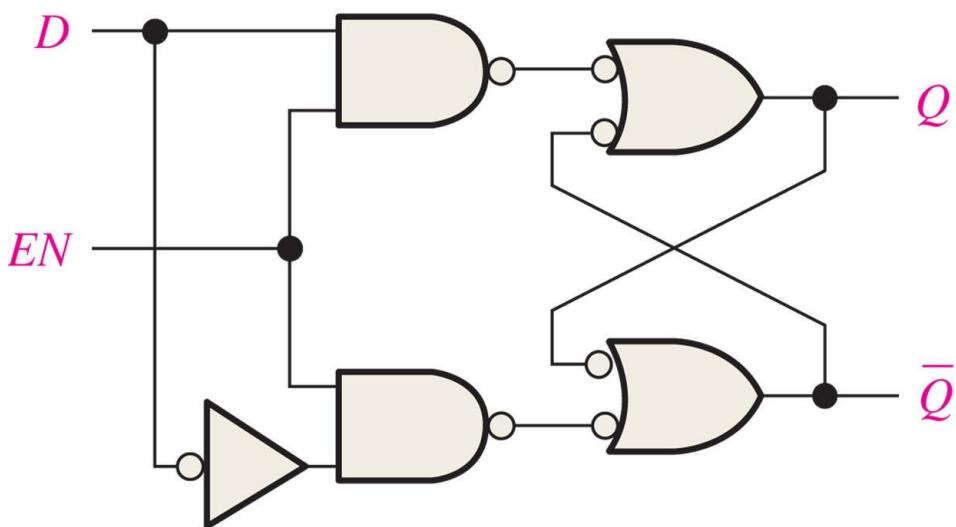
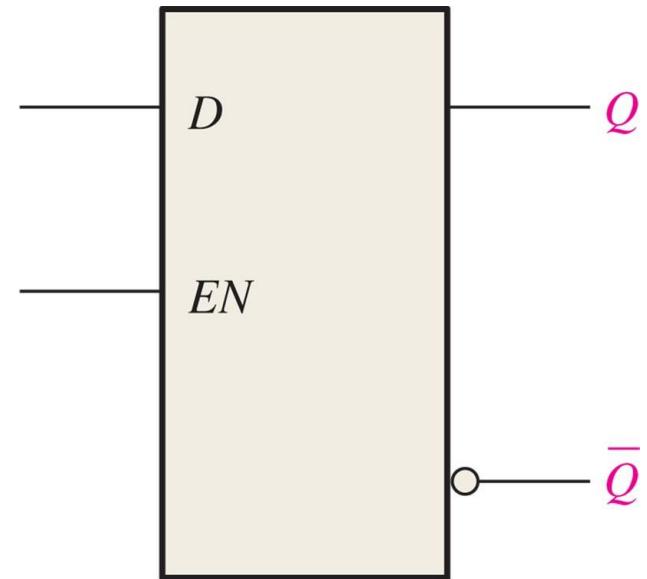


FIGURE 7-10 A gated D latch.



(a) Logic diagram



(b) Logic symbol

FIGURE 7-11

Determine the Q output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.

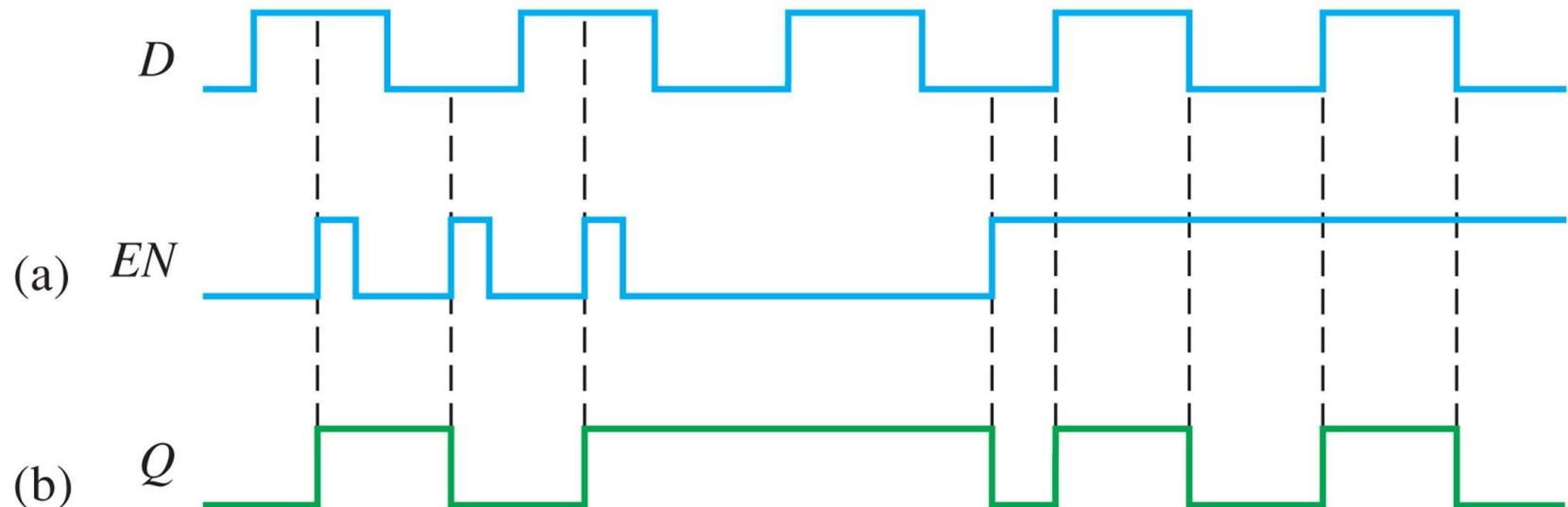
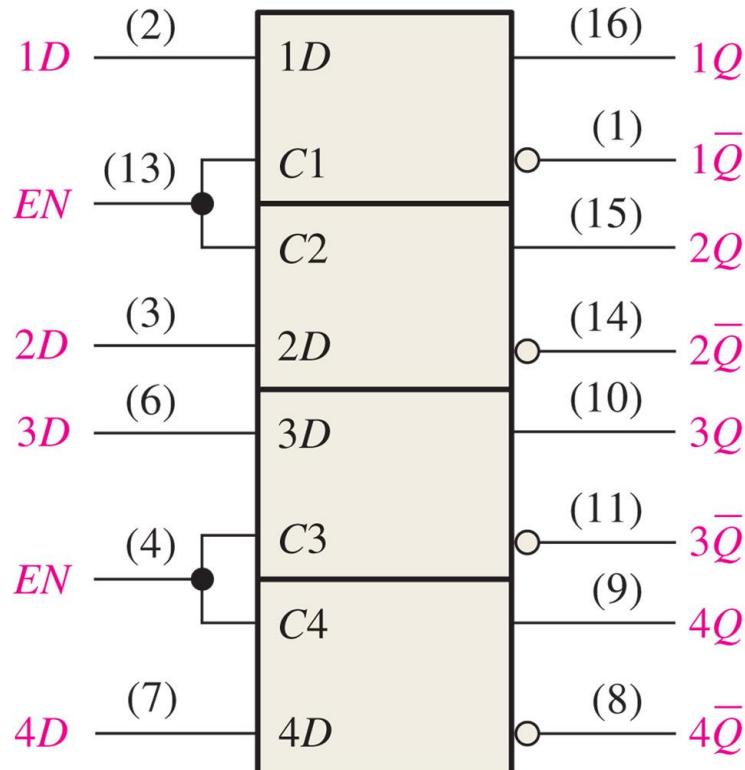


FIGURE 7-12 The 74HC75 quad D latch.



(a) Logic symbol

Inputs		Outputs		Comments
D	EN	Q	\bar{Q}	
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	\bar{Q}_0	No change

Note: Q_0 is the prior output level before the indicated input conditions were established.

(b) Truth table (each latch)

FIGURE 7-13 Edge-triggered flip-flop logic symbols (top: positive edge-triggered; bottom: negative edge-triggered).

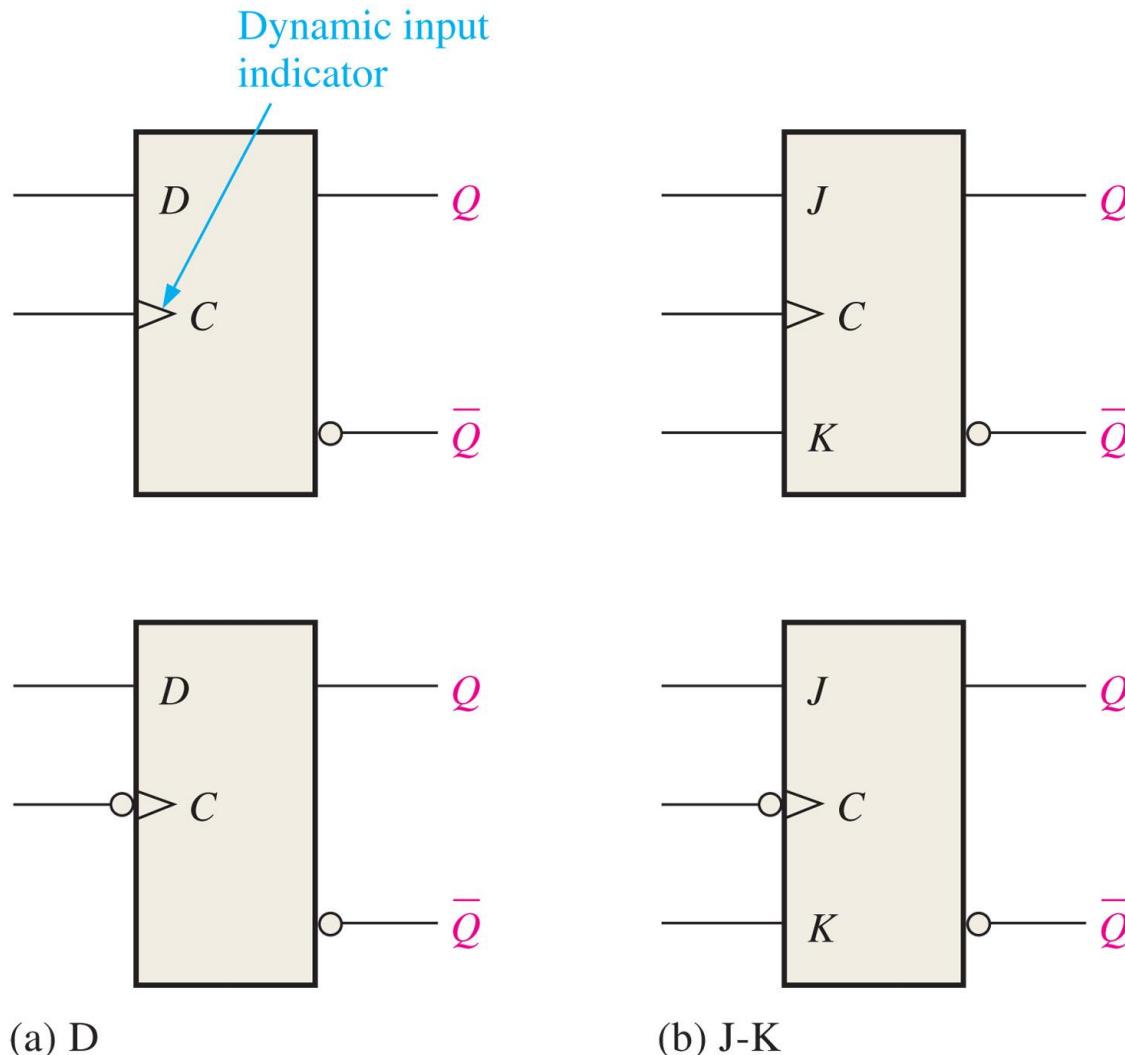
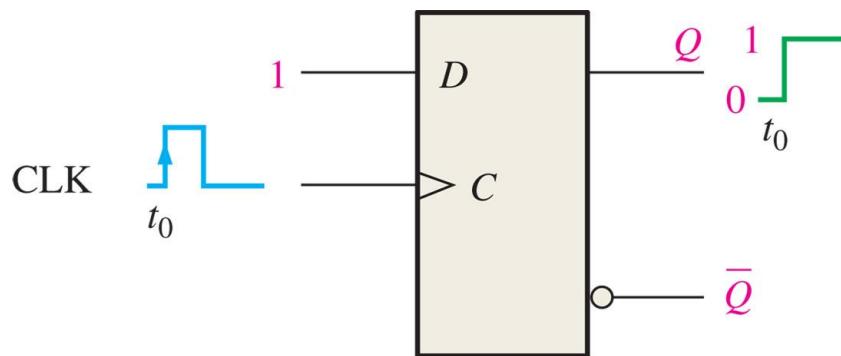
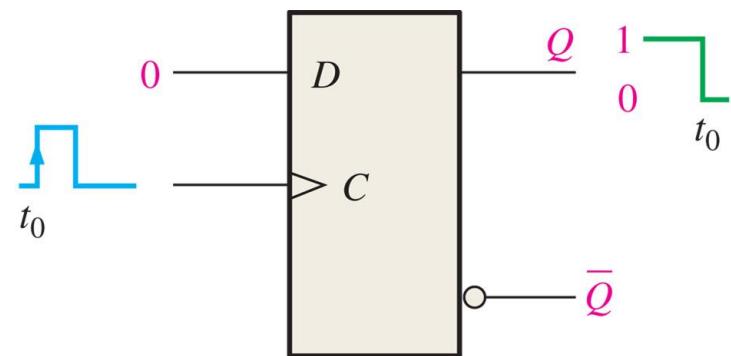


FIGURE 7-14 Operation of a positive edge-triggered D flip-flop.



(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

TABLE 7-2

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		Comments
D	CLK	Q	\bar{Q}	
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

FIGURE 7-15

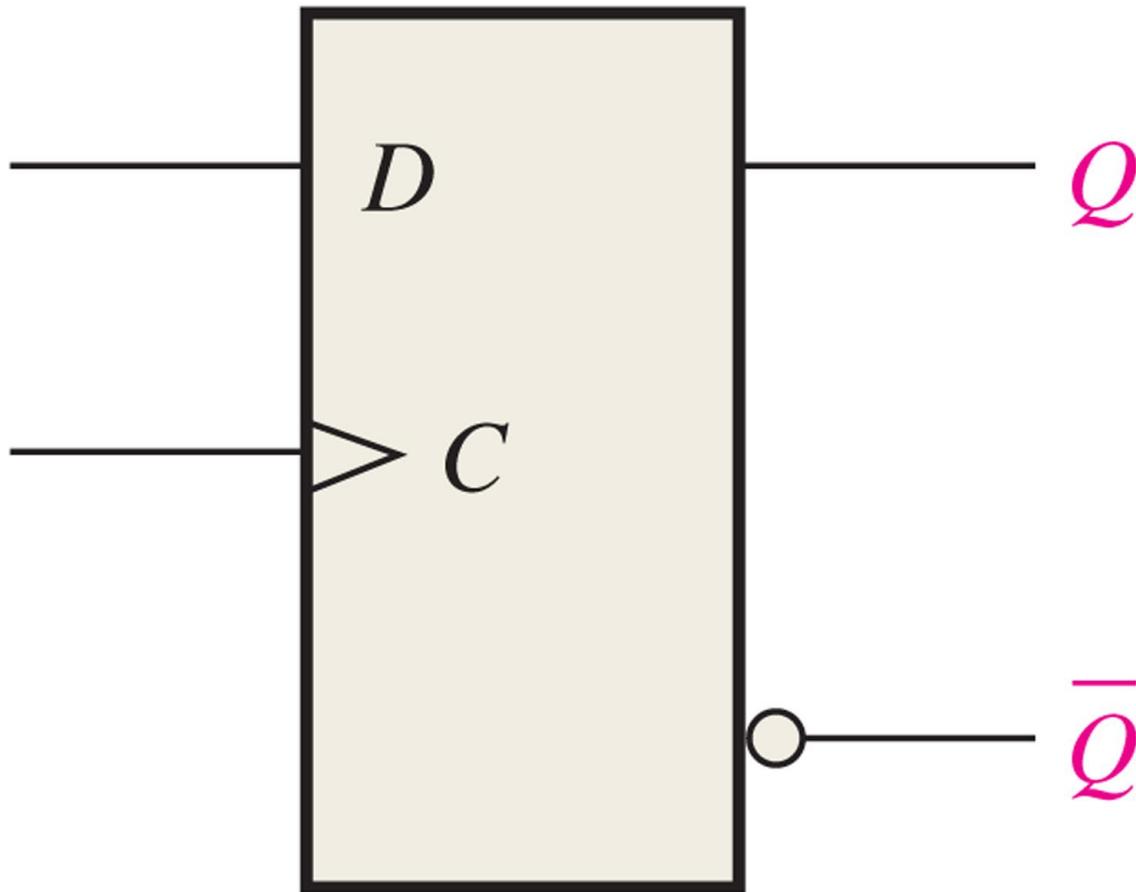


FIGURE 7-16

Determine the Q and \bar{Q} output waveforms of the flip-flop in Figure 7–15 for the D and CLK inputs in Figure 7–16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

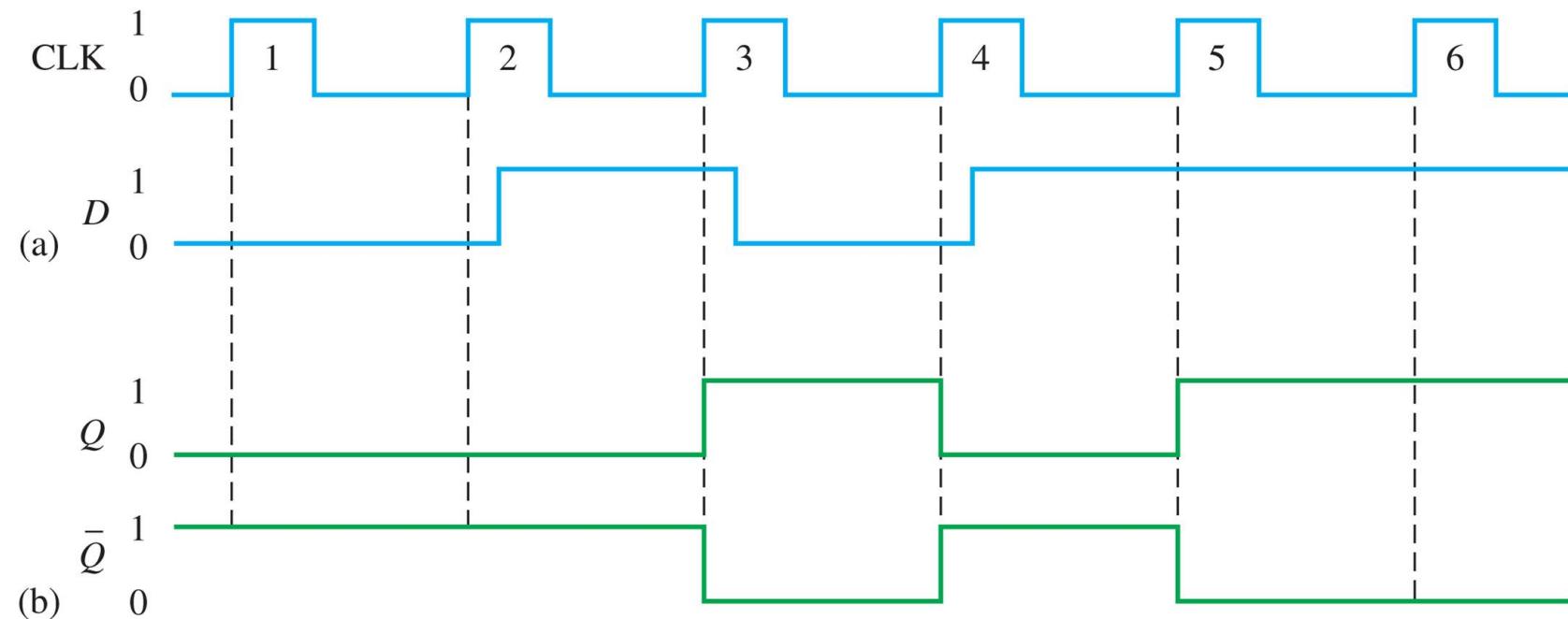
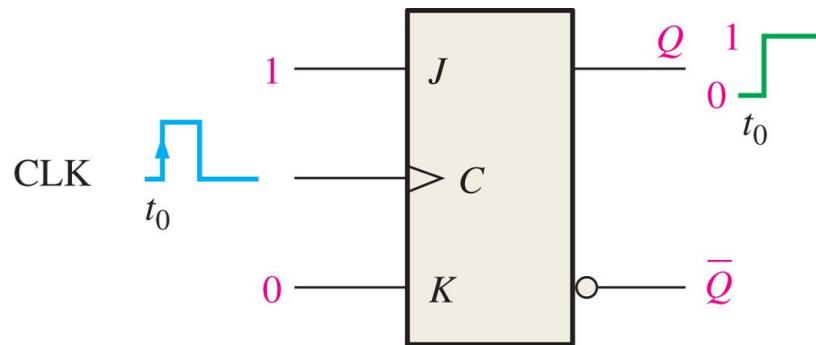
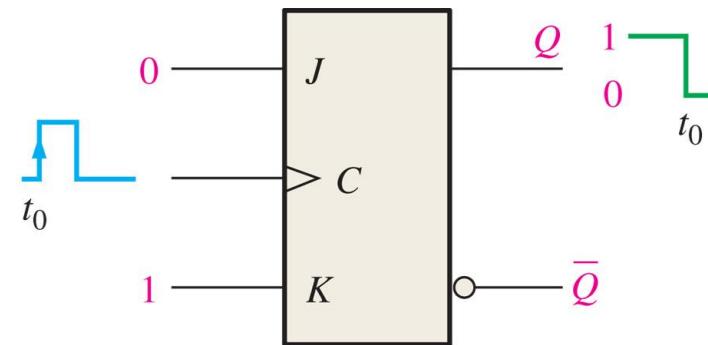


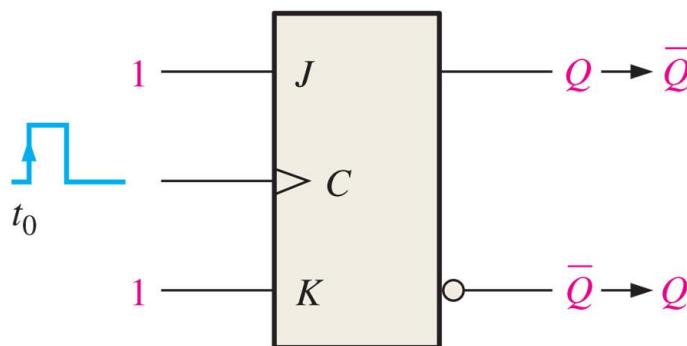
FIGURE 7-17 Operation of a positive edge-triggered J-K flip-flop.



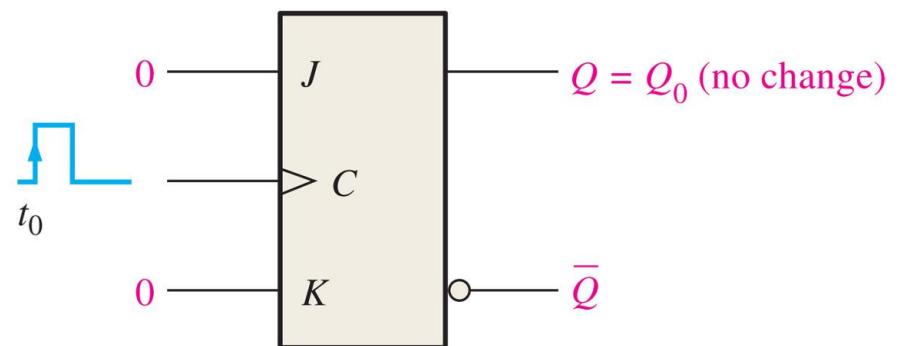
(a) $J = 1, K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $J = 0, K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $J = 1, K = 1$ flip-flop changes state (toggle).



(d) $J = 0, K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

TABLE 7–3

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		Comments
J	K	CLK	Q	\bar{Q}	
0	0	↑	Q_0	\bar{Q}_0	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	\bar{Q}_0	Q_0	Toggle

 \uparrow = clock transition LOW to HIGH Q_0 = output level prior to clock transition

FIGURE 7-18

The waveforms in Figure 7–18(a) are applied to the J, K, and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.

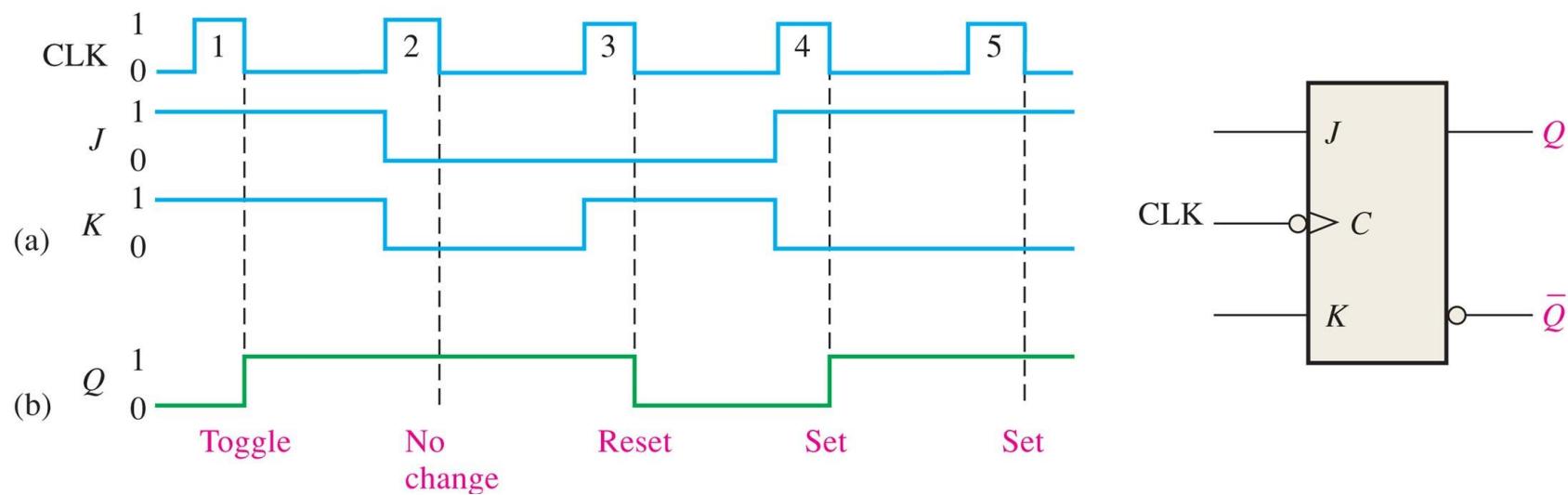
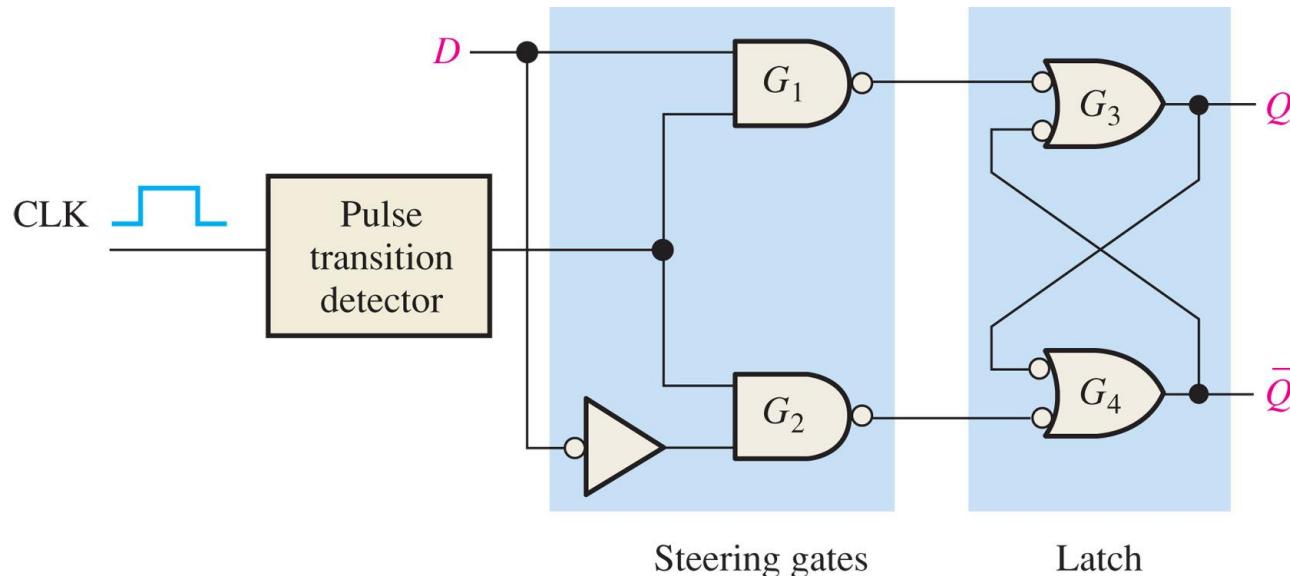
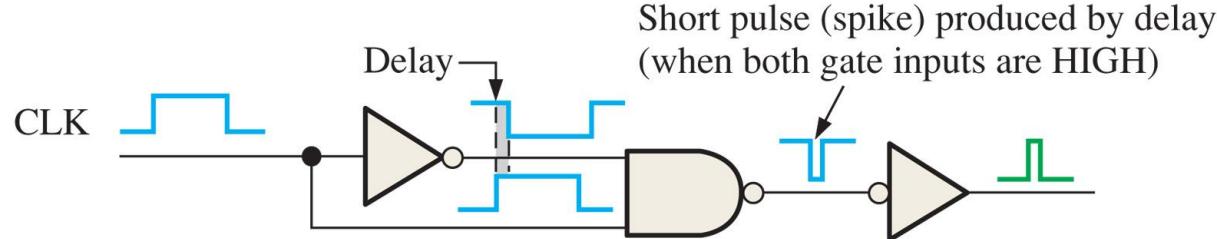


FIGURE 7-19 Edge triggering.

Notice that the basic D flip-flop differs from the gated D latch only in that it has a pulse transition detector



(a) A simplified logic diagram for a positive edge-triggered D flip-flop



(b) A type of pulse transition detector

FIGURE 7-20 Flip-flop making a transition from the RESET state to the SET state on the positive-going edge of the clock pulse.

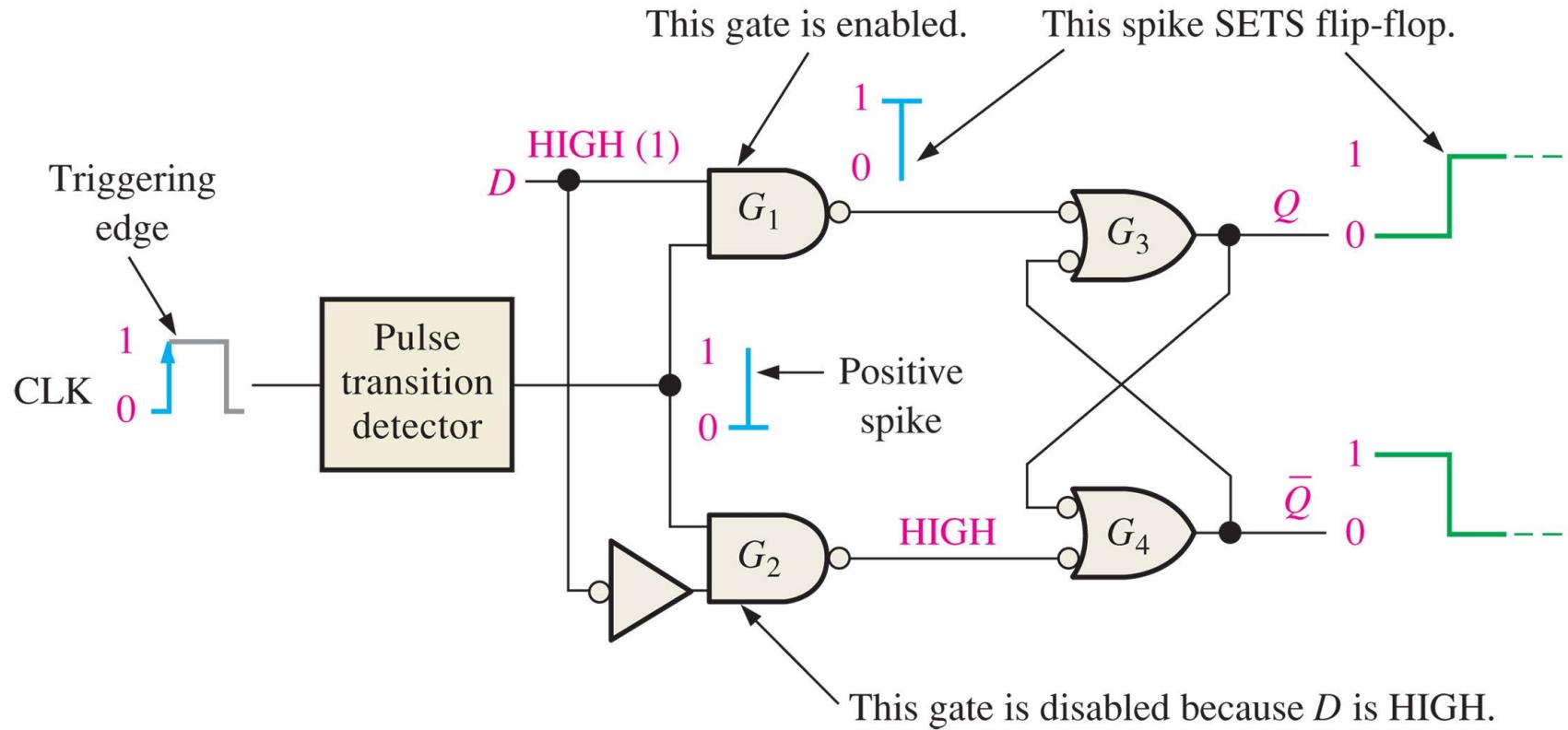


FIGURE 7-21 Flip-flop making a transition from the SET state to the RESET state on the positive-going edge of the clock pulse.

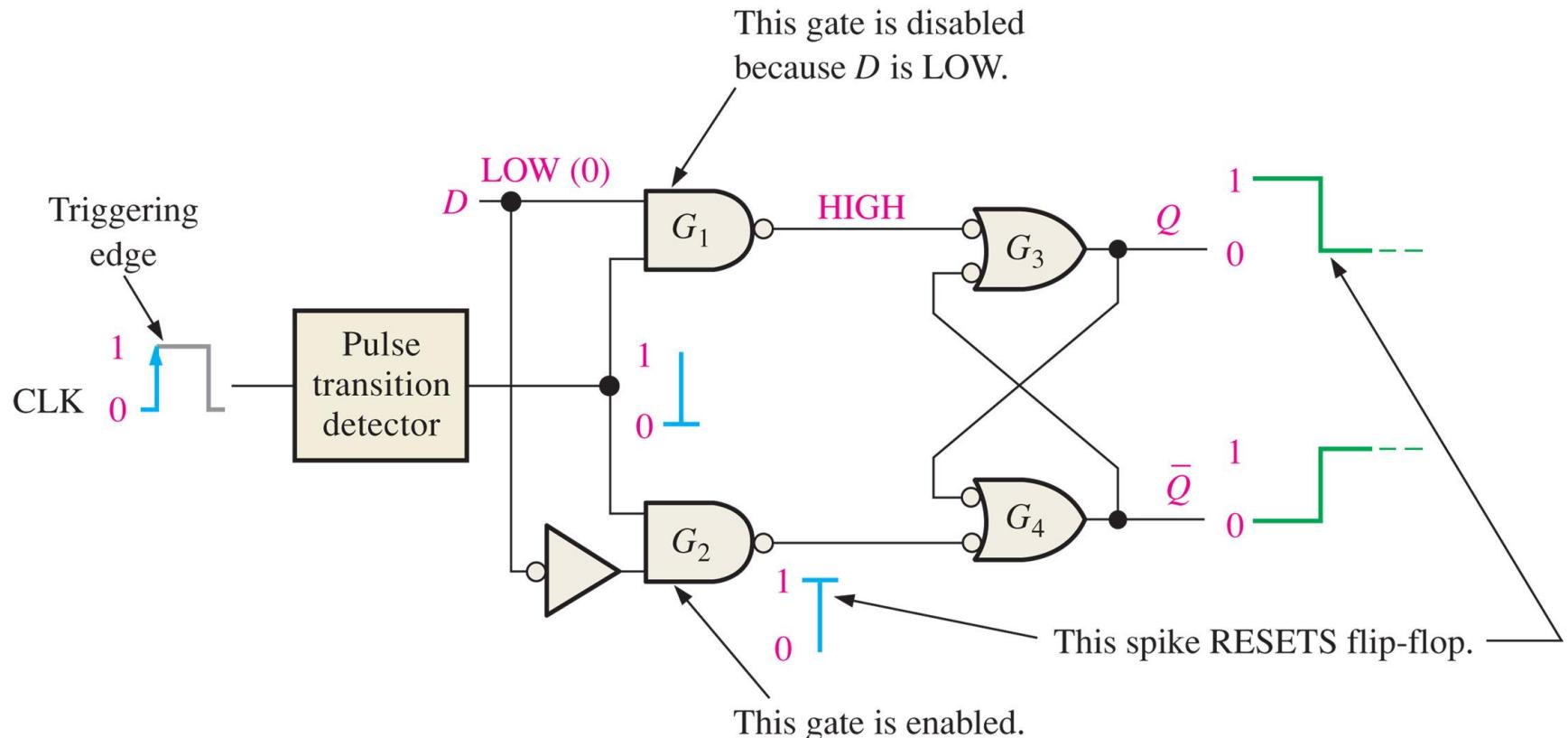
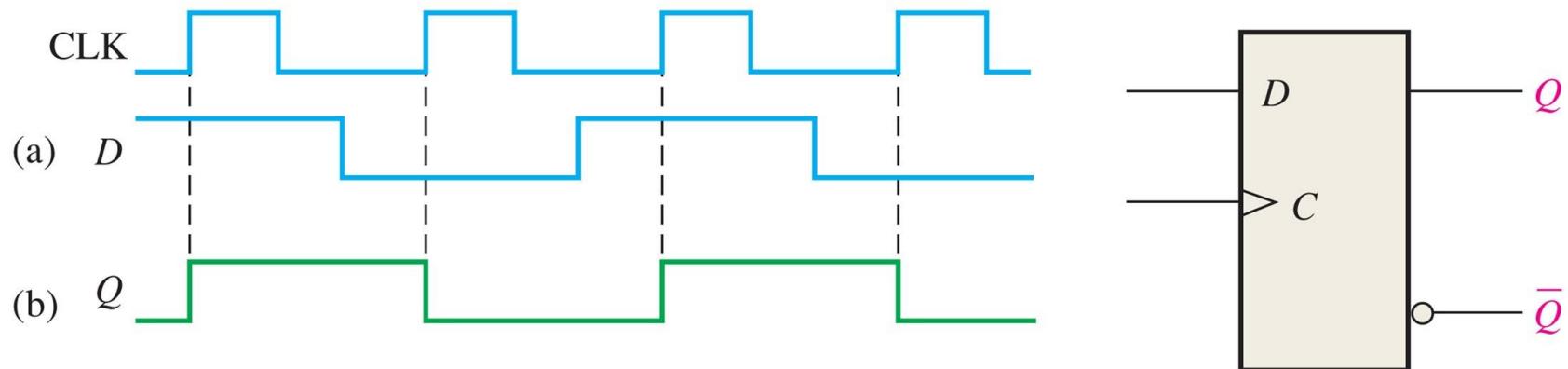


FIGURE 7-22

Given the waveforms in Figure 7–22(a) for the D input and the clock, determine the Q output waveform if the flip-flop starts out RESET.



J-K Flip-Flop

FIGURE 7-23 A simplified logic diagram for a positive edge-triggered J-K flip-flop.

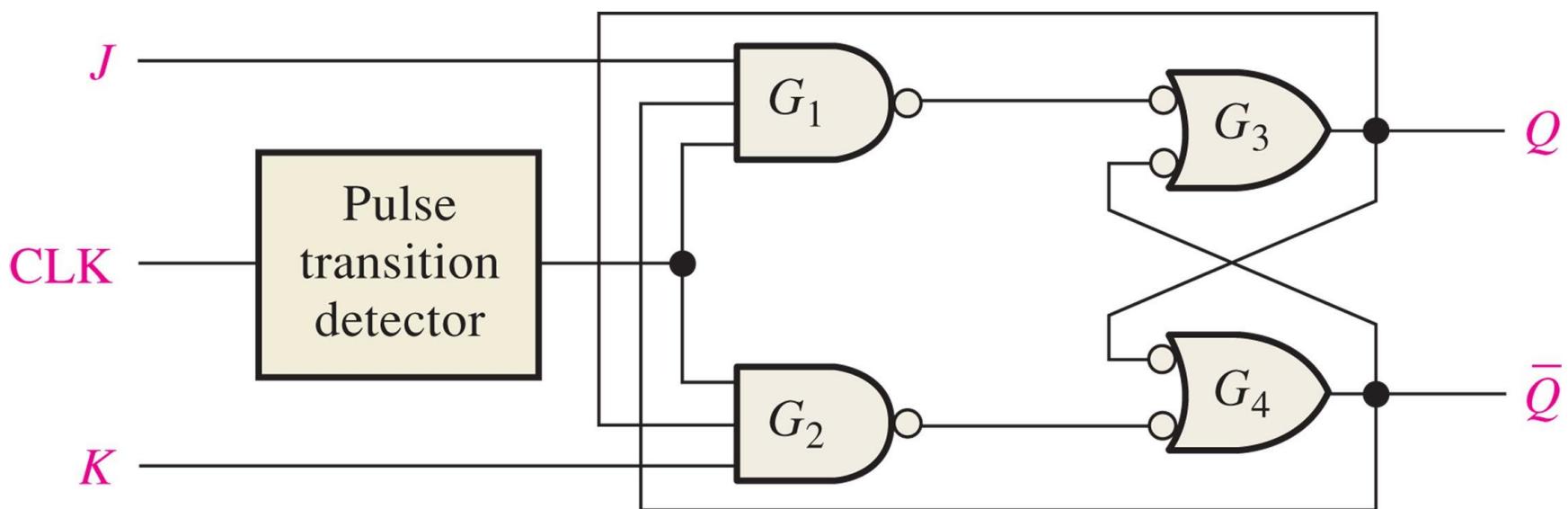


FIGURE 7-24 Transitions illustrating flip-flop operation.

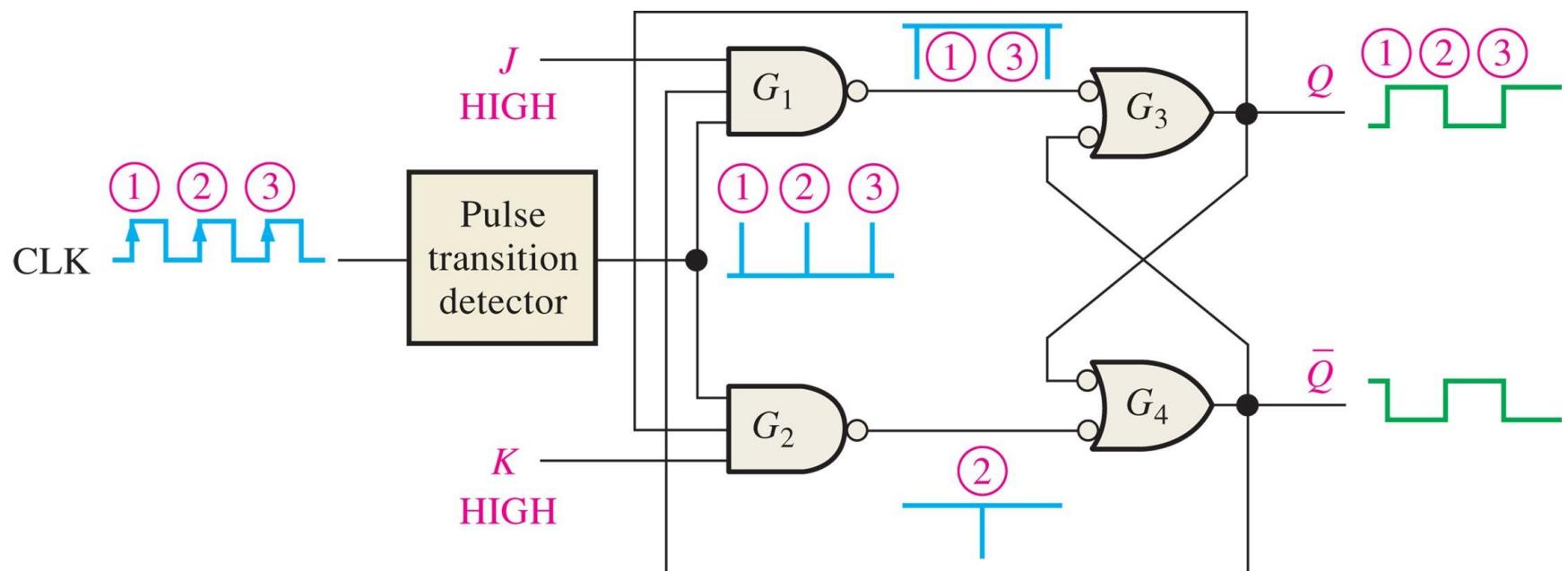


FIGURE 7-25 Logic symbol for a D flip-flop with active-LOW preset and clear inputs.

Most integrated circuit flip-flops also have asynchronous inputs. These are inputs that affect the state of the flip-flop independent of the clock. They are normally labeled preset (PRE) and clear (CLR)

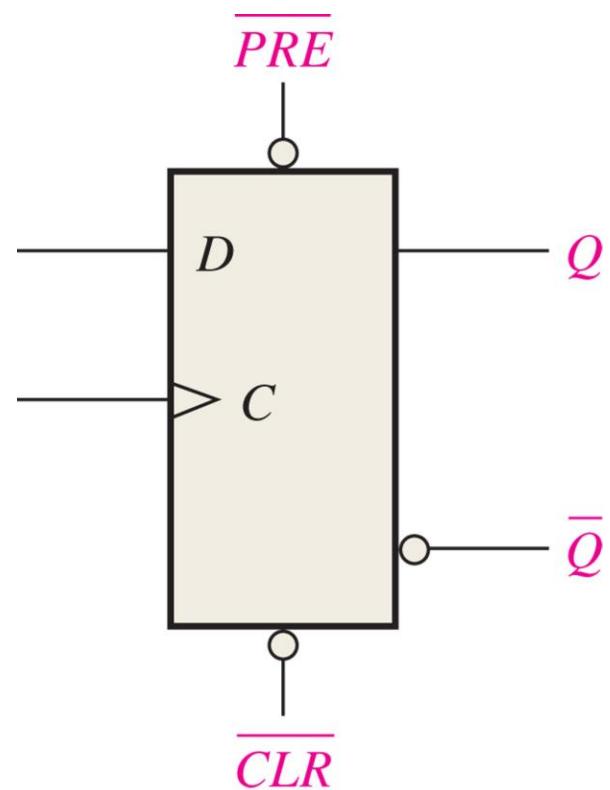
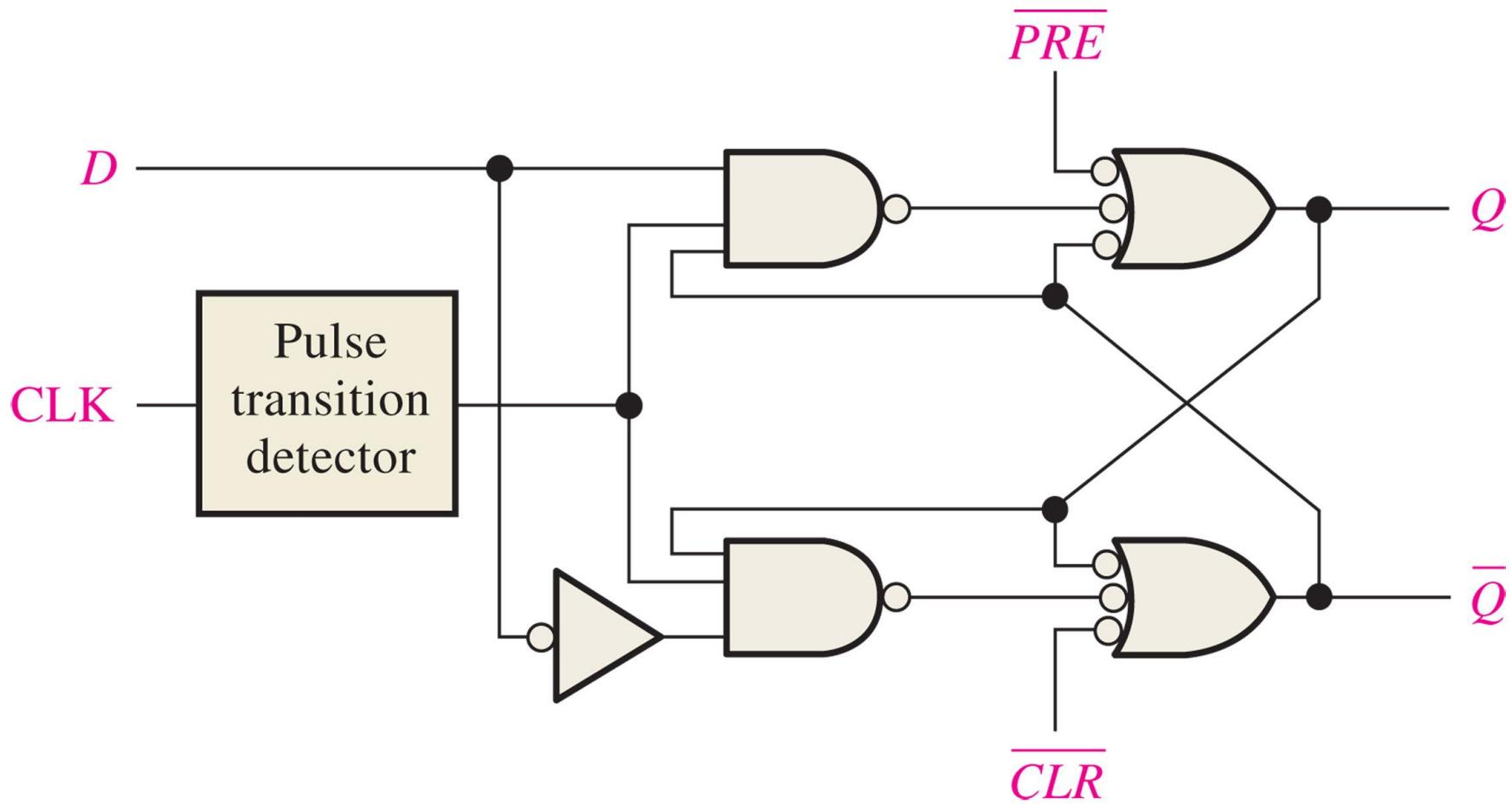


FIGURE 7-26 Logic diagram for a basic D flip-flop with active-LOW preset and clear inputs.



For the positive edge-triggered D flip-flop with preset and clear inputs in Figure 7–27, determine the Q output for the inputs shown in the timing diagram in part (a) if Q is initially LOW.

FIGURE 7-27

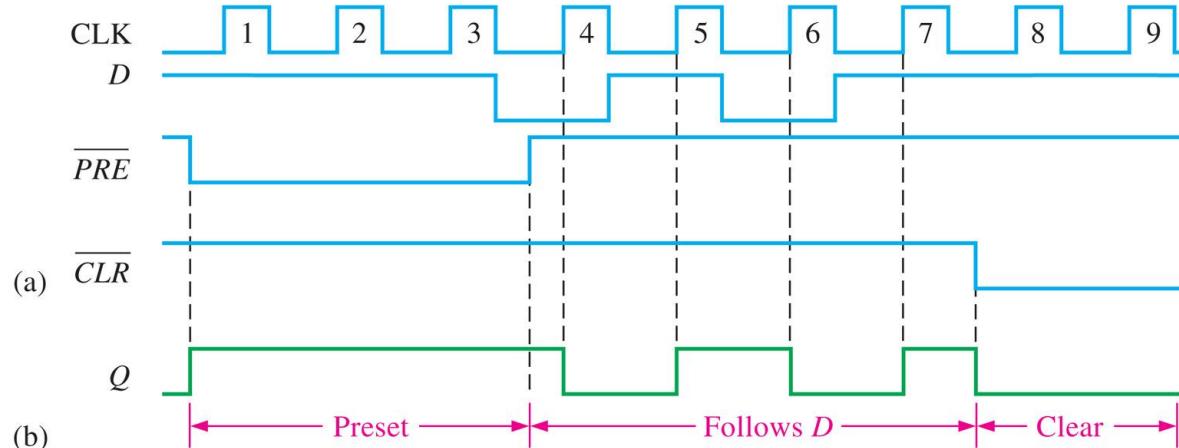
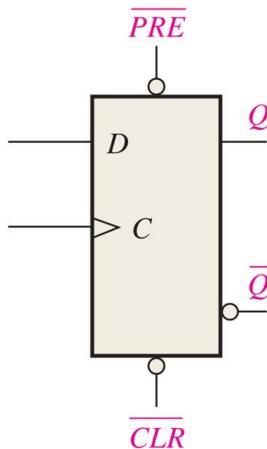
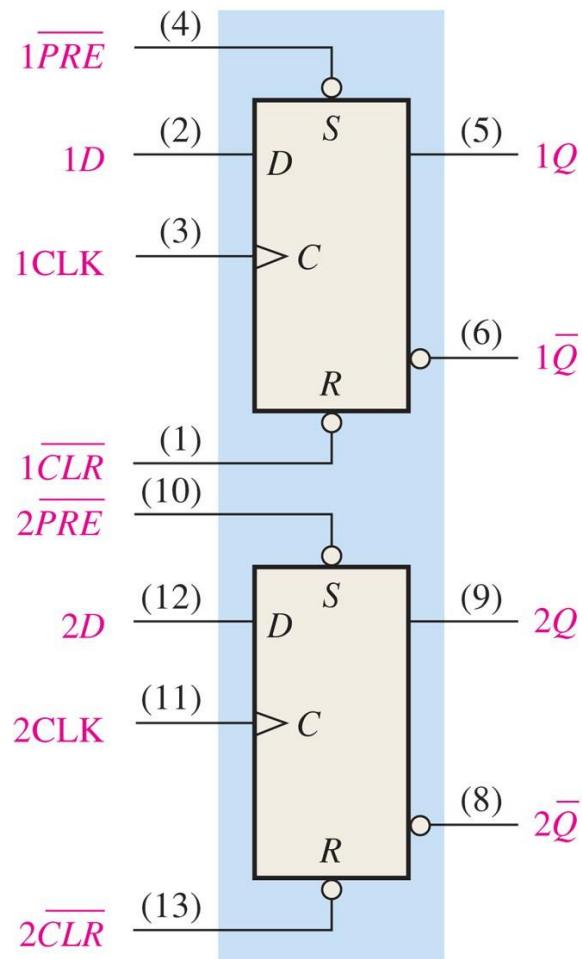
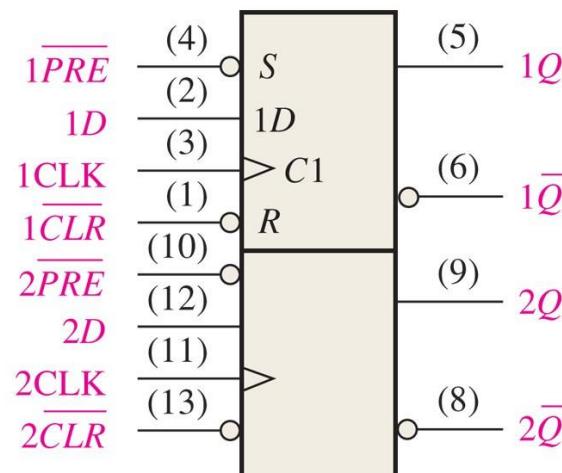


FIGURE 7-28 The 74HC74 dual positive edge-triggered D flip-flop.



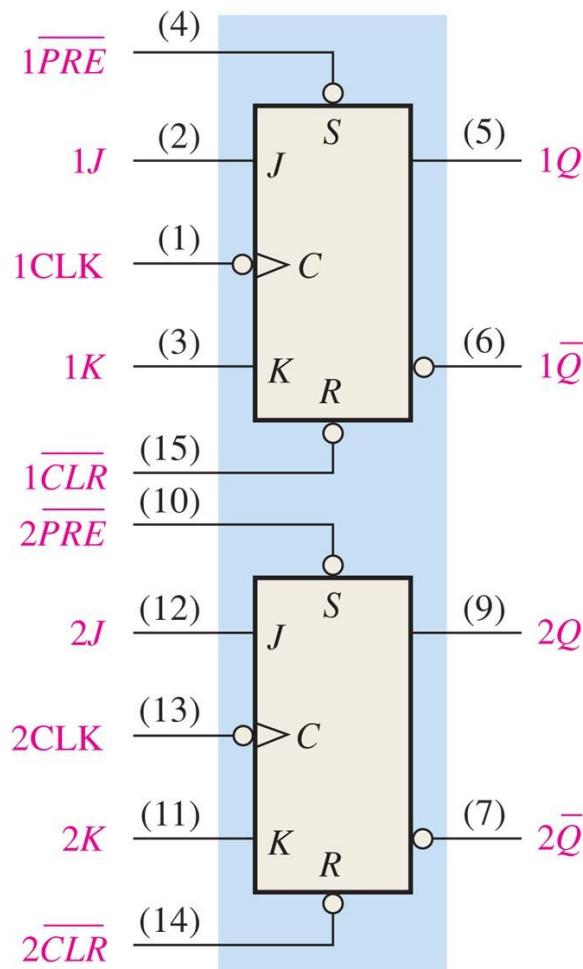
(a) Individual logic symbols



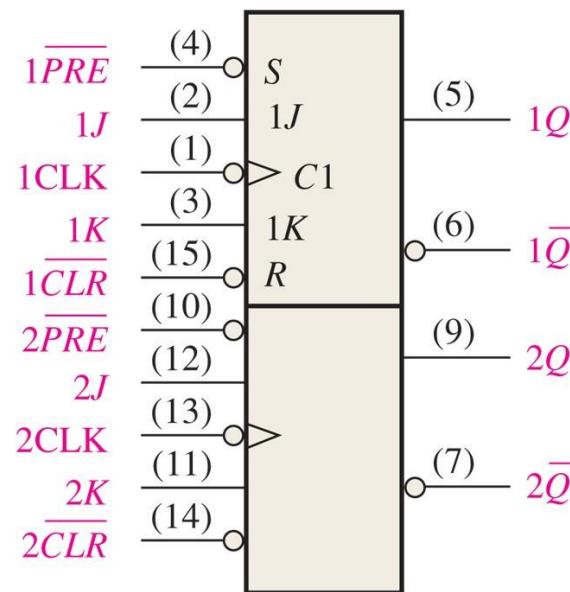
(b) Single block logic symbol

Note: The S and R inside the block indicate that \overline{PRE} SETS and \overline{CLR} RESETS.

FIGURE 7-29 The 74HC112 dual negative edge-triggered J-K flip-flop.



(a) Individual logic symbols



(b) Single block logic symbol

The 1J, 1K, 1CLK, 1PRE, and 1CLR waveforms in Figure 7–30(a) are applied to one of the negative edge-triggered flip-flops in a 74HC112 package. Determine the 1Q output waveform.

FIGURE 7-30

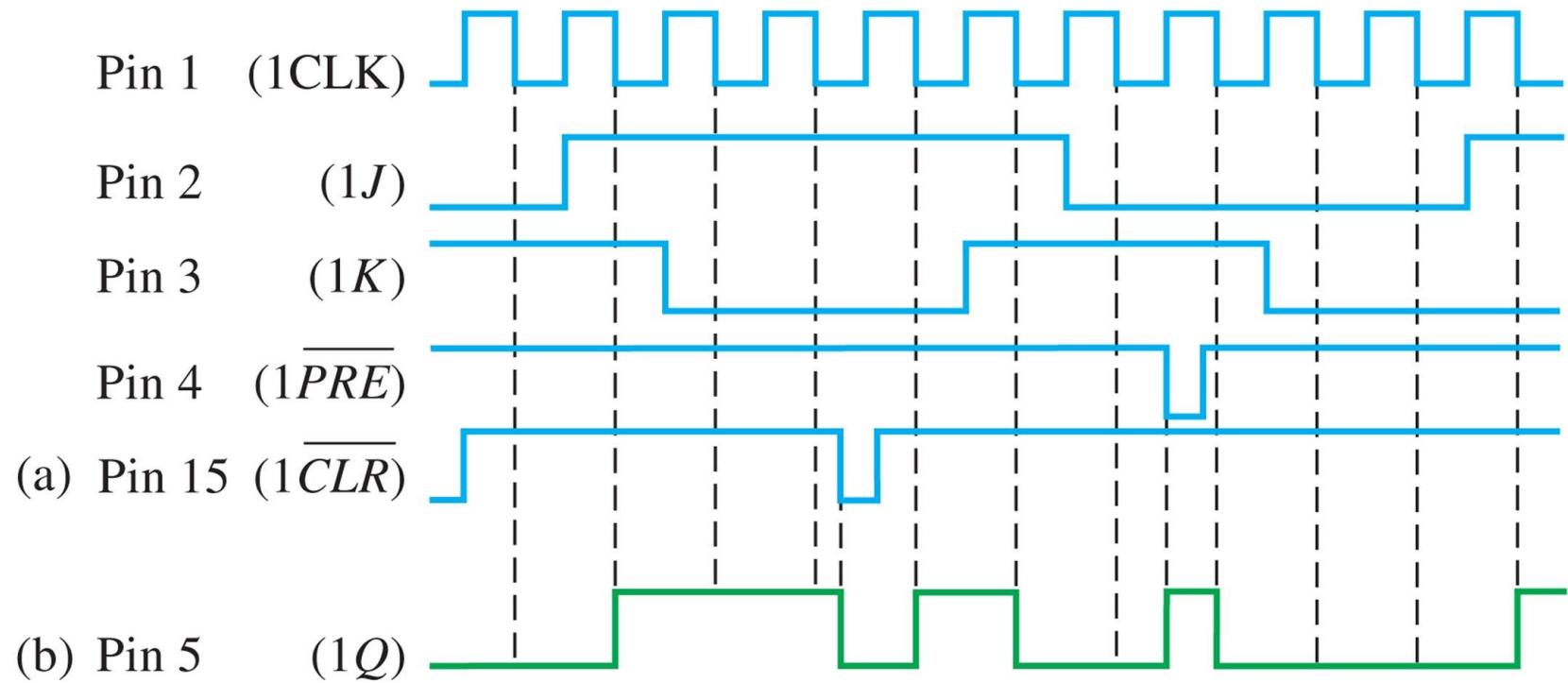
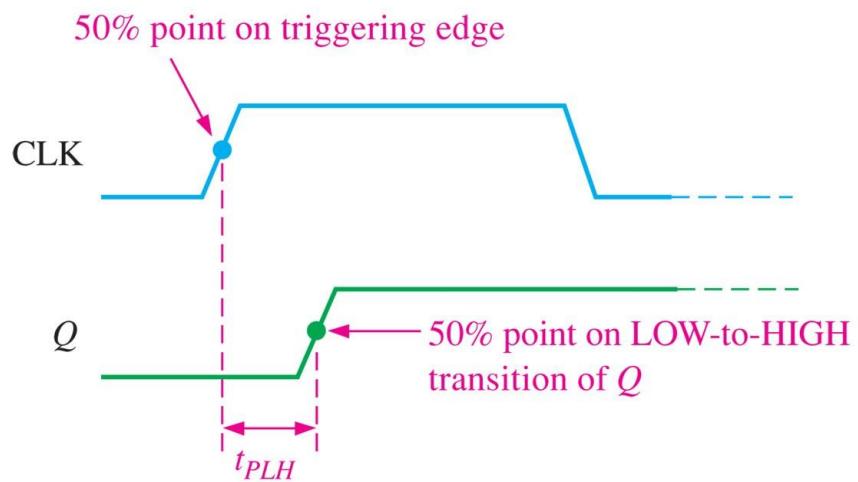
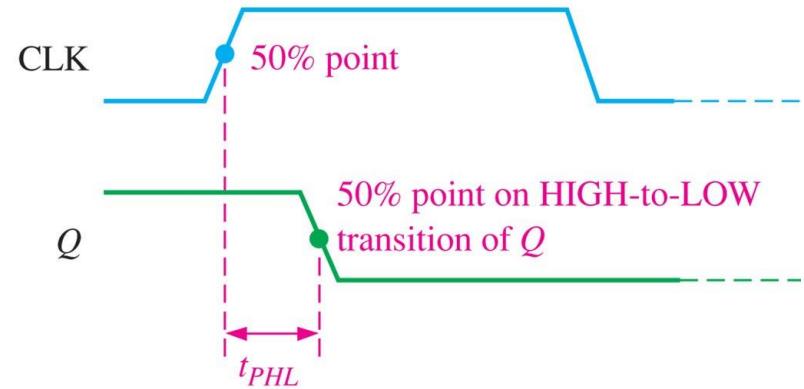


FIGURE 7-31 Propagation delays, clock to output.

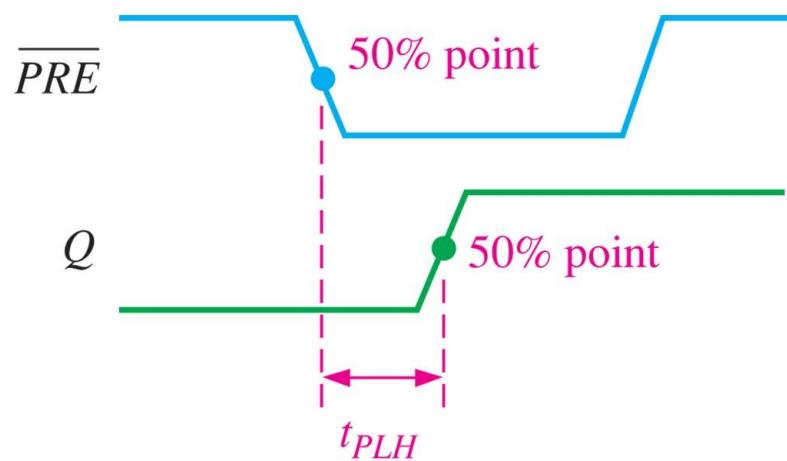


(a)

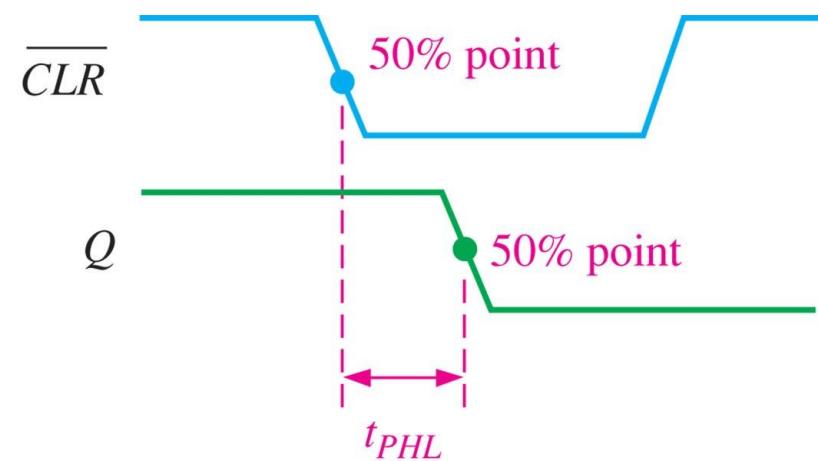


(b)

FIGURE 7-32 Propagation delays, preset input to output and clear input to output.



(a)



(b)

FIGURE 7-33 Set-up time (t_s). The logic level must be present on the D input for a time equal to or greater than t_s before the triggering edge of the clock pulse for reliable data entry.

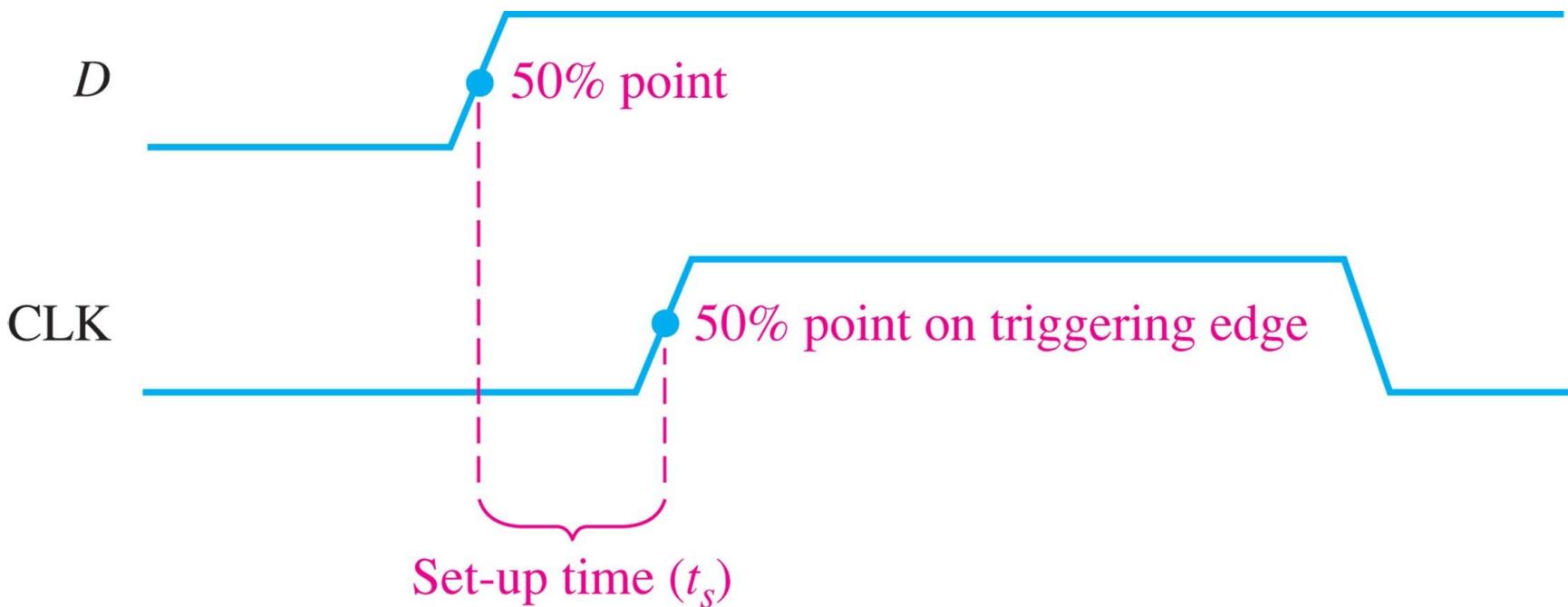


FIGURE 7-34 Hold time (t_h). The logic level must remain on the D input for a time equal to or greater than t_h after the triggering edge of the clock pulse for reliable data entry.

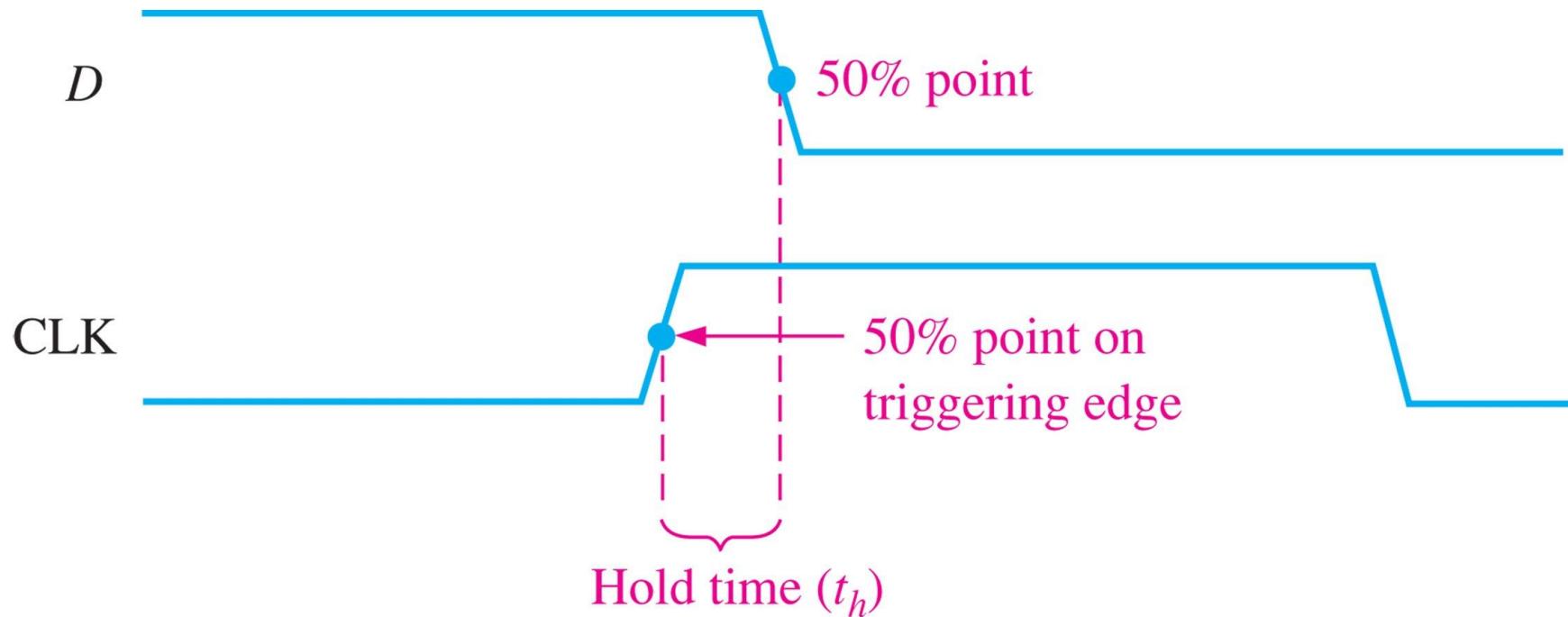
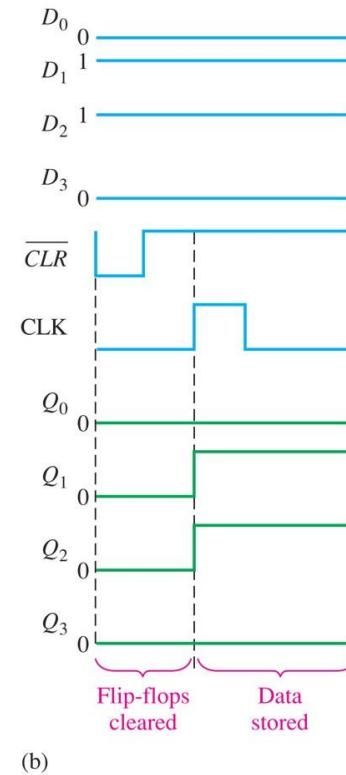
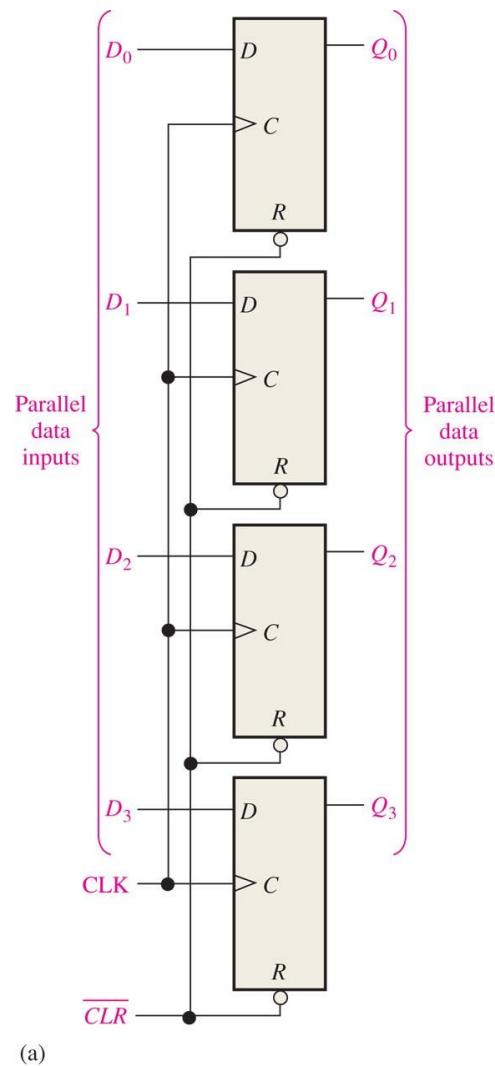


TABLE 7-4

Comparison of operating parameters for four IC families of flip-flops of the same type at 25°C.

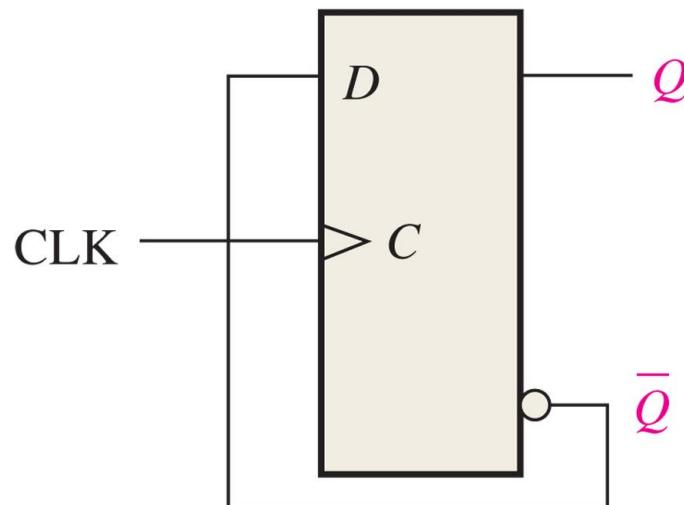
Parameter	CMOS		Bipolar (TTL)	
	74HC74A	74AHC74	74LS74A	74F74
t_{PHL} (CLK to Q)	17 ns	4.6 ns	40 ns	6.8 ns
t_{PLH} (CLK to Q)	17 ns	4.6 ns	25 ns	8.0 ns
$t_{PHL}(\overline{CLR}$ to Q)	18 ns	4.8 ns	40 ns	9.0 ns
$t_{PLH}(\overline{PRE}$ to Q)	18 ns	4.8 ns	25 ns	6.1 ns
t_s (set-up time)	14 ns	5.0 ns	20 ns	2.0 ns
t_h (hold time)	3.0 ns	0.5 ns	5 ns	1.0 ns
t_W (CLK HIGH)	10 ns	5.0 ns	25 ns	4.0 ns
t_W (CLK LOW)	10 ns	5.0 ns	25 ns	5.0 ns
$t_W(\overline{CLR}/\overline{PRE})$	10 ns	5.0 ns	25 ns	4.0 ns
f_{max}	35 MHz	170 MHz	25 MHz	100 MHz
Power, quiescent	0.012 mW	1.1 mW		
Power, 50% duty cycle			44 mW	88 mW

FIGURE 7-35 Example of flip-flops used in a basic register for parallel data storage.

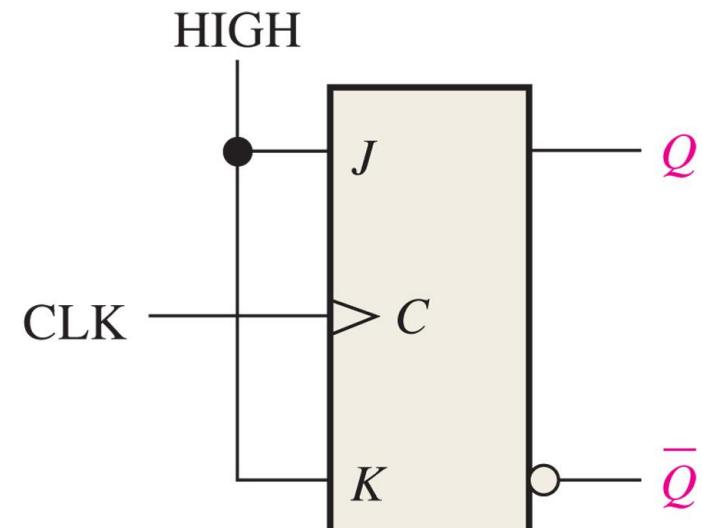


(b)

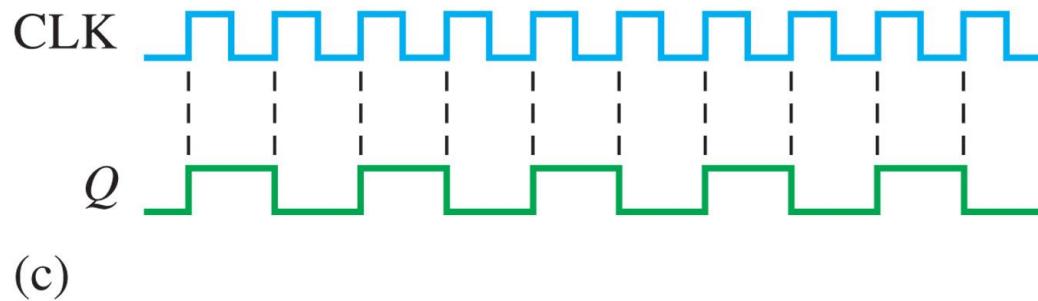
FIGURE 7-36 The D flip-flop and J-K flip-flop as a divide-by-2 device.
 Q is one-half the frequency of CLK.



(a)

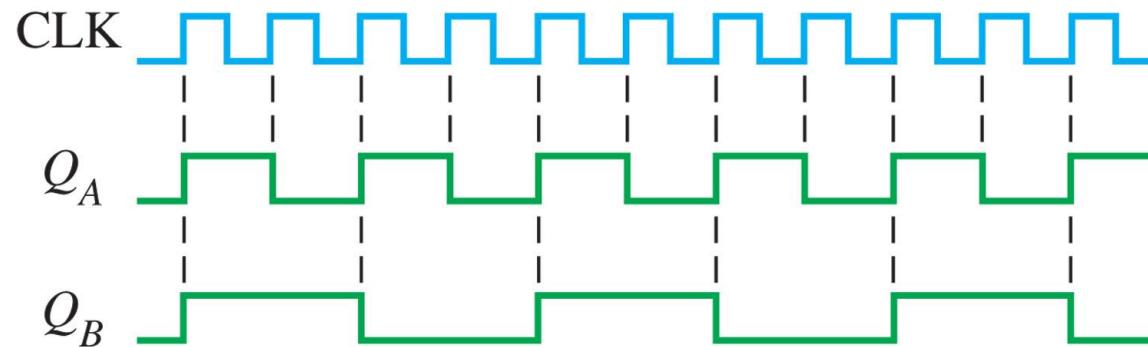
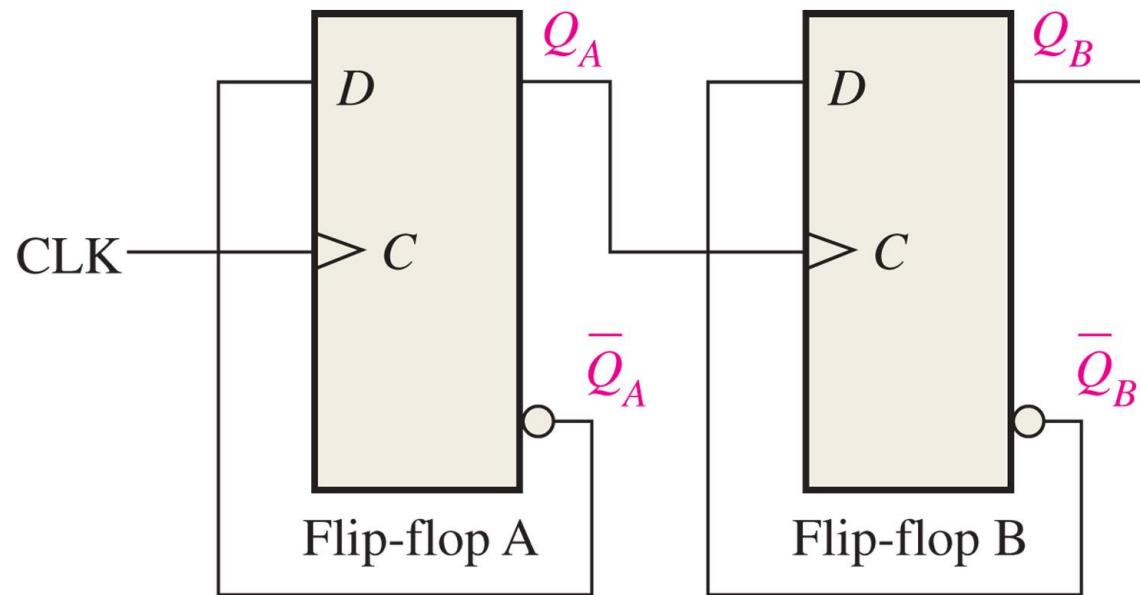


(b)



(c)

FIGURE 7-37 Example of two D flip-flops used to divide the clock frequency by 4. Q_A is one-half and Q_B is one-fourth the frequency of CLK.



The three flip-flops are connected to divide the input frequency by eight ($2^3 = 8$) and the QC (fout) waveform is shown in Figure 7–39. Since these are positive edge-triggered flip-flops, the outputs change on the positive-going clock edge. There is one output pulse for every eight input pulses, so the output frequency is 1 kHz. Waveforms of QA and QB are also shown.

FIGURE 7-38

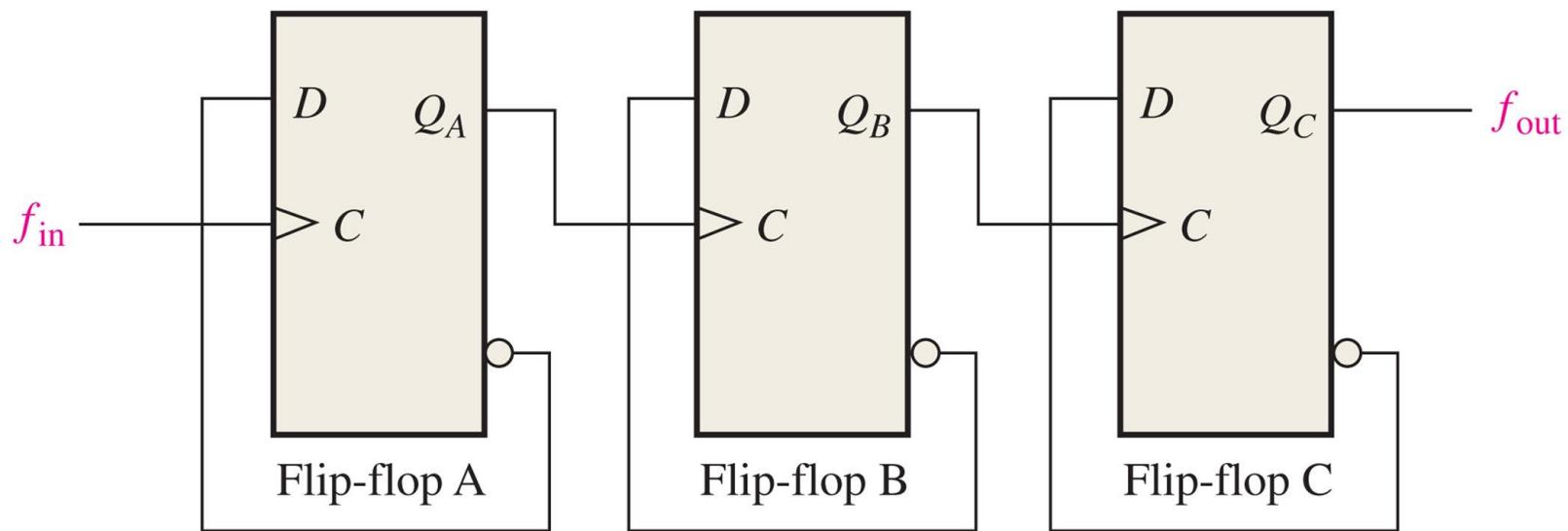


FIGURE 7-39

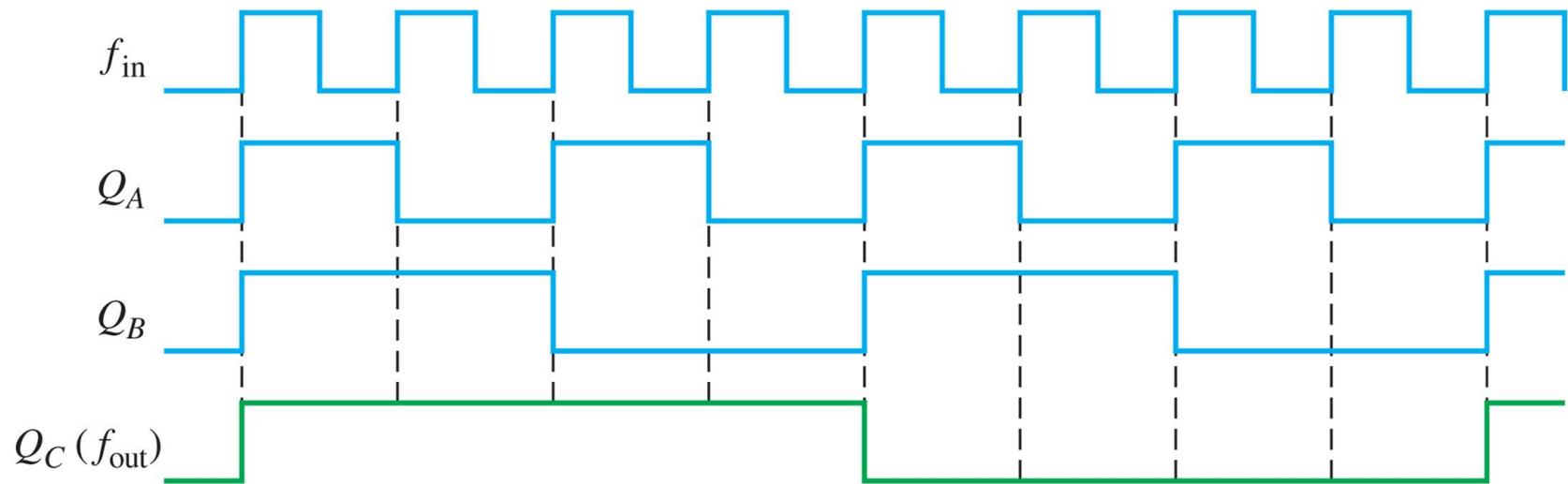


FIGURE 7-40 J-K flip-flops used to generate a binary count sequence (00, 01, 10, 11). Two repetitions are shown.

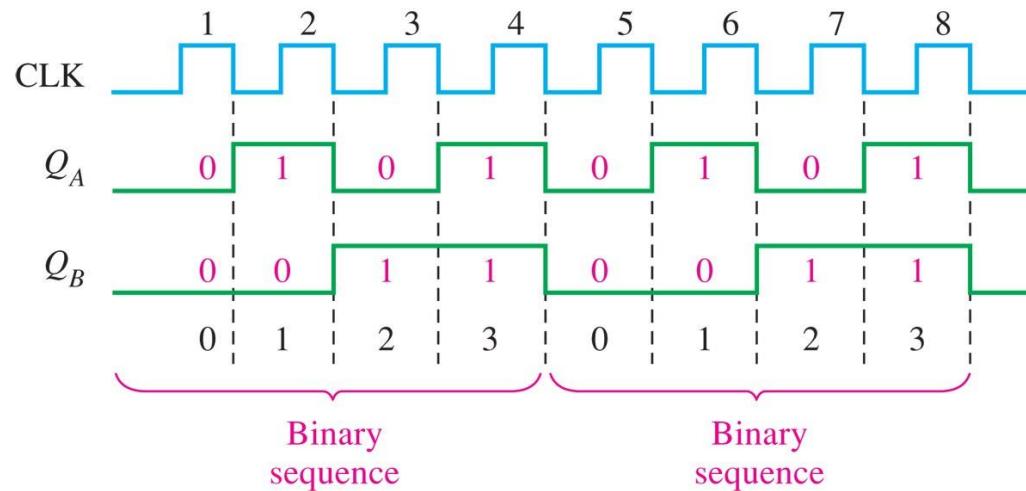
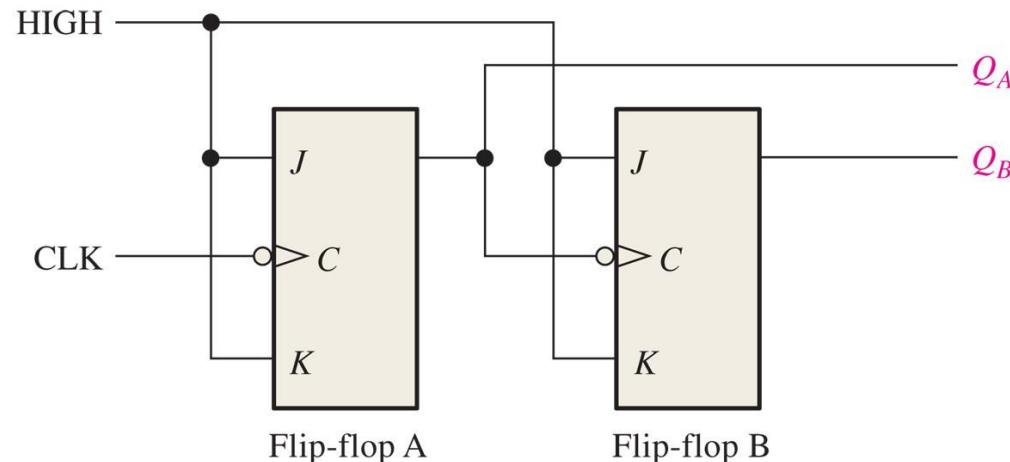


FIGURE 7-41

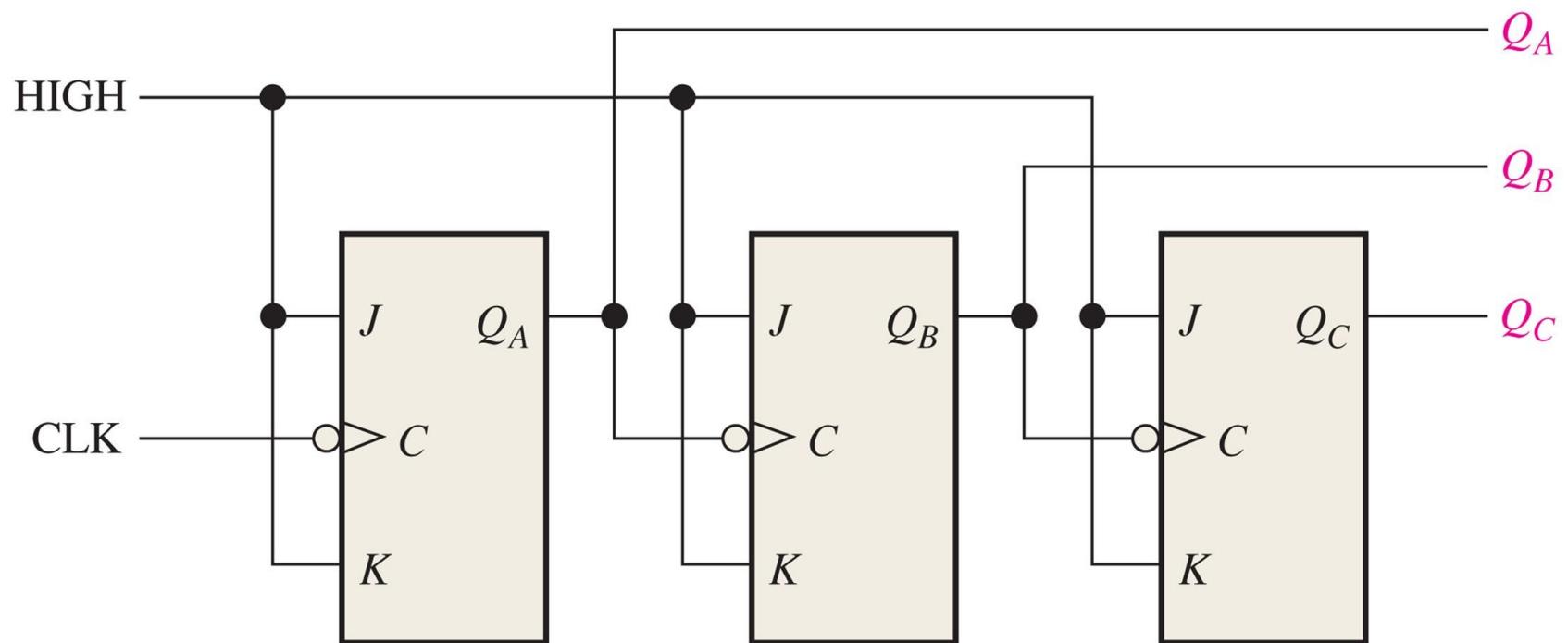
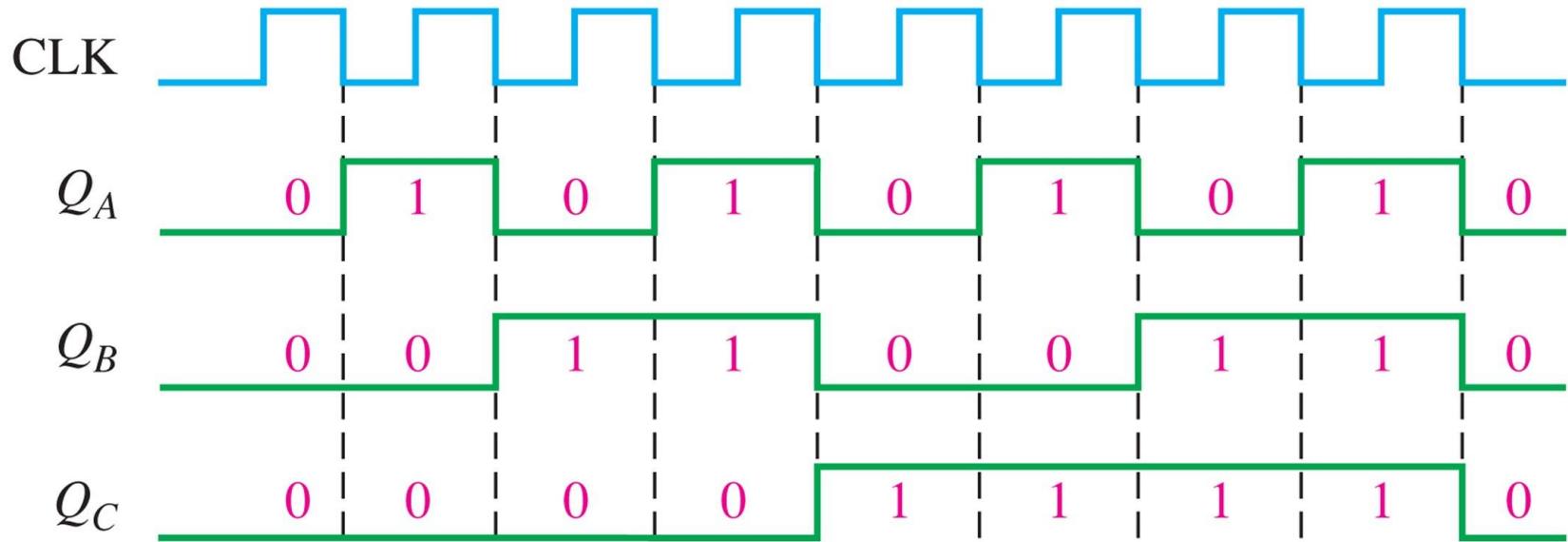


FIGURE 7-42



The output timing diagram is shown in Figure 7–42. Notice that the outputs change on the negative-going edge of the clock pulses. The outputs go through the binary sequence 000, 001, 010, 011, 100, 101, 110, and 111 as indicated.

FIGURE 7-43 A simple one-shot circuit.

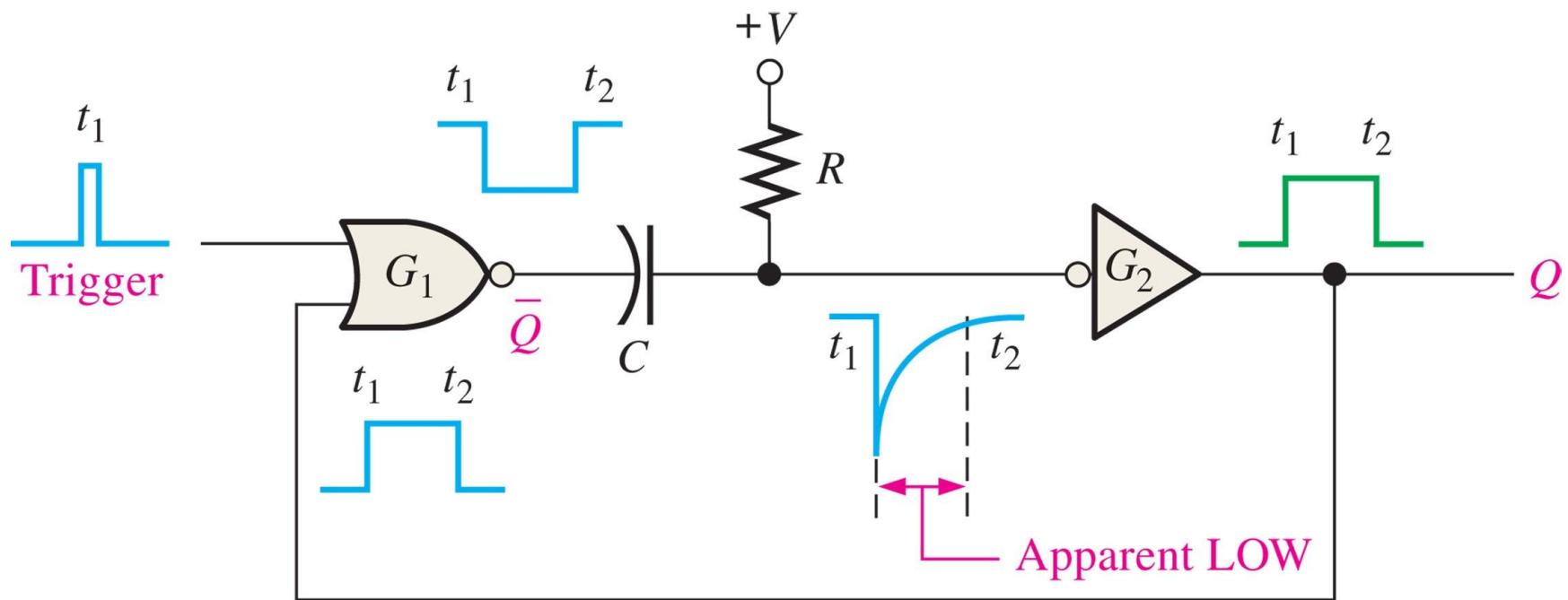


FIGURE 7-52 Internal functional diagram of a 555 timer (pin numbers are in parentheses).

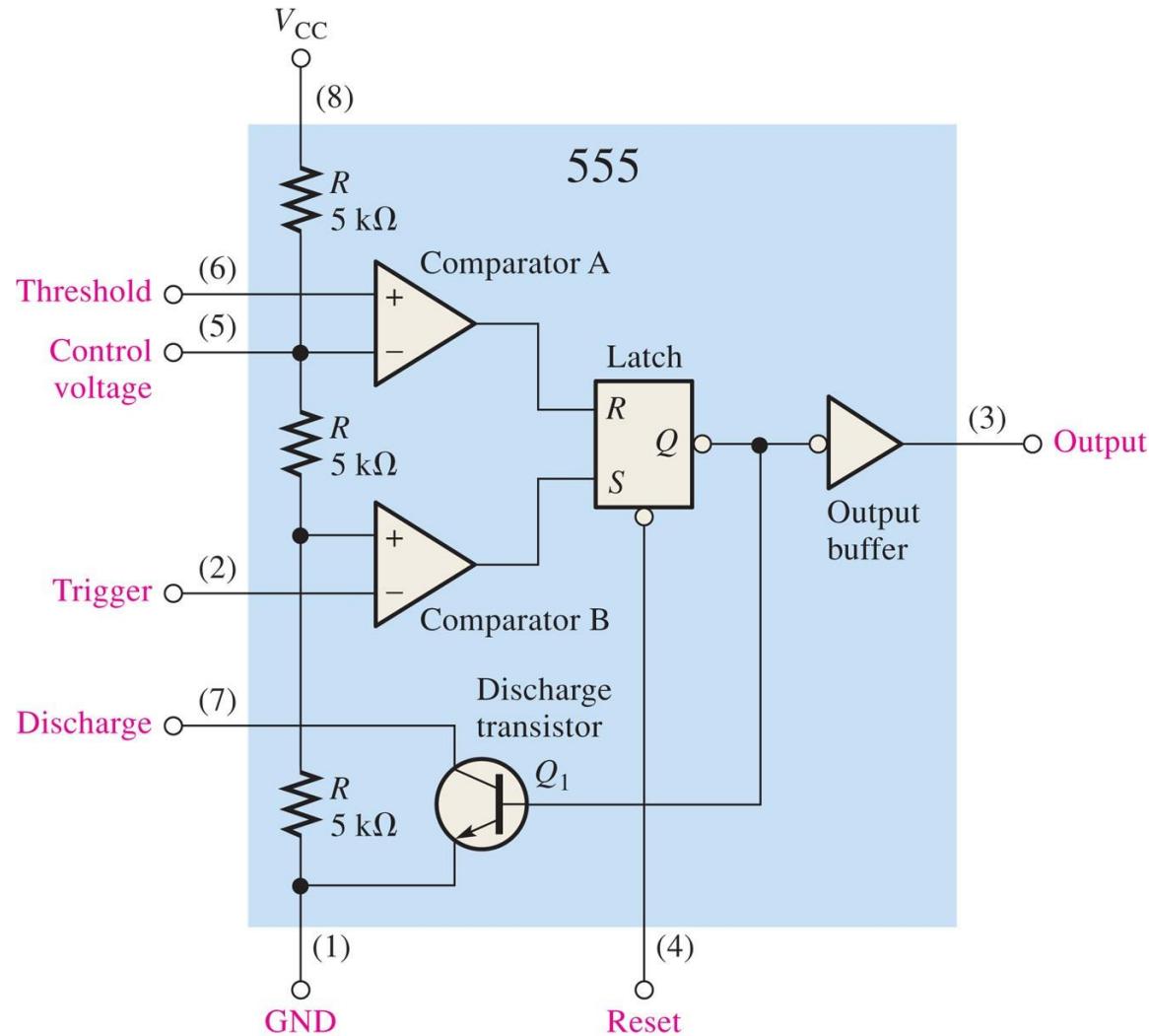


FIGURE 7-56 The 555 timer connected as an astable multivibrator (oscillator).

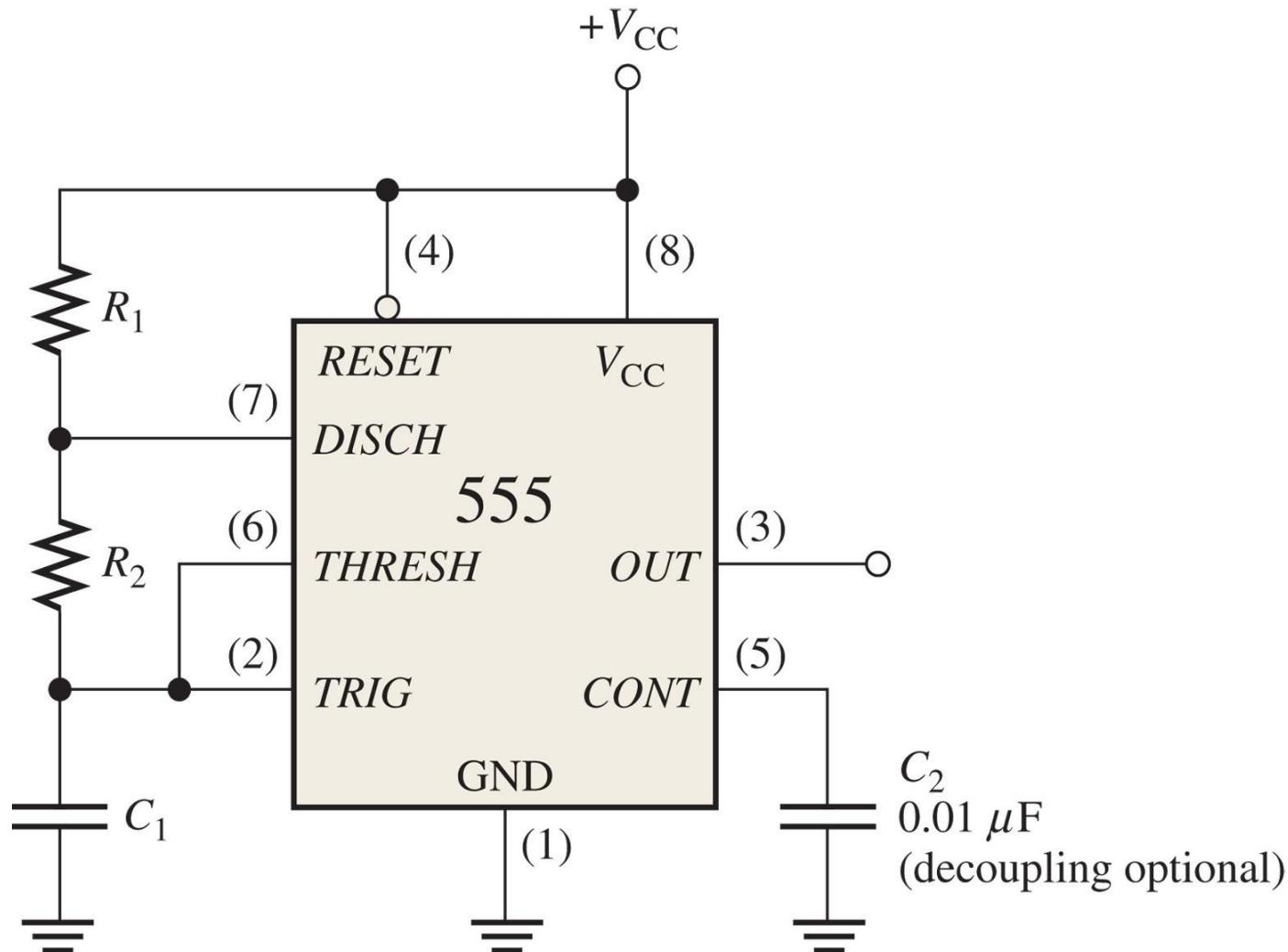


FIGURE 7-57 Operation of the 555 timer in the astable mode.

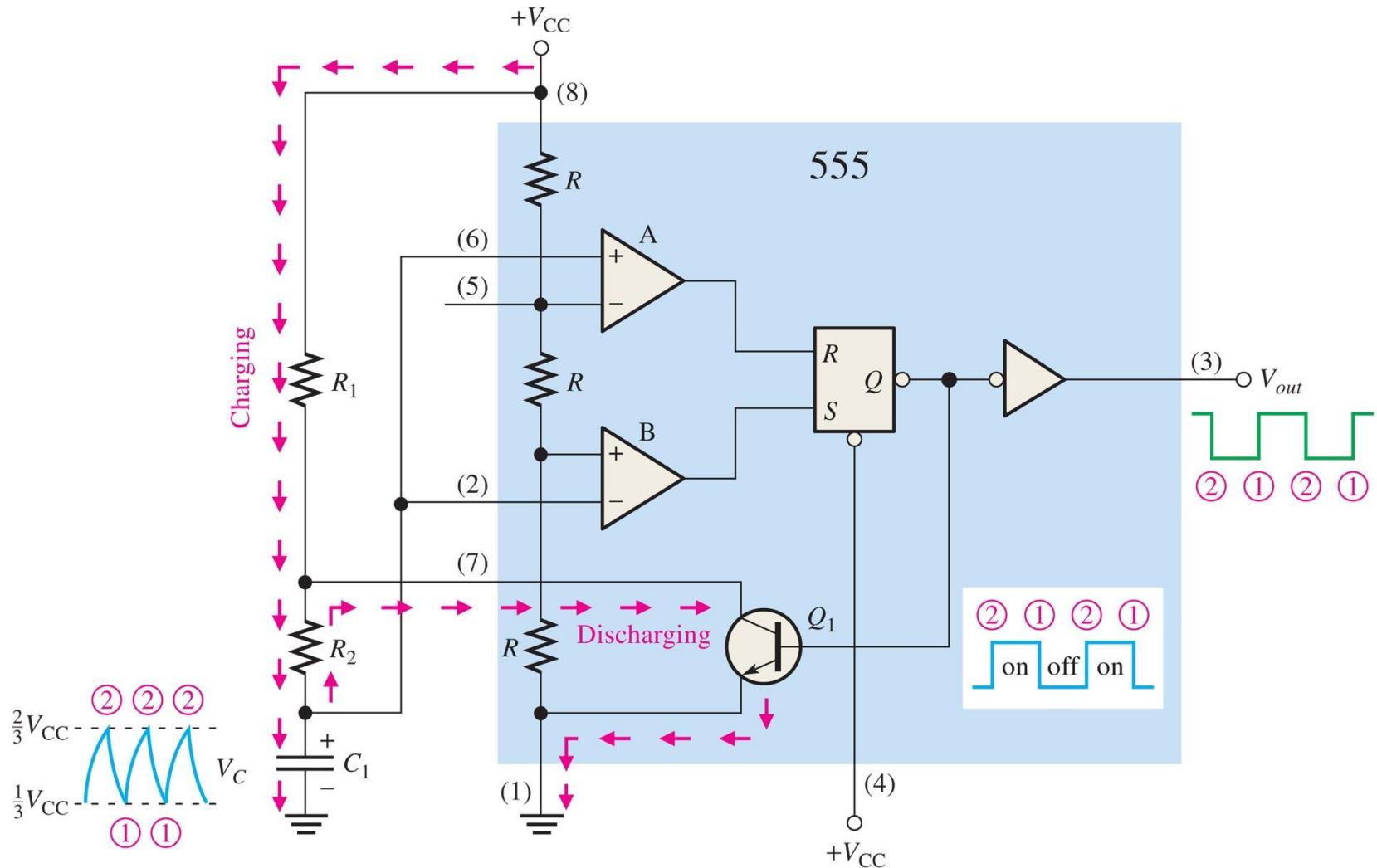
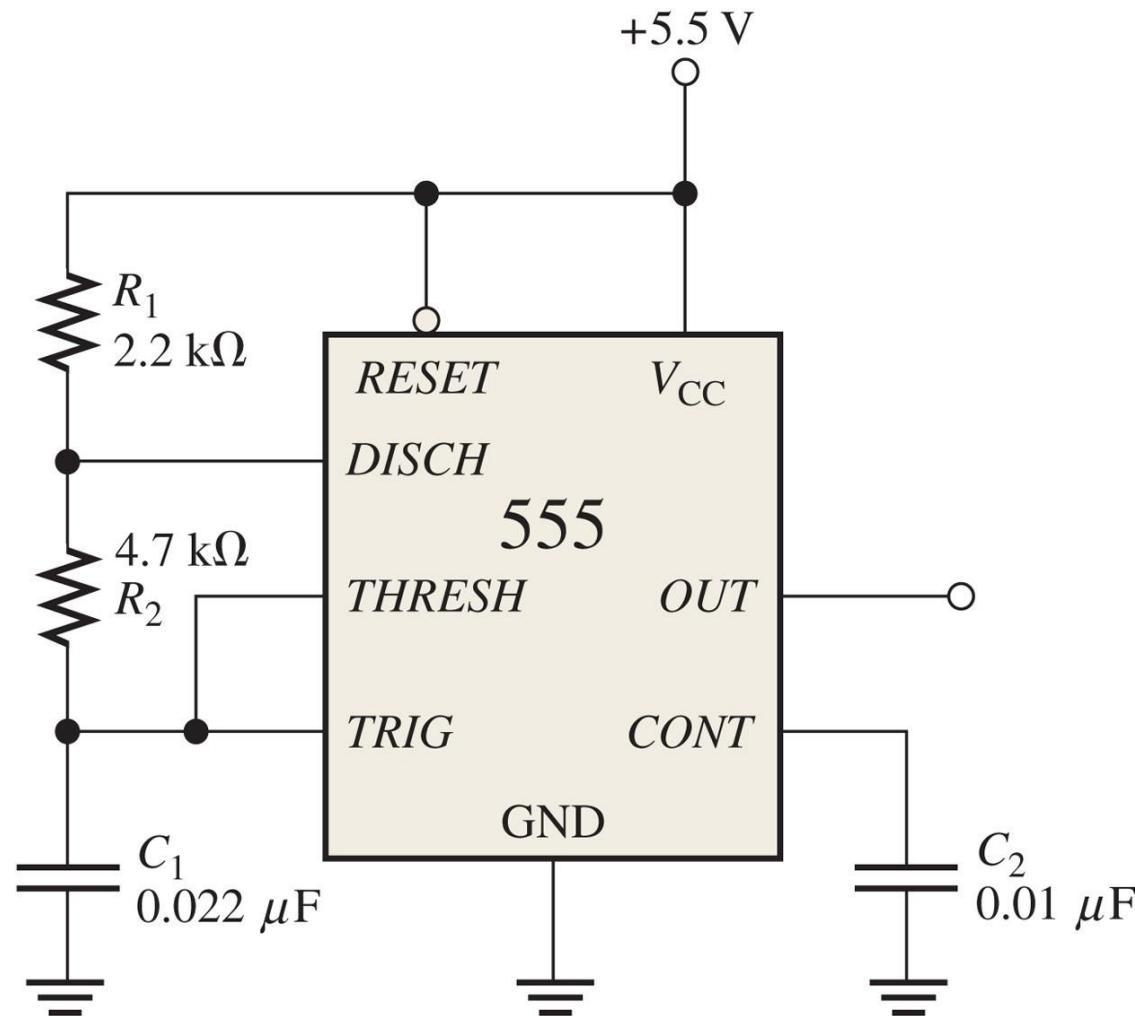


FIGURE 7-60



A 555 timer configured to run in the astable mode (pulse oscillator) is shown in Figure 7–60. Determine the frequency of the output and the duty cycle.

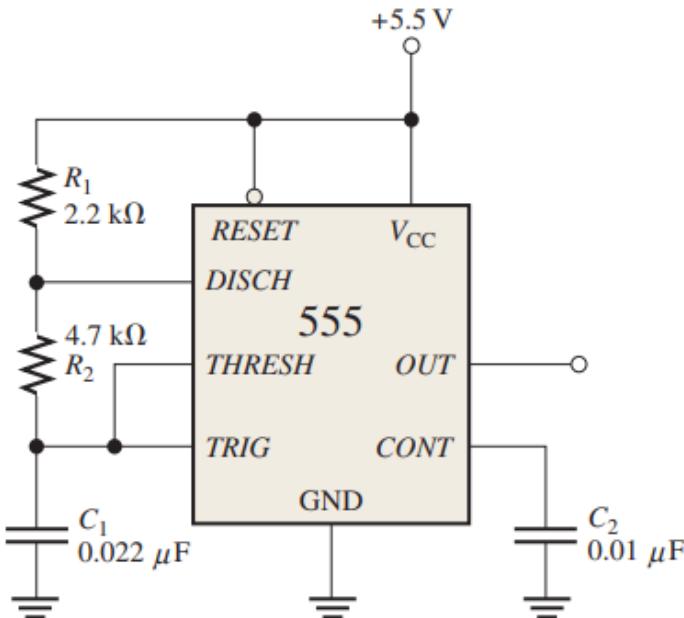


FIGURE 7–60 Open file F07-60 to verify operation.

Solution

Use Equations 7–4 and 7–7.

$$f = \frac{1.44}{(R_1 + 2R_2)C_1} = \frac{1.44}{(2.2 \text{ k}\Omega + 9.4 \text{ k}\Omega)0.022 \mu\text{F}} = 5.64 \text{ kHz}$$

$$\text{Duty cycle} = \left(\frac{R_1 + R_2}{R_1 + 2R_2} \right) 100\% = \left(\frac{2.2 \text{ k}\Omega + 4.7 \text{ k}\Omega}{2.2 \text{ k}\Omega + 9.4 \text{ k}\Omega} \right) 100\% = 59.5\%$$

FIGURE 7-64 Block diagram of the traffic signal controller.

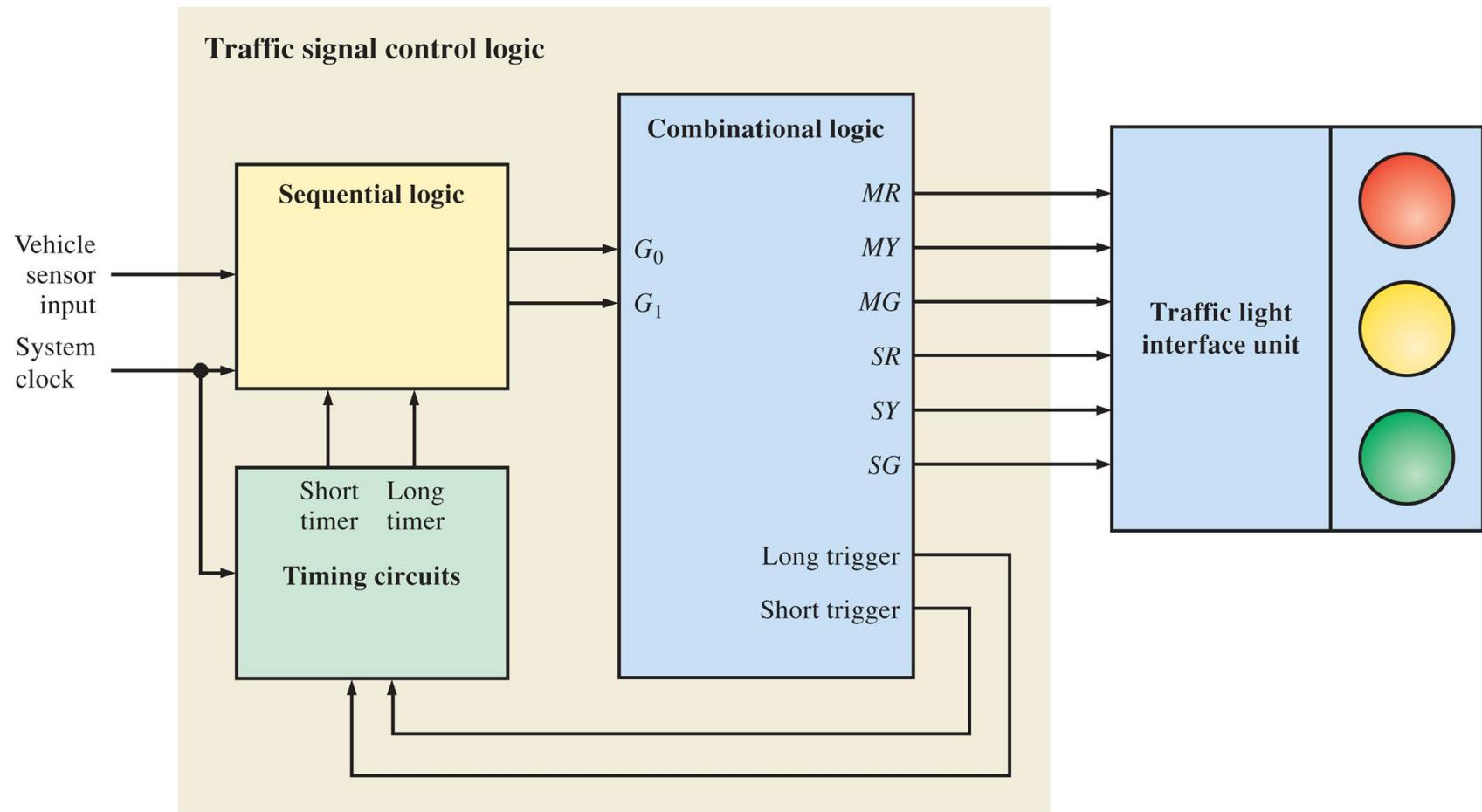


FIGURE 7-65 Block diagram of the timing circuits unit.

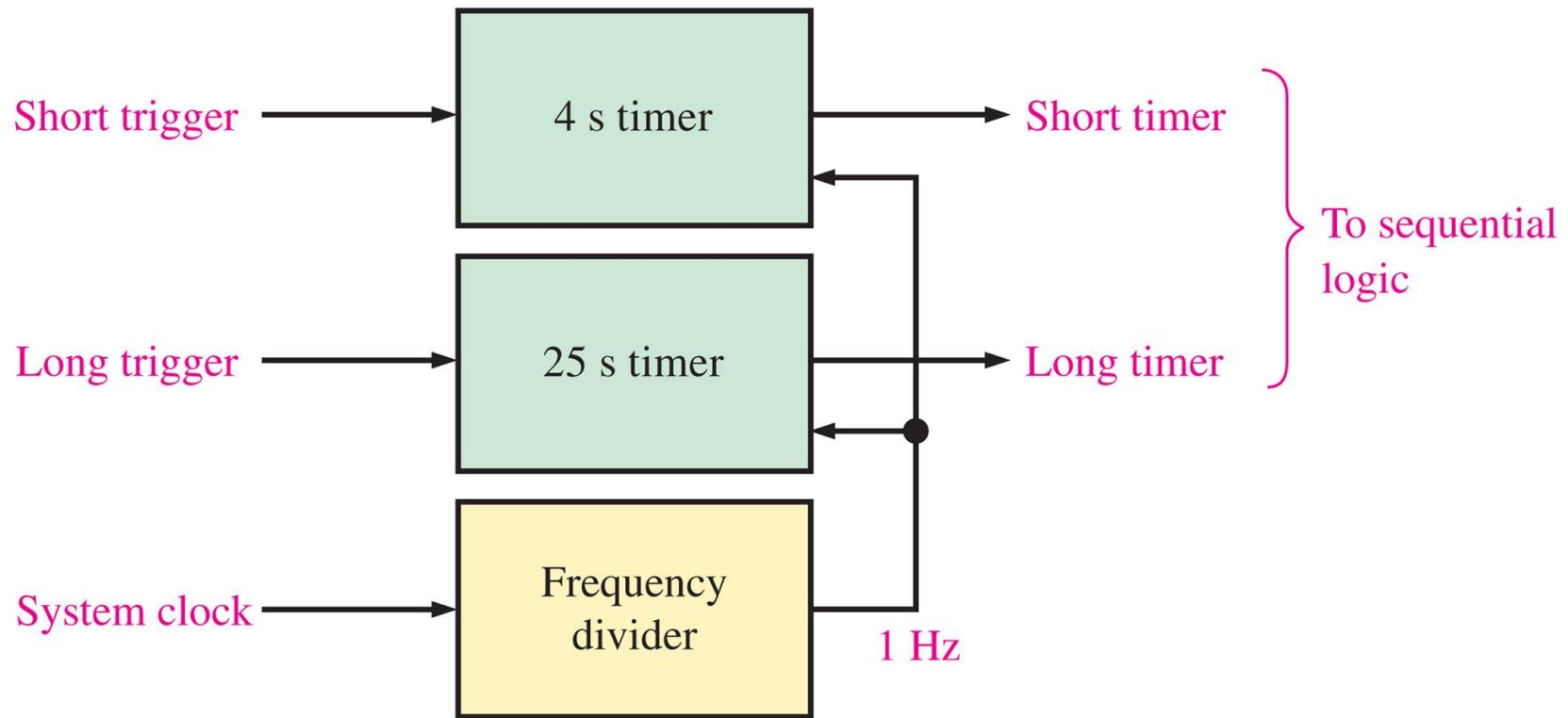


FIGURE 7-66 Programming model for the traffic signal controller.

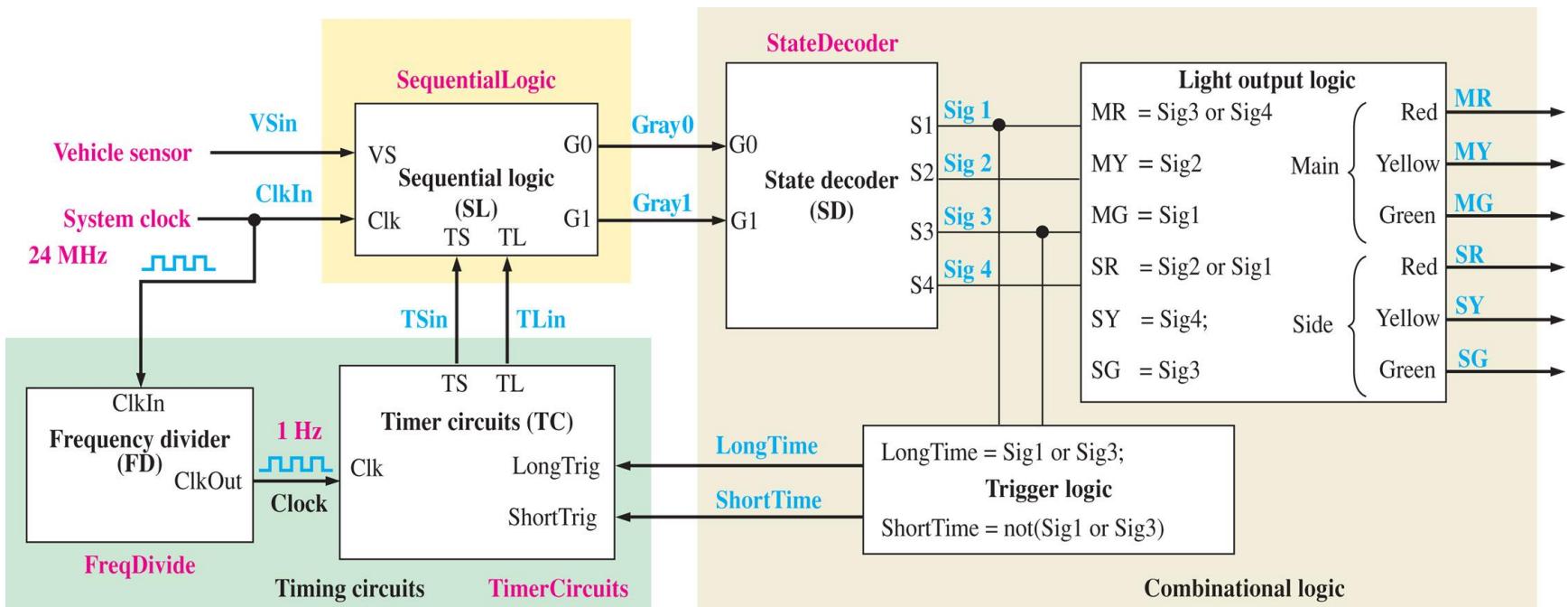
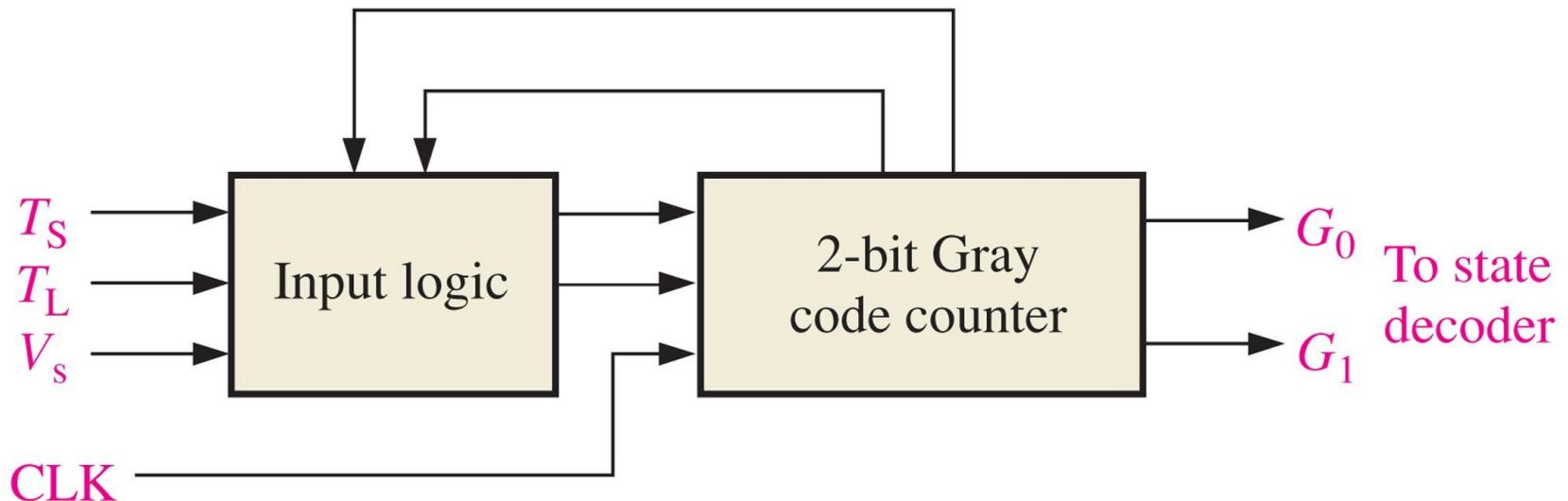


FIGURE 7-67 Block diagram of the sequential logic.



T_S : Short timer (4 s)

T_L : Long timer (25 s)

V_s : Vehicle sensor for the side street

FIGURE 7-68 Sequential logic diagram with two D flip-flops used to implement the 2-bit Gray code counter.

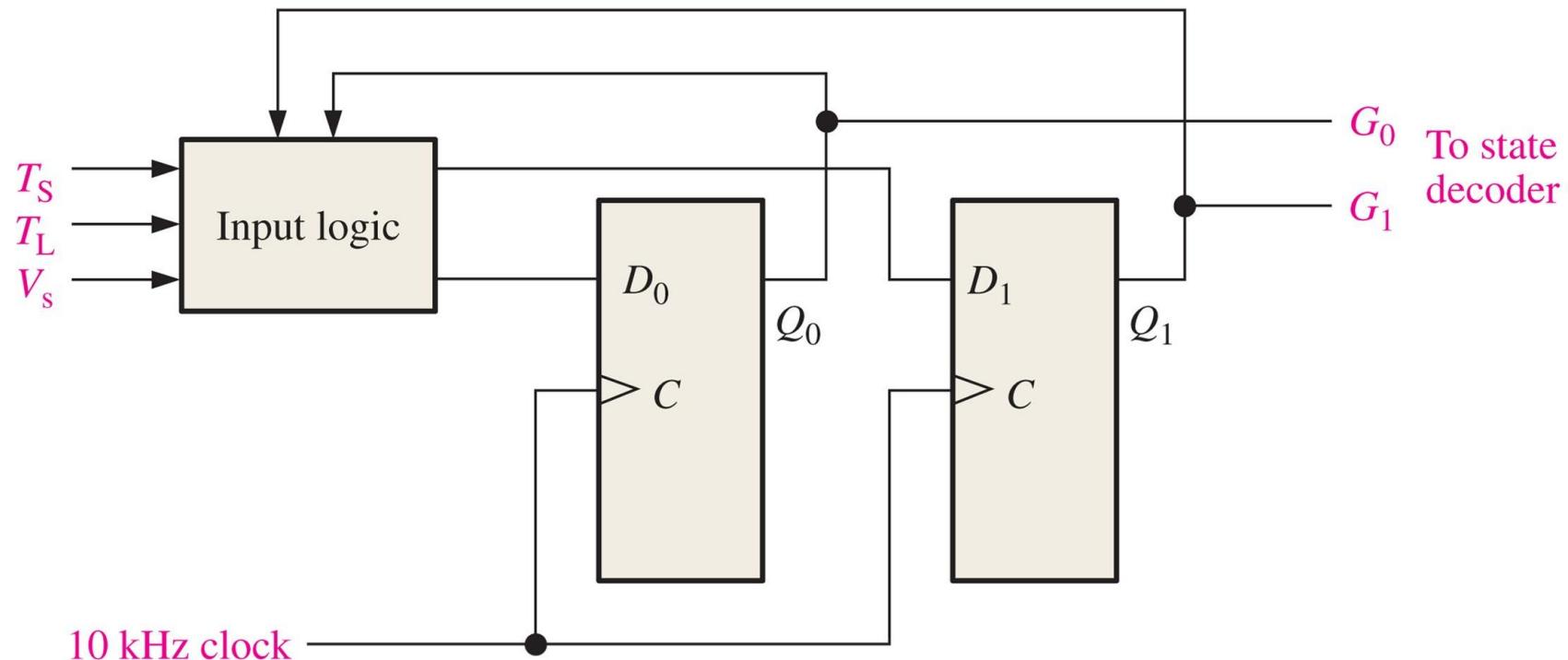


TABLE 7–5

D flip-flop transition table. Q_N is the output before clock pulse. Q_{N+1} is output after clock pulse.

Output Transitions		Flip-Flop Input
Q_N	Q_{N+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

TABLE 7–6

Next-state table for the counter.

Present State		Next State		Input Conditions	FF Inputs	
Q_1	Q_0	Q_1	Q_0		D_1	D_0
0	0	0	0	$T_L + \bar{V}_s$	0	0
0	0	0	1	$\bar{T}_L V_s$	0	1
0	1	0	1	T_S	0	1
0	1	1	1	\bar{T}_S	1	1
1	1	1	1	$T_L V_s$	1	1
1	1	1	0	$\bar{T}_L + \bar{V}_s$	1	0
1	0	1	0	T_S	1	0
1	0	0	0	\bar{T}_S	0	0

FIGURE 7-69 Complete diagram for the sequential logic.

