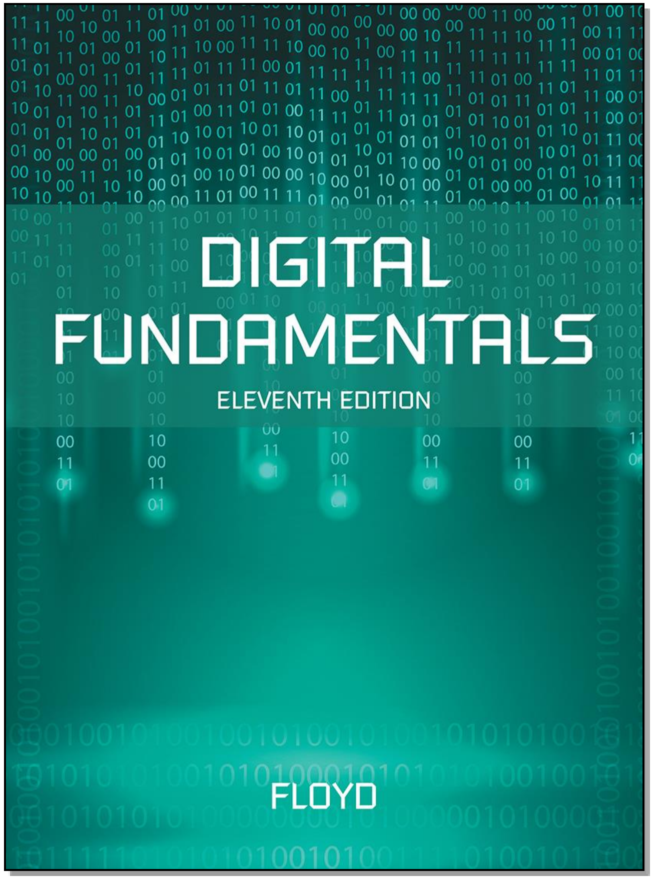
Digital Fundamentals

ELEVENTH EDITION



CHAPTER 1

Introductory Concepts

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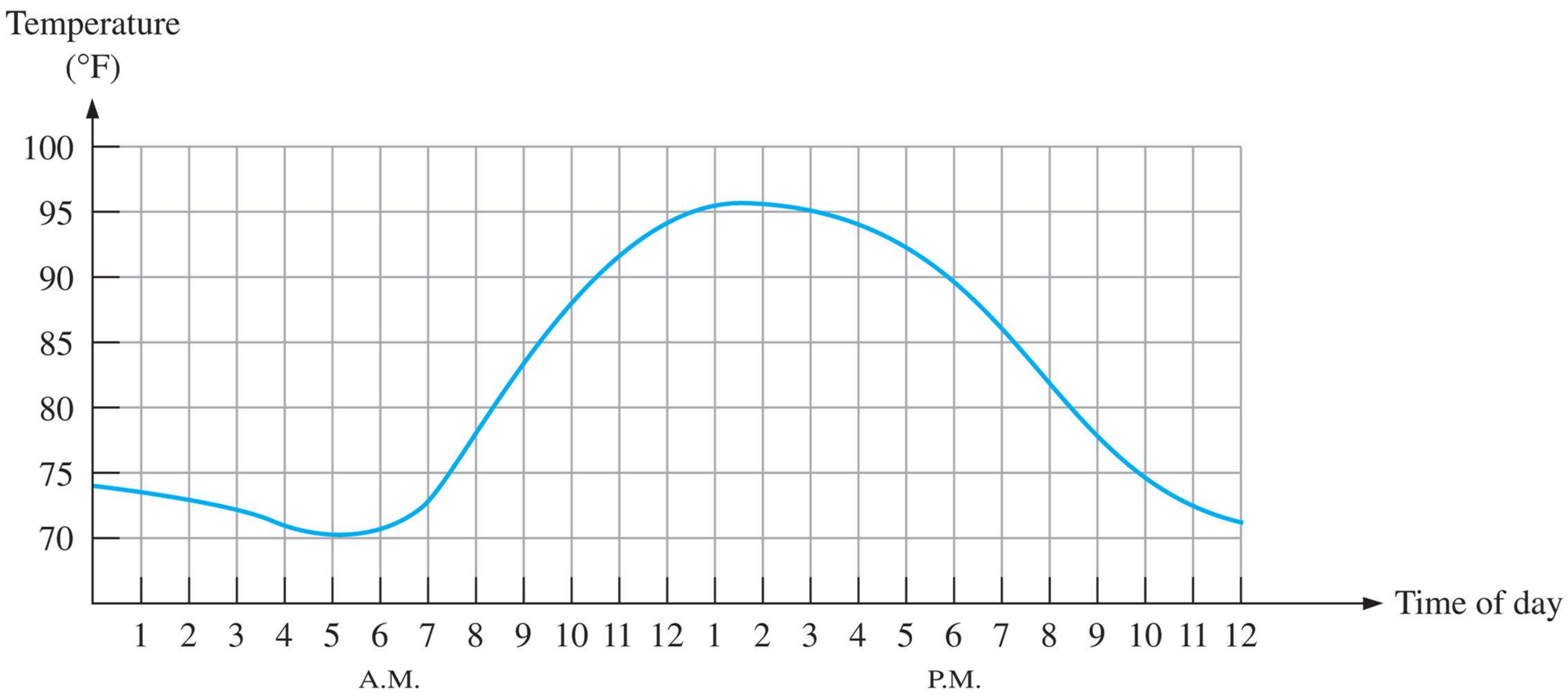
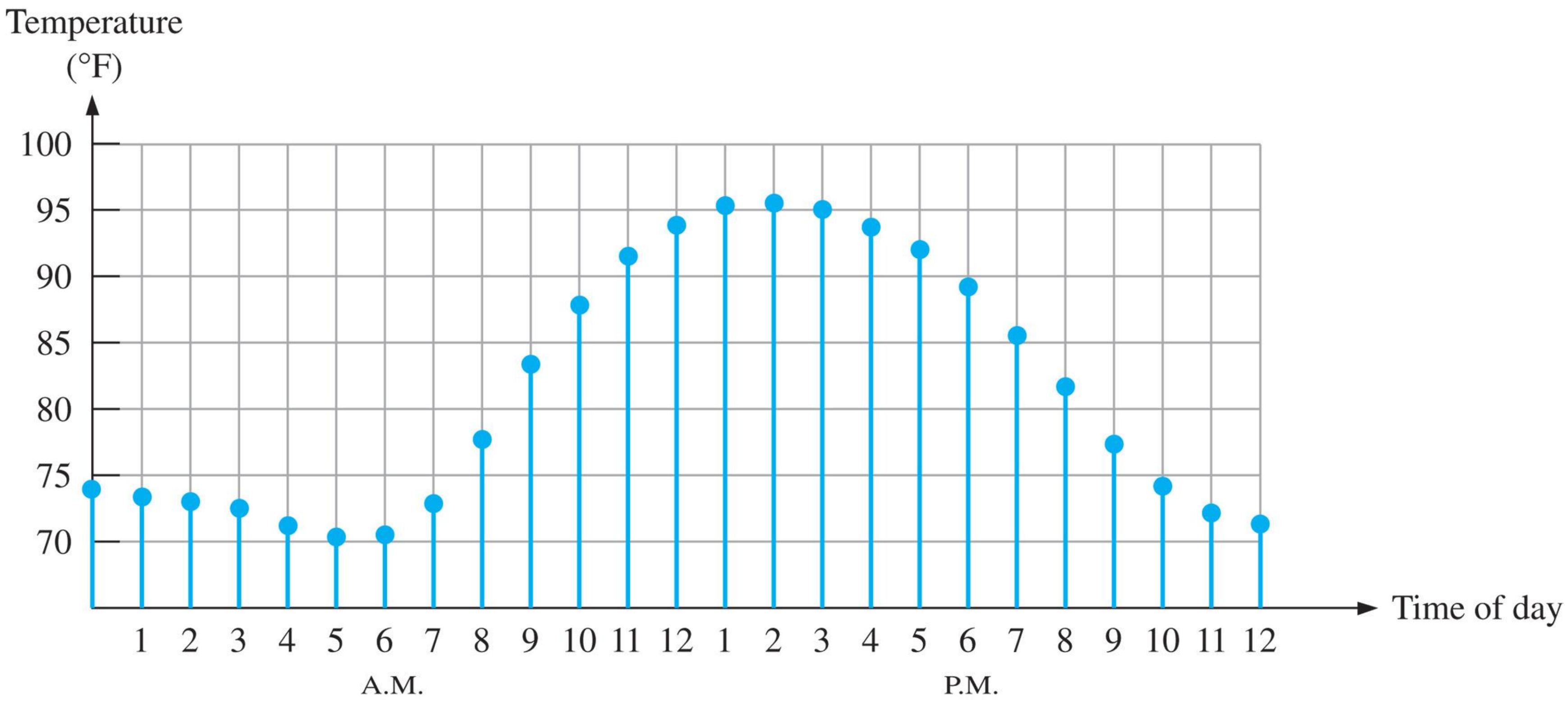
Graph of an analog quantity

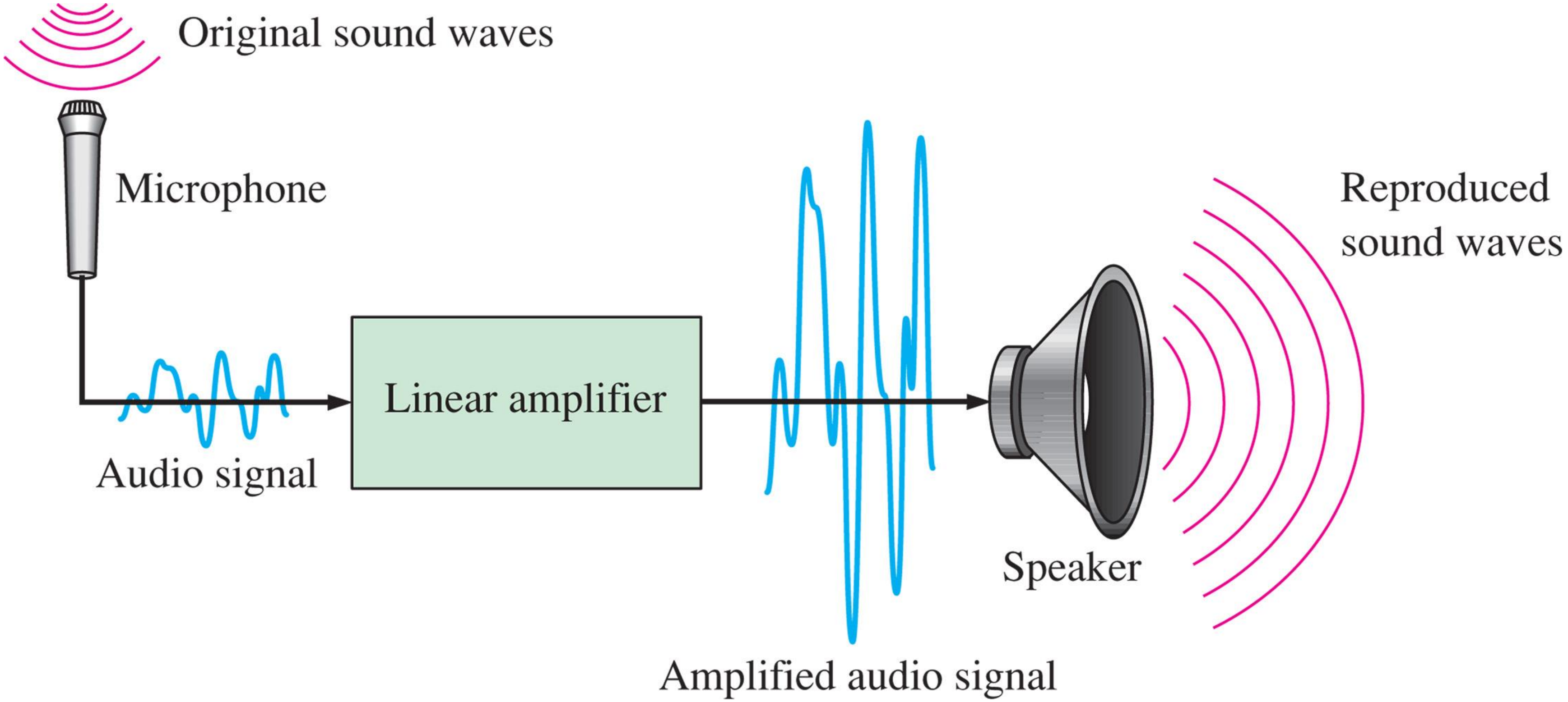


Sampled-value representation (quantization) of analog quantity.

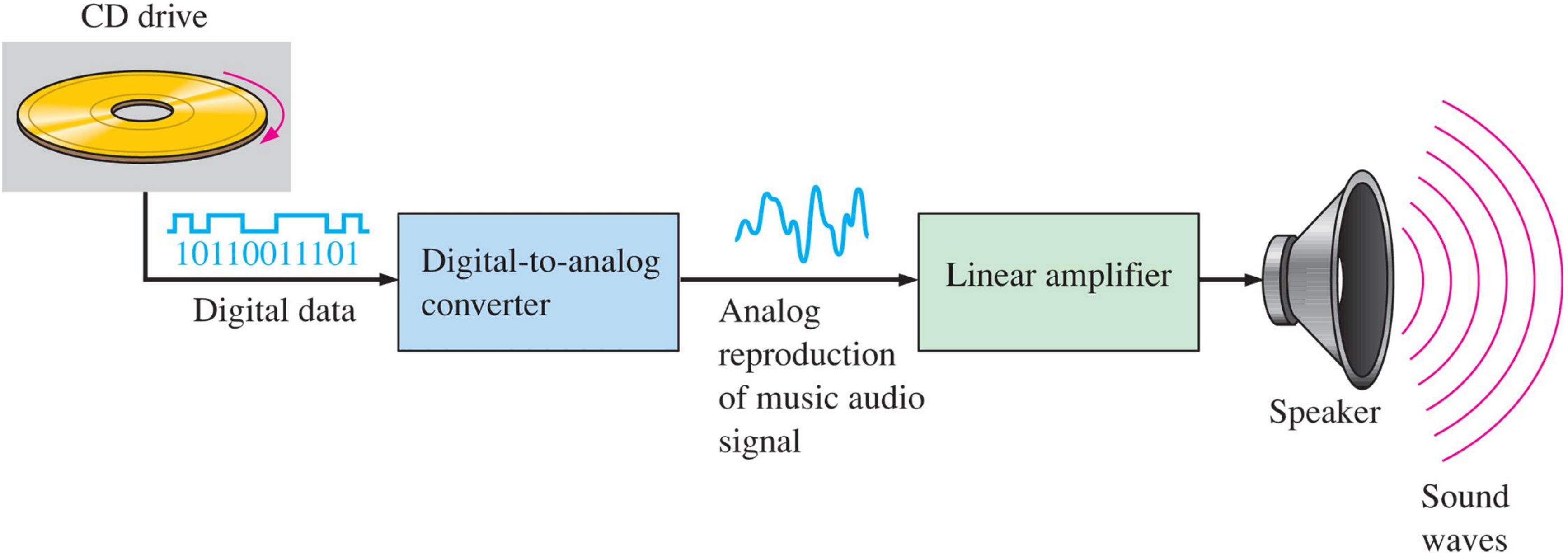
Each dot can be digitized by representing by series of 1s and 0s.



A basic audio public address system



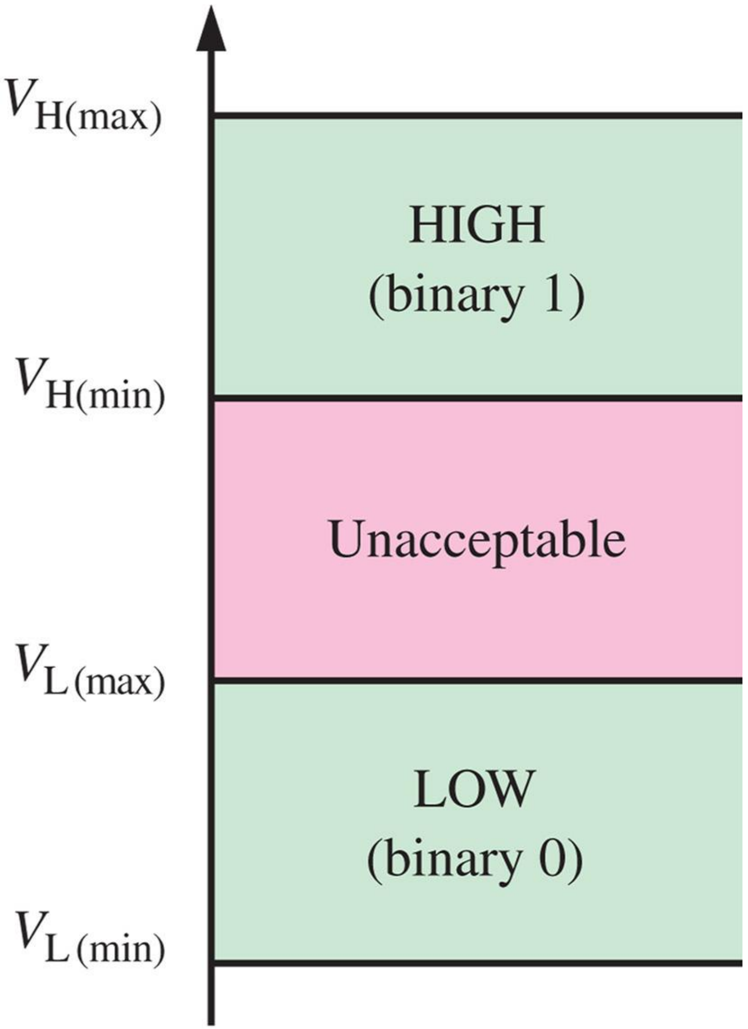
Basic block diagram of a CD player



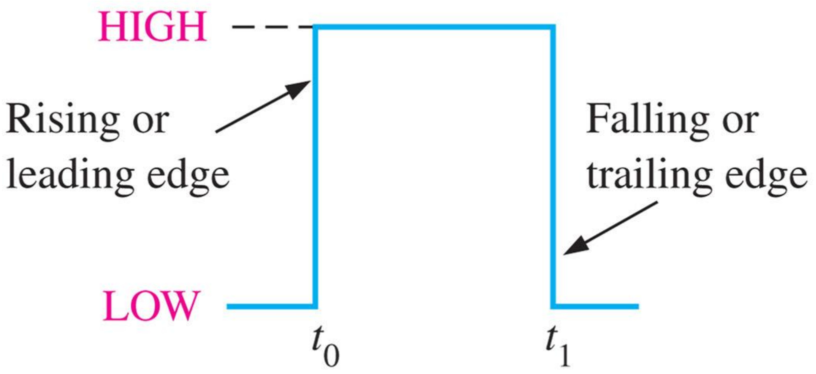
Binary Digits

HIGH = 1 and LOW = 0

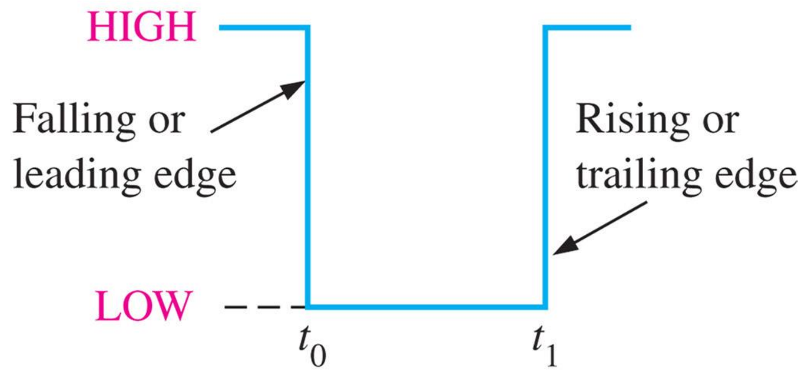
Logic level ranges of voltage for a digital circuit



Ideal pulses



(a) Positive–going pulse



(b) Negative–going pulse

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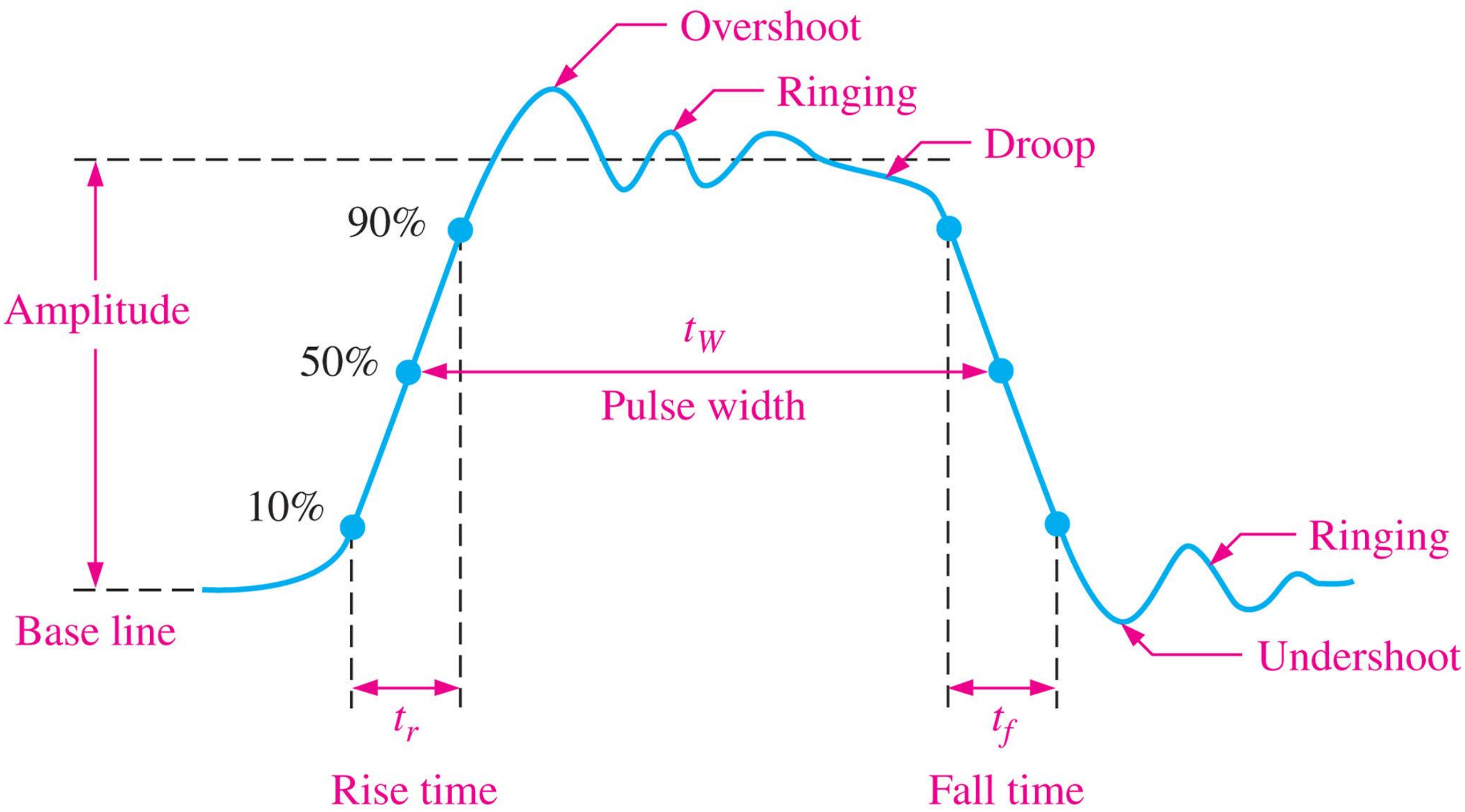
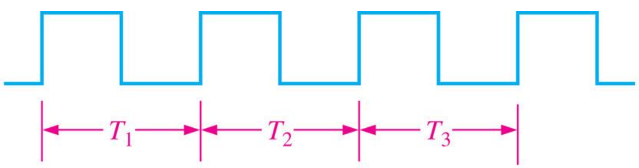
Nonideal pulse characteristics



Examples of digital waveforms



Period $= T_1 = T_2 = T_3 = \ldots = T_n$

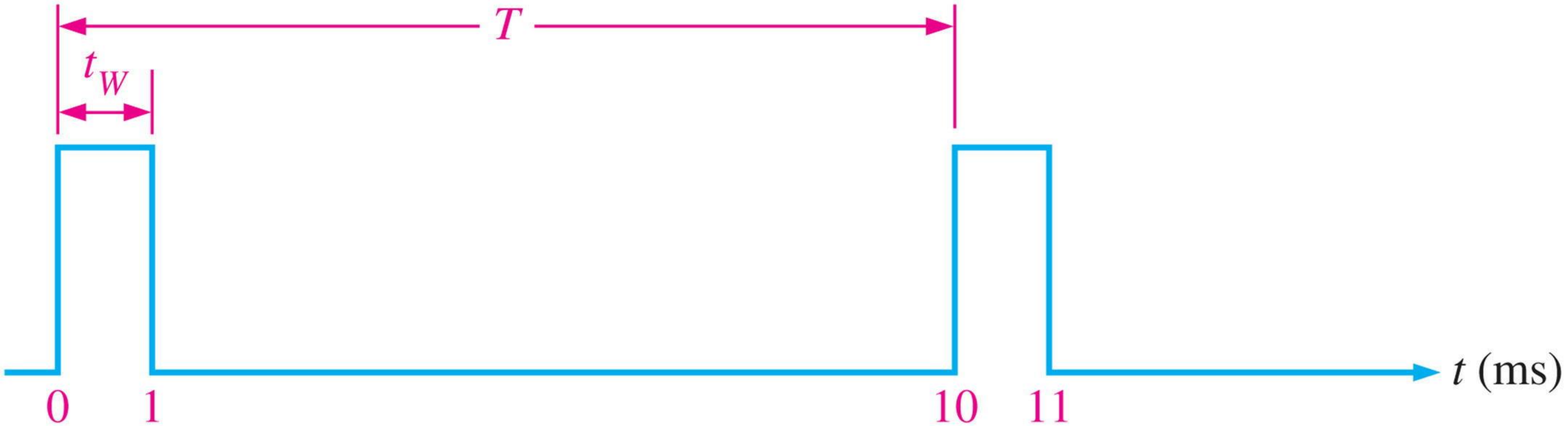
Frequency $= \frac{1}{T}$

(a) Periodic (square wave)

(b) Nonperiodic

$$f = \frac{1}{T}$$

$$T = \frac{1}{f}$$



$$\text{Duty cycle} = \left(\frac{t_W}{T}\right)100\%$$

Example

A portion of a periodic digital waveform is shown in Figure 1–10. The measurements are in milliseconds. Determine the following:

(a) period **(b)** frequency **(c)** duty cycle

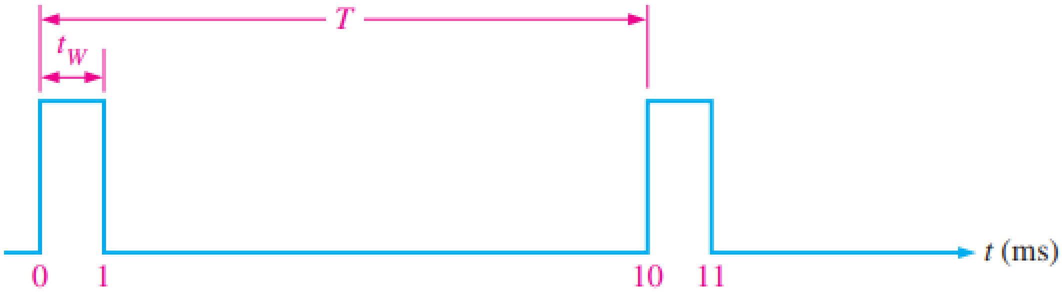


FIGURE 1–10

Solution

(a) The period (T) is measured from the edge of one pulse to the corresponding edge of the next pulse. In this case T is measured from leading edge to leading edge, as indicated. T equals **10 ms**.

(b) $f = \frac{1}{T} = \frac{1}{10\text{ ms}} = \mathbf{100\ Hz}$

(c) $\text{Duty cycle} = \left(\frac{t_W}{T}\right)100\% = \left(\frac{1\text{ ms}}{10\text{ ms}}\right)100\% = \mathbf{10\%}$

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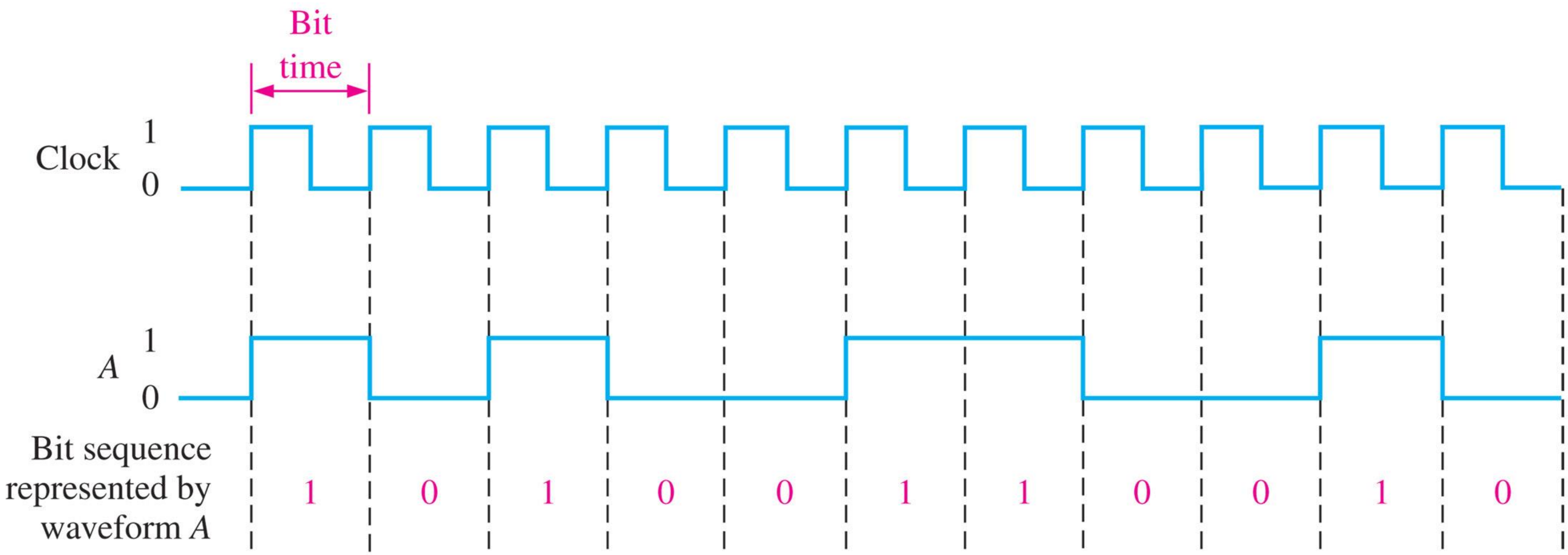
Example of a clock waveform synchronized with a waveform representation of a sequence of bits



Example of a timing diagram

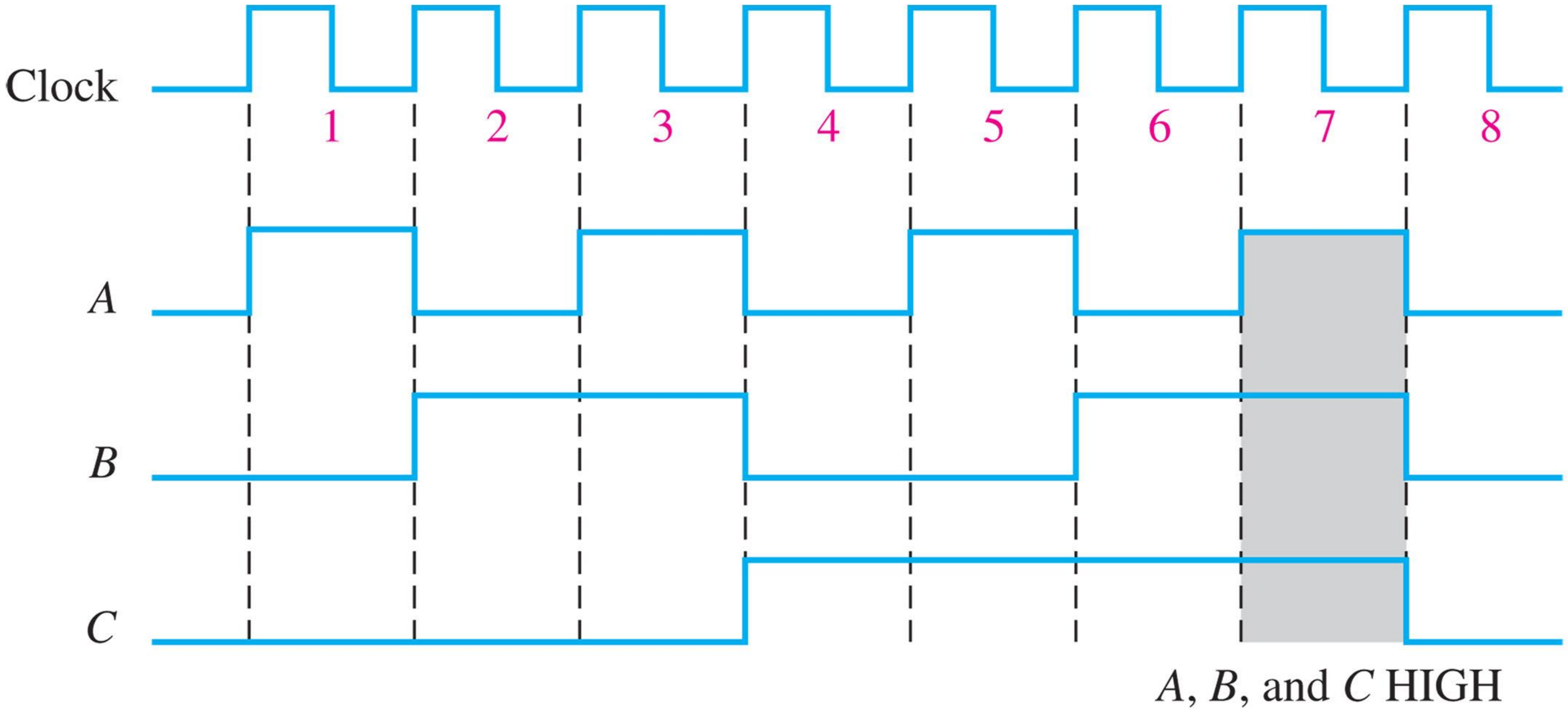
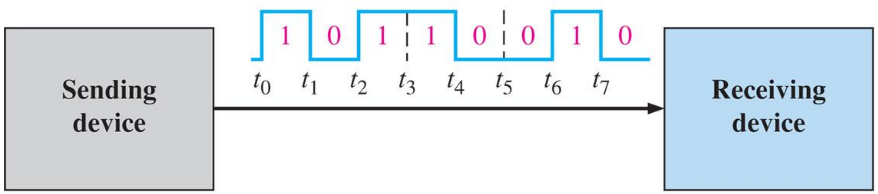
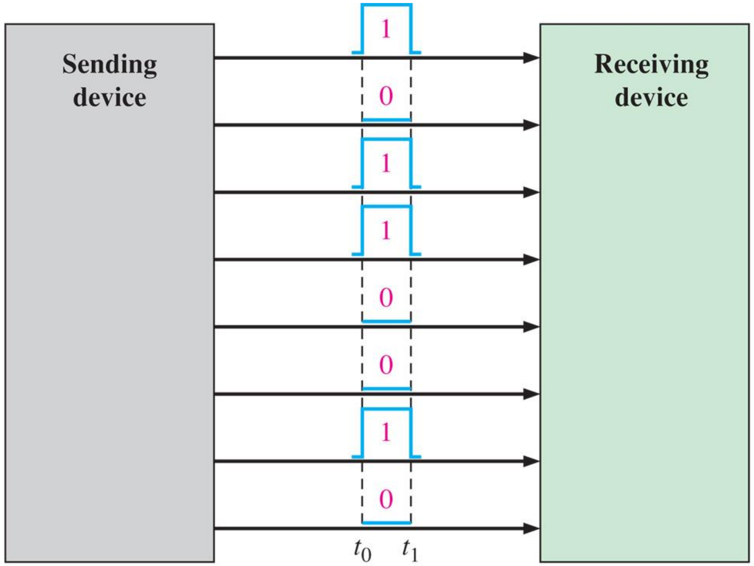


Illustration of serial and parallel transfer of binary data



(a) Serial transfer of 8 bits of binary data. Interval t_0 to t_1 is first.

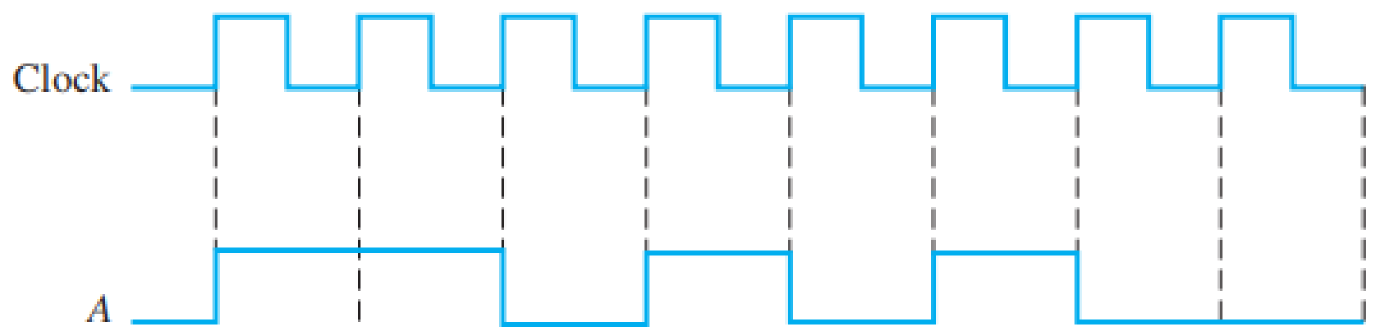


(b) Parallel transfer of 8 bits of binary data. The beginning time is t_0.

Example

(a) Determine the total time required to serially transfer the eight bits contained in waveform *A* of Figure 1–14, and indicate the sequence of bits. The left-most bit is the first to be transferred. The 1 MHz clock is used as reference.

(b) What is the total time to transfer the same eight bits in parallel?



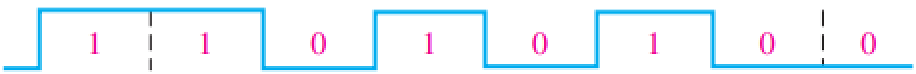
Solution

(a) Since the frequency of the clock is 1 MHz, the period is

$$T = \frac{1}{f} = \frac{1}{1\text{ MHz}} = 1\ \mu\text{s}$$

It takes 1 μs to transfer each bit in the waveform. The total transfer time for 8 bits is

$$8 \times 1\ \mu\text{s} = \mathbf{8\ \mu s}$$



The left-most bit is the first to be transferred.

(b) A parallel transfer would take **1 μs** for all eight bits.

Basic Logic Functions

- Define the NOT function
- Define the AND function
- Define the OR function

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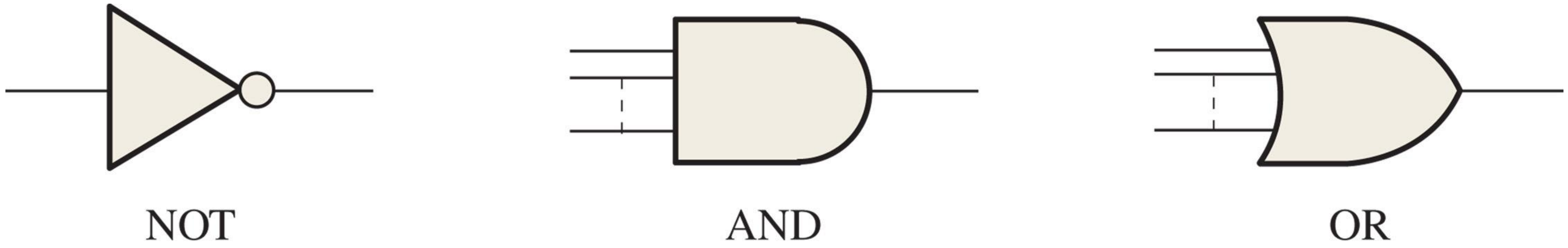
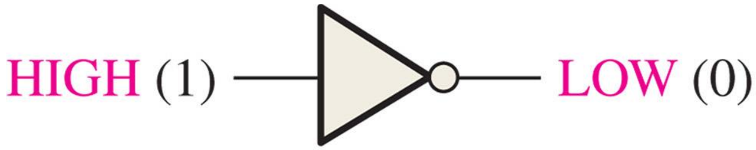
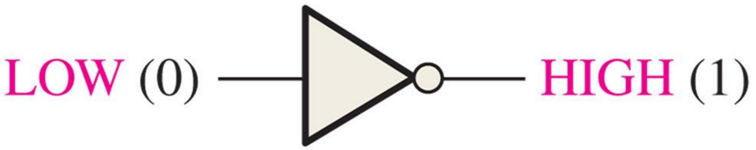
The basic logic functions and symbols

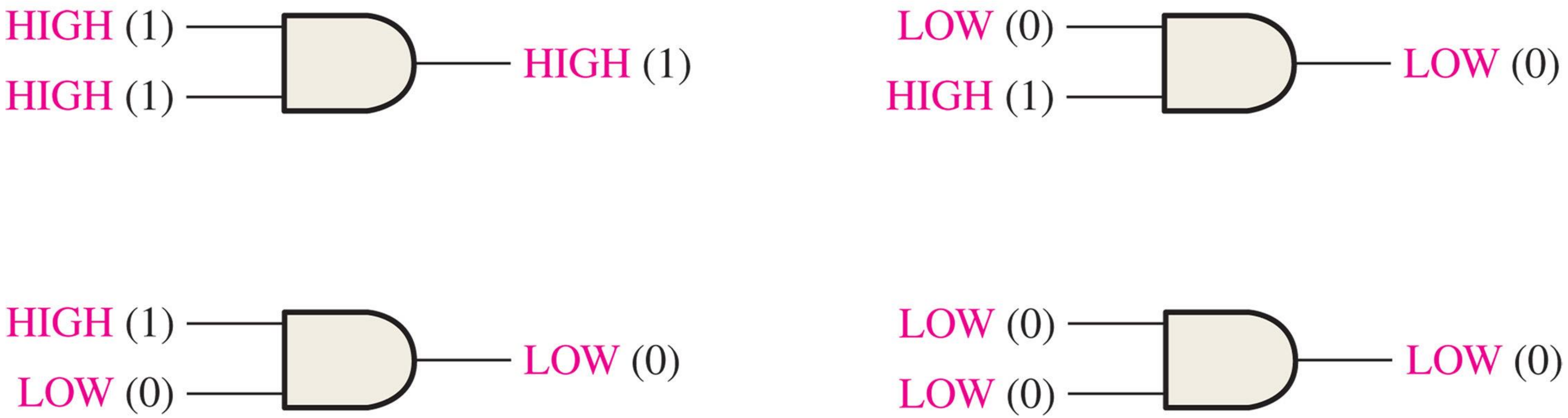


The NOT function

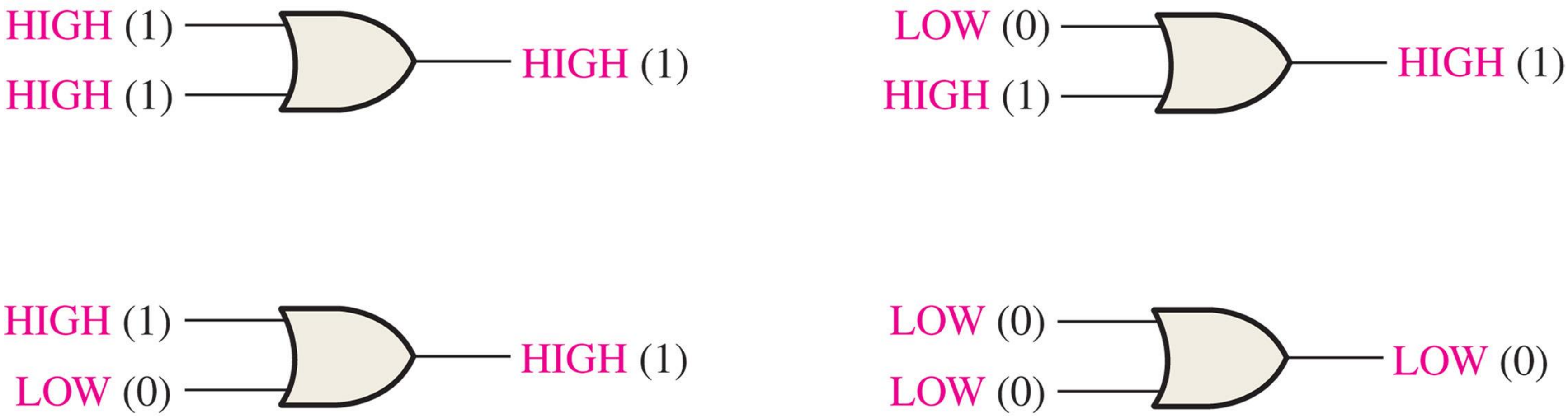




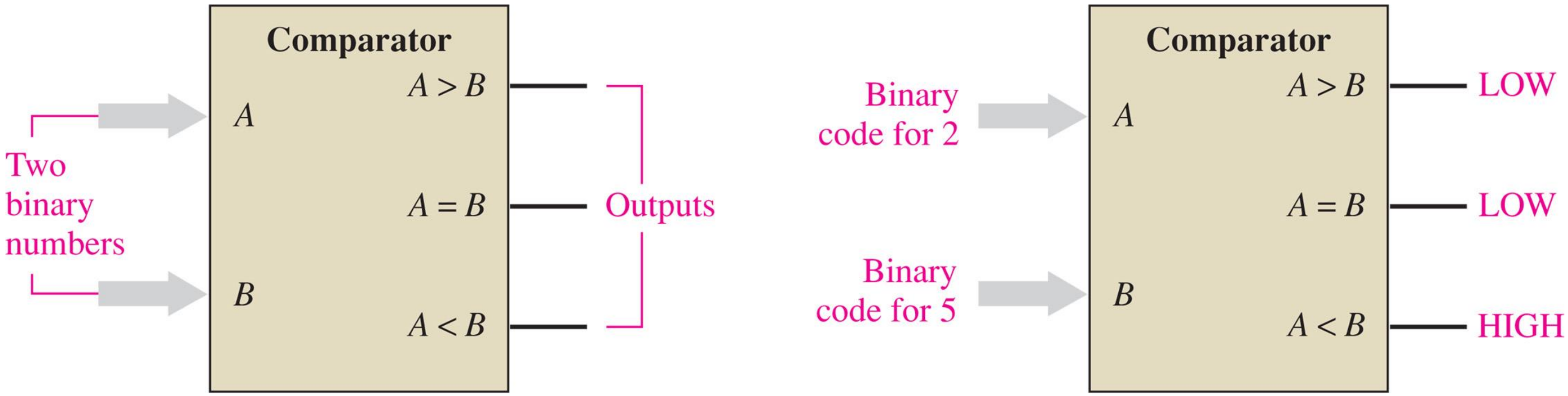
The AND function



The OR function



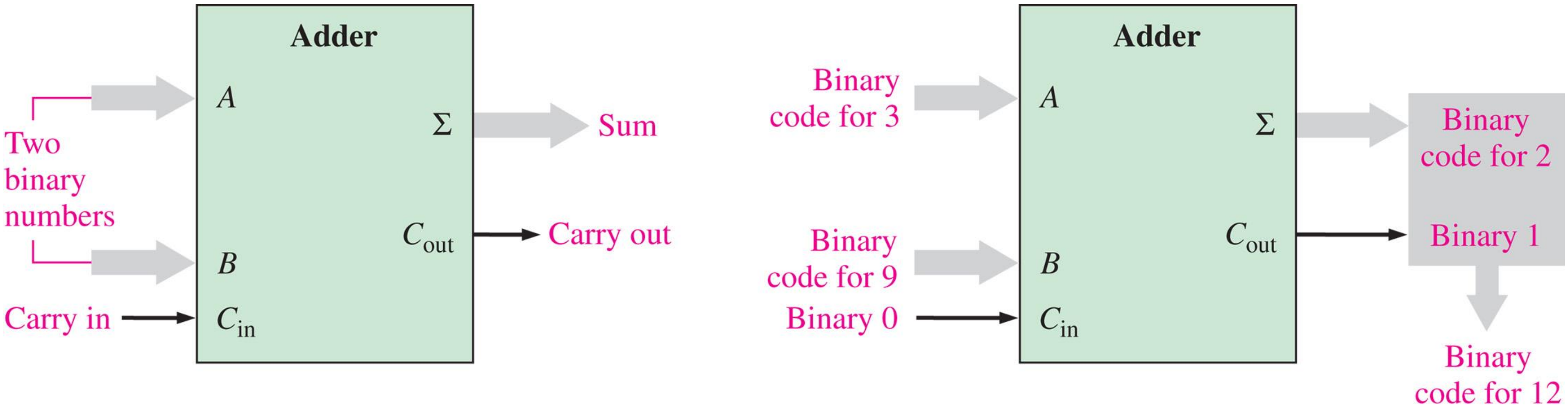
The comparison function



(a) Basic magnitude comparator

(b) Example: A is less than B ($2 < 5$) as indicated by the HIGH output ($A < B$)

The addition function



(a) Basic adder

(b) Example: A plus B ($3 + 9 = 12$)

The Arithmetic Functions

Addition,
Subtraction,
Multiplication,
Division

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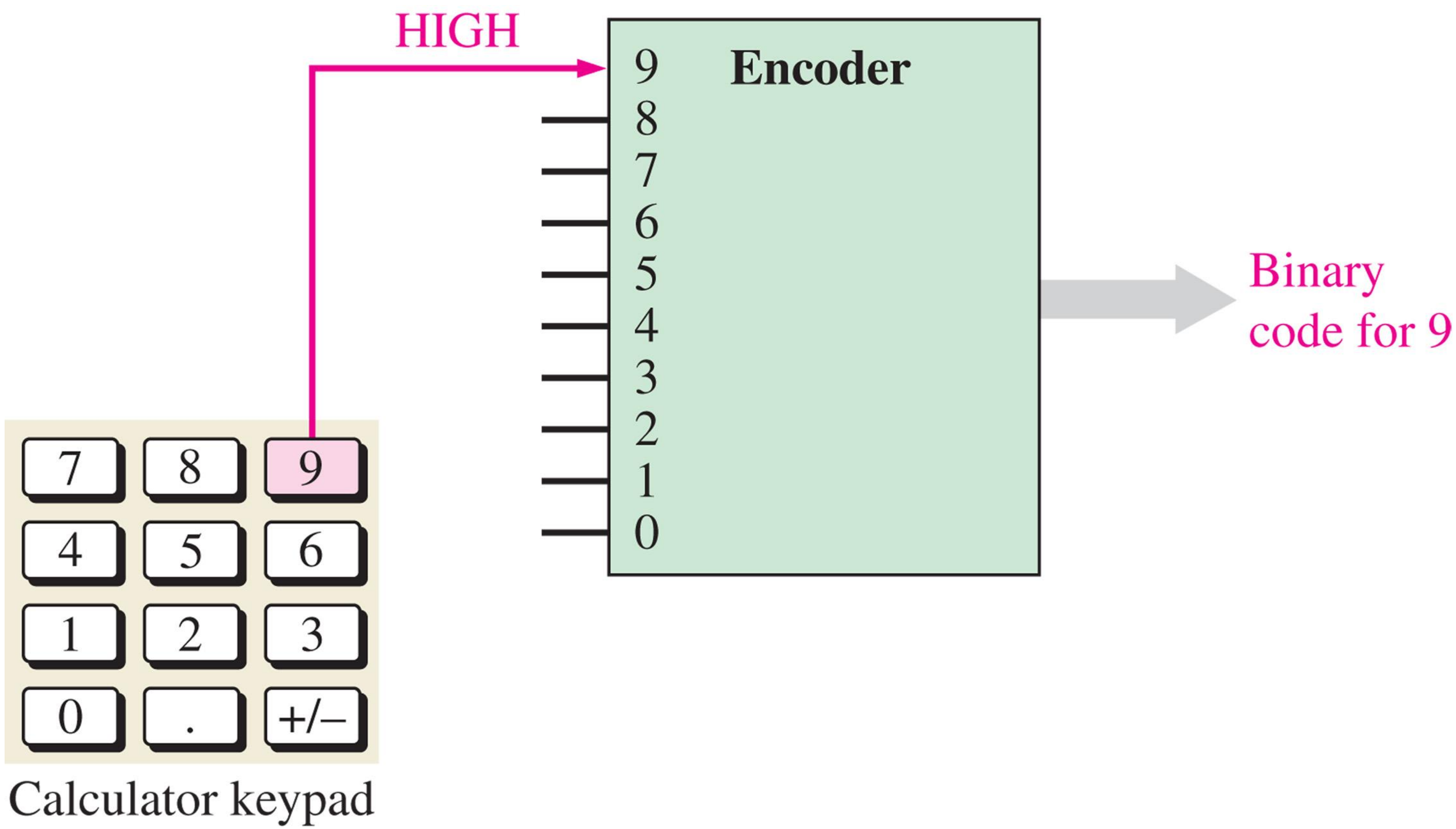
An encoder used to encode a calculator keystroke into a binary code



A decoder used to convert a special binary code into a 7-segment decimal readout

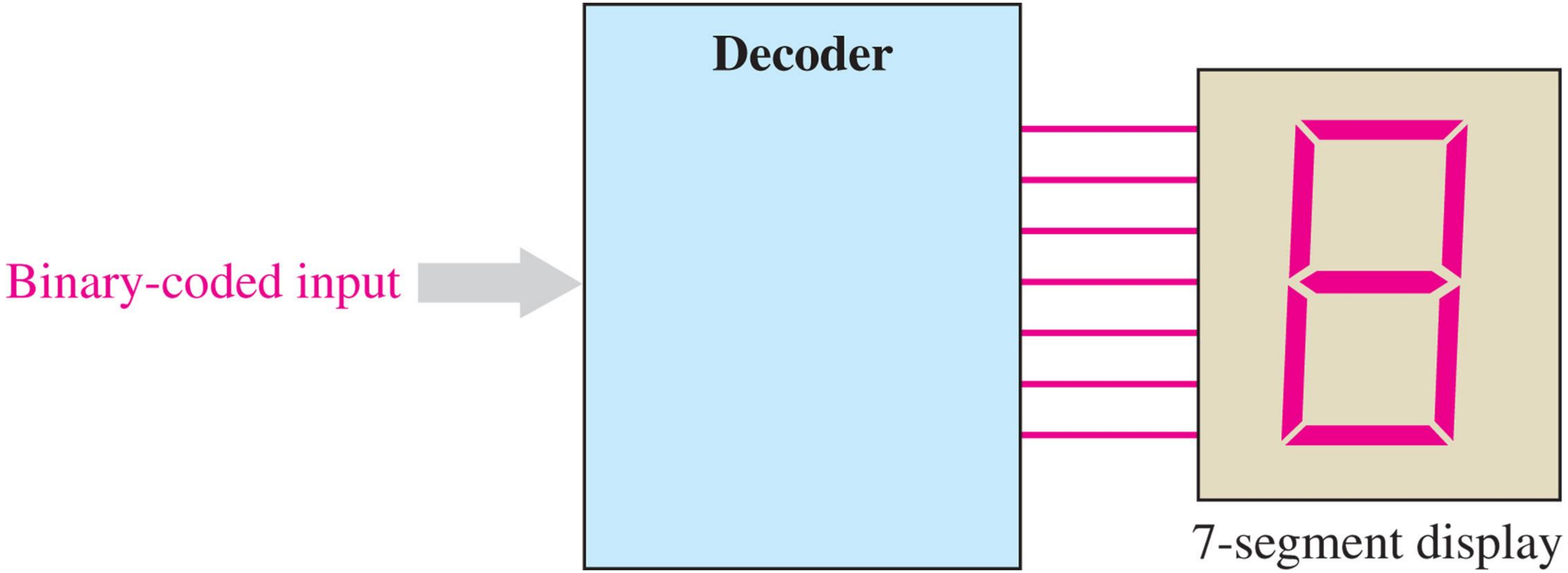
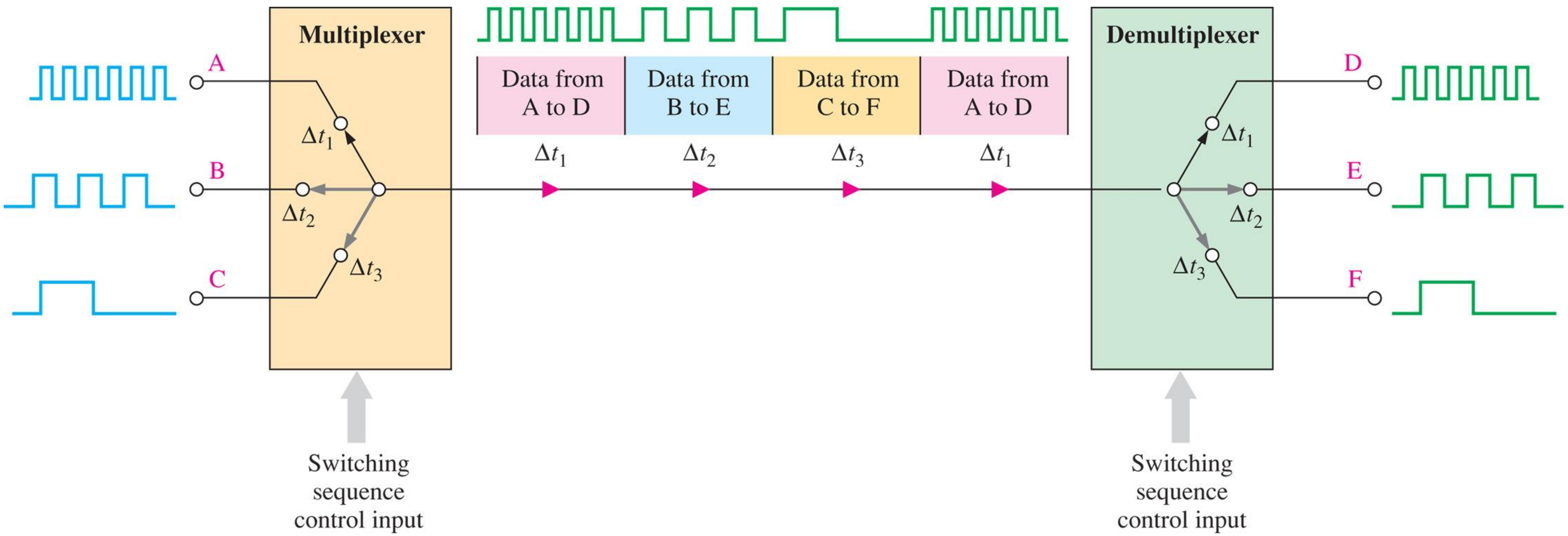
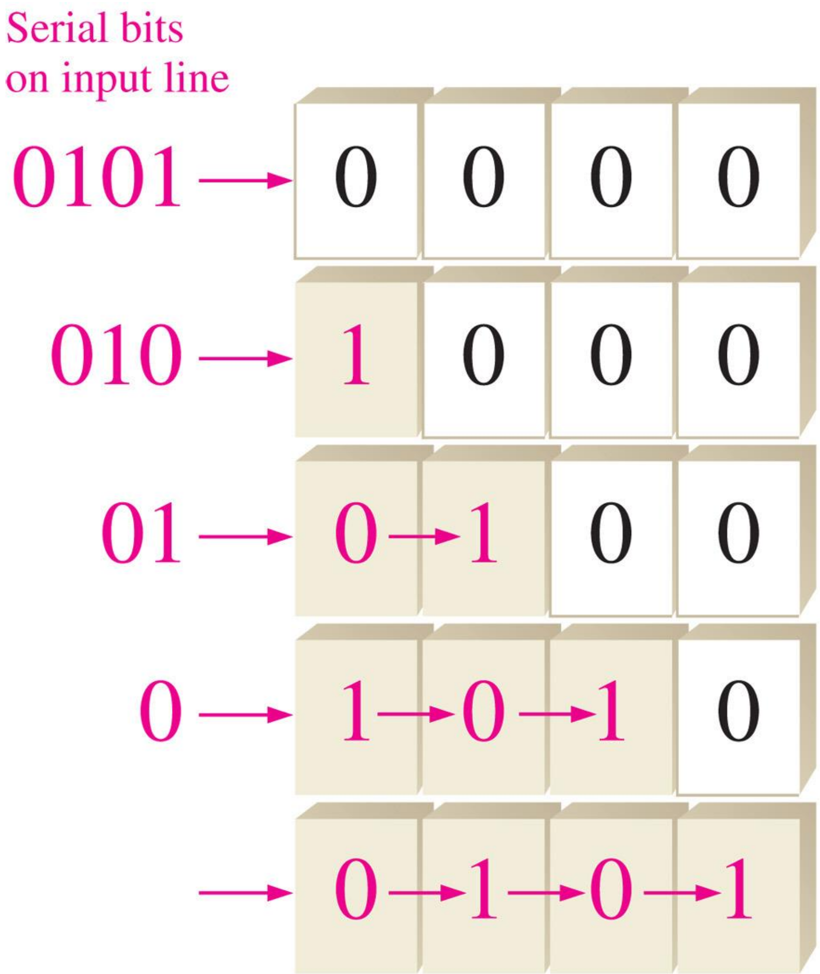


Illustration of a basic multiplexing/demultiplexing application



Example of the operation of a 4-bit serial shift register
Each block represents one storage "cell" or flip-flop



Initially, the register contains only *invalid* data or all zeros as shown here.

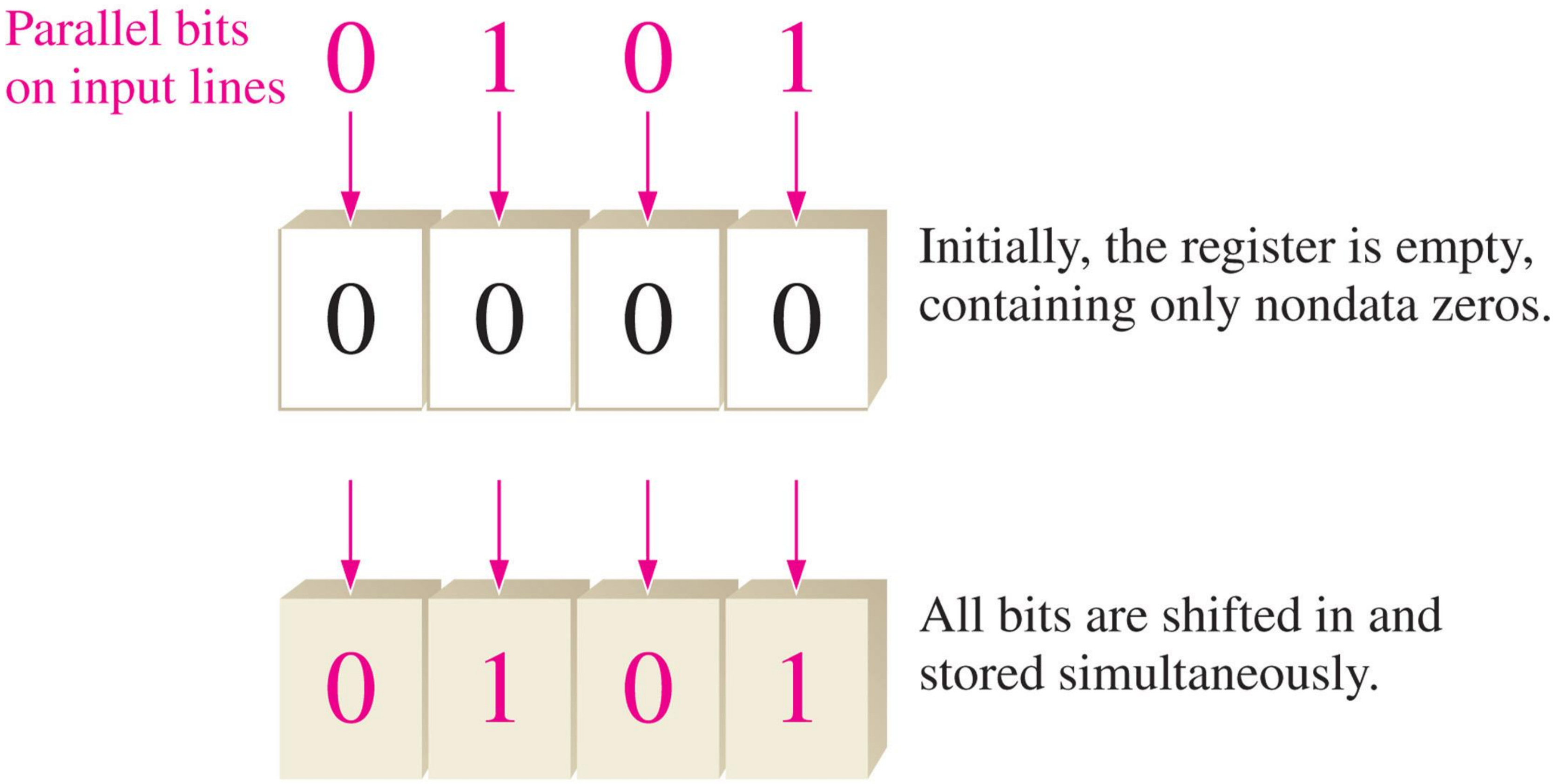
First bit (1) is shifted serially into the register.

Second bit (0) is shifted serially into register and first bit is shifted right.

Third bit (1) is shifted into register and the first and second bits are shifted right.

Fourth bit (0) is shifted into register and the first, second, and third bits are shifted right. The register now stores all four bits and is full.

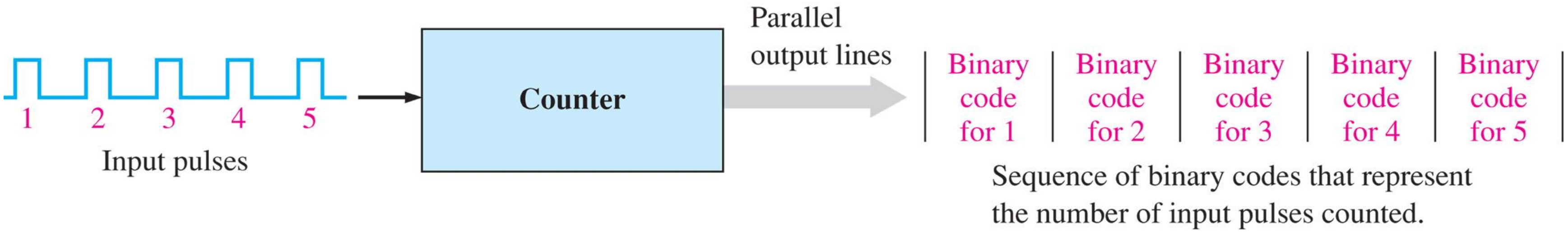
Example of the operation of a 4-bit parallel shift register



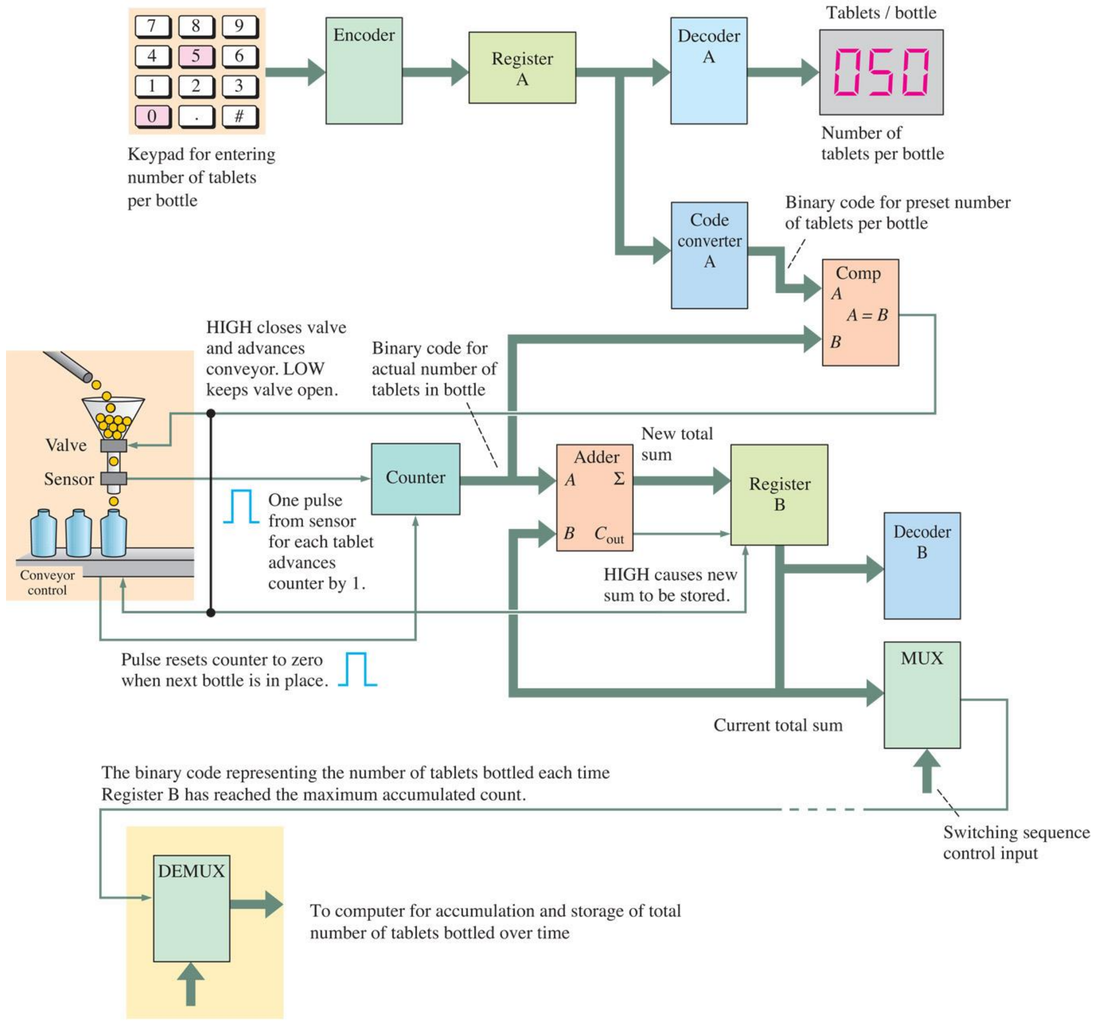
Memories

Semiconductor Memories,
Magnetic Memories,
Optical Memories

Illustration of basic counter operation



Block diagram of a tablet-bottling system



Programmable logic hierarchy