Transistor scaling with novel materials

Complementary metal-oxide-semiconductor (CMOS) transistor scaling will continue for at least another decade. However, innovation in transistor structures and integration of novel materials are needed to sustain this performance trend. Here we discuss the challenges and opportunities of transistor scaling for the next five to ten years.

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The MOSFET, or metal-oxide-semiconductor field-effect transistor, is the fundamental switching device in very large scale integrated (VLSI) circuits. A MOSFET (Fig. 1a) has at least three terminals – the gate, source, and drain. The gate electrode is separated electrically from the source and drain by a thin dielectric film. Shrinking transistors not only packs more devices into a given area, but also shortens the distance between the source and drain, or the gate length, which can improve the switching speed. However, the gate terminal can lose control of the channel electric carriers when the source and drain are brought into close proximity without scaling other device parameters. Eventually, the gate terminal cannot turn off the device and transistor action is no longer observed. This phenomenon is the so-called short channel effect (SCE). According to Dennard's constant-field scaling theory[1], the vertical dimensions (gate oxide thickness, junction depth, and depletion width) must be scaled down with the lateral dimension, such as the gate length.

This theory guarantees appropriate electrostatic characteristics when a larger device is scaled down to a smaller one. It also provides a design guideline for shrinking device dimensions to achieve higher density and performance. The industry has been following this concept, by and large, for shrinking MOSFETs. In practice, not all scaling elements have advanced at the same pace. Selective scaling is often used in technology. For example, gate oxides were aggressively scaled between the 250 nm and 90 nm node but then stalled after the 90 nm node. Moreover, gate lengths have been made smaller than the wiring half-pitch. Device scaling strategy is also application dependent. In system-on-chip applications, numerous device types (such as high-performance logic, input/output, analog, and static random access memory or SRAM) are integrated into the same chips. Compromises are frequently made to accommodate all device types.

There are many factors that affect the competitiveness of a scaled technology. Technology benchmarks often include performance, power, density, design compatibility, reliability, yield, cost, and time-to-market. Higher performance elements that are derived from design and process innovations can usually be engineered to achieve power and density benefits. The two major factors that contribute to the performance of MOSFETs are: (i) the channel length from the source to drain, and (ii) the speed at which channel charge carriers travel from the source to drain. The gate terminal must be made strong enough to control the channel carriers. High-*k* dielectrics and metal electrodes can increase the gate control capability and simultaneously reduce the tunneling gate leakage current. Innovation in device structure is also needed to continue channel length scaling. Strained-Si and orientation

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effects are two ways to increase the channel mobility. The total resistance and capacitance of a transistor can be divided into intrinsic and parasitic components. Transistor scaling and mobility enhancement can improve intrinsic resistance and capacitance. Parasitics are playing an ever-increasing role in circuit performance. The two major parasitic components in scaled technology are (1) contact resistivity between the silicide/Si interface and (2) the contact via resistivity.

The remainder of this review is organized as follows; we first discuss candidate transistor structures for continued device scaling; we then report a comparison of various mobility enhancement techniques; this is followed by a review of high-*k* gate stacks, novel contact technology, and silicides. The review closes with a summary of key messages.

Transistor structures

Ultrathin (UT) Si-on-insulator (SOI) MOS field-effect transistors (FETs) are an attractive option for device scaling because they can effectively reduce the SCE and eliminate most of the leakage paths (Fig. 1b)[2,3]. For thicker SOI channels, the drain field could easily penetrate into the source side through the channel or buried oxide when the gate length is reduced. The gate terminal can no longer prevent leakage from the drain to the source terminal. However, a thin SOI channel can resolve this problem. Unfortunately, the channel mobility is substantially degraded as the SOI thickness is reduced to below 10 nm[4].

The ultrathin SOI thickness requirement for SCE control in single-gate FETs can be relaxed by using a more complex 'double-gate' FET (Fig. 1c) that offers improved electrostatic gate control of the body. There are many reviews of double-gate devices[5-7]. The symmetric nature of a double-gate FET would require 50% less gate control capability for the same SCE characteristics. In a single-gate SOI device, the source potential could be affected by the drain potential through the buried oxide, resulting in a large leakage current. The double-gate structure can effectively eliminate this leakage because of the absence of buried oxide. Numerical simulations[2] indicate that double-gate FETs can be scaled to shorter gate lengths by a factor of 2.5-3. Because the double-gate device operates at much lower vertical electric fields, the mobility requirement in double-gate devices can be lower than that of conventional planar MOSFETs[8]. Double-gate FETs can be fabricated in many different ways. Of all the double-gate device structures, the FinFET[9,10] is the simplest to implement.

A successful semi-automatic microprocessor design migration, from planar to a double-gate FinFET design translation, has already been reported[11]. However, nonplanar transistor architecture will require new design infrastructure. The outlook from a recent panel discussion[12] on nonplanar transistors for logic applications was quite pessimistic. Any other ways to extend the conventional planar transistor architecture is therefore highly desirable.

An ion implantation technique called 'halo', where impurity dopants are placed next to the junction tip, is often used to control the SCE in planar transistors. The concept of 'super-halo'[13], where channel doping

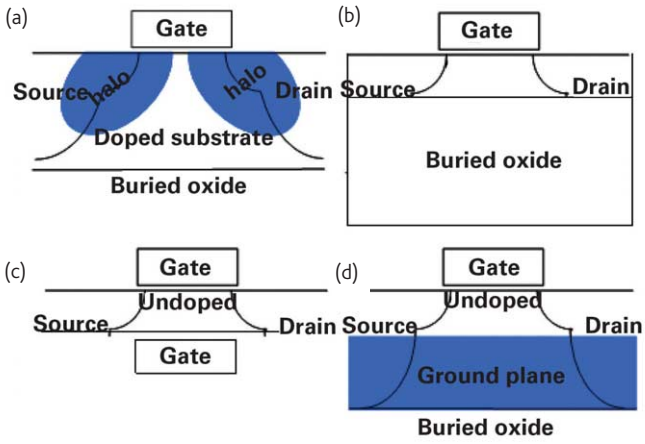

Fig. 1 Schematic device structures: (a) planar partially depleted Si-on-insulator (PDSOI); (b) ultrathin SOI (UTSOI); (c) double-gate MOSFETs; and (d) ground-plane SOI.

is highly localized, was proposed as the ultimate architecture for planar bulk CMOS transistor scaling. The super-halo profile could be produced by large-angle ion implantation and low thermal budget processes such as reversible spacer and laser spike anneal. However, topography restrictions (height and proximity of photoresist and poly-Si gate lines) tend to reduce the range of the implant angle. Ultra-scaled devices need a high halo concentration for SCE control; small-angle implants would have a reduced ability to position dopants underneath the gate. An alternative approach is to use an extreme super-steep retrograde well (SSRW) design called a ground plane (Fig. 1d) in a planar structure. For bulk MOSFETs or thick SOI devices, the high substrate doping needed in the ground plane architecture leads to increased band-to-band tunneling and junction capacitance, which are causes for concern. These problems can be alleviated by implementing the ground plane architecture on a thin body SOI substrate. High-performance ring oscillators with thin-body ground-plane CMOS and 35 nm gate lengths have been reported[14]. It should be noted that channel doping is likely to be needed for planar transistor scaling below 20 nm gate lengths. All reported sub-10-nm gate length planar transistors rely on a combination of channel doping with an extremely thin SOI[3] or very shallow junction[15]. In fact, for a given junction depth, UTSOI without channel doping is at least two times worse for SCE control[16] compared with that of bulk or thick SOI halo devices.

Mobility enhancement techniques: strain and orientation effects

Mobility enhancement is an attractive option because it can potentially improve device performance beyond any of the benefits resulting from device scaling. The two main approaches being pursued are strain engineering (both process- and substrate-induced) and orientation effects. Strain effects induced during the fabrication process can increase the channel mobility. Both tensile and compressive stresses

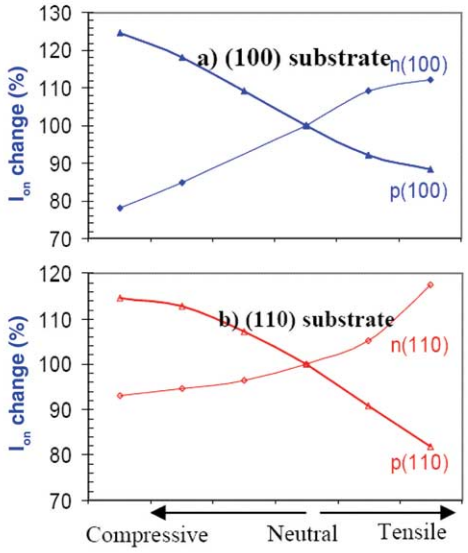

Fig. 2 The on-current (I_{on}) dependence on substrate surface orientation and type of longitudinal stress. The stress was varied by depositing different types (compressive, neutral, and tensile) and thicknesses of nitride films before the contact via process.

can be introduced in any one of three dimensions by process techniques. The electron and hole mobilities have different dependencies on the type of uniaxial stress[17]. On one hand, technology scaling will reduce the space available to introduce stress. On the other hand, a larger area will be under higher stress in shorter channel lengths in scaled technology. The scalability of local strain is one of the most important topics for future CMOS performance[18].

Inversion layer mobility depends on surface orientations and current flow directions. For *p*-channel MOSFETs, hole mobility is 2.5 times higher on (110)-oriented surfaces compared with that on standard wafers with (100) surface orientation[19]. However, electron mobility is the highest on (100) substrates. To realize the advantage of carrier mobility dependence on surface orientation fully, a new technology to fabricate CMOS on hybrid substrates with different crystal orientations has been developed[20], with nFETs on Si with (100) surface orientation and pFETs on (110) surface orientation. It has been shown that the strain and orientation effects on transistor performance are additive (Fig. 2)[18]. Full CMOS integration with ring-oscillator delay reduction has been demonstrated[21,22]. However, true transistor performance benefits in future scaled technology will need to be evaluated at the targeted dimension and pitch.

Strained-Si channels can also be produced by depositing Si epitaxially on relaxed SiGe crystals[23]. The strain is created from the differences in lattice spacing between Si and SiGe. While transistor performance enhancement has been reported, its progress has been hindered by the lack of low-cost, high-quality strained-Si substrates, as well as the challenges in materials and process integration. Alternative high mobility substrates such as the use of Ge[24] and III-V compound materials are being considered for post-CMOS applications. Basic scaling elements such as gate dielectrics and junction technology in these substrates are still in their very early research stages.

Novel gate stacks with high-*k* dielectrics and metal gates

For device scaling beyond the 65 nm node, the thickness of SiO_2-based gate oxides needs to be reduced to <1 nm. However, at these gate dielectric thicknesses a number of key dielectric parameters vital for high performance device operation, namely gate leakage current, oxide breakdown, and channel mobility, degrade[25]. A possible solution is to replace the conventional dielectric by a material with higher permittivity (*k*). High-*k* insulators can be grown physically thicker for the same (or thinner) equivalent electrical oxide thickness (EOT), thus offering significant gate leakage reduction[26]. After almost a decade of intense research on different high-*k* alternatives, the family of hafnium-oxide (HfO_2)-based materials has emerged as the leading candidate to replace SiO_2 gate dielectrics in advanced CMOS applications[27,28].

Combining poly-Si gates with HfO_2 was initially believed to be a 'simple' solution that would provide a significant gate leakage benefit while maintaining other dielectric properties similar to SiO_2. However, it became evident that poly-Si/HfO_2 stacks suffer from degraded electron mobility[29] (the result of soft optical phonon scattering[30]) and significant charge trapping (threshold voltage V_t shift with voltage or current stress)[31]. Both of these problems can be alleviated by replacing HfO_2 with HfSiO as the gate dielectric. Additional nitrogen incorporation into the HfSiO is beneficial since it suppresses high-*k* crystallization, increases the dielectric constant, and aids interfacial layer scaling. However, nitrogen close to the channel also introduces fixed charge that degrades carrier mobility through Coulomb scattering. Even with nitrogen incorporation, however, effective EOT (T_{inv}) scaling below 2 nm has been found to be difficult, largely because of poly-Si depletion (charge depletion in inversion region that accounts for ~0.3-0.4 nm or equivalent of parasitic capacitance). This issue remains a significant obstacle to the implementation of poly-Si/high-*k* stacks for high-performance logic applications. Another significant challenge for poly-Si/high-*k* stacks is the large observed V_t shift (~600 mV) of poly-Si pFET devices, attributed to Fermi-level pinning[32]. Recently, scalable capping layers have been developed that enable pFET V_t control without degrading device performance[33]. Combined with implant engineering, selective pFET implementation of such capped HfSiO gate dielectrics holds promise for successful poly-Si/high-*k* CMOS fabrication, especially for low standby power applications.

The use of metal gate electrodes, which eliminates poly-Si depletion and metal gate/high-*k* dielectrics, can result in aggressive scaling with EOT <1 nm. In order to achieve appropriate V_t it is essential to use metal gates with a near-band-edge work function for conventional planar MOSFETs. Research on band-edge dual work function (ϕ_m) metal gate electrodes has been gaining momentum, as conventional gate stacks run out of steam for sub-65 nm technologies. Thermal stability

requirements initially drove the need for low temperature (<600°C) gate last processes for metal gate/HfO_2 devices. However, while these stacks showed significantly lower charge trapping compared with poly-Si gates, it was also shown that low temperature processing results in degraded electron mobilities[34,35]. Increasing the thermal budget significantly improves electron mobilities[35], with the observed improvements attributed to a combination of processes including the formation of a relaxed SiO_2/Si interface at temperatures >950°C and structural relaxation and modification at the HfO_2/SiO_2 interface[36]. By careful process optimization, including the use of non-nitrogen interface layers, high-temperature processing, appropriate electrode materials, and electrode structures to prevent regrowth, record electron mobilities at a T_{inv} of 1.4 nm[36] as good as or better than aggressive poly-Si/SiON stacks have been obtained (Fig. 3).

The most critical challenge that remains for metal gate/high-*k* stacks is the V_t stability of metal gates when in contact with Hf-based dielectrics. For high ϕ_m metal gates (ϕ_m = 4.9-5.2 eV for pFETs), it has been observed that thermal processing induces significant drift in the V_t indicative of a midgap effective work function[37]. By using appropriate low temperature oxidizing ambients, most of this shift is recovered, suggesting that the the original shift toward a midgap effective work function at elevated temperatures is the result of an increase in the oxygen vacancy concentration in the HfO_2 near the metal contact[37]. On the other hand, low work function metal gates (ϕ_m = 4.1-4.4 eV for nFETs) are either unstable at high temperatures or are still significantly shifted from the Si conduction band edge. Therefore, while high mobility and T_{inv} scaling are now achievable with metal gates, band-edge work function metal/high-*k* stacks remain elusive and might require significant changes to conventional integration schemes.

An alternate and elegant approach to fabricating metal-like gates is to convert the conventional poly-Si gate into a silicide material after source/drain activation anneals to form fully silicided (FUSI) gates. In the last couple of years, NiSi-based silicides have emerged as the leading FUSI material[40]. Since undoped NiSi gates exhibit a midgap work function, achieving band-edge work functions is also a key issue with FUSI gates. Poly-Si predoping (e.g. As, Sb, or P ion implantation for nFETs and Al or B ion implantation for PFETs) of FUSI gates on SiO_2-based gate dielectrics can be used to adjust the V_t[40] within 150 mV (pFET) and 300 mV (nFET) from the midgap value of undoped NiSi. However, poly-Si predoping becomes less efficient in the case of FUSI gates on high-*k* dielectrics because of the Fermi-level pinning discussed previously. For FUSI gates, this problem can be mitigated by using: (i) metal- and Si-rich phases of Ni silicides[41]; (ii) Pt silicides or Pt alloys; and/or (iii) more stable silicate and nitrided silicate materials[42]. Another means of adjusting V_t is to alloy Ni silicides with elements that help to move the work function toward the band edges. For example, devices with NiPtSi FUSI gates show V_t close to a quarter-gap pFET value, whereas alloying with Al shifts the work function almost to

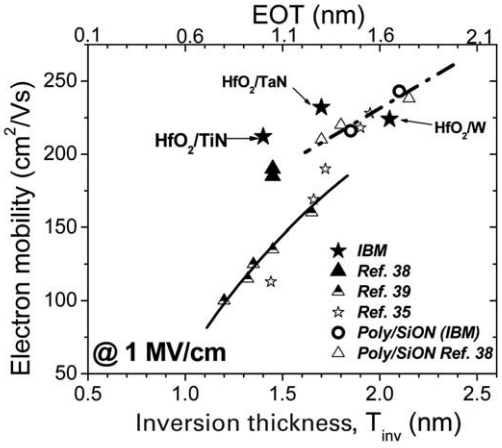

Fig. 3 Comparison of electron mobility (at 1 MV/cm) versus T_{inv} for different metal-gated HfO_2 gate stacks. The top trend line represents a typical mobility-T_{inv} relationship for polySi/oxynitride gate stack. The bottom trend line represents previously reported mobility-T_{inv} data for metal-gate/high-k gate stacks. (Adapted from[36]. Reprinted with permission. © 2006 IEEE.)

the nFET band edge[42]. The mechanism of this V_t modulation is not fully understood; it is believed that it could be caused by segregation of the alloying element at the FUSI/dielectric interface. Thus, while FUSI devices are an attractive metal gate integration option that offer a number of device benefits similar to deposited metal gates, the most significant challenge to overcome lies in the ability to silicide the poly-Si gates in both long- and short-channel devices simultaneously, while maintaining close to band-edge nFET and pFET V_t values.

Novel contact technology

As discussed earlier, one of the key obstacles in effective device scaling is the increasing extrinsic resistance of transistors[43]. Historically, the main components of this parasitic resistance consisted of channel, junction, and silicide-to-junction contact resistance components. However, as device dimensions approach the 45 nm technology node, an additional parasitic component, namely contact-level resistance, starts to influence the circuit performance increasingly[44]. Three critical notions need to be considered when scaling of the contact level is evaluated. First, contact resistance is inversely proportional to the contact area and hence for future technologies a dramatic increase of contact resistance is predicted (Fig. 4 indicates that contact resistance roughly doubles every new generation). Secondly, as the dimensions are scaled beyond the 45 nm technology node, a small variation in the contact geometry (via the diameter or height, as well as the liner thickness) will cause a strong response to the plug resistance range, i.e. an increased process dependent resistance spread (3 sigma value) will be observed (error bars in Fig. 4). Finally, for scaled-plug geometries, new materials and processes will need to be developed as the current W-based plug technology may not be sufficient beyond the 45 nm technology node. Hence, it is important to find possible solutions to retard the parasitic effects of contact scaling on transistor

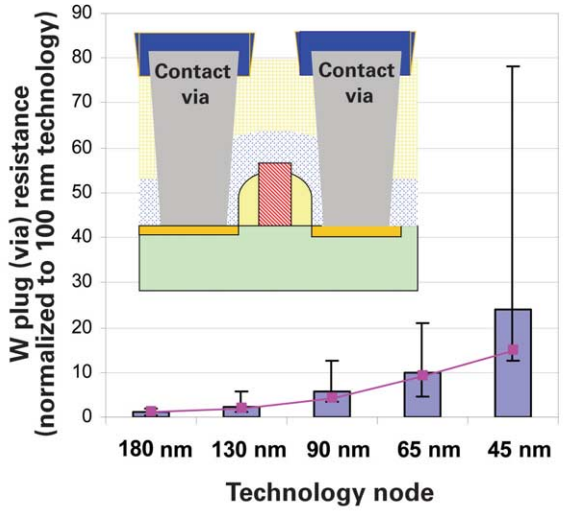

Fig. 4 Tungsten (W) plug contact scaling trend showing climbing resistance and increased process variability (3 sigma values) raising concerns for the next CMOS generations. A schematic of the contact via in MOSFETs is also shown.

performance. In practice, the reduction of contact resistance can be obtained by reducing the barrier (liner diffusion layer) thickness, as well as providing a lower resistance filling material. The limitation of the current W-based process is the inability to shrink highly resistive liners and nucleation layers reliably, as well as the lack of a low-resistance W deposition process with good fill capability (to minimize the creation of seams). Hence, alternative material options are being evaluated.

The ability to use the standard back-end-of-line (BEOL) or interconnect technology at the contact level would be extremely beneficial from a manufacturing point of view, as a full set of 300 mm Cu-based tools already exists. A few reports have demonstrated the successful use of a Cu metallization process at the contact level[45,46] using older generation hardware, and others show the potential of alternative BEOL solutions using other low-resistivity materials[47]. To prove the capability of new materials and their extendability for next technology generations, a variety of tests showing good front-end-of-line (FEOL) and BEOL reliability and yield still need to be demonstrated at these small dimensions. Since the contact level has vias with higher-than-standard BEOL aspect ratios, good fill capability will be hard to achieve. In addition, circuit measurements for transistors with single contacts are critical to evaluate the parasitic contributions to the transistor series resistance reliably.

Novel silicides

In the 90 nm technology node, it is estimated that the silicide/Si contact resistance R_{con} accounts for roughly half the total external resistance in a MOSFET[48]. As the contact length L_{con} is scaled, current crowding effects[49] result in a significant increase in R_{con} as shown in Fig. 5. For conventional silicides, i.e. NiSi and $CoSi_2$ (where the Schottky barrier height is roughly half the band gap and the active

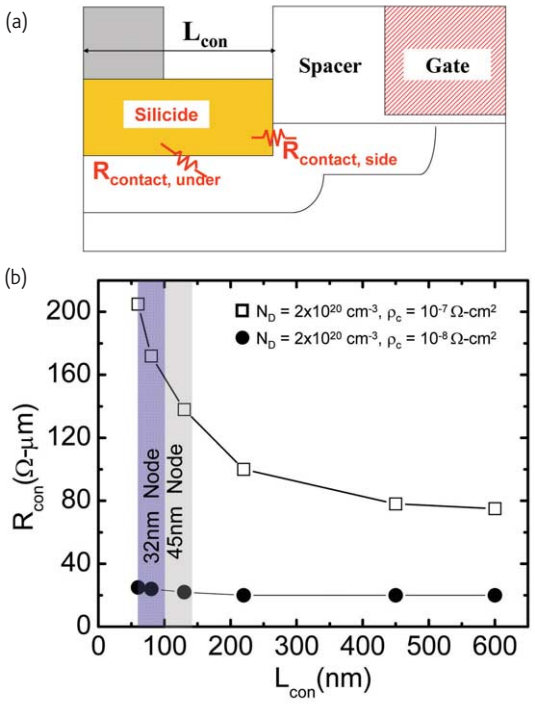

Fig. 5 (a) Schematic showing the silicide/Si contact near a MOSFET. (b) Silicide/Si contact resistance R_{con} as a function of contact length L_{con} for two different interface contact resistivities.

carrier concentration is limited by the dopant solid solubility to ~2 x 10^{20} cm^{-3}), it is estimated that for L_{con} ~100-150 nm (45 nm technology node) R_{con} will approach the maximum allowable external resistance prescribed by the International Technology Roadmap for Semiconductors (ITRS) roadmap for a MOSFET. For L_{con} ~60-100 nm (32 nm technology node), the silicide/Si contact resistance will exceed the maximum allowable parasitic external resistance prescribed by ITRS. In order to meet the scaling requirements for total external resistance, it is necessary to decrease the specific contact resistivity ρ_c of the silicide/Si interface by almost an order of magnitude from ~10^{-7} Ωcm^2 (achievable using conventional silicides and doping techniques) to ~10^{-8} Ωcm^2.

A promising approach to decreasing ρ_c involves the use of 'near-band-edge' silicides in place of conventional silicides. Unlike NiSi and $CoSi_2$, rare earth silicides such as Er and Yb silicide have a low Schottky barrier to the conduction band (<0.3 eV), making them ideal candidates for *n*-type contacts[50]. Similarly Pt and Ir silicides have a low Schottky barrier to the valence band (<0.3 eV) making them suitable for *p*-type contacts. While Schottky source/drain FETs have been demonstrated using Yb, Er, and Pt silicides[50-52], the impact of these novel silicides on the external resistance of high-performance conventional CMOS has yet to be clarified. In addition to the Schottky barrier, a number of other material and integration issues must be explored before the performance implications of these novel silicides can be fully understood. Some of the key material issues that require

further study include dopant segregation at the silicide/Si interface, thermal stability, narrow width effects on sheet resistance, etc. Integration issues such as the implementation of a 'dual silicide' process flow and yield detractors, such as silicide bridging over the source/drain spacer and silicide piping, also need to be addressed.

Alternative approaches for reducing the external resistance in MOSFETs involve decreasing the silicide/Si Schottky barrier by using a narrow band-gap material in the source/drain regions, e.g. $Si_{1-x}Ge_x$ and $Si_{1-y}C_y$. The increased solid solubility of B and the lower Schottky barrier at the Ge-silicide interface makes the SiGe source/drain approach particularly attractive for reducing the external resistance in pFETs[53]. Although recent studies indicate that a SiGe source/drain may also result in lower *n*-type contact resistance[53], SiGe induced compressive channel stress makes this approach less attractive for nFETs. Recently, $Si_{1-y}C_y$ alloys (where C ~1-2 at.%) have emerged as a viable alternative for low Schottky barrier contacts for nFETs.

Summary

Maintaining the performance of scaled transistors over the next decade will require innovation in device structures and integration of new materials. Although ultimate CMOS scaling will require nonplanar structures such as double- or multiple-gate devices, the design infrastructure and complexity of processing have hindered progress. The ground-plane structure is a promising alternative to ultrathin SOI devices. Strained-Si and orientation effects on mobility enhancement have been shown to be additive and are hence effective in improving performance without increasing leakage power. Metal-gate/high-*k* devices now exhibit high mobility at thin T_{inv}, however, controllable and reliable band-edge V_t still remains an issue. Parasitics could be the biggest factor in limiting performance in scaled high-performance transistors. It is therefore strategically important to start investigating alternative materials for the contact via and silicide processes. mt

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