CURRICULUM VITAE

Dr. Vikas Balikai

Assistant Professor || Electronics & Communication Engineering ||
District Coordinator IEEE
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EDUCATIONAL QUALIFICATIONS

Ph.D.- May 2021
School of Electronics Engineering - Vellore Institute of Technology, Vellore, INDIA
Thesis Title: A CMOS IMPLEMENTATION OF ALL DIGITAL PHASE LOCKED LOOP

M.Tech – Digital Communication - 2009-2011 *(8.91 CGPA)*
MSRIT, Bengaluru, Karnataka, INDIA

B.E – Electronics & Communication Engg - 2004-2008 *(68%)*
BLDEA's VP-PGHCET, Vijaypur, Karnataka, INDIA

Higher Secondary – 2004 – V. B. Darbar PU College, Vijaypur – 78.33 %
Secondary – 2002- V. B. Darbar High School -86%

EMPLOYMENT RECORD: Total: 10 years: (8 years in Teaching + 2 years in Industry)

Assistant Professor: KLS Vishwanathrao Deshpande Institute of Technology, Haliyal from 2014 onwards : : Department of Electronics & Communication Engineering.
Lecturer: KLS Vishwanathrao Deshpande Institute of Technology, Haliyal from 2013 to July 2014 : : Department of Electronics & Communication Engineering.
System Engineer: *Infosys Technologies* Ltd, Bengaluru from August 2011 to July 2013.
Has been a part of a project on ASIC DFT (Design for Test) at INTEL Corporation for six months during above tenure.
Research Intern: *Samsung India Software Operations*, Bengaluru from August 2009 to April 2010.

PROJECTS GUIDANCE

M. TECH. Thesis mentored

- FPGA implementation of high speed, low power architecture for Image compression using DCT, 2014-15.
- FPGA implementation of high speed wideband prescalar, 2017-18.

UG projects guided

- Current Project: Design and implementation of Low power phase locked loop.
- Exploring the unseen arena using Firebird V and spark V robots, 2019-20.
- Smart Library management system using Firebird V robot, 2019-20.
- Design and development of low-cost ECG system using microcontroller and MATLAB, 2014-15
- CMOS Implementation of a Novel Phase Frequency Detector, 2015-16.
- CMOS Implementation of Current Starved VCO and Digital Oscillator, 2015-16.
- Verilog implementation of JTAG architecture, 2017-18.

COURSES TAUGHT

VLSI Design - UG | Microelectronics – UG | Analog Circuits - UG |
Verilog HDL – UG | Basic Electronics - UG | Research Methodology – PG

RESEARCH PUBLICATIONS

- Vikas Balikai., & Kittur, H. (2021). A Low Power Phase Frequency Detector Suitable For biomedical applications" has been successfully submitted online for publication in International Journal of Electronics after revision – Taylor & Francis - TETN-2021-0129
- Vikas Balikai., & Kittur, H. (2021). Capacitive Boosted Ring Oscillator For ADPLLs has been accepted for publication in Vol 31, No 15, Dec 2021 edition of Journal of Circuits, Systems, and Computers (JCSC)– World Scientific - JCSC-2150273
- Vikas Balikai., & Kittur, H. (2020). A CMOS implementation of controller based all digital phase locked loop (ADPLL). Circuit World, 47(1), 71-85. https://doi.org/10.1108/cw-11-2019-0184.
- Vikas Balikai., & Kittur, H. M. (2019) Time amplifier based bang-bang phase frequency detector in 0.18µm CMOS technology. International Journal of Engineering and Advanced Technology, 9(1S3), 85-89. doi:10.35940/ijeat.a1017.1291s319.
- Vikas Balikai., & Kittur, H. M. (2019) Time amplifier based bang-bang phase frequency detector in 0.18µm CMOS technology in "The 2nd World Summit on Advances in Science, Engineering and Technology", October 3-5, 2019, Indiana University-Purdue University, Indianapolis, USA
- Vikas Balikai., & Kittur, H. M. (2017). Low power divide-by-16/17 pre-scalar using powerpc flip flop. 2017 International conference on Microelectronic Devices, Circuits and Systems (ICMDCS). https://doi.org/10.1109/icmdcs.2017.8211598.

PROFESSIONAL CONTRIBUTION as Expert Member & Reviewer for Journals/Conferences

Journal Name	Publisher
Circuit World (ISSN-0305-6120)	:Emerald Publishers
International Journal of Electronics (ISSN-0020-7217)	:Taylor and Francis
Canadian Journal of Electrical and Computer Engineering (ISSN-0840-8688)	:IEEE

Conference Name

IEEE Bangalore Humanitarian Technology Conference 2020

IEEE R10 Humanitarian Technology Conference 2021
IEEE DISCOVER 2021 (Conference Record #52564)
IEEE I2-CONECCT-2021 –A national Level Project Exhibition - Jury Member
IEEE CONECCT-2021

MEMBERSHIP OF PROFESSIONAL SOCIETIES:

- Member - IEEE. - 91176912
- Member Institution of Engineers –M-1697492

SPONSORED PROJECTS

- The Project titled "*Predictive agricultural Analytics*" has been sanctioned a grant of Rs. 3 Lacs under New Age Incubation network and GoK initiative.

ADMINISTRATIVE EXPERIENCE

- Director – Training & Placement from May 2019 to March 2021.
- VDIT IEEE student branch – Branch counsellor from Aug 2020 to till date.
- Member of Forum of Industry Institute Interaction Cell May 2017 to Mar 2020.
- Faculty Coordinator - Training & Placement Cell July 2015 to May 2019.

WORKSHOPS/TRAINING/COURSES ATTENDED

- *INUP familiarization workshop* on nanofabrication technologies in May 2014, IIT Bombay.
- Two Week ISTE STTP workshop on "*CMOS Mixed Signal and Radio Frequency VLSI Design*"-30-01-17 to 04-02-2017.
- Two week AICTE - FDP on "*Recent Advances and Challenges for Quality Assurance and Accreditation in the Higher Education for Modern World*" at University BDT College of Engineering during 11-23 Dec 2017.
- 12 week course on "*VLSI Physical Design*" conducted by NPTEL in the month of April 2018.
- 8 week course on "*CMOS Digital VLSI Design*" conducted by NPTEL in the month of April 2019
- One-week QIP STC on "*Analog Integrated Circuits Fabrication Process and Applications*", 13-17 Aug 2018 -Indian Institute of Science, Bengaluru.
- *e-Yantra Lab Setup Initiative* (eLSI), Workshop at IIT Bombay/DBCE Goa on 8-9 June, 2018/11-12 Jan 2019 respectively.
- One week AICTE Sponsored STC on *Phase locked loops* at IIT Madras from 17-22 Dec 2018.
- Two week AICTE STTP on "*Awareness of Intellectual property rights for Engineers and Industrialists*" Phase 2 from 07-12-2020 to 12-12-2020 & Phase 3 from 21-12-2020 to 26-12-2020 at SGBIT Belagavi.
- Two week joint FDP on *5G Design: Journey from Devices to Circuits* organized by Electronics and ICT Academies at IIT Guwahati, NIT Patna, MNIT Jaipur and IIITDM Jabalpur from 01 - 12 March, 2021.
- Two week joint FDP on "*RISC-V VLSI Implementation Flow: RTL2GDS*" organized by Electronics and ICT Academies at at IIT Guwahati, NIT Patna, MNIT Jaipur and IIITDM Jabalpur from 27-03-2021 – 10-04-2021.
- A 5 day "Memory Design Workshop", an online event organized by IEEE Circuits and Systems (CAS) Society Bangalore Chapter in association with IEEE Bangalore Section from 9th August to 13th August 2021.
- A 5-Day FDP on "Digital VLSI Design and Verification" from 23rd to 27th August 2021 Organized by Entuple Technologies Pvt Ltd , in Association with Department of ECE, Bangalore Institute of Technology and IEEE BIT CAS (Circuits and Systems) society.

WORKSHOPS CONDUCTED

- Successfully conducted a 4 Week course on Embedded Robotics for 30 students of VDIT-2019.
- Conducted a Short Term Training Program on "Verilog HDL" for Polytechnic students of 6 colleges at KLS VDIT from 1st January – 12th January 2018.
- Coordinated IOT challenge 2019 conducted by i3indya Technologies and IIT Bombay on Nov 3, 2018.
- Conducted a Hands-on Workshop on VLSI Design-from schematic to layout for 5th-semester students of ECE department from 19-08-2016 to 21-08-2016.

AWARDS / RECOGNITIONS / TALKS

- Nominated as IEEE Uttara Kannada District Coordinator from Aug 2020 to till date.
- Awarded with Class A certificate under E-Yantra TBT conducted by IIT Bombay in Feb 2019.
- Awarded as Young Achiever of the year at KLS VDIT in 2017.
- KSCST project funding of Rs. 5500/- in 2017 (37S0710).
- Appreciated by Texas instruments for mentoring projects in Texas Instruments Innovation Design Challenge India Design contest -2015.

TEACHING STATEMENT: I was originally attracted to an academic career in large part because of the opportunities it offers for teaching and mentoring activities. Over the past 8 years, my interest in teaching and mentoring has only become stronger and I believe that I have learned a lot and matured significantly in this time. I have taught more than 6 ECE subjects at under graduate and graduate levels.

I have consistently striven in my teaching and mentoring to achieve a balance between two goals: (1) to train students for productive personal careers in industry, government or academia in their immediate future, and (2) to educate future leaders, entrepreneurs and citizens in the long-term.

RESEARCH STATEMENT: Having been fortunate to have worked in VLSI industry, I believe I have good insight on these challenges. Therefore, my research vision is to create new mixed-signal architectures which will take advantage of the continued advantages of CMOS scaling, like improved transistor speed, while compensating for the growing disadvantages, such as larger process variations.

Under the above context, my work has centered on:

1) Analog, mixed-signal, circuits, aiming at enabling modeling, verification, and optimization of the interfaces of our electronic systems with the “real world”, which is the key bottleneck in advancing computing capabilities, design robustness, and energy efficiency for bio-medical applications.
2) Energy-efficient architectures, aiming at enabling design and analysis of large-scale systems that are responsible for distributing and regulating power, and hence playing a key role in robust low-power design.

FIELD OF RESEARCH INTEREST: Mixed mode VLSI design, All digital phase locked loops, Low power CMOS circuits.

REFERENCES

Dr. Harish M. Kittur (Ph.D Supervisor)
Professor & Dean
School of Electronics Engineering
VIT Vellore
Tamil-Nadu, INDIA
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Dr. B. K Sujatha (M.Tech Supervisor)
HOD, Dept of E&TC
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PERSONAL DETAILS

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Declaration

I hereby declare that the information furnished by me is true to the best of my knowledge.

Sincerely