B. Vikas Chandra

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Career Objective

To establish myself in an organization that provides ample opportunities for my development and to direct my knowledge, skill and attitude towards the fulfillment of organization's goal.

Major Skills

- Hardware Designing • PCB designing and assembly • Verilog and VHDL coding
• Cadence tool • Easy EDA tool • Xilinx ISE 14.7 • MatLab. • Modelsim

Career Profile

- Having one plus years of experience on image processing using MATLAB, Embedded Systems, FPGA design, Verilog and VHDL coding using XILINX and Cadence Tools
- Strong experience in VLSI coding
- Quite good in designing hardware and PCB design of size small to medium scale and assembling
- Worked on home automation devices using Bluetooth technologies
- Designed and Developed biometric products.

Activities and Achievements

- Participated in National Level Students Technical Paper Symposium held on 2015 at HMSIT, Tumakuru.
- Worked as an Intern at Inventeron Technologies and Business Solutions LLP on Embedded System (Dec-2014 to March 2015).
- Worked as an Intern at Certitude Technologies Pvt. Ltd.
- Participated and secured 3rd place in Panchajanya 2017 held on 27th March 2017 at Ekalavya Institute of Technology, Chamarajanagara.
- Participated in TECHXELLENCE 2017 held on 19th April 2017 at New Horizon College of Engineering, Bengaluru.
- Participated in NCICC 2017 held on 27th April 2017 at Shridevi Institute of Engineering and Technology, Tumakuru.

Projects Worked on

BACHELOR OF ENGINEERING PROJECT:

Title: CLOTHING PATTERN RECOGNITION FOR VISUALLY IMPAIRED PEOPLE USING IMAGE PROCESSING.

Team Size	4
Tools	Keil Compiler, MatLab
Language	Embedded C

Description: Clothes pattern recognition is challenging task for blind people. Automatic clothes pattern recognition is also challenging problem in computer vision due to large pattern variation. In this project, we represent a new method to classify clothes patterns into 4 categories and verbal output is given.

MASTER OF TECHOLOGY PROJECT:

Title: DESIGN AND IMPLEMENTATION OF MODIFIED PARTIAL PRODUCT FOR RADIX-4 BOOTH ALGORITHM USING FPGA.

Team Size	1
Tools	Xilinx ISE 14.7, ModelSim
Language	Verilog

Description: In digital signal processing, high speed multipliers plays vital role. Performance of system depends on type of multiplier used in system. Multiplier consumes more time compared to other athematic operators; the major issue in designing a system is its delay and area, if multiplication delay and area increases then system area and delay will be increased. Hence design of high speed multipliers to decrease the amount of calculation stages, for high speed multiplication Modified Booth encoding (MBE) multiplication scheme is used.

Personal Details

• **Name**	B. Vikas Chandra
• **DOB**	5th July 1993
• **Gender**	Male
• **Address**	Permanent Address
	S/O B. Ramachandraiah 7th main, Vasanth Nagar, Bangalore-560052
• **Languages Known**	English, Kannada, Telugu, Tamil.

Declaration

I declare that the information given above is true to the best of my knowledge.

Date: **Signature**

Place: **[B. Vikas Chandra]**