MATRUSRI ENGINEERING COLLEGE
SAIDABAD, HYDERABAD – 500 059
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Assignment III

Class/Branch: III SEM ECE **Date: 02.11.2025**
Subject: DLD **Max Marks: 10**

Syllabus: Unit III

1. Explain the architecture of CPLD in detail.
2. Write the classification of PLDs.
3. List differences between PLA & PAL.
4. Describe the general structure of PAL with neat diagram and Realize the half adder circuit using PAL.
5. Where PAL is same as PLA? Explain.
6. Explain detail about PLA & mention its advantages and disadvantages.
7. State any two applications of PLA's.
8. Analyze the block diagram of FPGA and explain the significance of each block.
9. Make use of programmable logic array. Realize the Boolean expression $f_1 = \Sigma m(2,4,6,7)$ & $f_2 =$ bc+a'bc'+abc.
10. Realize the given logic function using PAL $f_1 = x_1'x_2'x_3'+x_1'x_2x_3$ & $f_2 = x_1'x_2'+x_1x_2x_3$
11. Write the comparison between CPLD and FPGA.
12. What is LUT? Draw the diagram of 2-input LUT.
13. Draw the 3-input LUT and explain. Program the LUT to implement the logic function $F = X_1X_2'X_3$ where X_1 is the MSB.