Course Code	Course Title						Core/Elective
ES302ECU23	**Digital Logic Design**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
-	L	T	D	P			
	2	1	-	-	30	70	3

Course objectives:

1. Learn fundamental concepts & basic techniques for the design of digital circuits.
2. Understand the different number representations in digital electronic circuits and be able to convert between different representations.
3. Implement logical operations using combinational logic circuits.
4. Impart to student the concepts of sequential circuits, enabling them to analyse sequential systems in terms of state machines.
5. Summarize the concept of flip-flops, sequential circuits and their applications.

Course outcomes: After the completion of the course students will be able to

1. Understand the design process of digital hardware, use Boolean algebra to minimize the logical expressions and optimize the implementation of logical functions.
2. Understand the number representation and design combinational circuits like adders, MUX etc.
3. Design Combinational circuits using programmable logic devices.
4. Analyse sequential circuits using flip-flops and design the registers& counters.
5. Represent a sequential circuit using Finite State machine and apply state minimization techniques to design a FSM

Unit-I

Number System and Boolean Algebra: Number Systems Decimal, Binary, Octal, Hexa-decimal, Base Conversion Methods, Complements of Numbers, Binary to Gray & Gray to Binary. Logic gates, Realization using Gates, Postulates & Theorems of Boolean Algebra. Reduction of Boolean Expressions using Boolean Algebra

Unit -II

Minimization Techniques: The minimization with theorems, The Karnaugh Map Method, Three, Four and Five variable K- Maps, Quine-McCluskey Method

Combinational Circuits: Full adder, Subtractor, Multiplexer, Demultiplexer, Encoder, Decoder, Gray to Binary and Binary to Gray converter

Unit-III

Programmable Logic devices: Structure and implementation of PLA& PAL Structure of CPLDs, FPGA, Two input and three input lookup table

Unit -IV

Latches & Flip-Flops: SR, JK, D, T Flip-Flops, Characteristic tables, Characteristic equation, Excitation Table, Conversion of Flip-flops.

Sequential circuits: Synchronous, Asynchronous counters, Up-down counter, Modulus counter, Serial in- Serial out, Parallel-in parallel out, Parallel in Serial out & Universal registers.

Unit -V

Sequential Circuit design: Sequential design procedure, State diagram State table, Design of Modulus counter, Introduction to FSM, Mealy & Moore FSMs, Sequential detector.

Suggested Readings:

1. Moris Mano and Michael D CIletti, "*Digital Design, Pearson*", 4th edition,2008
2. Zvi Kohavi, "*Switching and Finite Automata Theory*", 3rd ed., Cambridge University Press-New Delhi, 2011.
3. Ronald J.Tocci, Neal S. Widmer & Gregory L.Moss, "*Digital Systems: Principles and Applications*", PHI, 10/e, 2009.
4. R. P Jain, "*Modern Digital Electronics*", McGraw Hill Education (India) Pvt. Limited, New Delhi
5. Anand Kumar A, "*Fundamentals of Digital Circuits*", Prentice-Hall of India private Limited, New Delhi
6. Thomas L Floyd and Jain, "*Digital Fundamentals*", Eleventh Edition, Pearson, 2015
7. Charles H. Roth, Jr., Larry L Kinney, "*Fundamentals of Logic Design*", Cengage Learning, 2013 Online