Digital Electronics and Logic Design(DELD)

(B.E IT IIIrd sem)

Question Bank

Short Answer Questions

Unit-I

1. What is Moore's law
2. Define analysis and synthesis of a logic circuit
3. 3.Implement XOR2 gate using NAND gates only
4. Define prime implicant and Essential prime implicants of a logic function
5. State Demorgan's law
6. Synthesize the logic function f= ab+a'b+ab'
7. Use algebraic manipulation to simplify x'y+xy+xz'+xy'z'

Unit-2

1. Perform the following arithmetic operations.
   a) 23+(-11) b) -16+9 c) -14-8
2. Write the truth table of half adder and realize it using logic gates
3. 3.State Shannon's expansion theorem
4. Obtain the truth table of 1-bit comparator and write thier logical expressions.
5. What is a priority encoder and write the truth table of 8 to 3 priority encoder
6. 6, Realize a full adder using half adders
7. Convert the following binary numbers to gray code
   i) 1101 ii) 1011 iii)10111
8. Realize a logic function f(a,b,c) = ∑m(0,1,4, 5,6,7) using a 4:1 MUX

Unit-3

1. Define a PLD. Differentiate PLA and PAL
2. Draw the structure of CPLD
3. Implement a OR2 gate using 2-input LUT
4. Write verilog code to realize the logic function f=ab+bc+ca
5. write veriog code for a full-adder.
6. Write verilog code for 2 to 4 decoder

Unit-4

1. Draw the logic diagram of basic SR latch using NOR gates and write its truth table
2. Differentiate combinational circuits and sequential circuits
3. Draw the logic diagram of gated SR latch using NAND gates and write its truth table
4. Draw the logic structures of D, JK, & T flip-flops and write their truth tables
5. Write the excitation tables of D, JK & T flip-flops and also write their characteristic equations
6. Differentiate synchronous and asynchronous counters
7. Write verilog code for D flip-flop

Unit-V

1. Draw the block diagrams of Mealy and Moore FSM
2. Compare Mealy and Moore FsM
3. Define state diagram and a state table
4. Draw a Mealy state diagram to detect a sequence '01;
5. Write the elements of ASM chart and draw their symbols.

Long Answer Questions

Unit-1

1. Explain the development process of digital hardware
2. Explain the design flow of logic circuits
3. 3.Obtain the minimal SOP of the following logic function using K-map and realize using NAND gates only
   $f(a,b,c,d) = \sum m(9,10,12) + d(3,5,6,7,11,13,14,15)$
4. Obtain the minimal POS of the following logic function using K-map and realize using NOR gates only

$f(x,y,z,w) = \prod M(3,6,8,11,13,14)\ .d(1,5,7,10)$

5. Obtain the minimal expression using the tabular (Quine-McClusky) method for the following function
   $f(A,B,C,D) = \sum m(0,1,3,4,5,7,10,13,14,15)$

Unit-II

1. Write the truth table of a full adder and obtain its logic diagram
2. Implement a 16:1 MUX using 4:1 MUX
3. Implement a 4 to 16 decoder using 3 to 8 decoders
4. Implement a BCD to seven segment display
5. Implement a BCD to excess-3 code converter
6. Realize a full adder using 3 to 8 decoder
7. Implement the following function using 4:1 MUX
   $F(x,y,z) = \Sigma m(0,2,3,5)$

Unit-III

1. Draw the PAL and PLA structure of full adder
2. Implement the following logic functions using PLA and PAL

$F_1(A,B,C) = \Sigma m(0,1,2,4)$, $F_2(A,B,C) = \Sigma m(0,5,6,7)$

3. Draw the structure of CPLD and explain its features
4. Draw the structure of FPGA and explain its features
5. Write verilog code for all logic gates

Unit IV

1. Design a Mod-6 asynchronous counter using T flip-flops
2. Draw the structures of 3-bit up and down asynchronous counters using T Flip-flops. Show the count sequence with a timing diagram.
3. Design a synchronous decade counter using JK flip-flops.
4. Explain about master-slave D flip-flop
5. Write verilog code for
   D FF ii. JK FF iii. T FF

Unit V

1. Draw the Mealy and Moore FSM for a serial adder/Full adder.
2. Write the basic design steps of designing synchronous sequential circuits
3. Draw the state diagram, state table of D, T and JK flip-flops
4. Obtain a state diagram and state table using Mealy FSM to detect the sequence '1111'.
5. Derive the state diagram for a FSM that has input w and output z. The machine has to generate z=1 when the previous two values of w is 11, otherwise z=0. Overlapping input patterns are allowed. An example of the desired behaviour will be

   w : 010101101110
   z : 000000010011

   Also draw the ASM for the same FSM.