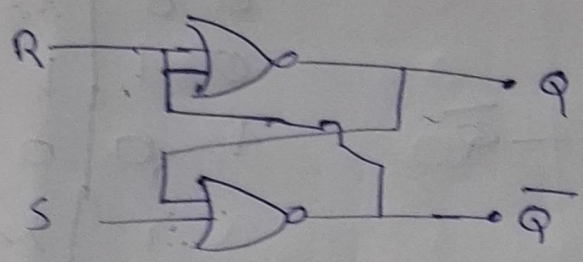
DLD Unit-4

SR latch by NOR



T.T of NOR gate

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

Case(i)

S=0, R=1

Q=0

$\bar{Q}$=1

S=0, R=0, Q=0, $\bar{Q}$=1 — memory

Case(ii)

S=1, R=0, Q=1 $\bar{Q}$=0

S=0, R=0, Q=1, $\bar{Q}$=0 — memory

Case(iii)

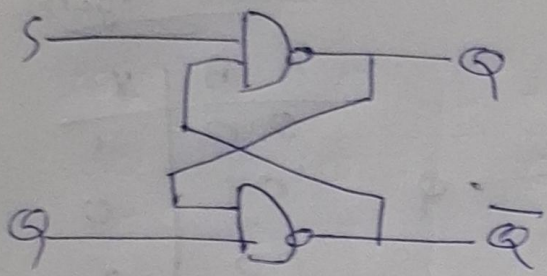
S=1, R=1, Q=0 & $\bar{Q}$=0

Q = $\bar{Q}$ ✗

S=0, R=0, Q=0, $\bar{Q}$=1

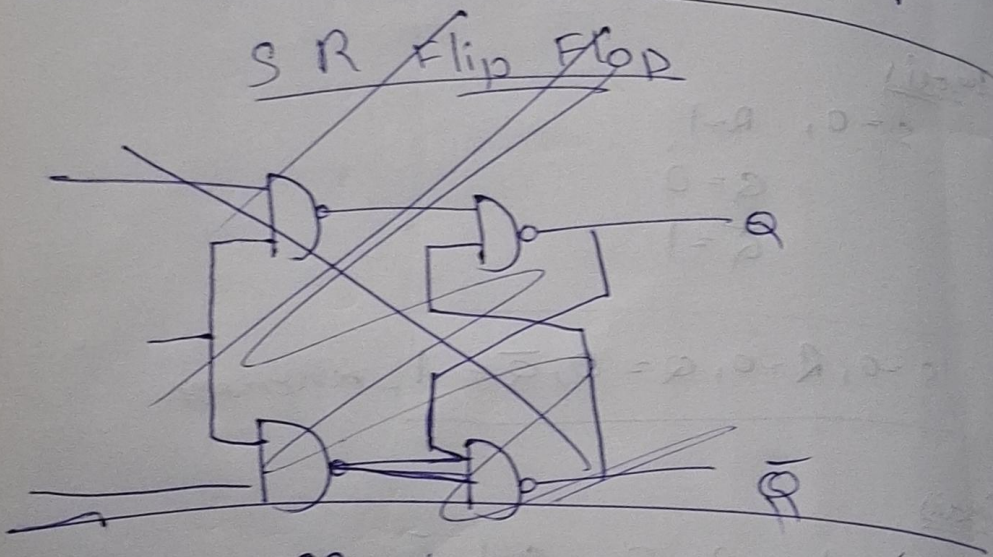
S	R	Q	$\bar{Q}$
0	0	memory	
0	1	0	1
1	0	1	0
1	1	Not use	

Latch NAND

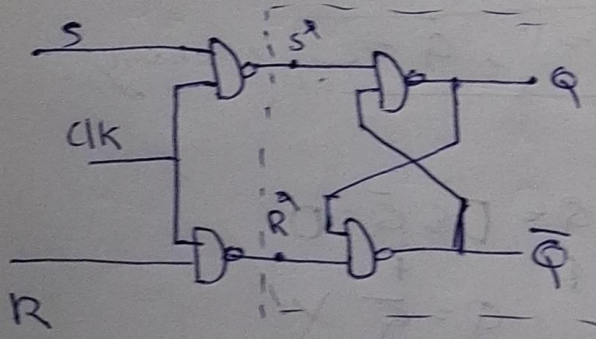


S	R	Q	$\bar{Q}$
0	0	Not used	
0	1	1	0
1	0	0	1
1	1	Memory	

S R Flip Flop



SR Flip Flop



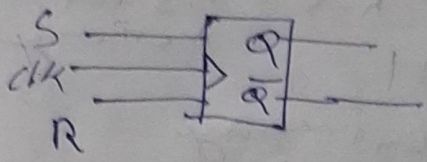
NAND latch

S^*	R^*	Q	$\bar{Q}$
0	0	Not used	
0	1	1	0
1	0	0	1
1	1	Memory	

$$S^* = \overline{S \cdot Clk} = \bar{S} + \overline{Clk}$$

$$R^* = \overline{R \cdot Clk} = \bar{R} + \overline{Clk}$$

Symbol



CLK = 1,
$S^* = S$
$R^* = R$

CLK = 0, $Q^* = \overline{CLK} + \bar{S}$
$1 + \bar{S} = 1$
$R^* = 1$

CLK	S	R	Q	$\bar{Q}$
0	x	x	Memory	
1	0	0	Memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	Not used	

Truth table

clk	S	R	Q_{n+1} (N.S)
0	x	x	$Q_n \rightarrow$ R.S
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid

Characteristic Table

assume CLK=1

N.S = P.S for memory

Q_n	S	R	Q_{n+1}
0	0	0	0 = (Q_n) memory
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
		memory	
1	0	1	0
1	1	0	1
1	1	1	X

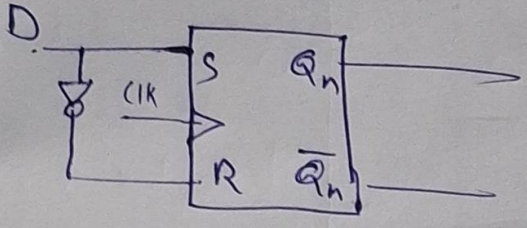
Excitation Table

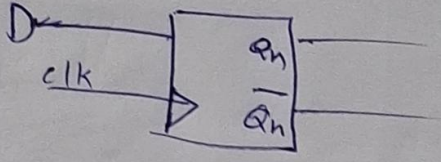
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D - Flip flop

Truth table SR Flip Flop

CLK	S	R	Q_{n+1}
0	x	x	Memory
1	0	0	Memory
1	0	1	0
1	1	0	1
1	1	1	invalid





Truth table D Flip Flop

clk	D	Q_{n+1}
0	x	Q_n
1	0	0
1	1	1

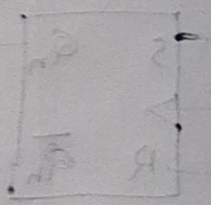
Characteristic Table

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

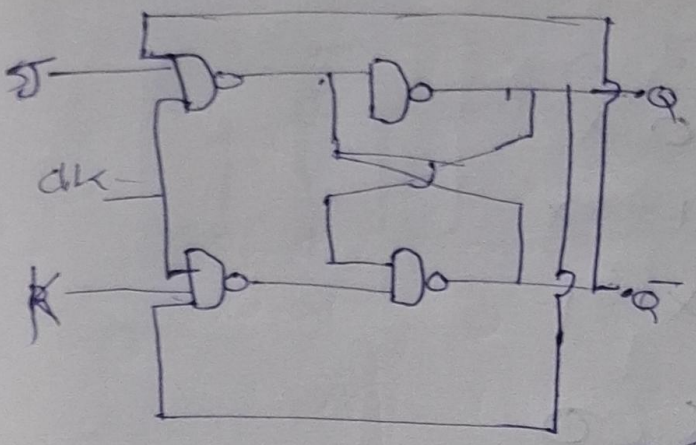
$Q_{n+1} = D$

Excitation Table :-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1



JK Flip Flop



T.T

clk	J	K	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n$ (toggle state)

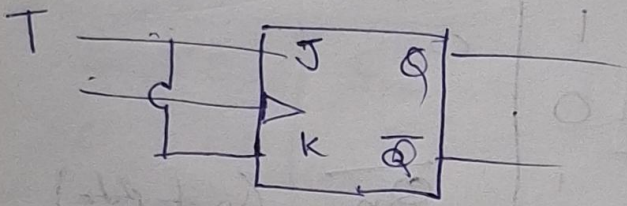
Ch Table

Q_n	J	k	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

T flip flop



T.T

J/K	T	Q_{n+1}
0	X	Q_n no change
1	0	Q_n no change
1	1	$\bar{Q}_n$

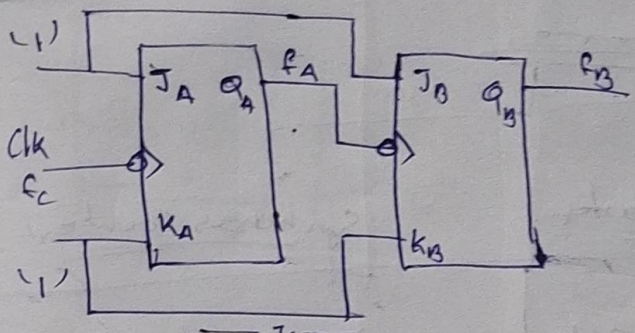
Ch. Table

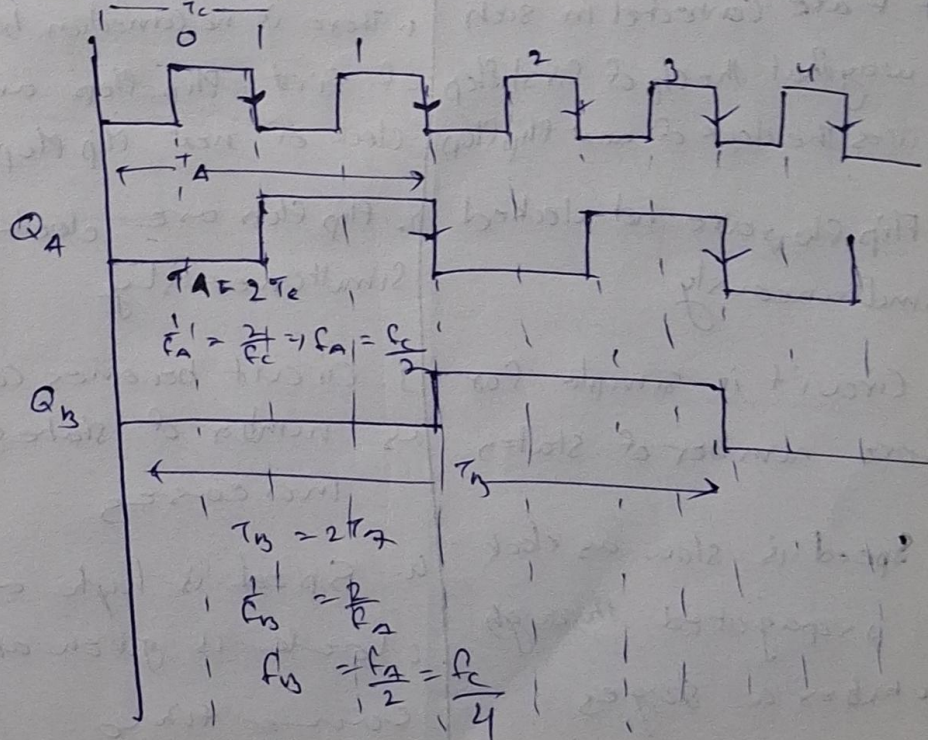
Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

FF as divide by 2(k) :- Counter





counter no of FF

2^n $n = 2$

$2^2 = 4$

clk	Q_B	Q_A
0	0	0
1	0	1
2	1	0
3	1	1

Counters

Asynchronous/Ripple counter

Synchronous Counter

- F.F are connected in such a way that the o/p of first flop drives the clock of next flip flop
- Flip flop are not clocked simultaneously
- Circuit is simple for more number of states
- Speed is slow as clock is propagated through number of stages

- There is no connection b/w o/p of first flip flop and clock of next flip flop
- Flip flop are clocked simultaneously
- Circuit becomes complicated as number of states increases
- Speed is high as clock is given at a same time

Counters (ASIS)

1. Upcounter
   0 - 1 - 2 - 3 - - -
2. Down counter
   7 - 6 - 5 - - - 0
3. Up/docon count
   Combination of both

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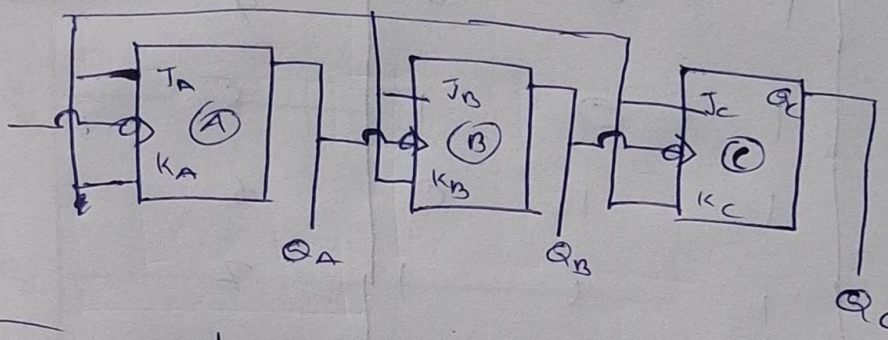
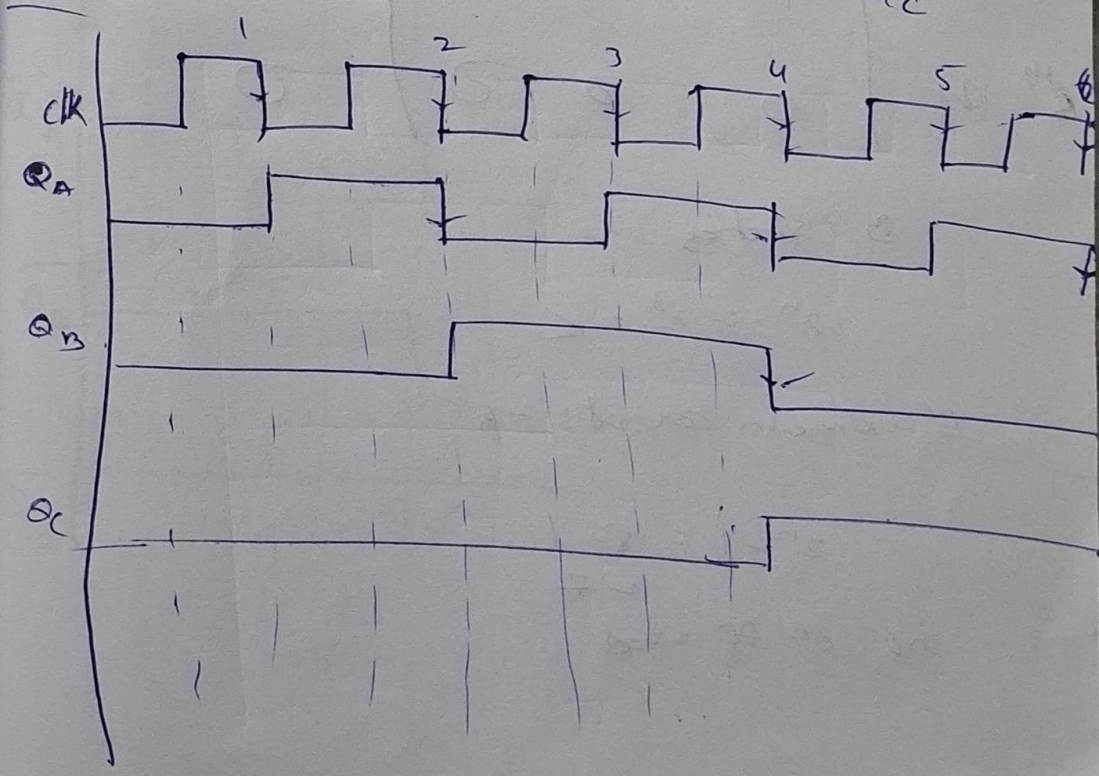
3 Bit Asynchronous up counter





clock	Q_C	Q_B	Q_A	Decimal eq
Initially	0	0	0	0
1st (↓)	0	0	1	1
2nd (↓)	0	1	0	2
3rd (↓)	0	1	1	3
4th (↓)	1	0	0	4
5th (↓)	1	0	1	5
6th (↓)	1	1	0	6
7th (↓)	1	1	1	7
8th (↓)	0	0	0	0

8 states

$2^n = 2^3 = 8$

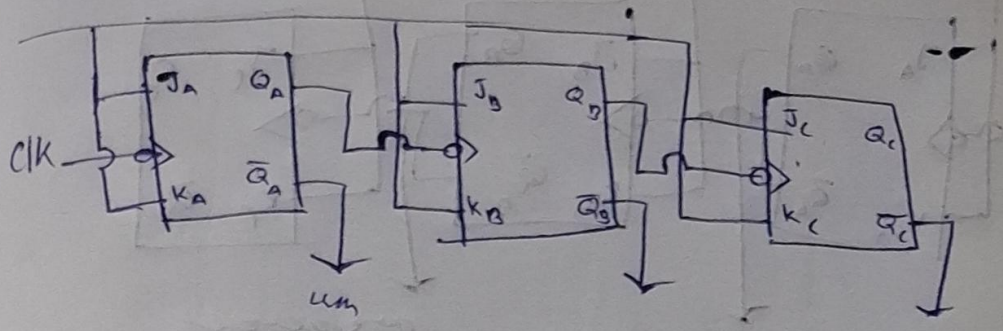
Maximum count = 8

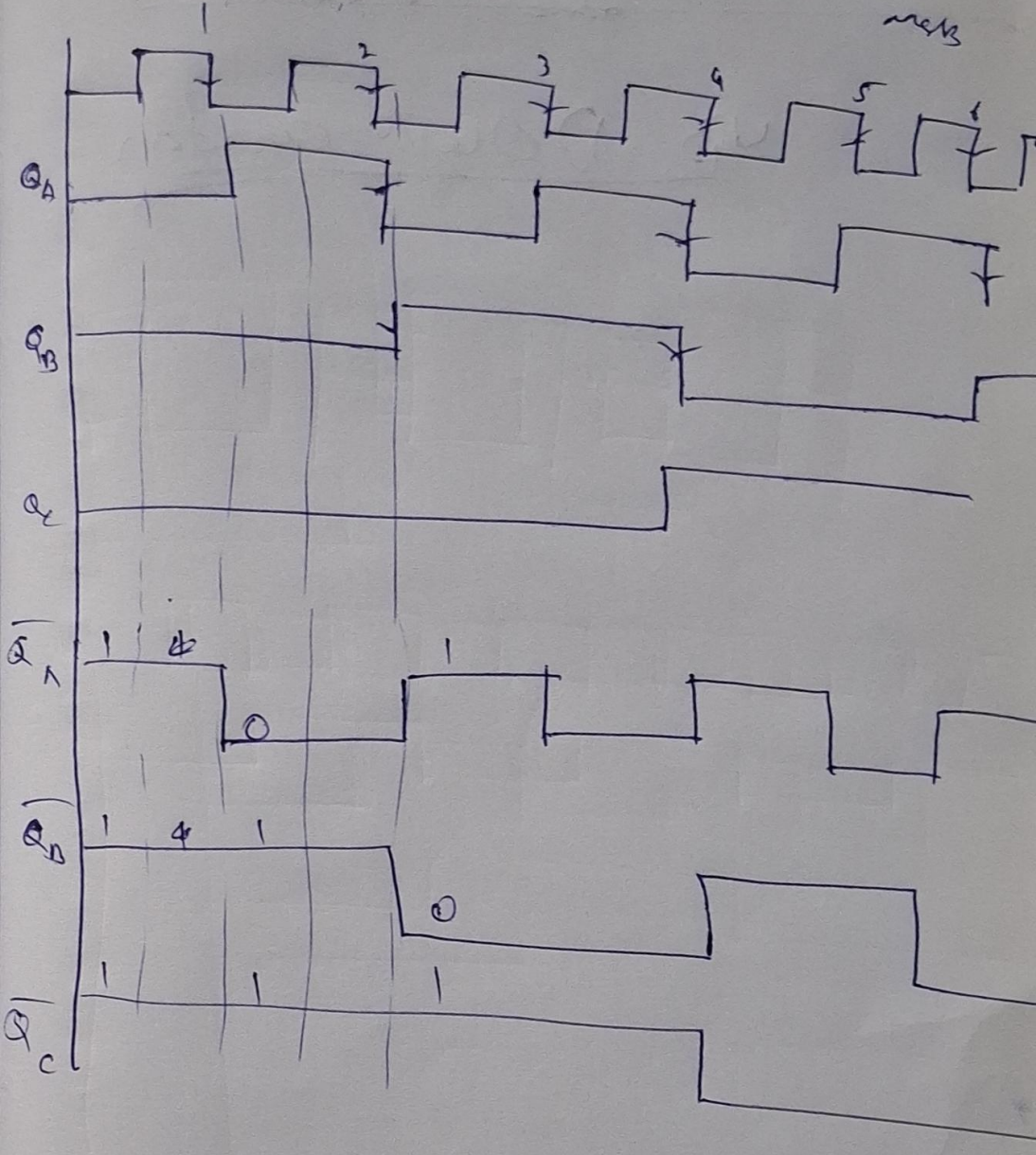
$2^n - 1 = 8 - 1$

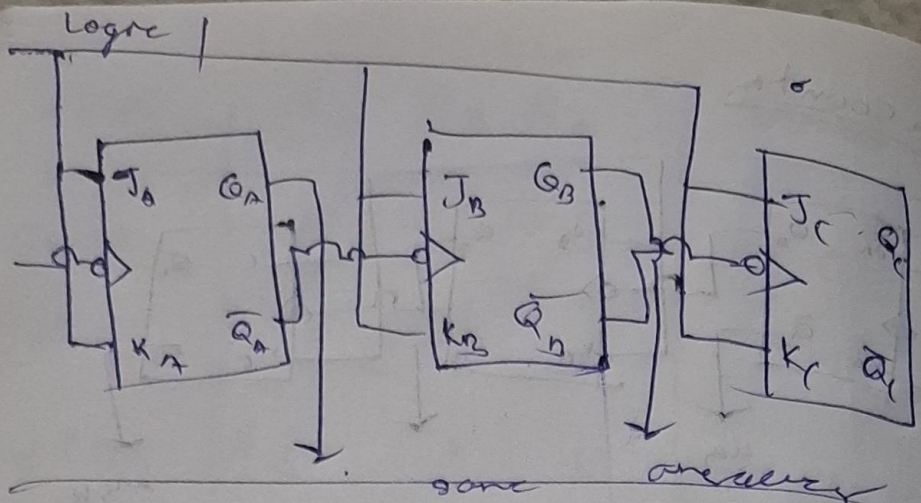
$= 7$

no. of ff used

Down counter







U,D DOWN counter