# Matrusri Engineering College

Sponsored by Matrusri Education Society, Estd.:1980
An Autonomous Institution | Approved by AICTE, Affiliated to Osmania University
#16-1-486, Saidabad, Hyderabad-500059, Ph:040-24072764
Department of Computer Science and Engineering


## Assignment II

**Class/Branch: III SEM CSE B & D** **Date: 17.10.2025**

**Subject: Digital Logic Design** **Max Marks: 10**

**Syllabus: Unit II**

**Minimization Techniques:** The minimization with theorems, The Karnaugh Map Method, Three, Four and Five variable K- Maps, Quine-McCluskey Method
**Combinational Circuits:** Full adder, Subtractor, Multiplexer, Demultiplexer, Encoder, Decoder, Gray to Binary and Binary to Gray converter

**COURSE OUTCOMES (COs):**

| **After the completion of the course students will be able to** | |
|---|---|
| CO1 | Understand the design process of digital hardware, use Boolean algebra to minimize the logical expressions and optimize the implementation of logical functions. |
| **CO2** | **Understand the number representation and design combinational circuits like adders, MUX etc.** |
| CO3 | Design Combinational circuits using programmable logic devices. |
| CO4 | Analyse sequential circuits using flip-flops and design the registers & counters. |
| CO5 | Represent a sequential circuit using Finite State machine and apply state minimization techniques to design a FSM |

| **Q.No** | **Question** | **CO** | **BL** |
|---|---|---|---|
| **PART-A** | **Short Answer Question** | | |
| 1. | Compare a) encoder and decoder with neat diagrams.<br>b) multiplexer and demultiplexer with neat diagrams. | CO2 | L2 |
| 2. | Design full adder and full subtractor circuits. | CO2 | L2 |
| **PART-B** | **Long Answer Question** | | |
| 3. | Simplify the following expressions using K-Map and realize the logic circuit.<br>(a)F = πM (1, 2, 3, 8, 9, 10, 11, 14). πd (7,15)<br>(b)F = ∑m (0,2,5,9,15) + ∑d(6,7,8,10,12,13)<br>(c)F = b'+ac'+a'cd | CO2 | L4 |
| 4. | Minimize the following function using tabular method and realize with universal gates.<br>(a)F = ∑m (0,2,5,9,15) + ∑d(6,7,8,10,12,13)<br>(b)F(w,x,y,z)=∑m(0,2,4,6,9,11,13,15,17,21,25,27,29,31) | CO2 | L2 |
| 5. | Design a 4 bit Gray to Binary code converter with circuit diagram. | CO2 | L3 |