Important Questions for MID II

1. Explain the structure of FPGA with neat diagram
2. Write the comparison between CPLD and FPGA.
3. Draw and explain the 3-input LUT. Program the LUT to implement the logic function F=X1X'2X3 where X1 is the MSB.
4. Realize the given logic function using PAL & PLA
   f1 = x1'x2'x3'+x1'x2x3 & f2 = x1'x2'+x1x2x3
5. Convert the T FF to JK FF. JK FF into D FF.
6. List out the classification of shift registers.
7. Design a synchronous MOD-11 up counter using D-flip-flop and explain its operation with a timing diagram.
8. Explain in detail the design and operation of a universal shift register.
9. Compare between the Mealy and Moore models with suitable diagrams.
10. What are the limitations of FSM?
11. Elaborate the steps involved in the design of synchronous sequential circuits.
12. Design an FSM circuit detecting the sequence 0101 using T flip-flop with overlap.