A 98.6 dB SNDR SAR ADC With a Mismatch Error Shaping Technique Implemented With Double Sampling

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***Abstract*—A novel mismatch error shaping (MES) method is proposed in noise-shaping (NS) SAR ADCs to break the SNDR limitation caused by DAC mismatch induced non-linearity. Through sampling the signal twice for one conversion, the input range of the ADC is increased to $2V_{ref}$. After the first sampling, only the MSB is resolved and the results feed back to the opposite side of the DAC. After the second sampling, the MSB result is reversed and a $+V_{ref}/2$ reference is generated at the side of the DAC which has low input while a $-V_{ref}/2$ reference is generated at the other side. Through this method, the dynamic range deduction caused by the MES technique is solved. The proposed SAR ADC is implemented in TSMC 65nm CMOS technology. The simulation results show that the new MES method improves the SFDR from 54 dB to 104.5 dB. The SNDR in 20kHz bandwidth is 98.6dB while power consumption is 513.2μW under a 1 V power supply at 20MS/s sampling rate.**

***Index Terms*—High resolution, high linearity, SAR ADC, noise shaping, mismatch error shaping.**

I. Introduction

AS KNOWN, the non-linearity of SAR ADC is mainly caused by the capacitor mismatch error and incomplete settling of DAC, and the input capacitance of comparator as well as the sampling switches [1], [2]. On the other hand, the incomplete settling error can be solved by providing enough settling time or redundant bit. Thus, it does not bring significant non-linearity in low speed and medium speed ADCs. In addition, the size of the comparator's input transistors and the sampling switches are trade-off with speed, which means the non-linearity due to variation of the parasitic capacitance can be reduced in low speed design. Consequently, the mismatch error of the DAC's capacitor array is the most significant source of the non-linearity [1].

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The calibration techniques are generally used in SAR ADC to reduce the mismatch errors. However, they are limited by the minimum available capacitors [2], [3]. The DWA technique is popular in high resolution DACs. But it cannot be directly employed in SAR ADCs which convert the analog signal to the digital signal one bit by one bit. But the concept of the DWA, which reduces the error through subtracting the error incurred in previous conversion by that in current conversion, can be introduced into the SAR ADC [4]. The MES technique added the previous LSBs signal to the input. During the conversion, error incurred in the present conversion subtracts the error in the previous conversion [1]. Thus, the error is reduced by a high pass filter. Furthermore, the distortion in the output spectrum caused by the mismatch error is reduced by the high pass filter. However, as the previous LSBs signal is added back to the input, the dynamic range is reduced by 6 dB. In this work, the input range is increased by two times through a double sampling scheme in the SAR ADC. Through this way, the flash ADC and the DWA circuit in the traditional design [1] is removed. The [5] solved the dynamic range problem through predicting the MSB and subtracting it after the LSBs reverse. In this work, the MSB is obtained through comparing the differential input with 0 after the first sample, which is more accurate.

II. Introduction of the MES Technique

For the MES technique, the MSB capacitor is used as the reference to define the mismatch of the LSBs capacitors. The LSB of the traditional SAR ADC is $W_0 = \frac{C_0}{C_{tot}}$. However, for a 8-bit ADC with MES technique, the LSB is defined as $W_0 = \frac{C_7}{2^7 C_{tot}}$. And the other LSBs are $W_i = \frac{C_7}{2^{7-i} C_{tot}}$. Consequently, the mismatch of the LSBs to MSB are $e_{i\ MSB} = C_i - \frac{C_7}{2^{7-i}}$, which means the $e_7 = 0$. The input of the ADC after sampling is expressed as

$$V_{IN}(n) = \sum_0^7 D'_i(n) W'_i + Q(n), \tag{1}$$

$$W'_i = W_i + e_i, \tag{2}$$

where the $D'_i(n)$ denotes the digital output when the ADC is affected by the mismatch error, and W'_i is the corresponding analog weights. $Q(n)$ denotes the quantization error. If the $D_i(n)$ represents the ideal output without the mismatch effect,

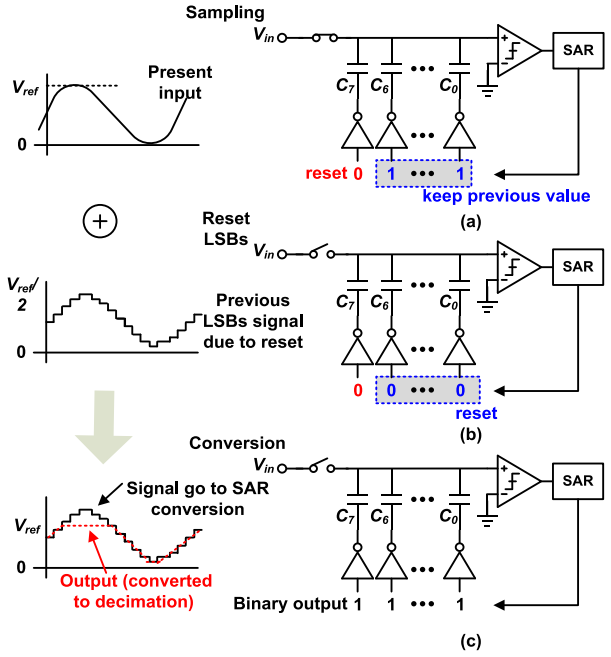


Fig. 1. Operation diagram of SAR ADC with MES: (a) sampling and reset of the MSB, (b) reset of the LSBs, (c) SAR conversion.

then,

$$V_{IN}(n) = D_7(n)W_7 + \sum_0^6 D'_i(n)W_i + \sum_0^6 D'_i(n)e_i + Q(n). \quad (3)$$

The term $\sum_0^6 D'_i(n)e_i$ denotes the conversion errors caused by the mismatch in the DAC, which need to be suppressed to enhance the linearity. If the $\sum_0^6 D'_i(n-1)W'_i$, which includes the error occurred in the previous conversion, is subtracted at both sides of the (3), the following equation can be obtained:

$$\begin{aligned} &V_{IN}(n) - \sum_0^6 D'_i(n-1)W_i - \sum_0^6 D'_i(n-1)e_i \\ &= D_7(n)W_7 + \sum_0^6 D'_i(n)W_i - \sum_0^6 D'_i(n-1)W_i + Q(n) \\ &\quad + \sum_0^6 D'_i(n)e_i - \sum_0^6 D'_i(n-1)e_i. \end{aligned} \quad (4)$$

As shown by the last two terms in (4), the conversion error due to DAC mismatch is reduced to

$$\Delta E = \sum_0^6 D'_i(n)e_i - \sum_0^6 D'_i(n-1)e_i. \quad (5)$$

The operation of the MES technique is depicted in Fig. 1. During the sampling phase, only the MSB is reset while the LSBs remain the previous value (Fig. 1 (a)). After the sampling, the LSBs are reset as shown in Fig. 1 (b), and the previous LSBs signal is added to the input as shown in Fig. 1 (c). Finally, the traditional SAR conversion is conducted. When the input signal is larger than $V_{ref}/2$, its amplitude after adding the previous LSBs is larger than V_{ref}, and the ADC is clipped at the level as shown by the red line which represents the output.

III. Conversion Scheme of a SAR ADC With the Proposed MES Technique

The conventional SAR ADC compares the differential input with 0 for MSB. Then, the output successively approximates to the input through comparing the residue signal for every bit conversion with analog reference $V_{ref}/2$, V_{ref} /4, V_{ref} /8, etc.. When the V_{ip}-V_{in} = V_{ref}, the digital outputs are all 1, and if V_{ip}-V_{in} = -V_{ref}, all the digital outputs are all 0. Thus, the input signal which is beyond the -V_{ref} to + V_{ref} (peak to peak differential) overdrives the ADC. The maximum input of the ADC is limited by the reference voltage of the SAR ADC. As illustrated in Fig. 1, the overdriving will happen when the input of an ADC with MES is higher than $V_{ref}/2$.

To solve this problem, the V_{ref} is subtracted from the differential input before the LSBs conversion. The process of the proposed double input range ADC for MES technique is shown in Fig. 2. Fig. 2(a) shows the 1st sampling of the SAR ADC, during which phase the input of the DAC's MSB is reset, while the LSBs keep previous value. After the first sampling, the LSBs are reset and the MSB conversion is conducted as shown in Fig. 2(b). Then the MSB output arrives the opposite side of the DAC through the reversion block. Thereafter, the ADC performs the second sampling rather than the next bit conversion. At the meantime, the S_{MSB} is turned on, the LSBs return to the previous value and the MSB is stored at the input of the DAC as shown in Fig. 2(c). After the 2nd sampling, and the MSB is reversed as shown in Fig. 2(d). Thus, the high output side of the DAC generates - V_{ref} /2 reference through the charge sharing between the MSB capacitor and the LSBs capacitors. Reversely, the low output side generates + $V_{ref}/2$ in the same method. In this way, the V_{ref} is subtracted from the differential input and the overdriving is avoided. Then, as shown in Fig. 2(e) the S_{MSB} is turned off before the LSBs reset again and the comparison for V_{ip} - V_{in} + $V_{preLSBs}$ to V_{ref} is performed. Next, the conventional SAR conversion is conducted. The input of the comparator is plotted in the Fig. 2(f). Consequently, the MES technique is implemented without any loss of the input range.

From the discussions above, two samplings are required for one conversion. The mismatch error between two samplings could generate distortion in the output spectrum. Thus, oversampling is necessary to decrease the time between the two samplings and thus reduce the error. On the other hand, the oversampling is also required by the NS technique and MES technique. Thus, this double input range ADC is feasible. To quantitatively analyze the influence of the mismatch error caused by double samplings, the output SNR is calculated. The mismatch between two samplings is derived for a sinusoid input signal $v(t) = A_0 sin(2\pi ft)$.

The derivative of the $v(t)$ with respect to t is expressed as:

$$\frac{dv}{dt}|_{rms} = \frac{A_0 2\pi f}{\sqrt{2}}. \quad (6)$$

Thus, the mismatch between the two samplings can be expressed as:

$$\Delta V_{rms} = \frac{A_0 2\pi f \Delta t}{\sqrt{2}}. \quad (7)$$

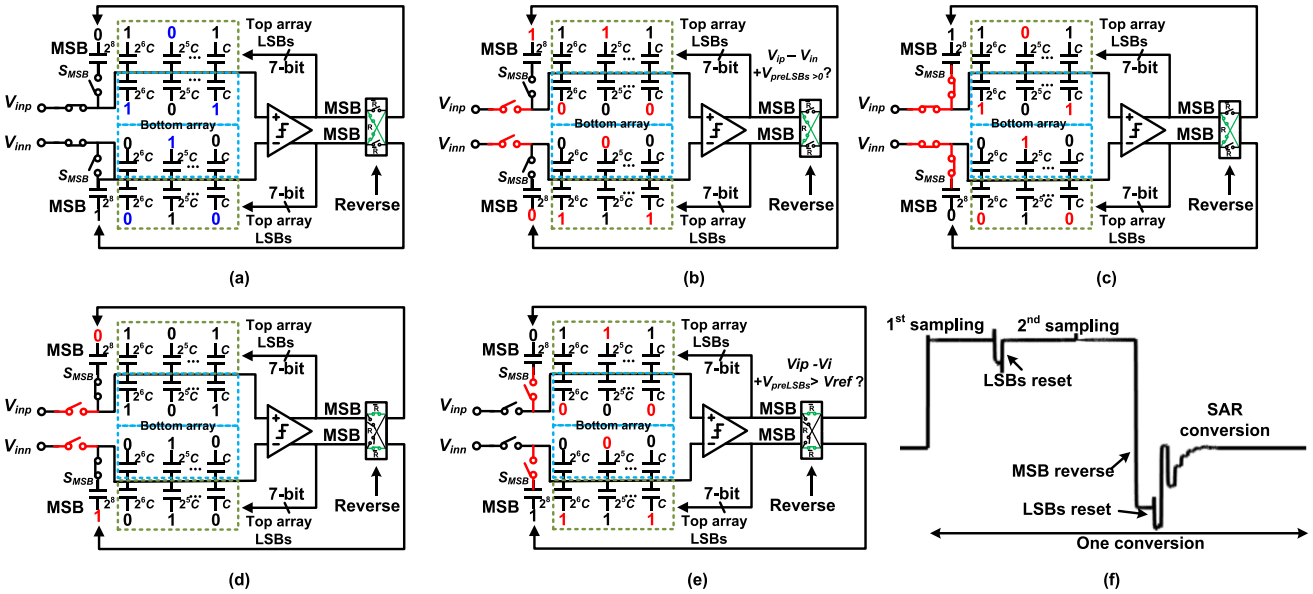


Fig. 2. Operation process of the double input range ADC with MES technique: (a) 1st sampling, (b) reset of the LSBs and MSB conversion, (c) 2nd sampling of the ADC, (d) reverse of the MSB output, (e) LSBs reset, and (f) differential input of the comparator.

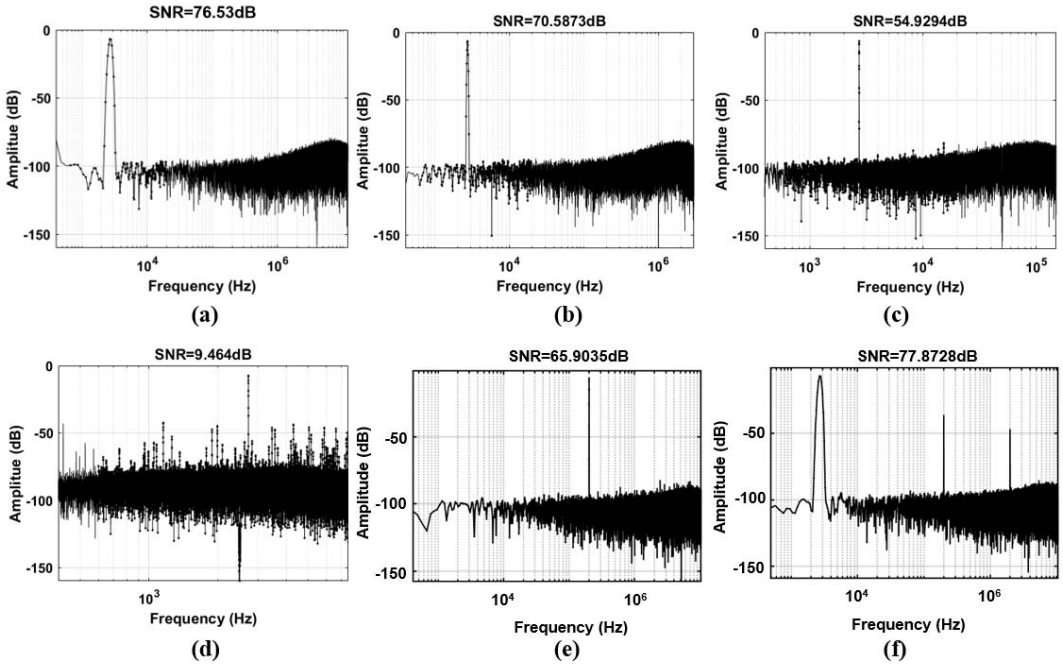


Fig. 3. The output spectrum when the input frequency is 2.73kHz and bandwidth is 20kHz with (a) 20MSps sampling rate, (b) 5MSps sampling rate, (c) 0.25MSps sampling rate, (d) 0.125MSps sampling rate, when the sampling rate fixed at 20MSps sampling rate (e) input frequency is 200kHz, and (f) input 2.3kHz signal with −30dBFS 200kHz and −40dBFS 2MHz interferences.

Furthermore, for a specified SNR, the frequency limitation caused by the double sampling can be calculated as:

$$f < \frac{10^{\left(\frac{SNR}{-20}\right)}}{2\pi\,\Delta t}. \tag{8}$$

A behavior model for the double input range ADC is built. The simulation results of the double input range ADC with different oversampling ratio are shown in Fig. 3. The Fig. 3(a) shows the spectrum when the sampling rate is 20 MSps and the input frequency is 2.73 kHz. The calculated output SNR in 20kHz bandwidth is $6.02\times8+10\log10(F_s/2BW)$ = 76.9 dB. Thus, the mismatch error caused by the double sampling does not deteriorate the SNR. The sampling rate in Fig. 3(b) and Fig. 3(c) are 5MSps and 0.25MSps respectively. The corresponding output SNR should be 70.9 dB and 57.8 dB respectively. Thus, when the sampling rate is lower than 0.25 MSps, the output SNR is reduced by the gap between two samplings. When the sampling rate reduces to 12.5kSps, the output spectrum is seriously flawed as shown in Fig. 3(d). Considering the high frequency

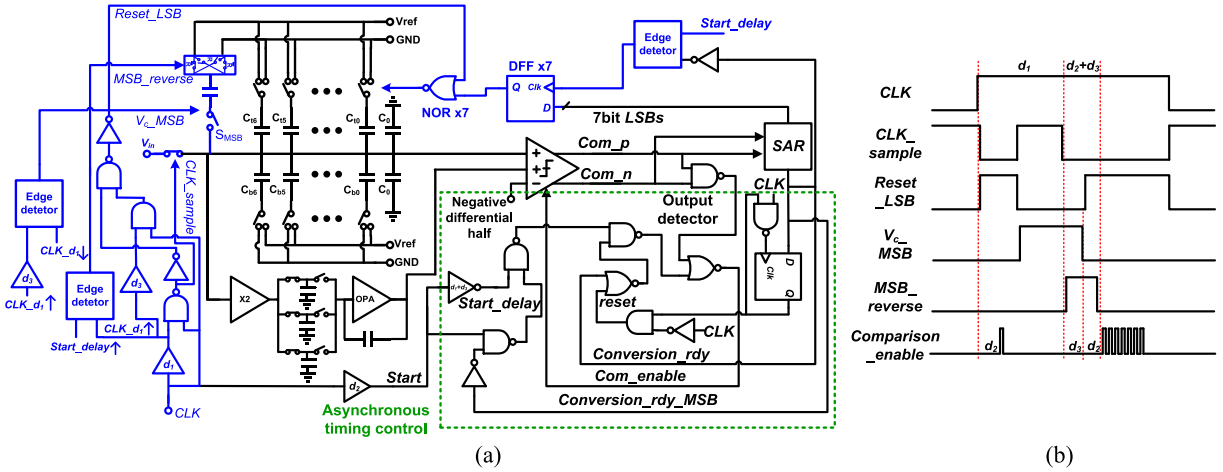


Fig. 4. (a) Architecture of the NS-SAR ADC with the new MES and (b) timing sequence of the ADC.

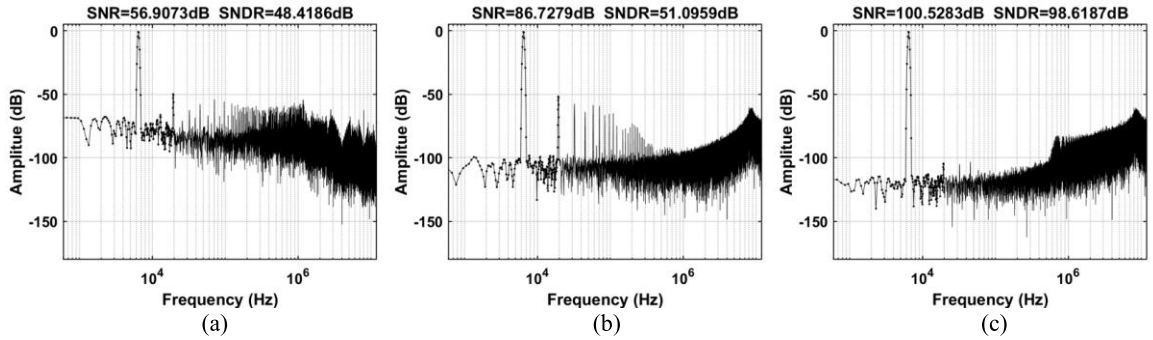


Fig. 5. Output spectrum of the ADC (a) without the MES and NS, (b) with the NS but without MES, (c) with MES and NS.

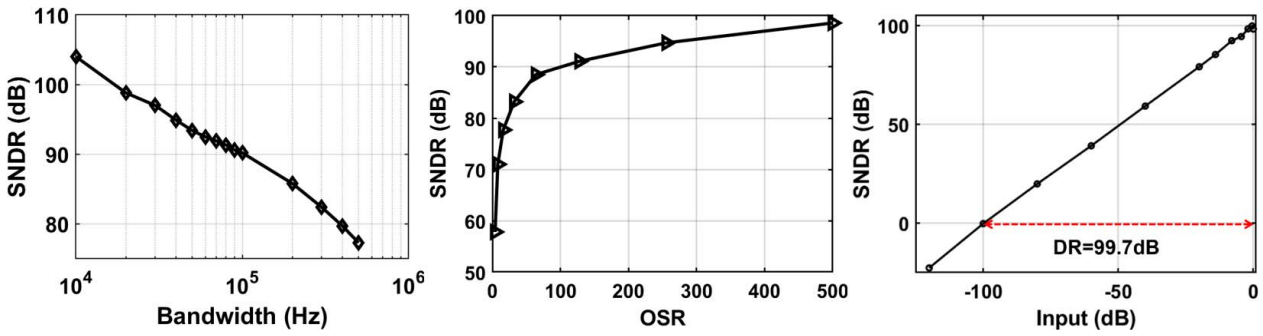
interferences, high frequency (200kHz) input is added into the model as shown in Fig. 3(e). When the sampling rate is 20MSps, the SNR in 200kHz bandwidth is not degraded. The interference of 200kHz (−30dBFS) and 2MHz (−40dBFS) are added to the 2.3kHz input. The output spectrum as shown in Fig. 3(f) proves that, the high amplitude interferences will not impact the SNR in 20kHz bandwidth. The bump at high frequency is caused by dithering inserted in the model which is used to randomize the quantization noise.

The double input range ADC can compensate the input range reduction caused by MES technique. For this, an 8-bit NS SAR ADC with asynchronous timing scheme [6] is implemented. In addition, to save switching energy and keep the input common-mode voltage of comparator unchanged, the split capacitor array is employed.

IV. MES Technique Based on the Double Input Range ADC

The completed architecture of the SAR ADC with the proposed MES technique and NS technique is shown in Fig. 4(a). The circuits in blue generate the logic signals for the MES. The timing sequence of the ADC is shown in Fig. 4(b). The sampling switches are enabled twice by *CLK_sample* which is generated by a delay cell (d_1) and a NAND gate. The delay time can be adjusted by 2-bit control signal to reduce effect caused by PVT variation. The LSBs are first reset by the *Reset_LSB* starting after the first sampling. Subsequently, after a time delay of d_2, the MSB conversion is conducted when the *Start* signal comes, and the result is fed into the DAC's input. Noted, there is no charge transfer in MSB capacitor as the S_{MSB} is off in this phase. Although the DAC's LSBs are reset, the previous LSBs are stored in the memory cell implemented by 7 DFFs for the second reset. The V_c*_MSB,* which is used to control the S_{MSB}, is generated through detecting the falling edge of the *CLK*_d_1 and the rising edge of the signal which is produced through delaying the *CLK*_d_1 by d_3. During the second sampling, the S_{MSB} is turned on and the LSBs are turned back to the previous values. Then the MSB input of the DAC is reversed by the *MSB_reverse* signal after the second sampling. The *MSB_reverse* is generated through detecting the rising edge of the *CLK*_d_1 and *Start_delay*. Next, V_c*_MSB* is turned off and the second reset of the LSBs is conducted. Subsequently, the 2nd MSB can be resolved through comparing the input signal with V_{ref}. Finally, the remaining LSBs are converted through the traditional SAR ADC schemes. After the LSB conversion, the residue signal is fed into the FIR-IIR filter where the NS is performed.

The LSBs are reset and the MSB is converted during the Δt which is between the end of the first sampling and start of the second sampling. Thus, the Δt includes the settling time of the LSBs' reset and one comparison time of the comparator, which is about 4.2ns in this design. As the mismatch in Δt may affect the SNR, high speed buffer and comparator are required.



(a) (b) (c)

Fig. 6. SNDR versus the (a) bandwidth and (b) OSR, and (c) dynamic range of the ADC with the proposed MES scheme.

However, high speed means high power consumption. Thus, there is a trade-off between the SNR and power consumption.

The noise shaping technique is employed in the ADC to increase the output SNR. A first order FIR-IIR filter based on switched capacitor circuits is implemented. As the NS technique cannot reduce the noise of the FIRIIR filter, the chopper is used in the buffer of the FIR filter and the amplifier in the IIR filter. The chopper frequency is 10MHz to ensure the in-band noise is ignorable. The output of the FIRIIR filter is added to the input through the comparator in the SAR ADC.

V. Simulation Results

The SAR ADC with the proposed MES technique is developed in TSMC 65 nm CMOS process. The simulation results are shown in Fig. 5. The input signal is 2 V (peak to peak, differential) with 6.4 kHz frequency. The ADC works at 20MSps sampling. The FFT used 20M data points. The quantization noise is shaped by the NS technique and thus the SNR is improved. To avoid the SNR limitation brought by noise during sampling, 1.28 pF sampling capacitor is used in the ADC. Thus, the LSB capacitor is 2.5 fF. Fig. 5(a) shows that the output without MES and NS. While the Fig. 5(b) shows the output spectrum without the MES but with NS, the SFDR is restrained to 54 dB by the mismatch error. In contrast, the SFDR is improved to 104.5 dB as shown in Fig. 5(c) after enabling the MES. These results demonstrate that, the MES technique based on the double input range ADC can reduce the distortions caused by mismatch error in DAC. In addition, the flash ADC and DWA digital circuits in [1] are not required. The SNDR versus the bandwidth is shown in Fig. 6(a), the SNDR at 500kHz is still about 80dB which is corresponding to 13bit ENOB. Fig. 6(b) shows the SNDR degradation with the decrease of the OSR. When the OSR is lower than 32, the SNDR is reduced due to the double sampling error. The dynamic range plot is shown in Fig. 6(c). The SAR ADC with the proposed MES schemes achieves about 99.7dB DR. The comparison with the state-of-the-art work is shown in Table I, where the SFDR is pretty competitive through employing the proposed MES method, and the *FoM* is comparable with the highest one.

TABLE I
Comparison of the Performance With the State-of-the-Art Works

	This work	ISSCC 2016 [1]	ISSCC 2020 [5]	ISSCC 2018 [7]	JSSC 2015 [8]	ASSCC 2011 [9]
Architecture	**NS-SAR with MES**	NS-SAR with MES	NS-SAR with 2nd MES	Incremental ΔΣ ADC	2-step Incremental ΔΣ ADC	Hybrid ΔΣ ADC
Technology	**65nm**	55nm	40nm	180nm	65nm	40nm
Supply voltage(V)	**1**	1.2	1.1	1.8	1.2	2.5/1.2
Sampling Rate	**20MSps**	1MSps	2MSps	30MSps	96kSps	6.5MSps
BW(Hz)	**20k**	1k	40k	100k	0.25k	24k
SNDR(dB)	**98.6**	101	90.5	86.6	90.8	90
SNR(dB)	**100.5**	104	90.9	87.3	100	90.7
SFDR(dB)	**104.5**	105.1	102.2	101.3	--	102
Power (W)	**513.2μ**	15.7μ	67.4	1098 μ	10.7 μ	500 μ
Active area (mm^2)	**0.097**	0.072	0.061	0.36	0.2	0.05
*FoMs** (dB)	**174.5**	178.9	182	166.2	164.5	166.8

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