A CMOS 8-Bit High-Speed A/D Converter IC

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Abstract—**A novel high-speed low-power CMOS balanced comparator circuit is proposed and implemented in an 8-bit fully parallel analog-to-digital (A/D) converter IC. A 20-MHz sampling rate with 350-mW power dissipation from a single 5-V power supply has been realized. Integral linearity of $\pm 1/2$ LSB to 8-bit conversion has been achieved through intensive transistor dimension optimization applied to the comparator circuit, instead of employing an offset canceling technique.**

I. Introduction

DEMANDS for a low-cost low-power high-speed analog-to-digital (A/D) converter are increasing rapidly in video applications. It is essential that the converter power consumption should be small, to obviate the necessity for forced cooling, and costs should be low for most applications. There are several bipolar products [1] commercially available, though none of them seems to satisfy these requirements. A combination of fully parallel A/D conversion technique and CMOS processing appears to be the potentially best combination to satisfy the requirements [2]. The MOS process has a potential advantage in regard to excellent producibility. Though MOS technology has less precision than bipolar technology, recent IC process innovation is now reaching sufficient precision for use in developing a flash A/D converter having video speed and up to around 8-bit accuracy without any offset cancelling technique. The key element to realize the IC is the comparator circuit, which is 2^N in number for N-bit conversion. A flash 8-bit A/D converter integrated circuit has been realized through the use of a high-speed low-power CMOS balanced comparator. An accuracy of $\pm 1/2$ LSB has been obtained through intensive transistor dimensions optimization instead of employing offset canceling techniques. The device showed low-power and high-speed performance applicable to video signal A/D conversion.

II. Comparator Circuit

The key in realizing a flash A/D converter is achieving a low-power high-speed and low-offset comparator circuit. Offset canceling is a popular technique in analog MOS circuits. However, if the time slot for comparison differs from the time slot for offset storage in an offset canceling technique, the stored offset voltage at the offset storage interval is not expected to be the same at the time slot for comparison. This may cause a large noise in the converted signal in a noisy environment, as in a flash A/D converter. Offset caused by switch feedthrough is also inevitable in this technique.

A standard deviation for each comparator offset voltage is the most important aspect to attain required accuracy for a flash A/D converter. Instead of employing offset canceling, a standard deviation of the offset voltage has been designed at less than one third of the A/D converter minimum resolution for ± 1 LSB accuracy, through a newly designed circuit configuration and intensive transistor dimensions optimization.

The comparator circuit proposed consists of a differential amplifier and a novel CMOS latch circuit, as is shown in Fig. 1. The differential amplifier with p-channel input transistors increases the input voltage range to the V_{ss} level, protects signals from noise sources, such as crosstalk or interference from power supply lines, and decreases feedthrough from the latch stage to the reference voltage network. Swing clipping transistors D_1 and D_2 in the amplifier assist the input signal tracking capability and decrease feedthrough from the amplified input signal to the reference resistor network. The amplified difference signal is fed to the discharge current controlling transistors connected to each drain in the n-channel flip-flop in the latch stage. The latch stage consists of discharge transistors, an n-channel flip-flop with a pair of n-channel transfer gates for strobing, p-channel flip-flop, and p-channel precharge transistors. Advantages for a flip-flop strobed at drain node over a flip-flop strobed at source node exist in regard to regeneration speed and offset. Since carier mobility is nearly twice faster at zero substrate bias than at a few volt substrate bias condition, regeneration speed for the flip-flop is faster for the drain strobing scheme. In addition, since strobing transistors isolate the flip-flop from output nodes and work as the load device for the flip-flop, load capacitances become only the gate capacitance of the flip-flop itself. Offset voltage caused by a channel-length fluctuation, which is estimated as the main source of the total offset voltage, is much lower at zero volt substrate bias. Therefore, transistor channel lengths can be decreased and

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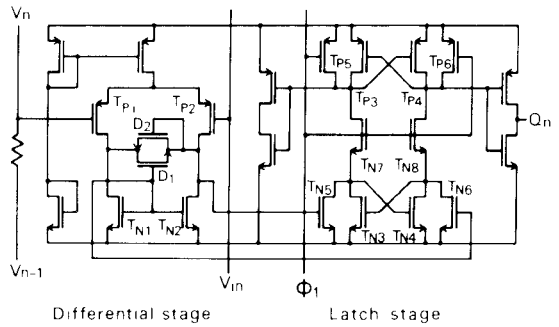

Fig. 1. Comparator circuit diagram.

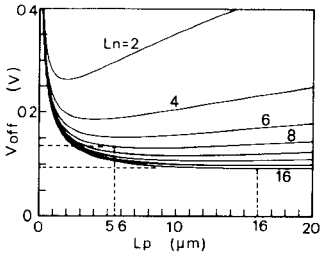

Fig. 2. Offset voltage dependence on channel-length unbalance as a function of p-channel driver transistor. Parameter is n-channel load transistor channel length. Unbalance is normalized to 1 μm.

the flip-flop speed can be made faster, as a result. An inverter buffer is connected to both output nodes of the p-channel flip-flop to give the same loading effect to the flip-flop.

As the MOS transistor dimensions decrease, long-term stability has to be considered, especially for analog components. An instability caused by hot carriers may have to be considered. However, since the differential amplifier has a p-channel input transistor configuration, which is more stable to voltage stress than an n-channel input transistor configuration, and since voltage stress at each node for the differential amplifier is limited to less than 3 V, accuracy degradation would be expected to be small, due to the surface state density fluctuation, generated by hot carriers in this stage. Therefore, further scaling would be applicable without sacrificing stability.

The dynamic operation of this circuit is divided into reset interval and comparison interval. At the reset interval, ϕ_1 is low, transfer gates T_{N7} and T_{N8} are "off" and p-channel precharge transistors T_{P5} and T_{P6} are "on". Therefore, both the p-channel flip-flop nodes, formed by T_{P3} and T_{P4}, are charged up to power supply voltage level, and n-channel flip-flop nodes, formed by T_{N3} and T_{N4}, are discharged to ground level through n-channel discharge transistors. When ϕ_1 goes high, charging current starts to flow from the p-channel side to the n-channel flip-flop. A part of the current is discharged through discharge transistors T_{N5} and T_{N6}, whose gates are controlled by the differential amplifier. Since current values differ between two discharge transistors, a large voltage difference is obtained when the n-channel flip-flop drain voltages exceed the threshold voltage. The voltage difference is amplified quickly after the flip-flop reaches more than unity gain. The amplified difference is transferred through the transfer gates, which operate as grounded gate configurations, to the p-channel flip-flop, and are amplified to a voltage swing nearly equal to the power supply voltages.

III. Comparator Design Constraints

There are two constraints to the comparator circuit. One is common mode input voltage range. The other is the comparator offset voltage distribution.

Common mode input voltage range, for the power applied to a differential amplifier, can be derived from the fact that each transistor in the amplifier works in the saturation region. The range can be written as

$$V_{Tn} + V_{Tp} + \sqrt{2I_o/K_n} < V_i < V_{dd} + V_{Tp} - \sqrt{2I_o/K_p} - \sqrt{4I_o/K_{ps}} \quad (1)$$

where V_{Tn}, V_{Tp}, I_o, K_n, K_p, and K_{ps} denote n-channel transistor threshold voltage, p-channel transistor threshold voltage, current flow in each half-amplifier circuit, n-channel transistor device constant, p-channel transistor device constant, and p-channel current source device constant, respectively. The n-channel transistor threshold voltages employeed here have been designed smaller than that employed in the logic portion, to extend the common mode input voltage range to analog ground potential.

Since the offset voltage in the latch stage is divided by the differential amplifier gain, which is about 40 in this case, as in the input offset voltage, most of the offset sources are in the differential stage. There are two kinds of offset sources in an MOS differential amplifier. They are charge density fluctuation, such as surface states and impurity doping concentration, and dimension fluctuation. Assuming a differential amplifier with p-channel driver transistor and n-channel load transistors, offset voltage can be written as

$$V_{\text{off}} = D * (1/L_n + 1/L_p)\sqrt{I_o/2K_p} + VT_p + \sqrt{K_n/K_p}VT_n \quad (2)$$

where D denotes channel-length imbalance between transistor pairs, for both p-channel and n-channel. The first term comes from dimension fluctuation. The second and third terms come from charge fluctuation. Since surface state density and impurity concentration can be controlled well, and since the last two terms are proportional to gate oxide thickness, these terms would be expected to decrease as the oxide thickness was decreased in the future. However, the first term is increased in inverse proportion to channel lengths, according to a constant field scaling. Therefore, the first term was assumed dominant for the comparator design.

The offset voltage dependence on channel length fluctuates as a function on p-channel driver transistor is shown in Fig. 2. The fluctuation value is normalized by 1 μm. The parameter is n-channel load channel length. Each curve has a minimum at the point where both driver and

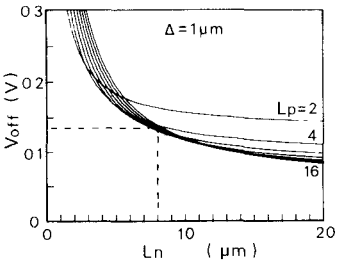

Fig. 3. Offset voltage dependence on channel-length unbalance as n-channel load transistor function. Parameter is p-channel driver transistor channel length. Unbalance is normalized to 1 μm.

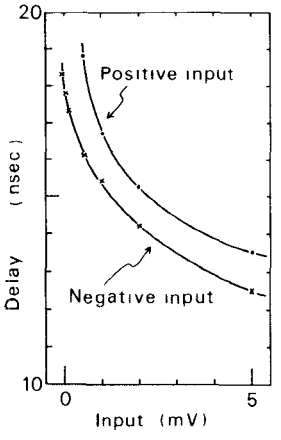

Fig. 4. Simulated comparator sensitivity.

load transistor channel lengths are the same. In these curves, threshold change due to channel-length fluctuation is excluded. This effect is negligible for a more than 5-μm channel length. Actual channel-length imbalance was estimated by test amplifier measurements. Around 2-mV offset has been observed as a standard deviation as a result of measurements on long-channel amplifiers. A systematic offset has not been considered for the comparator. If the channel length is assumed to be 16 μm, the fluctuation is expected to be about 600 Å between a pair of transistors. To realize an A/D converter with 10-mV accuracy, about 3-mV offset is allowed as the standard deviation. The 5.6-μm effective channel length was employed for the p-channel drived transistors.

An offset voltage dependence on channel lengths fluctuation as a function of n-channel load transistors is shown in Fig. 3. The fluctuation value is also normalized by 1 μm. The curves increase monotonically as the n-channel transistor channel length is decreased. The curves start to increase quickly from around 8 μm. The n-channel load transistor channel length was designed at 8 μm in the present comparator. The amplifier has about 5-MHz full gain bandwidth, according to a SPICE simulation.

A simulated sensitivity curve for the comparator is plotted in Fig. 4. The delay time was defined as the time required from the beginning of a strobe pulse rise to the time when one of the inverter buffer outputs crosses 2.5 V. The strobe pulse was 5 V at 7-ns rise time. The positive input in the figure is for positive input voltage referred to reference input node. A systematic offset voltage of about -0.2 mV is expected, due to the feedthrough from the

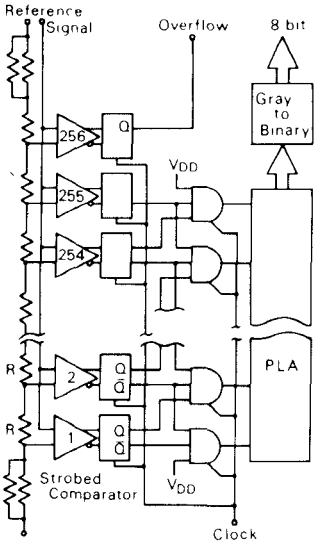

Fig. 5. A/D converter block diagram.

latch stage to the unbalanced differential amplifier output impedance. The time required to return the latch stage to the initial condition is about 10 ns.

The voltage applied between individual nodes in the transistors, whose parameters affect analog performances, is less than 3 V, which is the bandgap between Si and oxide. Therefore, little hot carrier instability would be expected and further shrinking would be deemed applicable to channel length, channel width, and gate oxide thickness without any trouble.

IV. A/D Converter Structure

Device block structure is similar to structures previously reported [2], [3], as shown in Fig. 5. The converter basically consists of 259 identical resistors made as a diffused layer, 256 comparators, 255 AND gates, and PLA, a gray code to binary code conversion logic circuit, and nine output latches. 255 of the resistors are connected in series. Two resistors are connected in parallel and connected at both ends of the series resistor array. The resistance of each resistor was 10 Ω. This array generates equally spaced reference voltages. Individual voltages are fed to each comparator. 255 comparators handle 8-bit resolution and one handles overflow detection.

The results compared for each comparator are transferred to AND gates. There, a transition point from logical "0" to "1" is detected by three adjacent comparator products. The transition information, obtained at 255 AND gates, is converted to an 8-bit gray code by the PLA. When PLA latches the data from the AND gates at transition, there are possibilities that two successive AND gates would give logical 1 level. Therefore, gray code is employed to eliminate large code jump in this condition. Code conversion logic, from the gray code to binary code, consisting of seven EX–OR units, is placed in between master and slave output latches.

The chip photo is shown in Fig. 6. The 256 comparators are divided into eight rows. Each row has a clock driver on

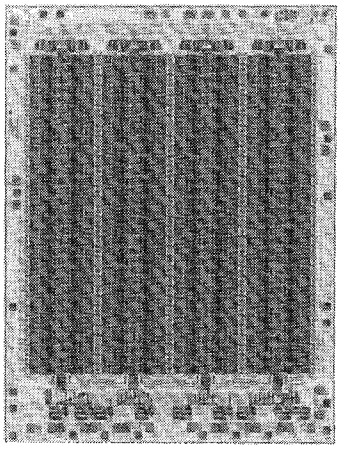

Fig. 6. Chip photomicrograph.

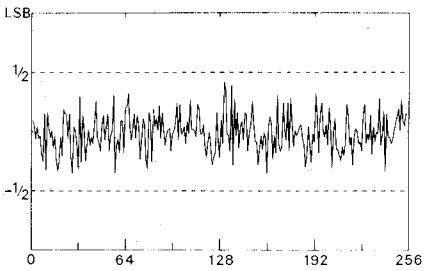

Fig. 7. Integral linearity: V – ref = 3.8 V, 15-MHz clock.

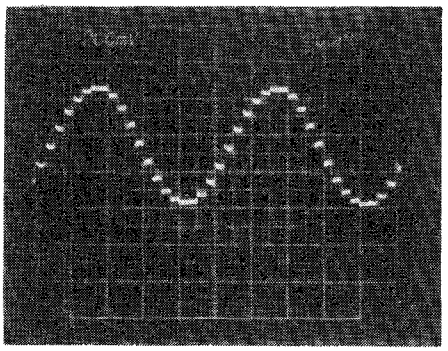

Fig. 8. Regenerated 1-MHz sine wave at 20-MHz clock.

top of the layout. The PLA AND array is divided into four blocks. Each of the four PLA AND arrays covers 64 selector outputs, and the product is transferred to an OR array.

The converter was fabricated using a p-well bulk CMOS process with 3.5-μm minimum mask channel length for the digital portion of both n- and p-channel transistors.

V. Results

Linearity to a slowly changing input is shown in Fig. 7. A 15-MHz clock frequency was employed in this measurement. Reference voltage was 3.84 V. Therefore, step voltage was 15 mV. The integral linearity was within $\pm 1/2$ LSB. The measured offset voltage was typically -0.15 mV on an average and standard deviation was 2.4 mV to each comparator making up the converter.

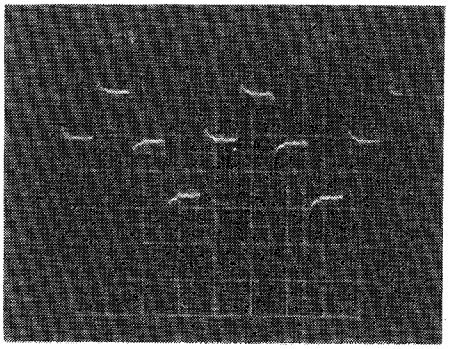

Fig. 9. Regenerated 5-MHZ sine wave at 20-MHz clock.

TABLE I
A/D Converter Charateristics

Supplying power voltage	5 V
Power dissipation	350mW (Clock 20MHz)
Max.operating rate	>20MHz
Input voltage range	0-3.9V
Resolution	8-bit
Linearity	±1/2LSB (3.84V reference)
Signal bandwidth	5 MHz
Signal input impedance	70 pF
Input/Output levels	TTL compatible
Chip size	4.8mm X 6.3mm
Package	24pin DIP

Regenerated sine-wave signals coded by the A/D converter, are shown in Figs. 8 and 9. The clock for both was 20 MHz. The sine-wave frequency was 1 MHz for Fig. 8 and 5 MHz for Fig. 9, respectively.

Differential gain (DG) and differential phase (DP) characteristics were measured using at NTSC color test signal. Typical 3-percent DG and 2° DP results were measured. These values were satisfactory for most video applications.

Performances are summarized in Table I. Chip size is 4.8 mm $\times$ 6.3 mm.

VI. Conclusion

A high-speed low-power compact CMOS comparator circuit is proposed and implemented to an 8-bit fully parallel A/D converter IC. Less than 3-mV offset as a standard deviation has been obtained, as was expected, without any offset canceling technique. The converter handled 20 M sample/s with 350-mW power dissipation from a 5-V single power supply and less than $\pm 1/2$ LSB linearity. The IC was fabricated using 3.5-μm rule lithography. The voltage applied to each analog transistor is less than 3 V. Although the technology employed was not sufficient for $\pm 1/2$ LSB accuracy, the performance would be expected to be improved further, if 2 μm or less projection lithography become available.

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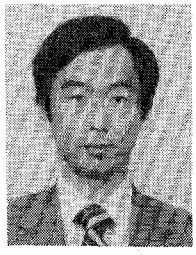

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