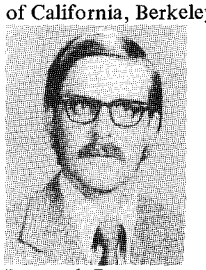
for their prompt, thorough, and competent criticism. The combination of these efforts has resulted in what I believe to be a very interesting issue.

GARY L. BALDWIN
Guest Editor



Gary L. Baldwin (M'66) was born in El Centro, Calif., on October 12, 1943. He received the B.S., M.S., and Ph.D. degrees in electrical engineering in 1966, 1967, and 1970, respectively, all from the University of California, Berkeley.

He was employed by the IBM Corporation, San Jose, Calif., on a work-study program from 1963 to 1966. In the summer of 1968 he was involved in linear integrated circuit design with the Advanced Circuits Research Group, Signetics Corporation, Sunnyvale, Calif. He was an Acting Assistant Professor of Electrical Engineering at the University of California, Berkeley, during 1969 and 1970. He is now a member of the Technical Staff in the Systems Elements Research Department, Bell Laboratories, Holmdel, N.J.

Dr. Baldwin is a member of Eta Kappa Nu and Sigma Xi.

All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques—Part I

JAMES L. McCREARY, STUDENT MEMBER, IEEE, AND PAUL R. GRAY, MEMBER, IEEE

Abstract—**This two-part paper describes two different techniques for performing analog-to-digital (A/D) conversion compatibly with standard single-channel MOS technology. In the first paper, the use of a binary weighted capacitor array to perform a high-speed, successive approximation conversion is discussed. The technique provides an inherent sample/hold function and can accept both polarities of inputs with a single positive reference. The factors limiting the accuracy and conversion rate of the technique are considered analytically. Experimental results from a monolithic prototype are presented; a resolution of 10 bits was achieved with a conversion time of 23 μs. The estimated die size for a completely monolithic version is 8000 mil^2.**

The second paper [3] describes a two-capacitor successive approximation technique, which, in contrast to the first, requires considerably less die area, is inherently monotonic in the presence of capacitor ratio errors, and which operates at a somewhat lower conversion rate. Factors affecting accuracy and conversion rate are considered analytically. Experimental results from a monolithic prototype are presented; a resolution of 8 bits was achieved with an A/D conversion time of 100 μs. Used as a D/A converter, a settling time of 13.5 μs was achieved. The estimated total die size for a completely monolithic version including logic is 5000 mil^2.

I. INTRODUCTION

MOST conventional techniques for analog-to-digital (A/D) conversion require both high-performance analog circuitry, such as operational amplifiers, and digital circuitry for counting, sequencing, and data storage. This has tended to result in hybrid circuits consisting of one or more bipolar analog chips and an MOS chip to economically perform the digital functions [1]. This paper describes a new, all-MOS technique which is realizable in a single chip and performs a 10-bit conversion in 23 μs [6]. It includes an intrinsic sample-and-hold function, accepts both bipolar and unipolar inputs, and is realizable with standard N-channel metal gate technology.

For the realization of a fast, successive-approximation A/D converter in MOS technology, conventional voltage driven R-$2R$ techniques are cumbersome since diffused resistors of proper sheet resistance are not available in the standard single-channel technology. A complex thin-film process must be used. Furthermore, these approaches require careful control of the "ON" resistance ratios in the MOS switches over a wide range of values.

In contrast to its utilization as a current switch, the MOS device, used as a charge switch, has inherently zero offset voltage and as an amplifier has very high input resistance. In addition, capacitors are easily fabricated in metal gate technology. Therefore, one is led to use capacitors rather than resistors as the precision components, and to use charge rather than current as the working medium. This technique, referred to as charge-redistribution, has been used in some discrete component A/D converters for many years [2], [7]. However, these converters have required high-performance operational amplifiers which are difficult to realize in single-channel MOS technology.

This paper describes a new A/D conversion technique using charge redistribution on weighted capacitors, while a companion paper [3] describes another application of the charge redistribution concept using two equal capacitors. In Section II of this paper, the binary-weighted capacitor capacitor array and its operation is described. In Sections III and IV, the limitations on the speed and resolution are analyzed. Ex-

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The authors are with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, Calif. 94720.

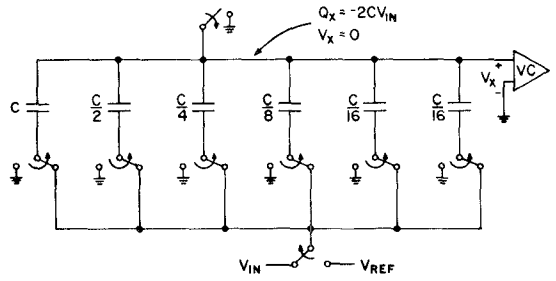

Fig. 1. Conceptual 5-bit A/D converter illustrating the sample mode operation.

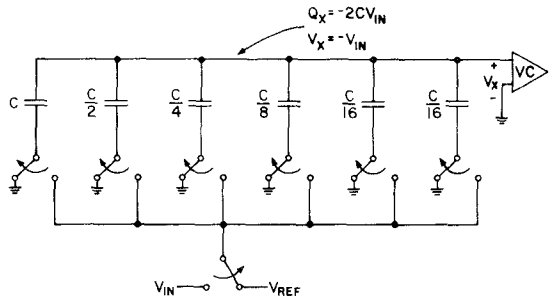

Fig. 2. Pre-redistribution hold mode operation.

perimental results from a prototype system are presented in Section V.

II. Charge Redistribution A/D Conversion Technique Using Binary Weighted Capacitors

The new A/D conversion technique is illustrated with a conceptual 5-bit version of the converter shown in Fig. 1. It consists of a comparator, an array of binary weighted capacitors plus one additional capacitor of weight corresponding to the least significant bit (LSB), and switches which connect the plates to certain voltages. A conversion is accomplished by a sequence of three operations. In the first, the "sample mode" (Fig. 1), the top plate is connected to ground and the bottom plates to the input voltage. This results in a stored charge on the top plate which is proportional to the input voltage V_{in}. In the "hold mode" of Fig. 2, the top grounding switch is then opened, and the bottom plates are connected to ground. Since the charge on the top plate is conserved, its potential goes to $-V_{in}$. The "redistribution mode," shown in Fig. 3, begins by testing the value of the most significant bit (MSB). This is done by raising the bottom plate of the largest capacitor to the reference voltage V_{ref}. The equivalent circuit is now actually a voltage divider between two equal capacitances. The voltage V_x, which was equal to $-V_{in}$ previously, is now increased by $\frac{1}{2}$ the reference as a result of this operation.

$$V_x = -V_{in} + \frac{V_{ref}}{2}.$$

Sensing the sign of V_x, the comparator output is a logic '1' if $V_x < 0$ and is a '0' if $V_x > 0$. This is analogous to the interpretation that

$$\text{if } V_x < 0 \quad \text{then } V_{in} > \frac{V_{ref}}{2};$$

hence the MSB = 1; but

$$\text{if } V_x > 0 \quad \text{then } V_{in} < \frac{V_{ref}}{2};$$

therefore the MSB = 0. The output of the comparator is, therefore, the value of the binary bit being tested. Switch $S1$ is returned to ground only if the MSB b_4 is a zero. In a similar manner, the next MSB is determined by raising the bottom plate of the next largest capacitor to V_{ref} and checking the polarity of the resulting value of V_x. In this case, however,

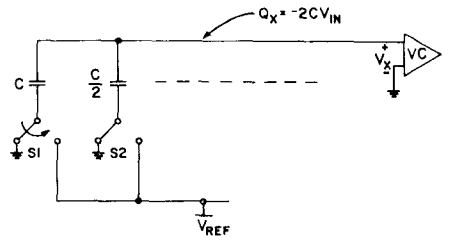

Fig. 3. Redistribution mode operation.

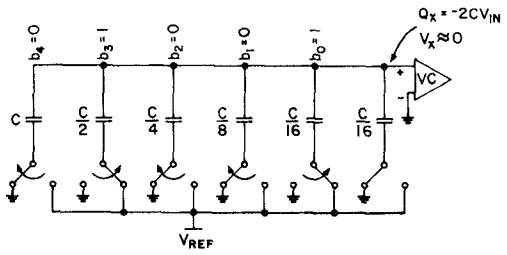

Fig. 4. Example of a final configuration.

the voltage division property of the array causes $V_{ref}/4$ to be added to V_x:

$$V_x = -V_{in} + b_4 \frac{V_{ref}}{2} + \frac{V_{ref}}{4}.$$

Conversion proceeds in this manner until all the bits have been determined. A final configuration is illustrated in Fig. 4 for the digital output 01001. Notice that all capacitors corresponding to a '0' bit are completely discharged. The total original charge on the top plates has been redistributed in a binary fashion and now resides only on the capacitors corresponding to a '1' bit. N redistributions are required for a conversion resolution of N bits. In contrast to earlier charge redistribution techniques, the capacitance of the lower plate switch does not affect the accuracy of the conversion [4]. This fact is evident since the switch capacitance is either discharged to ground or is charged by V_{ref} but never absorbs charge from the top plate. Therefore, the switch devices can be quite large permitting rapid redistributions. On the other hand, the top plate of the array is connected to all the capacitors and to a switch and to the comparator resulting in a large

parasitic capacitance from the top plate to ground. The nature of the conversion process, however, is such that V_x is converged back towards zero—its initial value. Hence, the charge on this parasitic is the same in the final configuration as it was in the sample mode. Therefore, the error charge contributed by this parasitic is very near zero. For the 10-bit converter the parasitic capacitance at the top plate can be 100 times the value of the smallest capacitor and still cause only 0.1 bit offset error. This is equivalent to saying that the smallest capacitor may be much smaller than the parasitic and consequently the largest capacitor may be reduced in value proportionally. Furthermore, the initial value of V_x need not necessarily be zero but can be the threshold voltage of the comparator. This fact allows cancellation of comparator offset by storing the offset in the array during the sample mode. The linearity then is primarily a function of the ratio accuracy of the capacitors in the array.

By only a slight modification of the array switching scheme bipolar voltage inputs can be encoded while still using only the single positive reference. This is achieved by connecting the bottom plate of the largest capacitor to V_{ref} during the sample mode resulting in a stored charge:

$$Q_x = -C_{TOT}\left(\frac{V_{\text{in}}}{2} + \frac{V_{\text{ref}}}{2}\right).$$

Each bit is then tested in sequence just as before except that the largest capacitor is switched from V_{ref} to ground during its test, while all the other capacitors are switched from ground to V_{ref}. Also, as before, a bit value is true if V_x is negative after the test. The expression for V_x again converges back towards zero:

$$V_x = -\frac{V_{\text{in}}}{2} + V_{\text{ref}}\left(-\frac{b_{10}}{2^1} + \frac{b_9}{2^2} + \frac{b_8}{2^3} + \cdots + \frac{b_1}{2^{10}}\right) \approx 0.$$

For a 10-V reference, b_{10} is '0' for $0 \leqslant V_{\text{in}} \leqslant 10$ V, but is '1' for -10 V $\leqslant V_{\text{in}} < 0$. Therefore, b_{10} represents the sign bit and its function is to level shift V_x in order to accommodate negative inputs. Hence, a 10-bit conversion is achieved over the input range ±10 V with negative numbers expressed in 1's complement.

III. Factors Limiting Accuracy

While monolithic circuit technology has had great impact on the cost of many analog circuit functions, such as operational amplifiers, the impact on the cost of A/D and D/A converters has not been as great. This is due to the complexity of a complete converter, and more importantly, to the problem of component matching. Because of the difference between the aspect ratios of diffused resistors of practical value versus those of capacitors, the attainable matching accuracy is higher for capacitors given the same overall die area. The flexibility of capacitor geometry allows them to be made square or even circular so as to optimize matching accuracy, as discussed further in the companion paper [3].

In this technique a mismatch in the binary ratios of capacitors in the array causes nonlinearity. It cannot cause a gain

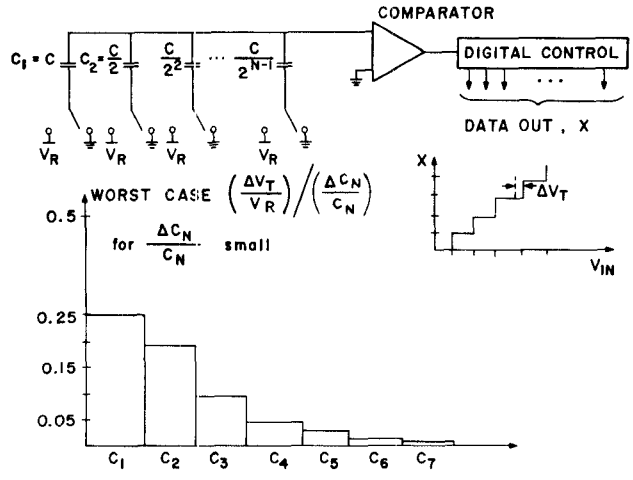

Fig. 5. Sensitivity of A/D conversion linearity to individual capacitor value.

error because the end points of the transfer function curve, V_{out} versus V_{in}, are not dependent on capacitor matching. This results from the fact that no net charge redistribution between capacitors occurs for either zero or full-scale input since all capacitors are either fully discharged or fully charged, respectively. For the same reason no offset error can arise from capacitor mismatch since the mismatch cannot be manifested unless a charge redistribution exists in the final configuration.

First consider the ideal case in which all the capacitors of the general N-bit converter shown in Fig. 5 have the precise binary weight values. For this case the digital output x is a regular staircase when plotted against V_{in}, and every transition occurs at a precise value of V_{in} designated V_T. On the other hand, changing one capacitor from its ideal value by a small amount ΔC_N causes all transition points to shift somewhat, but there will be one worst case transition. The ratio $\Delta V_T/V_R$ is the normalized worst case fraction deviation in transition point from the ideal. This is also a measure of the nonlinearity. The ratio of this deviation to the fractional change in capacitor value $\Delta C_N/C_N$ represents the sensitivity of linearity to individual capacitor value. The plot of sensitivity, also shown in Fig. 5, shows that linearity is very sensitive to a fractional change in the large capacitors, but not very dependent upon similar fractional changes in the smaller capacitors. Therefore, the smaller capacitors have great allowable tolerances. It should be pointed out that actually all capacitors have simultaneous deviations which cause ratio errors and the worst case combination of these must always be considered. Thus, the optimization of the ratio accuracy in the array is a prime consideration.

Capacitor ratio error results from several causes, one of which is the undercutting of the mask which defines the capacitor. Consider two capacitors C_4 and C_2, shown in Fig. 6, which are nominally related by a factor of 2: $C_4 = 2C_2$. During the etching phase of the photomask process a poorly controlled lateral etch occurs called undercut. Let Δx be the undercut length and L_4 be the side length of C_4, also shown in Fig. 6. Then a ratio error is produced between C_4 and C_2 which is proportional to the undercut length:

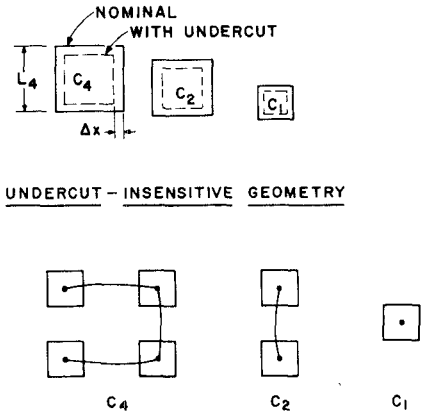

Fig. 6. Capacitor ratio error due to photomask undercut.

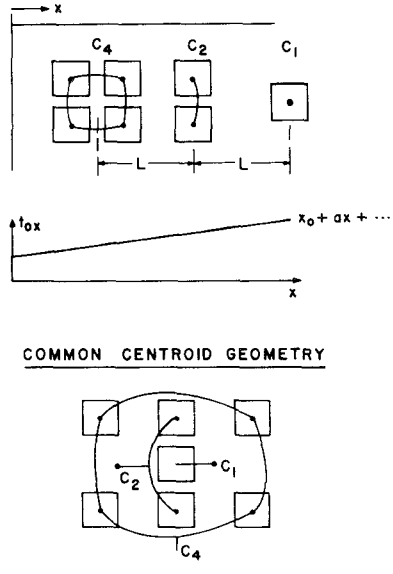

Fig. 7. Capacitor ratio error due to oxide gradients.

$$C_4 = 2C_2(1 + \epsilon); \qquad \epsilon \simeq 4\frac{\Delta x}{L_4}.$$

This problem can be circumvented by a geometry such that the perimeter lengths as well as the areas are ratioed. This can be done, as seen in Fig. 6, by paralleling identical size plates to form the larger capacitors. Thus the capacitor ratios are not affected by undercut.

Long range gradients in the thin capacitor oxide can also cause ratio errors. These gradients arise from nonuniform oxide growth conditions. If this variation in oxide thickness is approximated as first-order gradient, as shown in Fig. 7, then the resulting ratio error is proportional to the fractional variation in oxide thickness:

$$C_2 = 2C_1(1 + \epsilon L)$$

$$C_4 = 4C_1(1 + 2\epsilon L); \qquad \epsilon = \frac{a}{x_0}.$$

Experimentally, values of 10–100 ppm/mil have been observed for the factor ϵ. Error from this source can be minimized by improved oxide growth techniques and by a common centroid geometry. This is done in Fig. 7 by locating the elements of the capacitors in such a way that they are symmetrically spaced about a common center point. In this way the capacitor ratios may be maintained in spite of first-order gradients. Although undercut and oxide gradient errors can be minimized, a random edge variation will still exist and cause small ratio errors.

Any significant variation of small signal capacitance with dc terminal voltage would limit the accuracy because a nonlinearity would result. For MOS capacitors on heavily doped N+ back plates voltage coefficients of less than 24 ppm/V have been observed. This is insignificant at the 10-bit converter level.

Dielectric absorption is a phenomenon in which a residual voltage appears on a capacitor after it has been rapidly discharged. However, MOS capacitors display a relaxation which is unimportant for the 10-bit converter.

The voltage comparison process is fundamental to A/D conversion. The offset voltage of the comparator is usually manifested as an offset error in the digital conversion. Because of the relatively large gate-source voltage mismatch in MOS differential amplifiers, the offset voltage of the all-MOS comparator must be eliminated as a source of error. This can be accomplished either by digital means or by offset cancellation techniques. In this circuit the offset is stored and then subtracted at a later time by the sequence of events illustrated in Fig. 8. During the sample mode, V_{in} remains connected to the bottom plates but switch $S1$ is also ON and precharges the top plate of the array to the threshold voltage of stage $A1$. $S1$ then turns off, but since $A2$ is identical to $A1$ its input is also at the threshold. Since $S2$ is ON in the "up" position the output of $A2$ is saved at a storage node at one input of $A3$. During the subsequent redistribution mode $S1$ always remains OFF but $S2$ turns ON in the "down" position after each redistribution loading the output of $A2$ at the other storage node input of $A3$. This provides a first-order cancellation of switch feedthrough at both storage nodes. Since $A3$ is a difference amplifier, the offset of $A1$ and $A2$ together with the feedthrough of $S1$ have been cancelled. The offset of $A3$ is

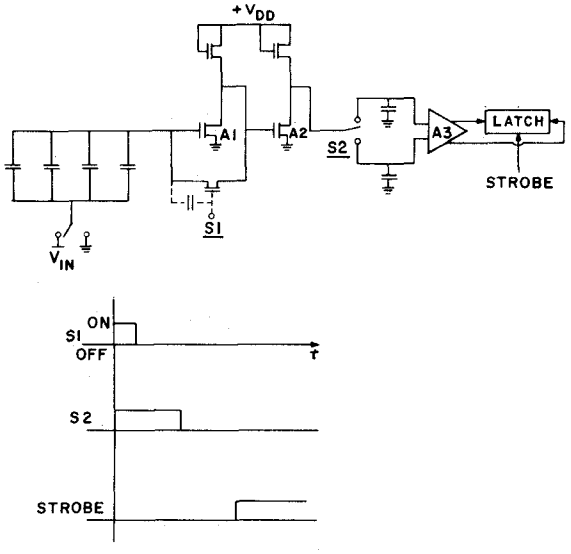

Fig. 8. Comparator offset cancellation.

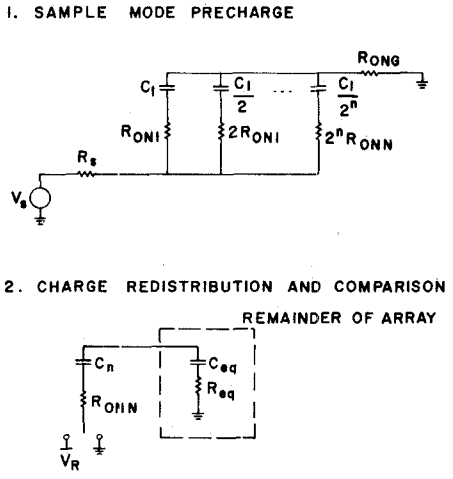

Fig. 9. Factors limiting conversion rate.

therefore the only significant offset in the comparator. This offset is reflected back through the gain stages $A1$ and $A2$ giving an effective offset [5]:

$$V_{OS_{\text{effective}}} = \frac{V_{OS_{A3}}}{G_{A1} \cdot G_{A2}}.$$

The gain product $G_{A1} \cdot G_{A2} \approx 50$ for this circuit.

The conversion technique as described thus far produces a transfer characteristic like that shown in Fig. 5 in which the first transition occurs at one LSB voltage away from the origin. Actually, for minimum quantization error this first transition should occur only $\frac{1}{2}$ LSB voltage away from the origin. The cancellation of this offset may be accomplished by returning the lower plate of the smallest capacitor to $V_{\text{ref}}/2$ rather than ground after the sample mode.

A great advantage of the S_iO_2 dielectric capacitor is its very low temperature coefficient of approximately 20 ppm/°C in contrast with approximately 2000 ppm/°C for diffused resistors and several hundred ppm/°C for thin film and implanted resistors. Thus, capacitor ratios are less sensitive to temperature gradients than resistor ratios. Since component mismatch usually has a greater effect upon linearity than upon gain or offset errors, the temperature coefficient of nonlinearity is lower for this conversion technique in comparison with R-$2R$ approaches.

IV. Factors Limiting Conversion Rate

Compared with many conversion techniques, the successive approximation method used in this circuit is capable of rapid conversion. The conversion requires two distinct operations. The first is the charging of the capacitor array to the input voltage during the sample mode, and the second is the redistribution of the charge on the capacitor array during the successive approximation conversion process. The equivalent circuit during the sample mode is shown in Fig. 9. The total array capacitance C_T is charged through the source resistance R_s, and equivalent ON resistance of the top plate grounding switch R_{ON_G}, and the equivalent ON resistance of the binarily scaled switches. The time constant is thus:

$$\tau_1 = \left[R_S + \frac{R_{ON_1}}{2} + R_{ON_G}\right] C_T.$$

During the redistribution cycle, also illustrated in Fig. 9, the time constant is the series combination of the capacitor being tested and its switch resistance plus the equivalent capacitance and resistance of the remaining elements of the array:

$$\tau_2 = \frac{R_{ON_1}}{2} C_T.$$

The maximum conversion rate is determined by the time required for one sample mode precharge and subsequently for ten redistribution cycles to go to completion, with time allowed for one comparison after each redistribution. In the experimental circuit to be described later, each of these delays contribute to the total conversion time, but it is instructive to consider the fundamental limitations on the conversion rate of this technique.

Assuming that the source resistance R_s can be made small, the acquisition time τ_1 is dependent upon R_{ON_1} and R_{ON_G}. The former can be made small compared to R_{ON_G} since the gate-source and gate-drain capacitance of the bottom plate switches do not result in conversion errors. The gate-drain capacitance of the grounding switch, however, can affect the accuracy of the conversion [8]. In the realization described later this error is cancelled, but assume for the time being that this was not done. The time constant during precharge for this limiting case is

$$\tau_1 = R_{ON_G} C_T = \frac{C_T}{\mu \frac{w}{L_C} C_0 (V_{GS}(\text{ON}) - V_T)}.$$

Assuming an optimum gate drive signal on the grounding

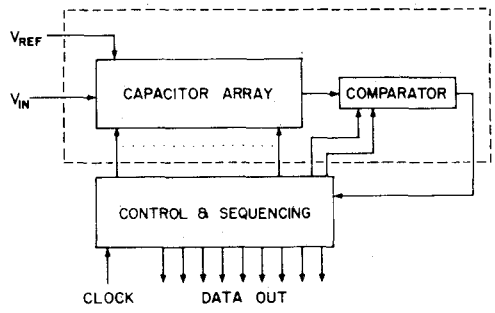

Fig. 10. Complete A/D converter.

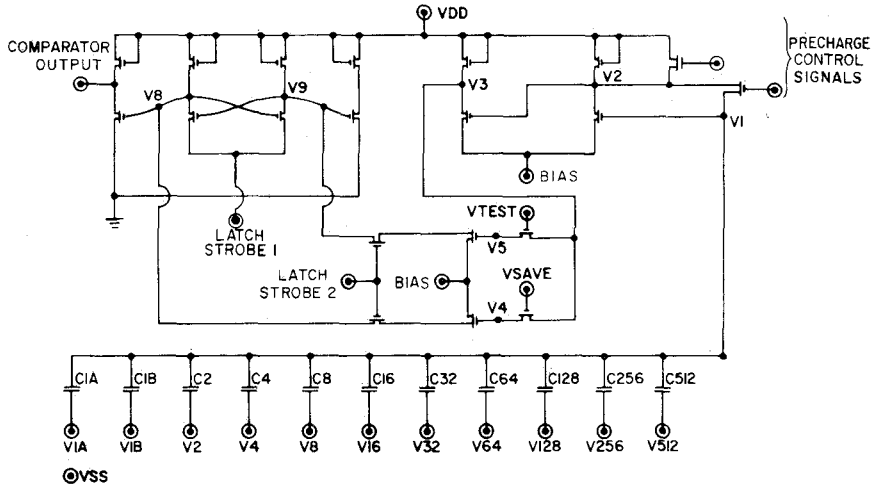

Fig. 11. Schematic of the experimental integrated circuit.

switch, the error voltage is given by

$$V_E = \frac{C_{GS}}{C_T}(V_{GS}(\text{ON}) - V_T)$$

and therefore

$$V_E \tau_1 = \frac{C_{GS}}{\frac{w}{L_C} C_0} \simeq \frac{L_C^2}{\mu}.$$

Here the overlap capacitance has been neglected, and it has been assumed for simplicity that the error charge transferred to C_T is simply the channel inversion layer charge, represented by the quantity $C_{GS}[V_{GS}(\text{ON}) - V_T]$. This result implies for example, that for a 0.1 percent error, 10-μ channel length, and N-channel devices, a minimum acquisition time of about 3 μs is required.

Actually, this source of error is not a fundamental limitation on accuracy since it is simply an offset error and can be cancelled by using either analog or digital techniques. These techniques, however, require considerable time for the sampling and processing of the offset voltage so that this problem does place a practical limit on the conversion rate.

The redistribution time τ_2 is dependent on R_{ON} of the bottom plate switches which can be made arbitrarily small at the cost of the die area. For very large devices, the redistribution time will approach that required for the switches to change their own drain-bulk capacitance.

Following each redistribution, a time interval is required for the voltage comparator to settle to the correct state. This time interval becomes longer as the resolution becomes higher and the minimum overdrive signal becomes smaller. Comparator delay is a fundamental limiting factor in the rate at which conversions can be accomplished.

V. Circuit Description and Experimental Results

Fig. 10 shows a complete A/D converter using the technique described in this paper. In block diagram form the system is composed of a capacitor array, a comparator, and control and sequencing logic. The feasibility of this technique was investigated by fabricating only the critical portions of the circuit, the array and the comparator, in monolithic form using standard N-channel MOS technology. Although the control and sequencing logic was composed of TTL gates, the monolithic realization of this circuit in MOS technology is straightforward.

The experimental integrated circuit schematic is shown in Fig. 11. During the sample mode, offset cancellation is accomplished by the precharge control signals. After precharge is completed, the initial value of V_1 is saved at a storage node V_4 by the action of a transmission gate. After each redistribution, the amplified value of V_1 is transmitted to node V_5 in

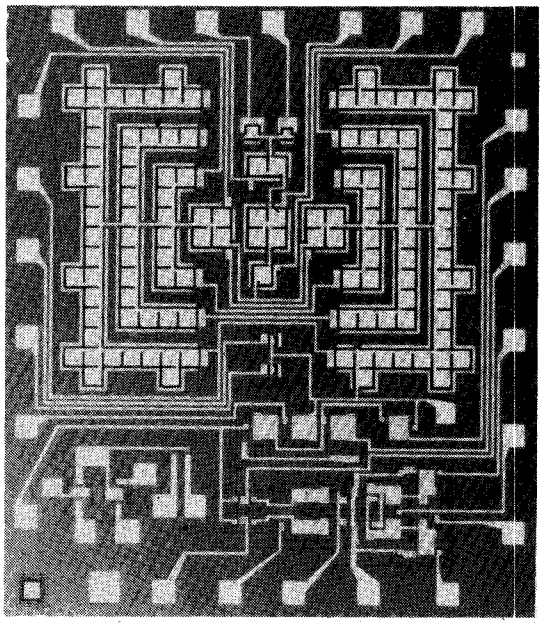

Fig. 12. Die photo.

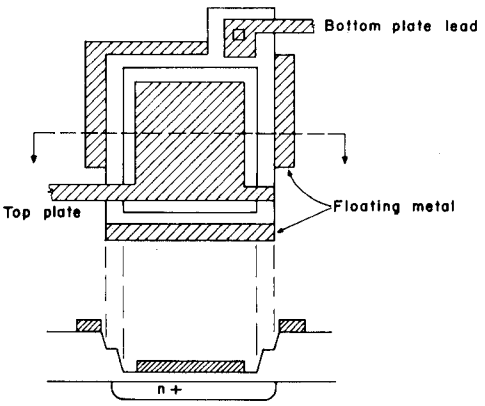

Fig. 13. MOS capacitor structure.

preparation for the subsequent test of the bit value. Since both latch strobe signals are initially high the difference signal at the latch is given by

$$(V_8 - V_9) = (V_4 - V_5) \cdot G_{A3}$$

where G_{A3} is the gain of amplifier $A3$ previously discussed. The total signal gain from the comparator input to the latch input is about 200, hence a 10-mV change in V_1 produces a 2-V differential signal at the latch. When the latch strobe signals go low the cross-coupled pair becomes regenerative and the full gain of the comparator is realized. The final state of the latch is then buffered off chip.

The die photo of Fig. 12 shows the capacitor array totaling 240 pF positioned above the comparator. The extreme right and left segments of the array are connected in parallel to form the largest capacitor. The next two segments on each side compose the next largest capacitor and so on, so that the common centroid is the center of the array. Note that the larger capacitors are composed of small squares 3 X 3 mils to reduce the sensitivity to undercut. The capacitor array has dimensions 75 X 58 mils, and an estimated die size including the digital control is 90 X 90 mils.

The MOS capacitor structure is shown in Fig. 13. Notice that only the metal edge defines the capacitor area, thus taking advantage of the better resolution properties of some positive photoresists. The floating redundant metal strips maintain a relatively constant etchant concentration at every capacitor edge, thereby assuring nearly uniform undercutting effects for all capacitors. The capacitor interconnect spans the thin oxide of each capacitor in a single direction so that capacitor area is insensitive to mask alignment errors. The area of the interconnect over the thin oxide is included in capacitor area calculations, while the area over the thicker oxide is neglected. Interconnect that passes over field oxide causes a parasitic capacitance from the top plate to ground which does not affect circuit performance as previously shown. A first-order cancellation of corner-rounding effects is made by designing each capacitor with an equal number of 90° and 270° corners.

The central question of the feasibility of this approach is the

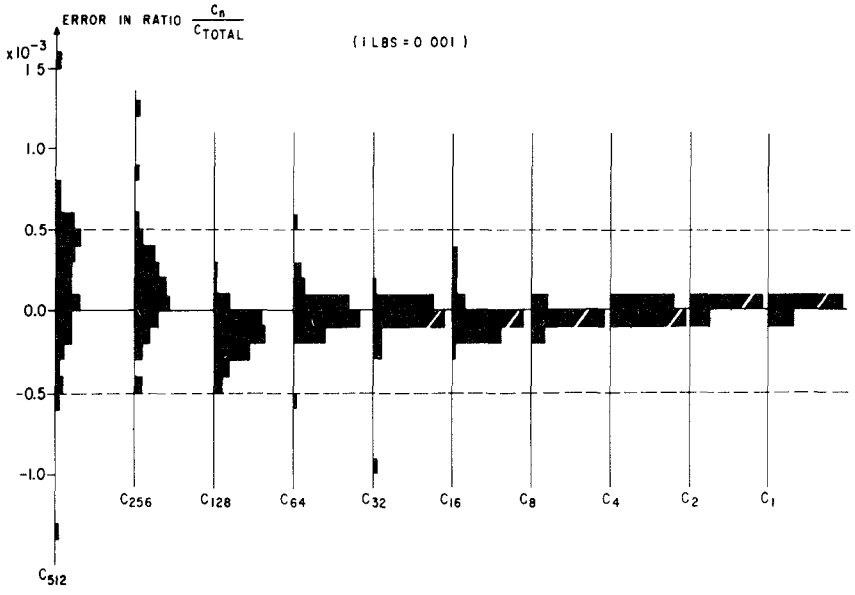

Fig. 14. Distribution of capacitor ratio errors for 47 10-bit converter arrays. Vertical axis is the fractional ratio error while the horizontal axis is the frequency of occurrence for each capacitor.

accuracy with which the capacitor ratios can be maintained using conventional photomasking. Extensive data have been gathered on the ratio accuracy of the array and typical results from three different wafers are shown in Fig. 14. This is the distribution of measured errors in the ratio of each individual capacitor to the total array capacitance. The horizontal axis represents the frequency of occurrence. Assume for a moment that capacitor ratio error were the only factor affecting yield. Then from these data the yield for $\pm\frac{1}{2}$ LSB linearity for 8, 9, and 10 bits resolution would be 98 percent, 94 percent, and 45 percent, respectively, for this sample of 47 functional arrays.

The feasibility of the technique was further studied by operating the experimental chip with external logic as a complete A/D converter. The linearity and offset of a sample of devices were evaluated using the experimental procedure shown in Fig. 15. The output of the A/D was connected to a 12-bit D/A converter. Since V_{in} was a long period ramp, the output of the D/A was a staircase. The difference between these signals is a representation of the total conversion error, and is connected to the y-axis of the plotter. The zero-to-full-scale recording of the output is shown also in Fig. 15. Since the 10-mV marks correspond to the $\frac{1}{2}$ LSB error levels the error is seen to be less than $\frac{1}{2}$ LSB. An expanded recording which permitted the visual resolution of all 1024 states was used for actual verification of the results.

A summary of the measured results is shown in Table I. The sample mode acquisition time is the minimum precharge time required for an accurate conversion of a 5-V step change at the input. The total conversion time corresponds to a 44-kHz sampling frequency.

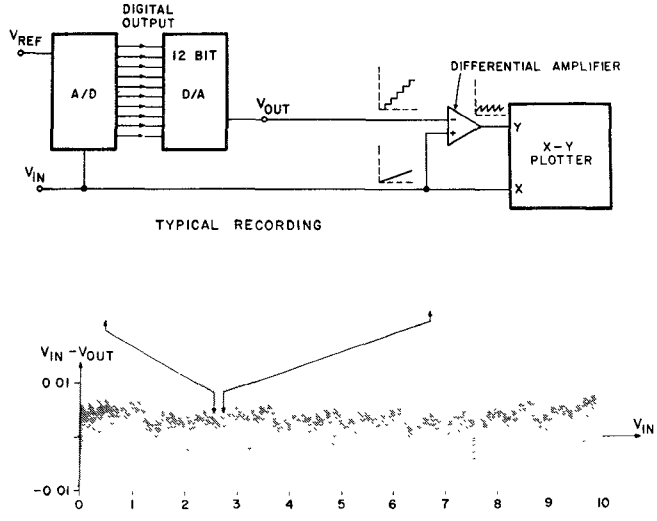

Fig. 15. Experimental measurement of A/D converter nonlinearity.

TABLE I
MEASURED PERFORMANCE DATA

Resolution	10 bits
Linearity	±1/2 LSB
Input voltage range	0–10 V
Input offset voltage	2 mV
Gain error	<0.05 percent (external reference)
Sample mode acquisition time	2.3 μs
Total conversion time	22.8 μs

VI. SUMMARY

A new, all MOS A/D conversion technique has been demonstrated which, with the addition of an external reference, can be used to realize a standard-process A/D converter on a single chip. Experimental data were presented which indicated that 8-bit resolutions can be attained at very high yield and low cost using standard N-channel MOS technology, and that 10-

bit resolution can be achieved at somewhat lower yield. It is believed by the authors that more careful control of photolithographic processing would result in very high yield at the 10-bit level and significant yield at even higher resolutions.

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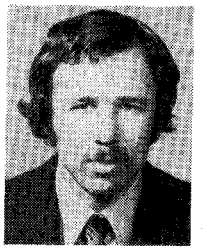

James L. McCreary (S'73) received the B.S. degree in electrical engineering from the University of Texas, Austin, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1968, 1971, and 1975, respectively.

Prior to attending the University of California at Berkeley, where his doctoral research area was analog-to-digital conversion techniques with MOS integrated circuit technology, he spent three years in the U.S. Navy as an Instructor in Nuclear Propulsion Systems. He is currently with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, and will join the Research Staff of Bell Laboratories, Holmdel, N.J., in January 1976.

Dr. McCreary is a member of Sigma Xi.

Paul R. Gray (S'65–M'69) was born in Jonesboro, Ark., on December 8, 1942. He received the B.S., M.S., and Ph.D. degrees from the University of Arizona, Tucson, in 1963, 1965, and 1969, respectively.

In 1969 he joined the Research and Development Laboratory, Fairchild Semiconductor, Palo Alto, Calif., where he was involved in the development and application of new technologies for analog integrated circuits. In 1971 he joined the Department of Electrical Engineering and Computer Science, University of California, Berkeley, where he is now an Associate Professor. Since 1971 he has acted as Consultant to Fairchild Semiconductor and Signetics Corporation.

Dr. Gray is a member of Eta Kappa Nu and Sigma Xi.

All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques—Part II

RICARDO E. SUÁREZ, MEMBER, IEEE, PAUL R. GRAY, MEMBER, IEEE, AND DAVID A. HODGES, SENIOR MEMBER, IEEE

Abstract—**This two-part paper describes two different techniques for performing analog-to-digital (A/D) conversion compatibly with standard single-channel MOS technology. In the first paper, the use of a binary weighted capacitor array to perform a high-speed successive approximation conversion was discussed.**

This second paper describes a two-capacitor successive approximation technique, which, in contrast to the first, requires considerably less die area, is inherently monotonic in the presence of capacitor ratio errors, and which operates at somewhat lower conversion rate. Factors affecting accuracy and conversion rate are considered analytically. Experimental results from a monolithic prototype are presented; a resolution of eight bits was achieved with an A/D conversion time of 100 μs. Used as a digital-to-analog (D/A) converter, a settling time of 13.5 μs was achieved. The estimated total die size for a completely monolithic version including logic is 5000 mil^2.

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R. E. Suárez was with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, Calif. He is now with the Instituto Venezolano de Investigaciones Cientificas (I.V.I.C.), Caracas, Venezuela.

P. R. Gray and D. A. Hodges are with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, Calif. 97420.

I. INTRODUCTION

AS DISCUSSED in Part I [9] of this paper, widespread application of techniques for digital processing of analog signals has been hindered by the unavailability of inexpensive functional blocks for analog-to-digital (A/D) conversion. Traditional approaches to A/D conversion have required the simultaneous implementation of high-performance analog circuits, such as operational amplifiers, and of digital circuitry