A 1.5V, 10-bit, 14MS/s CMOS Pipeline Analog-to-Digital Converter

Andrew M. Abo and Paul R. Gray

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley
Berkeley, CA, USA

Abstract

A 1.5V, 10-bit, 14.3MS/s pipeline analog-to-digital converter was implemented in a 0.6μm CMOS technology. Emphasis was placed on observing device reliability constraints at low voltage. MOS switches were implemented without low-threshold devices by using a bootstrapping technique that does not subject the devices to large terminal voltages. The converter achieved a peak SNDR of 58.5 dB, maximum DNL of 0.51 LSB, maximum INL of 0.66 LSB and a power consumption of 36 mW.

Introduction

In mixed-mode analog-to-digital interfaces, there are many applications where a video-rate A/D converter is integrated with complex DSP blocks in a compatible, low-cost technology–particularly CMOS. Such applications include camcorders, wireless LAN transceivers, digital set-top boxes, and others.

Advances in CMOS technology, however, are driving the operating voltage of integrated circuits increasingly lower. It is clear that circuits will need to operate at 1.5V and below within the decade [1] [2]. As device dimensions shrink, the applied voltages will need to be proportionately scaled in order to guarantee long-term reliability.

The voltage limitations of the technology dictate that the A/D converter operate at the same low voltage as the digital circuitry. Furthermore, in achieving low-voltage operation, the reliability constraints of the technology must not be violated. Previous low-voltage, video-rate ADCs have either used clock multiplication techniques that introduce potential reliability problems [3], or utilized special enhancements to the CMOS technology such as low-threshold devices [4] or BiCMOS [5]. This paper describes a 1.5V, 10-bit, 14.3MS/s, pipeline ADC implemented in a CMOS technology with standard threshold voltages that avoids reliability problems.

Pipeline ADC architecture

The ADC uses a pipeline 1.5-bit/stage architecture with 9 stages as shown in figure 1. Each stage resolves two bits with a sub-ADC, subtracts this value from its input and amplifies the resulting residue by a gain of two. The stages are buffered by switched-capacitor gain blocks that provide a sample-and-hold between each stage, allowing concurrent processing. The resulting 18 bits are combined with digital correction to yield 10 bits at the output of the ADC.

This architecture has been shown to be effective in achieving high throughput at low power [3]. The low number of bits per stage coupled with digital correction relaxes the constraints on comparator offset voltage and DC opamp gain.

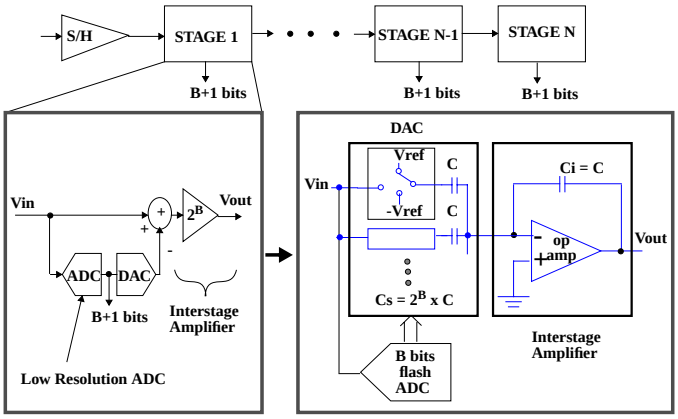

Fig. 1. Pipeline ADC 1.5-bit/stage architecture

Low-voltage circuit techniques and reliability

In order to design within the reliability limits of the technology, it is important to understand the mechanisms of device breakdown. Gate oxide breakdown and tunneling leakage limit the gate-source and gate-drain potential differences that can be applied to a transistor [6]. Also hot electron effects can damage the device and degrade performance over time [7], limiting the V_{DS} that can be applied. Similarly punch-through limits the magnitude of V_{DS}. If these critical terminal voltages, V_{GS}, V_{GD}, and V_{DS}, are kept within the rated operating voltage V_{DD} of the technology, device reliability can be assured.

Furthermore, these terminal voltages are only relative to each other and not to an absolute reference such as ground. Therefore, the absolute V_G referenced to ground may exceed the rated

V_{DD} if $V_{GS} < V_{DD}$ is maintained. This fact has been exploited in implementing the low-voltage MOS switch described below. Care must be taken, however, that the source-to-substrate and drain-to-substrate junctions do not exceed reverse breakdown voltages. These voltages are referenced to absolute ground. The reverse breakdown is typically much larger than the supply because the substrate is doped much less than the drain and source diffusions.

A. Reliable, high-swing MOS switch

Transmission gates were used extensively in the switched-capacitor gain stages of the pipeline. Because the threshold voltages of the NMOS and PMOS transistors were 0.7V and 0.9V respectively, conventional transmissions gates with any usable signal swing were not directly realizable. Therefore, a bootstrapped switch was required. Earlier bootstrap implementations [3] resulted in voltage stress exceeding the supply by a large margin. In this work, a bootstrap switch was designed to observe device reliability considerations. This switch is conceptually a single NMOS transistor as shown in figure 2.

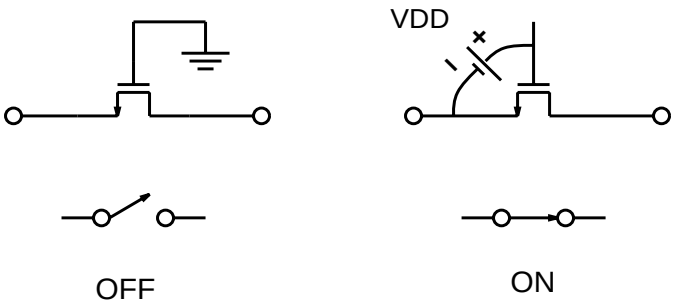

Fig. 2. Bootstrapped MOS switch

In the "off" state, the gate is grounded and the device is cutoff. In the "on" state, a constant voltage of V_{DD} is applied across the gate to source terminals, and a low on-resistance is established from drain to source independent of the input signal. Although the absolute voltage applied to the gate may exceed V_{DD} for a positive input signal, none of the terminal-to-terminal device voltages exceed V_{DD}.

Figure 3 shows the actual bootstrap circuit. It operates on a single phase clock ϕ that turns the switch M11 on and off. During the off phase, ϕ is low. Devices M7 and M10 discharge the gate of M11 to ground. At the same time, V_{DD} is applied across capacitor C3 by M3 and M12. This capacitor will act as the battery across the gate and source during the on phase. M8 and M9 isolate the switch from C3 while it is charging. When ϕ goes high, M5 pulls down the gate of M8, allowing charge from the battery capacitor C3 to flow onto the gate G. This turns on both M9 and M11. M9 enables the gate G to track the input voltage S shifted by V_{DD}, keeping the gate-source voltage constant regardless of the input signal. For example,

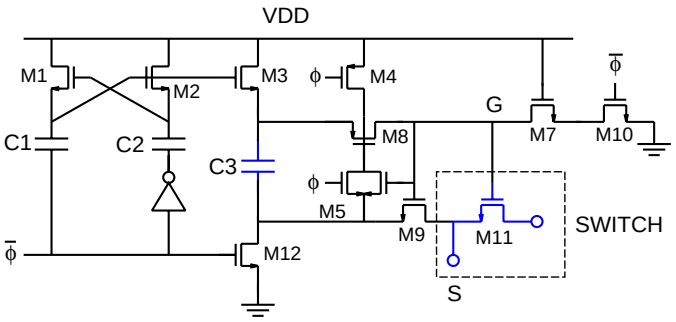

Fig. 3. Bootstrap circuit

if the source S is at V_{DD}, then gate G is at $2V_{DD}$, however, $V_{GS} = V_{DD}$.

M1, M2, C1, and C2 form a clock multiplier [3] that enables M3 to unidirectionally charge C3 during the off phase. This entire circuit was carefully designed such that no device is stressed beyond a voltage of V_{DD}. This circuit is similar to a previous low-distortion sampling switch [8].

B. Opamp

The opamp topology used in the gain stages is shown in figure 4. This two-stage, fully differential amplifier consists of a folded-cascode first stage followed by a common-source second stage. The common-source stage increases the DC gain to the order of 60 dB and maximizes the signal swing for a given voltage supply. Cascode compensation was used to improve the bandwidth over conventional Miller compensation. A high bandwidth was necessary to achieve fast linear settling. Switched-capacitor common-mode feedback was employed to stabilize the common-mode output voltage. Due to the limited operating voltage of 1.5V, several devices were biased at moderate to weak inversion.

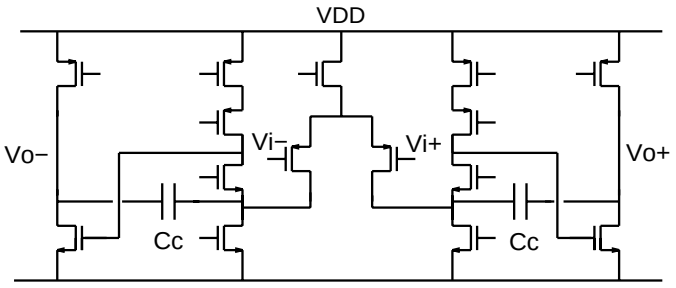

Fig. 4. Low-voltage opamp

C. Comparator

The sub-ADC in each pipeline stage consists of two fully differential comparators, such as the one shown in figure 5. In

the 1.5 bit per stage architecture, the sub-ADC thresholds are $+V_{ref}/4$ and $-V_{ref}/4$, where the ADC input range is $-V_{ref}$ to $+V_{ref}$ differential. The switched-capacitor comparator operates on a two phase non-overlapping clock. The differencing network samples V_{ref} during phase ϕ_2 onto capacitor C, while the input at capacitor $3C$ is shorted giving differential zero. During phase ϕ_1, the input signal V_i is applied at the inputs of both capacitors, causing a differential voltage proportional to $V_i - V_{ref}/4$ to appear at the input of the comparator preamp. At the end of phase ϕ_1' the regenerative flip-flop is latched to make the comparison and produce digital levels at the output V_o.

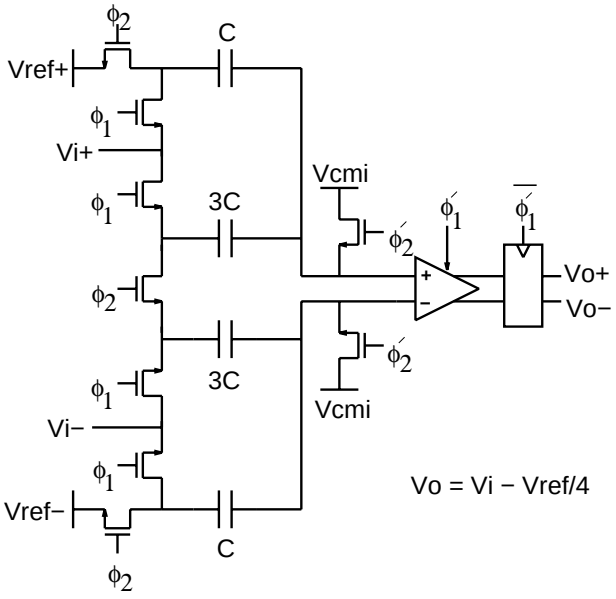

Fig. 5. Differential comparator

The preamp and latching circuit is shown in figure 6. During phase ϕ_1' the input $(V_i^+ - V_i^-)$ is amplified by the input transistors which are connected to PMOS triode load devices. During phase $\overline{\phi_1'}$, the input is disconnected and the the NMOS flip-flop regenerates the voltage difference. Digital inverters buffer the outputs and restore full logic levels. Due to digital correction, a comparator error of $V_{ref}/4$ (200 mV) can be tolerated.

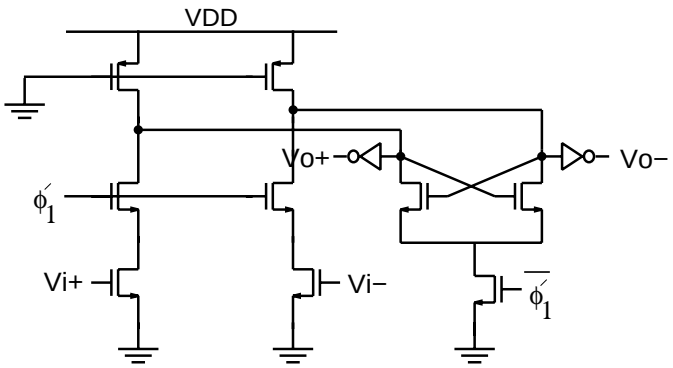

Fig. 6. Comparator preamp and latch

LSB, and the maximum integral non-linearity was measured at 0.66 LSB. Figure 8 shows the DNL and INL versus output code. The power consumption at a clock frequency of 14.3MHz was 36 mW from a 1.5V supply. Table I summarizes all the measured results.

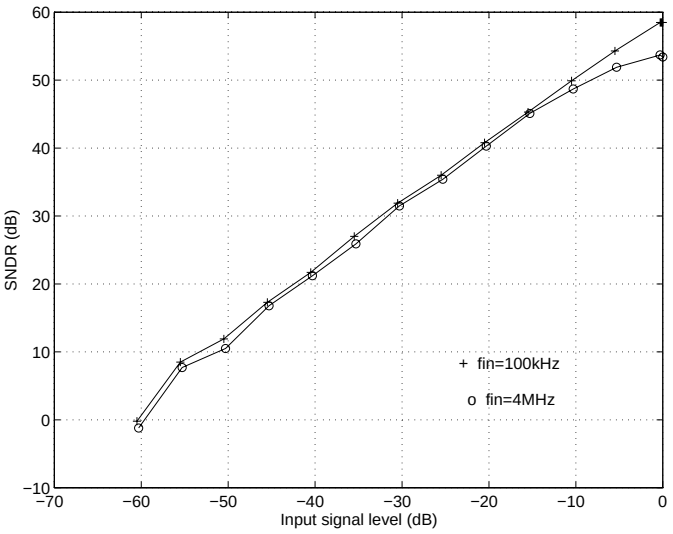

Fig. 7. SNDR vs input level

Measured results

An experimental prototype of the A/D converter was fabricated in a 0.6μm, single-poly, triple-metal CMOS technology with threshold voltages $V_{tn} = 0.7V$, $V_{tp} = 0.9V$ and a poly/n+ linear capacitor option. The die area not including the pad ring is 2.3 x 2.5 mm^2. Figure 9 shows the die photo.

The peak SNDR for a 100kHz sine wave input was measured at 58.5 dB with a clock frequency of 14.3MHz. Figure 7 shows the SNDR versus input level at a clock frequency of 14.3MHz. The maximum differential non-linearity was measured at 0.51

Conclusion

The trend toward lower voltage supplies is driven by reliability issues as device geometries become increasingly smaller. Therefore, an emphasis was placed on reliable low-voltage design. The bootstrapped MOS switch achieves rail-to-rail signal swing at low voltage without requiring low-threshold devices. Furthermore, this was achieved without overstressing any MOS devices. This 1.5V, 10-bit, 14.3MS/s, 36 mW pipeline A/D converter implemented in a 0.6μm CMOS technology demonstrates that video-rate analog signal processing

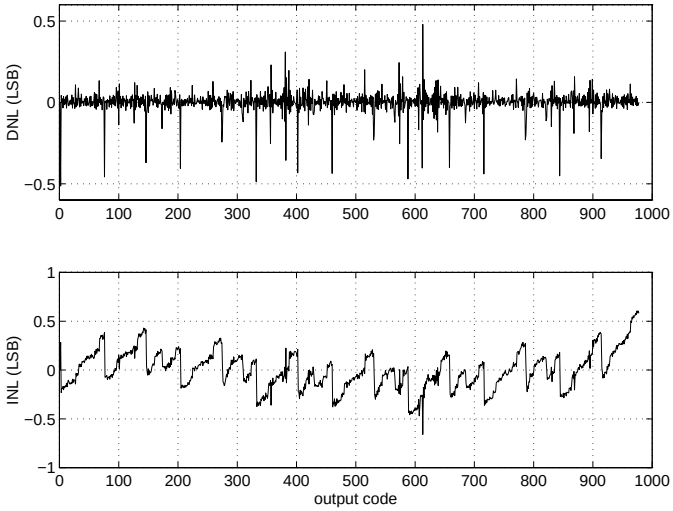

Fig. 8. INL and DNL versus output code

V_{DD}	1.5 V
Technology	0.6 μm CMOS $V_{tn} = 0.7V$, $V_{tp} = 0.9V$
Resolution	10 bits
Conversion rate	14.3 MS/s
Active area	2.3 x 2.5 mm^2
Input range	$\pm$800 mV differential
Power dissipation	36 mW (no pad drivers)
DNL INL	0.51 LSB 0.66 LSB
SNDR	58.5 dB (f_{in} = 100 kHz)

TABLE I
Measured A/D performance at 25° C

can be achieved at low voltage without requiring special enhancements to CMOS technology.

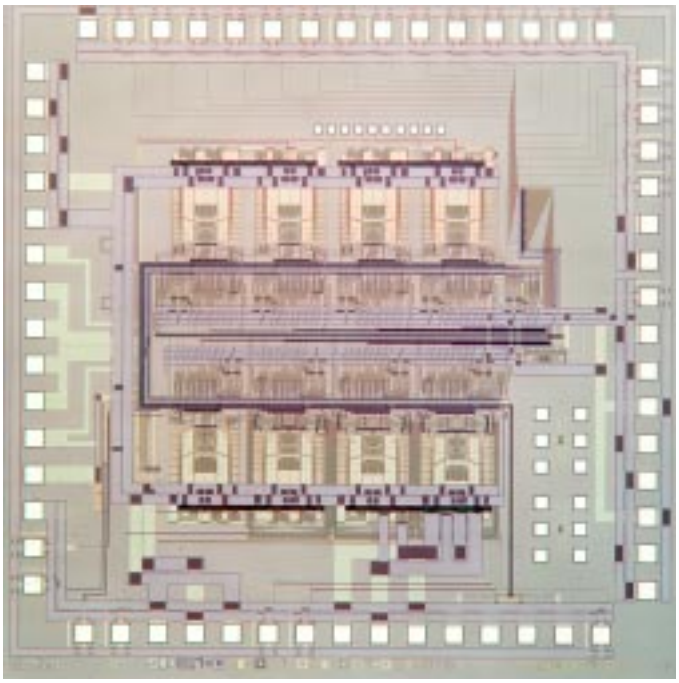

Fig. 9. Die photo

Acknowledgments

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