Switches

Requirements of an Ideal Switch:

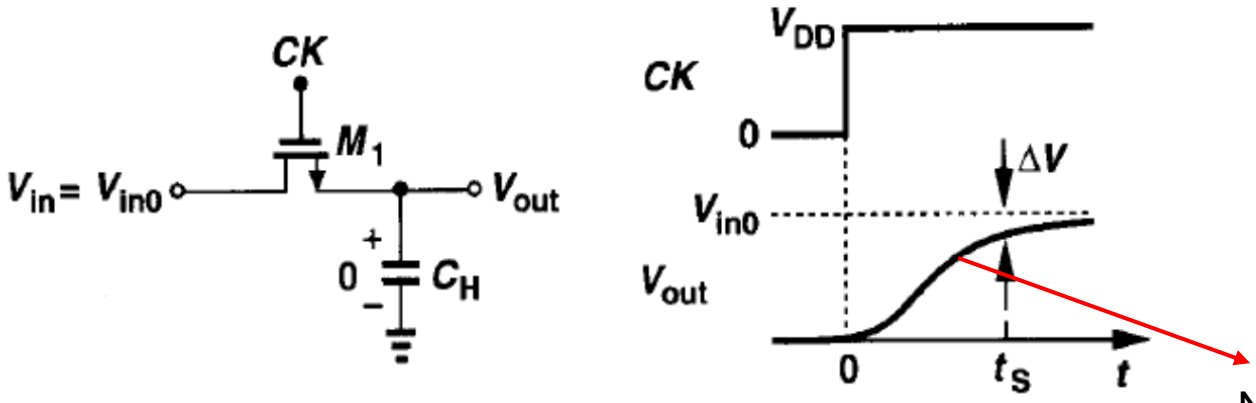
➔ Tracking (o/p tracks i/p)
➔ No Delay and Distortion
➔ No leakage (in both on and off states)

Ideal Switch Does not exist!

➔ Tracking range (0-Vdd)
➔ Speed(R_{on} and C_{par})
➔ Leakage and Distortion (Non-linearity of R_{on}, C_{par}, Channel Charge injection, Clock feed-through, Clock Jitter, Aperture Timing Error etc.)

Ref:- Advanced Analog Building Blocks : CMOS Switches, Wei Shen (Heidelberg University)

Switch speed:



➔ Input voltage dependent triode resistance

➔ Larger W/L improves speed (more distortion!)

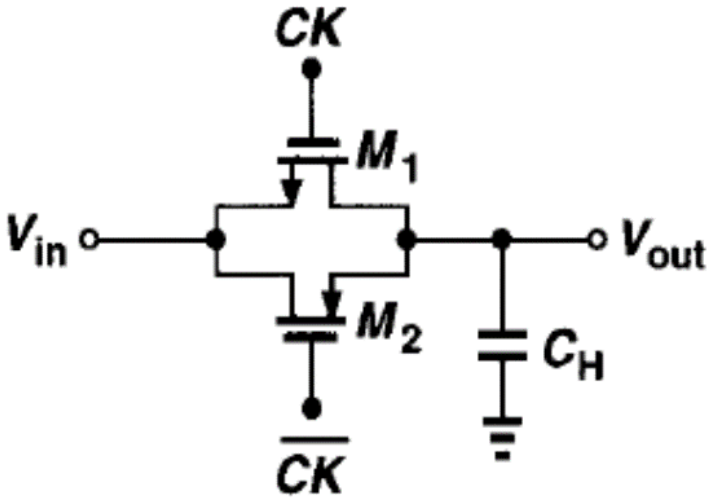
Not exponential!

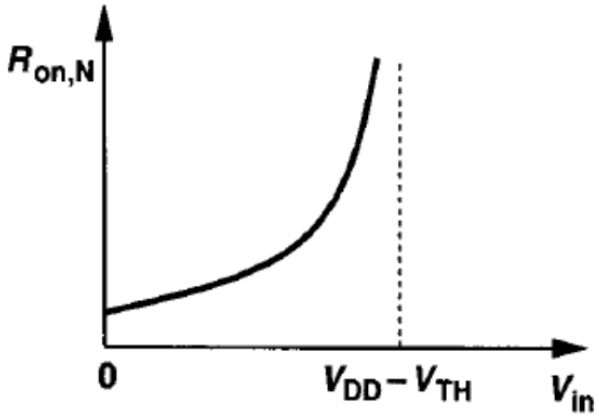
$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_{in,max} - V_{TH})} = \frac{4}{\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_{TH})}$$

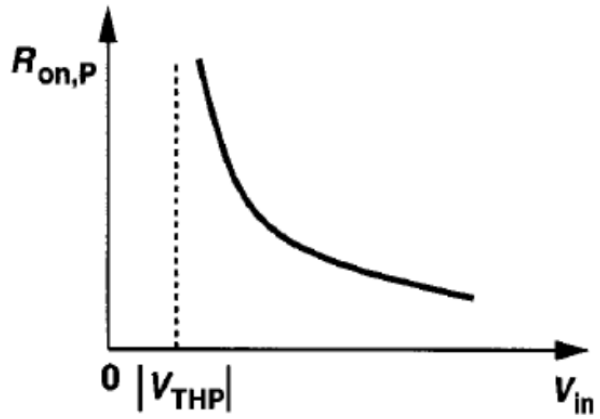
When V_{in} limited to 0-V_{DD}/2

"To maintain same resistance and smaller size(small C_{par}) we can increase control voltage and reduce W"

Complimentary Switches:

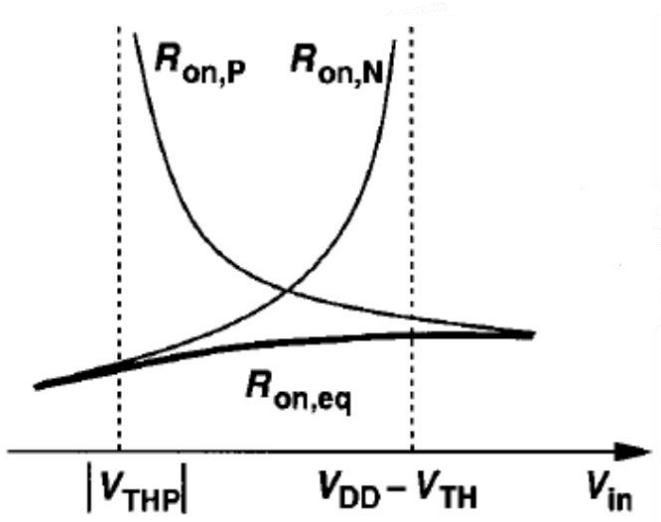






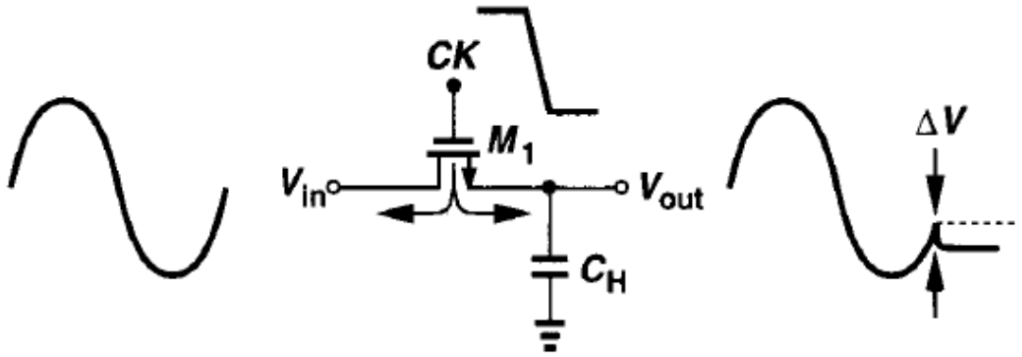
$$R_{on,eq} = R_{on,N} \| R_{on,P}$$

$$= \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_N (V_{DD} - V_{THN}) - \left[\mu_n C_{ox}\left(\frac{W}{L}\right)_N - \mu_p C_{ox}\left(\frac{W}{L}\right)_P\right] V_{in} - \mu_p C_{ox}\left(\frac{W}{L}\right)_P |V_{THP}|}$$



By proper selection of sizes of PMOS and NMOS to eliminate V_{in} dependence (Overestimation!)

Channel Charge injection:



Size dependent

$$Q_{ch} = WLC_{ox}\ (V_{dd} - V_{in} - V_{th})$$

Input voltage dependent

When clock transitions from high to low charge in the channel must flow somewhere!

-> Also depends on parasitic capacitance (voltage dependent) and substrate potential.

$$V_{out} = V_{in} - \frac{WLC_{ox}}{C_H}\left(V_{DD} - V_{in} - V_{TH0} - \gamma\sqrt{2\phi_B + V_{in}} + \gamma\sqrt{2\phi_B}\right)$$

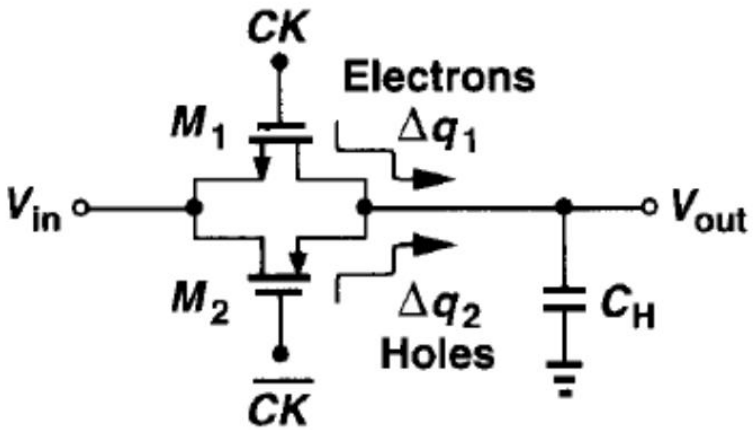
$$= V_{in}\left(1 + \frac{WLC_{ox}}{C_H}\right) + \gamma\frac{WLC_{ox}}{C_H}\sqrt{2\phi_B + V_{in}} - \frac{WLC_{ox}}{C_H}\left(V_{DD} - V_{TH0} + \gamma\sqrt{2\phi_B}\right).$$

Remedies:

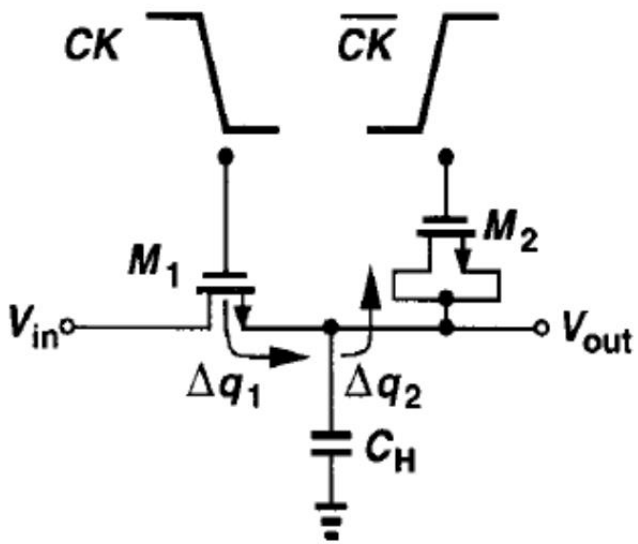
->complimentary switch

Cancellation (only at particular i/p)

->Dummy transistors

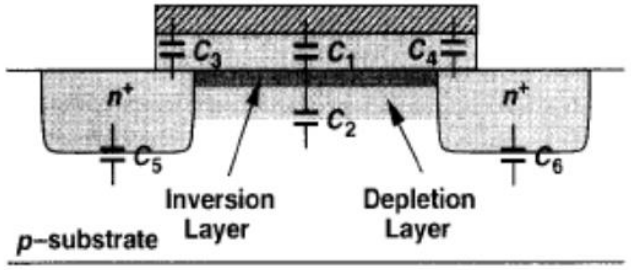


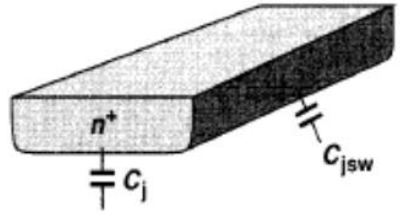
$$W_1 L_1 C_{ox}(V_{CK} - V_{in} - V_{THN}) = W_2 L_2 C_{ox}(V_{in} - |V_{THP}|)$$

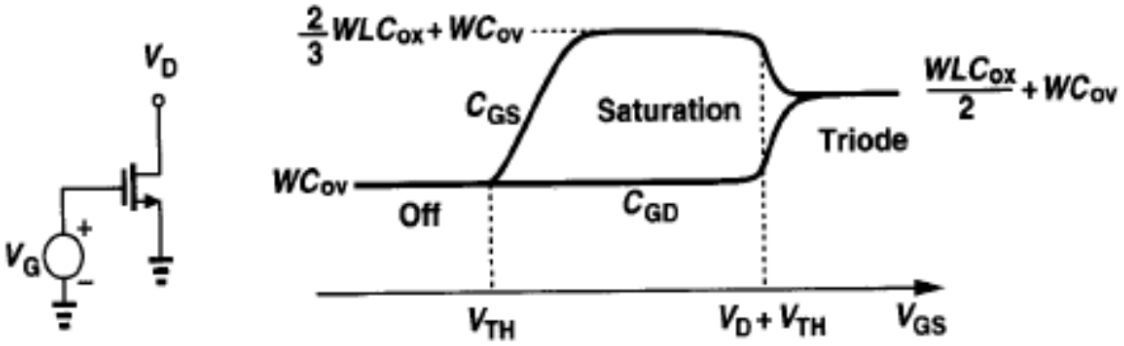


-> Charge redistribution to dummy channel

Parasitics:

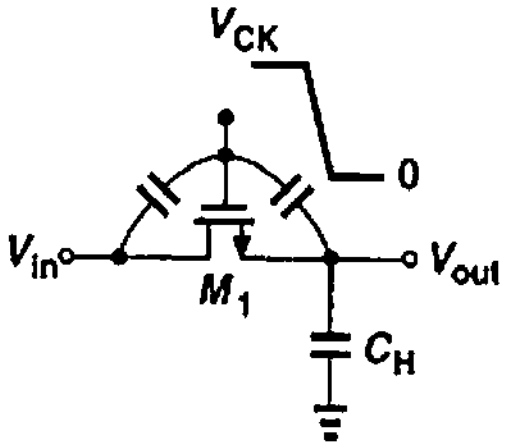






➔ The triode parasitics influence speed
➔ Off parasitics influence charge injection induced effects

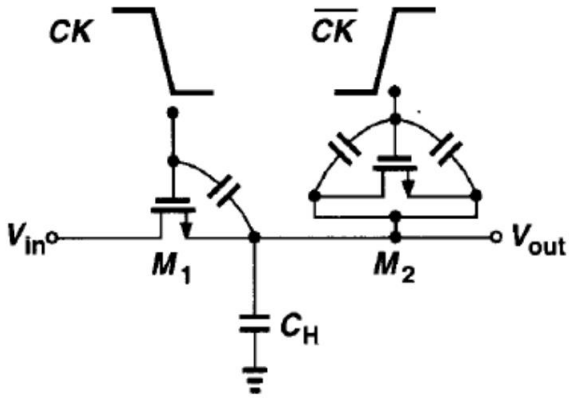
Clock Feedthrough:

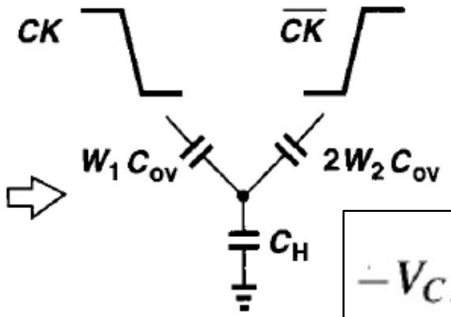


$$\Delta V = V_{ck} \frac{WC_{ov}}{WC_{ov}+CH}$$

-> Input voltage dependent (not visible From simple analysis)

Remedy:





$$-V_{CK}\frac{W_1C_{ov}}{W_1C_{ov}+C_H+2W_2C_{ov}}+V_{CK}\frac{2W_2C_{ov}}{W_1C_{ov}+C_H+2W_2C_{ov}}=0.$$

Make W_2 = 0.5* W_1

Imperfections of CMOS Switches:

➔ Channel Charge injection
➔ Clock Feedthrough

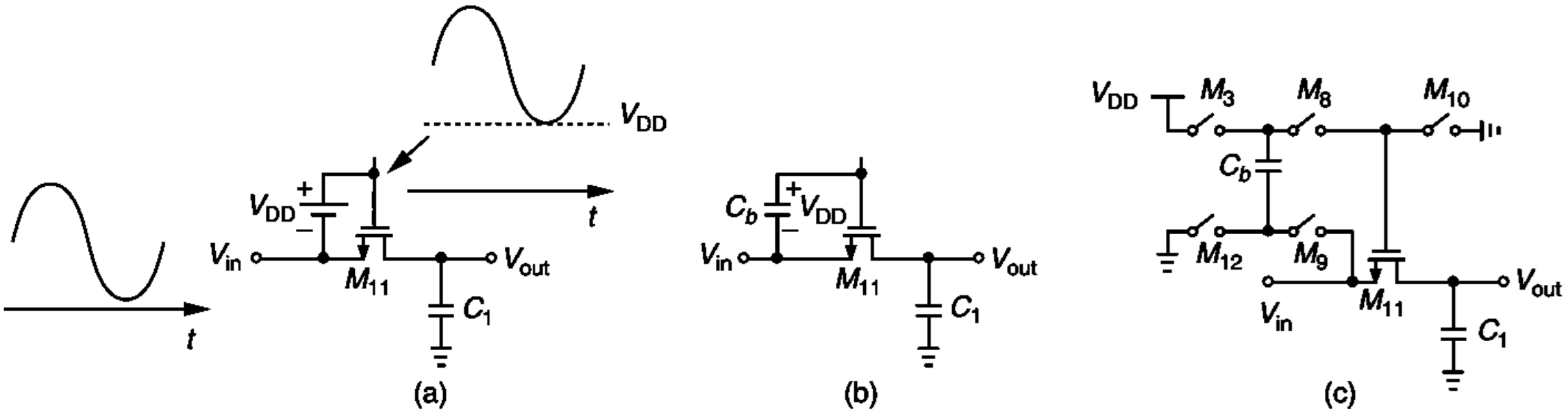
➔ Threshold voltage on substrate coupling

Can be eliminated by making Vgs constant (i.e provide offset 'V_{in}' to Control (gate) voltage)

Bootstrapping!

If MOSFET'S and supply voltage are small - not serious

Bootstrapping:

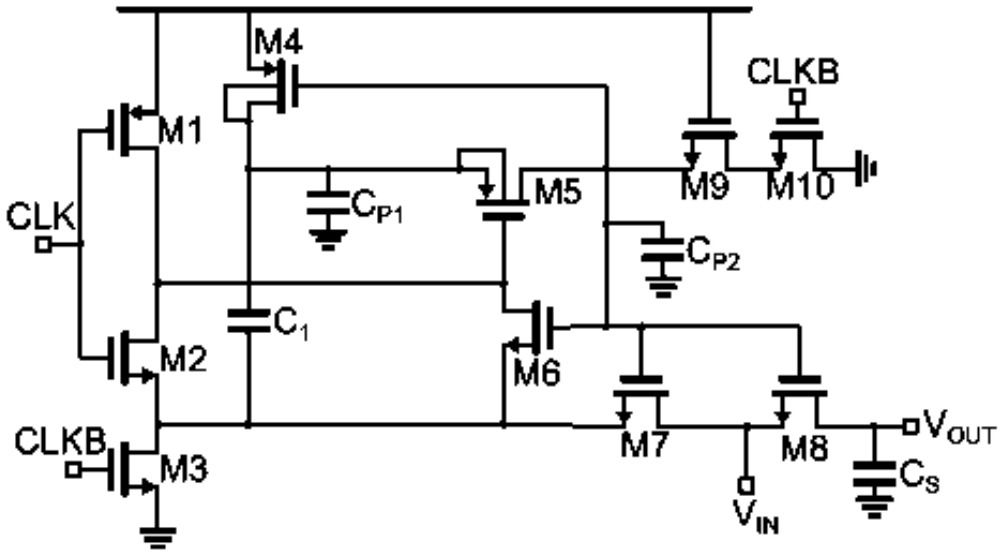


(a) Bootstrapping the gate to the input by a battery, (b) the use of a capacitor to approximate the battery, and (c) the addition of other switches to allow *M*11 to turn off and *Cb* to recharge

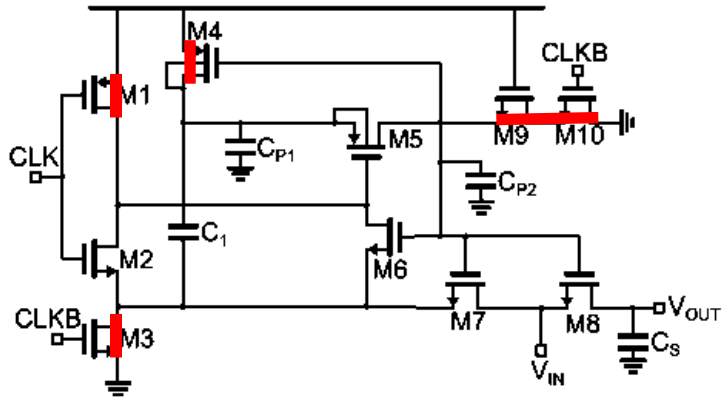
Ref:- A Bootstrapped Switch (2015), Behzad Razavi

Topology 1:

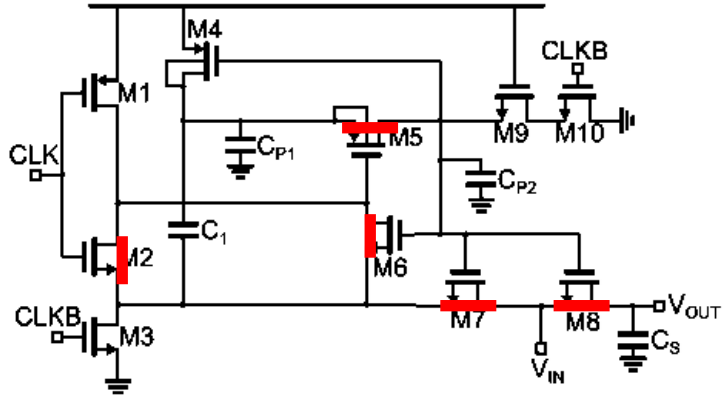
1)



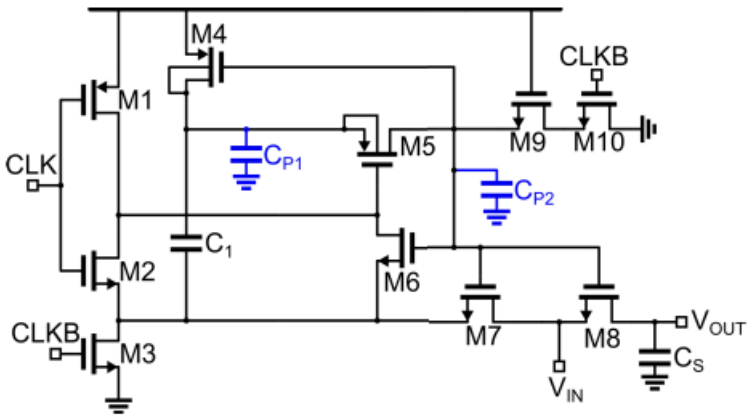
When CLK = 0 and CLKB = 1,
M1,M3, M4, M9, and M10 are turned on.
M2,M5, M6, M7, and M8 are turned off



When CLK = 1 and CLKB = 0
M1,M3, M4, M9, and M10 are turned off.
M2,M5, M6, M7, and M8 are turned on.



Ref: “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” IEEE J. Solid-State Circuits **45** (2010) 731 (DOI: 10.1109/JSSC.2010.2042254)



*C_{p1} and C_{p2} are parasitic capacitances

$$V_{G8} = \frac{C_1 + C_{P1}}{C_1 + C_{P1} + C_{P2}} V_{DD} + \frac{C_1}{C_1 + C_{P1} + C_{P2}} V_{IN}$$

$$V_{GS8} = \frac{C_1 + C_{P1}}{C_1 + C_{P1} + C_{P2}} V_{DD} + \left(\frac{C_1}{C_1 + C_{P1} + C_{P2}} - 1 \right) V_{IN}$$

$$R_{ON8} = \frac{1}{\mu_n c_{ox} \left(\frac{W}{L} \right)_8 (V_{GS8} - V_{TH8})}$$

If $C_{p1} + C_{p2} << C_1$, Then $V_{GS8} = VDD$

Bootstrap switch Design parameters and simulation results
Topology (1)

Ideal Calculations

(Assumption Vin,pk = VDD/2)

$$\text{D.R.} = 20\log\left(\frac{v_D}{2\sqrt{2}\sqrt{\frac{kT\alpha}{C}}}\right) = 20\log\left[v_D\sqrt{\frac{C}{\alpha}}\right] + 75\ dB$$

Where C in pF

$$\Rightarrow Let\ C = 10pF; \alpha = 2$$

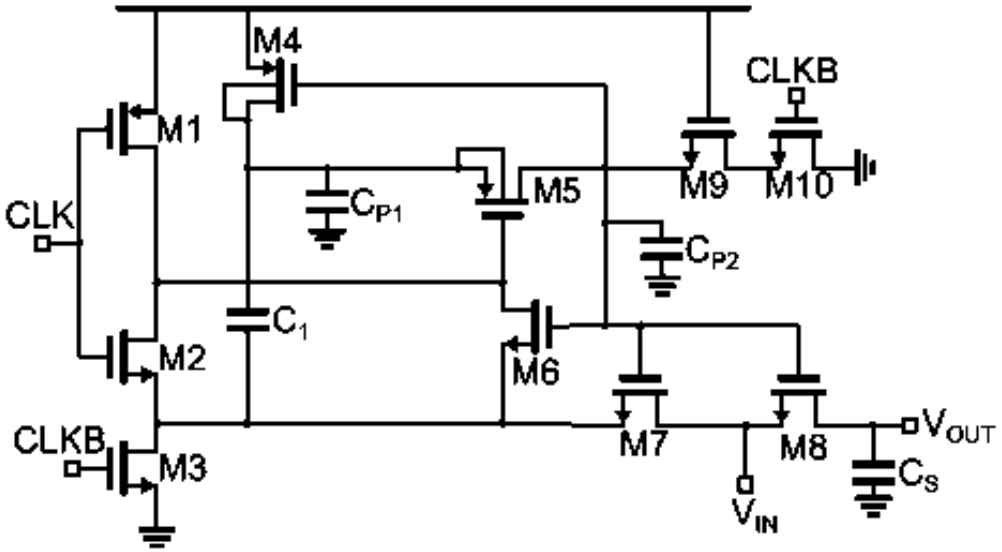
$$D \cdot R \cdot = 20\log 0.8\sqrt{\frac{10}{2}} + 75 = 80\ \mathrm{d}B$$

$$N = \frac{D \cdot R \cdot -1.78}{6.02} = 13bits$$

In practice ENOB = N-1 =12 bits.

*This is valid when system is limited by thermal noise

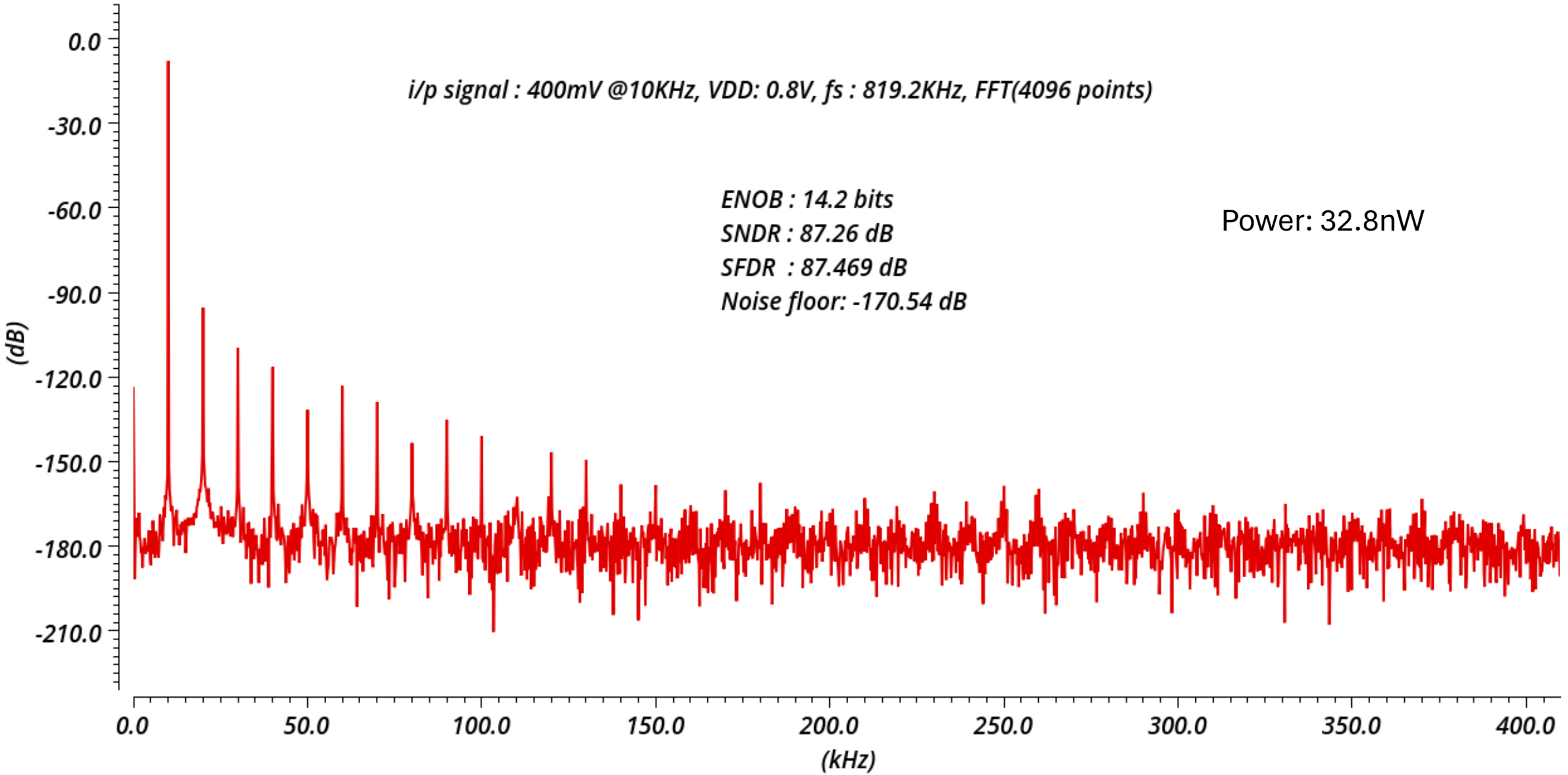
Topology 1: Design parameters



M1,M2,M3,M4,M5,M6	200n/60n
M7,M10	200n/60n
M9	200n/60n (stack of 2)
M8	800n/60n
C1	100f
Cs	10p

Ron,M8 = 550 Ω

Output Spectra of Switch

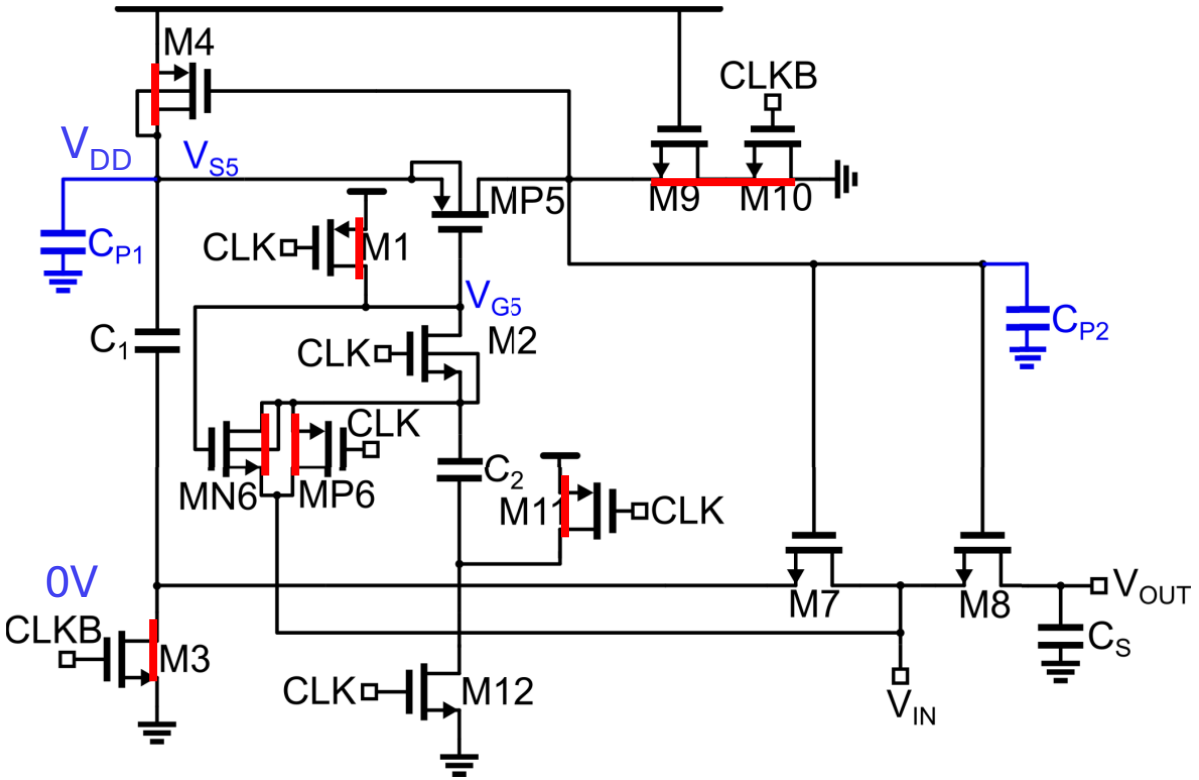


Power: 32.8nW

Fs = 128KHz
Fin= 6.375KHz,
FFT points (1024)
VDD = 0.8V

Vin ()	power	spectrum_sinad	spectrum_sfdr	spectrum_enob
100.0m	20.69n	88.99	89.01	14.49
200.0m	21.34n	83.91	83.97	13.64
300.0m	22.38n	81.38	81.47	13.22
400.0m	24.46n	79.60	79.72	12.93
500.0m	29.08n	78.02	78.19	12.67
600.0m	42.38n	76.31	76.60	12.38
700.0m	97.71n	73.86	74.57	11.98
800.0m	355.5n	62.20	66.54	10.04

Topology 2:



Analyzing the Switch:

When CLK = 0 and CLKB = 1 (hold state),

➔ C_2 top plate charged to V_{in}, bottom plate to V_{DD}.

➔ M2,MP5 are turned off

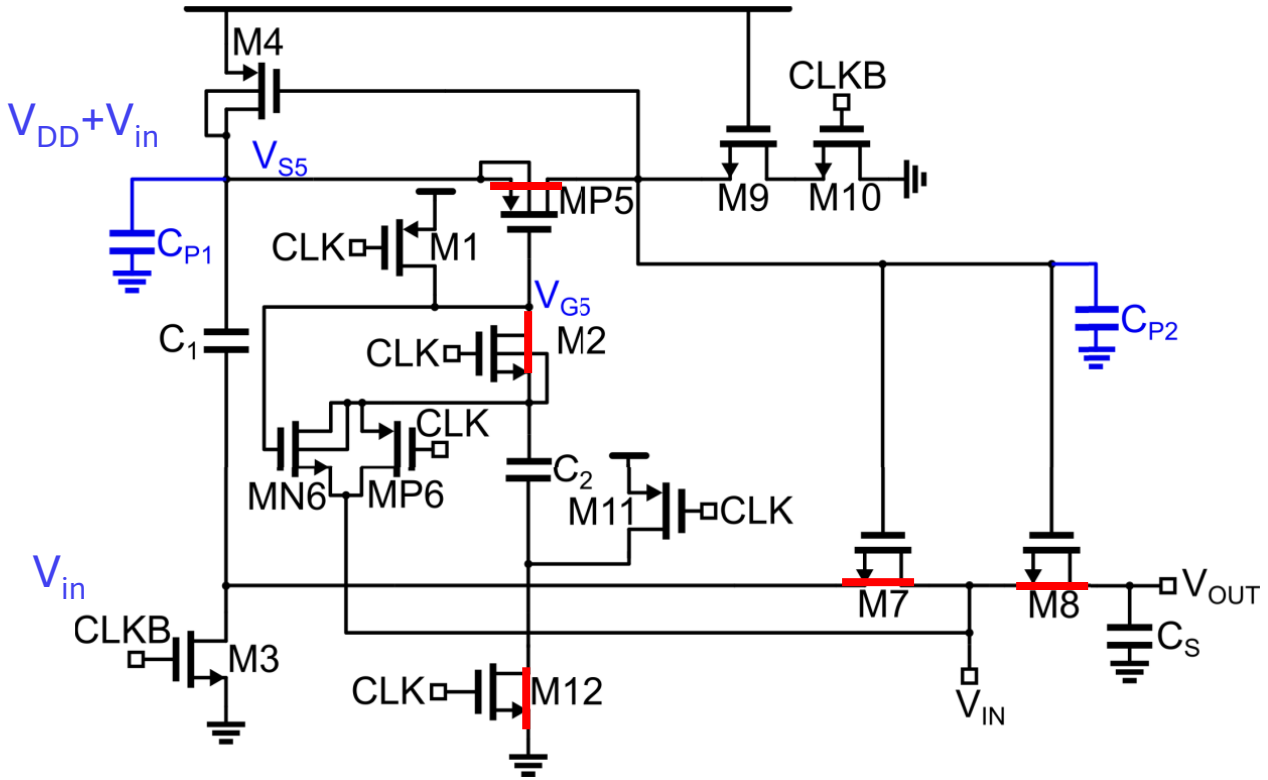
➔ The working state of the other transistors is the same as that of bootstrapped switch (previous)

$$V_{G5} = V_{DD}$$

$$V_{TOP\text{-}PLATE} = V_{IN}$$

$$V_{BOTTOM\text{-}PLATE} = V_{DD}$$

Ref: ‘‘Bootstrapped switch with improved linearity based on a negative-voltage bootstrapped capacitor’’(IEICE,2021). Cong Wei, Rongshan Wei, and Minghua He.



When CLK = 1 and CLKB = 0 (sampling state),

➔ MN6 and MP6 are turned off

➔ M12 is turned on

➔ C_2 top plate charged to V_{in}-V_{DD}, bottom plate to gnd.

$$V_{BOTTOM\text{-}PLATE} = 0$$

$$V_{TOP\text{-}PLATE} = V_{IN} - V_{DD}$$

$$V_{GS7} = V_{IN} + V_{DD} - V_{IN} = V_{DD}$$

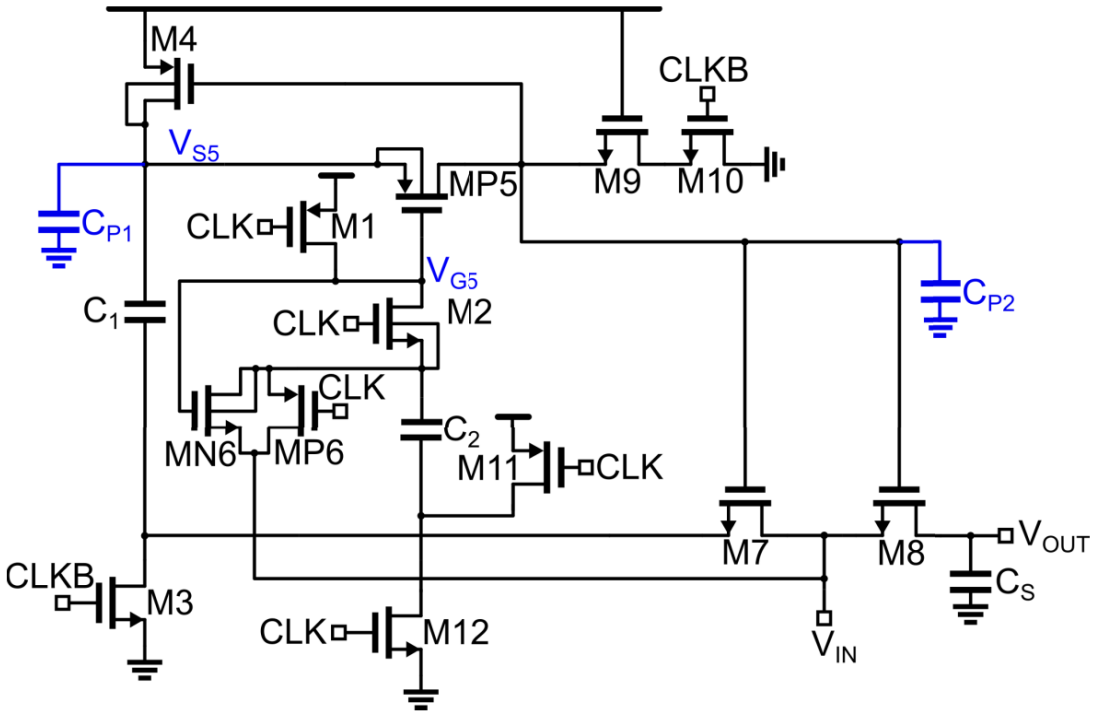
$$V_{G5} = V_{TOP\text{-}PLATE} = V_{IN} - V_{DD}$$

$$V_{GS5} = V_{IN} + V_{DD} - (V_{IN} - V_{DD}) = 2V_{DD}$$

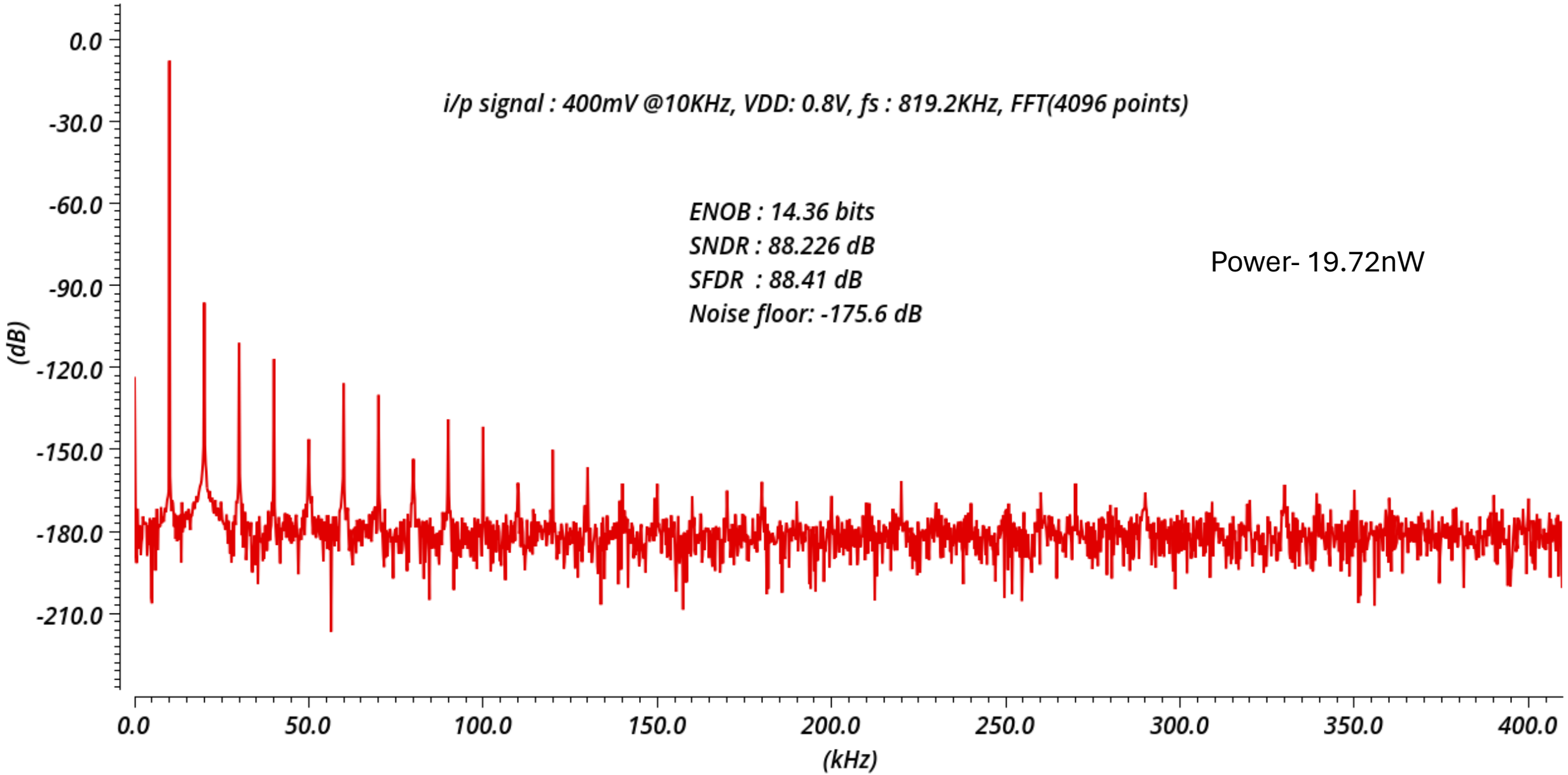
$$V_{GS8} = V_{IN} + V_{DD} - V_{IN} = V_{DD}$$

We were able to reduce size of MP5 without changing the resistance (as previous M5). $C_{p1,p2}\downarrow$

Bootstrap switch Design parameters and simulation results
Topology (2)



M1,M2,M3,M4,MP5,M6	200n/60n
M7,M10	200n/60n
M9	200n/60n (stack of 2)
M8	800n/60n
M11,M12	200n/60n (stack of 2)
MP6	200n/60n
MN6	removed
C1,C2	100f
Cs	10p


i/p signal : 400mV @10KHz, VDD: 0.8V, fs : 819.2KHz, FFT(4096 points)
ENOB : 14.36 bits
SNDR : 88.226 dB
SFDR : 88.41 dB
Noise floor: -175.6 dB
Power- 19.72nW
0.0
-30.0
-60.0
-90.0
-120.0
-150.0
-180.0
-210.0
(dB)
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
(kHz)

Fs = 128KHz
Fin= 6.375KHz
FFT points (1024)
VDD = 0.8V

Vin ()	power	spectrum_sinad	spectrum_sfdr	spectrum_enob
100.0m	15.35n	89.37	91.41	14.55
200.0m	15.43n	85.25	86.19	13.87
300.0m	15.51n	82.81	83.75	13.46
400.0m	15.66n	81.46	81.91	13.24
500.0m	15.90n	79.87	80.29	12.97
600.0m	16.24n	78.10	78.54	12.68
700.0m	16.71n	75.05	76.13	12.17
800.0m	17.47n	62.06	66.70	10.02