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Improved Complementary Bootstrap Switch Based on Negative Voltage Bootstrap Capacitance

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Abstract

The sample-and-hold (S/H) circuit is an important part of the ADC. An improved complementary bootstrap switch is proposed in this paper. A negative voltage bootstrap capacitance is introduced to reduce the parasitic capacitance of key nodes by minimizing the size of the transistor. The sampling MOSFET in this structure is composed of complementary NMOS and PMOS, which reduces the channel charge injection effect. The simulation results show that the effective number of bits (ENOB), signal to noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) of the structure are 16.5 bits, 101.11 dB and 101.83 dB respectively at the sampling frequency of 50 MHz and full swing voltage input of 1.8V based on SMIC 0.18 μm process. Compared with the traditional NMOS switch, ENOB, SDNR, and SFDR are increased by 2.3 bits, 14.9 dB, and 13.3 dB, respectively.

1. Introduction

The sample-and-hold (S/H) circuit is a critical part of ADC, and it largely determines the performance of ADC. However, the S/H circuit has many non-ideal characteristics, such as clock jitter, thermal noise (kT/C), charge injection, and clock feedthrough, which reduce the precision and speed of the circuit [1].

To alleviate the influence of these non-ideal factors, researchers have proposed many optimized structures. For example, add PMOS for sampling switch to reduce charge injection effect or remove the voltage doubler circuit to reduce the area [2] [3]. The parasitic capacitance of MOS is also a non-ideal factor affecting performance. The researcher designed a bootstrap switch based on a negative voltage bootstrap capacitor for this problem [4]. This structure enables the gate-source voltage of the PMOS switch to be maintained at about $2V_{DD}$ when it is turned on. Therefore, when the on-resistance (R_{ON}) remains the same, the PMOS can use a smaller size, thereby reducing the parasitic capacitance. On this basis, a sampling switch composed of complementary NMOS and PMOS is proposed in this paper, and a structure to maintain the gate-source voltage constant is designed for the PMOS switch.

2. Analysis of Negative Voltage Bootstrap Switch

The negative voltage bootstrap switch is shown in Figure 1. When CLK=0, CLKB=1, the switch is in the hold phase. M1, M3, M4, and M5 are turned on, M2, M6, and M7 are turned off, and the potential of the lower plate of the capacitor C_1 is V_{SS}, and the potential of the upper plate is V_{DD}. M8, M10, M11, M12 are turned on, M9, and M13 are turned off, the potential of the lower plate of capacitor C_2 is connected to V_{DD}, and the potential of the upper plate is changed to V_{IN} through the transmission gate. When CLK=1 and CLKB=0, the switch is in the sampling phase. The switches M1-M7 change to the opposite state, the potential of the lower plate of the capacitor C_1 is V_{IN}, and the potential of the upper plate is

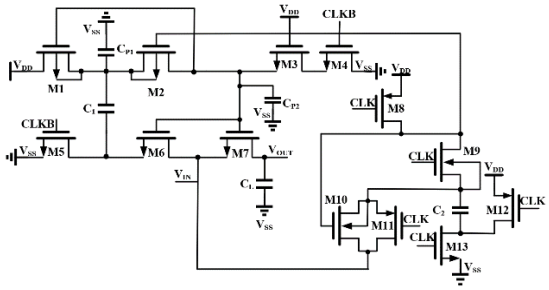

Figure 1. Conventional bootstrap switch circuit

V_{DD}+V_{IN}. M9 and M13 are turned on, M8, M10, M11, and M12 are turned off, and the potential of the lower plate of capacitor C_2 is pulled to V_{SS}. Because of charge conservation, the potential of the upper plate of C_2 becomes V_{IN}-V_{DD}.

When sampling, the gate-source voltage of the sampling switch M7 can be expressed as:

$$V_{GS7}=\frac{C_1+C_{P1}}{C_1+C_{P1}+C_{P2}}V_{DD}+\left(\frac{C_1}{C_1+C_{P1}+C_{P2}}-1\right)V_{IN} \quad (1)$$

where C_{P1} and C_{P2} are the parasitic capacitances of the key node transistors. The R_{ON} of M7 can be expressed as

$$R_{ON7}=\frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{M7}\left(V_{GS7}-V_{TH7}\right)} \quad (2)$$

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the length and width of the MOS, and V_{TH} is the threshold voltage. When C_{P1}+C_{P2}<<C_1, the gate-source voltage of M7 is V_{DD}. M2 is an important source of parasitic capacitance, and the R_{ON} of M2 can be expressed as

$$R_{ON2}=\frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{M2}\left(V_{SG2}-\left|V_{TH2}\right|\right)} \quad (3)$$

The gate-source voltage of M2 in the sampling stage is $2V_{DD}$, and the gate-source voltage of M2 in the traditional structure is about V_{DD} [5]. When R_{ON2} remains unchanged, the width-to-length ratio of M2 is reduced, thereby reducing the parasitic capacitances C_{P1} and C_{P2}.

3. Proposed Complementary Bootstrap Switch

The conventional bootstrap switch still has two problems. First, the source (S) and drain (D) of the sampling switch M7 are not fixed. When S is connected to V_{OUT}, the R_{ON} of M7 may change drastically; secondly, only the sampling switch composed of NMOS has the channel charge injection effect.

In order to solve these two problems, this paper continues to improve on the basis of the circuit in Figure 1. The sampling switch is made of NMOS and PMOS, and the related circuit is designed for the PMOS switch. The specific circuit is shown in Figure 2.

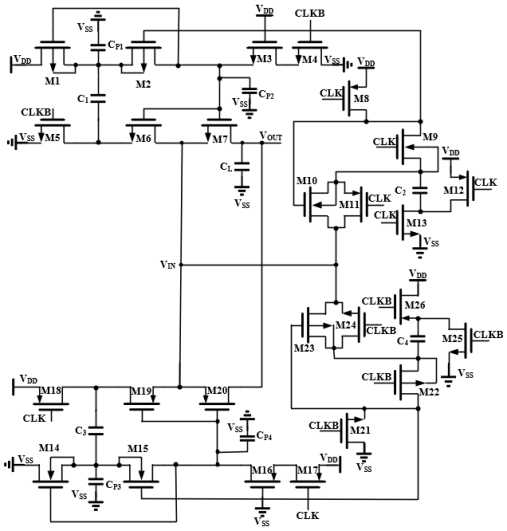

Figure 2. Proposed bootstrap switch circuit

When CLK=0 and CLKB=1, the circuit is in the hold phase, the potentials of the upper and lower plates of C_3 are V_{SS} and V_{DD}, and the C_4 is V_{IN} and V_{SS}. When CLK=1, CLKB=0, the circuit is in the sampling phase, C_3 becomes V_{IN}-V_{DD} and V_{IN}, and C_4 potential becomes V_{IN}+V_{DD} and V_{IN}. When sampling, the gate-source voltages of M15 and M20 are represented as follows:

$$V_{GS15}=\left(V_{IN}+V_{DD}\right)-\left(V_{IN}-V_{DD}\right)=2V_{DD} \quad (4)$$

$$V_{SG20}=V_{IN}-\left(V_{IN}-V_{DD}\right)=V_{DD} \quad (5)$$

Two advantages are shown by using complementary sampling switches. First, the variation in R_{ON} is reduced, improving the linearity of the circuit. The equivalent R_{ON} of the complementary switch can be expressed as:

$$R_{ON,eq}=\frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{M7}\left(V_{DD}-V_{TH7}\right)+\mu_P C_{ox}\left(\frac{W}{L}\right)_{M20}\left(V_{DD}-\left|V_{TH20}\right|\right)} \quad (6)$$

Second, the channel charge injection effect can be eliminated when equation (7) is satisfied.

$$W_7L_7C_{ox}\left(V_{DD}-V_{TH7}\right)=W_{20}L_{20}C_{ox}\left(V_{DD}-\left|V_{TH20}\right|\right) \quad (7)$$

4. Simulation results

The conventional and the proposed switches are simulated in Cadence Spectre in SMIC 0.18 μm CMOS technology. When sampling 4096 points for FFT, the output spectra of proposed and conventional bootstrap switches are shown in Figure 3 and Figure 4.

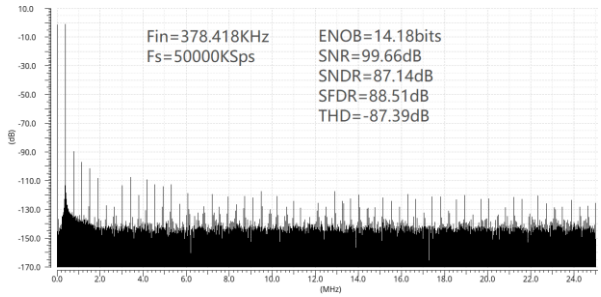

Figure 3. FFT of the conventional bootstrap switch

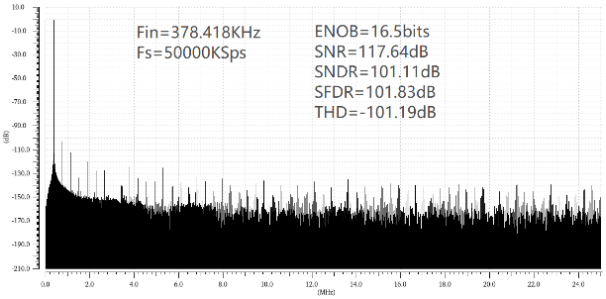

Figure 4. FFT of the proposed bootstrap switch

The ENOB of the proposed circuit and the conventional circuit are 16.5 bits and 14.48 bits, SDNR are 101.11 dB and 87.14 dB, and SFDR are 101.83 dB and 88.51 dB, respectively. The gate-source voltage of M2 is close to $2V_{DD}$ during sampling phase, and the transient simulation is shown in Figure 5. The gate-source voltage of M15 is the same. The layout and post-simulation FFT of the proposed circuit are shown in Figure 6 and 7. Compared with the pre-simulation, the ENOB loses about 1 bit.

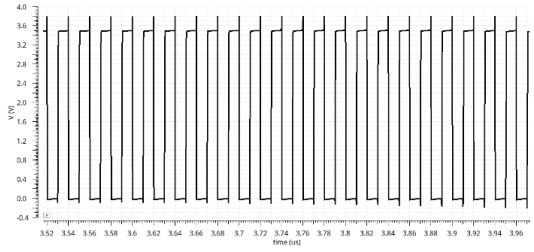

Figure 5. Gate-source voltage of M2

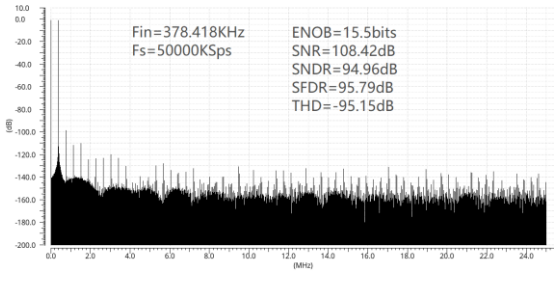

Figure 6. FFT of the proposed circuit

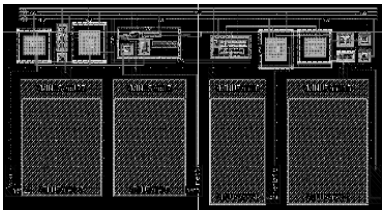

Figure 7. Layout of the proposed circuit

Table. 1 Performance comparison with references

	[3]	[4]	[5]	This work
Fs (MSps)	100	50	1	50
Fin (MHz)	0.2	0.34	0.1	0.38
ENOB (bits)	13.7	13.6	14	16.5
SNDR (dB)	84.4	83.7	86.9	101.1
SFDR (dB)	107	83.9	87.3	101.8

5. Summary

An improved complementary gate voltage bootstrap switch is propoesd in this paper. Compared with the negative voltage switch structure, the proposed structure reduces the change of the R_{ON} of the sampling switch by introducing the PMOS switch, and weakens the channel charge injection effect. The SNDR and SFDR are increased by 17.1% and 15.03% respectively.

Acknowledgments

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