Ring-oscillator-based timing generator for ultralow-power applications

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***Abstract*—Many integrated circuit functional blocks, such as data and power converters, require timing and control signals consisting of complex sequences of pulses. Traditionally, these signals are generated from a clock signal using a combination of flip-flops, latches and delay elements. Due to the large internal switching activity of flips-flops and due to the many, effectively unused, clock cycles, this solution is inefficient from a power consumption point of view and is, therefore, unsuitable for ultralow-power applications. In this paper we present a method to generate non-overlapping control signals without using flip-flops or a clock. We propose to decode and translate the internal states of a ring oscillator into the desired control signal sequence. We show how this can be achieved using a simple combinatorial logic decoder. The proposed architecture significantly reduces the switching activity and the capacitive load, largely reducing the consumed power. We show an example implementation of a 9-bit SAR logic utilizing our proposed method. Furthermore, we show simulation results and compare the power consumption of the example SAR implementation to that of a functionally identical flip-flop-based state-of-the-art ultralow-power SAR. We were able to achieve a 5.8x reduction in consumed power for the complete SAR and 8x for the one-hot generation sub-part.**

Keywords*—*timing generation, sequence generation, clock, state machine, ultralow power, low power, ring oscillator, SAR ADC

I. Introduction

With the need for ever lower power consumption of electronic devices, significant advances have been made to optimize the consumption of core function blocks such as power and data converters, switched capacitor networks, etc. This has resulted in a substantial reduction in the power consumed in those core function blocks, [4] [1], leaving the control and timing circuitry, such as oscillators and state machines, required to control the cores as significant power drains on the system level.

The availability of functional blocks consuming just a few microwatts has made it possible to use untraditional power sources such as energy harvesters, [3]. These ultralow-power systems are often highly integrated system-on-chip solutions featuring sensor and communication interfaces, power management units as well as data processing units. Mixed-signal/switched-mode blocks like these require timing signals composed of complex, often non-overlapping, sequences. A traditional approach to generate such timing signals is to derive them from a single-ended clock with $50\,\%$ duty cycle using a combination of flip-flops, latches and delay lines. However, due to the high switching activity of the clock, this approach is in general not power efficient. The frequency of the generated timing signals is fundamentally lower, or at most the same, as the frequency clock they are derived from, leading to inefficient use of clock cycles.

Our goal with the approach proposed in this paper is to generate timing and control signals in a power-efficient way. While we target ultralow-power applications, such as self-powered and battery-powered systems, our solution can be applied to low-power systems in general. Since the proposed approach is based on a ring oscillator architecture, the timing of the resulting control signals is inherently jittery. However, this is rarely a limitation for the systems we target.

II. Proposed oscillator-based timing generator

We propose a method to generate timing and control signals in which the use of a traditional clock and flip-flops is avoided. Instead, we utilize a ring oscillator with a twofold purpose: (1) to provide timing, much like in a traditional oscillator role, and (2) to store states, similar to how flip-flops and delay lines are used in a traditional timing generator. This concept is shown in Fig. 1 where a one-hot timing sequence illustrates the operation of the generator.

A. Oscillator State Decoding

Consider the ring oscillator and its internal state signals P_n shown in Fig. 1; it has N stages and 2N internal states. The oscillator switches between states in a circular fashion, much like a counter driven by a clock. We recognize two important time periods in the oscillator operation: (1) a major period at which the internal states repeat, we denote its length by T; and (2) a minor period which corresponds to the delay through one delay element, we denote its length by τ. The length of the major period is $2N\tau$.

By observing the outputs of the delay cells each oscillator state can be uniquely distinguished. Therefore, it is possible to design a combinatorial logic decoder which translates the oscillator states to essentially any timing sequence (C_m in Fig. 1) with a maximum length of $2N\tau$, a period of T and a shortest pulse width of τ. Due to the sparse coding of the oscillator states, the decoder needs a relatively shallow logic depth. In fact, control signals which have two transitions, consisting of single pulses per major period, can be decoded with a single two-input logic gate. This is illustrated in Fig. 1 where a one-hot (also called a traveling one) timing sequence is generated using a single layer of NOR gates with inputs connected across the delay elements. Notice that by connecting a NOR gate across more than one delay element we can generate pulses of length that is an integer multiple of τ. In order to generate signals with more than two transitions per major period we

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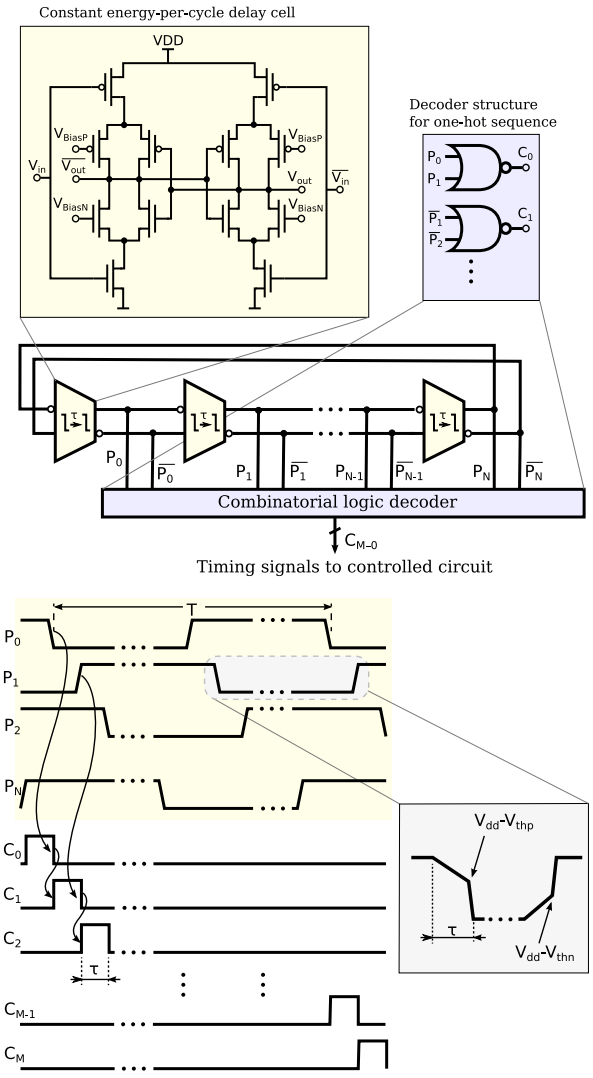


Fig. 1. Ring oscillator-based sequencer; example one-hot sequence.

need to use gates with more inputs or more than one layer of gates. It is important to note that the length of the generated pulses, that is the minor period, is dependent only on the delay of the delay cells and not on the frequency of the ring oscillator. This is in contrast to the traditional solution where the length is directly determined by the clock period.

In case non-overlapping is required between the output phases it can be achieved by adding a guard transistor to the standard logic gates of the decoder as shown in Fig. 2. The gate of transistor M_{guard} is driven by the preceding phase, this prevents a low-to-high transition in the current timing phase to occur before the previous (guard) phase has already transitioned from high to low. Furthermore, the guard transistor prevents short circuit current to flow when the output transitions from low to high, thus reducing the dynamic power consumption.

B. Ring oscillator architecture

Since the ring oscillator is a central part of the proposed timing generator, in order to achieve an overall high power

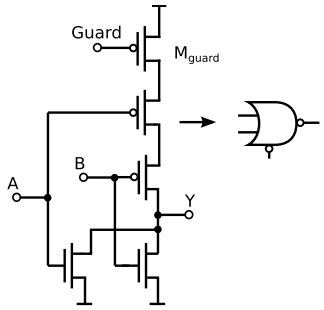


Fig. 2. NOR gate with a pull-up enable guard input for generating non-overlapping timing signals. The guard signal is driven by the preceding control phase.

efficiency it is essential to keep the power consumed by the oscillator at a minimum. In [2] Lee et al. propose a low-power constant-energy-per-cycle delay cell and show that from a power consumption point of view and for low frequencies it is advantageous to use differential delay cells with a brake-before-make operation in the ring oscillator. This is because at low oscillation frequencies the traditional delay cells based on current-starved inverters consume excessive amount of short-circuit current. Furthermore, compared to a general oscillator application, using differential delay elements to construct a timing generator remains advantageous even at frequencies that would otherwise require single-ended circuits. There are two reasons for this: (1) differential delay elements can form a ring oscillator with an even number of cells making it possible to optimize the number of states; and (2) having the inverted representation of the state signals allows a simpler and, therefore, more power efficient decoder implementation.

Since the ring oscillator determines the timing performance, such as jitter and frequency accuracy it should be carefully designed and biased. For applications requiring accurate frequency, the oscillator can be trimmed.

Due to the above reasons, we employ the delay cell proposed in [2] in our timing signal generator. Figure 1 shows the schematic of the delay cell, as well as the general shape of the output signal waveform. Notice that two phases can be distinguished in the output transition of the delay cell: a delay phase where the voltage is slowly ramping up or down; and a switching phase where the voltage is rapidly pulled towards supply or ground, Fig. 1. This latching behavior is especially useful as it allows conventional CMOS logic gates to be driven directly without causing wasteful short-circuit current. This is crucial for low-frequency operation where a conventional delay-cell might transition for a long time causing prohibitively large power consumption. Furthermore, the latching behaviour guarantees the signal integrity inside the ring oscillator.

III. Power Consumption and Implementation Example

In order to analyze the power consumption of the proposed architecture, as an example, we use a conventional successive-approximation-register (SAR) architecture based on flip-flops and latches, as shown in Fig. 3a. We also implement the same SAR functionality with the proposed method and compare the simulated power consumption of both.

The conventional SAR consists of two layers, a flip-flop-based one-hot sequencer and a latch-based memory layer for storing the comparator results. This two-layer architecture has been used previously for building ultralow-power SAR ADCs [4]. Notice that the sequence generated at the outputs of the flip-flop layer is, indeed, that of a one-hot counter. We implement this layer by using our proposed approach to decode a ring oscillator's internal states. For this example we chose to use a SAR for a 9-bit ADC and we also include the generation of the sample signal for a total of N=10 output phases and control signals. The resulting circuit is shown in Fig. 3b. We are able to entirely remove the clock signal needed to drive the flip-flops, furthermore, we substitute them with NOR gates. This significantly reduces the switching activity as well as the total switched capacitance. Since, as discussed previously, we can make the one-hot sequence non-overlapping by adding a guard transistor in the decoder gates, thus avoiding the race condition that may occur in the conventional implementation of Fig. 3a.

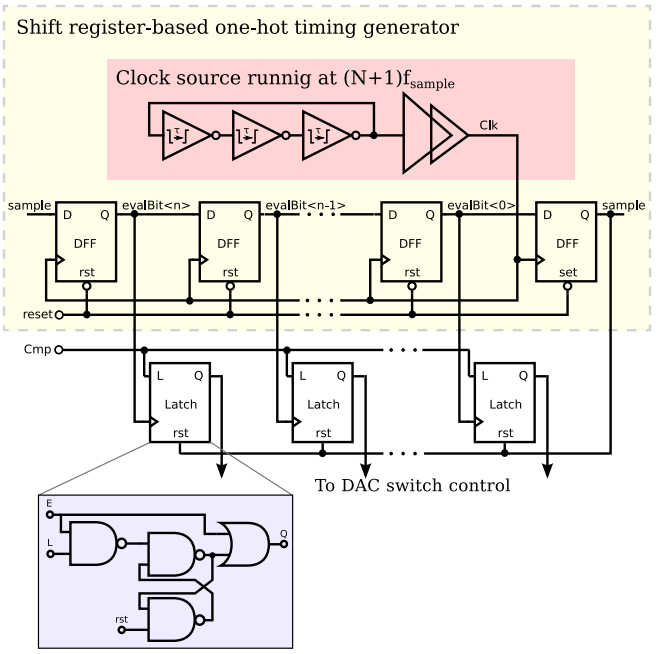
Due to the significantly different switching activities and capacitive loads of the two one-hot sequencer implementations it is hard to analytically estimate the potential power savings. Therefore, we simulate both implementations shown in Fig. 3 and compare the results.

Since the power for the clock generation for the conventional architecture can be significant, in our example, we include a ring oscillator generating a clock, as well as a buffer driving the flip-flops. In order to make a fair comparison, we use the same delay cell described in [2] to build the oscillators for both cases. However, since the proposed timing generator uses all available oscillator states, its oscillator needs to be tuned at 2N times lower frequency compared to the clock of the conventional architecture. Furthermore, in order to keep the power consumption low for the conventional SAR we use only three delay cells and we tune the bias current to achieve the desired frequency. On the other hand, since the number of delay cells for the proposed architecture is required to be at least one for every two output phases we need five for our example. We use a $1\,\mu s$ bit-evaluation time which requires $1\,MHz$ oscillation frequency for the conventional implementation and $100\,kHz$ for the proposed one. The resulting sequence, which is a typical SAR ADC control sequence, is identical in both cases. The memory/latch layer is also the same, therefore, we implement both with the topology shown in Fig. 3a.

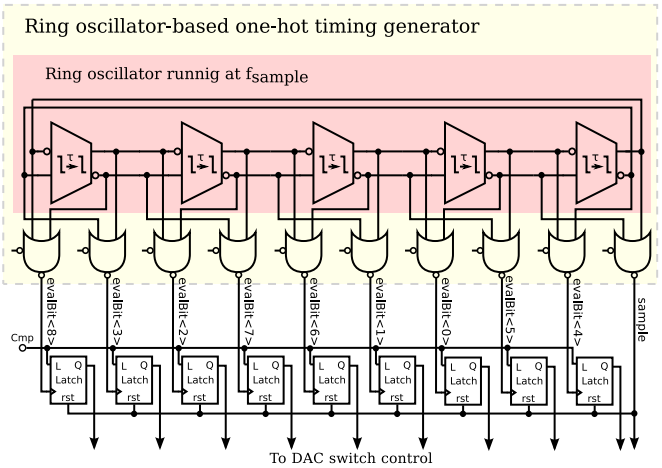
For our simulations we use a $0.18\,\mu m$ CMOS technology, a power supply of $1.2\,V$ and nominal process corner at a temperature of $27\,^{\circ}C$. All transistors are minimum size, except the current sources in the delay cell which are $6\,\mu m$ long and $500\,nm$ wide.

A. Simulation results

Table I shows a summary of the simulated power consumption. A significant reduction is achieved for the one-hot sequence generator part. This is, on the one hand, due to the reduction of the oscillation frequency, which is divided by the number of one-hot phases, and on the other, due to the removal of the flip-flops. As expected, the energy consumption per cycle per delay cell remains approximately the same – $9.3\,fJ/cycle$ for the conventional architecture and $8.2\,fJ/cycle$



(a)



(b)

Fig. 3. Two successive-approximation-register architectures: (a) conventional, flip-flop-based SAR; (b) SAR based on the proposed method of decoding the internal states of a ring oscillator.

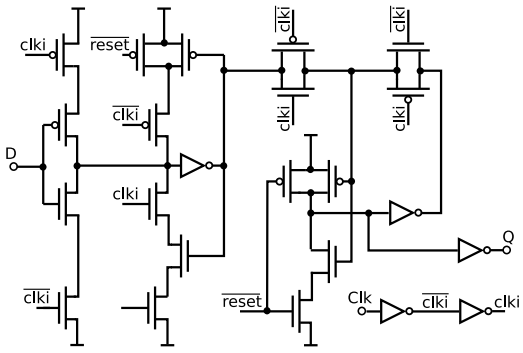


Fig. 4. The flip-flop used to simulate the power consumption of the conventional SAR. All transistors are minimum size.

for the proposed. The relatively high consumption of the shift register can be explained by the large number of, essentially wasted, transitions of the clock. While, for every major cycle, there are in total four transitions at the inputs of each of the NOR gates of the decoder, there are ten clock cycles (20 transitions) at the clock input of the flip-flops. Furthermore, the flip-flops present a significantly higher capacitive load. It should be noted that at a fixed minor period, the power consumption of the proposed architecture depends linearly on the number of output phases, while that of the conventional – quadratically. The proposed architecture produces an output transition for every two decoder input transitions, this remains true even if the number of output phases is changed. The slight increase in power consumed by the latches can be explained by the somewhat longer rise/fall times at the output of the NOR gates used to drive them, which leads to a corresponding increase in the short-circuit current.

TABLE I. SIMULATED POWER OF TWO 9-BIT SARS USING THE PROPOSED OSCILLATOR-BASED AND A CONVENTIONAL FLIP-FLOP-BASED TIMING GENERATORS.

Power consumption component	Proposed implementation, nW	Flip-flop-based implementation, nW
Oscillator	41	281
Decoder / shift register*	9.6	126
Latches	22	19
Total	73	426
Total, one-hot generation	**51 nW**	**407 nW**

* Including clock buffer for the flip-flop based implementation

B. Conventional clocking

It should be noted that removing a conventional clock signal as we did in our SAR example may not always be easy when a larger, more complete system is considered. However, it could be argued that if a conventional clock is still needed in the system then more states can be integrated into the oscillator-based timing generator, potentially eliminating the need for a conventional clock altogether. Even if conventional timing is still required, reducing the capacitive load on the clock by utilizing the proposed solution is still beneficial as can be seen in Table I. When ultralow-power operation is a requirement such increase in system complexity could be justified.

IV. CONCLUSION

In this paper we present a novel, to the best of our knowledge, approach for generating timing and sequencing control signals. We recognize that the internal states of a ring oscillator can be uniquely distinguished and, therefore, mapped to timing signals with a desired sequence and timing. We were able to achieve this using a simple, yet flexible, combinatorial logic decoder. We showed that by utilizing our proposed architecture it is possible to significantly reduce the power consumption relative to a traditional flip-flop-based architecture run by a clock. As an example, we implemented a successive-approximation-register with our technique as well as with a conventional flip-flop-based approach. The simulation results suggest a 5.8x decrease in consumed power, for the complete SAR, and a 8x for the one-hot generation part of the SAR. The reduction in power consumption is due to the significantly lower oscillation frequency as well as due to the reduction in switching activity and load for the proposed solution.

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