Pre-Layout Simulation Results for 10- Bit Monotonic SAR ADC

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Capacitor Sizing For DAC

➔ Mismatch limitation
➔ Speed Limitation
➔ Noise Limitation
➔ Architecture Dependence (Switching Techniques)
➔ Effects like Charge injection, Kickback noise From Comparator

Sizing of Capacitors (Effect of Mismatch):

For a Binary Weighted DAC: $\sigma_{DNL,MAX} = \sqrt{2^N - 1}\frac{\sigma_u}{C_u}LSB$ **>** $\sigma_{INL,MAX} = \sqrt{2^{N-1}}\frac{\sigma_u}{C_u}LSB$

For a MIM Capacitor,

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{K_\sigma}{\sqrt{A}}$$

$$C = K_C \cdot A$$

For High Yield, $3\sigma_{DNL,MAX} < 0.5$ LSB

$$C_U = 18 \cdot (2^N - 1) \cdot K_\sigma^2 \cdot K_C$$

K_σ = matching Coefficient

K_C = capacitor density parameter

For 65nm Process,
K_C = 1.6f F to 1.9f F/μm^2

For **$K_\sigma \leq 0.5\%$** μm, we get $C_u \approx 1$fF

Process Sets the lower limit for C_u

Ref:- Design of Ultra-Low-Power Analog-to-Digital Converters [D. Zhang, 2012]

Sizing of Capacitors(Effect of Speed and Thermal Noise):

From Track Bandwidth, with settling error <0.5LSB

$$e^{-\frac{t}{R_{ON}C_S}} < \frac{1}{2^{N+1}}$$

$$f_{3dB} > \frac{ln2 \times (N+1)}{\pi} f_S$$

➔ $C_S < \frac{1}{2 \cdot R_{sw} \cdot ln2 \cdot (N+1) f_S}$

From Thermal Noise requirement, with Thermal noise < 0.25LSB

$$\overline{V_q^2} = \frac{V_{FS}^2}{12 \cdot 2^{2N}} > 4\frac{KT}{C_S}$$

➔ $C_S > \frac{48 \cdot KT \cdot 2^{2N}}{V_{FS}^2}$

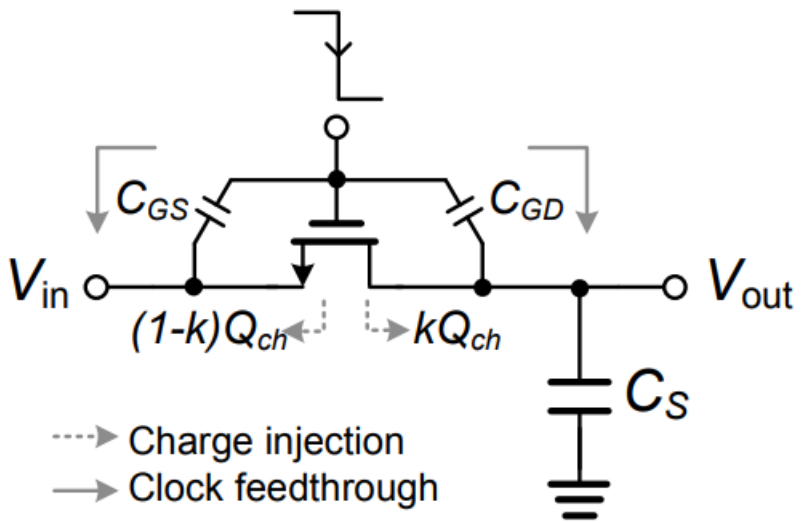
With N = 10, gives C_S > 208fF

Ref:- Design of Ultra-Low-Power Analog-to-Digital Converters [D. Zhang, 2012]

Sizing of Capacitors(Effect of Charge injection and Clock Feedthrough):

$$\Delta V_{e,N} = -\frac{kW_N L_N C_{OX}(V_{DD} - V_{THN} - V_{IN})}{C_S} - \frac{C_{GD,N}}{C_S + C_{GD,N}} V_{DD}$$

$$\Delta V_{e,P} = \frac{kW_P L_P C_{OX}(V_{IN} - |V_{THP}|)}{C_S} + \frac{C_{GD,P}}{C_S + C_{GD,P}} V_{DD}$$

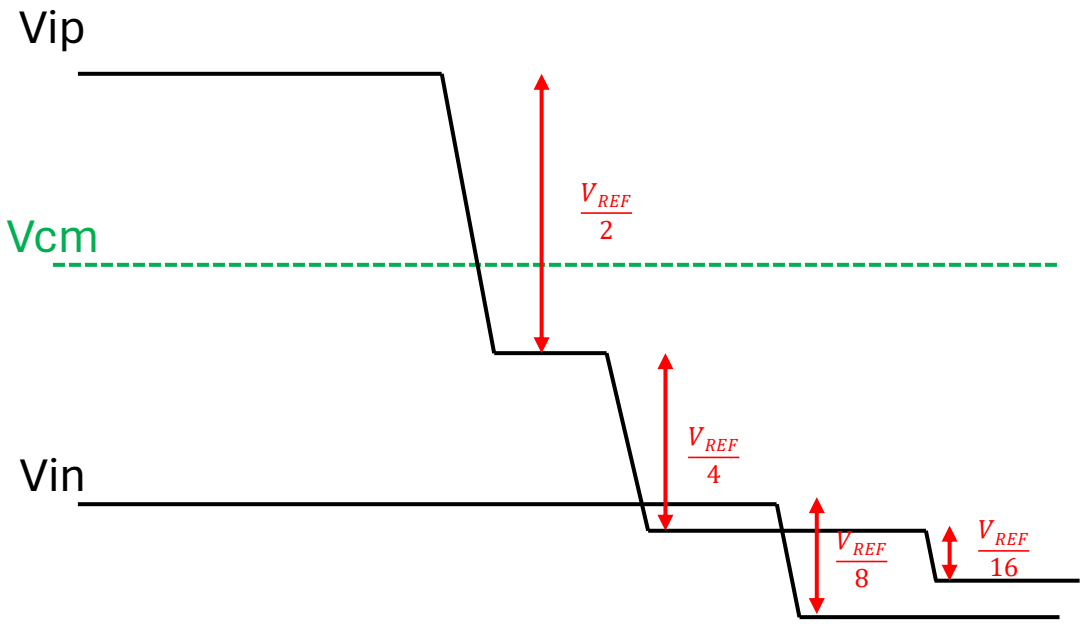


Ref:- Design of Ultra-Low-Power Analog-to-Digital Converters [D. Zhang, 2012]

DAC Switching Techniques (Monotonic):-

1. Set and Down Architecture
2. ERMS
3. V-cm based monotonic switching

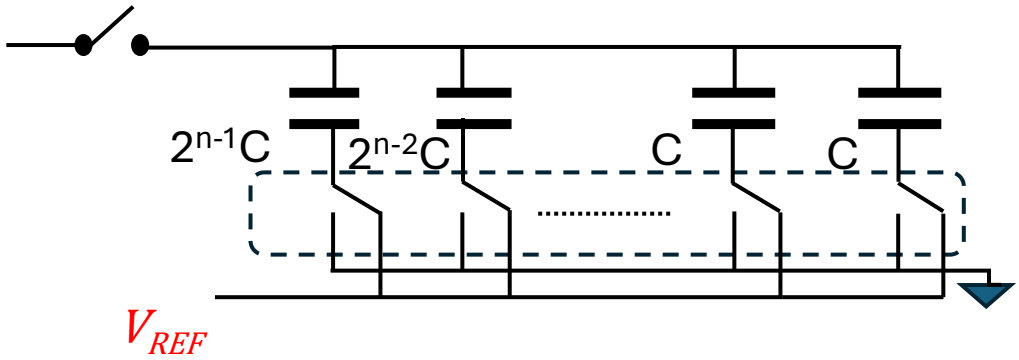
Set and Down (Monotonic) Architecture:



➔ It is a simple architecture, based on comparison and reducing the Higher node potential by binary weighted V_{REF} , till the binary weighted V_{REF} converge to LSB. It is a differential architecture. Binary weighted capacitor array for bottom DAC is shown below. Once the Input voltage is sampled onto top plate of every capacitor with bottom plate connected to V_{REF} , then sample switch turns off and comparison phases start.

➔ For the MSB phase, let's assume Vip > Vin, so bottom plate of MSB cap of upper DAC array is switched from VREF to gnd. Which Reduces Top plate voltage by V_{REF} / 2.

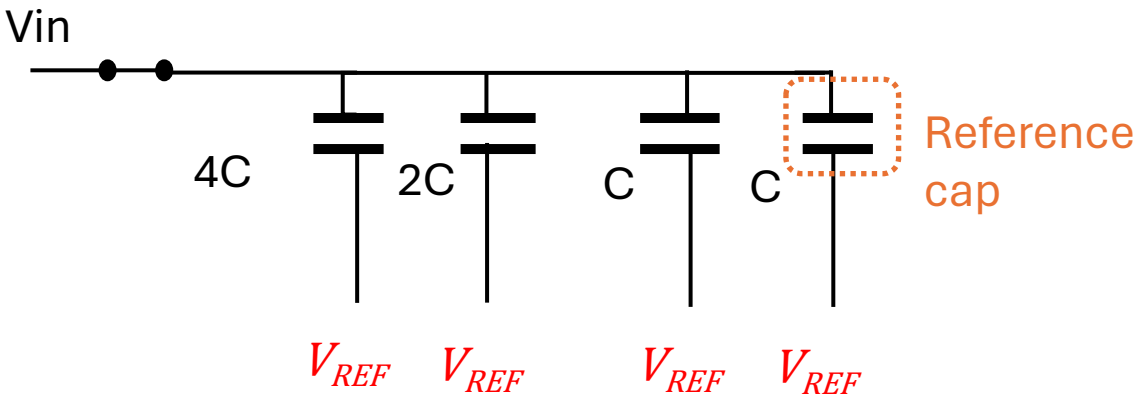
➔ Similarly for the other bits, comparison and conversion are Performed.



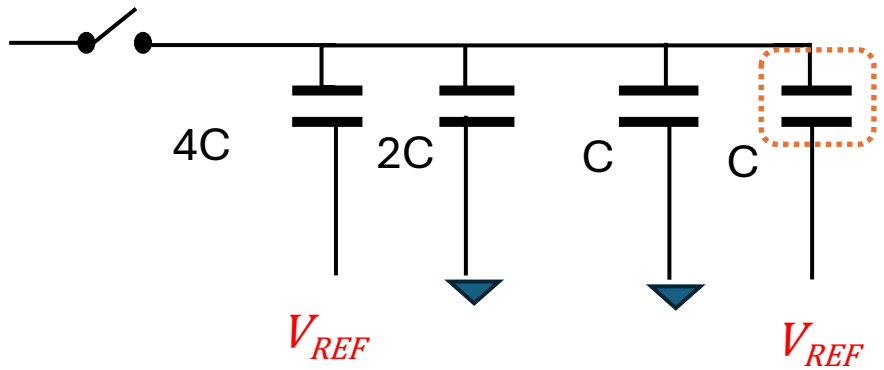
Average Switching Energy:- $$E_{\text{avg,mono}} = \sum_{i=1}^{n-1} (2^{n-2-i}) C V_{\text{ref}}^2$$

Example: How Voltage across Top plate of capacitor varies (4-bit DAC)

Sampling Phase



End of Conversion Phase



$Q1 = 8*C*(Vin - V_{REF})$

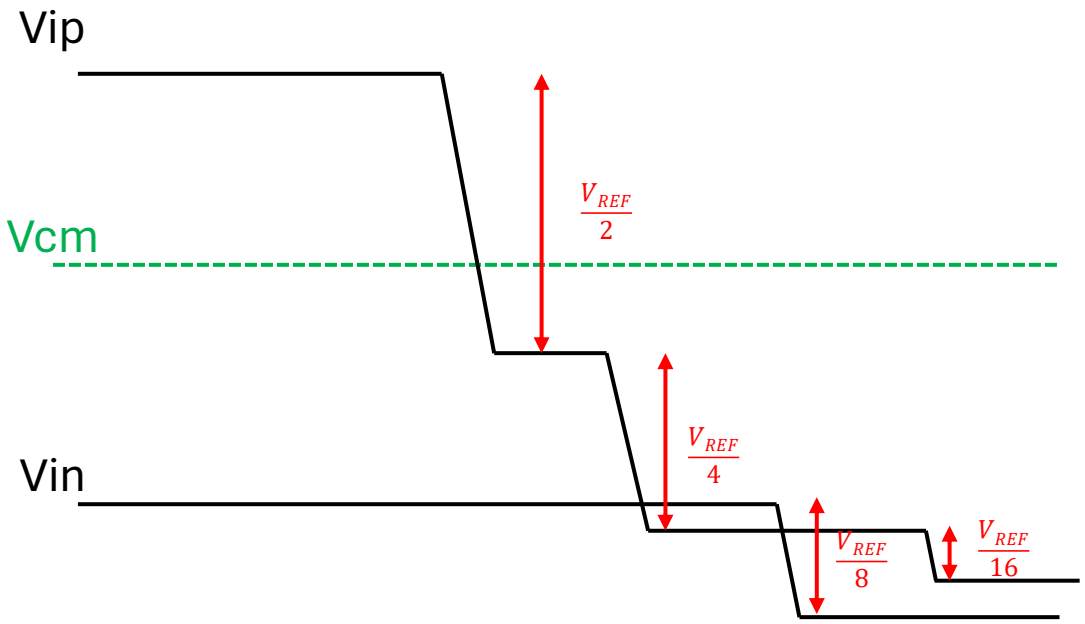
$Q2 = 5C*(V-V_{REF}) + 3*C*V$

From Q1 =Q2, (since total charge is not lost during conversion)

$$8V = 8*Vin - 3*V_{REF}$$

$$\rightarrow V = Vin - \frac{3}{8} * V_{REF}$$

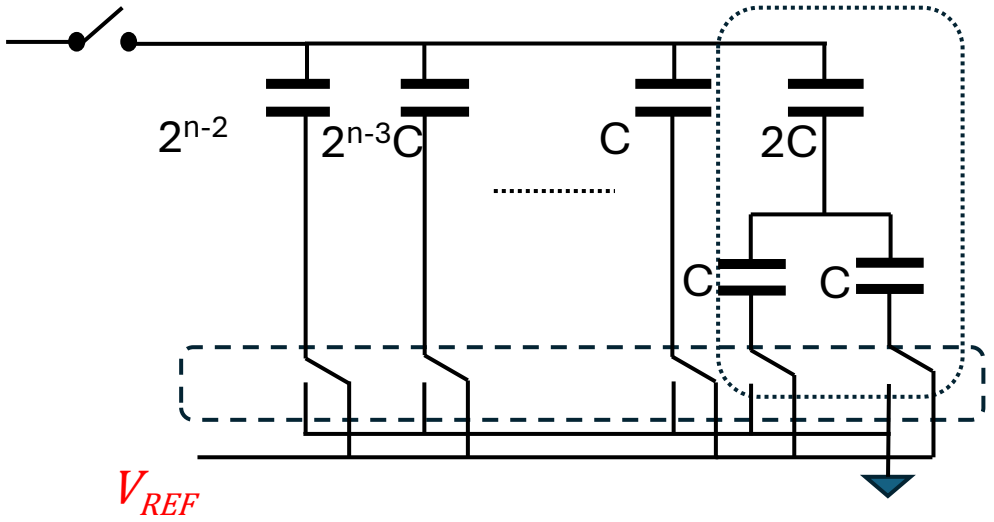
ERMS: Energy efficient Reference free Monotonic capacitor switching scheme



➔ Switching scheme is same as monotonic but reference is converted to C-2C dummy capacitor which helps in adding 1 bit accuracy and reduces overall capacitance and switching energy .

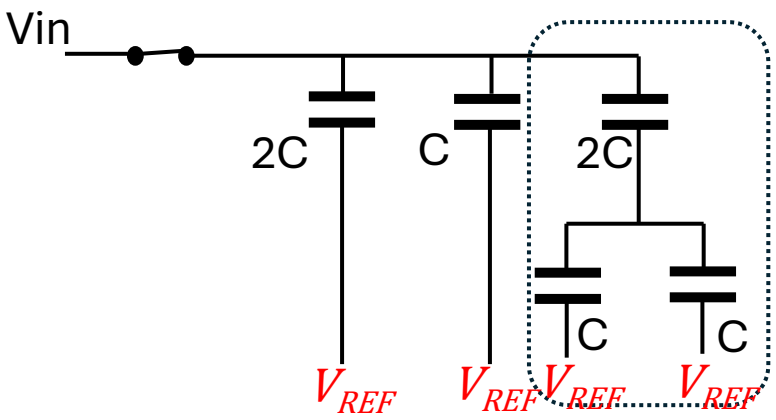
Average Switching Energy:-

$$E = \left(\sum_{i=1}^{n-2} 2^{n-3-i} + \frac{1}{2}\right) CV_{REF}^2$$

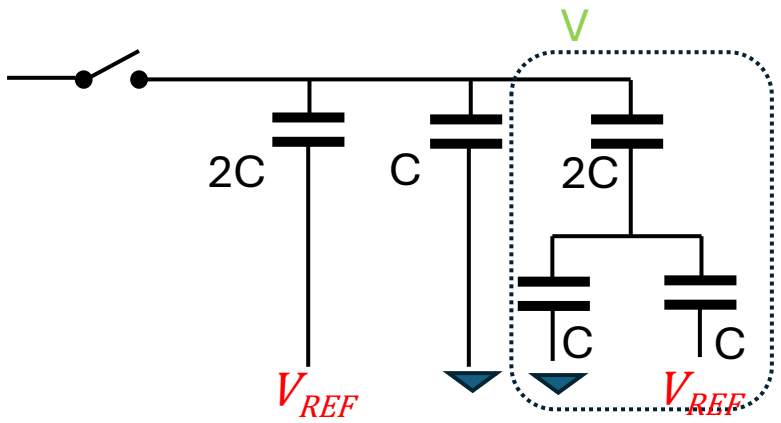


Example: How Voltage across Top plate of capacitor varies (4-bit DAC)

Sampling Phase



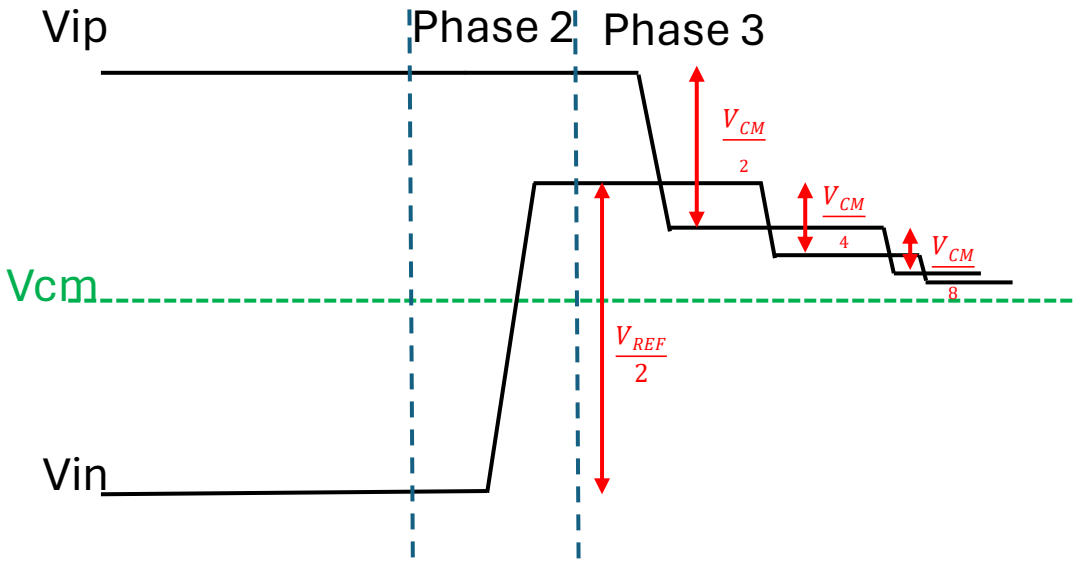
End of Conversion Phase



From Principle of superposition,

We get, ➔ $V = Vin - \frac{1}{2} * V_{REF} + \frac{1}{8} * V_{REF} = Vin - \frac{3}{8} * V_{REF}$

Vcm Based Monotonic Switching



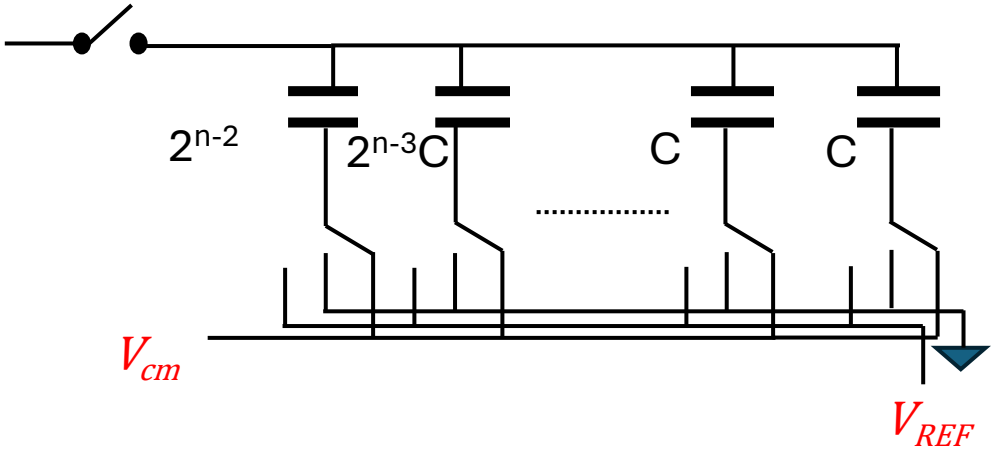
Choosing $V_{REF} = 2*V_{CM}$

➔ This Scheme has 3 Phases

Phase 1: Sampling Phase
Top plate is connected to Vip/Vin. Bottom Plate is connected to Vcm.

Phase 2: MSB Phase
Perform the comparison and replace the bottom plate of DAC of the lower potential side with V_{REF} . (This increases the lower Potential Top plate Voltage level by V_{REF} / 2).

Phase 3: Other Bits (same as monotonic)



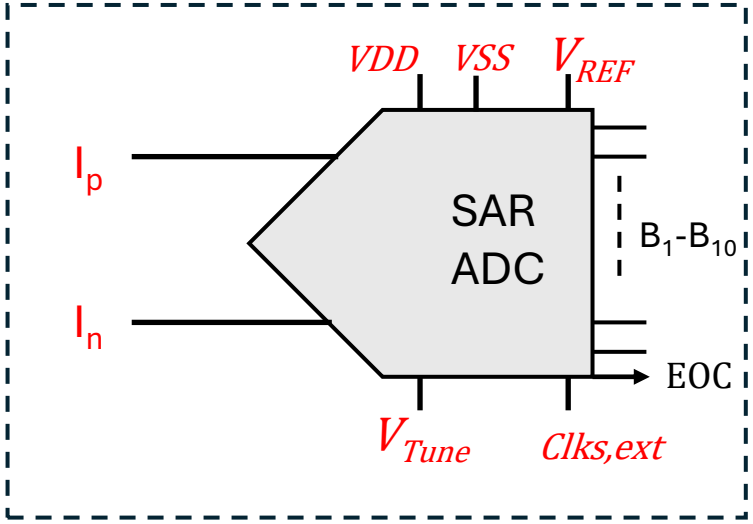
Average Switching Energy:- $E_{avg} = \sum_{i=1}^{N-2} (2^{N-i-5}) C V_{REF}^2$

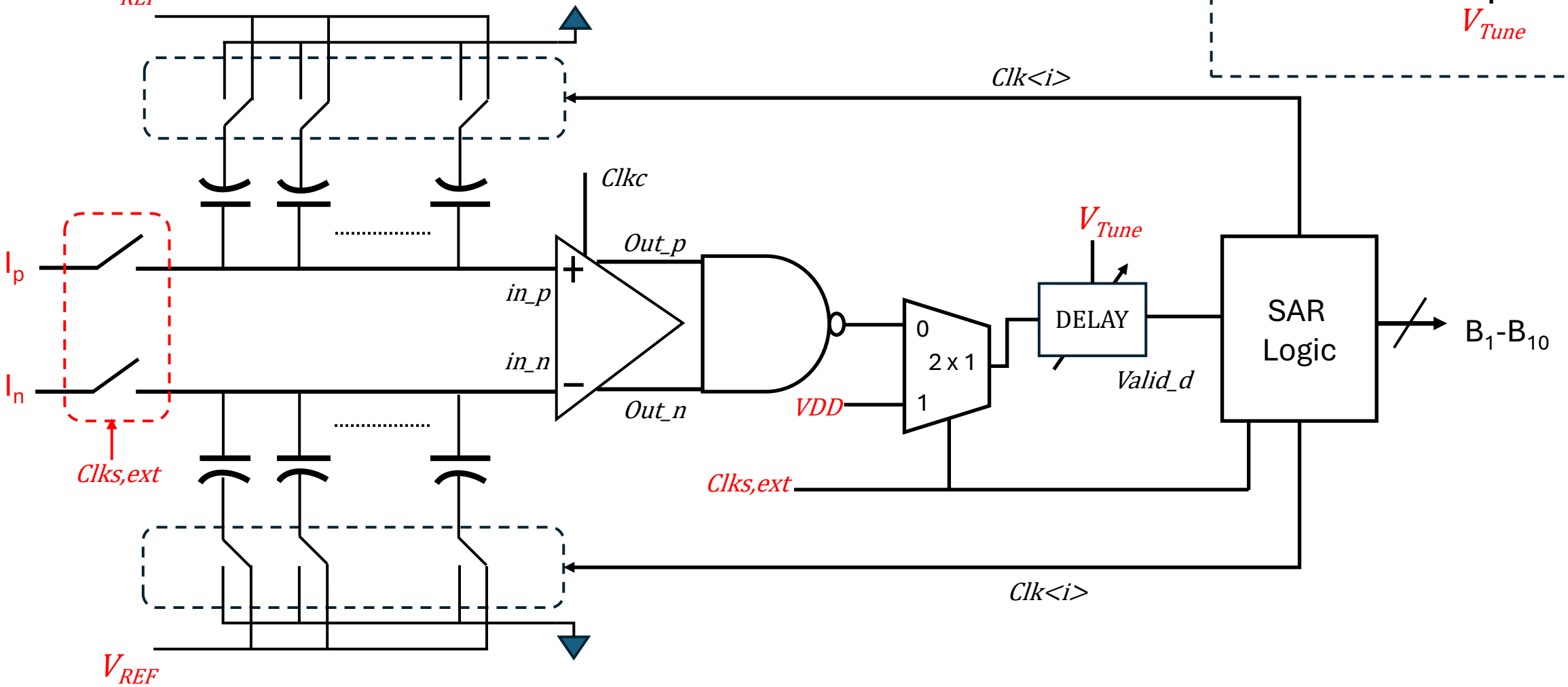
Comparison:

[10bit}	Unit Capacitors	Switches	Avg. Switching Energy (CV^2_{REF})
Conventional (Bi-directional)	2048	68	1363.3
Monotonic [Set and Down]	1024	40	255.5
ERMS	518	40	128
Vcm - Monotonic	512	-	31.88

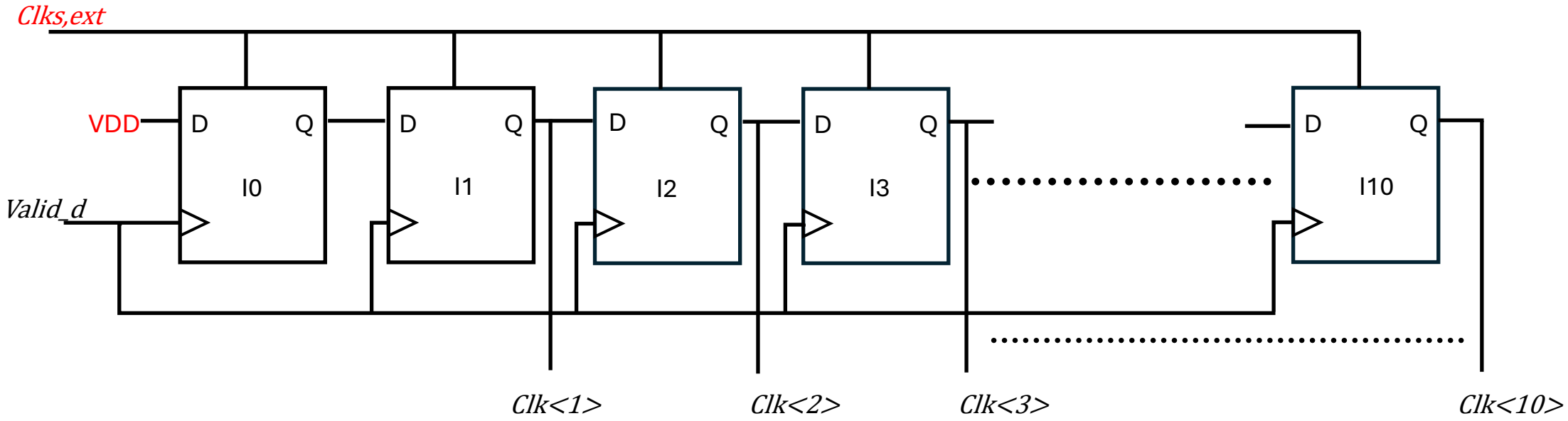
Block Diagrams And Results

Asynchronous SAR ADC Block Diagram



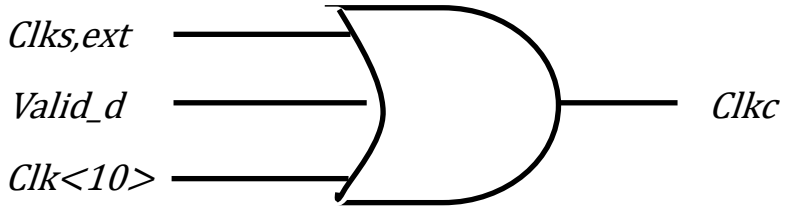


Shift Register For Asynchronous Control Signal Generation

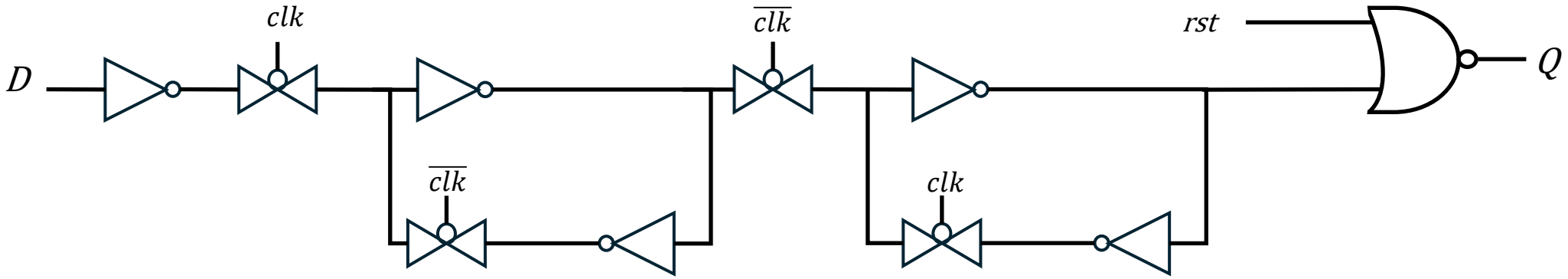


Function:

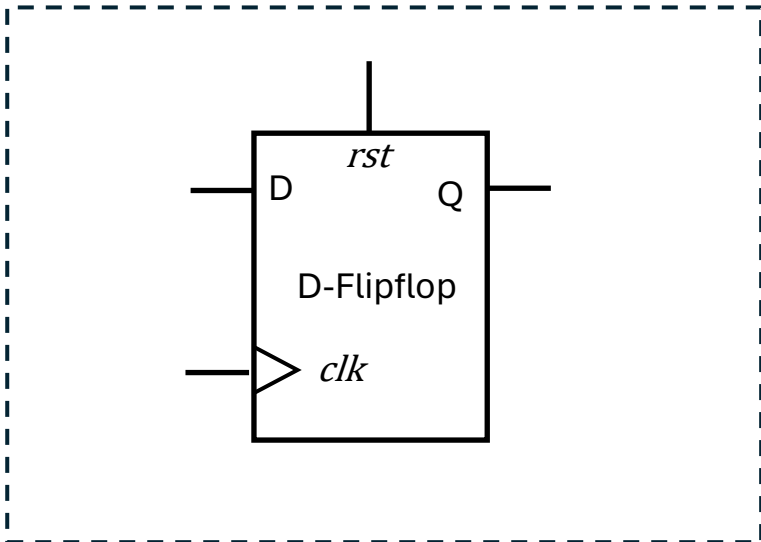
➔ For every valid_d clock cycle it generates a control signal in a sequential fashion.



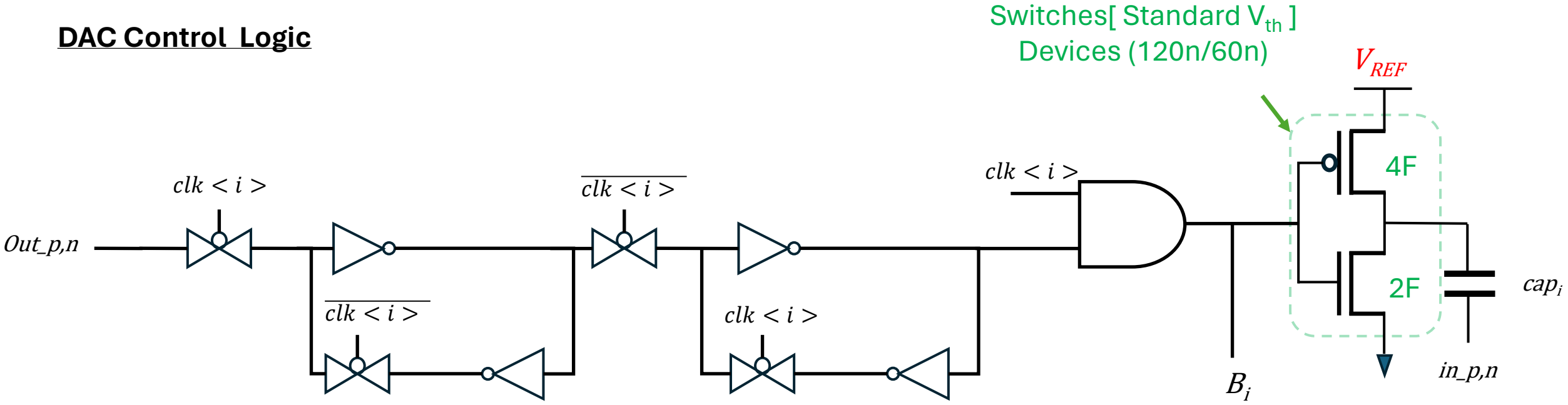
D-Flipflop with rst For Shift Register



Minimum size transistors : 120n/60n (high V_{th})
Inverters use stack of 2 pmos (minimum size) to reduce leakage.



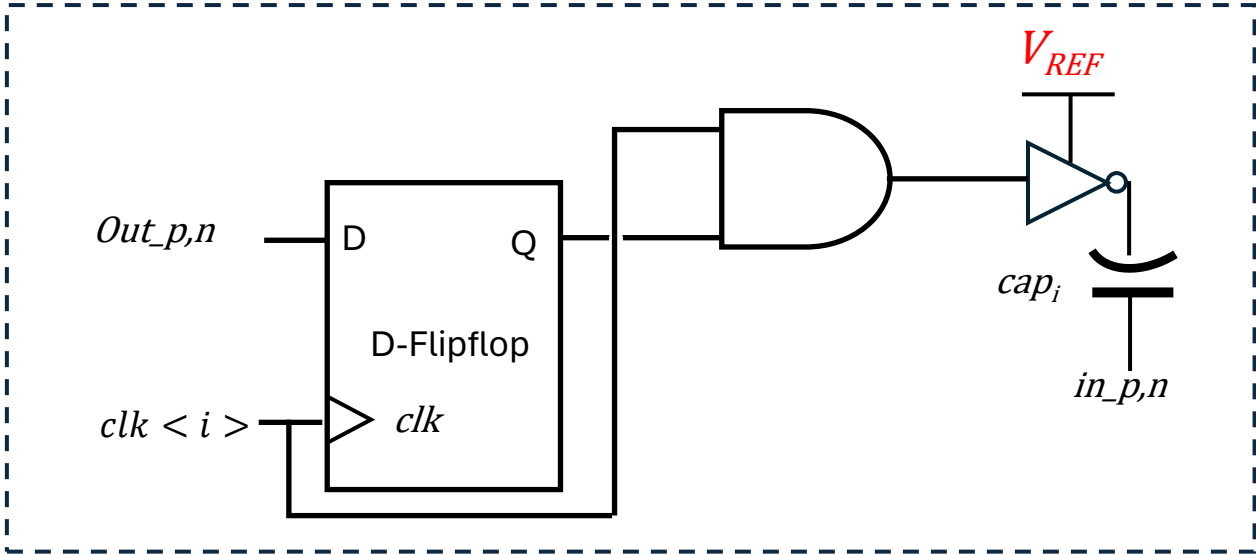
DAC Control Logic

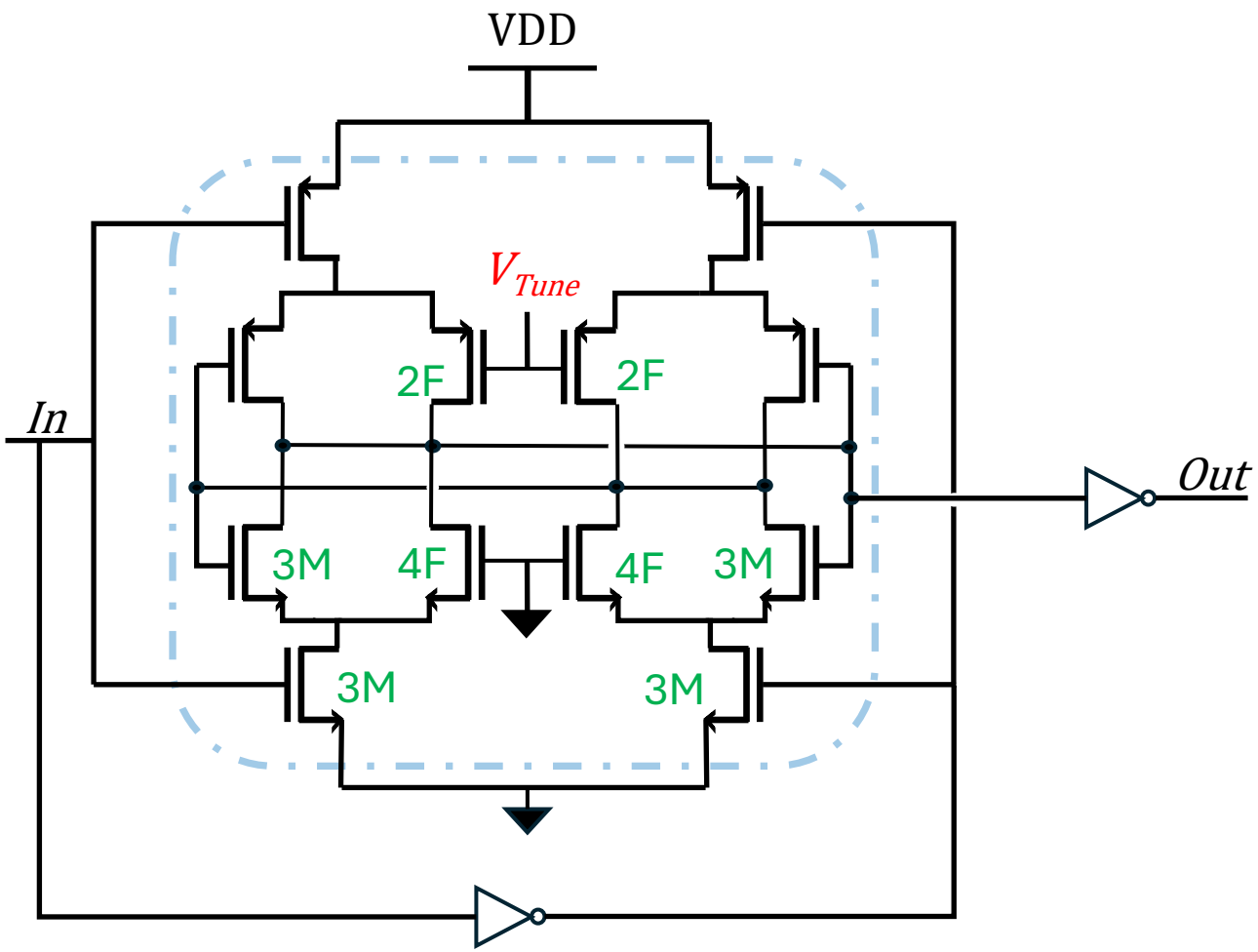


Function:

➔ It is responsible for generating valid digital code word for the sampled differential signal.

➔ It generates bit[i] at the rising edge of clk<i>, by identifying the output of comparator and respectively switches the cap_i bottom plate node voltage to gnd if comparator is high, else remains connected to V_{REF} .



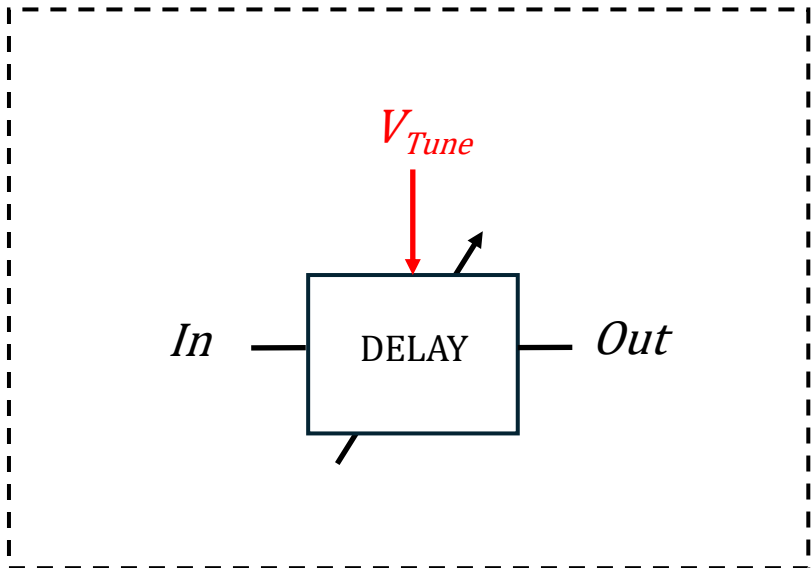


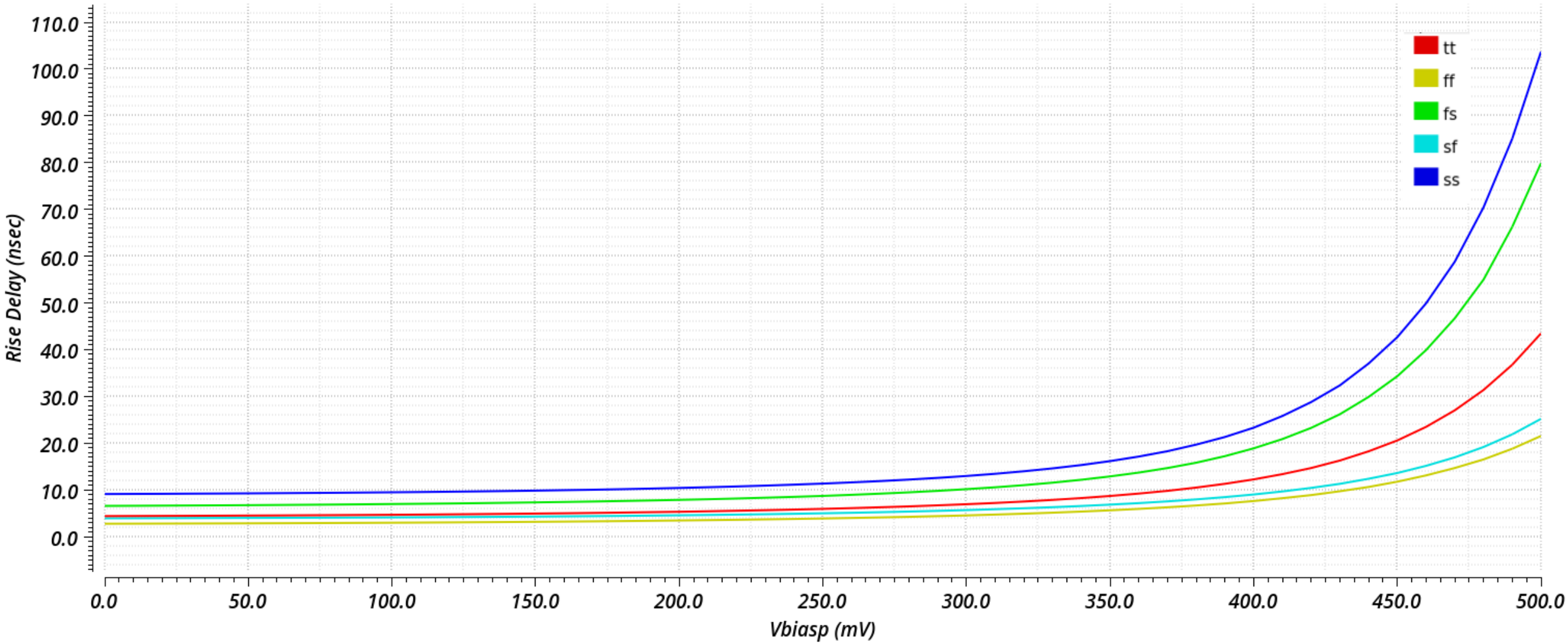
Delay Cell

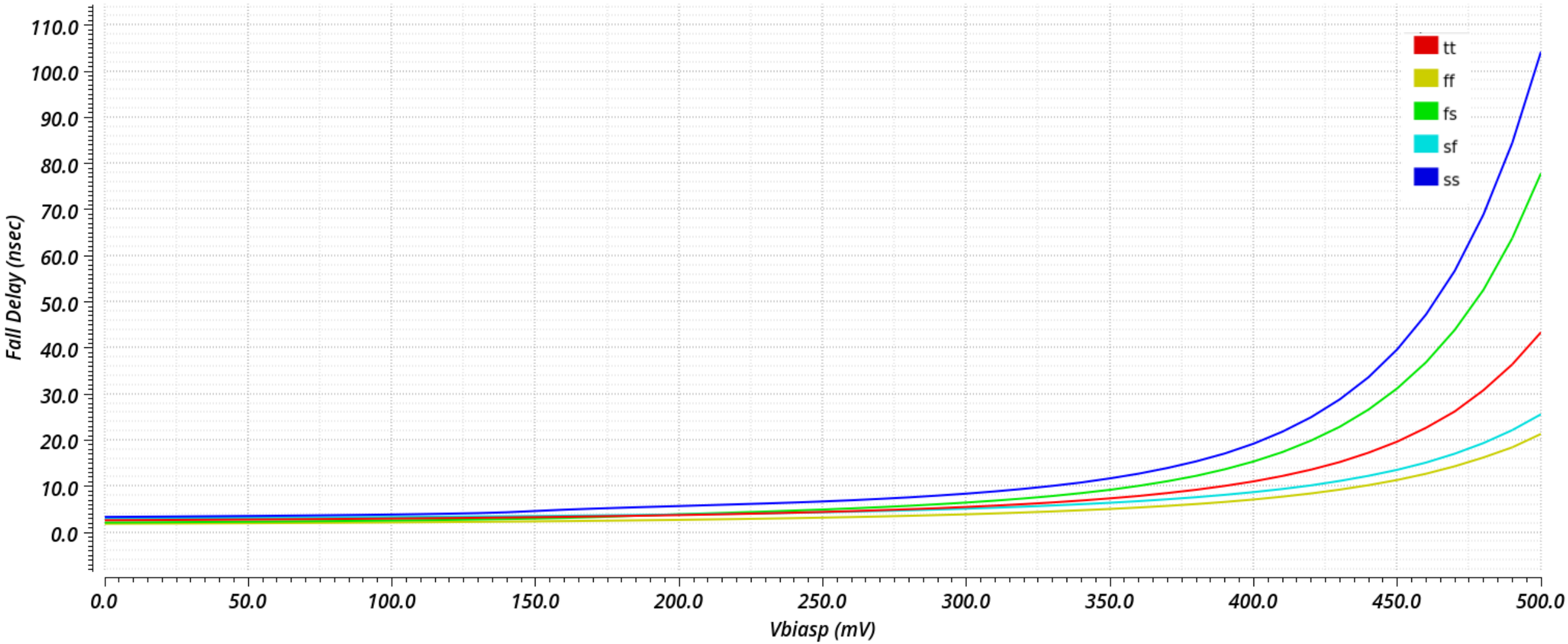
Core of delay cell uses low V_{th} MOS cells (W/L =480n/480n).

➔ Delay is needed to ensure DAC capacitors settle during switching and to ensure comparator has enough time to compare and regenerate.

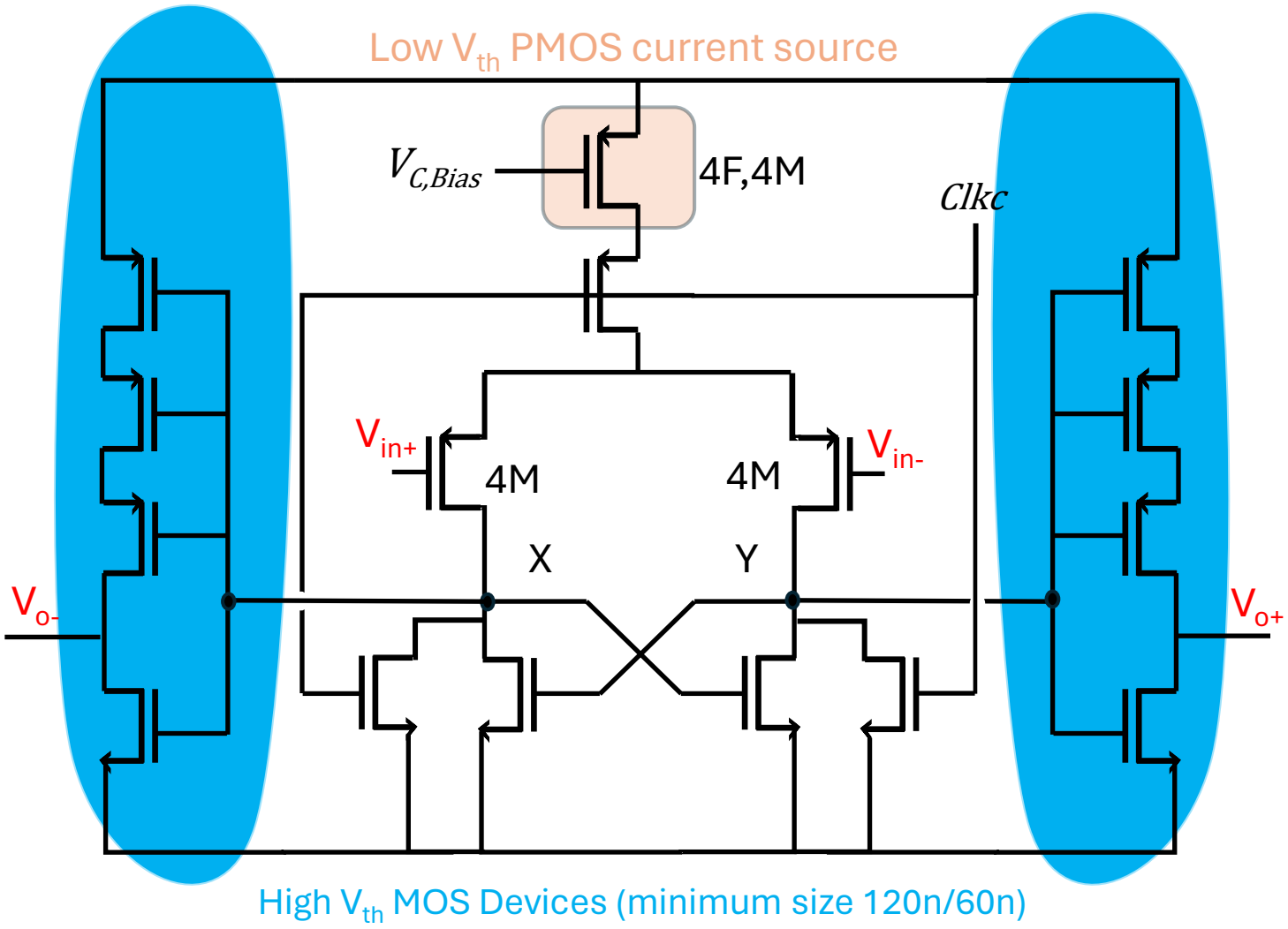
➔ Generating delay is crucial in Asynchronous SAR ADC.

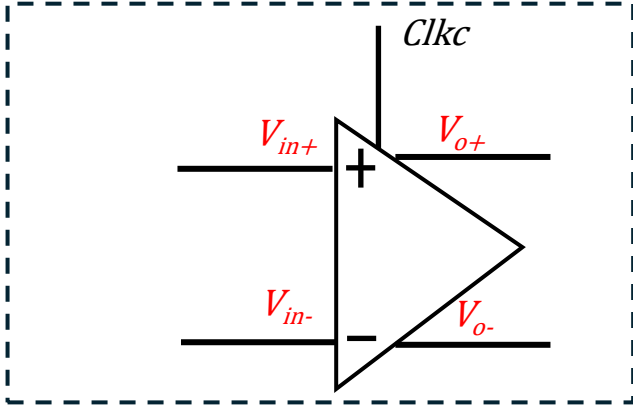



Rise Delay (nsec)
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Vbiasp (mV)
tt
ff
fs
sf
ss


Fall Delay (nsec)
110.0
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Vbiasp (mV)
tt
ff
fs
sf
ss

Dynamic Comparator(Strong Arm Latch)





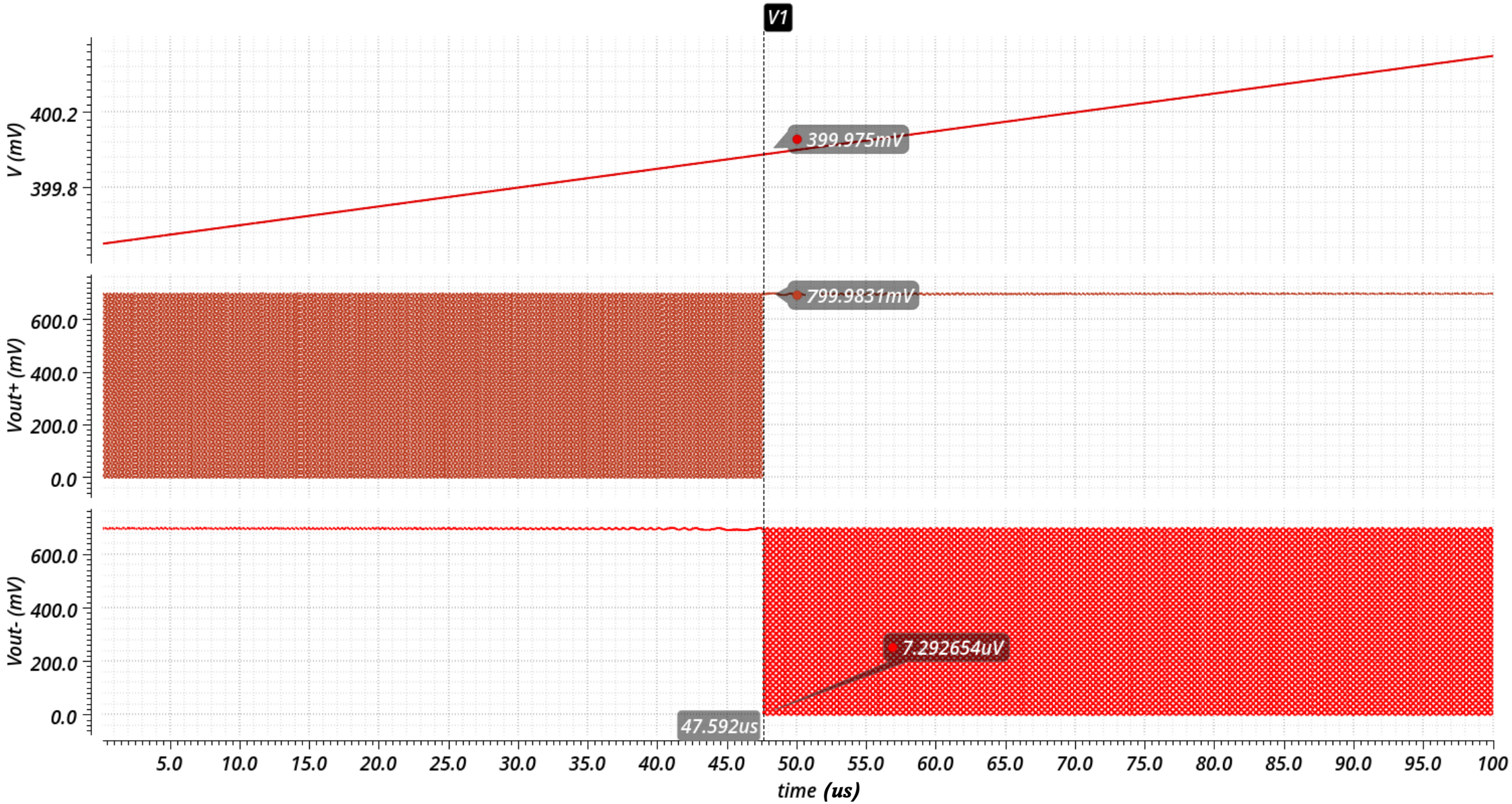
Pre-amp latch stage MOS devices have W/L = 200n/200n.

Principle of operation:

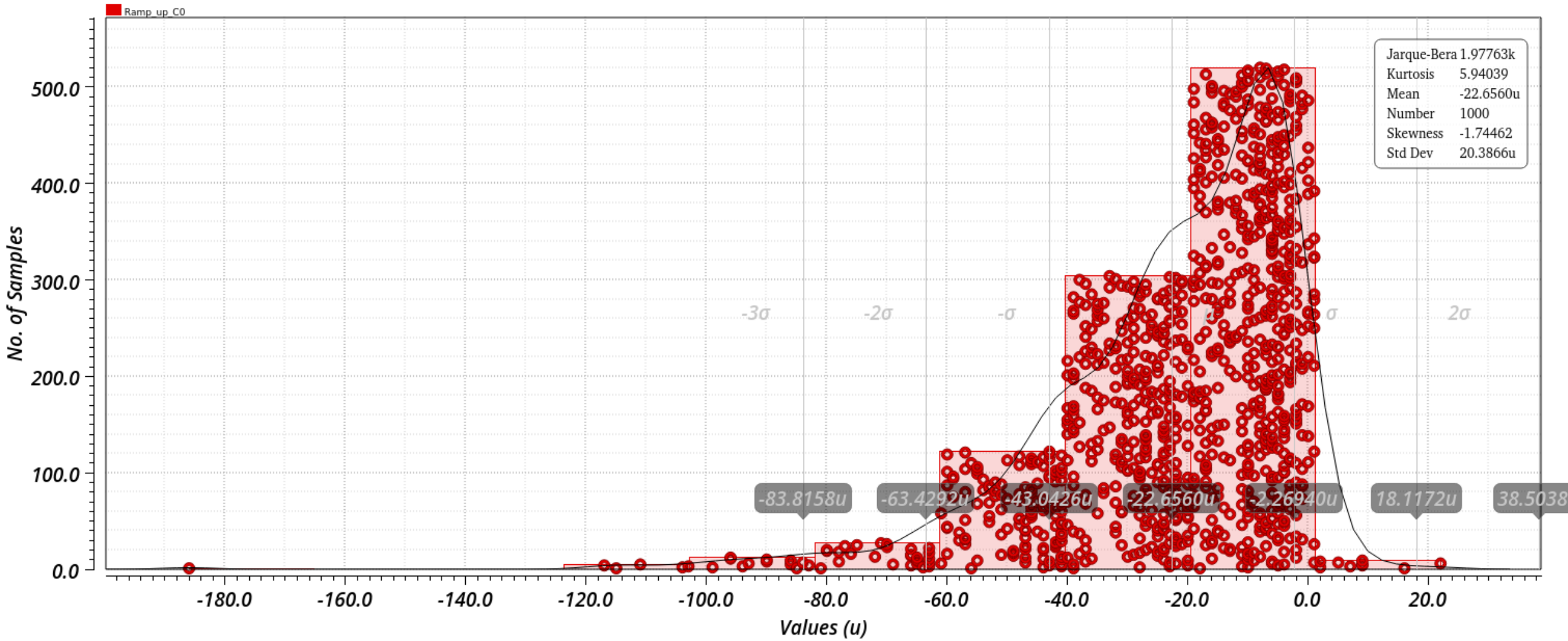
➔ Incoming differential voltage signal is amplified by differential pair to a moderate value, then cross coupled nMOS kicks in and regenerates the X,Y nodes to high/low by the action of positive feedback.

➔ This regeneration action takes time, which can be controlled by PMOS current source.

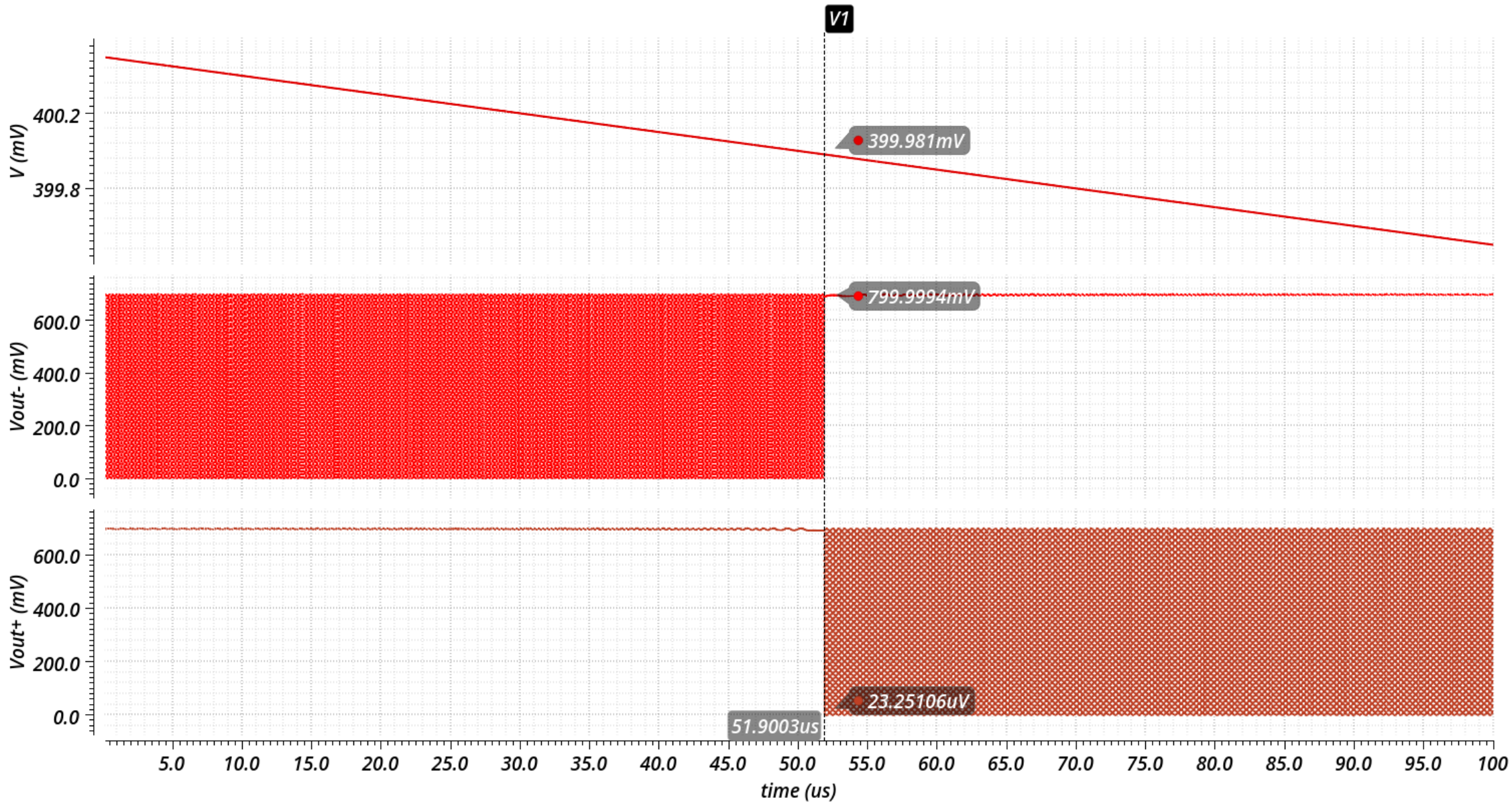
Ramp Up Test (load 10fF with Vin- =400mV):-



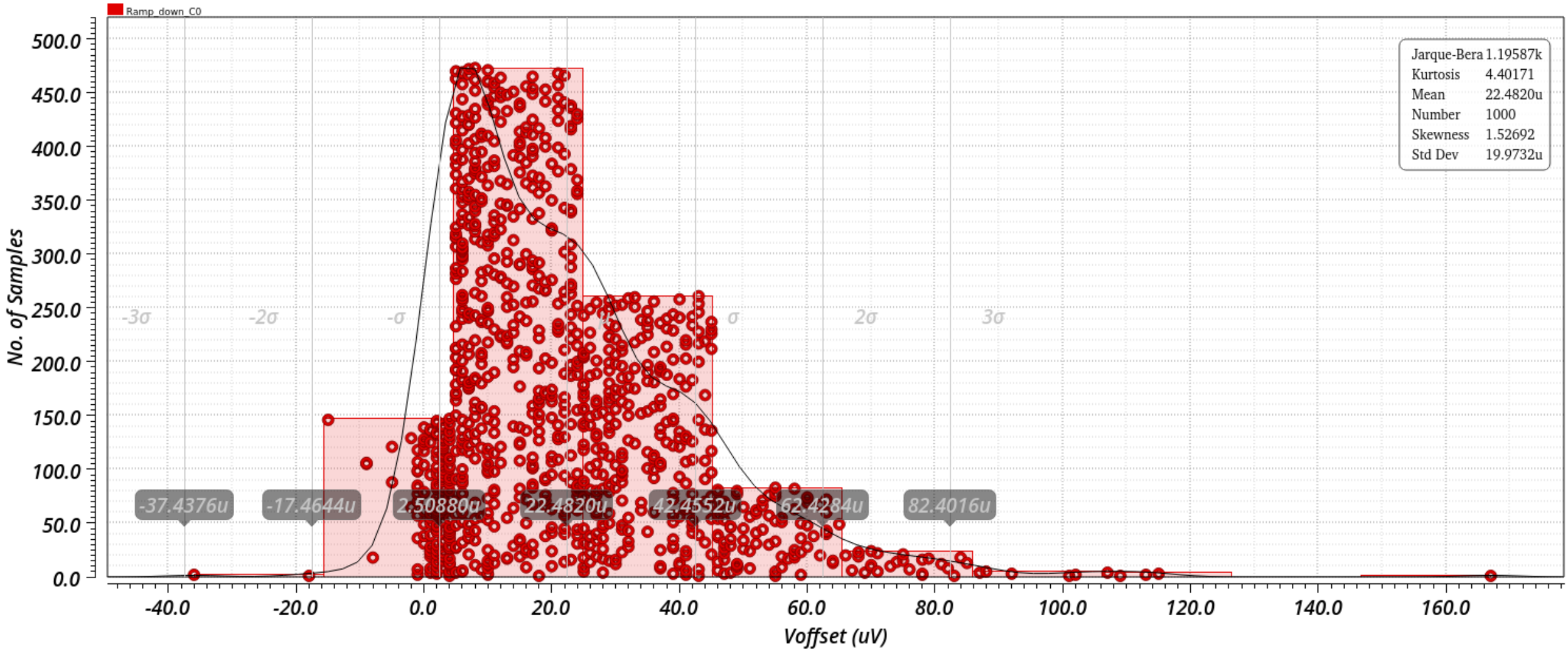
Ramp up Test (load 10fF with Vin- =400mV, Monte Carlo with Process and Mismatch):-



Ramp Down Test (load 10fF with Vin- =400mV):-



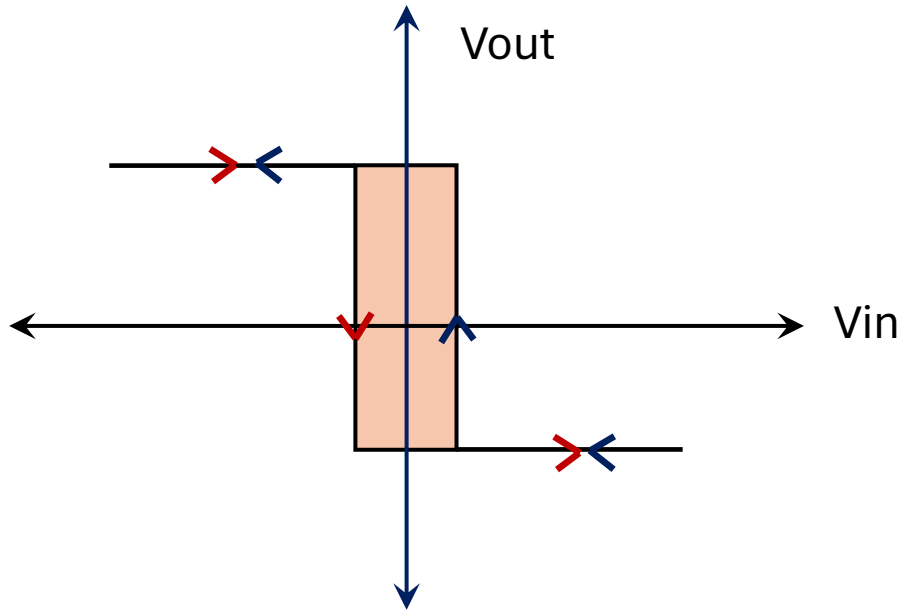
Ramp Down Test (load 10fF with Vin- =400mV, Monte Carlo with Process and Mismatch):-



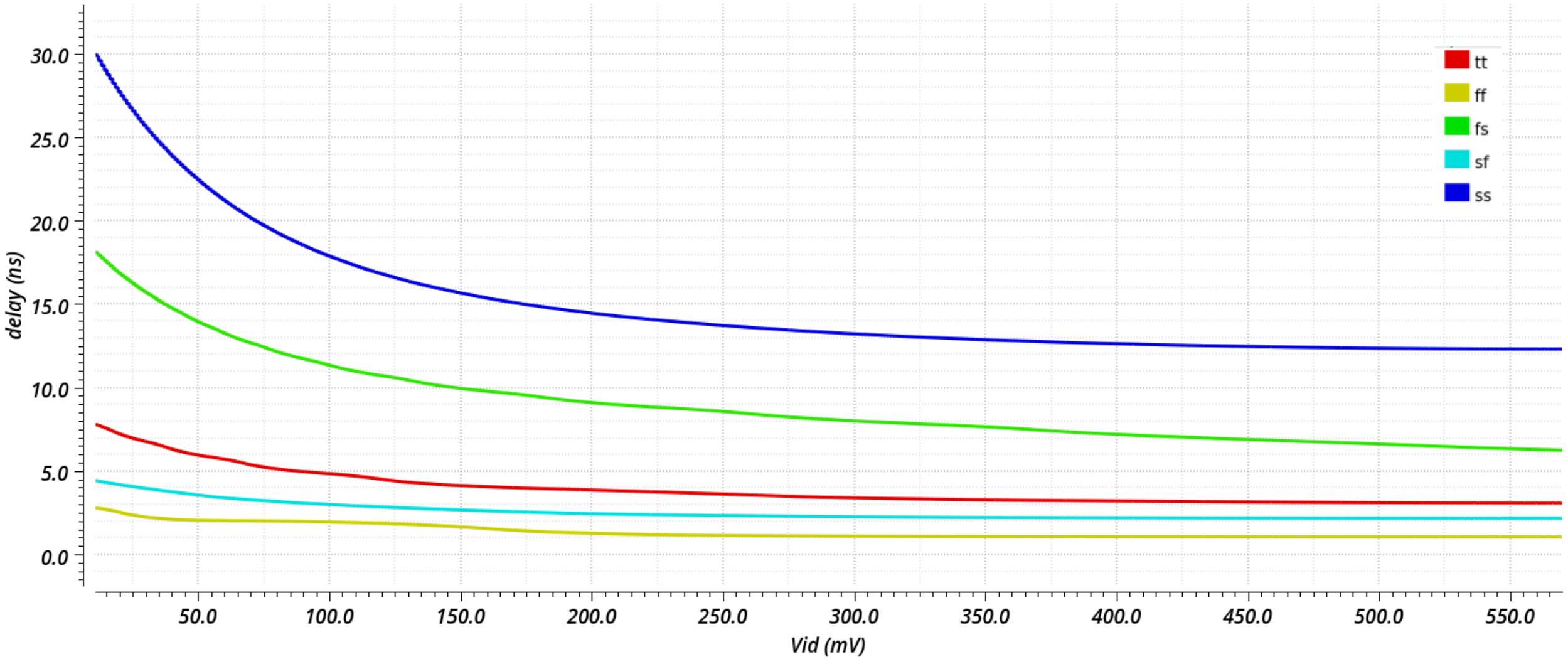
Hysterisis :-

Hystersis Window =| μ_{up} - μ_{down} | = 45uV

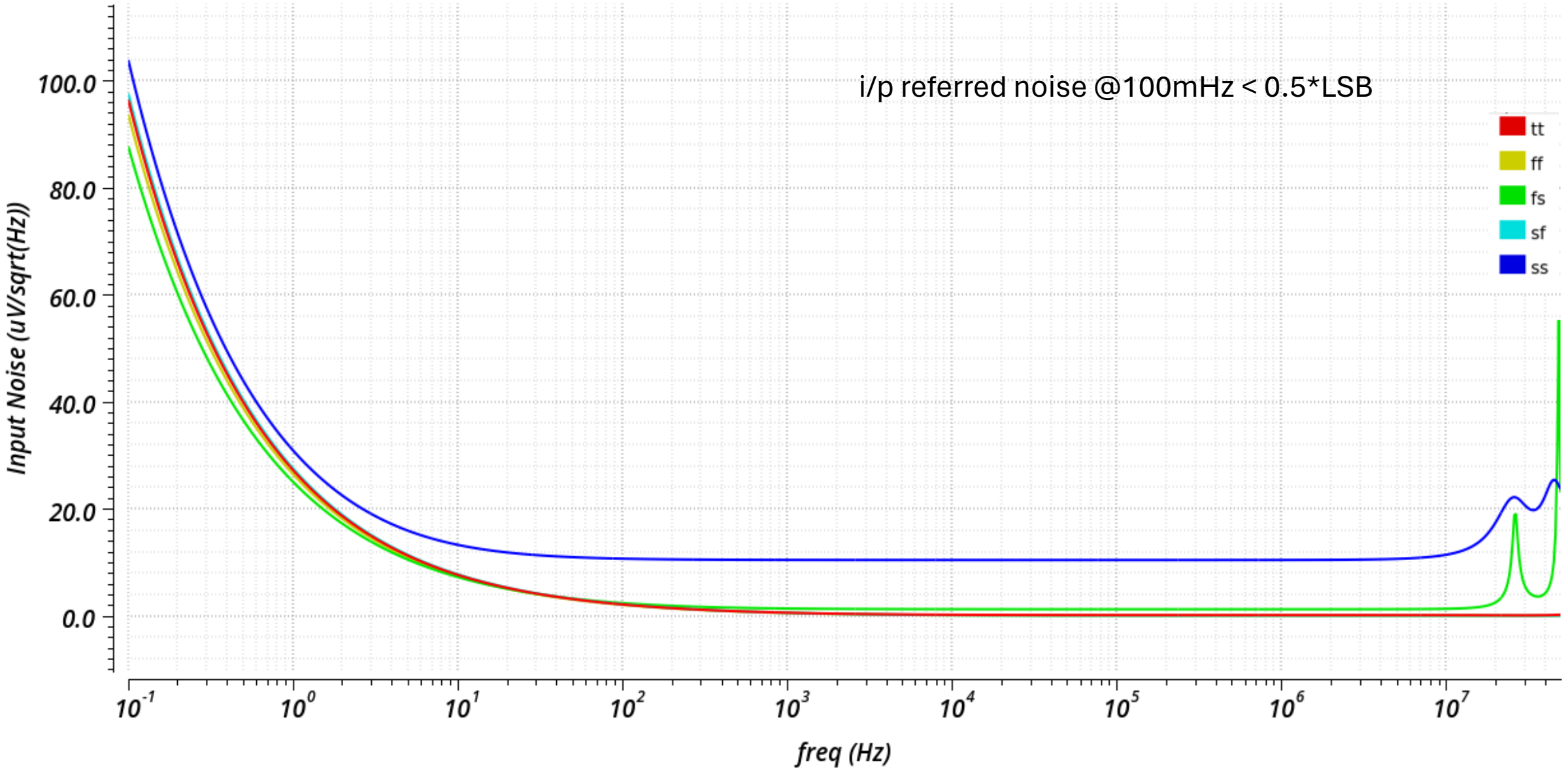
Hysteris Is centered around Vcm = $V_{DD}/2$



Delay vs input voltage [Simulated with Vcm=400mV and Load =10fF]

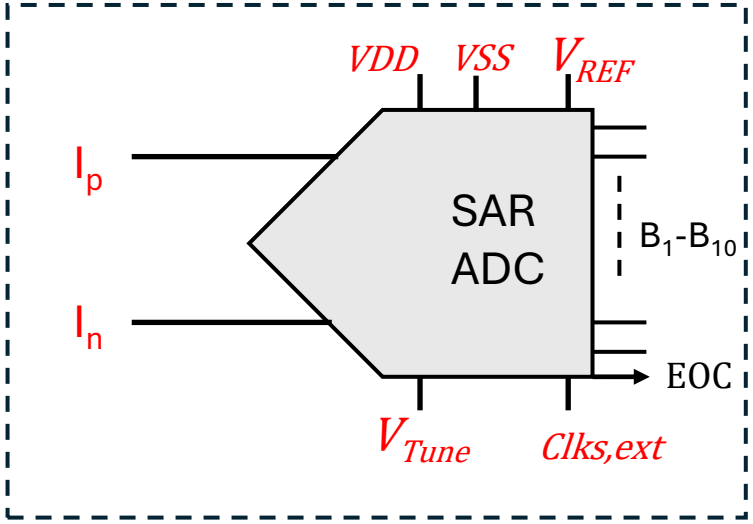


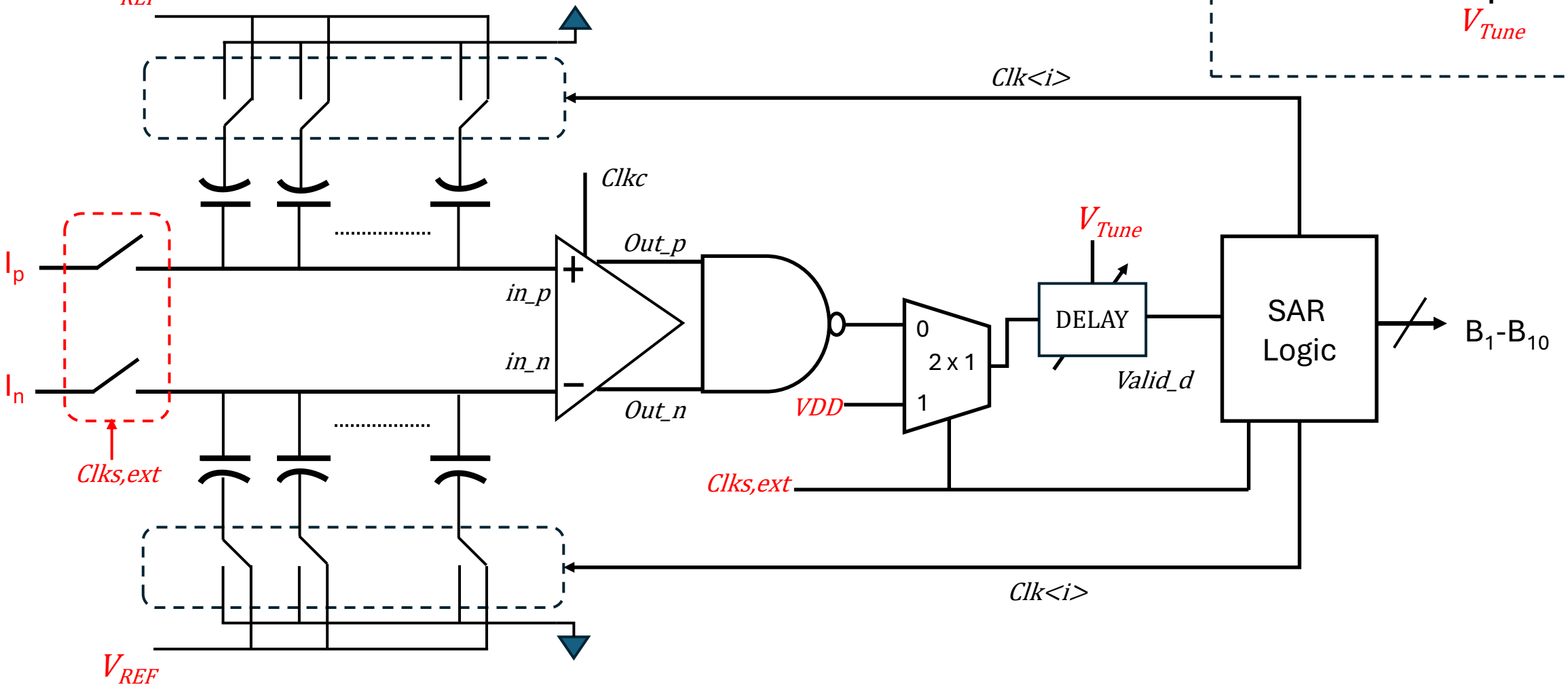
Input referred Noise [Simulated with Load =10fF]



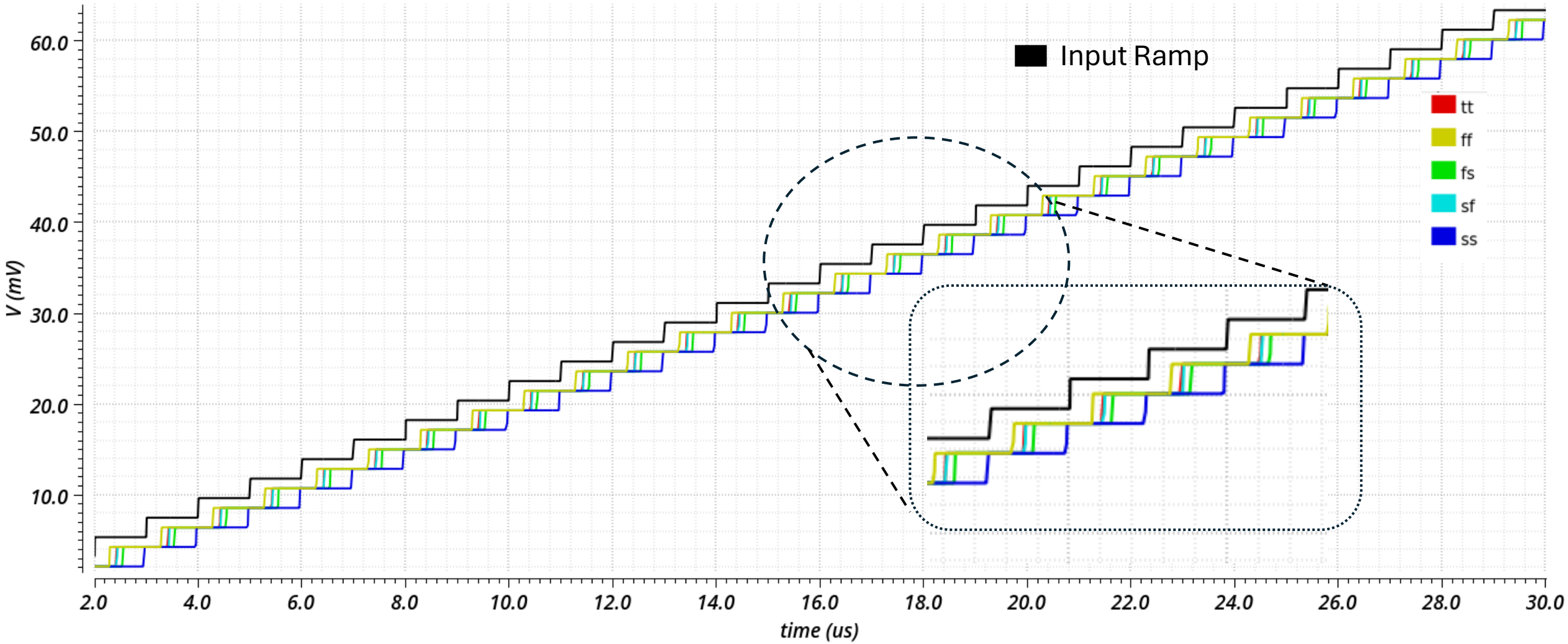
[@load10fF,VDD=0.8]	tt	ff	fs	ss	sf
Power (avg) W	124.4n	132.1n	91n	124.6n	146n

Asynchronous SAR ADC Block Diagram



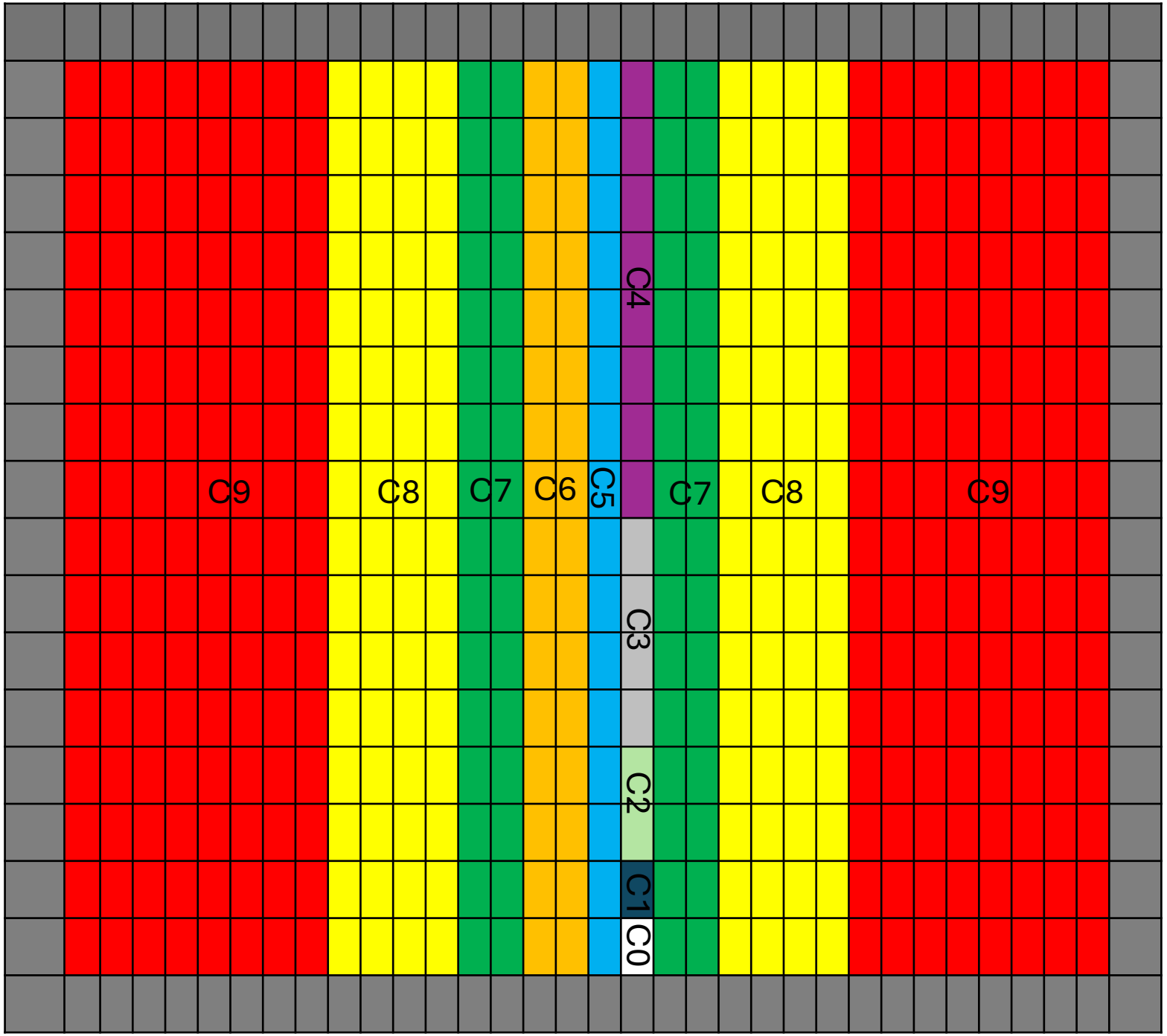


ADC Ramp Test: V_{tune} = 250mV, V_{REF} =550mV, VDD = 0.8V



[VDD=0.8] Ramp Test Results	tt	ff	fs	ss	sf
Power (avg) W	971.2n	986n	986.3n	990n	1080n

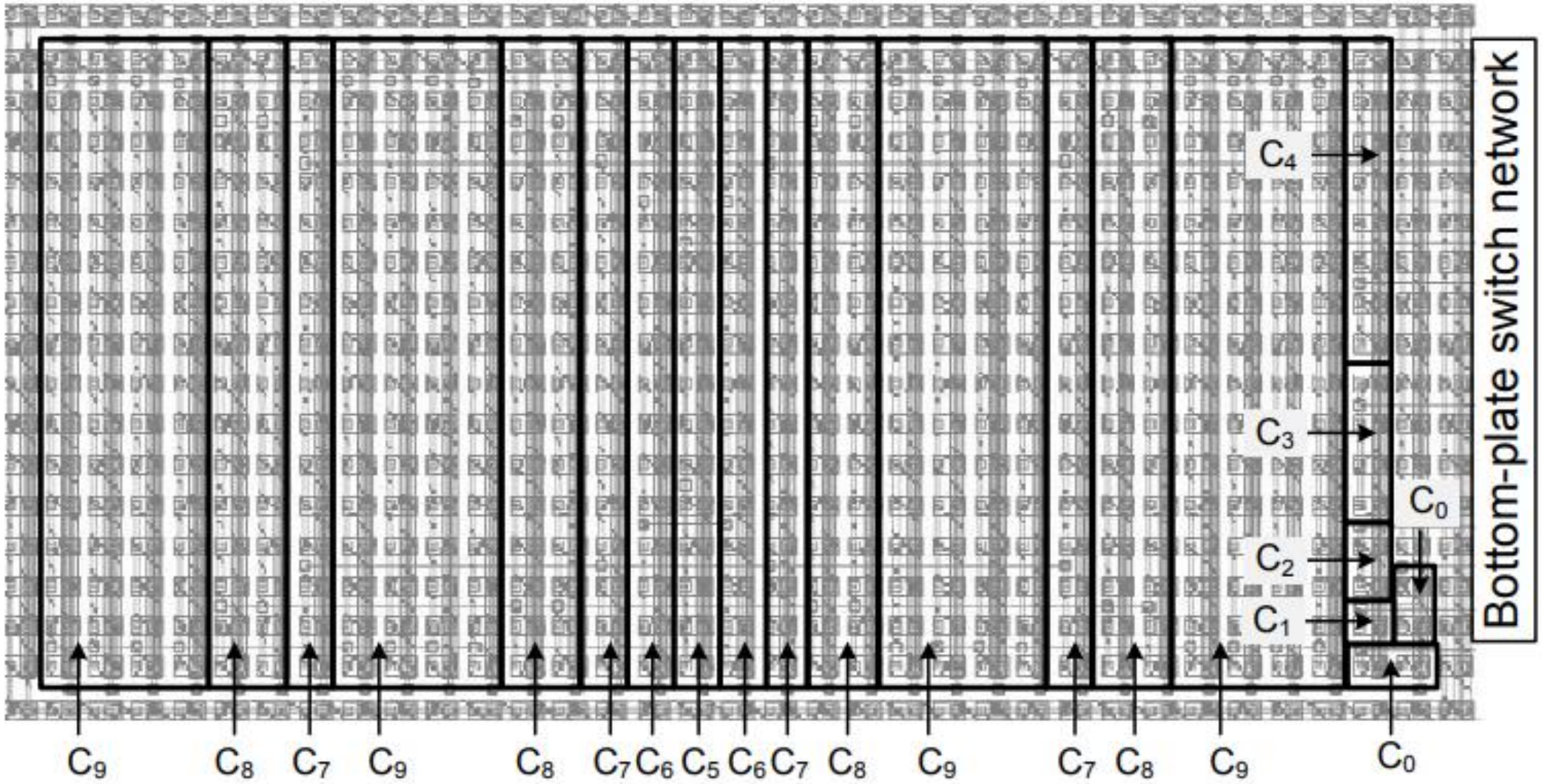
DAC ARRAY FLOOR PLANS



DAC Capacitor Array

Unit cell = 575n x 575n
(C=1.05fF)

Common Centroid Layout



Partial Common Centroid Layout (C9-C5), C4-C0 are placed Close to bottom plate switching Network.
[1] Shows reduced Mismatches and better DAC Linearity with Partial Common centroid Layout

References:

[1] Design of Ultra-Low-Power Analog-to-Digital Converters [D. Zhang, 2012]
[2] A Constant Energy-Per-Cycle Ring Oscillator Over a Wide Frequency Range for Wireless Sensor Nodes [JSSC,2016]