A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter

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Abstract—**This paper describes a 10 b, 20 Msample/s pipeline A/D converter implemented in 1.2 μm CMOS technology which achieves a power dissipation of 35 mW at full speed operation. Circuit techniques used to achieve this level of power dissipation include digital correction to allow the use of dynamic comparators, and optimum scaling of capacitor values through the pipeline. Also, to be compatible with low voltage mixed-signal system environments, a switched capacitor (SC) circuit in each pipeline stage is implemented and operated at 3.3 V with a new high-speed, low-voltage operational amplifier and charge pump circuits. Measured performance includes 0.6 LSB of INL, 59.1 dB of SNDR (Signal-to-Noise-plus-Distortion-Ratio) for 100 kHz input at 20 Msample/s. At Nyquist sampling (10 MHz input), SNDR is 55.0 dB. Differential input range is ± 1 V, and measured input referred RMS noise is 220 μV. The power dissipation at 1 MS/s is below 3 mW with 58 dB of SNDR.**

I. Introduction

REDUCTION of the power dissipation associated with high-speed sampling and quantization is a major problem in many applications, including portable video devices such as camcorders, personal communication devices such as wireless LAN transceivers, in the read channels of magnetic storage devices using digital data detection, and many others. In the past high-speed A/D converters required for these applications in the sampling rate range above 5 Msample/s (MS/s) with 8–12 b of resolutions have consumed large power ranging typically from 100–500 mW. For battery-powered portable applications, this level of power consumption may not be suitable, and further power reduction is essential for power-optimized A/D interfaces.

Low-voltage operation is another important key factor in these portable A/D interface environments. With the trend that A/D interfaces are incorporated as a cell in complex mixed-signal IC's containing mostly digital blocks for DSP and control, the use of the same supply-voltage for both analog and digital circuits can give advantages in reducing the overall system cost by eliminating the need of generating multiple supply voltages with dc-dc converters. Therefore, in order to be compatible with low-voltage systems, a new generation of A/D converters that can operate at supply voltage below 5 V is desired.

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In CMOS, two A/D converter architectures attractive for sampling rate above 10 MS/s and resolution of 10 b are 2step-flash and pipeline. For the 2step-flash architecture, the main advantage is that it requires a smaller number of comparators ($\sim 2^{N/2+1}$) compared to the full flash architecture ($\sim 2^N$) and no operational amplifiers for sample-and-hold (SH) [1], [2]. However, the input bandwidth is usually limited to relatively low frequency compared to the high conversion rate, because of the inherent parallel signal quantization scheme in which comparator offsets and mismatches in signal paths get worse at high speed. Therefore, without the use of a dedicated input SH circuit, the 2step-flash architecture is limited to applications where the input signal bandwidth is limited to relatively low frequency.

On the other hand, the pipeline A/D converter [3], [4] can achieve good high input frequency dynamic performances due to a SH circuit in each stage of the pipeline which allows the signal to be processed through one single low-noise path. In this way, path matching problems that are critical in flash and two-step architectures can be eliminated. In addition, the SH circuit implemented in switched capacitor (SC) gain configuration can provide amplification of the signal for finer conversion. When the interstage gain is incorporated with the use of digital correction, the comparator accuracy requirements can be relaxed by making each stage of the pipeline capable of correcting comparator offset errors from previous stages. Although precision operational amplifiers are required to implement the SH circuit in each stage, potential advantages in good dynamic performance and tolerance to comparator offset errors make a pipeline approach attractive for video-rate applications.

In this paper, a power-optimized implementation of a 10 b CMOS pipeline A/D converter that operates at 3.3 V and achieves 1.75 mW per MS/s of sampling rate at 20 MS/s is presented in four main parts. Section II gives an overview of the 1.5 b/stage pipeline architecture. Section III introduces power reduction techniques. In Section IV, low voltage implementations of key building blocks are described. Finally, experimental results of the prototype are presented in Section V.

II. 1.5 b/Stage Pipeline Architecture

A block diagram of a typical pipeline A/D converter is shown in Fig. 1. It consists of a cascade of N identical stages in which each stage performs a coarse quantization, a D/A function on the quantization result, subtraction, and

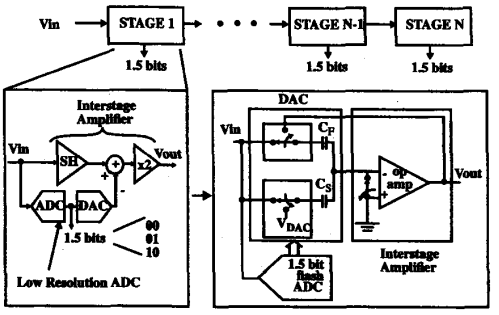


Fig. 1. A 1.5 b/stage pipeline architecture.

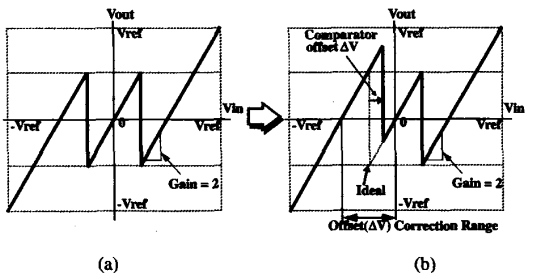


Fig. 2. Residue plots (a) ideal (b) with comparator offset ΔV.

amplification of the remainder. A SH function in each stage allows all stages to operate concurrently, giving a throughput of one output sample per clock cycle. Fig. 1 illustrates the particular configuration of interest here in which the D/A, subtraction, amplification, and SH functions are performed by a switched capacitor (SC) circuit, with a resolution of 1.5 b/stage and an interstage gain of 2. The D/A function is performed by two equal capacitors. When the input signal is applied, each stage samples and quantizes the signal to its per-stage resolution of 1.5 b [4], [8] (i.e., 2 decision levels and 3 possible output codes, 00, 01, and 10 excluding 11), subtracts the quantized analog voltage from the signal by connecting the bottom plate of capacitor C_S to $V_{\text{DAC}}(\pm V_{\text{ref}}$ or 0), and passes the residue to the next stage with amplification for finer conversion. Then, 1.5 b from all stages are collected and produce a full 10 b representation of the applied analog input signal.

The resolution of 1.5 bs/stage is chosen in this pipeline implementation mainly for the following two reasons. The first reason is to maximize the bandwidth of the SH/Gain SC circuit which limits the overall conversion rate. In order to perform fast interstage signal processing, the output of operational amplifier in the SC circuit has to settle in half the clock period to the given accuracy of each stage prior to the next stage sampling instance. Since the bandwidth of the SC interstage amplifier depends on its interstage gain, choosing the per-stage resolution which allows the low closed-loop gain configuration for fast settling is essential. With the resolution of 1.5 b/stage, the closed-loop gain of only 2 allows configuration for low load capacitance (composed of only two sampling capacitors of the next stage and input capacitance of two comparators in the flash A/D section) and large feedback factor (of about 1/3), and as a result a large interstage amplifier bandwidth can be achieved compared to that of larger per-stage resolution (2–3 b/stage).

Also, the resolution of 1.5 b/stage allows large correction range for comparator offsets in the flash A/D section. Only two comparators are required in the flash A/D section of each stage, and the comparator offset up to $\pm V_{\text{ref}}/4$ can be tolerated without degradation of the overall linearity or SNR. This is illustrated with residue plots in Fig. 2. Input and output ranges of each stage are both $\pm V_{\text{ref}}$. Fig. 2(a) shows ideal case with zero comparator offsets, and in Fig. 2(b), the shifted residue plot due to the comparator offset ΔV is shown. With the use of digital correction algorithm in 1.5 b/stage pipeline architecture, the overflow of present stage output from the input range of the following stage can be prevented even with the presence of a large comparator offset up to $\pm V_{\text{ref}}/4$, so that this offset error amplified down the pipeline can be detected for correction.

This large error correction range can also eliminate the dedicated input SH circuit. Instead, the input signal can be sampled simultaneously by the switched capacitor amplifier and by the dynamic comparators of the flash A/D section in the first stage. This is made possible by the fact that digital correction allows comparator errors up to $\pm V_{\text{ref}}/4$ without degradation of linearity or SNR. The overall pipeline contains 9 2-b flash quantizers and 8 interstage amplifiers.

III. Power Reduction Techniques

In pipeline A/D converters, a major portion of the total power dissipation is from the static power dissipated in analog circuit components that require dc bias currents, such as precision comparators and op amps. The charging/discharging of sampling capacitors, clock drivers and digital circuits contribute a relatively small amount to the overall power dissipation. Therefore, in this implementation, major effort is taken to reduce dc power dissipation. One effective method is to use dynamic comparators to implement the low-resolution flash A/D section in each stage, since the digital correction can relax the comparator accuracy requirements as mentioned in Section II. In this way, static power dissipation of precision comparators can be eliminated. Also, a substantial power reduction can be achieved by using the minimum possible size of sampling capacitors at each point in the pipeline, as dictated by kT/C thermal-noise considerations. This is possible since later stages can tolerate more noise due to decreasing stage resolution down the pipeline and therefore can be made small to reduce power consumption. These design approaches are discussed in detail in the following sections.

A. Dynamic Comparators

In high resolution A/D converters, precision comparators consume dc power since low-offset pre-amp stages are required to amplify the signal before an accurate comparison is made. However, in the pipeline architecture, the error from a large comparator offset in flash A/D section of each pipeline stage can be easily compensated with digital correc-

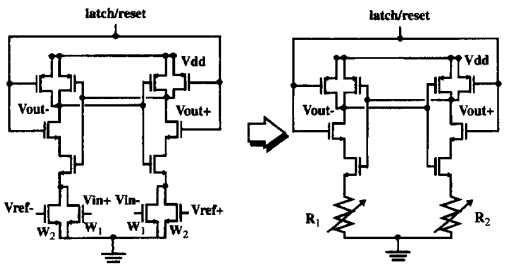


Fig. 3. A dynamic comparator with a built-in threshold level.

tion. As mentioned above, for a 1.5 b per-stage resolution, the comparator offset up to $\pm V_{\text{ref}}/4$ can be corrected. So, for example, with a reference voltage of 1 V used in the prototype, comparator offset up to ±250 mV can be tolerated. In typical dynamic cross-coupled inverter latches, process variations and mismatches can result in large offset voltage but they can still meet this offset requirement easily. So, without the use of a pre-amp, simple dynamic latches can implement the comparators in the low resolution flash A/D converter to remove dc power dissipation.

One implementation of a dynamic comparator is shown in Fig. 3. Here the lower set of NMOS devices operate in the triode region and they are connected to the input and the reference. As the upper cross-coupled inverter-latch regenerates when the latch clock goes high, the drain currents of the active switching NMOS devices are steered to obtain a final state determined by the mismatch in the total resistance. In this case, resistances (R_1 and R_2) or conductance ($G_1 = 1/R_1$ and $G_2 = 1/R_2$) of NMOS pairs biased in triode region are given to the first order by

$$G_1 = \frac{1}{R_1} = kp\left[\frac{W_1}{L}\cdot(V_{\text{in}+} - V_{th}) + \frac{W_2}{L}(V_{\text{ref}-} - V_{th})\right], \tag{1}$$

$$G_2 = \frac{1}{R_2} = kp\left[\frac{W_1}{L}\cdot(V_{\text{in}-} - V_{th}) + \frac{W_2}{L}(V_{\text{ref}+} - V_{th})\right]. \tag{2}$$

The input voltage which causes G_1 equal to G_2 is the comparator threshold voltage. From (1) and (2), it is given by

$$V_{\text{in}}|_{\text{threshold}} = \frac{W_2}{W_1}\cdot V_{\text{ref}} \tag{3}$$

where $V_{\text{in}} = V_{\text{in}+} - V_{\text{in}-}$ and $V_{\text{ref}} = V_{\text{ref}+} - V_{\text{ref}-}$.

Therefore, arbitrary noncritical thresholds can be set by properly ratioing the triode region device widths, (W_2/W_1), without the use of any sampling capacitors or switches at the input. In this implementation, the required (W_2/W_1) ratio is 1/4 to generate comparator threshold levels at $\pm V_{\text{ref}}/4$. Of the 35 mW total dissipation in the experimental A/D converter operating at 20 MS/s, it is estimated that only 3.5 mW was dissipated in 18 comparators.

B. Scaling of SC Circuits Through the Pipeline

A fundamental noise source present in A/D converters is thermal noise, and the magnitude of this noise is a function of the sampling capacitor size ($\sigma^2_{\text{thermal}} \sim kT/C$). For instance if the input signal is sampled on a 1 pF capacitor through a MOS transmission gate, the voltage sampled on the capacitor contains not only the signal but also the noise voltage whose rms value is 64 μV at room temperature. Therefore, in this ideal case, the minimum achievable power dissipation in a MOS sample/hold circuit is set by the maximum allowable value of this kT/C noise to achieve the required signal-to-noise-ratio (SNR) before quantization. This sets the minimum sampling capacitor value, which in turn sets the minimum power dissipation for a given sample rate assuming the capacitor must be completely discharged on each sample period. At room temperature this limit corresponds to about 0.2 μW per MS/s at the 10 b resolution level, assuming the rms thermal noise is set to cause 1 dB decrease in overall SNR over and above that contributed by ADC quantization noise in the ideal case, and that the signal swing is equal to the supply voltage. The required power dissipation quadruples for each additional bit of resolution and is independent of power supply voltage.

This limit is about four orders of magnitude below the dissipation achieved in recently described high-speed A/D converters. In practice, the SH power is dominated by dissipation in the (usually class A) operational amplifier or buffer that drives the sampling capacitor in the sample and/or charge transfer modes. As a practical matter, power minimization in the overall A/D converter translates to minimizing the power in the active circuitry driving the sampling capacitor whose kT/C noise limits the SNR of the converter.

In the pipeline architecture, this again translates into minimizing the SC circuit power in each stage. In order to do so, the minimum allowable value of sampling capacitor must be used at each point of pipeline, since it becomes the load capacitance of the previous stage and the size of the amplifier is proportional to that of the capacitor for given speed. Thus, optimization of the power dissipation of each of the operational amplifier in the pipeline can be performed taking into account the source, load, and feedback capacitors seen by each one. Noting that the stage requirements on the speed and accuracy become less stringent as the stage resolution decreases down the pipeline, stages in the later part of the pipeline can be scaled down by using smaller sampling capacitors and op amps. In this case, the sizes of sampling capacitors and op amps near the front end are determined by the noise floor, and toward the end of the pipeline, parasitic capacitances begin to dominate, and so settling time requirements determine the size of each stage.

In the prototype, the optimization resulted in power dissipation ranging from 4.8 mW in the first stage amplifier to 0.5 mW in the last stage amplifier. In Fig. 4, normalized op amp bias currents of each stage are shown. Through this optimization process, the power dissipation can be reduced by about 40–50% relative to the dissipation if all stages are identical.

One implication of the use of small capacitors in the first three stages is that the 0.1% matching in the D/A capacitors required for 10 b INL will not be achieved in the as-fabricated state. Calibration circuitry has been incorporated into the first

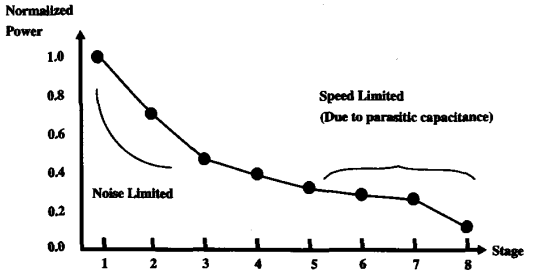


Fig. 4. Scaling of pipeline stages.

three stages to remove these mismatch errors [5]. This circuitry consists of a small T network of trim capacitors around the input sampling capacitor, and in the prototype, these are adjusted using external calibration logic control.

IV. Low Voltage Operation

For compatibility with low voltage digital IC systems, 3.3 V supply was chosen for the prototype, and this requires the solution of two problems to operate SC circuits at low voltage. First, a high-speed 3.3 V op amp with an output swing that is a large fraction of the supply voltage, and with large enough voltage gain for the desired resolution, is required. A second major problem in standard CMOS technologies is the fact that for 3.3-volt supplies, transmission gates produce a high (or infinite) resistance region near the mid-supply voltage due to insufficient gate drive. Solutions to these two problems are described next.

A. High-Speed 3.3 V Op Amp

In the pipeline architecture the most stringent requirement on the op amp is on the first stage where dc gain in excess of 60 dB and 0.1% settling time under ~20 ns are required to implement an accurate SC SH/Gain block for 10 b 20 MS/s operation. In a typical 1.2 μm CMOS technology, designing such an op amp with power consumption of a few mW's is a difficult task. Especially with a 3.3 V supply, it becomes more challenging where the triple-cascode op amp structure, the simplest way to increase gain while maintaining high speed as in [3] and [4] cannot be used due to a limited output swing. While a folded cascode op amp can be used at 3.3 V, its folded implementation requires a slow PMOS transistor in the signal path and degrades achievable dc-gain due to reduced output resistance at the folding node compared to straightforward cascode. To improve the dc-gain, multi-stage configurations with pole-split compensation are attractive, but because of the nondominate pole resulting from the load capacitance and the necessity of driving a compensation capacitor, a substantial degradation in achievable bandwidth and settling time at a given power dissipation can result.

For 10 b 3.3 V operation, however, another viable solution is to use a cascode stage with a low-gain, wideband preamplifier to increase the gain by a factor of about 2. While this does add another stage with its power dissipation, it has only NMOS transistors in its signal path and preserves the very desirable

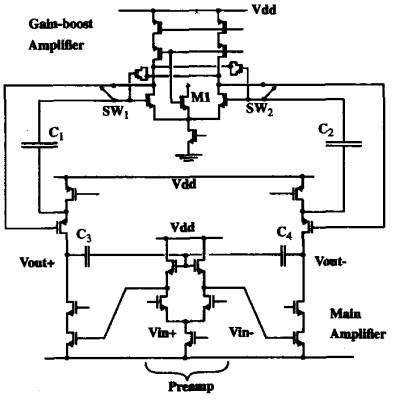


Fig. 5. A 3.3 V high-speed high-gain op amp.

property of the cascode amplifier that the load capacitance is also the compensation capacitance. The low-gain preamplifier increases the effective *gm* of the transconductance stage and provides necessary dc bias level shifting for the second stage input. However, a nondominant pole is introduced due to the input capacitance of the transconductance stage. In this case, choosing the optimum value for preamplifier gain is important not to waste any achievable bandwidth. For example, if the preamplifier gain is too small, the "boosting" effect on the *gm* of the transconductance stage will be sub-optimum. If it's too large, then the nondominant pole will be brought down and limit the bandwidth. Therefore, there will be an optimum value for the preamplifier gain for the given SC configuration which achieves minimum settling time.

This configuration was utilized in the prototype, and its circuit diagram is shown in Fig. 5. The optimum value for the preamplifier gain for the given SC configuration was about 1.75. In the particular technology used for the prototype, the output resistance of the PMOS transistor was much worse than that of the NMOS transistor for the same bias condition. Thus series feedback gain-boost amplifiers [6] are included in the PMOS current source to provide an adequate voltage gain as shown in Fig. 6. These amplifiers implemented in differential configuration are capacitively coupled into the signal path using level shift capacitors C_1 and C_2 which are initialized by closing switches SW_1 and SW_2 with transistor M_1 connected to desired input common mode level. The common-mode feedback of the main amplifier is also capacitive through C_3 and C_4. This is also illustrated in Fig. 6.

Running on a single 3.3 V supply, the first stage amplifier achieved a simulated 0.1% settling time of about 17 ns with $C_S = C_F = 0.39$ pF and external load of 1.8 pF. Power dissipation of the first stage op amp is 4.8 mW and from experimental results it can be deduced that the voltage gain is greater than 60 dB. Gain-boost amplifiers are used only for first three stages, since dc gain requirements in later stages are relaxed.

In Fig. 10, differential nonlinearity (DNL) and integral nonlinearity (INL) versus input code are plotted. The magnitude of the maximum DNL and INL are 0.5 LSB and 0.6 LSB, respectively.

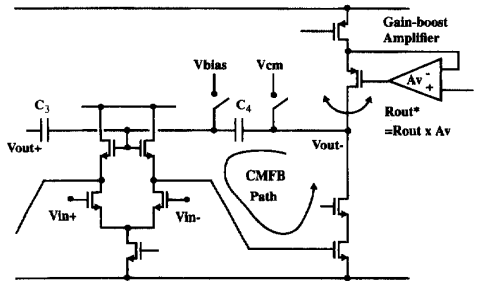


Fig. 6. CMFB and gain-boost amplifier.

B. Low Voltage Operation of SC Circuits

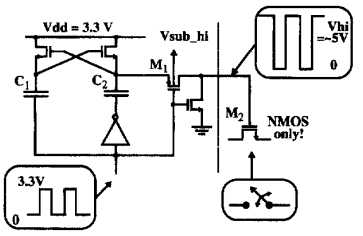
In standard CMOS technologies, the threshold voltage of MOS transistors (typically $|\sim 0.8\,\mathrm{V}|$) does not scale with the supply voltage, and it becomes a large portion of the supply voltage leading to problems when MOS transistors are used as switches at low voltages. For instance, assuming supply voltage of 3.3 V, the input signal voltage at the mid-point of the supply, and threshold voltage of about 1.3 V with body-effect, the gate voltage overdrive given by $(V_{gs}-V_{th})$ becomes 0.35 V ($V_g - V_s - V_{th} = 3.3\,\mathrm{V} - 1.65\,\mathrm{V} - 1.3\,\mathrm{V} = 0.35\,\mathrm{V}$). In this case, switch on-resistance can vary by 30–60% if threshold voltage changes by ±100–200 mV with process variations, resulting in speed degradation of the SC circuits. Although large transistor switches can be used for the worst case V_{th} design, the switch parasitic capacitance can significantly overload the output of SC circuits, especially in later stages where they are small due to scaling. Therefore, in order to solve this problem, increasing $(V_{gs} - V_{th})$ is desirable to implement low on-resistance MOS switch without adding too much parasitic capacitance.

There are several possible ways to increase this gate voltage drive. One method is to reduce V_{th} by including an extra low-threshold (~0–0.3 V) transistor in the process. However, this adds process complexity. Another method is to increase V_{gs} by using one large 5 V supply created from 3.3 V chip supply to drive all switches on the chip, but potential problems of this method include possible crosstalk to some sensitive nodes through the shared supply and difficulty in estimating the total charge drain to drive all switches. Another viable solution is to simply use a dynamic circuit to locally boost the clock drive. In this case each individual charge pump circuit drives each transmission gate or set of transmission gates that use the same clock to avoid the problem of crosstalk through the clock line.

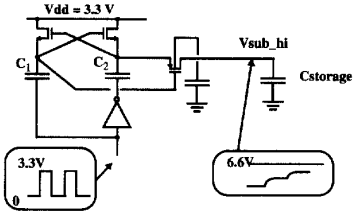
In the prototype, the last approach is used with the use of a high voltage generator circuit shown in Fig. 7(a). By applying a square wave input signal of 3.3 V, C_1 and C_2 are self-charged to 3.3 V through the cross-coupled NMOS transistors [7], and an inverted square wave output of (5 V is generated according to

$$V_{hi} = 2V_{dd} \cdot \frac{C_2}{C_{\mathrm{gate},M2} + C_2 + C_{\mathrm{parasitic}}}. \qquad (4)$$

where $C_{\mathrm{gate},M2}$ is the gate capacitance of transistor M_2. Because this gate voltage overdrive is much higher than the signal common-mode voltage ($\approx V_{dd}/2$), sampling switches



(a)



(b)

Fig. 7. (a) A high voltage generator for switches. (b) A bias voltage generator for the well of M_1 to prevent latch-up.

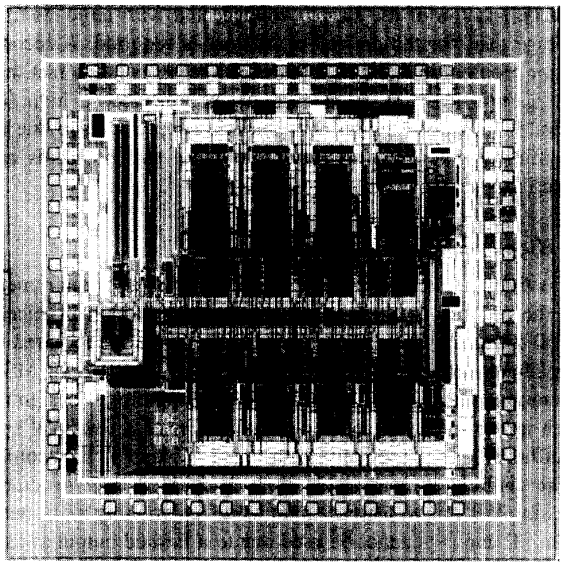


Fig. 8. A die photo.

are implemented with only NMOS transistors, and the parasitic capacitance from PMOS transistors is eliminated. Fig. 7(b) shows the bias voltage generator for the n-well of the PMOS transistor M_1, which has been designed to prevent latch up during the initial power-up transient. Reliability is not a concern here since 5-volt-capable technology is used at 3.3 V.

V. Experimental Results

A prototype A/D converter based on the above architecture was fabricated in a double-poly double-metal 1.2-μm CMOS technology. It consists of 8 pipelined stages and one flash

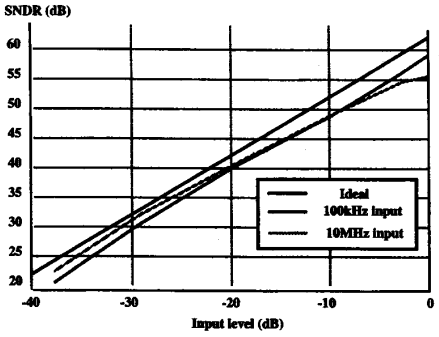


Fig. 9. SNDR versus the input amplitude.

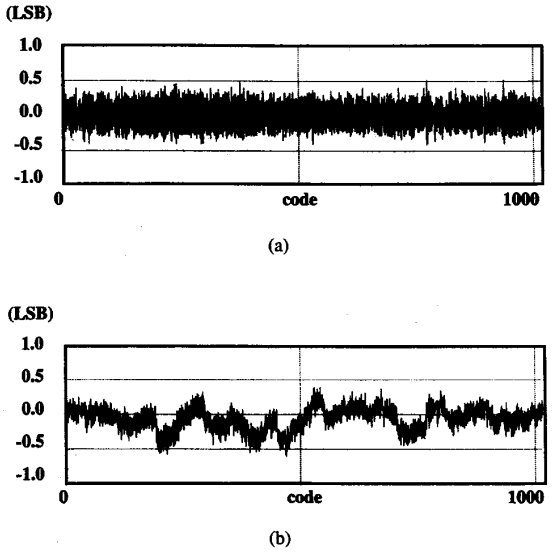


Fig. 10. (a) Differential nonlinearity (DNL). (b) Integral nonlinearity (INL) versus Code.

A/D section in the end. Capacitors in the first three stages are calibrated with trim capacitor arrays to achieve high accuracy. A die photo is shown in Fig. 8. Clock lines are routed in the middle, and the analog signal path is folded around to make the chip area square. Op amp bias circuits are shared between several op amps, and all bias currents are controlled by one external master bias current. Chip area not including the pad ring is 3.2 × 3.3 mm^2.

Fig. 9 shows SNDR versus the input amplitude for 100 kHz and 10 MHz input frequencies at 20-MS/s conversion rate. The peak SNDR is 59.1 dB for 100 kHz input sine wave. At Nyquist sampling (10 MHz input), the SNDR is 55.0 dB.

Fig. 11 shows the probability of getting a code i versus the dc input voltage near the code transition. The extracted total input-referred RMS noise voltage from this plot was ~220 μV while the designed value was 216 μV. This confirms the *kT/C* noise-limited design in the prototype.

Fig. 12 shows the measured power consumption versus the sampling frequency on a log-log scale. Of 35 mW of total power dissipation at 20 MS/s, static power consumption was

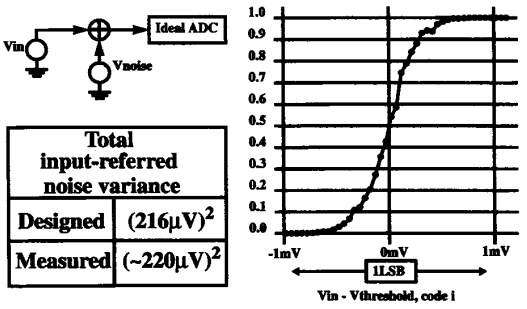


Fig. 11. Measured probability of getting a code i versus the dc input voltage.

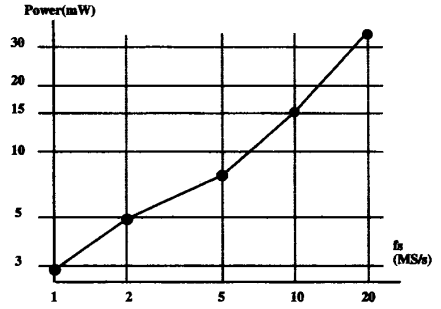


Fig. 12. Power versus the sampling frequency.

TABLE I
A/D PERFORMANCE: 3.3 V AND 25°C

Technology	1.2-μm CMOS
Resolution	10 b
Conversion Rate	20 MS/s
Active Area	3.2 x 3.3 mm^2
Differential Input Range	± 1 V
Input Capacitance	1 pF (single-ended)
Power Dissipation	35 mW *
DNL	0.5 LSB
INL	0.6 LSB
SNDR	59.1 dB (Fin = 100 kHz) 55.0 dB (Fin = 10 MHz)

* Output pad driver power consumption not included.

about 20 mW. At a reduced bias current and a sampling frequency of 1 MS/s, the power consumption was 2.8 mW with peak SNDR of 58 dB.

VI. SUMMARY

This paper describes a 10 b, 20 MS/s, 35 mW pipeline A/D converter in 1.2 μm CMOS technology, and its performance is summarized in Table I. The key features of this converter are: the usage of dynamic comparators and careful scaling of SC circuits down the pipeline to achieve low power dissipation, and new low voltage op amps and charge pump circuits to implement SC circuits for low voltage operation of pipeline stages. This shows that low voltage, low power operation of pipeline A/D converters can be achieved for video-rate applications.

REFERENCES

[1] K. Kusumoto *et al.*, "A 10-b 20-MHz 30-mW pipelined interpolating CMOS ADC," in *ISSCC Dig. Tech. Pap.*, Feb. 1993, pp. 62–63.

[2] M. Ito *et al.*, "A 10-b 20-Ms/s 3 V-supply CMOS A/D converter for integration into system VLSIs," in *ISSCC Dig. Tech. Pap.*, Feb. 1994, pp. 48–49.

[3] T. Matsuura *et al.*, "A 95-mW, 10-b 15-MHz low-power CMOS ADC using analog double-sampled pipelining scheme," in *VLSI Symp. Dig. Tech. Pap.*, 1992, pp. 98–99.

[4] S. H. Lewis *et al.*, "10-b 20-Msample/s analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, pp. 351–358, Mar. 1992.

[5] Y. M. Lin, B. Kim, and P. R. Gray, "A 13-b 2.5 MHz self-calibrated pipelined A/D converter in 3-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 26, pp. 628–636, Apr. 1991.

[6] K. Bult and G. J. G. M. Geelen, "A fast-settling CMOS opamp with 90-dB dc gain and 116 MHz unity-gain frequency," in *ISSCC Dig. Tech. Pap.*, Feb. 1990, pp. 108–109.

[7] Y. Nakagome *et al.*, "Experimental 1.5-V 64-Mb DRAM," *IEEE J. Solid-State Circuits*, vol. 26, pp. 465–472, Apr. 1991.

[8] G. Jusuf, "A 1-bit/cycle algorithmic analog-to-digital converter without high-precision comparators," Electron. Res. Lab., Univ. of California, Berkeley, Memo. UCB/ERL M90/69, Aug. 1990.

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