A 100-MHz Pipelined CMOS Comparator

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Abstract — **This paper describes the design of a VLSI-compatible CMOS comparator for high-speed applications. An examination of various generic approaches to obtaining the nonlinear "amplification" needed to perform the function of comparison leads to the conclusion that this amplification can best be obtained by means of regeneration. Based on this conclusion, a CMOS comparator has been designed wherein voltage comparisons are accomplished directly by means of a pipelined cascade of two regenerative sense amplifiers, without the use of a preamplifier. To ensure an input resolution of at least 8 bits, offset cancellation is incorporated in the first sense amplifier. In addition, an input sampling network comprised of only passive devices is used to sample the two analog inputs and cancel their common-mode voltage. The comparator has been integrated in a 2-μm CMOS technology and has a maximum sampling rate of over 100 MHz; it operates from a single +5-V supply and dissipates only 3.6 mW at its maximum sampling rate.**

I. Introduction

THE performance of high-speed data conversion and digital communication interfaces is generally limited by the speed and precision with which the function of comparison can be performed. MOS comparators suitable for integration in VLSI technologies have been successfully realized for audio frequency applications, such as analog-to-digital (A/D) converters for voice-band telecommunications systems [1], [2]. Moreover, the potential of MOS technology in high-speed applications has been demonstrated by a 750-MHz comparator implemented in a 1-μm NMOS technology [3]. However, in applications requiring at least 8 bits of resolution, previously reported MOS comparators have been limited to sampling rates of at most 30 MHz, even when integrated in an advanced 1.5-μm CMOS technology [4]–[10].

The speed and resolution of MOS comparators are typically limited by the inherent MOSFET characteristics of low transconductance and relatively large device mismatches. However, MOS technologies also offer the substantial advantages of zero-offset analog switches and high-impedance charge storage. These attributes allow for the extensive use of circuit techniques such as dynamic offset cancellation, dynamic biasing, and analog pipelining to significantly improve the speed and resolution achievable in an MOS comparator.

This paper describes the design of a VLSI-compatible CMOS comparator wherein voltage comparisons are accomplished directly by means of regenerative sensing. Input sampling, offset correction, and common-mode cancellation have been incorporated into a pipelined cascade of regenerative sense amplifiers so as to avoid the need for preamplification. The circuit is fully differential and has been integrated in a standard 2-μm CMOS technology. It operates at a maximum sampling rate of over 100 MHz, while dissipating only 3.6 mW of power from a single +5-V supply. Although designed specifically for use in fully parallel analog-to-digital converters, the comparator is suitable for a variety of high-speed instrumentation and communications applications.

In Section II of this paper, the nonlinear amplification needed for performing the comparison function is studied using small-signal models for three generic approaches; this study leads to the conclusion that the amplification can best be obtained by means of regeneration. Based on the assessment of Section II, a pipelined CMOS comparator is introduced in Section III. Sections IV and V provide detailed descriptions of circuits used in the comparator, including the input sampling network and an autocalibrated regenerative sense amplifier. Experimental results are presented in Section VI.

II. Comparator Amplification Techniques

The basic function of a comparator is that of providing amplification sufficient to ensure that digital output levels can be generated in response to small differences between two input signal levels. This amplification need not be linear, nor continuous in time; consequently, it can be realized using nonlinear gain stages and, in applications where the latency can be tolerated, the total amplification can be distributed along a cascade of pipelined stages.

Three generic approaches to obtaining the amplification needed in a comparator are a single-pole amplifier (SPA), a multistage amplifier (MA) comprising a cascade of N identical SPA's, and a regenerative sense amplifier (RSA) that can be implemented using a pair of cross-coupled SPA's. Shown in Fig. 1 are small-signal models representative of each of these approaches, along with waveforms depicting the nature of the transient output responses for the circuits.

Manuscript received May 1, 1988; revised August 15, 1988. This work was supported by the U.S. Army Research Office under Contract DAAL03-87-K-0111 and by grants from Tektronix, Inc. and Fairchild Semiconductor Corporation.

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IEEE Log Number 8824072

0018-9200/88/1200-1379$01.00

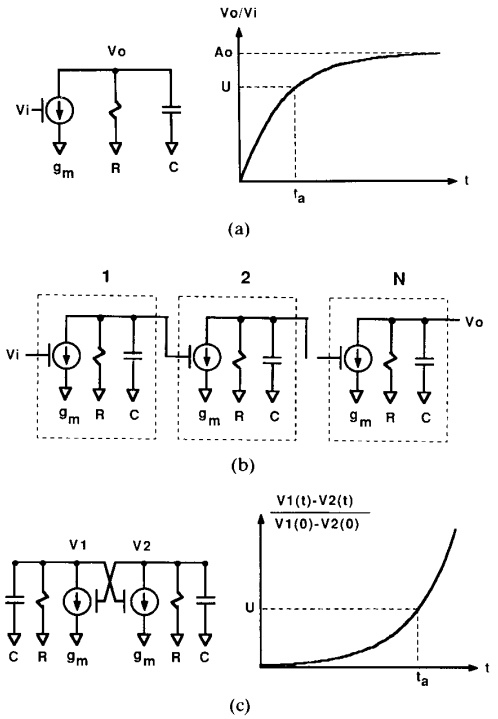


Fig. 1. Generic approaches to obtaining amplification in comparators. (a) Single-pole amplifier (SPA). (b) Multistage amplifier (MA). (c) Regenerative sense amplifier (RSA).

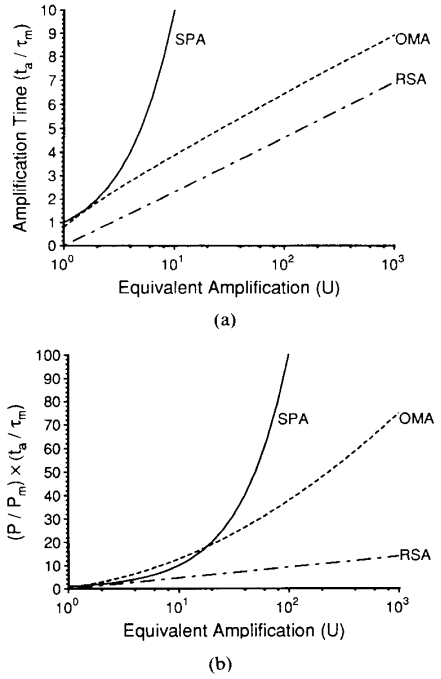


Fig. 2. Comparisons of (a) delay and (b) power–delay product for SPA, OMA, and RSA configurations.

For the SPA and MA configurations of Fig. 1, it is assumed that a step waveform is applied at the input. Because linear amplification is not required in comparison applications, the output need not settle close to its steady-state value at the time the comparison actually takes place. Thus, the equivalent amplification U for these circuits is defined as the ratio of the output V_o to the input step amplitude V_i after an amplification time t_a, as indicated in Fig. 1. If the MOSFET output conductances are neglected, the relationships between t_a and U for the SPA and MA are simply

$$t_a(\text{SPA}) = \tau_m \times U \tag{1}$$

and

$$t_a(\text{MA}) = \tau_m \times (U \times N!)^{1/N} \tag{2}$$

where $\tau_m = C/g_m$, g_m is the transconductance of each amplifier stage, and C is the capacitance at each output node. The inverse of τ_m is the unity-gain bandwidth of a transistor with a transconductance of g_m driving a capacitive load C.

For the MA, there exists an optimum number of stages, N_{op}, for which $t_a(\text{MA})$ is minimized. The relationship between N_{op} and $\ln(U)$ is nearly linear and is closely approximated by

$$N_{op} \approx 1.1 \times \ln(U) + 0.79 \tag{3}$$

for $U < 1000$. From (2) and (3) it is possible to determine the delay of a multistage amplifier with an optimum number of cascaded stages (OMA).

As indicated in Fig. 1, an RSA can also be used as a nonlinear gain stage. The equivalent amplification U of such a stage is defined as the ratio of the differential output, $V_1(t) - V_2(t)$, to the initial unbalance, $V_1(0) - V_2(0)$, after a regeneration time period of t_a. Again neglecting the MOSFET output conductance, the amplification time $t_a(\text{RSA})$ is related to U by

$$t_a(\text{RSA}) = \tau_m \times \ln(U). \tag{4}$$

Unlike the case for the SPA and MA configurations, where the equivalent amplification is limited by the low-frequency gain of the individual SPA stages, U for an RSA is limited only by dc bias conditions and the supply voltage. It is, of course, essential that the initial input imbalance of the RSA, $V_1(0) - V_2(0)$, at the time the amplifier is clocked be directly related to the comparator inputs.

Fig. 2 shows comparisons of the relative total delays and power–delay products needed to achieve a given equivalent amplification with the SPA, OMA, and RSA configurations. In these comparisons it has been assumed that the power dissipation P_m and delay τ_m are the same for each SPA stage.

Based on the analytical results of Fig. 1 it is clear that the amplification required in a comparator is best obtained by means of regeneration. However, from a practical standpoint this may be difficult to accomplish. In MOS comparators it is usually necessary to compensate for relatively large offsets within the sense amplifier. Conse-

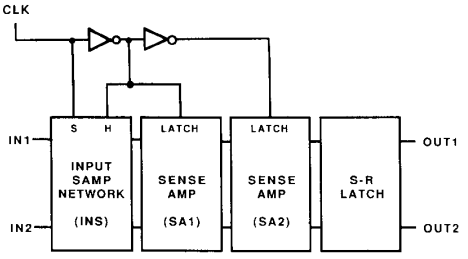


Fig. 3. Comparator architecture.

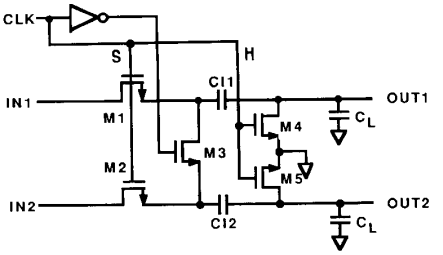


Fig. 4. Input sampling network (INS).

quently, the regenerative latch is typically preceded by a preamplifier [7], [8], [10]. The situation is further complicated if the comparator must accommodate large variations in the common-mode input level, such as those inherent in flash A/D converters. However, these difficulties can be overcome through the use of offset compensation directly within the regenerative amplifier itself together with an input sampling network that removes the common-mode input voltage.

III. Comparator Architecture

The architecture of the comparator proposed herein is shown in Fig. 3. It comprises a pipelined cascade of an input sampling network (INS), two regenerative sense amplifiers *SA*1 and *SA*2, and an *S-R* latch. The function of the input network is to sample the two analog input signals and then generate an output proportional to the voltage difference between them, while canceling the common-mode input voltage. The two pipelined gain stages, *SA*1 and *SA*2, provide the necessary amplification for the comparator. To achieve a resolution of at least 8 bits, offset cancellation is incorporated within the first sense amplifier *SA*1. The second regenerative amplifier is used to avoid the need for full-CMOS levels at the output of *SA*1. In its reset mode, both outputs of *SA*2 are low; the regenerated outputs of this amplifier can thus be stored using a simple *S-R* latch, and the overall comparator outputs will be valid at all times other than during the *SA*2 regeneration transition. Operation of the pipeline in the comparator is controlled by a single external clock with a 50-percent duty cycle, inverted and delayed as appropriate for each stage. The comparator is fully differential so as to achieve the highest possible noise immunity, and it is designed to operate from a single +5-V power supply.

Each of the sense amplifiers has two modes of operation: a reset mode and a regeneration mode. A balanced bias condition is set up within an amplifier during the reset mode. An imbalance at the sense-amplifier input is then "amplified" during the regeneration mode. *SA*1 and *SA*2 can be cascaded together in a pipelined configuration wherein when one sense amplifier is in the reset mode, the other is in the regeneration mode.

The *S-R* latch following *SA*2 stores the digital outputs from *SA*2. When *SA*2 is in the regeneration mode, its outputs rise and fall to complementary full-CMOS digital output levels and steer the *S-R* latch. After the regeneration, *SA*2 switches to the reset mode and both of its outputs return to 0 V without glitching; thus, the *S-R* latch remains in its previous state and stores the result of the regeneration in *SA*2.

Amplifiers *SA*1 and *SA*2 provide the voltage amplification needed to convert a small input voltage difference into digital output levels that correctly represent the polarity of the input difference. In this design, the analog input is assumed to range from 0 to 2 V. To achieve an 8-bit dynamic range with $\pm 1/2$ LSB resolution, the comparator must be able to resolve input differences less than $2\text{ V}/(2^8 \times 2) \approx 3.9$ mV. For a digital output swing of 5 V, the two sense amplifiers together must therefore provide an equivalent voltage amplification of at least $2 \times 2^8 \times (5\text{ V}/2\text{ V}) = 1280$.

To achieve the required input resolution, offset cancellation is embedded within amplifier *SA*1. The equivalent amplification of *SA*1 reduces the influence of *SA*2's input offset. In this case, the minimum equivalent amplification provided by *SA*1 is 10, while *SA*2 provides the remaining gain.

IV. Input Sampling Network

The input sampling network (INS) shown in Fig. 4 is similar to one used previously in an instrumentation amplifier [11], except that it does not employ active feedback. In the schematic of Fig. 4, the capacitance C_L represents the total equivalent load at each output node of the network. When the input clock *CLK* is high, the network is in the sampling mode; both outputs are shorted to *GND* and the analog input signals V_{i1} and V_{i2} are stored on capacitors *CI*1 and *CI*2. When *CLK* falls low, the circuit switches to the hold mode. *M*1 and *M*2 are first turned off, decoupling *CI*1 and *CI*2 from the inputs, while *M*4 and *M*5 open, releasing the outputs. *M*3 then turns on and, assuming ideal switches and matched capacitors, the differential and common-mode outputs of the network change to

$$V_{o1} - V_{o2} = -(V_{i1} - V_{i2}) \times [C_I/(C_I + C_L)]$$
$$V_{o1} + V_{o2} = 0 \tag{5}$$

where $C_I = CI1 = CI2$. The outputs contain only the difference between the inputs, although the magnitude of this difference has been attenuated by the presence of C_L.

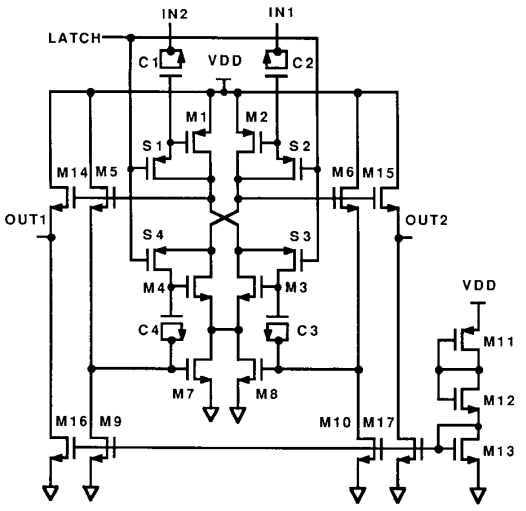


Fig. 5. Sense amplifier *SA*1.

If the devices and capacitors in the input sampling network are well-matched, clock feedthrough and charge injection in the switches $M1-M5$ will generate only a small common-mode output signal that should have no effect on the following sense amplifier, *SA*1.

V. Sense Amplifiers

Fig. 5 shows the circuit schematic for the autocalibrated regenerative sense amplifier *SA*1. The positive feedback loop providing regeneration consists of a differential pair, $M3$ and $M4$, and the source followers $M5$ and $M6$. The PMOS input transistors, $M1$ and $M2$, serve to unbalance the loop, in response to the input voltage difference, at the beginning of the regeneration cycle. They also function as active loads for the $M3, M4$ differential amplifier. An essential feature of this sense amplifier is the use of capacitive signal coupling at both the inputs ($C1$ and $C2$) and within the feedback loop ($C3$ and $C4$) to provide voltage level shifting as well as offset storage and cancellation. Source followers $M14$ and $M15$ buffer the positive feedback loop from transients in the following amplifier, *SA*2.

The operation of *SA*1 is governed by switches $S1-S4$. When the comparator clock *CLK* is high, during which time the analog inputs are being sampled by the input network and the inputs of *SA*1 are shorted to *GND*, the LATCH input to *SA*1 is low and *SA*1 is in the reset mode with switches $S1-S4$ closed. In this mode $S3$ and $S4$ disable the positive feedback loop, and a balanced bias condition is established by the replica bias circuit $M11-M13$ together with the common-mode negative feedback loop formed by source followers $M5$ and $M6$ and the current sources $M7$ and $M8$. When the amplifier reaches the steady state in the reset mode, the bias voltages, including dc offsets, corresponding to a balanced condition in the regeneration loop are stored on the capacitors $C1-C4$.

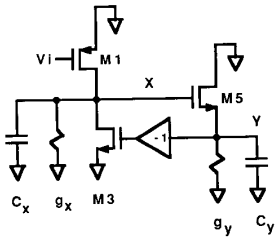


Fig. 6. Small-signal equivalent differential half-circuit for *SA*1 in regeneration mode.

Regeneration in *SA*1 is initiated by the opening of switches $S1-S4$ when *CLK* falls (LATCH goes high). At the same time, INS changes to the hold mode, and the difference between the INS outputs is coupled through $C1$ and $C2$ to the input transistors $M1$ and $M2$ in *SA*1. This difference establishes the initial imbalance in *SA*1 and triggers the regeneration. For this design, the outputs of *SA*1 are restored to a dc level of approximately 2.1 V in the reset mode; during regeneration the outputs settle to levels of 2.5 and 0.2 V.

The basic regeneration process in *SA*1 can be analyzed using the small-signal differential half-circuit model shown in Fig. 6. In this equivalent circuit, $M1$ represents the input transistors $M1$ and $M2$ in *SA*1, $M3$ corresponds to the differential pair $M3$ and $M4$, and $M5$ models the source followers $M5$ and $M6$. C_x and C_y represent the total equivalent small-signal capacitance to ground at nodes X and Y, including gate, source/drain junction, and interconnection capacitances. g_x and g_y are the equivalent small-signal conductances to ground at X and Y; g_x includes the output conductances of transistors $M1$ and $M3$, while g_y represents the output conductances of the source follower $M5$ and its current source. Thus, in the circuit of Fig. 6 transistors $M1$, $M3$, and $M5$ simply represent the equivalent transconductances of the corresponding transistors in *SA*1.

If the output conductances g_x and g_y are negligible in comparison with the transconductances of $M1$, $M3$, and $M5$, then the regeneration transient response of *SA*1 is governed primarily by two characteristic frequencies ω_3 and ω_5, where ω_3 is the unity-gain bandwidth of the $M3$, $M4$ differential pair driving the load capacitance represented by C_x, and ω_5 is the unity-gain bandwidth of the source followers $M5$ and $M6$ driving the capacitance represented by C_y. The regeneration transient waveform of the differential voltage V_y between the source nodes of M_5 and M_6 can be approximated by the following equation:

$$V_y = -V_i \times \frac{g_{m1}}{g_{m3}} K \times e^{t/\tau_r} \tag{6}$$

where

$$\tau_r = \frac{2}{\omega_5 \left[\sqrt{4\frac{\omega_3}{\omega_5} + 1} - 1\right]} \tag{7}$$

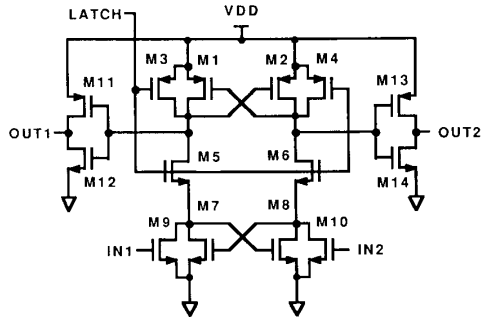


Fig. 7. Sense amplifier *SA*2.

and

$$K = \frac{1}{2}\left[1 + \frac{1}{\sqrt{4\frac{\omega_3}{\omega_5} + 1}}\right]. \tag{8}$$

In (6) V_i is the amplitude of the step input waveform, while g_{m1} and g_{m3} are the equivalent transconductances of transistors $M1$ and $M3$. In calculating values for ω_3, ω_5, g_{m1}, and g_{m3} it is important to take into account the reduction of the transistors' equivalent transconductance due to voltage division in the capacitor-coupling networks at the inputs of both the $M1, M2$ and $M3, M4$ pairs.

From (6) it is apparent that the initial imbalance for regeneration is provided by the input V_i scaled by K and g_{m1}/g_{m3}. Since the positive feedback loop includes both the $M3, M4$ differential pair and the source followers $M5$ and $M6$, the regeneration time constant τ_r is a function of both ω_3 and ω_5. It is therefore crucial that both of these "bandwidths" be as large as possible for high-speed applications.

Once the difference between the outputs of *SA*1 reaches at least 100 mV, the second sense amplifier *SA*2 can be switched to the regeneration mode while *SA*1 is reset. The circuit schematic for *SA*2 is given in Fig. 7. This design is based on the latch used in a previously reported comparator [7]. During regeneration the outputs of *SA*2 settle to full-CMOS logic levels of V_{DD} and *GND*.

Fig. 8 shows simulated transient waveforms at the outputs of *SA*1 and *SA*2 for a sampling rate of 100 MHz. These waveforms were obtained for a worst-case overdrive condition where the difference between the inputs to the comparator changes from the maximum differential input of 2 V to the specified minimum resolvable difference of 4 mV. From these simulations, the equivalent regeneration time constant for *SA*1 is estimated to be 1.22 ns, while that for *SA*2 is 0.42 ns.

VI. Experimental Results

The pipelined comparator has been integrated in a standard 2-μm CMOS technology, and a photograph of the die is shown in Fig. 9. The area of the circuit is $441 \times 100\ \mu m^2$. The coupling capacitors in *SA*1, $C1$–$C4$, can be realized simply with enhancement NMOS transistors since under

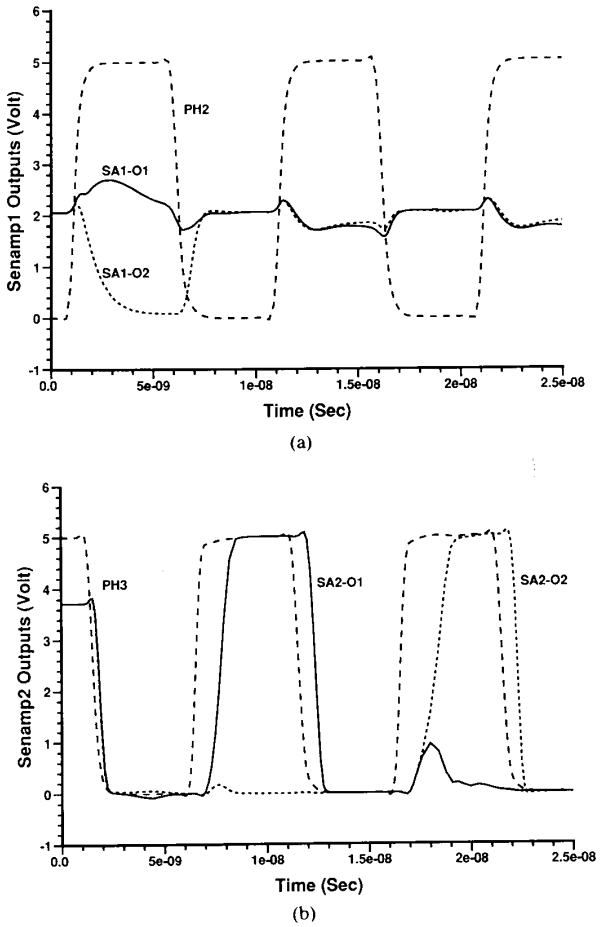


Fig. 8. Simulated transient waveforms at the outputs of *SA*1 and *SA*2 for a clock rate of 100 MHz. (a) *SA*1 outputs. (b) *SA*2 outputs.

normal bias conditions they will be kept in strong inversion. However, specific capacitor structures are needed to implement the capacitors in the input sampling network. Wherever possible a folded layout arrangement of the transistors is used to minimize the parasitic junction capacitance at critical nodes. That is, two devices of the same type and channel width share a common drain/source region at the critical nodes.

The performance of the integrated comparator has been characterized experimentally by measuring its input sensitivity V_{sn} and residual input-referred offset V_{os}. These parameters are defined in terms of dc input levels as shown in Fig. 10, and measured as functions of the clock rate. The input sensitivity is a measure of the range of dc input differences for which the output of the comparator is uncertain, and the input-referred offset is simply the displacement of the center of this uncertainty range from zero.

Measured values of V_{sn} and V_{os} at room temperature for two typical chips are plotted in Fig. 11 as functions of the sampling rate. As indicated in Fig. 11, V_{sn} remains less than 4 mV out to sampling rates as high as 100 MHz. The residual offset is less than 2 mV up to sampling rates of

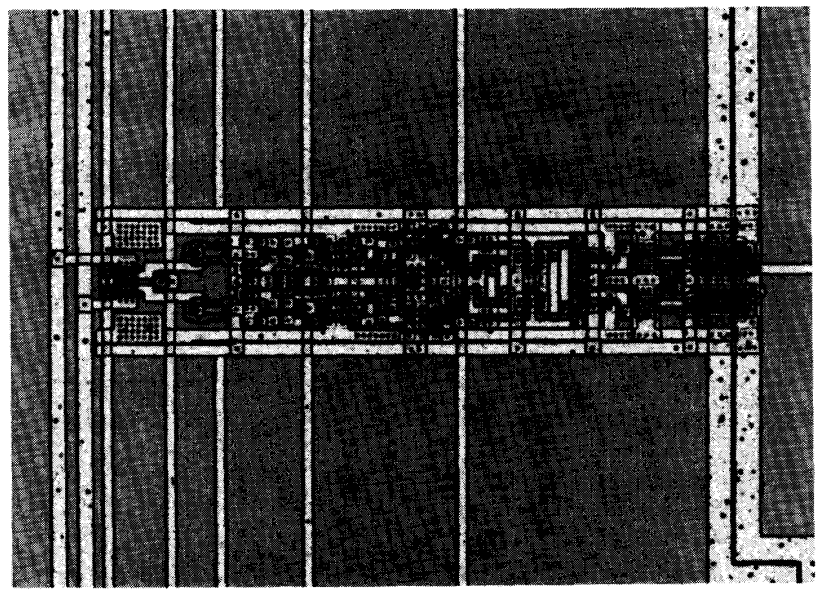


Fig. 9. Photograph of the comparator test die.

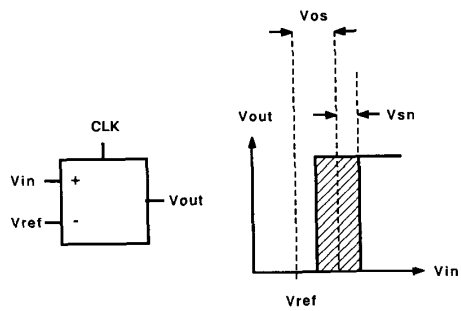
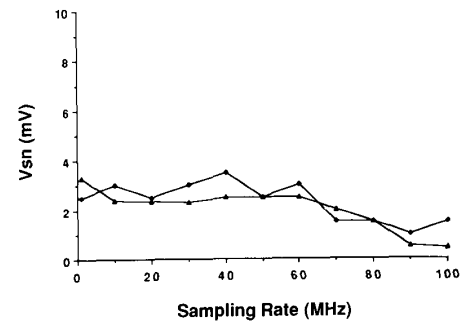


Fig. 10. Definition of comparator sensitivity V_{sn} and input-referred offset V_{os}.



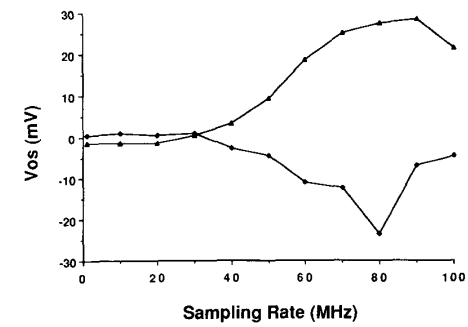
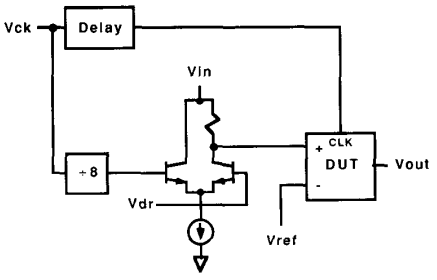


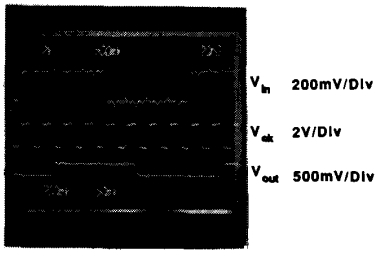
Fig. 11. Measured (a) sensitivity and (b) offset at room temperature for two typical experimental circuits.

nearly 40 MHz. Above 40 MHz, the increase in V_{os} is believed to be a consequence of clock-feedthrough overshoot and ringing at the inputs of the comparator. Simulations and experimental observations indicate that there is substantial clock feedthrough from the input sampling network into the comparator input nodes. As a result of the imperfect termination of the inputs, and in particular the inductive nature of these terminations, substantial overshoot and ringing occur; overshoot amplitudes greater than 100 mV have been observed. It is the mismatch in these feedthrough waveforms that results in the increased equivalent offset above 40 MHz. Since there is no increase in V_{sn} at sampling rates above 40 MHz, and since the circuit does not exhibit any measurable hysteresis up to clock rates of over 100 MHz, the increase in V_{os} does not appear to be the result of residual charge storage.

The overdrive recovery of the comparator has been examined using the test configuration shown in Fig. 12(a). In this experiment a square-wave signal was applied to one of the inputs of the comparator and a precisely variable dc reference, V_{ref}, was applied to the other. The square wave and reference were adjusted so that the difference between the inputs stepped from a relatively large value of 300 mV to within the minimum resolvable differential input. The input square wave was synchronized to the sampling clock with a frequency of one-eighth the sampling rate, resulting in an equivalent data pattern of 00001111 $\cdots$. Fig. 12(b)



(a)



(b)

Fig. 12. Overdrive recovery performance. (a) Test circuit. (b) Photograph of typical comparator response.

TABLE I
COMPARATOR PERFORMANCE SUMMARY

Comparator in 2μm CMOS Technology	
Sensitivity @ 100MHz	< 4 mV
Single Power Supply	+5 V
Power Dissipation @ 100 MHz	
SA1	2.01 mW
SA2	1.20 mW
S-R latch	0.38 mW
Total	3.59 mW
Input Range	0–3 V
Input Capacitance	550 fF
Area	441×100 μm^2

shows a photograph of the response of a typical comparator chip to the overdrive recovery test when the input difference changed from -300 mV to a positive value less than $+4$ mV. On the basis of such tests it was determined that a resolution of better than 4 mV was maintained from low frequencies up to sampling rates as high as 40 MHz.

The performance of the integrated comparator circuit is summarized in Table I.

VII. CONCLUSION

Since the amplification required in a comparator need not be linear, nor continuous in time, substantial reductions in delay and power dissipation can be achieved through performing comparisons directly by means of regenerative sensing. Thus, regenerative sensing and the analog pipelining capability inherent in MOS technology have been exploited to significantly improve the performance obtainable in high-speed CMOS comparators. Comparisons at rates as high as 100 MHz have been achieved in a 2-μm CMOS technology by combining a pipelined cascade of two regenerative sense amplifiers with a passive input sampling network that cancels the common-mode input voltage. Offset cancellation was incorporated within the first sense amplifier to achieve a resolution of 8 bits at clock rates as high as 40 MHz. The comparator circuit is fully differential, operates from a single +5-V supply, and dissipates only 3.6 mW when operating at its maximum sampling rate. It is thus suitable for use in the design of fully parallel high-speed A/D converters, as well as a variety of other instrumentation and communications circuits.

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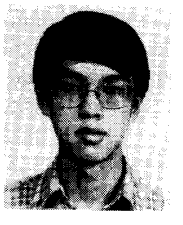

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