A 0.7-V 0.6-μW 100-kS/s Low-Power SAR ADC With Statistical Estimation-Based Noise Reduction

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***Abstract*— This paper presents a power-efficient noise reduction technique for successive approximation register analog-to-digital converters (ADCs) based on the statistical estimation theory. It suppresses both comparator noise and quantization error by accurately estimating the ADC conversion residue. It allows a high signal-to-noise ratio (SNR) to be achieved with a noisy low-power comparator and a relatively low resolution digital-to-analog converter (DAC). The proposed technique has low hardware complexity, requiring no change to the standard ADC operation except for repeating the least significant bit (LSB) comparisons. Three estimation schemes are studied and the optimal Bayes estimator is chosen for a prototype 11-b ADC in 65-nm CMOS. The measured SNR is improved by 7 dB with the proposed noise reduction technique. Overall, it achieves 10.5-b effective number of bits while operating at 100 kS/s and consuming 0.6 μW from a 0.7-V power supply.**

***Index Terms*— Analog-to-digital converter (ADC), comparator noise, data converter, high resolution, low power, statistical estimation, successive approximation register (SAR).**

I. Introduction

RAPID advances in wireless sensor nodes and biomedical devices place demanding requirements on low power and high resolution analog-to-digital converters (ADCs) [1], [2]. Successive approximation register (SAR) ADC is a popular choice due to its simple architecture and short development cycle. It can achieve an excellent power efficiency of only a few femtojoule (fJ) per conversion step, especially at low resolution with a target effective number of bits (ENOB) below 10 b [3], [4]. Despite these advantages, it is nontrivial to design a high resolution SAR ADC and maintain a high power efficiency when extending the resolution beyond 10 b. To reach higher signal-to-noise ratio (SNR), the comparator noise needs to be reduced. This can be accomplished by brute-force analog scaling, but it requires four times the comparator power for every 1-b reduction in noise [5]. The other challenge for a high-resolution SAR ADC is its exponentially growing capacitive DAC size and power. Facing these challenges, it is highly desirable to develop a more efficient way to increase SAR ADC resolution without significantly increasing the comparator power and the DAC size.

There are prior works that can reduce the comparator power and noise. The technique of [6] arranges two comparators with different noise and power levels. Its limitation is that the offsets of the two comparators need to be tightly matched, which is nontrivial at high resolution. To address this issue, the majority voting technique is developed [7]. It uses only one low-power high-noise comparator. When low comparator noise is needed at critical decision points, the comparator is fired multiple times and the decision is made via majority voting. However, it requires a carefully tuned metastability detector to sense the comparator input voltage. A similar technique using an optimized vote allocation is reported in [8]. The majority voting technique of [7] and [8] can reduce the comparator noise, but they do not make *full* use of the information embedded in the voting results. It only cares about whether there are more "1"s or more "0"s, and uses it *only* to make a 1-b majority decision. It does not take advantage of the detailed distributions of "1"s and "0"s, which carry valuable information.

This paper presents a statistical estimation-based technique that can reduce both the comparator noise and the quantization error in SAR ADCs. Its circuit implementation is simple. It does not require any change to the standard SAR ADC operation except for repeating the last LSB comparison for multiple times [9]. It exploits *all* the information embedded in the comparator output distribution, not just making a binary majority decision for the LSB bit as in [7] and [8], but to estimate the magnitude of the comparator input voltage. A useful property of an SAR ADC is that the comparator input voltage is the ADC conversion residue. If we are able to estimate the residue, we can subtract it from the ADC output to increase the ADC resolution. Note that this reduces not only the comparator noise, but also the quantization error, which is impossible with prior works [6]–[8]. Although a "1"-b high-noise comparator cannot provide an accurate estimation for its input if used only once, we can improve the estimation accuracy by repeating the comparison for multiple times and examining the number of comparator outputs being "1" or "0." It turns out that the estimation of an unknown value via multiple noisy binary tests is a classic *statistical estimation problem* [10]. Thus, we can directly borrow the concepts and theories from *statistics* to solve our estimation problem. Specifically, this paper discusses three widely used statistical

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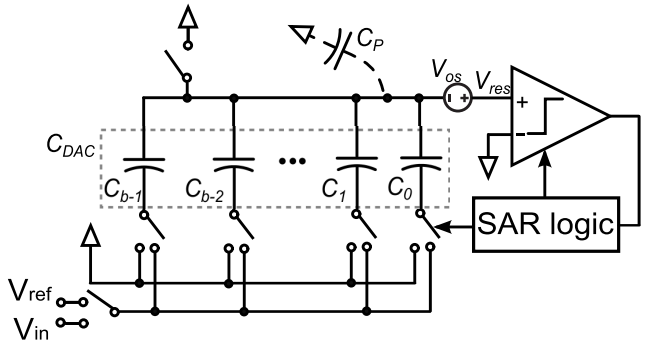

Fig. 1. Diagram for a b-bit SAR ADC.

estimators: the averaging-based estimator, the maximum likelihood estimator (MLE), and the Bayes estimator (BE). Out of them, the BE achieves the lowest estimation error, and thus, is chosen for our proposed SAR ADC.

This paper introduces the statistical estimation theory to the field of ADC design and offers a new perspective. The theories from statistics are helpful when we deal with multiple noisy comparator outputs, as in our case. The concept of statistical estimation has been used in prior studies. For example, the stochastic flash ADC of [11] exploits random offsets in an array of comparators to obtain a 6-b estimation of its input. Recently, it has been used as a back end of an SAR ADC [13]. Though independently developed, the work of [13] shares a similar big picture as our work as it uses multiple comparison results to estimate the SAR conversion residue. However, this paper has two key advantages for our intended applications both in the choice of the estimator and the circuit. First, the work of [13] uses MLE, which is a suboptimal choice compared with the BE used in this paper. Second, it arranges 16 different comparators for the LSB estimation. Their offsets need to be carefully calibrated, which is a big burden especially for high resolution applications and considering process, voltage, and temperature (PVT) variations. By contrast, we just reuse the original comparator in the SAR ADC, and thus, do not have the offset mismatch problem. Our tradeoff is reduced conversion speed as it requires a larger number of comparison cycles. Yet, for the intended low-speed sensor applications, the speed penalty is a minor issue.

To validate the proposed noise reduction technique, a prototype 11-b SAR ADC is implemented in 65-nm CMOS. Using the proposed technique, the SNR is improved by 7 dB, which matches well with the theoretical prediction. Overall, the prototype ADC achieves an ENOB of 10.5 b at 100 kS/s while consuming 0.6 μW of power from a 0.7-V supply.

This paper is organized as follows. Section II describes the basic idea of the proposed technique. Section III discusses three statistical estimators. Section IV presents the prototype ADC design. Section V shows measurement results. The conclusion is given in Section VI.

II. Statistical Estimation-Based Noise Reduction Technique: Basic Idea

Fig. 1 shows the simplified block diagram of a single-ended b-bit bottom-plate sampled SAR ADC. We can derive the following relationship between the ADC input V_{in} and the output D_{out}:

$$D_{\text{out}} = V_{\text{in}} + n_s + V_{\text{os}} + V_{\text{res}} \quad (1)$$

where n_s represents the sampling kT/C noise, V_{os} is the comparator offset, and V_{res} is the conversion residue with V_{os} taken out. Here, for simplicity of presentation, we have made two assumptions that do not undermine the practicality of the proposed technique: 1) we assume the parasitic capacitor $C_P = 0$; it can be added in (1) by applying a scaling factor to V_{res} and V_{os} and 2) we ignore the effect of capacitor mismatch. In practice, if capacitor mismatch is a problem, classic mismatch calibration techniques [14] can be applied.

As shown in (1), the ADC conversion error, defined as $(D_{\text{out}} - V_{\text{in}})$, consists of n_s, V_{os}, and V_{res}. V_{os} acts as a global ADC offset and does not affect the SNR. n_s is directly added to V_{in} during the sampling phase. To reduce n_s, the only option is to increase the DAC capacitance C_{DAC}, which is not the focus of this paper. In an SAR ADC, its noise is typically dominated by V_{res} [7], [19], [20]. Thus, this paper focuses on reducing V_{res}. V_{res} consists of three parts: the quantization error, the comparator noise, and the DAC noise. If the ADC does not have any comparator noise or DAC noise, V_{res} is simply the quantization error and is uniformly distributed between $\pm 1/2$ LSB. By contrast, in the presence of large comparator noise (in an SAR ADC the comparator noise is typically much large than the DAC noise), V_{res} is Gaussian distributed with a standard deviation close to the comparator noise. To reduce V_{res}, a straightforward way is to use a low-noise comparator and a high-resolution DAC; however, both lead to greatly increased circuit power.

This paper proposes a power efficient way to reduce V_{res}. The core idea is that if we can estimate V_{res}, denoted as $\hat{V}_{\text{res}}$, we can increase the ADC SNR by subtracting $\hat{V}_{\text{res}}$ from D_{out}

$$D^*_{\text{out}} = D_{\text{out}} - \hat{V}_{\text{res}} = V_{\text{in}} + n_s + V_{\text{os}} + (V_{\text{res}} - \hat{V}_{\text{res}}) \quad (2)$$

which shows that the noise of the new ADC output D^*_{out} is limited not by V_{res} but by the estimation error $(V_{\text{res}} - \hat{V}_{\text{res}})$. An interesting note is that if the estimation error can be made small, the SNR of D^*_{out} can even surpass the limit set by the ADC quantization error. This implies that the proposed technique can actually permit, for example, an SAR ADC with a b-bit DAC array to reach more than b-bit resolution.

Now with the core idea captured in (2), the key question is how we can estimate V_{res}. Since V_{res} is readily available at the comparator input, we propose to use the original noisy SAR comparator to estimate V_{res}. This may appear counterintuitive, because the comparator can only provide a binary decision and its output is error prone due to its high noise. Certainly, one-time comparison is insufficient. What we propose is to simply repeat the LSB comparison for a total of N times and estimate V_{res} by examining the number of "1"s, denoted as k. This is doable because the comparator output carries information on its input. Qualitatively speaking, if $k = N$, we know that V_{res} is most likely a large positive value; if $k = 0$, V_{res} is most likely negative with a large magnitude, and if $k = N/2$, V_{res} is highly probable to be close to zero.

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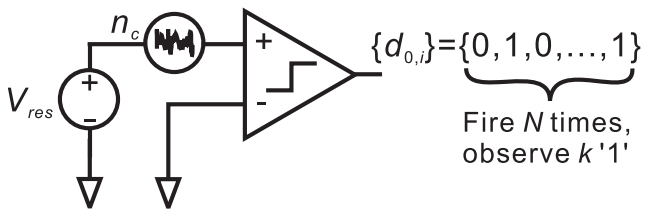

Fig. 2. Simplified SAR ADC model during the LSB comparison.

III. Proposed Statistical Estimators

After presenting the basic idea of our proposed noise reduction technique, we now quantitatively answer what is the optimum choice of the estimator $\hat{V}_{\text{res}}$ given the number of LSB comparisons N and the number of "1"s k. Let us focus our attention on the repeated LSB comparison, whose model is shown in Fig. 2. $d_{0,i}$ presents the ith LSB comparison result, where i is from 1 to N. n_c represents the total noise referred to the comparator input. It includes both the comparator noise and the DAC noise. It is typically dominated by the comparator noise. n_c is zero mean, and we denote its standard deviation as σ in the following discussion. Our goal is to form an estimator $\hat{V}_{\text{res}}$ that minimizes the mean square error (mse), defined as

$$\text{MSE} = \text{Var}(V_{\text{res}} - \hat{V}_{\text{res}}) = E[(V_{\text{res}} - \hat{V}_{\text{res}})^2] \tag{3}$$

where Var and E stand for statistical variance and expectation, respectively [10]. Specifically, we discuss three widely used statistical estimators: the simple averaging based estimator, the MLE, and the BE. They all can be implemented as precomputed lookup tables with similar hardware costs.

A. Estimator Based on Averaging

One straightforward way to define $\hat{V}_{\text{res}}$ is $+1$ LSB for all straight "1"s, -1 LSB for all straight "0" s, and performing linear interpolation for other values of k, as follows:

$$\hat{V}_{\text{res,avg}}(k) = \frac{2k - N}{N}. \tag{4}$$

Although $\hat{V}_{\text{res,avg}}$ is easy to construct, it has several drawbacks. First, because $\hat{V}_{\text{res,avg}}$ is bounded by ± 1 LSB, it cannot estimate V_{res} that is outside of that range. This can be observed from Fig. 3 that plots the mse of $\hat{V}_{\text{res,avg}}$ as a function of V_{res}, N, and the comparator noise σ. If the comparator noise σ is large, there is a high probability for $|V_{\text{res}}| > 1$ LSB, and $\hat{V}_{\text{res,avg}}$ does not work well. Second, the shape of its mse curve varies substantially with the comparator noise σ. The reason is that the comparator noise affects the value of k, but such influence is not captured in (4). The overall best performance for $\hat{V}_{\text{res,avg}}$ in terms of a small and relatively flat mse is obtained only when the comparator noise σ is close to 1 LSB [see Fig. 3(c)]. This limits its applicability. Furthermore, although its mse decreases as N increases, the region with a small mse becomes narrower (see Fig. 3). For a nonzero V_{res}, the mse of $\hat{V}_{\text{res,avg}}$ does not decrease to 0 even if N goes to infinity. The reason is that $\hat{V}_{\text{res,avg}}$ is a biased estimator of V_{res}, and the bias does not converge to zero [10].

B. Maximum Likelihood Estimator

A key reason that $\hat{V}_{\text{res,avg}}$ does not achieve a low estimation error is that it does not assume any prior information on the comparator noise σ. In practice, σ is chosen by the designer. It can be extracted via SPICE simulations or obtained by performing a simple foreground estimation. We can set $V_{\text{in}} = 0$ by shorting the ADC input, and monitor the standard deviation of D_{out}. Since we have assumed that comparator noise σ is the dominant random source, the standard deviation of D_{out} simply reflects the value of σ. Given this, we can take advantage of σ to form a much better estimator, which is the MLE.

The definition of MLE is easy to understand. Given the number of comparisons N and the number of "1"s k, we define the estimator $\hat{V}_{\text{res}}$ to be the value that maximizes the probability of observing k "1"s out of N comparisons. MLE has been thoroughly studied in statistics and has several merits. First, it is consistent. As N increases, $\hat{V}_{\text{res,MLE}}$ converges to V_{res} and can achieve arbitrary precision [10]. Second, it is highly efficient from the information usage point of view. It achieves the Cramer–Rao lower bound as N goes to infinity, which means that MLE achieves the lowest asymptotic mse [10]. We can derive $\hat{V}_{\text{res,MLE}}$ for our problem [10]

$$\hat{V}_{\text{res,MLE}}(k) = \sigma \cdot F^{-1}\left(\frac{k}{N}\right) \tag{5}$$

where $F(x)$ is the cumulative distribution function of the normal distribution with mean of 0 and variance of 1. Equation (5) shows that $\hat{V}_{\text{res,MLE}}$ is linearly proportional to the comparator noise σ. This is different from $\hat{V}_{\text{res,avg}}$ that has no dependence on σ [see (4)].

$\hat{V}_{\text{res,MLE}}$ defined in (5) has one limitation that it does not work for $k = 0$ and $k = N$. If we plug $k = 0$ or $k = N$ into (5), $\hat{V}_{\text{res,MLE}}$ is $\pm\infty$. This is expected because $\hat{V}_{\text{res,MLE}} = -\infty$ achieves the highest probability for $k = 0$, and $\hat{V}_{\text{res,MLE}} = \infty$ ensures that $k = N$. This issue may be minor for a large N, because the probability of $k = 0$ and $k = N$ would approach zero. However, for a small N, $k = 0$ and $k = N$ do appear, which causes an estimation failure. To solve this problem, we redefine $\hat{V}_{\text{res,MLE}}(0) = \sigma \cdot F^{-1}(0.2/N)$ and $\hat{V}_{\text{res,MLE}}(N) = \sigma \cdot F^{-1}(N - 0.2/N)$. For other k lies in $[1, N-1]$, we still follow the definition of (5). Fig. 4 shows $\hat{V}_{\text{res,MLE}}$ as a function of k and N. Different from $\hat{V}_{\text{res,avg}}$, the relationship between $\hat{V}_{\text{res,MLE}}$ and k is nonlinear. The range of $\hat{V}_{\text{res,MLE}}$ expands with N, from $\pm 1.6\sigma$ at $N = 3$ to $\pm 2.3\sigma$ at $N = 15$. This means that $\hat{V}_{\text{res,MLE}}$ can approximate a wider range V_{res} as N increases.

To evaluate how accurate $\hat{V}_{\text{res,MLE}}$ is, we plot its estimation error as a function of V_{res} and N in Fig. 5. In general, its mse decreases as N increases. For the same N, its mse is small for a small V_{res} value, but increases as the amplitude of V_{res} increases. The reason is that the value of $\hat{V}_{\text{res,MLE}}$ is bounded for a given N (see Fig. 4) and, thus, does not work well for a very large V_{res}. However, unlike $\hat{V}_{\text{res,avg}}$, the range of $\hat{V}_{\text{res,MLE}}$ increases with N, and thus, its region with a small mse is broadened. This is a key advantage of $\hat{V}_{\text{res,MLE}}$ compared to $\hat{V}_{\text{res,avg}}$. It enables $\hat{V}_{\text{res,MLE}}$ to accurately estimate a wide range of V_{res} especially for a large N.

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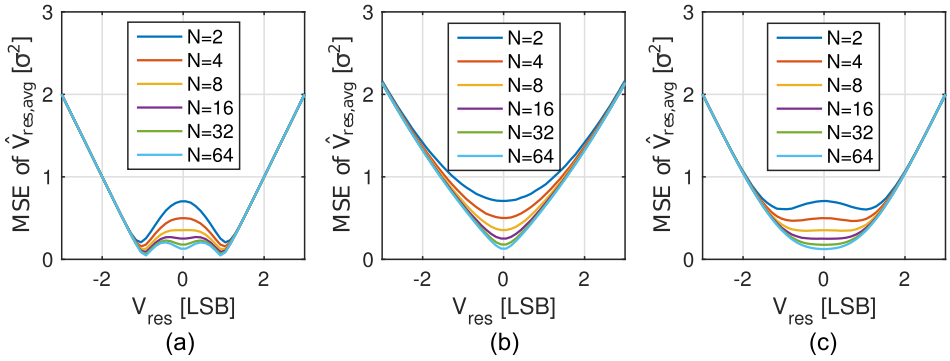

Fig. 3. MSE of $\hat{V}_{\text{res,avg}}$ for various N. (a) $\sigma = 0.5$ LSB. (b) $\sigma = 2$ LSB. (c) $\sigma = 1$ LSB.

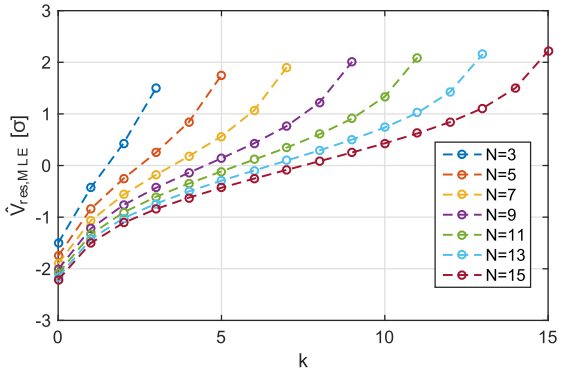

Fig. 4. Value of $\hat{V}_{\text{res,MLE}}$ as a function of N and k.

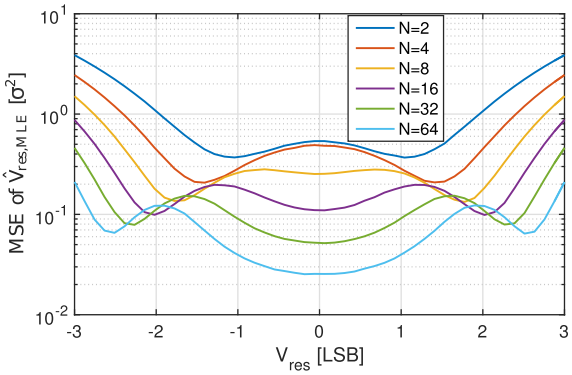

Fig. 5. MSE of $\hat{V}_{\text{res,MLE}}$ for different values of V_{res}.

C. Bayes Estimator

MLE is a significant improvement over the simple averaging based estimator, but it still does not achieve the lowest estimation error. There is one extra piece of information that MLE does not make use of, which is the distribution of V_{res}. Fig. 6 shows the simulated histograms of V_{res} for an 11-b SAR ADC assuming the comparator noise $\sigma = 1$ LSB. Three different input signals are used. Sinusoidal inputs with -6 and -20 dBFS are used in Fig. 6(a) and (b), respectively. A Gaussian random input with a standard deviation of 10% ADC full swing is used in Fig. 6(c). As can be seen, there is negligible difference in the V_{res} distribution among the three cases. They are all close to Gaussian distribution with zero mean and a standard deviation of 1 LSB. This shows that the distribution of V_{res} has very weak dependence on the ADC input V_{in}. This is not hard to understand especially in a power optimized design where the comparator noise usually dominates over the quantization noise. By the end of the 11-b SAR conversion, the conversion residue V_{res} is almost completely uncorrelated with V_{in}, and is basically set by the comparator noise. Given this observation, we can approximate V_{res} as a Gaussian random variable and its probability density function (pdf) $g(V_{\text{res}}) \equiv f(V_{\text{res}}/\sigma)$, where $f(\cdot)$ is the pdf of Gaussian distribution with zero mean and standard deviation of 1.

Now let us derive the BE. For simplicity, let us consider an example of $N = 3$. We can have four different values for k, which is 0, 1, 2, and 3. For each case, we can calculate the posterior distribution $g(V_{\text{res}}|k)$ using the Bayes theorem [10]

$$g(V_{\text{res}}|k) = \frac{P(k|V_{\text{res}})g(V_{\text{res}})}{\int_{-\infty}^{+\infty} P(k|V_{\text{res}})g(V_{\text{res}})dV_{\text{res}}} \tag{6}$$

where $P(k|V_{\text{res}})$ is the probability of observing k "1"s conditioning on V_{res}. Fig. 7 plots the V_{res} prior distribution $g(V_{\text{res}})$ together with its posterior distributions $g(V_{\text{res}}|0)$, $g(V_{\text{res}}|1)$, $g(V_{\text{res}}|2)$, and $g(V_{\text{res}}|3)$. Bayes rule basically allows us to update the distribution of V_{res} given the observation result k. We see that the prior and posterior distributions are different, which is enabled by the knowledge of k. For example, compared to $g(V_{\text{res}})$, the posterior distribution $g(V_{\text{res}}|0)$ is shifted toward the negative side. This is because after observing all "0"s from the comparator outputs, we can update the distribution of V_{res}, which should be more negatively biased.

The BE is defined as the mean of the posterior distribution

$$\hat{V}_{\text{res,BE}}(k) \equiv E(V_{\text{res}}|k) = \int_{-\infty}^{+\infty} V_{\text{res}} \cdot g(V_{\text{res}}|k)dV_{\text{res}}. \tag{7}$$

For the case of $N = 3$, we can calculate that $\hat{V}_{\text{res,BE}}(0) = -1\sigma$, $\hat{V}_{\text{res,BE}}(1) = -0.3\sigma$, $\hat{V}_{\text{res,BE}}(2) = +0.3\sigma$, and $\hat{V}_{\text{res,BE}}(3) = +1\sigma$, respectively. Note that (6) and (7) are computationally intensive. Fortunately, we do not need to solve $\hat{V}_{\text{res,BE}}$ for every ADC output. We only need to compute once, and store the results for all possible k values in a lookup table. This way, once we know k, $\hat{V}_{\text{res,BE}}$ can be directly obtained from the table.

The BE can be proved to achieve the minimum mse. It is easy to derive that the mse for an estimator $\hat{V}_{\text{res}}$ with the

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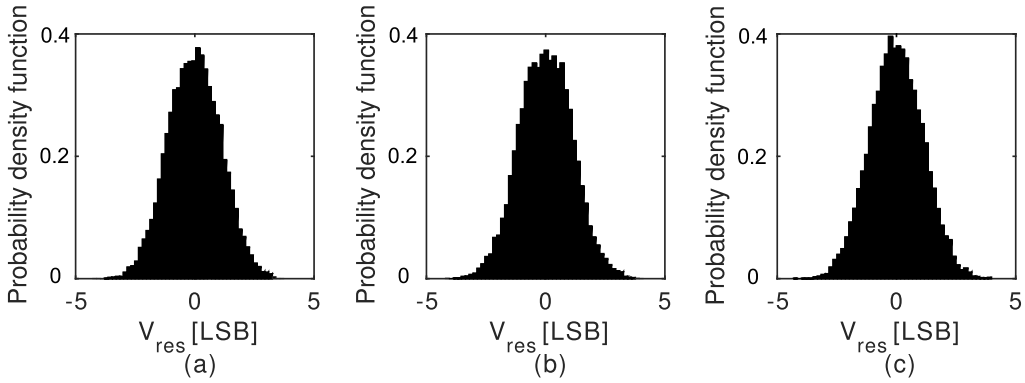

Fig. 6. Histogram of V_{res} for (a) -6 dBFS sinusoidal input, (b) -20 dBFS sinusoidal input, and (c) Gaussian random input with standard deviation of 10% ADC full range.

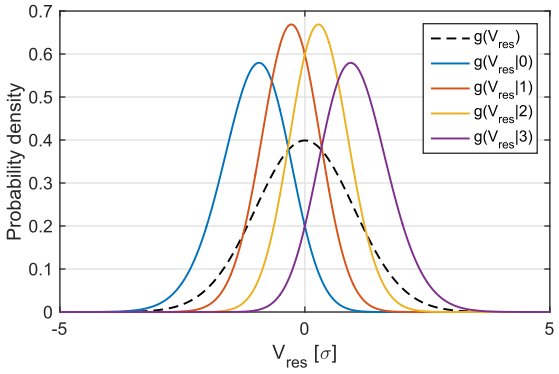

Fig. 7. Prior distribution $g(V_{\text{res}})$ and posterior distribution $g(V_{\text{res}}|k)$ for $N = 3$.

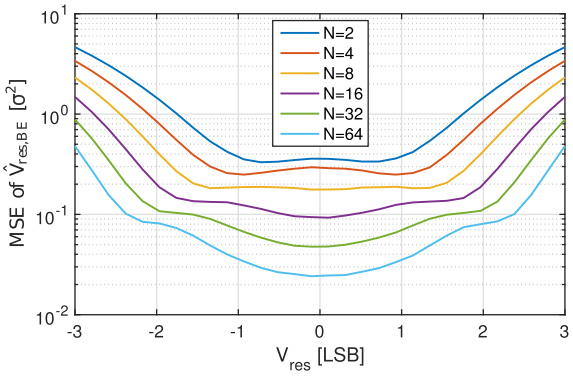

Fig. 9. MSE of $\hat{V}_{\text{res,BE}}$ for different values of V_{res}.

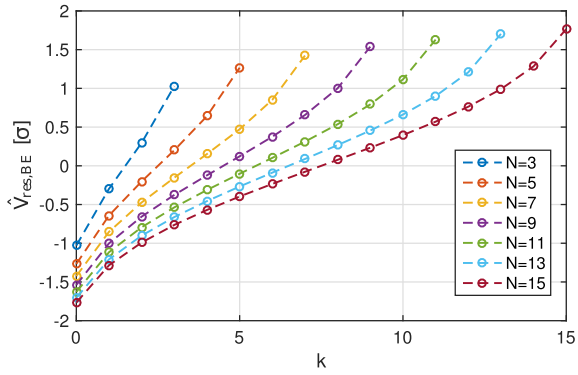

Fig. 8. $\hat{V}_{\text{res,BE}}$ as a function of N and k.

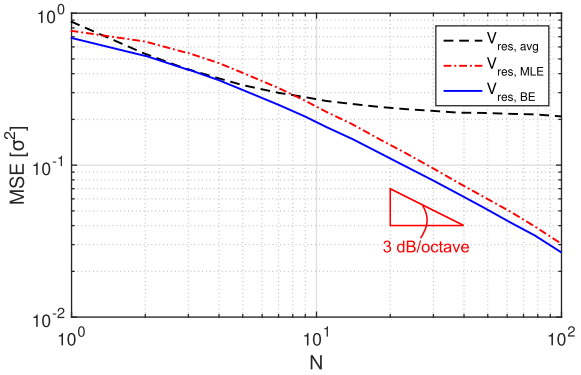

Fig. 10. MSE versus N for a normal distributed V_{res} with $\sigma = 1$ LSB.

observation k is given by

$$\begin{aligned}\text{MSE}(k) &= E[(V_{\text{res}} - \hat{V}_{\text{res}})^2 | k] \\ &= \hat{V}_{\text{res}}^2(k) - 2 \cdot E(V_{\text{res}}|k) \cdot \hat{V}_{\text{res}}(k) + E\left(V_{\text{res}}^2 | k\right). \quad (8)\end{aligned}$$

It is minimized by choosing the BE defined in (7).

Fig. 8 shows $\hat{V}_{\text{res,BE}}$ as a function of k and N. Comparing it with $\hat{V}_{\text{res,MLE}}$ shown in Fig. 4, the range of $\hat{V}_{\text{res,BE}}$ is smaller than that of $\hat{V}_{\text{res,MLE}}$. The reason is that $\hat{V}_{\text{res,BE}}$ makes use of the prior distribution of V_{res}. Since V_{res} is concentrated around zero, $\hat{V}_{\text{res,BE}}$ is biased more toward zero. Fig. 9 shows mse for $\hat{V}_{\text{res,BE}}$ as a function of V_{res} and N. Comparing it with Fig. 5 of $\hat{V}_{\text{res,MLE}}$, the mse of $\hat{V}_{\text{res,BE}}$ is smaller than that of $\hat{V}_{\text{res,MLE}}$ for a small V_{res} in $[-2\sigma, +2\sigma]$, but is slightly larger for $|V_{\text{res}}| > 2\sigma$. However, because V_{res} is known to concentrate around 0, it is expected that the overall mse of $\hat{V}_{\text{res,BE}}$ is smaller than that of $\hat{V}_{\text{res,MLE}}$.

To compare the estimation error for the three estimators, we compute the mse of $\hat{V}_{\text{res,avg}}$, $\hat{V}_{\text{res,MLE}}$, and $\hat{V}_{\text{res,BE}}$ for $\sigma = 1$ LSB, and plot them as a function of N in Fig. 10. As expected, the mse of $\hat{V}_{\text{res,BE}}$ is consistently smaller than that of $\hat{V}_{\text{res,avg}}$ and $\hat{V}_{\text{res,MLE}}$, indicating the highest estimation accuracy. The mse asymptotic slopes for $\hat{V}_{\text{res,MLE}}$ and $\hat{V}_{\text{res,BE}}$ are both 3 dB/octave, which is set by the Cramer–Rao lower bound [10].

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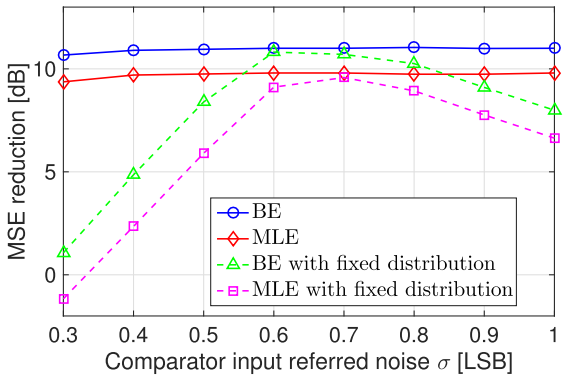

Fig. 11. MSE reduction versus various comparator noise σ.

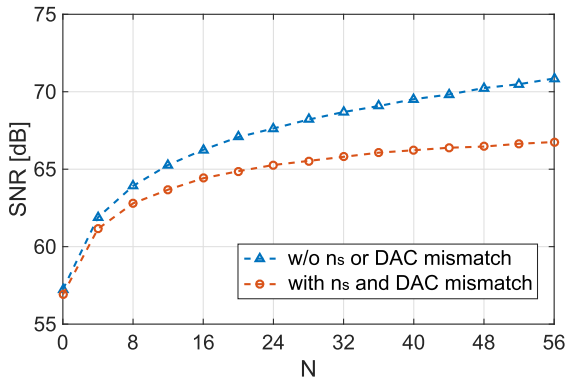

Fig. 12. Simulated SNR versus N with/without the 0.1 LSB sampling noise n_s and 1% unit capacitor mismatch.

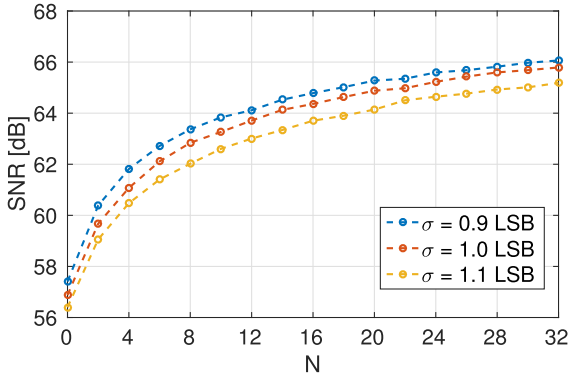

Fig. 13. Simulated SNR versus N with $\pm$10% variations in the comparator noise σ.

So far we have assumed $\sigma = 1$ LSB. The BE also works for other σ values. If σ is small, $g(V_{\text{res}})$ is no longer Guassian, but it can be obtained by either more complicated hand calculation or running behavioral simulation. Once $g(V_{\text{res}})$ is obtained, the rest of the computation for $\hat{V}_{\text{res,BE}}$ remains the same as in (6) and (7). Fig. 11 shows the simulated mse reduction versus σ for $N = 32$. BE works well and always outperforms MLE. As σ reduces, both BE and MLE become less effective. This is because statistical estimation relies on the comparator noise to randomize the comparator output. If σ is too small, the comparator outputs tends to be all "1"s or "0"s, and the information that can be extracted from the comparator output reduces. The dotted lines in Fig. 11 plot the mse reduction using fixed BE and MLE obtained at $\sigma = 0.65$ LSB. They clearly show that both BE and MLE require accurate knowledge of σ. As σ varies, both BE and MLE need to be recomputed to ensure consistent mse reduction.

D. Practical Considerations

As mentioned in Section II, the proposed technique can improve the ADC SNR by minimizing the effect of V_{res}, but it cannot reduce the sampling kT/C noise n_s, which cannot be differentiated from V_{in} after the sampling. Another source of error that cannot be reduced is the capacitor mismatch that causes DNL/INL errors. As a result, the sampling noise and the capacitor mismatch reduce the ADC SNR improvement and place an upper bound for the maximum achievable SNR. Fig. 12 shows the simulated SNR versus N for an 11-b SAR ADC with 1 LSB comparator rms noise. Without the sampling noise and the capacitor mismatch, the SNR increases at the asymptotic rate of 3 dB/octave. With 0.1 LSB rms sampling noise and 1% unit capacitor mismatch added, the SNR improvement degrades. The gap between two curves widens as N increases due to the increasing proportion of n_s and the mismatch error in the total ADC error.

Another practical issue to consider is that the comparator noise σ may not be known with 100% accuracy. Thus, it is important to examine the sensitivity of the proposed technique to the inaccuracy in the estimated value of σ. Let us assume σ is estimated to be 1 LSB from the foreground estimation. However, due to PVT variation, the value of σ changes to 0.9 or 1.1 LSB, but we still use $\sigma = 1$ LSB in the BE. Fig. 13 shows the simulated SNR versus N, including the sampling noise and the capacitor mismatch. The proposed technique still works well with 0.1 LSB inaccuracy in the value of σ. In practice, the comparator noise can vary by more than $\pm$0.1 LSB. For example, our simulation shows that the noise of the comparator used in the prototype ADC varies from 0.4 to 1 LSB across all corners, $\pm$10% power supply variation, and $-40°$ to $80°$ temperature variation. Here, we assume that the ADC reference voltage is generated from a bandgap circuit, and thus, the LSB size is insensitive to PVT variation to the first order. Our strategy to ensure the robustness of the algorithm is to precompute and prestore three lookup tables for the comparator noise σ of 0.5, 0.7, and 0.9 LSB, respectively. We track the comparator noise variation by performing a periodic foreground comparator noise estimation and, then, choose the appropriate lookup table to use. This ensures that no on-the-fly computations for the BE values are needed, which reduces the hardware complexity.

E. Comparison to Oversampling and Analog Scaling

Oversampling can also be used to reduce ADC noise by averaging. The merit of oversampling is that it reduces both the sampling noise n_s and the comparison noise n_c, while the proposed technique only reduces n_c. However, as mentioned earlier, in an SAR ADC, the noise is typically dominated by

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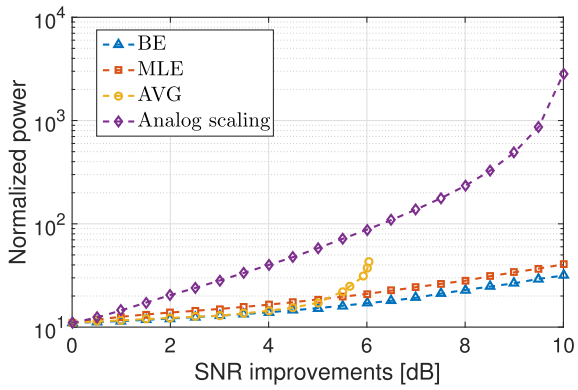

Fig. 14. Simulated normalized total comparator power versus SNR improvement for analog scaling, estimation based on averaging, MLE and BE with 11-b quantization noise.

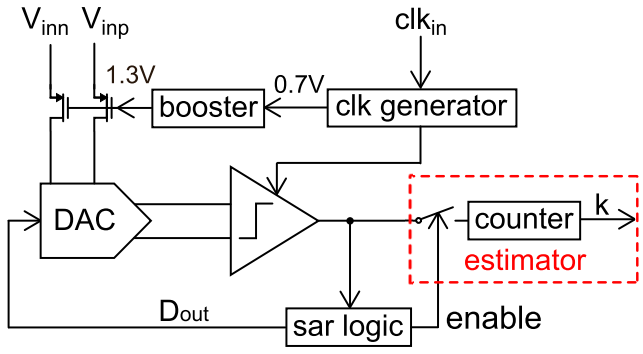

Fig. 15. Proposed SAR ADC architecture.

n_c, and thus, their effect in total noise reduction is similar. The disadvantage of oversampling is that it *cannot* improve the ADC power efficiency. Every doubling of the oversampling ratio leads to twice the ADC power, as it requires repeating all the sampling, comparison, and DAC switching operations. By contrast, the proposed technique only increases the number of LSB comparisons, so its required total number of comparator operations is much smaller. Additionally, the DAC is not switched and, thus, does not consume any extra power. Thus, the power efficiency of the proposed technique is much higher than oversampling.

As in any noise reduction technique, there is always a cost of power. Fig. 14 shows the simulated normalized total comparator power versus SNR improvement for an 11-b SAR ADC using analog scaling, the proposed estimation technique based on averaging, MLE, and BE. The total comparator power on the y-axis is normalized to the power of a comparator with the rms noise of 1 LSB firing once. As shown in Fig. 14, the SNR improvement for analog scaling is limited to 10 dB (its maximally achievable SNR is 68 dB set by the 11-b quantization noise), no matter how much more power is consumed by the comparator. The power efficiency of estimation based on averaging (AVG) is good when the SNR improvement is low. However, its SNR improvement is limited to 6 dB, which matches the analysis shown in Fig. 10. This is because the estimator based on averaging is intrinsically biased and cannot achieve consistent SNR improvement. By contrast, both MLE and BE can consistently improve SNR. Because they also reduce the quantization noise, they can even break the SNR limit set by the quantization noise. For the same SNR improvement, the power required by BE is always the lowest. It is about 20% lower than that of MLE.

IV. Prototype ADC Design

To verify the proposed technique, an 11-b prototype SAR ADC is designed, whose architecture is shown in Fig. 15. There are only two simple changes made to the standard SAR ADC architecture: 1) the SAR logic is modified to repeat the LSB comparison for $N = 17$ times and 2) a counter is used to count the number of "1"s during LSB comparisons to obtain k. A low power supply voltage of 0.7 V is chosen to demonstrate the effectiveness of the proposed technique for low voltage and low power applications.

The DAC is implemented using MoM capacitors. Since the DAC power is proportional to the total capacitance, it is desirable to reduce the unit capacitor C_u for power saving. Considering the noise and matching requirement, this design chooses $C_u = 2$ fF. A bidirectional single-side (BSS) switching technique is adopted to further reduce the DAC reference power by 86% compared to the conventional switching scheme [21], [22]. BSS reduces the number of unit capacitors by four times, leading to a small capacitor array of $\{256, 128, 64, 32, 16, 16, 8, 4, 2, 1, 1\}C_u$ for an 11-b ADC. This is helpful in reducing the total DAC capacitance when the unit comparator size is not limited by the matching requirement. Compared to the widely used monotonic switching technique of [23], BSS achieves higher SNDR as the comparator input common-mode voltage $V_{\rm cm}$ variation is reduced and $V_{\rm cm}$ can converge to half V_{dd} instead of ground. A redundant capacitor of $16C_u$ is added to recover possible errors due to incomplete DAC settling and $V_{\rm cm}$ variation during the first several MSB comparisons [21]. The total capacitance is $528C_u = 1056$ fF, leading to 88-μV differential sampling kT/C noise.

To ensure a high sampling linearity, bottom-plate sampling is used. In addition, a clock booster shown in Fig. 16(a) is employed to boost the sampling clock voltage. Thus, small nMOS transistors can be used to sample $V_{\rm in}$ instead of an array of bootstrapped switches or large CMOS switches to reduce the design complexity and the switch driving power. Fig. 16(b) shows the dynamic comparator. In this design, the SPICE simulated comparator rms noise is 480 μV or 0.7 LSB. Note that this is much larger than the sampling kT/C noise. Thus, the overall ADC noise is dominated by the comparator noise. The ADC timing diagram is shown in Fig. 16(c). It uses a synchronous clocking scheme implemented using a simple DFF-based clock divider and several AND gates. The frequency of the master clock is 32 times faster than the sampling rate. The first 4 clock cycles are used for the input sampling to ensure a high sampling linearity, the subsequent 11 cycles are used for normal SAR operation, and the final 17 cycles are used for repeated LSB comparisons. When the normal SAR operation ends, a 5-b ripple counter is enabled, which records the number of "1"s during the LSB comparisons to obtain k.

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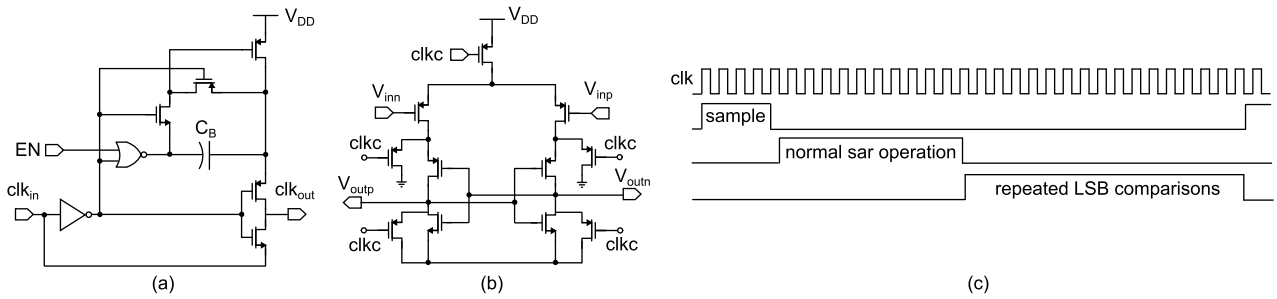

Fig. 16. Schematic of (a) clock booster, (b) comparator, and (c) timing diagram.

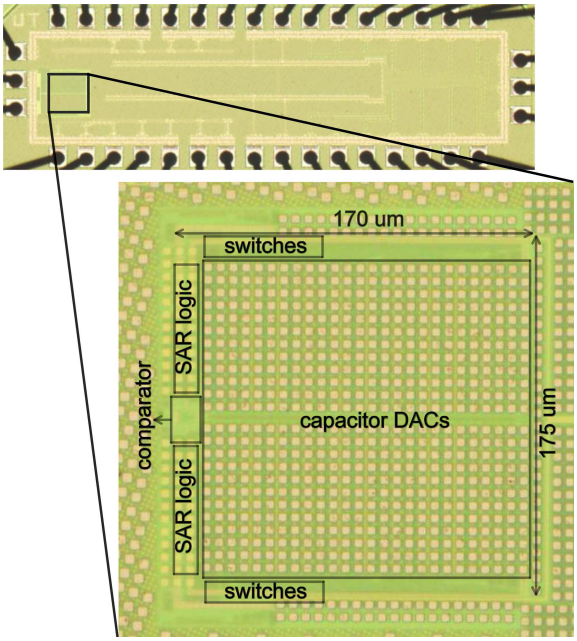

Fig. 17. Die micrograph.

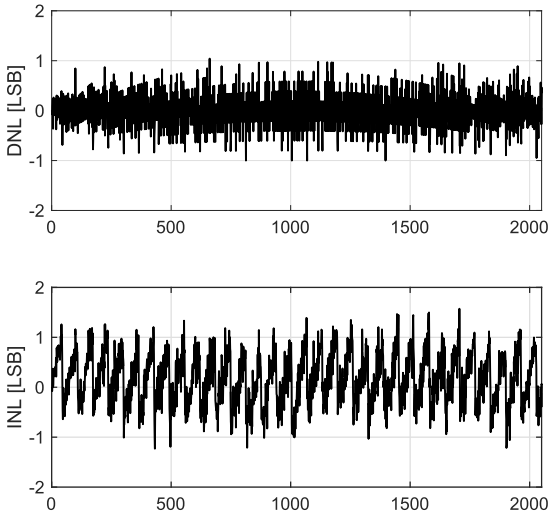

Fig. 18. Measured DNL and INL.

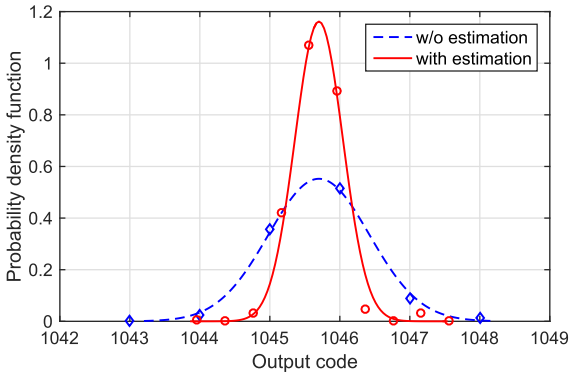

Fig. 19. D_{out} distribution with and without estimation at $V_{\text{in}} = 0$.

V. Prototype ADC Measurement Results

The prototype ADC is implemented in the 65-nm CMOS process. Fig. 17 shows the die photo. The power supply is 0.7 V. The sampling rate is 100 kS/s. Fig. 18 shows the DNL and INL, which are $+1.04/-1$ LSB and $+1.57/-1.23$ LSB, respectively. The INL plot shows a 1-LSB systematic mismatch between the 6 MSB capacitors and the 6 LSB capacitors. A simple foreground calibration of [17] is performed and the periodic INL transition pattern disappears [9].

To verify the proposed noise reduction technique, we first measure the ADC noise (e.g., the variance of D_{out}) at $V_{\text{in}} = 0$. The measured distributions of D_{out} before and after noise reduction are shown in Fig. 19 together with fitted normal distributions. Before noise reduction, the standard deviation of D_{out} is 0.73 LSB. It indicates that the comparator input referred noise is about 500 μV, which is in agreement with SPICE simulation. After noise reduction, the standard deviation of D^*_{out} is reduced by 7 dB to 0.33 LSB, which matches well with the estimation theory. Note that if the conventional SAR ADC design approach is used, the comparator noise needs to be reduced to 0.16 LSB in order for the total ADC noise to be 0.33 LSB, which also includes the 0.29 LSB quantization error. This means that the total comparator power needs to be increased by 21 times. By contrast, for our proposed technique, the total comparator power is only increased by 2.5 times, which proves its higher power efficiency compared to brute-forth analog scaling.

Fig. 20 shows the measured spectrum for a 96-kHz full-scale input sampled at 100 kS/s. The reason for choosing the 96-kHz frequency input is our high-quality low-distortion bandpass filter has a bandwidth from 90 to 110 kHz. The measured SNDR and SNR are 59.4 and 59.7 dB, respectively.

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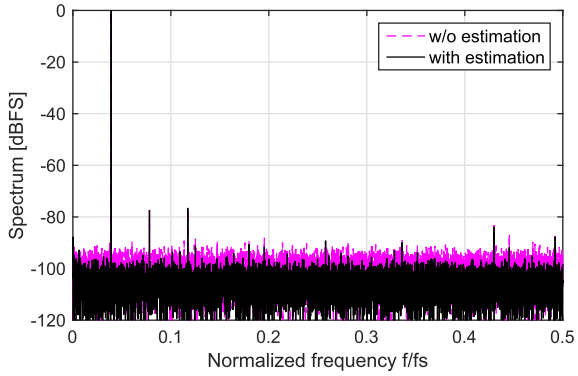

Fig. 20. Measured 2^{14}-point ADC output spectrum with 96-kHz input.

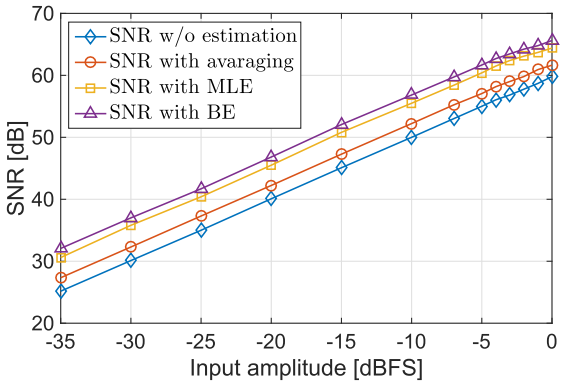

Fig. 21. Measured SNR versus input amplitudes.

After applying the proposed technique, the noise floor is lowered. SNDR and SNR are improved to 64.5 and 65 dB, respectively. The corresponding ENOB is 10.5 b.

Fig. 21 shows the measured SNR versus input amplitudes. The SNR improvement using simple averaging-based estimator $\hat{V}_{\text{res,avg}}$ is limited to only 2.2 dB. MLE achieves 5.8-dB SNR improvement. With BE, the SNR is improved by 7 dB, which is 4.8 dB better than that of averaging and 1.2 dB better than that of MLE. This matches well with the analysis in Section III. When the input is large, the SNR improvement decreases slightly to 5.3 dB, which is caused by the unwanted capacitive coupling from the ADC input to the reference lines, discovered during measurements. Such SNR loss can be recovered by layout optimization to reduce the coupling.

To evaluate the robustness of the proposed technique in the presence of errors in the extracted value of the comparator noise σ, we have tested the SNR improvement as a function of the comparator noise σ value used in the BE. Fig. 22 shows both the simulated and the measured results. As expected, the highest SNR improvement is obtained when we use the accurate σ value of 0.73 LSB. The SNR improvement decreases if an inaccurate σ value is used. Nevertheless, as long as the value of σ is within $[0.6, 0.86]$ LSB, the SNR improvement is greater than 6 dB. This shows that the proposed technique is robust and can tolerate up to 15% error in σ with less than 1-dB SNR degradation.

The prototype ADC consumes 0.6 μW from a 0.7-V power supply. The comparator, DAC, clock generator, and SAR logic

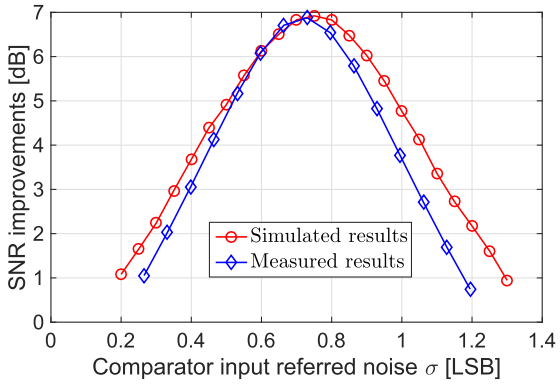

Fig. 22. Simulated and measured SNR improvements versus various comparator noise σ.

TABLE I
MEASURED PERFORMANCE SUMMARY

Process [nm]	65	
Sampling rate [kS/s]	100	
Resolution [bit]	11	
Active area [mm^2]	0.03	
Power supply [V]	0.7	
Total power [μW]	0.6	
Walden FoM [fJ/conv-step]	4.5	
With noise reduction?	No	Yes
Dynamic range [dB]	60	67
Peak SNR [dB]	59.7	65
Peak SNDR [dB]	59.4	64.5
ENOB [bit]	9.6	10.5

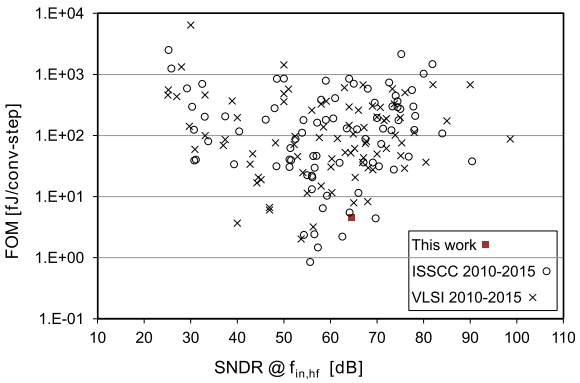

Fig. 23. FOM versus SNDR plot for this work and recently published ADCs in ISSCC and VLSI conferences.

consume 70, 102, 193, and 280 nW, respectively. With the noise reduction technique, the comparator power accounts for only 10% of the total power at the ENOB of 10.5 b. The digital power, including both clock generator and SAR logic, dominates the overall ADC power. It can be substantially reduced via optimization and/or going to a more advanced technology node, without affecting SNR. The measured Walden figure of merit (FOM) of the prototype ADC is 4.5 fJ/conversion-step. The performance of the proposed ADC is summarized in Table I. Fig. 23 shows the Walden FOM versus SNDR for

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this paper and recently published ADCs in ISSCC and VLSI conferences [24].

VI. Conclusion

This paper has presented a noise reduction technique for SAR ADC based on statistical estimation. To the best of our knowledge, this is the first work that comprehensively introduces the statistical estimation theory to the field of ADC design. The proposed technique requires minimum change to the original SAR ADC design. It can reduce both the comparator noise and the quantization error. It is suitable for applications that require low-power high-resolution SAR ADCs.

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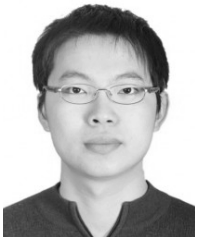

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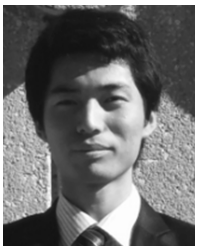

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