A Low-power, High-resolution, 1 GHz Differential Comparator with Low-Offset and Low-Kickback

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Abstract— **A high speed, high resolution and low power comparator is designed and analyzed in this work. The proposed comparator is designed in low power TSMC 65 nm CMOS technology with 1.2 V power supply. The new presented comparator also has low power consumption. High resolution of the proposed comparator and the propagation delay are less than 1 µV and 300 ps. The comparator is clocked at 1 GHz frequency and the measured power consumption in 1 GHz clock frequency is 277 µW. The offset cancellation method is also proved to be 4.29 mV by running Monte Carlo simulation with 400 iterations.**

Keywords— High speed comparator; low offset; low power; low kickback noise

I. INTRODUCTION

With the rising demand for data conversions with higher resolution, higher speeds and also lower power, analog-to-digital converters (ADCs) require careful design of comparators due to their important role in determining the ADC's performance and efficiency [1-7]. Even though dynamic comparators are more preferable in today's applications than static comparators since they offer higher speeds and reduced power consumption, other challenges like offset voltage and kickback noise arise due to the feedback capacitive path from the outputs to the input nodes. As a result, digitally-assisted circuits, multiple stages, and more complex techniques are applied to improve the comparator performance [8-10].

Comparator is one of the major blocks that plays a crucial role in analog, RF and mixed-signal domains and electronic devices especially portable ones. They have several applications such as high-gain dynamic pre-amplifier [11] and edge pursuit comparator [12] in high resolution SAR ADCs and inverter based comparator [13], VCO based comparator [14] and current mode comparator [15] in Flash ADCs.

In this paper, the conventional Comparator is explained in Section II. The original design and the analysis of the proposed comparator are discussed in Section II, followed by the modifications applied to it for performance improvements. Section III presents the obtained simulation results. Finally, the comparator performance is concluded in Section IV.

II. CONVENTIONAL COMPARATOR

Circuit diagram of the conventional comparator is shown in Fig. 1 [16]. The comparator output is pulled down in reset phase. M_1 to M_4 transistors act as a simple differential amplifier to provide the amplification of the input signal. M_6 and M_5 transistors simply mirror the current difference to the output latch. M_{10} and M_7 are turned off in the sampling phase and the latch initiates the regeneration base on the current difference. The speed is limited due to the static power consumption and dependency to the current in second stage.

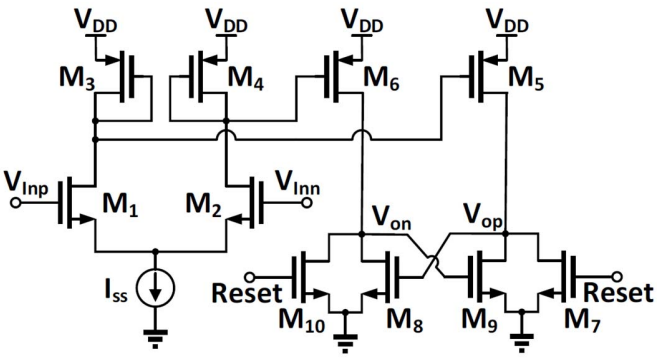

Fig. 1. Conventional comparator.

III. CIRCUIT IMPLEMENTATION

The proposed circuit is a two-stage comparator of differential nature in order to be more immune to noise and process variations. As shown in Fig. 2, the first stage is the preamplifier circuit that receives the input, the reference, and the common mode signals, and offers the amplification to the input voltage difference. The second stage is the regenerative latch that initiates the regeneration according to the voltage difference between the two inputs.

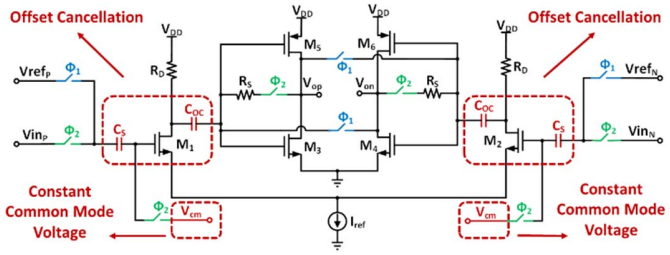

Fig. 2. Original proposed comparator circuit.

To decrease the complexity of the system, only one clock signal and its inverse are used for the sample and the reset phases respectively. During the reset phase, the latch is deactivated while the preamplifier amplifies the input difference, saving power and preventing the comparator output from saturating. The regeneration in the sample phase is very fast due to the strong back to back inverter used at the comparator output.

The original circuit is modified mostly by adding switches to significantly reduce the power consumption. The double-tail idea is applied using two tail switches that separate the regenerative latch from the power supplies during the reset mode. Additionally, the output nodes are pulled to ground when the latch is not in use. In order to further reduce the chip size along with the power, the resistive loads of the preamplifier are replaced with active loads.

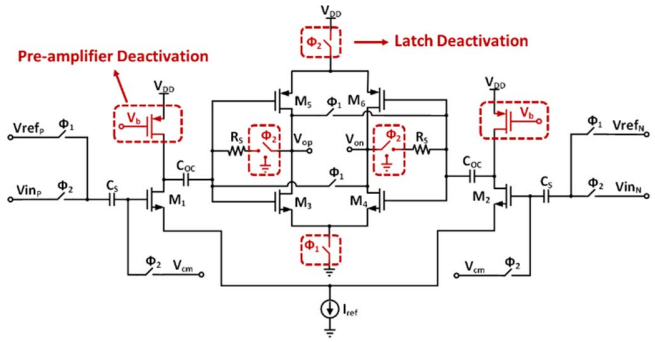

Fig. 3. Modified comparator circuit

In both cases, the comparator delay consists of the delay from both the preamplifier and the latch. Latch delay can be written as shown in [17]:

$$t_{Latch} = \frac{C_L}{g_{m,eff}} \ln\left(\frac{\Delta Vout}{\Delta Vin}\right) \quad (1)$$

Where $g_{m,eff}$, ΔV_{out}, C_L, and ΔV_{in} are defined as back-to-back effective transconductance, output differential voltage, load capacitor and differential input voltage, respectively. The differential preamplifier gain and output voltage can be calculated as follows:

$$A_{Pre} = \frac{g_m \cdot R_D}{1+\frac{j\omega}{\omega_0}} \quad (2)$$

$$\Delta V_{o,Pre} = 2\, R_D\, \omega_0 \left(\frac{I_{D,1}}{V_{OD,1}} + \frac{I_{D,2}}{V_{OD,2}}\right) e^{-\omega_0 t_{Pre}} \quad (3)$$

Where R_D is the differential pair output resistor, ω_0 is the 3dB-bandwidth of the preamplifier, $I_{D,i}$ and $V_{OD,i}$ are the i-th transistor biasing current and overdrive voltage. Based on (3) and (1), the total propagation delay for the two-stage comparator is found as:

$$t_p = t_{Latch} + t_{Pre} \quad (4)$$

$$t_p = \frac{C_L}{g_{m,eff}} \ln\left(\frac{\Delta Vout}{\Delta Vo,diff}\right) + \ln\left(\frac{2\, R_D\, \omega_0}{\Delta Vo,diff} \times \frac{V_{OD,1}\, I_{D,2} + V_{OD,2}\, I_{D,1}}{V_{OD,2}\, V_{OD,1}}\right)^{\frac{1}{\omega_0}} \quad (5)$$

From (5), it is evident that the propagation delay of the comparator is in inverse relationship to the input common mode voltage. The common mode voltage is kept constant in the reset phase through the ϕ_2 switch.

IV. SIMULATION RESULTS

Both comparators are designed using the TSMC 65nm technology and are compared at 300 µV input voltage with respect to the reference voltage, in order to further be used in high speed 12-bit ADCs. The clock signal used for sampling ϕ_1 is set to be 1 GHz, with the reset signal ϕ_2 being of 180° phase difference from the sampling clock. Measuring the comparator delay as the time from when the sampling cycle begins till the regeneration starts to take effect, the delay has found to be 76 ps in the original circuit and 169 ps after modification. But the power has been significantly reduced to 220 µW after modifications. Fig. 4 shows the input and the resulted output waveforms after performing overdrive recovery test at 300 µV input difference. The difference is reduced to find the minimum input difference at which the comparator still works and where the delay is maximum. The comparator can operate properly till a resolution of 327 nV while dissipating only 276 µW and having a worst delay of 272 ps.

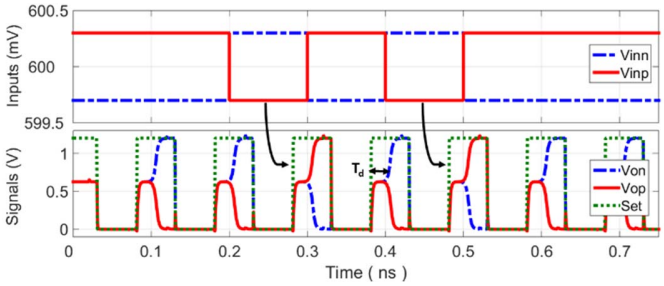

Fig. 4. Comparator overdrive recovery test (V_{in} = 300 µV and frequency = 1 GHz)

Due to the presence of parasitic capacitances and the capacitances used for offset cancellation, voltage variations and clock feedthrough effects are coupled to the input nodes, resulting in what is called kickback noise voltage. Prior stages connected to the comparator's inputs are adversely impacted and the system's efficiency can be degraded considerably by this kickback noise. Using the setup shown in Fig. 5 [18], the kickback noise voltage due to the switching activity is reduced in the modified circuit from 11.32 mV and 7.77 mV to 5.52 mV and 2.5 mV for the input levels higher and lower than reference, respectively. Kickback noise voltage simulation results are presented in Fig. 6.

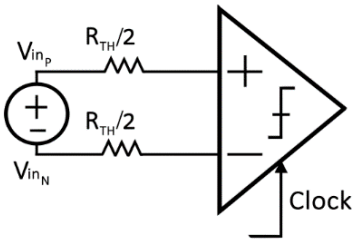

Fig. 5. Kickback noise measurement setup

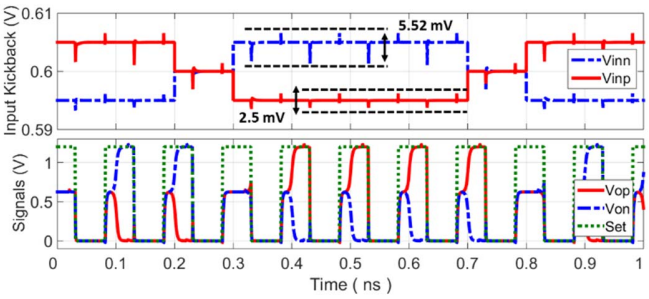

Fig. 6. Kickback noise voltage simulation

The delay of the proposed comparator is simulated and measured versus the differential input voltage. As mentioned before, the comparator delay highly depends on the input voltage difference from the reference voltage and the common mode voltage. The comparator delay is measured by increasing the input voltage and shown in Fig. 7. The higher input voltage results in the lower output delay and vice versa.

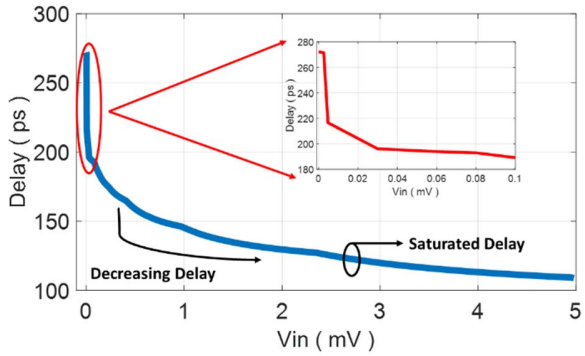

Fig. 7. Comparator delay versus input difference

The proposed comparator offset performance is proved by running the Monte Carlo simulation with 400 iterations. Monte Carlo shows the input referred offset voltage of σ_{OS} = 4.29 mV. Simulated Monte Carlo histogram is shown in Fig. 8.

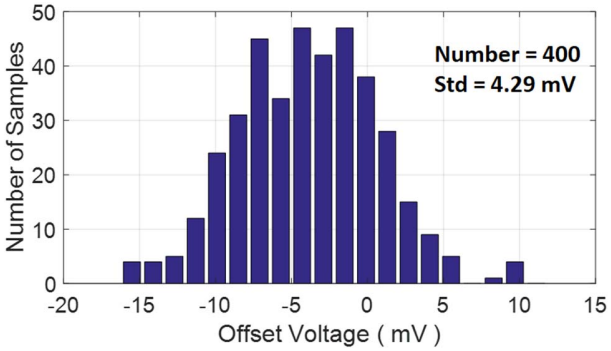

Fig. 8. Monte Carlo simulation

A comparison is made between the original circuit, the modified circuit and a state of the art work in Table I. As a figure of merit, the energy efficiency is measured using equation (6):

$$E_{eff} = \frac{\text{Power [Watt]}}{\text{Speed [Hz]}} \quad (6)$$

V. Conclusion

A high speed, high resolution, low power comparator designed using the TSMC 65 nm CMOS technology is presented in this paper. The proposed comparator achieves a resolution of 327 nV and a power consumption of 220 µW at a supply voltage of 1.2 V and a common mode voltage of 0.6 V. Power consumption is considerably reduced by using switches that cut down the power in the reset phase of the comparator's operation. The presented idea operates with 1 GHz sampling frequency and a dual offset cancellation technique to reduce offset voltage and kickback noise voltage to the input, making the proposed comparator an appealing choice for applications that require high-speed and high resolution analog-to-digital converters.

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Table I. Performance summary and comparison to the previous works

Parameter	Original Proposed Comparator [19, 20[	Modified Proposed Comparator	Reza Lotfi's Comparator [17]
Supply Voltage	1.2 V	1.2 V	1.2 V
Common Mode Voltage	0.6 V	0.6 V	0.6 V
Average power	712.3 µW @ 1GHz	220 µW @ 1GHz	329 µW @ 500 MHz
Resolution	47 µV	327 nV	1 mV
Worst Case Delay	127 ps	272 ps	550 ps
Kickback Noise Voltage	11.32 mV	5.52 mV	>43 mV
Delay/log (ΔVin)	25 ps/dec	44 ps/dec	69 ps/dec
Energy Efficiency	0.71 pJ	0.22 pJ	0.66 pJ
Offset	723 µV	4.29 mV	7.8 mV

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