Dynamic Latched Comparator

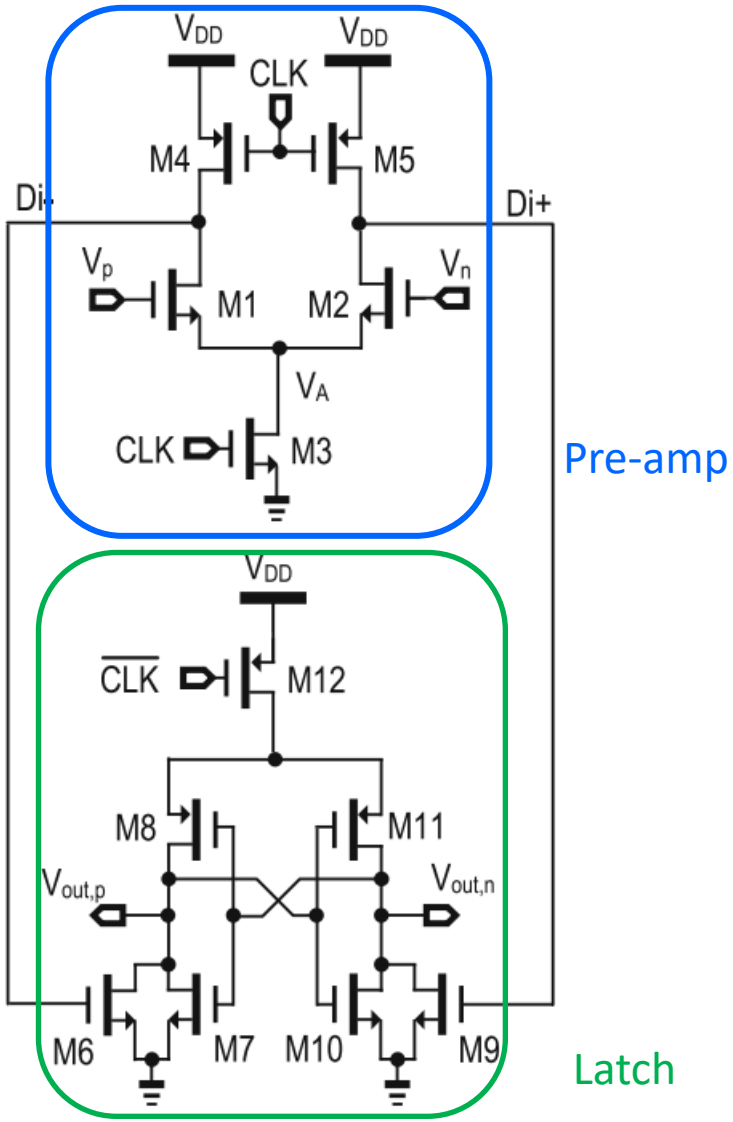


Fig. Conventional Dynamic latched Comparator

A dynamic latched comparator can suffer from three non-idealities:

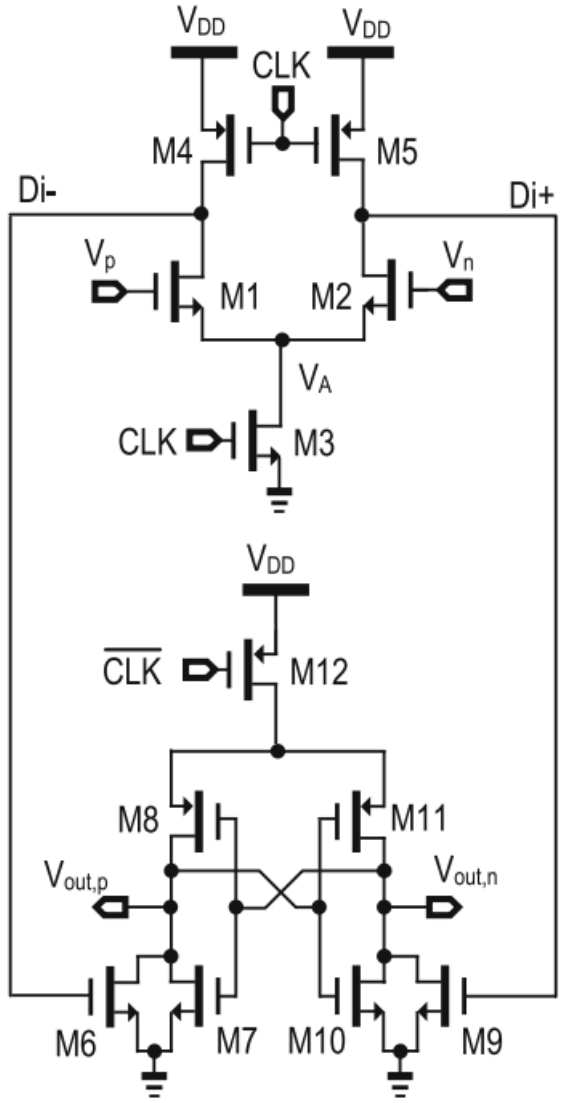
➔ offset voltage (due to mismatches, PVT)

➔ random noise (inherent)

➔ kickback noise (due to channel charge induced effect. It affects conversion speed And ENOB)

Ref: Systematic analysis and cancellation of kickback noise in a dynamic latched comparator(2013). (Ka-Meng Lei , Pui-In Mak , Rui P. Martins)

Generation of Kickback noise:



➔ Assume Vp and Vn connected to Vcm.
➔ When CLK is low (reset) both Di+ and Di- are connected to VDD.
➔ Node V_A is floating.

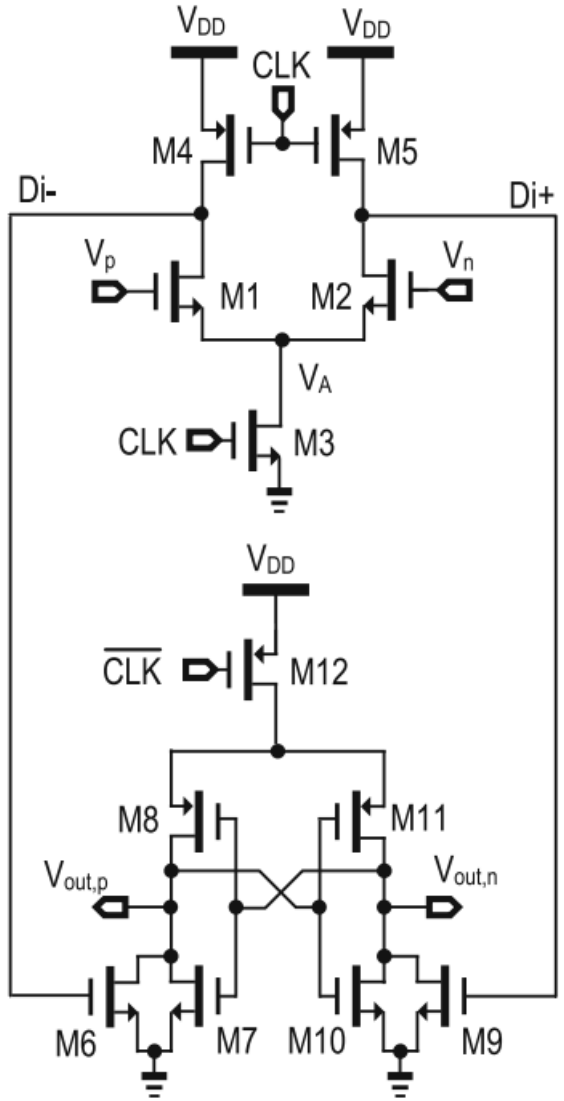
For M1,M2,

$$Q_{G,off} = V_{cm}C_{GB} + V_{GS}C_{GSO} + (V_{cm} - V_{DD})C_{GDO}$$

➔ For the ↑ edge of the clock, $M_{4,5}$ turn off and M_3 turns on.
➔ Node A is grounded first. Driving $M_{1,2}$ to saturation

$$Q_{ch,sat}(t) = -\frac{2}{3}WLC_{OX}(V_{cm} - V_A(t) - V_t)$$

$$Q_{G,sat}(t) = -Q_{ch,sat}(t) + (V_{cm} - V_A(t))C_{GSO} + (V_{cm} - Di_+(t))C_{GDO}$$



➔ When $M_{1,2}$ are turned on nodes Di+ and Di- will be discharged through M1. Rate of discharge depends on inputs and result is generated by positive feedback formed by two cross coupled inverters.
-> As Di+ and Di- are small enough $M_{1,2}$ are driven to triode

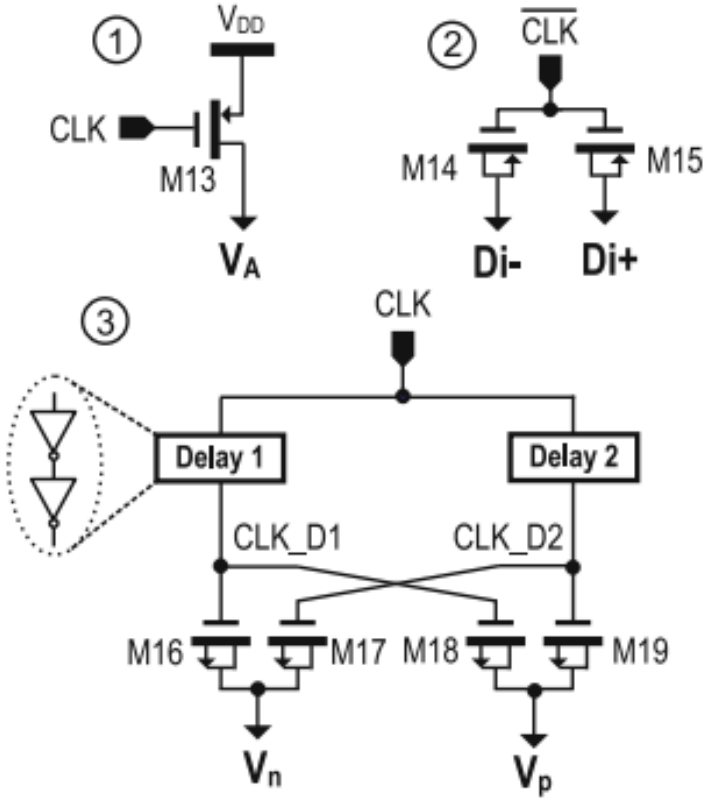
$$Q_{ch,Triode}(t) = -WLC_{OX}(V_{cm} - V_A(t) - V_t)$$

$$Q_{G,triode}(t) = -Q_{ch,triode}(t) + (V_{cm} - V_A(t))C_{GSO} + (V_{cm} - Di_+(t))C_{GDO}$$

*$D_{i+,-}$ and VA vary over time, the voltage variation (even in sub-threshold) will couple back to the gate producing the kickback noise.

Mitigation of kickback noise:

-> Compensate Induced charge with proper charge during appropriate time for different regions of operation.



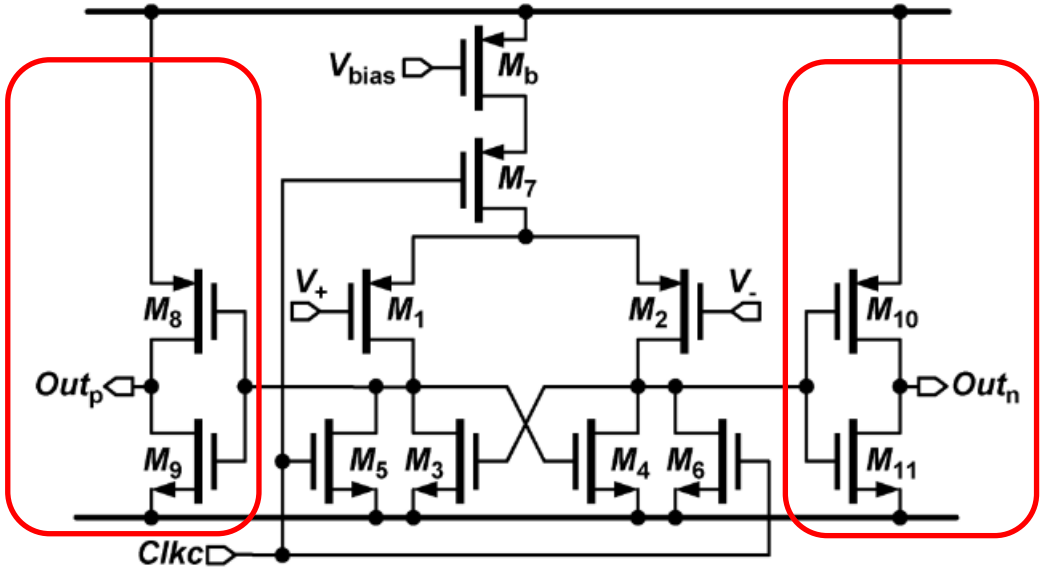
1) Node V_A is pulled to VDD when clock is low (removes uncertainty, increases recovery time of Node A)

2) Two clocked PMOS capacitors (M14 & M15) to absorb charges from M4 and M5 channel during the rising edge of clock. (sizing 0.5 times $M_{4,5}$)

3) M16 and M18 compensate the loss of charge due to switching of the transistors from the off-region to saturation region. M17 and M19 compensate the loss of charge due to the switching of transistors from saturation to triode regions. There are two delay blocks to synchronize the switching times of the different sets of MOS capacitors to accurately neutralize the charges induced.

Comparator Topologies

Topology



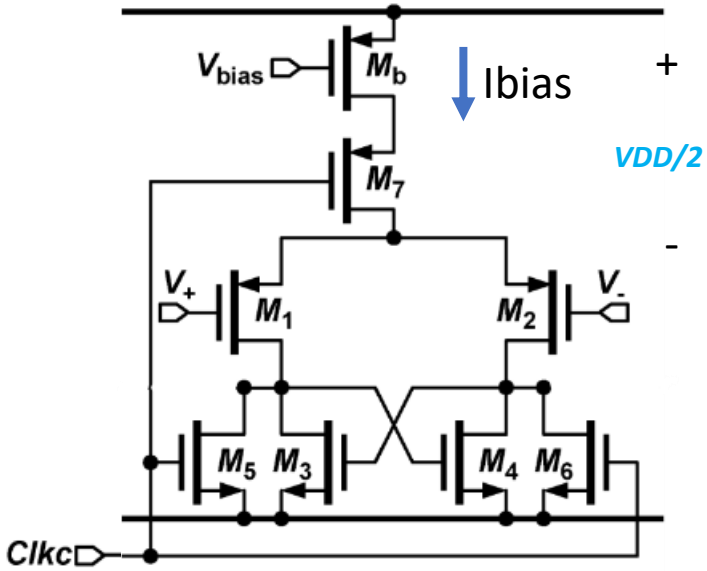
Primarily 2 stages:

1) Preamp and Latch
2) Buffer (inverter Stages)

❖ Buffers are needed to generate full rail- rail digital signals (0,VDD).

Ref: “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” IEEE J. Solid-State Circuits **45** (2010) 731 (DOI: 10.1109/JSSC.2010.2042254)

Design analysis:



Input Range : ± 1mV to 100mV (Vcm =0V)

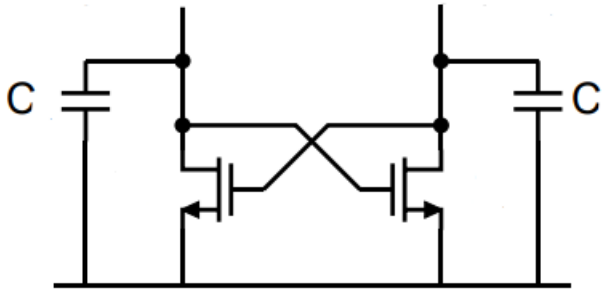
Half of Vmin = ±0.5mV (design for min. (sets Ibias))

o/p nodes swing to VDD/2 or 0 V. (Ideally assuming switch drop 0V)

Main source of amplification is Latch!

$$T=\frac{C}{gm} * \ln\left(\frac{Vo}{Vin}\right)$$

4T to 5T -> settling time



For a 50% compare-reset comparator @ 10MHz, Lets assume time for the node to reach its steady state value by 10% of Clock period.

(i.e) T = 0.1 * 100n/5 =2nsec

Now, C/gm = 2n/ln(VDD/[2*Vin])

Latch sees the amplified Signal from preamp!

➔ Assumption $A_{V,pre}$=4.

➔ $V_{in,latch}$ = 4*1m =4 mV

VDD =1	VDD=0.8	VDD=0.6
C/gm =4.14E-10	C/gm =4.343E-10	C/gm =4.63E-10

gm is dependent on Capacitance load to maintain same Settling Time! C↑ gm↑ Ibias↑

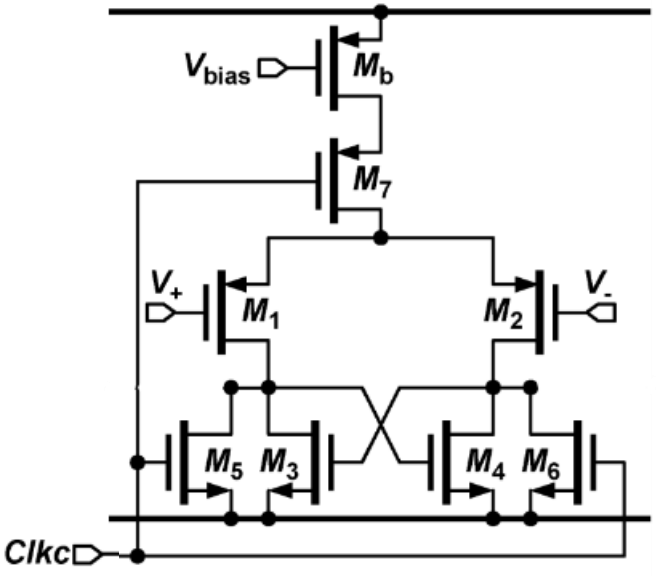
C=1fF, VDD=1V	**C=1fF, VDD=0.8V**	**C=1fF, VDD=0.6V**
gm =2.42uS	gm=2.302uS	gm=2.16uS

Now to calculate the current needed to properly set the amplification, We assume that one of the transistor Of latch enters (weak inversion or sub-threshold) and the complete bias current is steered into it once regeneration is complete.

	I_bias (VDD=1V) gm/I_bias =10	I_bias (VDD=0.8V) gm/I_bias =20	I_bias (VDD=0.6V) gm/I_bias =20
C=1f	0.240u	0.115u	0.108u
C=10f	2.4u	1.15u	1.08u
C=100f	24u	11.5u	10.8u

* For VDD=0.8,0.6 the mosfets are in subthreshold region (since Threshold Voltage near 400mV for 65nm Technology)

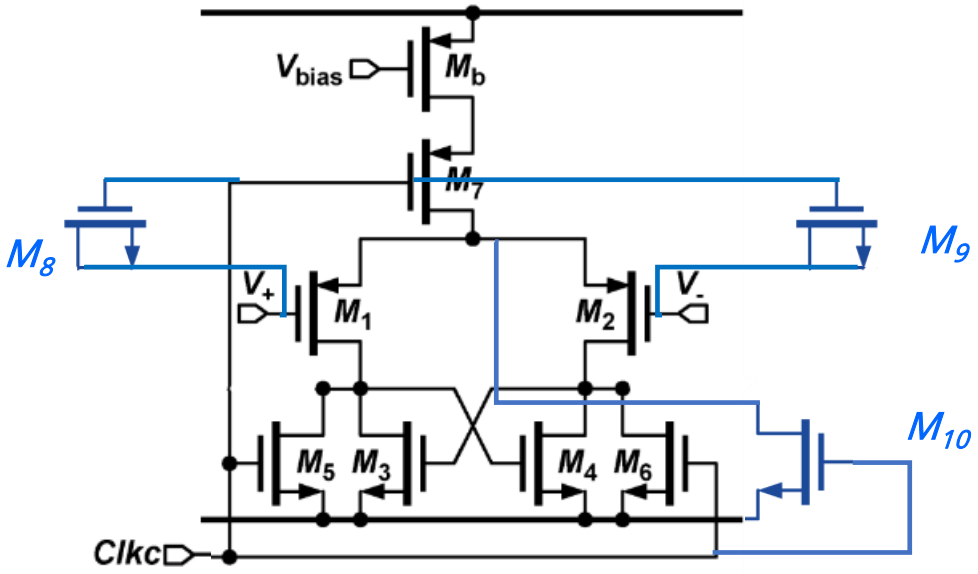
Design For case of Cload=1fF, fcomp=10MHZ, VDD=0.8V



Standard feature Size = 200n/60n

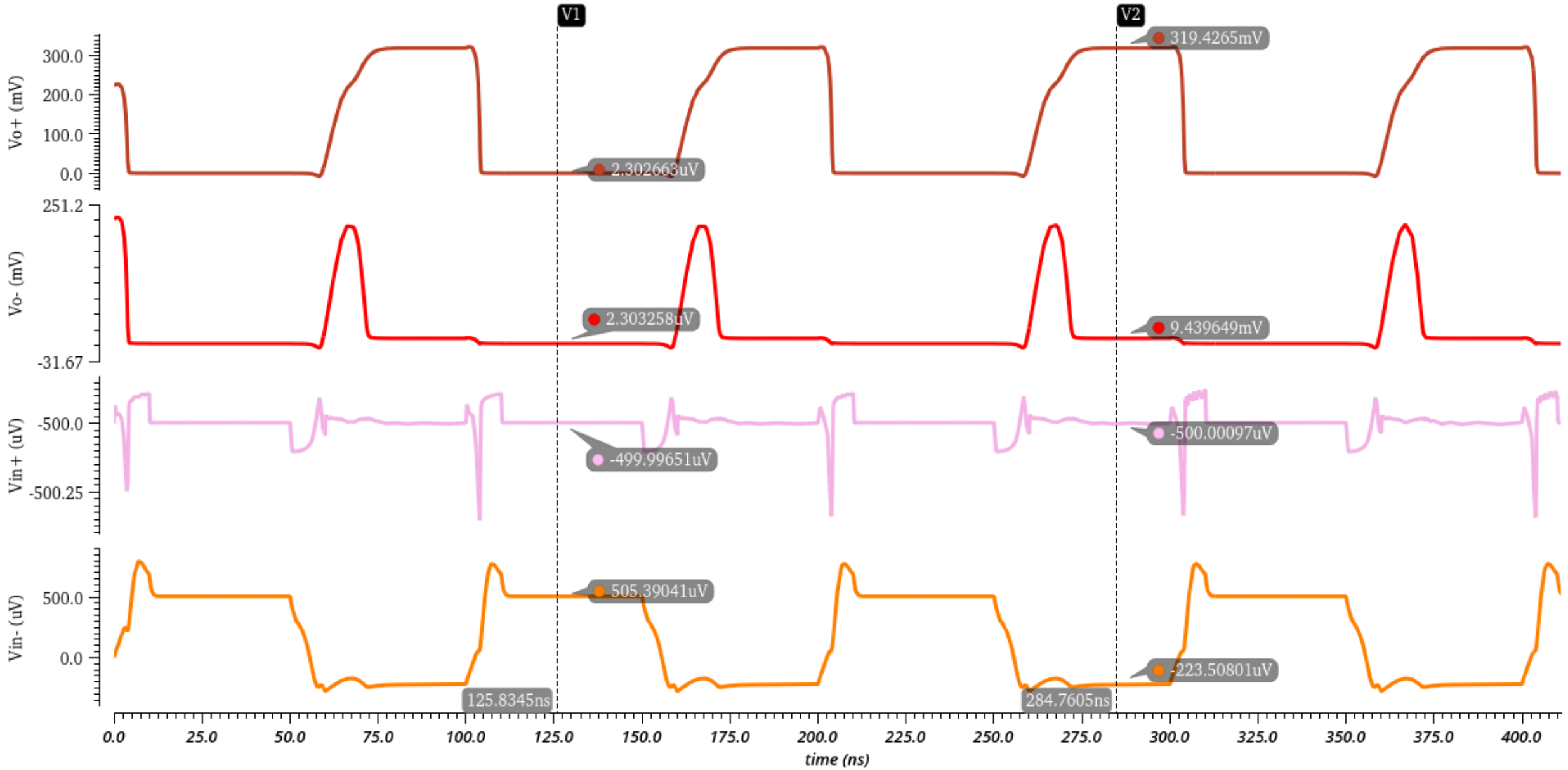
	A.R.	gm (simulated for Vin = ± 0.5m)	Ro (simulated for Vin = ± 0.5m)
Mb	200n/180n	2.94uS	
M7,5,6	400n/180n (2F)	2.5uS (On Mx)	
M1,2	200n/180n	2.92uS (On Mx)	9.3M Ohm (On Mx)
M3,4	200n/180n	2.21uS (On Mx)	0.79M Ohm (On Mx)
Vbias	530m		

Modifications to minimize Kickback noise:-



M8,M9	120n/60n
M10	200n/60n

i/p: ±0.5mV DC (-ve side sampled cap array 100fF), fcomp=10MHz, VDD=0.8V, Cload= 1fF (Vcm=0)



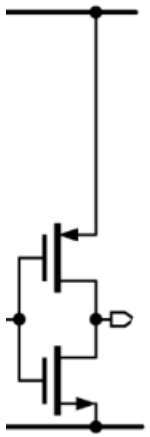
Observations:

-> There is a shift in Vo from analysis values. Reason being gm’s are not equally matched (need irregular A.R’s) .

-> Kickback noise variation (Vin negative side = 725uV. For a 100fF capacitor array).

-> Ibias= 132nA, Energy per conversion = 5.3fJ

Buffer design:



Power calculations

Switching power: $0.5*CV^2f$ (for alpha =0.5)

CLoad	VDD=1	VDD=0.8V	VDD=0.6V
1f	5nW	3.2nW	1.8nW
10f	50nW	32nW	18nW
100f	500nW	320nW	180nW

f= 10MHz

This is ideal power consumed by single buffer.

Calculating the current to be delivered during transition at o/p (0->1)

$$I = C\frac{dv}{dt}$$

(Spike in transient) Transition time = 10% of clock period

Cload	I(VDD=1)	Ron(1V)	I(VDD=0.8)	Ron(0.8)	I(VDD=0.6)	Ron(0.6)
1f	100nA	10MΩ	80nA	10MΩ	60nA	10MΩ
10f	1uA	1MΩ	800nA	1MΩ	600nA	1MΩ
100f	10uA	100KΩ	8uA	100KΩ	6uA	100KΩ

Choosing A.R. for Buffer Transistors:-

For a 10fF load, with 10nsec transition time

$$5*R*C = 10^{-8}$$

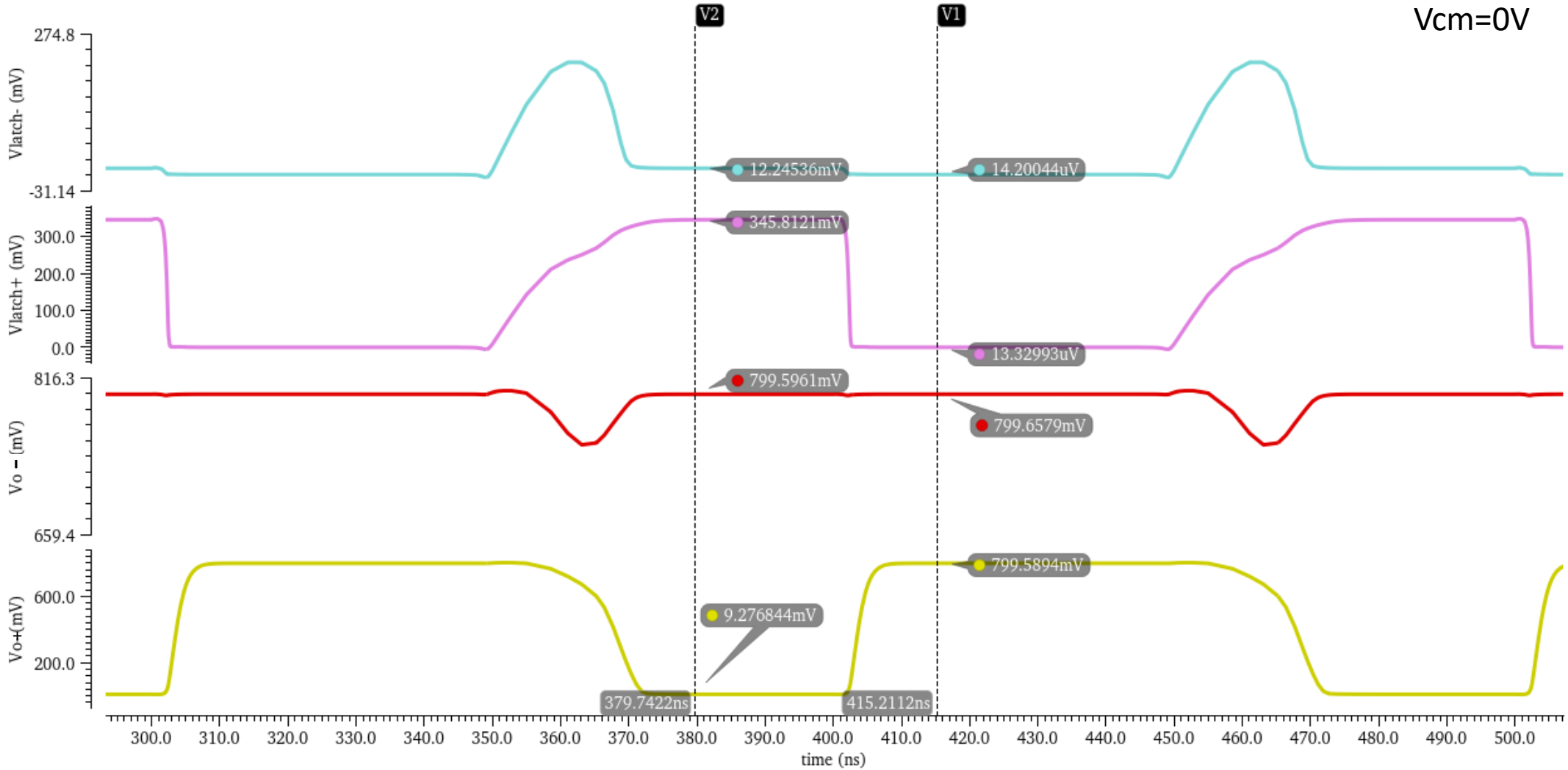
R= 200k ohms

By increasing resistance of MOS, we are inherently increasing C_{par} which increases settling time.
(requires careful sizing to meet constraints)

Leakage!

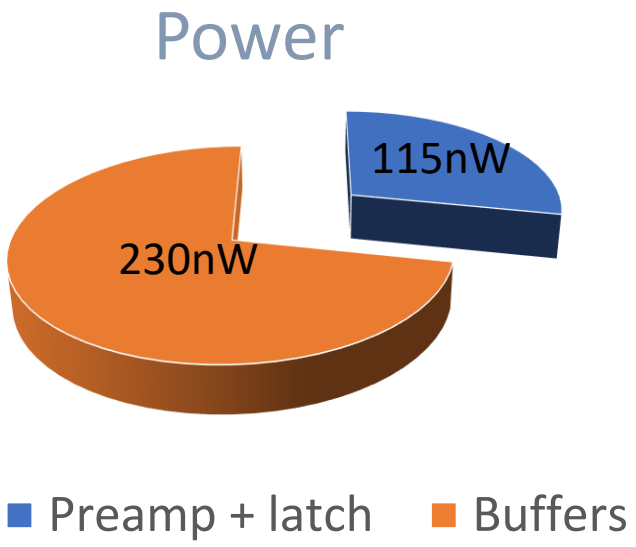
@Vcm=0V	A.R.	0->1 State (o/p)	1->0 State (o/p)
PMOS	200n/300n (stack of 4)	80K ohms (combined)	2M ohms (Combined)
NMOS	200n/60n	473M ohms	59.2K ohms

Transient response : i/p : ±0.5mV , VDD = 0.8, freq =10MHz, Duty cycle = 60%, Cload=10fF (power achieved = 345nW)



Observations:

➔ The initial design for pre-amp latch was found to be slower (reason: node cap > 1fF, so increased Ibias to 230nA)
➔ The Buffers ideally should consume 76.8nW. But due to leakage in PMOS and additional parasitic capacitances, Power Consumption is roughly 230nW for 60% D.C (5% rise and fall times).



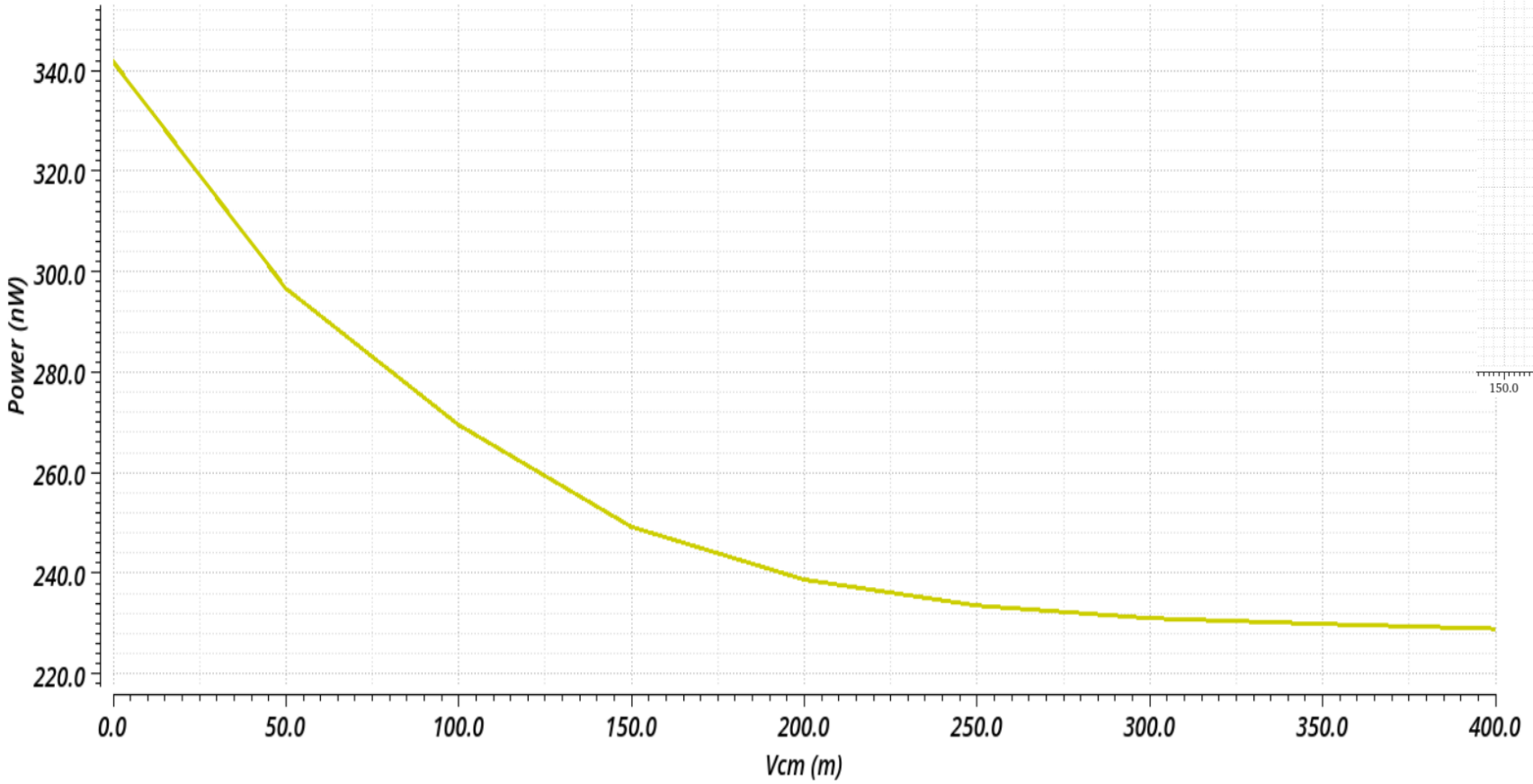
Solutions:

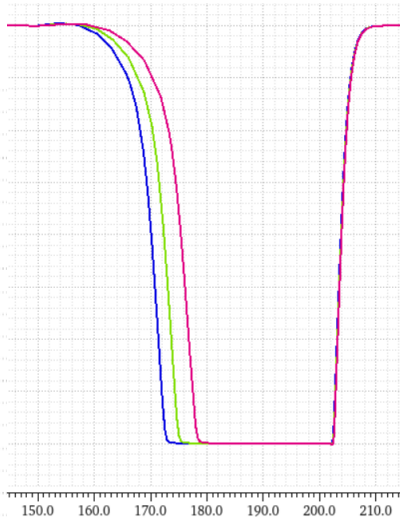
-> Stacking of more PMOS (more Area, more parasitics, Increase in power consumption of Preamp latch stage!).

-> Increase in input common mode voltage from 0V (Increases Preamp High logic Voltage level, reduces leakage in PMOS and NMOS).

-> Move to lower voltage supply. (Decreasing VDD reduces leakage since it increases resistance, Without affecting parasitics and reduces Switching power)

@Vin=±0.5mV,fcomp=10MHz, 60% D.C. Same (W/L)'s for devices





Vcm=200mV
Vcm=300mV
Vcm=400mV

@Vcm=200mV	0->1 State (o/p)	1->0 State (o/p)
PMOS	80K ohms (combined)	28M ohms (Combined)
NMOS	600M ohms	59.2K ohms

Effects of Vcm:

➔ Reduction of leakage power by 100nW for Vcm =200mV (Power consumption = 240nW)

➔ Settling time slightly increases with Vcm