Department of Electronic Systems Engineering

PhNEICS Lab
Photonic & Nano-Electronic Integrated Circuits & Systems Laboratory

Modelling of SAR ADC

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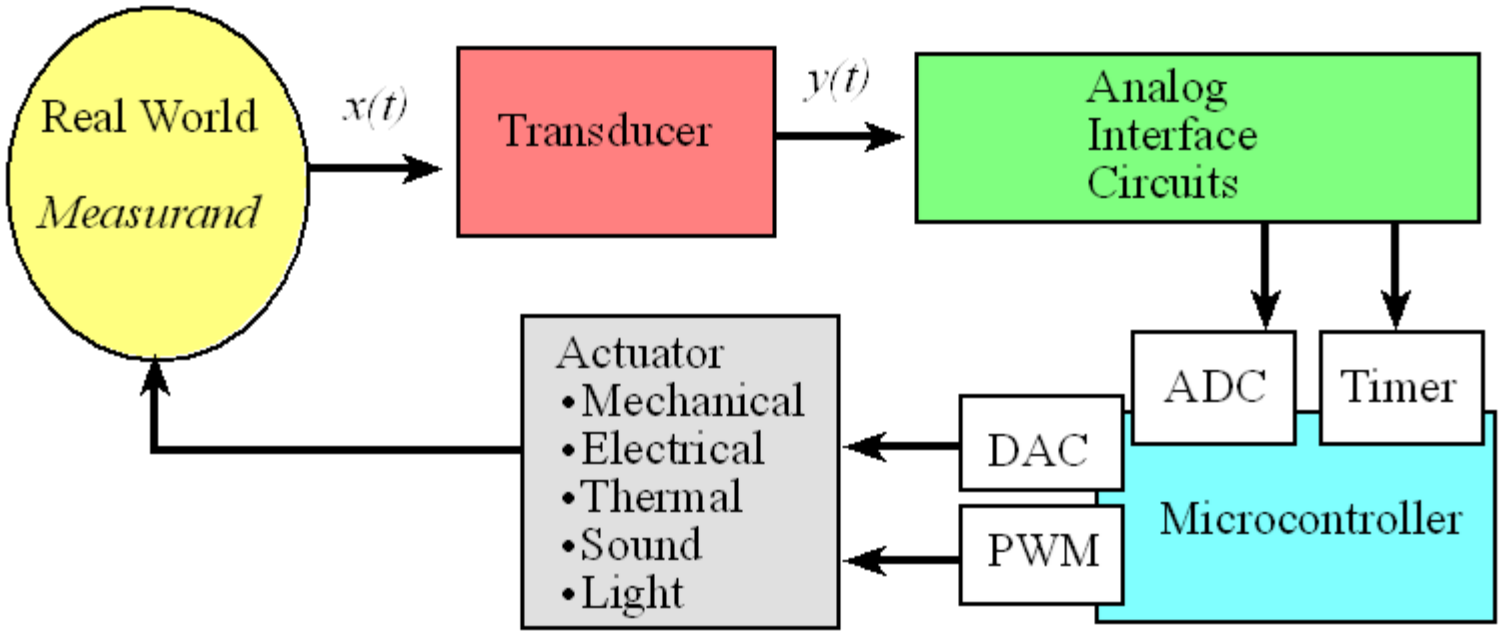


Ref: https://users.ece.utexas.edu/~valvano/Volume1/E-Book/C14_ADCdataAcquisition.htm

Successive Approximation Register ADC

➔ Maps continuous time, continuous-amplitude signals into a discrete representation via sampling and quantization.
➔ Traditionally used in medium to high resolution, and low to medium speed applications.
➔ Invented more than 60 years ago!
➔ It benefits from technology scaling (due to its mostly digital architecture [Energy efficiency!])

$$FoM = \frac{Power}{2 \cdot BW \cdot 2^{ENOB}}$$

*FoM_w = Walden's Figure of Merit

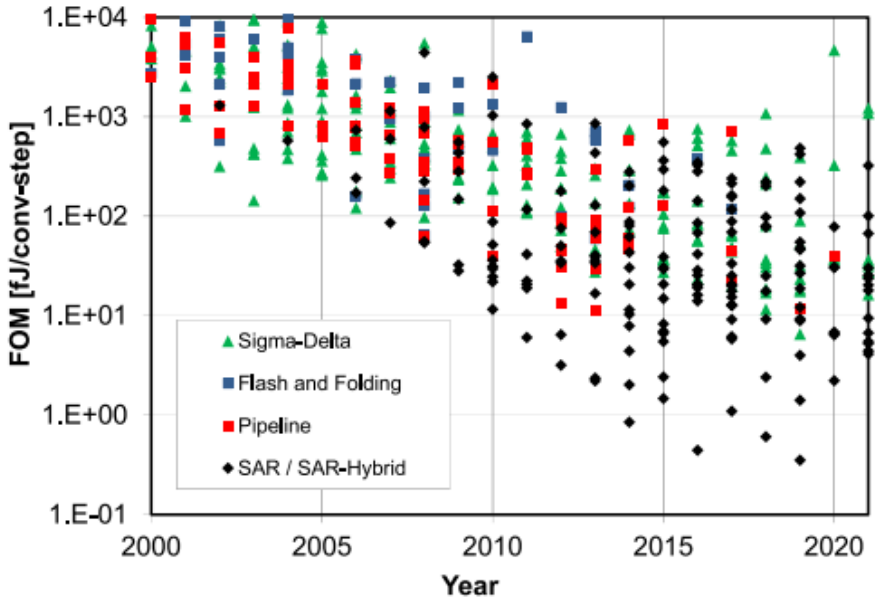


Fig. 1. ADC energy efficiency (FoM) over the years

Ref: Low-Power SAR ADC Design: Overview and Survey of State-of-the-Art Techniques (Nan Sun et al, June 2022)

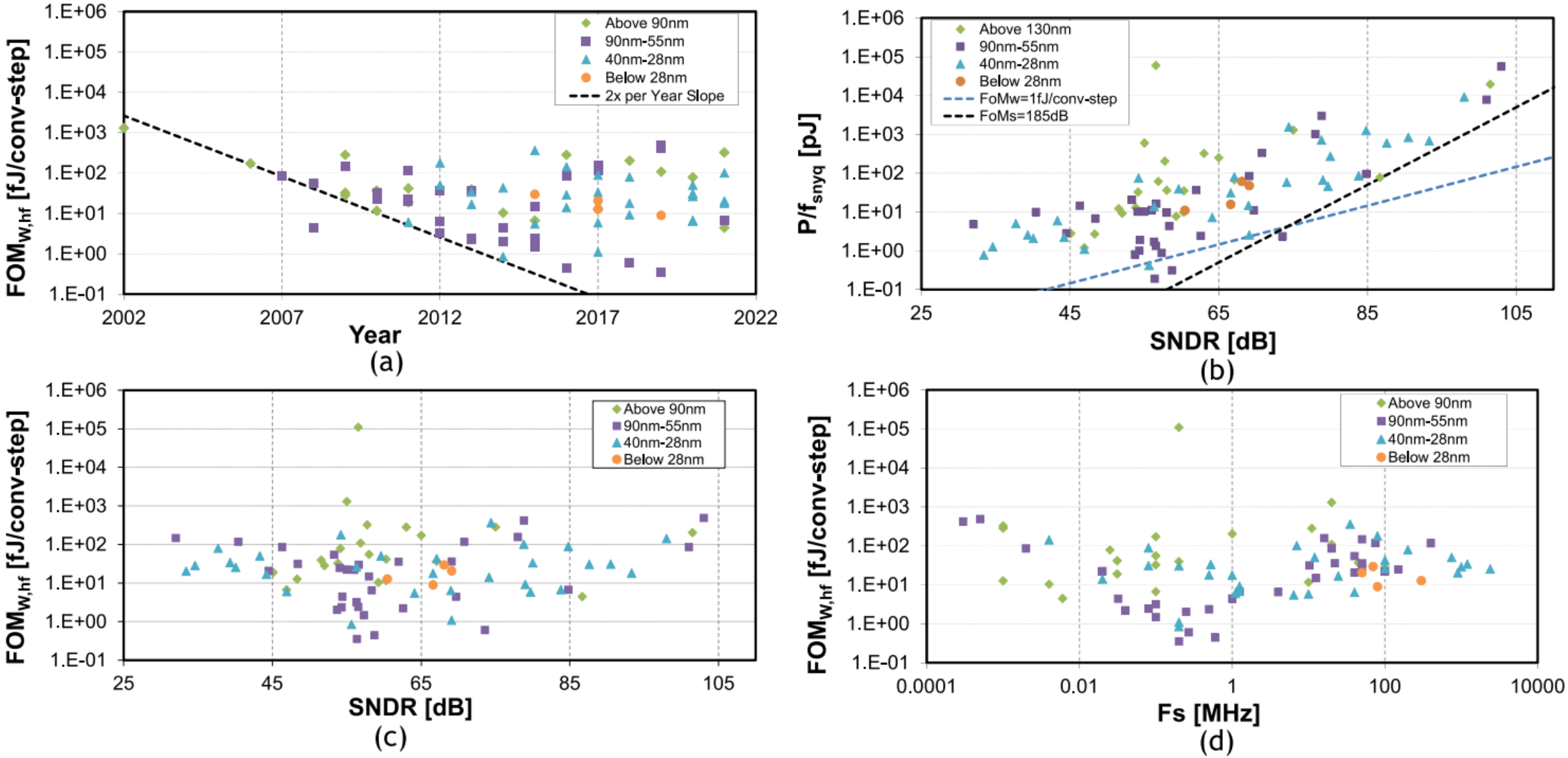
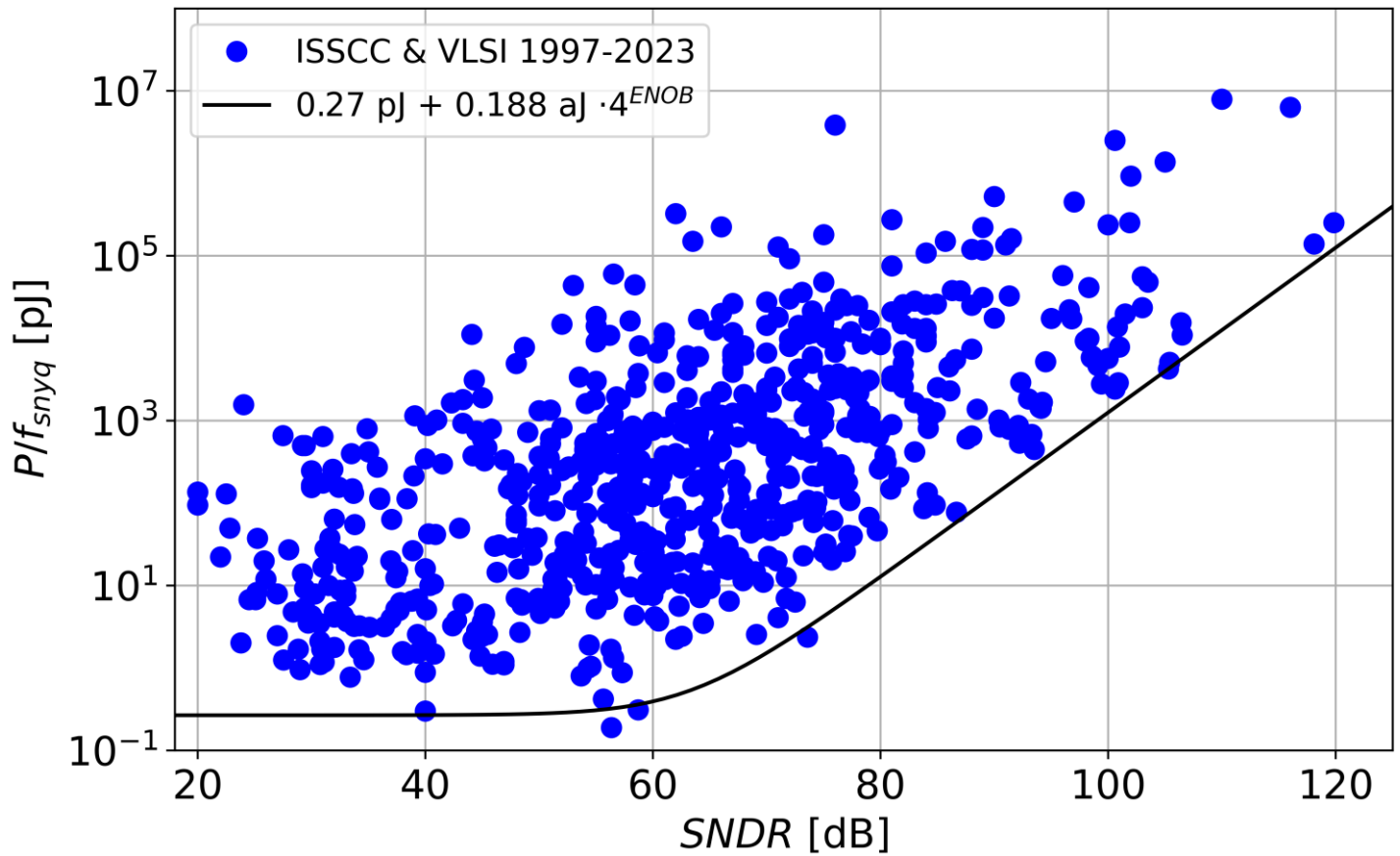


Fig. 2. a) FoM$_W$'s over years b) Conversion Energy c) FoM$_W$'s over SNDR d) FoM$_W$'s VS Conversion Frequency

Ref: B. Murmann, "ADC Performance Survey 1997-2023," [Online]. Available: https://github.com/bmurmann/ADC-survey



Ref: B. Murmann, "ADC Performance Survey 1997-2023," [Online]. Available: https://github.com/bmurmann/ADC-survey

Trends Summary:

- ➔ For low-to-medium speed SAR converters, the technology sweet spot is presented between 90nm and 55nm, where the digital power has been reduced substantially.
- ➔ Since 2016, the SAR energy efficiency has not improved much. Focus is on High performance-driven designs (High-Precision [≥ 14 bits] and High speed [≥ 200MS/s] converters).
- ➔ Below 28nm, SAR Power is limited by Thermal Noise (Thermal Noise does not scale with Advanced technology!).
- ➔ For SAR Converters below 10 bits, the energy efficiency is limited by digital circuits (2 X per bit trend, FoM_w's).
- ➔ For SAR Converters Over 13 bits, the power consumption is dominated by Analog components such as comparators (4 X per bit trend, FoM's).

Working of SAR ADC

SAR Principle:

➔ For an input with no prior Knowledge, most efficient search algorithm is binary search!

➔ It includes 2 core functions,
1) Search Voltage Generation
2) Comparison

➔ This translates to 3 core functional components,
a) DAC – generates comparison voltage V_{dac}
b) SAR logic – configures DAC
c) Comparator – makes decision

$$N = \log_2 \left(\frac{FS}{LSB}\right)$$

N= minimum no. of weights.
FS= Full Scale i/p.
LSB = Least Significant Bit.

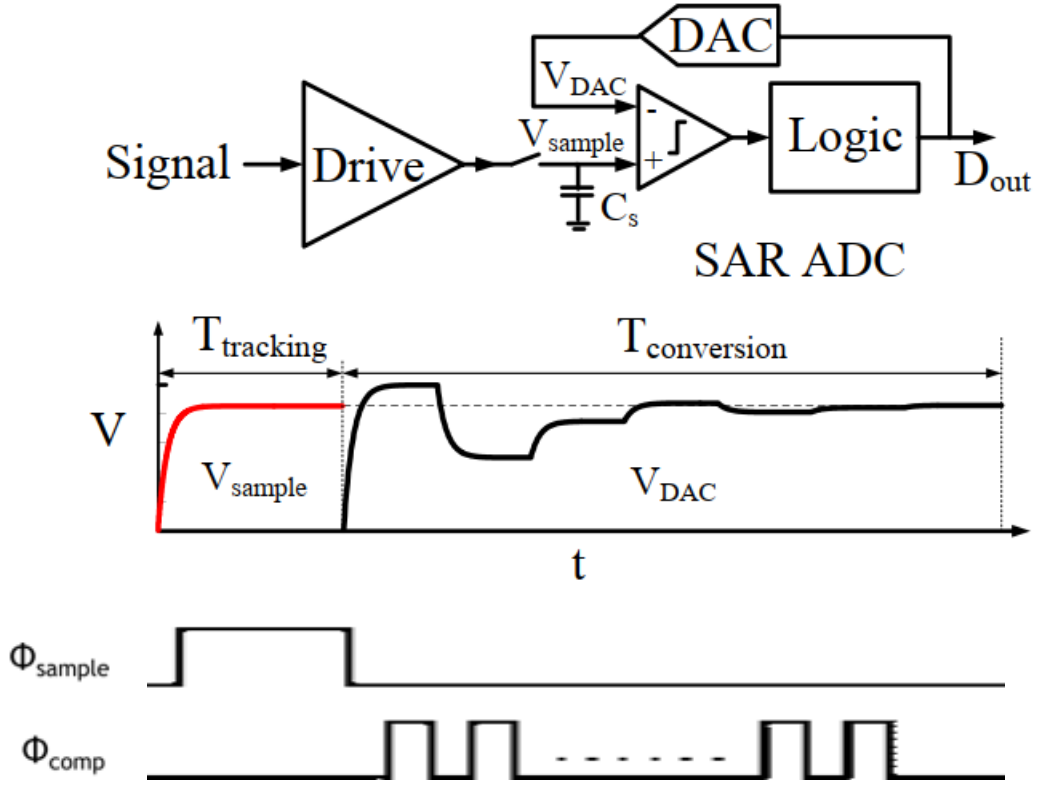
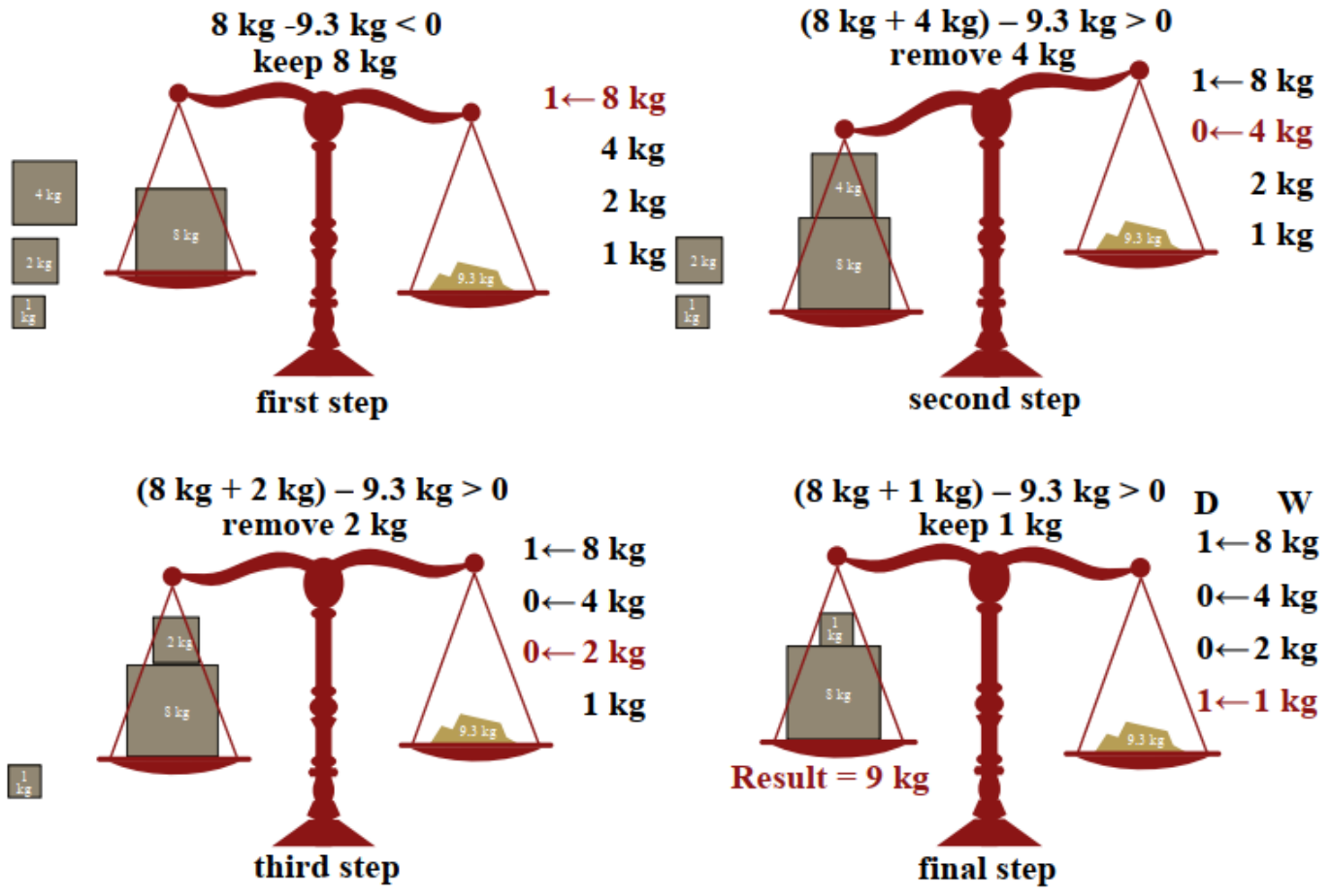


Fig. 3. Single ended SAR Block diagram, Voltage and Timing waveforms (Traditional ADC with differential switching)

ILLUSTRATION (using a scale):



Ref: HIGH-RESOLUTION SAR A/D CONVERTERS WITH LOOP-EMBEDDED INPUT BUFFER [M. Kraemer, Stanford]

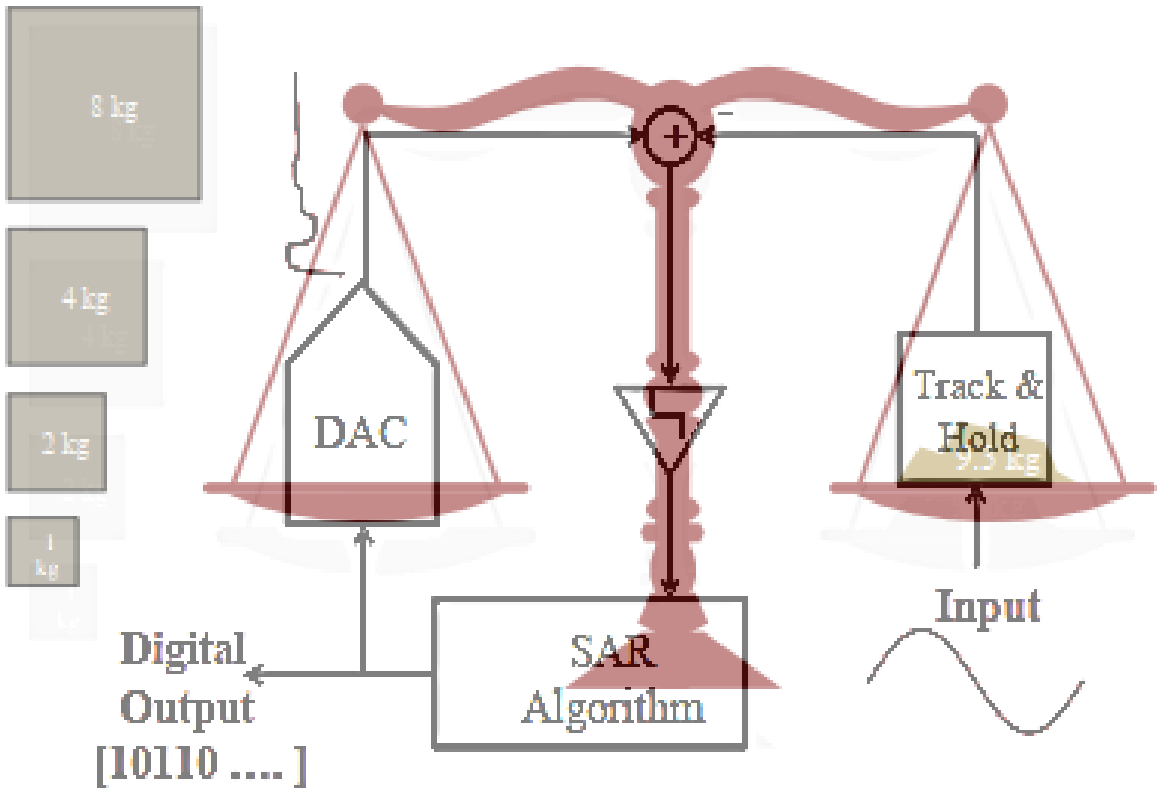
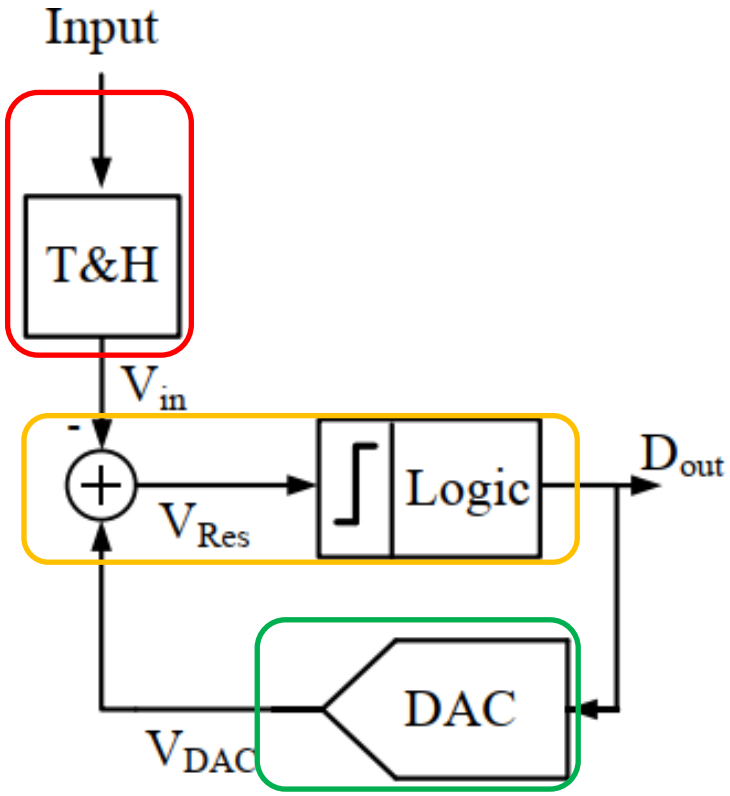


Fig. 4. From the Scale to SAR ADC Block Diagram

➔ Fulcrum acts as summing node and takes decision. (Comparator and SAR Logic)

➔ Left plate acts as a weight generator. (DAC)

➔ Right plate holds the weight to be measured. (Sampled input)



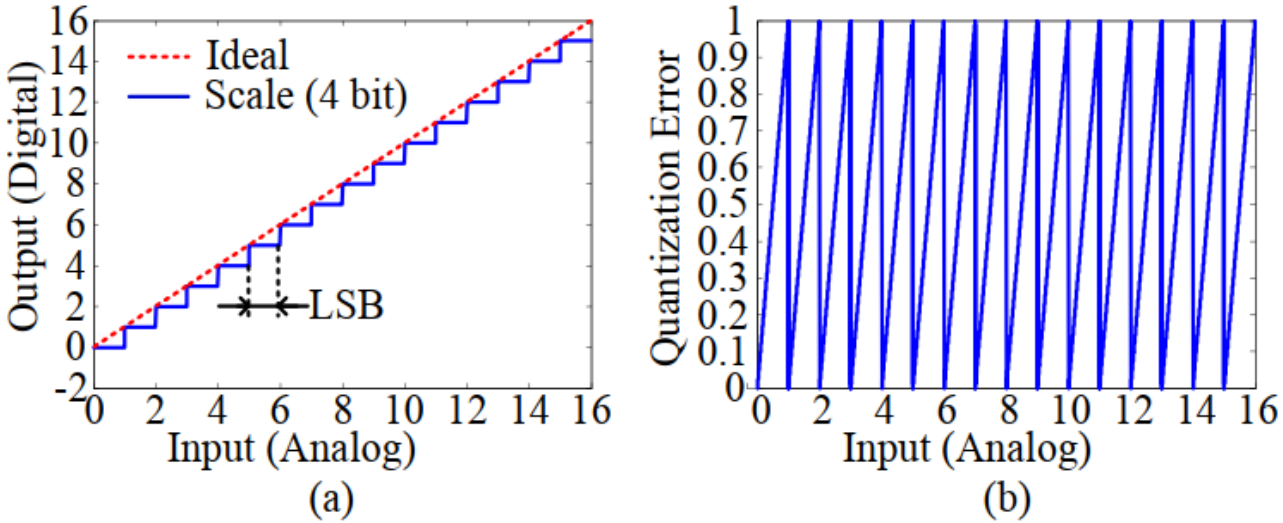
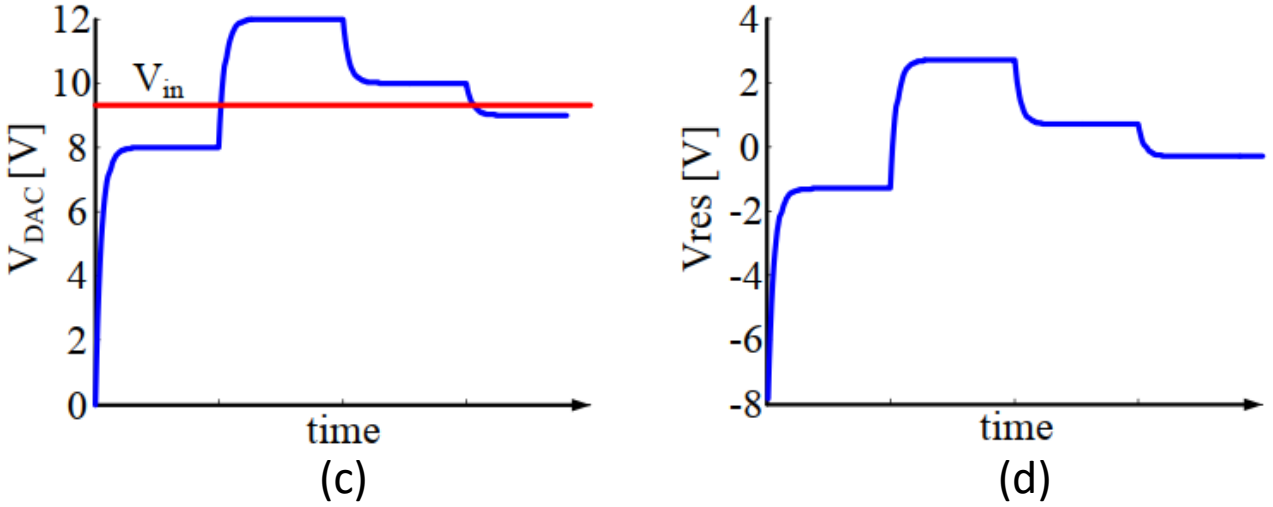


Fig. 5. (a) Scale Transfer Function (b) Q.E. vs Scale input



(c) V_{DAC} vs time

(d) V_{RES} vs time

Notation:

Weights as a vector, W_b = [8 4 2 1] kg.

Results of each scale measurement in vector, D = [1 0 0 1].

(zero for removing the weight and One for keeping the weight)

Our measurement result can be elaborated as,

$$W_b \cdot D^T = (8*1 + 4*0 + 2*0 + 1*1) = 9 \text{ kg}$$

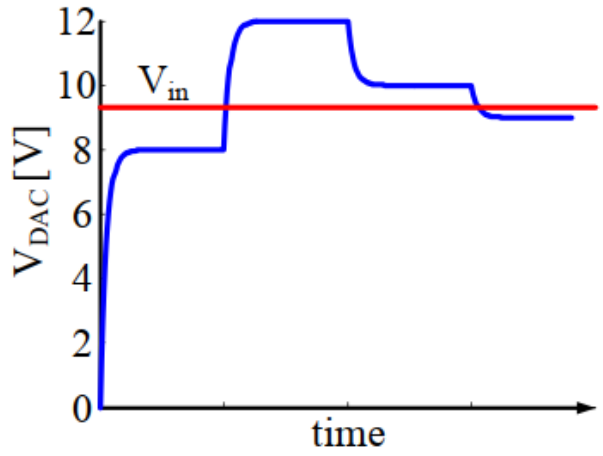


Fig. 5. (c) V_{DAC} vs time

Redundancy in SAR ADC

➔ In a typical hardware implementation, mapping of A/D is impaired by non-idealities of electronic components.
➔ In practice, these nonidealities can be mitigated via a number of design techniques that can be categorized into the following groups:

(1) Precision analog design (By construction. Overhead in terms of area and power dissipation)

(2) Analog or digital calibration techniques (Correction of induced errors by measuring them and adjustment of correction circuit in analog or digital domain)

(3) Redundancy (Errors are tolerated and rejected by conversion algorithm)

Ref: ON THE USE OF REDUNDANCY IN SUCCESSIVE APPROXIMATION A/D CONVERTERS (2013, Boris Murmann)

➔ Redundancy allows us to correct for decisions that happened earlier.

Trade off :- additional measurements (Time and resources) to recover!

➔ SAR algorithm does not have to use a binary weight reference vector W. Use of binary weights only minimizes the number of measurements, but the SAR algorithm can still converge for non-binary weights.

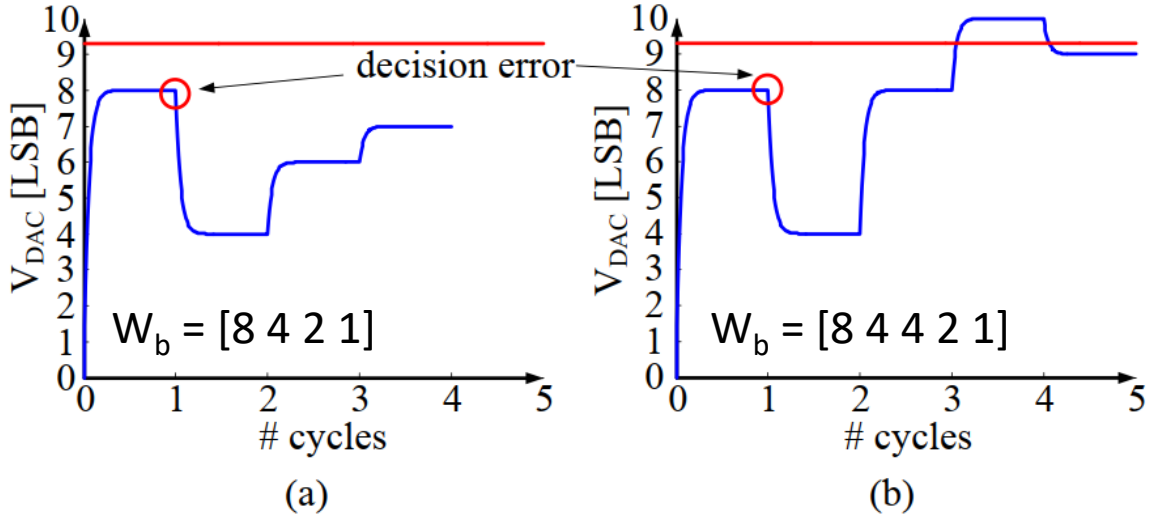


Fig. 6. Decision Error during first cycle
(a) Without Redundancy (b) With Redundancy

➔ Max recoverable error, q(k) of the k^{th} step

$$q(k) = -W(k+1) + LSB + \sum_{n=k+2}^{M} W(n)$$

Where M=vector length of W

➔ The SAR algorithm will not converge within LSB when any one of q(k) is negative.

➔ If q(k) is zero for any k, that means redundancy is already used up and it cannot recover.

➔ The SAR algorithm will not converge with in an LSB for all codes if any one of the q(k) is negative.

Settling Behaviour of the DAC:

➔ Modelling the settling-behaviour of the DAC with a single pole.

➔ Code-dependent output waveform as a function of time can be written as follows,

$$V_{DAC}(t) = \sum_{p=0}^{M-1} W(p+1)D(p+1)\left[1 - e^{\left(-\frac{t-pT_C}{\tau}\right)}\right] s(t - pT_C)$$

W,D are pre-defined Weight and Reference Vectors of DAC with length M.
T_C is allowed time for single cycle.
s(t) is step function.
τ is the time constant related to single pole of DAC.

➔ we can write the time-dependent settling error as:

$$V_{set\ error}(t) = \sum_{p=0}^{M-1} W(p+1)D(p+1)e^{\left(-\frac{t-pT_C}{\tau}\right)} s(t - pT_C)$$

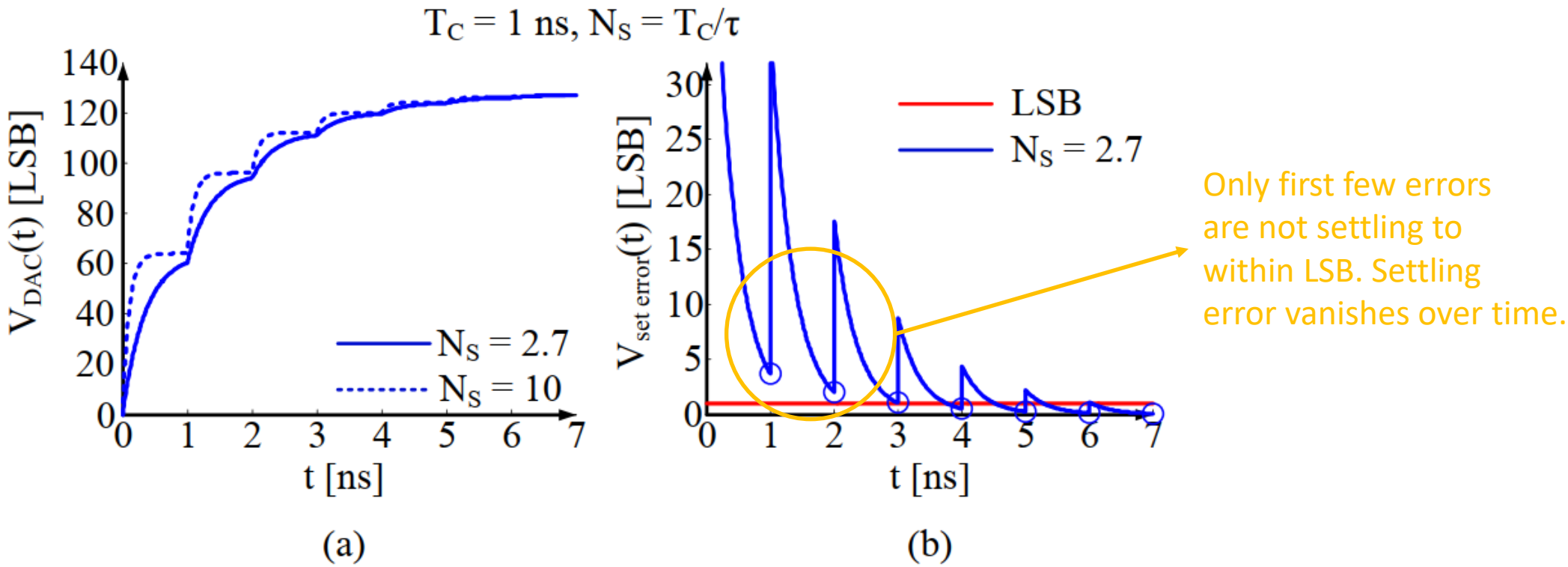


Fig. 7. (a) DAC voltage (normalized to LSB) versus time for two different numbers of settling time constants (b) Settling error (normalized to LSB) versus time

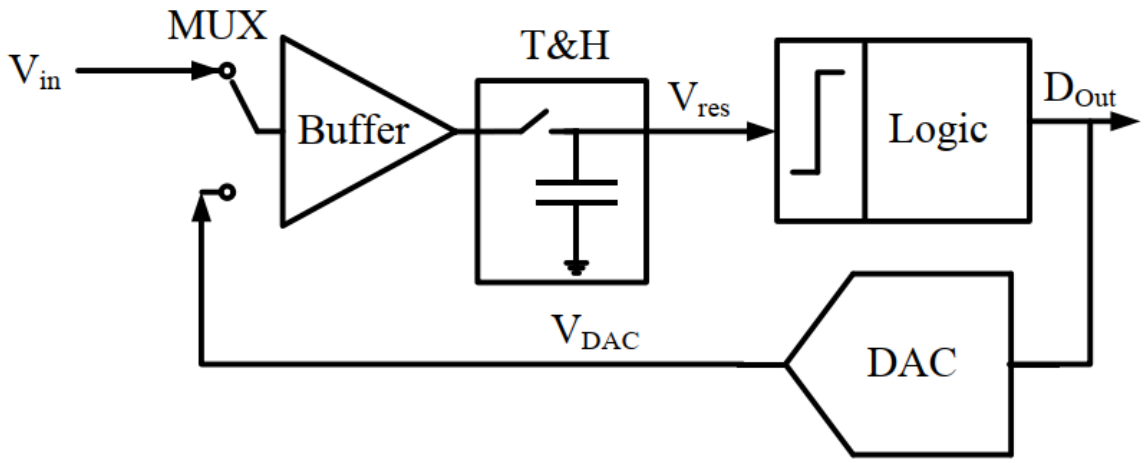
DAC Switching Techniques:

➔ DAC capacitor size is limited by Sampling noise requirement.

➔ But Higher DAC Capacitor load puts significant pressure on ADC drive circuit.

➔ Many Commercial Stand-alone SAR ADC's use buffer in between sampler and DAC. But buffers like source followers are poor in linearity in modern processes.

➔ Doris et al. showed that it is possible to linearize a buffer by placing buffer inside a feedback loop.



Ref: A 480mW 2.6GS/s 10b 65nm CMOS time-interleaved ADC with 48.5dB SNDR up to Nyquist (JSSC'11, K.Doris et al)

ADC First order Model

ADC Model Analysis

y_1 and y_2 are the distorted input and DAC voltages.

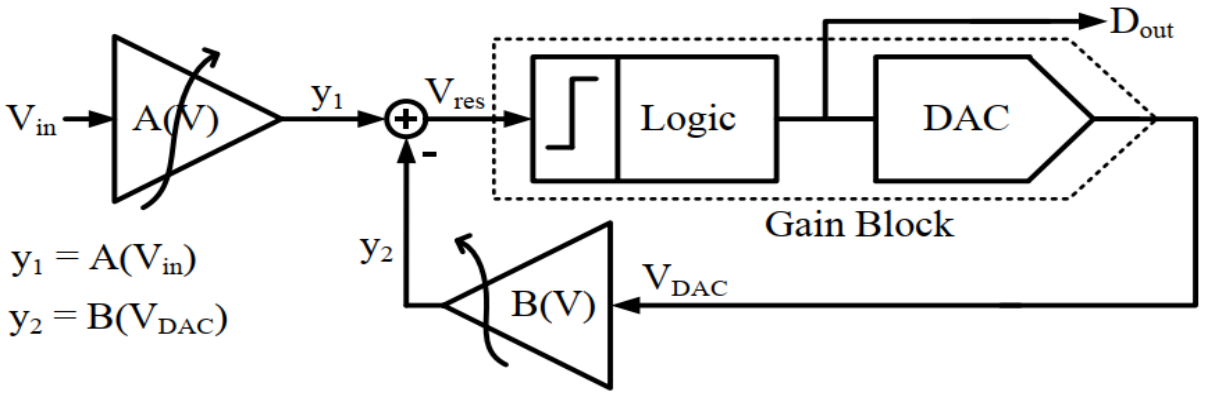


Fig. 8. Basic ADC Model

$$y_1 - y_2 = V_{res} \approx LSB \approx 0 \qquad (1)$$

$$y_1 = A(V_{in}) = a_1 V_{in} + a_3 V_{in}^3 \qquad (2)$$

$$y_2 = B(V_{DAC}) = b_1 V_{DAC} + b_3 V_{DAC}^3 \qquad (3)$$

$$V_{DAC} = \sum_{n=1}^{\infty} B_n y_2^n = \sum_{n=1}^{\infty} B_n y_1^n = \sum_{n=1}^{\infty} B_n [a_1 V_{in} + a_3 V_{in}^3]^n \qquad (4)$$

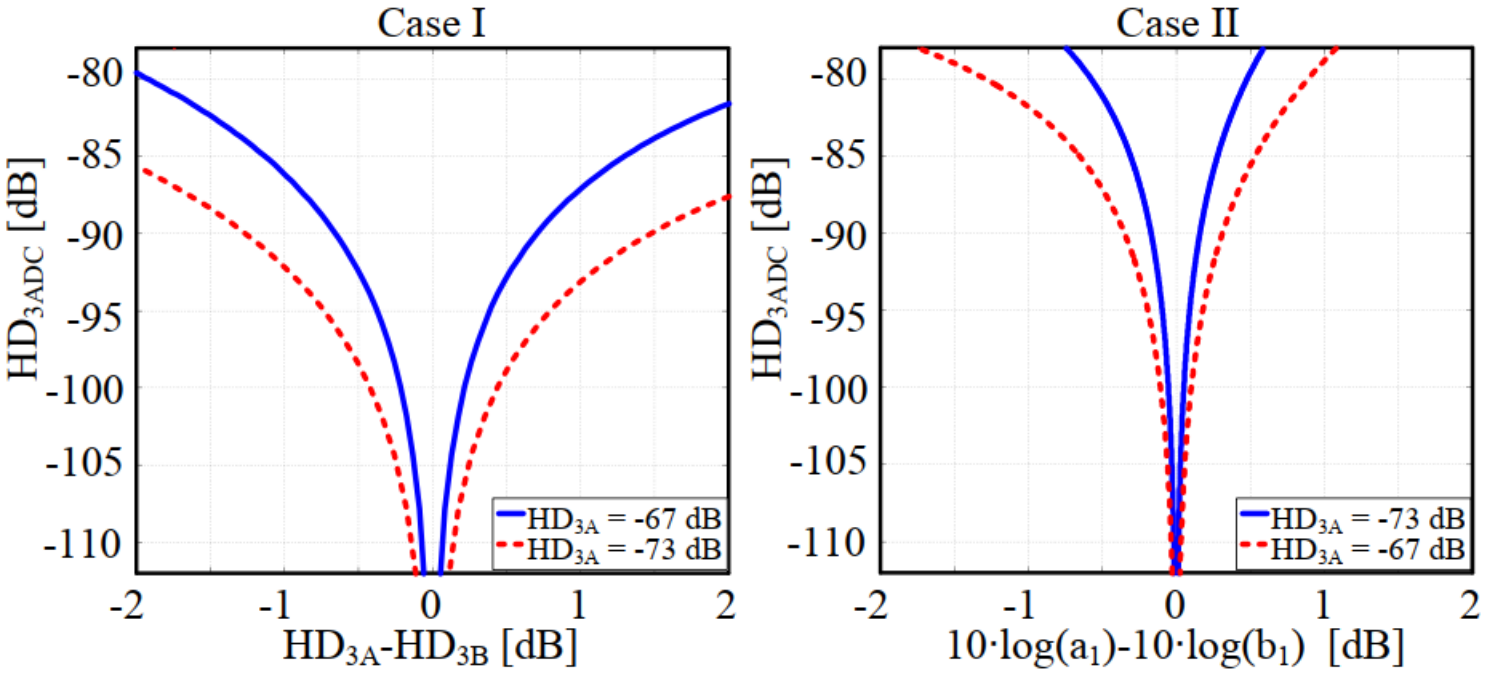
(Series reversion)

$$B_1 = \frac{1}{b_1}, B_2 = 0, B_3 = \frac{-b_3}{b_1^4}, B_4 = 0$$

$$V_{DAC} \approx \frac{a_1}{b_1} V_{in} + \left[\frac{a_3}{b_1} - \frac{a_1^3 b_3}{b_1^4}\right] V_{in}^3 \qquad (5)$$

$$HD_3 = 0.25 \text{ x } \left[\frac{a_3}{a_1} - \frac{a_1^2 b_3}{b_1^3}\right] V_{in}^2$$

Ref: HIGH-RESOLUTION SAR A/D CONVERTERS WITH LOOP-EMBEDDED INPUT BUFFER [M. Kraemer, Stanford]



Case 1: $b_1 = a_1$ and $b_3 = a_3 + \Delta$

Case 2: $b_1 = a_1 + \Delta$ and $b_3 = a_3$

$$HD_{3A} = \frac{1}{4}\frac{a_3}{a_1}V_{in}^2$$

$$HD_{3B} = \frac{1}{4}\frac{a_3 + \Delta}{a_1}V_{in}^2$$

Effect of Comparator offset

(Present only during Conversion)

$$Take,\ \ y_2 = y_1 + V_{off}$$

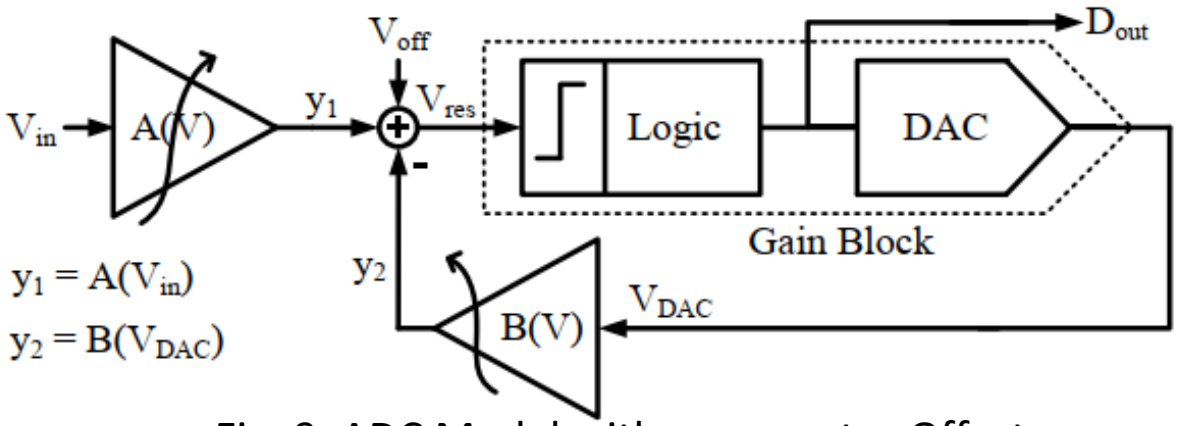


Fig. 9. ADC Model with comparator Offset

$$\sum_{n=1}^{\infty} B_n y_2^n = \sum_{n=1}^{\infty} B_n (y_1 + V_{off})^n = \sum_{n=1}^{\infty} B_n [a_1 V_{in} + a_3 {V_{in}}^3 + V_{off}]^n \quad (6)$$

$$B_1 = \frac{1}{b_1}, B_2 = 0, B_3 = \frac{-b_3}{b_1^4}, B_4 = 0$$

After Simplification,

$$V_{DAC} \approx V_{in} - \frac{3a_3 V_{off}}{a_1^2} V_{in}^2 + \frac{V_{off}}{a_1} \quad (7)$$

$$HD_2 = 0.5 \text{ x } \frac{3a_3 V_{off}}{a_1^2} V_{in}$$

Assuming a_1=1, a_3 < 0.01 V^{-2} then V_{off} = 2 to 3 mV is Sufficient to ensure 90dB SFDR!

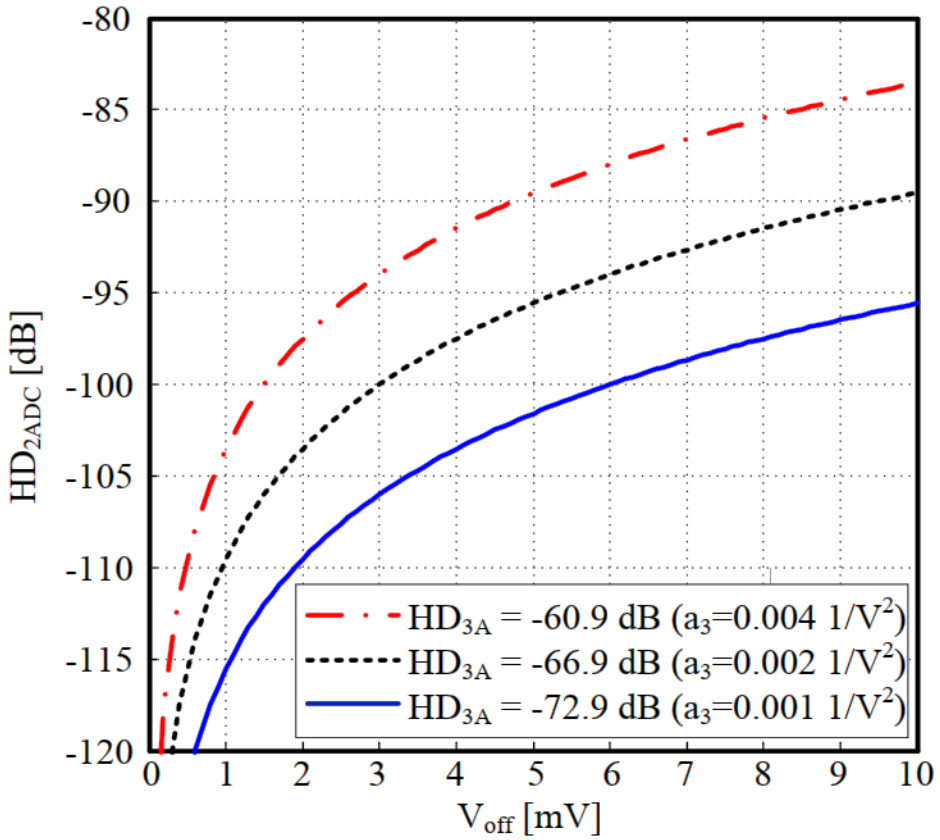


Fig. 10. $HD_{2,ADC}$ VS Comparator Voltage with a_1=0.9

Effect of Phase Imbalance in ADC's differential input path

(Present only during Tracking phase)

$$A_s(V) = a_1 V + a_2 V^2 + a_3 V^3$$

Second order term only cancels if the differential signal is perfectly balanced ($|V_{ip}|=|V_{in}|$ and 180° out of phase).

$$V_{ip} = V_i \sin(\omega t),\ V_{in} = -V_i \sin(\omega t + \phi)$$

$$y_1(t,\phi) = \left(2a_1 v_i + \frac{3a_3 v_i^3}{2}\right)\cos\left(\frac{\phi}{2}\right)\sin(\omega t + \phi_1)$$

$$-a_2 v_i^2 \sin\phi \sin(2\omega t + \phi_2)$$

$$-\left(\frac{a_3 v_i^3}{2}\right)\cos\left(\frac{3\phi}{2}\right)\sin(3\omega t + \phi_3) \qquad (8)$$

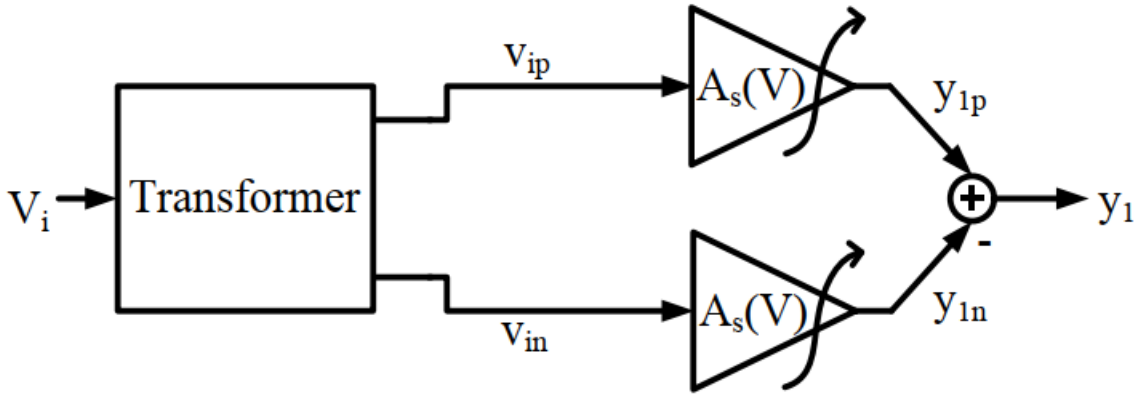


Fig. 11. Differential model of ADC input path

$$Fund_{y_1} \approx 2a_1 \cos\left(\frac{\phi}{2}\right) v_i$$

$$HD_{3,y_1} \approx \frac{a_3 \cos\left(\frac{3\phi}{2}\right)}{4a_1 \cos\left(\frac{\phi}{2}\right)} v_i^2$$

$$HD_{2,y_1} \approx \frac{a_2 \sin\phi}{2a_1 \cos\left(\frac{\phi}{2}\right)} v_i \approx \frac{a_2 \sin\phi}{2a_1} v_i$$

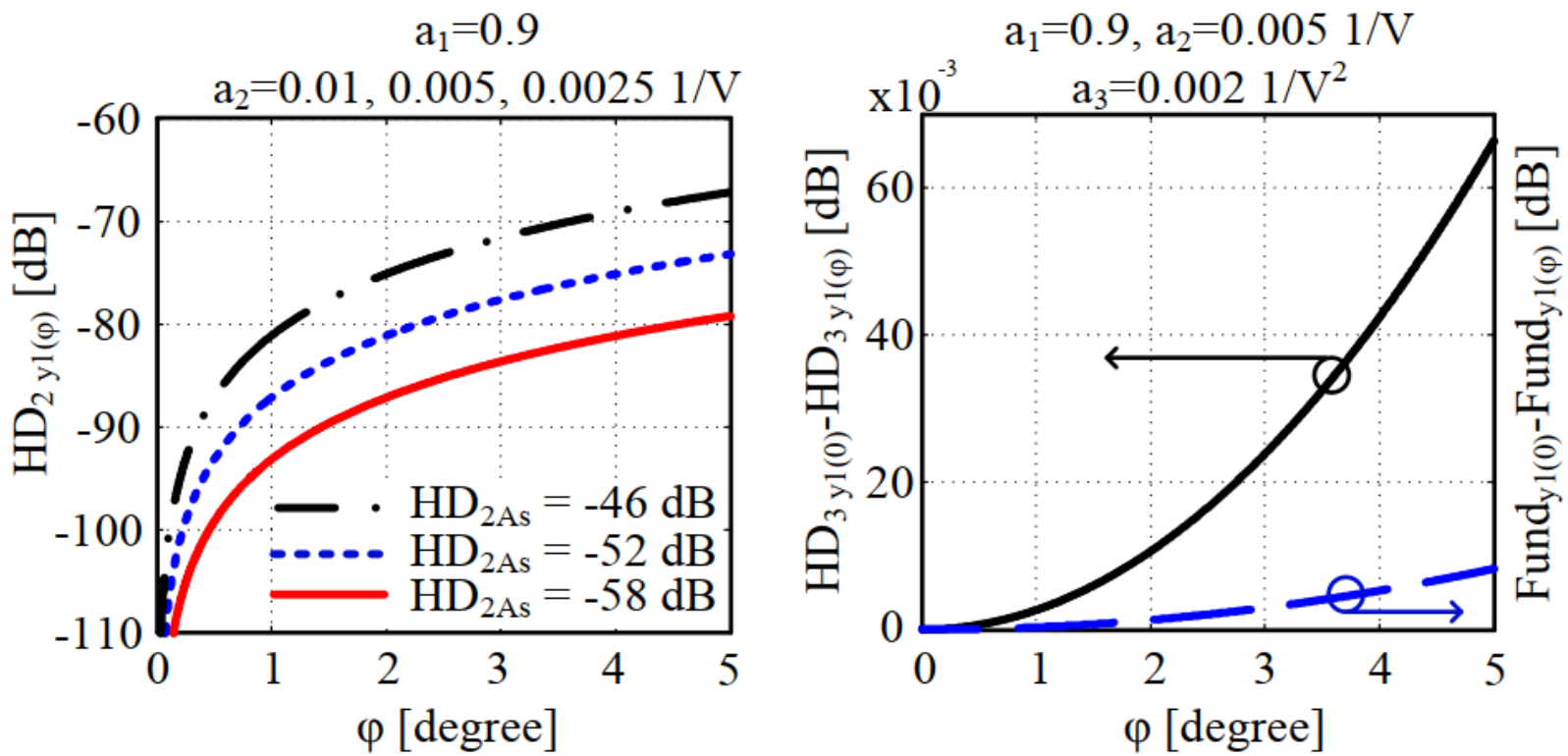
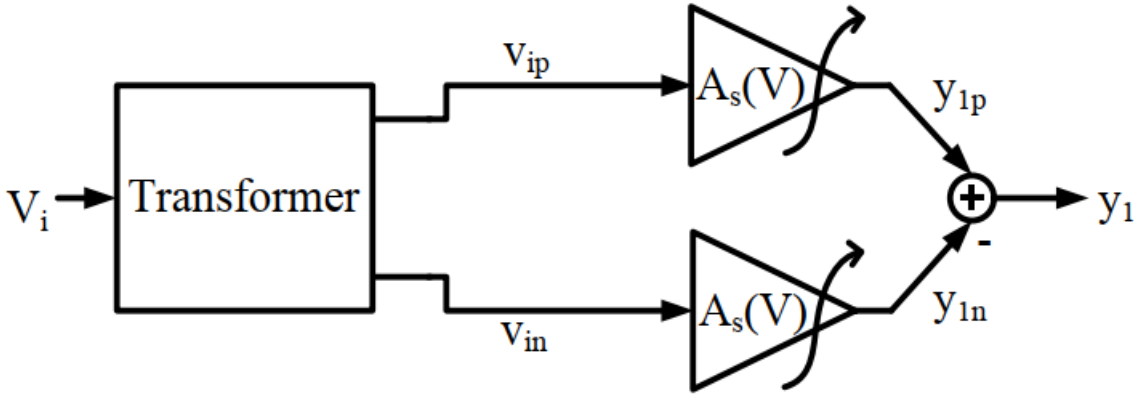


Fig. 12. (a) $HD_{2,y1}$ VS Phase imbalance (b) Fundamental and $HD_{3,y1}$ VS Phase imbalance

$$y_2 = y_1 - a_2 v_i^2 \sin\phi \sin(2\omega t + \phi_2)$$



$$V_{DAC} \approx V_{IN} - \frac{3\left(a_3 a_2 v_i^2 \sin\phi \sin(2\omega t + \phi_2)\right)}{a_1^2} V_{IN}^2 + \frac{a_2 v_i^2 \sin\phi \sin(2\omega t + \phi_2)}{a_1} \qquad (9)$$

Fourth order term

$$Where, \quad V_{IN} \approx 2v_i \sin(\omega t + \phi_1)$$

$$HD_{2ADC} \approx HD_{2,y_1} \approx \frac{1}{2}\frac{a_2}{a_1}\sin(\phi) v_i$$

Noise Modelling (First Order)

ADC Noise Model

$$\overline{V_{ADC}^2} = \overline{e_q^2} + \overline{V_{SN}^2} + \overline{V_{CN}^2}$$

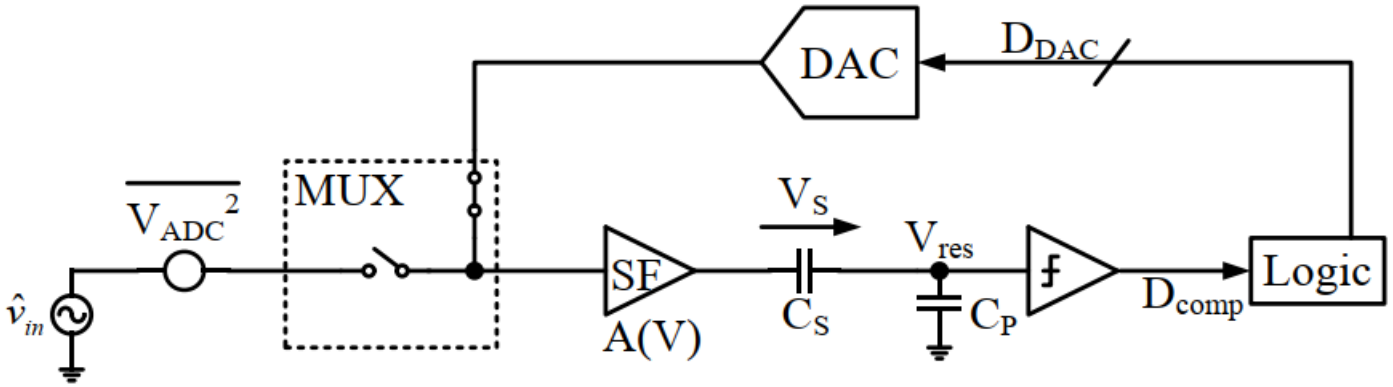


Fig. 13. ADC Noise Model showing input referred ADC noise

$\overline{e_q^2}$ = Quantization Noise

$\overline{V_{SN}^2}$= Sampling Noise

$\overline{V_{CN}^2}$ = Conversion Noise

Tracking Phase

Equivalent noise bandwidth = f_N

$$f_N = \frac{\pi}{2}\frac{1}{2\pi R_{sw}C_s} = \frac{1}{4R_{sw}C_s}$$

$$\overline{V_{SN_{Mux}}^2} = \frac{kT}{C_s}\frac{R_{Mux}}{R_{sw}}G_{SF}^2$$

$$\overline{V_{SN_{sw}}^2} = \frac{kT}{C_s}n_f$$

$$\overline{V_{SN}^2} = 2\left(\overline{V_{SN_{Mux}}^2} + \overline{V_{SN_{sw}}^2}\right)$$

$$\overline{V_{SN_{RES}}^2} = \overline{V_{SN}^2}\cdot\left(\frac{C_s}{C_s + C_P}\right)^2 = \overline{V_{SN}^2}\cdot G_C^2$$

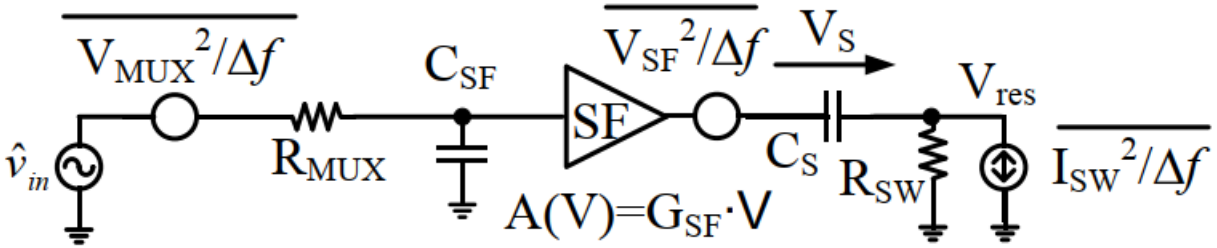


Fig. 14. Half Circuit noise model in Sampling Phase

$$V_{s_{RES}} = V_{in}G_{SF}G_C$$

Conversion Phase

High Bandwidth nodes V_{DAC}, V_{res}
(can cause significant noise increase)

➔ Employment of Gm-C integrator (limits noise Bandwidth)

Equivalent noise bandwidth = f_{NBW}

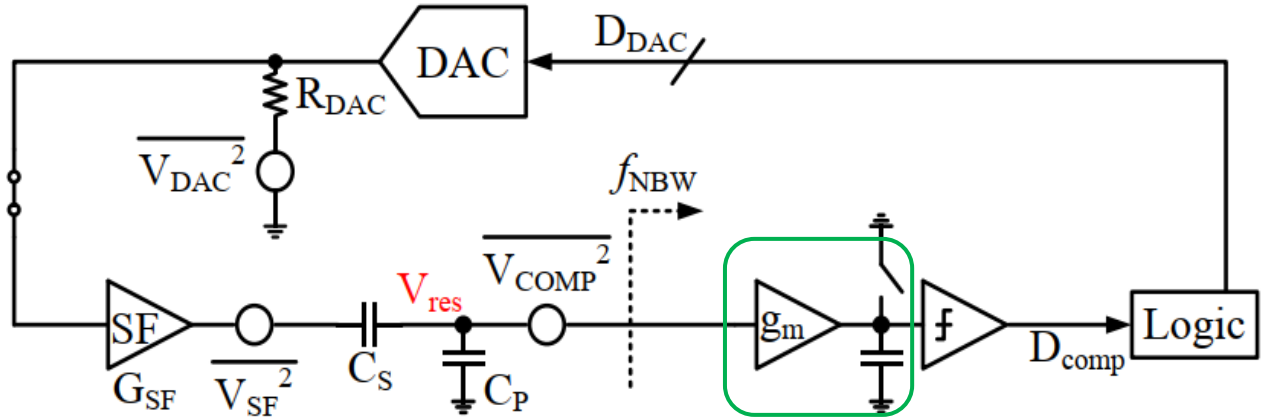


Fig. 15. Noise model for Conversion Phase

$$f_{NBW} = \frac{1}{2\Gamma_{int}}$$

Integration time

$$\overline{V_{SN_{RES}}^2} = \left(G_{SF}^2 G_C^2 \frac{\overline{V_{DAC}^2}}{\Delta f} + G_C^2 \frac{\overline{V_{SF}^2}}{\Delta f} + \frac{\overline{V_{COMP}^2}}{\Delta f} \right) f_{NBW}$$

$$SNR_{ADC} = \frac{\frac{1}{2}\left(V_{s_{RES}}\right)^2}{\overline{e_q^2} G_{SF}^2 G_C^2 + \overline{V_{SN_{RES}}^2} + \overline{V_{CN_{RES}}^2}}$$

INSIGHTS:

➔ Both quantization noise and signal are scaled by buffer gain. No quantization noise penalty for buffer gain < 1.

➔ Conversion Noise depends strongly on T_{int} , To run ADC faster we need to lower T_{int} which increases noise which can be compensated by decreasing R_{DAC} and increasing $g_{m,comp}$ and $g_{m,SF}$ (Increases Power Consumption).

➔ R_{MUX} must be less than $R_{SW.}$

References:

[1] http://www.analog.com/library/analogDialogue/archives/39- 06/data_conversion_handbook.html