Full-Speed Testing of A/D Converters

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Abstract —High-precision analog-to-digital converters (ADC's) are sought for digital audio and instrumentation and high-speed converters for video applications. Improved methods of converter testing at full speed are needed. This paper describes improved computer-aided ADC characterization methods based on the code density test and spectral analysis using the fast Fourier transform (FFT). The code density test produces a histogram of the digital output codes of an ADC sampling a known input. The code density can be interpreted to compute the differential and integral nonlinearities, gain error, offset error, and internal noise. Conversion-rate and frequency-dependent behavior can also be measured.

I. INTRODUCTION

THIS paper describes improved computer-based methods of testing high-precision and high-speed analog-to-digital converters (ADC's) at full speed with full-range dynamic inputs.

A known periodic input is converted by an ADC under test at sampling times that are asynchronous relative to the input signal. The relative number of occurrences of the distinct digital output codes is termed the *code density*. These data are viewed in the form of a normalized histogram showing the frequency of occurrence of each code from zero to full scale. The code density data are used to compute all bit transition levels. Linearity, gain, and offset errors are readily calculated from a knowledge of the transition levels. This provides a complete characterization of the ADC in the amplitude domain. The precision of this measurement may be extended without limit by taking additional data.

Output samples from an ADC also may be processed with a fast Fourier transform (FFT) algorithm to define the linearity and noise properties of the ADC in the frequency domain. This is analogous to the use of analog spectrum analysis to test digital-to-analog (D/A) converters.

For an ideal ADC, the code density is independent of conversion rate and input frequency. The characteristics of practical ADC's (with their associated sample/hold circuits) can be exhaustively tested by varying both the sampling frequency and input frequency. Overall frequency

response can be evaluated using the code density test for several input frequencies.

In high-precision converters ($\geq$ 12 bits), noise is a major concern. The statistical nature of the code density test gives a more accurate characterization of converter noise compared to conventional tests in which each output code is attained only once. Noise amplitude can be computed in rms, peak, or spectral (from FFT) form.

Traditional tests use a digital voltmeter (DVM) to attain high measurement accuracy, but the tests are done with a static or slowly varying input signal. A dynamic input can be created using a digital-to-analog converter (DAC), but it is difficult to separate the errors of the DAC and ADC. Furthermore, resolution is limited; testing a 16 bit ADC with an 18 bit DAC (if it exists) only yields 1/4 bit precision in the ADC test.

II. CODE DENSITY TEST THEORY

The histogram or output code density is the number of times every individual code has occurred. The first observation is that an output code density or histogram bin equal to 0 is a missing code. A shift in the density is an offset error. A change in slope of the ADC transfer curve causes a gain error that may be found by comparison to external amplitude measurements.

For an ideal ADC with a full scale ramp input and random sampling, an equal number of codes is expected in each bin. Differential nonlinearity is the deviation from one least significant (LSB) of the range of input voltages that give the same output code. The number of counts in the ith bin $H(i)$ divided by the total number of samples N_t is the width of the bin as a fraction of full scale. The ratio of bin width to the ideal bin width $P(i)$ is the differential linearity and should be unity. Subtracting one LSB gives the differential nonlinearity in LSB's [1]:

$$DN(i) = \frac{H(i)/N_t}{P(i)} - 1. \qquad (2.1)$$

Integral nonlinearity is the deviation of the transfer curve from ideality. By compiling a cumulative histogram, the cumulative bin widths are the transition levels. Once the transitions are known, the ADC is characterized.

Overall noise is measured by grounding the ADC input and accumulating a histogram. Only the bin for zero input should have counts in it. Any other counts are caused by noise in the ADC.

By increasing the ADC conversion rate and comparing the desired properties such as linearity, the maximum conversion rate for a desired accuracy can be determined. Similarly, varying the input test frequency is a frequency response measurement, a true dynamic test of the ADC. If an external sample-and-hold is used with the ADC, it is also being tested as part of the whole system.

A. Choice of Input Waveform

At first glance, the choice for an input would be a ramp or triangle wave. An equal number of samples per bin is expected, except for the first and last bins which would accumulate all counts for inputs outside the converter's range.

The fundamental drawback to this is the distortion or nonlinearity in the ramp. For a differential nonlinearity test, a 1 percent change in the slope of the ramp would change the expected number of codes by 1 percent. But these errors would quickly accumulate and make the integral nonlinearity test unfeasible. Brief consideration makes it clear that the input source must be known with better precision than the converter being tested.

A random voltage with an equal likelihood of all voltages over a range is desired. Notice that this is not "white noise" which is equal amplitudes at all frequencies. A possible way to generate such a signal is to generate a pseudorandom digital sequence and then use an analog low-pass filter to generate the "random" voltage [2]. The drawback to this method is that the digital sequence must not change amplitude and the filter must be ideal so as not to introduce distortion.

We have used a sine wave signal source. It is precisely known mathematically, and commercial ultralow distortion oscillators have total harmonic distortion < -95 dB. This can be confirmed by a spectral analysis. It is much harder to measure the linearity of a ramp to a comparable level of accuracy.

1) Sine Wave Probability Density: The probability density $p(V)$ for a function of the form $A \sin \omega t$ is

$$p(V) = \frac{1}{\pi\sqrt{A^2 - V^2}}. \tag{2.2}$$

Integrating this density with respect to voltage gives the distribution function $P(V_a, V_b)$:

$$P(V_a, V_b) = \frac{1}{\pi}\left\{ \sin^{-1}\left[\frac{V_b}{A}\right] - \sin^{-1}\left[\frac{V_a}{A}\right] \right\}. \tag{2.3}$$

This is the probability of a sample being in the range V_a to V_b.

For an ADC, let $V_b - V_a = 1$ bit and convert the continuous probability distribution to a discrete distribution:

$$P(i, A) = \frac{1}{\pi}\left\{ \sin^{-1}\left[\left(\frac{2i - 2^n - 1}{2^n}\right)\frac{V_{\text{ref}}}{A}\right] \right.$$
$$\left. - \sin^{-1}\left[\left(\frac{2i - 2^n - 3}{2^n}\right)\frac{V_{\text{ref}}}{A}\right] \right\}. \tag{2.4}$$

This is the probability that a code will be in bin [i] for an input sine wave of amplitude A.

If the input has a dc offset, it is of the form $V_0 + A \sin \omega t$ with density

$$P(V) = \frac{1}{\pi\sqrt{A^2 - (V - V_0)^2}}. \tag{2.5}$$

The new distribution is just shifted by V_0 as expected from the shifted histogram.

$$P(V_a, V_b) = \frac{1}{\pi}\left\{ \sin^{-1}\left[\frac{V_b - V_0}{A}\right] - \sin^{-1}\left[\frac{V_a - V_0}{A}\right] \right\}. \tag{2.6}$$

The discrete distribution becomes

$$P(i, A, V_0) = \frac{1}{\pi}\left\{ \sin^{-1}\left[\left(\frac{2i - 2^n - 1 - 2V_0}{2^n}\right)\frac{V_{\text{ref}}}{A}\right] \right.$$
$$\left. - \sin^{-1}\left[\left(\frac{2i - 2^n - 3 - 2V_0}{2^n}\right)\frac{V_{\text{ref}}}{A}\right] \right\}. \tag{2.7}$$

B. Frequency of Input Waveform

The foundation of the test is that a sine wave is sampled randomly. Sampling at random by its strict definition would be impossible. What must be done is to assure that the sine wave input is not sampled repetitively at the same level. By choosing the sample frequency to be nonharmonically related to the sine wave frequency, we are assured of this. Any jitter in the sample timing or drift in the oscillator frequency will just tend to randomize the sampling.

The effect of sampling at a frequency harmonically related to the input would be n bins with huge positive differential nonlinearity where n is the ratio of sample to input frequency. This can be easily distinguished from differential nonlinearity by varying either the sample or input frequency since differential nonlinearity is independent of frequency.

For a high-speed converter, the conversion rate may exceed the rate at which a computer can assemble the histogram. It is permissible to use very second or nth sample and throw the extras away. Since the samples are taken at random, it does not matter if the first M samples are used or if M out of N samples are chosen.

C. Number of Samples Needed

To find the minimum number of samples needed for estimating the differential nonlinearity, a $100(1 - \alpha)$ percent confidence interval of the form $(\mu - Z_{\alpha/2}\sigma, \mu - Z_{\alpha/2}\sigma)$ is set up. This says that the measured differential nonlinearity lies in the range $(\mu - Z_{\alpha/2}\sigma, \mu + Z_{\alpha/2}\sigma)$ with $100(1 - \alpha)$ percent probability. α is chosen for the desired confidence level. $Z_{\alpha/2}\sigma$ is the precision to which the measured value differs from the true value μ. The derivation of σ and the subsequent minimum number of samples needed is carried out in the Appendix.
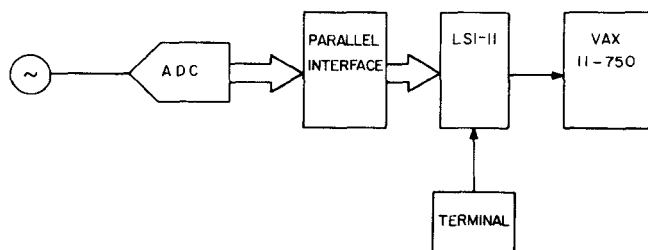
Fig. 1.   Experimental setup for testing an ADC with the code density test or FFT test.

The minimum number of samples N_t needed for β bit precision and $100(1-\alpha)$ percent confidence is given by (2.8) where $Z_{\alpha/2}$ can be found in a table of the standard normal distribution function:

$$N_t \geq \frac{Z_{\alpha/2}^2 \pi 2^{n-1}}{\beta^2}. \tag{2.8}$$

To know the differential nonlinearity for an 8 bit converter to within 0.10 bit with 99 percent confidence, 268 000 samples are needed. In the 12 bit case, for 99 percent confidence and 0.10 bit precision, 4.2 million samples are needed.

III. HARDWARE FOR A/D CONVERTER TESTING

The experimental setup shown in Fig. 1 consists of the input source, ADC system under test, a parallel interface to an LSI-11 minicomputer, and a VAX 11-750. The ADC system consists of the ADC, a sample-and-hold if needed, voltage references, and control circuitry.

Parallel data from the ADC are latched and buffered on the interface board before being read by the LSI-11 through a parallel I/O port. The LSI-11 was used to accumulate the data since it had a parallel input port and 64K of 16 bit memory, enough to test a 16 bit ADC, and was available with the *Speechlab* [3] program for digital I/O, as well as communication with a VAX 11-750 running UNIX.

Any computer can be used to compile the histogram provided it has enough n-bit memory for 2^n bins and the I/O histogram program. Depending on the time needed to compute the ADC transitions and the availability of a high-level language, the characterization could be computed on the same machine. In our work, once a histogram is completed, it is written to a UNIX file on a VAX 11-750 where the nonlinearity computations are carried out.

IV. SOFTWARE FOR A/D CONVERTER TESTING

The software is used in two stages. *Speechlab* is used to take the histogram and *JADE* to compute the ADC errors. *Speechlab* is a general-purpose program written in C for an LSI-11 to do analog I/O via an ADC and DAC, as well as digital I/O through a DRV-11 parallel I/O board.

A modified version of *Speechlab* is used to gather data to test ADC's. Originally input data were stored sequen-
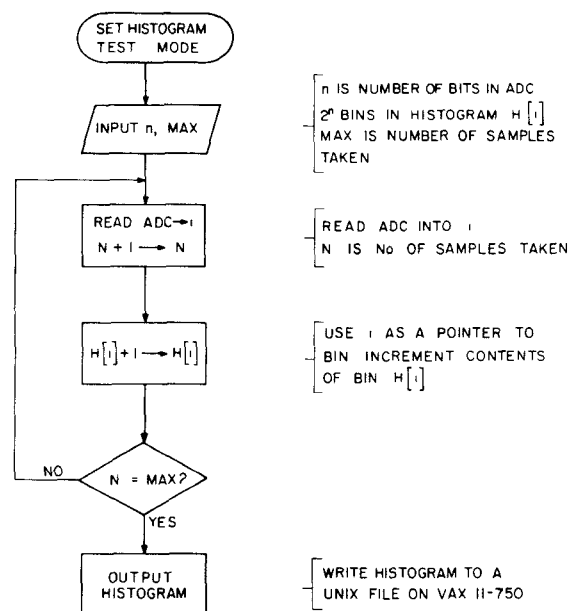

Fig. 2.   Flowchart for histogram accumulating program running on the LSI-11.

tially in memory so only 64K samples could be taken. This is barely enough for testing an 8 bit ADC. The main modification was to use the digital code as a pointer to a memory location used as a counter as shown in Fig. 2. Incrementing that counter each time it is accessed forms the histogram.

A future improvement will be to write the data input and histogram routine in Assembly language rather than C to improve upon the 9 kHz data input rate by approximately a factor of 2.

Program *JADE* does the ADC analysis from the histogram data and is shown functionally in Fig. 3. It is written in C and runs on a UNIX system.

The program first gets command line arguments to set options such as data type and output listings. The user then enters the name of the binary file containing the histogram. Next the offset voltage is computed and a cumulative histogram is compiled. From this, the transition levels are computed, leading to the nonlinearity calculations.

Once an ADC is characterized, the differential nonlinearities and integral nonlinearities can be written to ASCII or binary files and plotted on a graphics terminal. A statistics file contains informations such as the input offset, LSB size, and the maximum and minimum nonlinearities, etc.

A. Algorithms for A/D Converter Error Computation

The offset voltage is found from the shift of the histogram about the midpoint 0 V. If $V_0 = 0$, the number of codes above zero, N_p, equals the number of codes below zero, N_n:

$$N_n = \sum_{i=1}^{2^{n-1}} H[i] \qquad N_p = \sum_{i=2^{n-1}+1}^{2^n} H[i]. \tag{4.1}$$

START

READ n, FILENAME

READ H[i]

$\frac{\pi}{2} \text{SIN} \frac{N_p - N_n}{N_p + N_n} \rightarrow V_0$

$\sum_{j=0}^{i} H[j] \rightarrow CH[i]$

$\cos(\frac{\pi CH[i]}{N_T}) \rightarrow V[i]$

$\frac{V[i] - V[i]}{1 LSB} - (i-1) \rightarrow IN[i]$

$\frac{V[i+1] - V[i]}{1 LSB} \rightarrow DN[i]$

OUTPUT NONLINEARITIES

GET PROGRAM OPTIONS

ENTER NUMBER OF BITS AND HISTOGRAM FILENAME

READ HISTOGRAM FILE TO H[i]

COMPUTE OFFSET VOLTAGE, V_0

COMPILE CUMULATIVE HISTOGRAM, CH[i]

COMPUTE TRANSITION VOLTAGES, V[i]

COMPUTE INTEGRAL NONLINEARITY, IN[i]

COMPUTE DIFFERENTIAL NONLINEARITY DN[i]

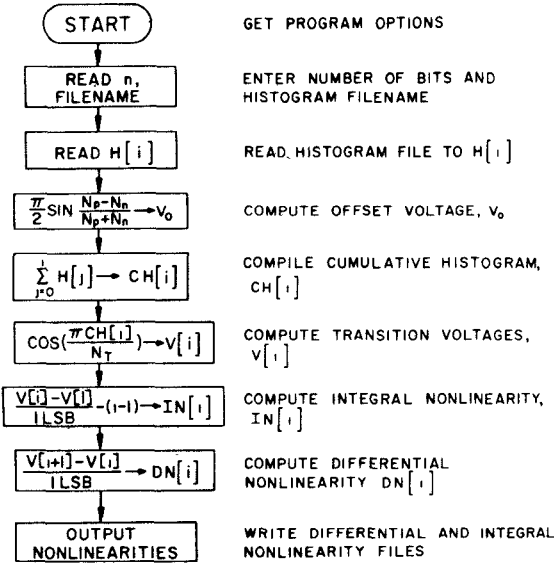WRITE DIFFERENTIAL AND INTEGRAL NONLINEARITY FILES

Fig. 3. Flowchart for code density analysis program which computes the ADC transitions from the histogram.

The probability p_p that any randomly sampled voltage is positive is the probability that it is in the range $(0, A + V_0)$ and is found from (2.6) to be

$$p_p = \frac{1}{\pi} \left\{ \sin^{-1}(1) - \sin^{-1}\left[\frac{V_0}{A}\right] \right\} \qquad (4.2)$$

$$= \frac{1}{2} + \frac{1}{\pi} \sin^{-1} \frac{V_0}{A}. \qquad (4.3)$$

And the probability p_n that a negative voltage is sampled is

$$p_n = 1 - p_p. \qquad (4.4)$$

Solving (4.3) and (4.4) for V_0,

$$V_0 = A \frac{\pi}{2} \sin(p_p - p_n). \qquad (4.5)$$

An estimate of V_0, $\hat{V}_0$ can be obtained by replacing the unknown population frequencies p_p and p_n by the observed sample frequencies N_p/N_t and N_n/N_t:

$$\hat{V}_0 = A \frac{\pi}{2} \sin \frac{N_p - N_n}{N_p + N_n} \qquad (4.6)$$

where N_p and N_n are the number of positive and negative samples, respectively.

When the offset voltage is small relative to the sine amplitude, this can be approximated

$$\hat{V}_0 = A \frac{\pi}{2} \frac{N_p - N_n}{N_p + N_n}. \qquad (4.7)$$

In computing the differential nonlinearity, substituting (2.7) into (2.1) for $P(i)$ is unfeasible and incorrect.

It is unfeasible since the amplitude of the sine wave A must be known with great precision because the differential nonlinearity calculation is a very strong function of A. To see the accuracy and precision to which A must be known, assume a perfect ADC. Now if A is thought to be

equal to full scale, a certain number of codes is expected in bin [1] and bin $[2^n]$. But if A is just $A - 1/2$ LSB, approximately $1/2$ as many codes will be obtained and the differential nonlinearity will be $-1/2$ bit in these two bins. When too few codes go into these two bins, other bins get the extra codes, resulting in excess positive differential nonlinearity.

V_{ref}, the full-scale voltage reference, is needed, but being a dc quantity, it can be measured with a DVM to sufficient precision. The term A, however, is the peak voltage with a dc offset, not an rms voltage, and is measured less accurately with a DVM than a dc voltage. Most DVM's measure ac quantities at 60 Hz and do not have the bandwidth to measure A at a few kilohertz.

The second consideration is due to the nonlinearity of the sine wave. Twice as many codes are not expected from a bin that is twice as wide as an ideal bin (i.e., 1 LSB differential nonlinearity). As the bins get narrower with a higher precision converter, the density can be linearized, but this is an approximation.

The statistically correct method to measure the nonlinearities is to estimate the transitions from the data. Then the differential nonlinearity is the difference between adjacent transition levels minus 1 LSB. The integral nonlinearity is the difference between the estimated transition level and the ideal transition level.

In (2.6) and (2.3), $P(V_a, V_b)$ is replaced by the measured frequency of occurrence H/N_t using the "frequency substitution principle" and then solved for $\hat{V}_b$, which is an estimate of V_b.

In solving (2.6), the offset V_0 can be eliminated since it only shifts $\hat{V}_b$ and V_a. It does not affect the integral or differential nonlinearity. Thus, the simpler (2.3) can be solved for $\hat{V}_b$. Taking the cosine of both sides of (2.3) and using the following identities yields (4.10):

$$\cos(\alpha - \beta) = \cos(\alpha)\cos(\beta) + \sin(\alpha)\sin(\beta) \qquad (4.8)$$

$$\cos\left(\sin^{-1}\frac{V}{A}\right) = \frac{\sqrt{A^2 - V^2}}{A} \qquad (4.9)$$

$$\hat{V}_b^2 - \left(2V_a\cos\left(\frac{\pi H}{N_t}\right)\right)\hat{V}_b$$
$$- A^2\left(1 - \cos^2\left(\frac{\pi H}{N_t}\right)\right) + V_a^2 = 0. \qquad (4.10)$$

The quadratic equation (4.10) can be solved for $\hat{V}_b$. In the solution, the positive square root term is used so that $\hat{V}_b$ is greater than V_a:

$$\hat{V}_b = V_a\cos\left(\frac{\pi H}{N_t}\right) + \sin\left(\frac{\pi H}{N_t}\right)\sqrt{A^2 - V_a^2}. \qquad (4.11)$$

This gives $\hat{V}_b$ in terms of V_a. In general,

$$\hat{V}_i = V_{i-1}\cos\left(\frac{\pi H(i)}{N_t}\right) + \sin\left(\frac{\pi H(i)}{N_t}\right)\sqrt{A^2 - V_{i-1}^2}. \qquad (4.12)$$

Rather than a recursive formulation that is subject to cumulative errors, $\hat{V}_i$ can be computed directly by using the boundary condition $V_0 = -A$ and using a cumulative histogram $CH(i)$ of i bins instead of the ith histogram bin $H(i)$:

$$\hat{V}_i = -A \cos\left(\frac{\pi CH(i)}{N_t}\right). \qquad (4.13)$$

A is not known, but being a linear factor, all transitions $\overline{V}_i$ can be normalized to A so that the full range of transitions is ± 1.

To estimate the integral nonlinearity with the same precision as the differential nonlinearity, many more samples and a much longer testing time are required. Thus, drifts in the ADC voltage reference and the sine wave oscillator's amplitude and offset voltage can give erroneous results. The FFT test is not sensitive to these problems since very few samples are needed.

V. FFT INTEGRAL NONLINEARITY TEST

The discrete Fourier transform computed with a fast Fourier transform algorithm can be used to measure the nonlinearity of the ADC transfer function. The setup is as before, but this time the data taken are not put in a histogram. They are just stored in the sequence taken, sent to a UNIX file, and then Fourier transformed.

The spectrum of the output will contain the input sine wave, quantization error, and any harmonic distortion caused by integral nonlinearity. The theoretical signal-to-noise ratio is $(6n + 1.8)$ dB [4]. If the harmonic distortion is more than $6n$ dB below the fundamental amplitude, the error caused by integral nonlinearity can be concluded to be less than 1 bit and therefore negligible.

The input frequency must be chosen so that harmonics aliased into the baseband do not add to the fundamental. The raw data from the ADC were modified by a "Hanning window" [5] to reduce the effects of truncating a sine wave before a FFT. If the sampled data contain an integral number of periods of the input sine wave, the FFT will be accurate. If the samples contain a fraction of a sine wave period, the FFT will have gross distortions.

VI. TESTING FOR SPECIFIC APPLICATIONS

The specific application and nonlinearity errors of the ADC should dictate the type of test to be performed. If the application is for instrumentation, the quantity to be tested is differential and integral nonlinearity so the code density test is appropriate. If the use is in a digital audio system, the appropriate tests would be in the frequency domain. The FFT would be interpreted for harmonic distortion, frequency response, S/N, etc.

The code density test is most sensitive to differential nonlinearity errors, while an FFT test is most sensitive to integral nonlinearity errors. Thus, the type of error to be
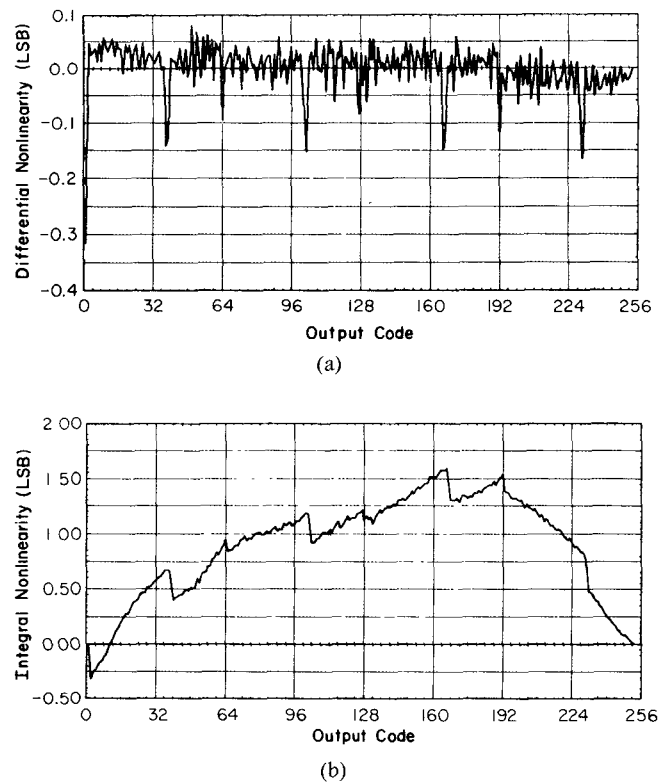

(a)

(b)

Fig. 4.   8 bit, CMOS, resistor-string ADC. (a) Differential nonlinearity. (b) Integral nonlinearity.

measured, rather than the application of the ADC, would be a factor in determining which test to use.

VII. CODE DENSITY TEST RESULTS

Three different designs of A/D converters were tested. All were of the successive approximation variety. The first was an 8 bit, resistor-string, CMOS converter, the second a 12 bit, bipolar, laser-trimmed, R-$2R$ ladder converter, and the third a 15 bit, CMOS, self-calibrating ADC with a capacitor array and resistor string.

For the 8 bit, resistor-string ADC, 268 000 samples corresponding to a 0.1 bit precision with 99 percent confidence were taken. The differential nonlinearities and integral nonlinearities are shown in Fig. 4(a) and (b). There are no differential nonlinearities greater than 1/4 bit; thus, the integral nonlinearity is smooth and is never greater than 2 bits. Manufacturers will often pass a best-fit-line through this integral nonlinearity plot and claim ± 1 LSB integral nonlinearity with a gain and offset error. There is no pattern to the errors that are from random mismatches in the resistor string.

With only 5000 samples, the integral nonlinearity is no longer smooth, but has the same shape and approximately the same worst case error. However, the differential nonlinearity has a large degree of uncertainty, but the major nonlinearities are visible.

For the 12 bit, R-$2R$ ADC, the major carries are clearly visible where the integral nonlinearity jumps 1 bit. The differential nonlinearity in Fig. 5(a) shows large spikes that
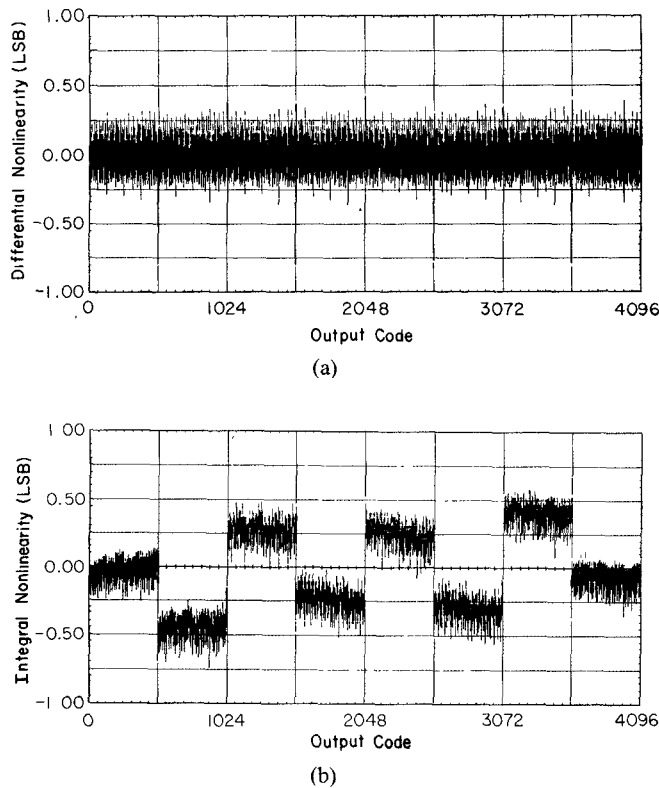
(a)

(b)

Fig. 5. 12 bit, bipolar, laser-trimmed, R-$2R$ ADC. Note the spikes in the differential nonlinearity and jumps in the integral nonlinearity at the major carry transitions. (a) Differential nonlinearity. (b) Integral nonlinearity.
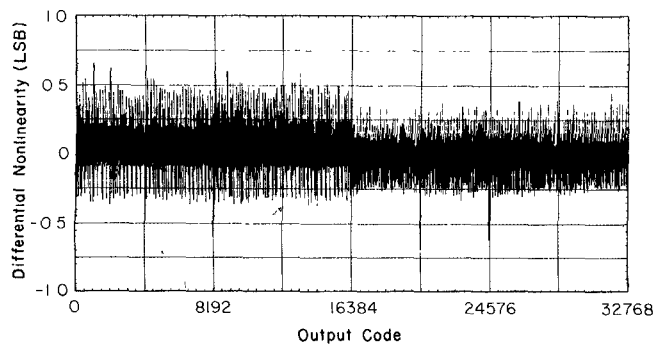

Fig. 6. Differential nonlinearity for 15 bit, CMOS, self-calibrating ADC with capacitor array main DAC and resistor-string sub-DAC.

correspond to resistor mismatches. The other errors appear periodic since the resistors with untrimmed, random errors are used repeatedly over the range of the ADC. This is in contrast to the resistor string where each resistor is used once; hence, the errors are not periodic.

The 15 bit self-calibrating ADC with capacitor-array main DAC and resistor-string sub-DAC differential non-linearity plot is shown in Fig. 6.

A. FFT Test Results

The 12 bit R-$2R$ ADC was used for the FFT test. Fig. 7(a) is a 4096-point FFT of a 495 Hz sine wave sampled at 8012 Hz. The harmonics are clearly visible 72 dB below the fundamental, corresponding to 12 bit integral linearity. This is within the 1 bit integral nonlinearity specified for
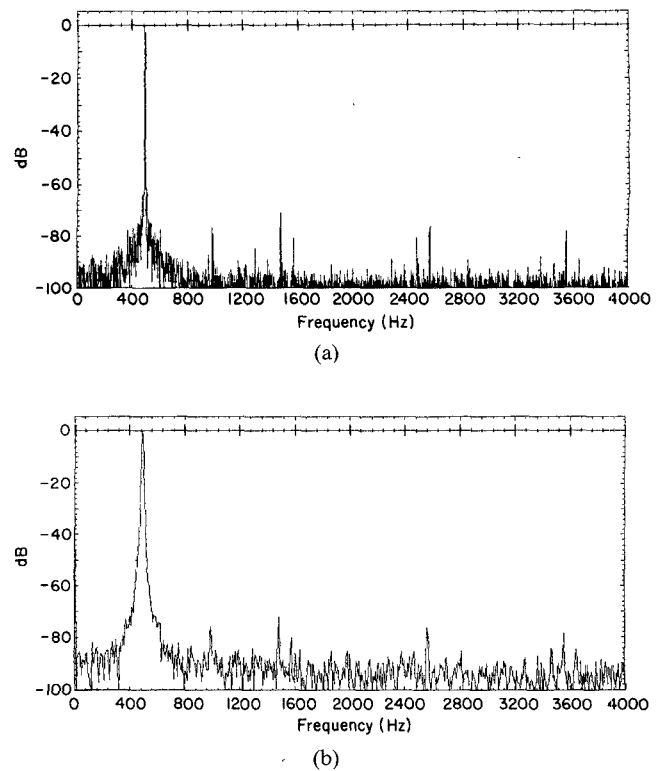

(a)

(b)

Fig. 7. FFT spectrum for a 12 bit ADC sampling a 495 Hz sine wave. (a) 4096-point FFT. (b) 1024-point FFT.
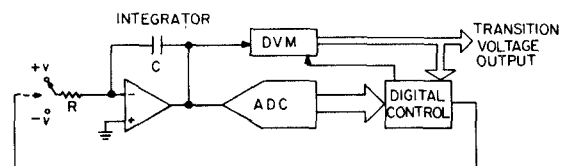

Fig. 8. Classical method of ADC testing. The integrator is forced to the transition voltage and measured by the DVM.

the converter. In Fig. 7(b), 1024 samples are used. Since each sample in the time domain corresponds to one point in the frequency domain, the features are less clear. The decreasing number of samples again increases the noise level, as would a less precise A/D converter.

VIII. COMPARISON TO CLASSICAL TESTING

A classical ADC test is shown conceptually in Fig. 8 [6]. The integrator is driven to each transition and held at that voltage while a computer-controlled DVM measures the transition point. This is an extremely slow process since the integrator loop must settle and then the DVM takes a reading.

The first drawback to this test is that the accuracy of the test depends on the DVM. More important is that this is a static test of the ADC. The ADC is measuring a dc voltage, not a high-frequency input. Most converters are tested this way, but they claim the same characteristics and accuracy for a maximum conversion rate dynamic input. There is no measurement of dynamic errors. With the histogram and FFT tests, the input can be as high a frequency as desired to test for frequency-dependent errors.
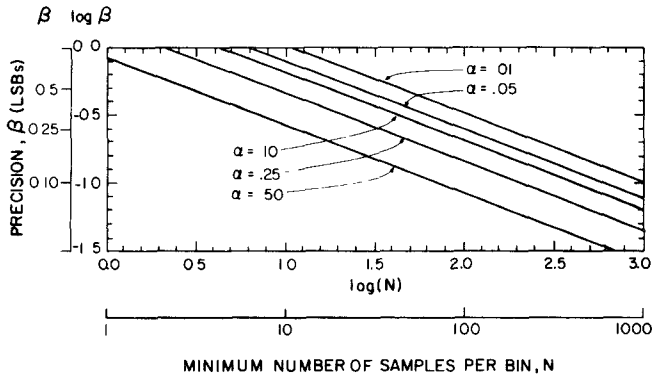
Fig. 9. Minimum number of samples needed per bin for differential nonlinearity test. The parameters are β, the precision of the estimate, and α, the confidence level.

Testing a high-precision converter by the classical method can be in error due to noise at the ADC input. But the histogram test being statistical and sampling each bin many times rather than once will average out any random noise.

The precision of the classical test is limited by the DVM. But in the histogram test, taking more samples increases the precision. Extending the classical test to higher precision converters is again limited by DVM precision and accuracy. With a histogram test, the input source must be known to more precision than the ADC and can be easily verified with a spectrum analyzer. Lastly, the minicomputer must have enough memory to store 2^n histogram bins.

The integrator loop takes approximately 5 s to measure each transition or 5 2/3 h to completely test a 12 bit ADC. If a precision DAC is used instead of an integrator, the speed should increase by a factor of 10 to about 30 min, which is still very slow.

With a histogram of 1000 counts per bin, for 99 percent confidence with 0.1 bit precision, it will take 9 min to take the data at a 8 kHz input rate. For production testing, the confidence level and precision can be reduced to 95 percent and 0.25 bit precision, decreasing the number of samples needed and the testing time by a factor of 10. Fig. 9 shows the tradeoffs among confidence level, precision, and the number of samples required. The testing time can also be reduced by taking the data faster since the rate is currently limited by the minicomputer, not the ADC under test.

IX. D/A CONVERTER TESTING

To test D/A converters, a dual of the histogram test is sought. This would be a number generator input to the DAC and a device quantizing the analog output and counting the number of occurrences of each output to get a histogram. But the quantization is done by an ADC, and has the same disadvantages as using a DAC to test the ADC's, that is, speed, precision, and noise.

However, a dual of the FFT test is an analog spectrum analysis. Input a digital since wave to the DAC and look at the spectrum. Ideally, there will be the fundamental, quan-

tization noise, and harmonic distortion. The level of harmonic distortion is related to the nonlinearity of the DAC transfer curve just as integral nonlinearity in the ADC was deduced from a FFT.

X. SUMMARY

The code density test produces a histogram of the digital output codes of an ADC sampling a known input. The code density is used to compute the voltage transition levels that characterize the ADC. This test is completely general in that it tests high-precision and high-speed converters. It is superior to a traditional "transition test" since it is done at full speed with a dynamic input and the results do not depend on the accuracy of a DAC or DVM. FFT tests are performed to measure the integral nonlinearity, distortion, and signal-to-noise ratio. Unlike classical test methods, the methods proposed here also test the "sample-and-hold" and can measure the internal noise of the ADC. D/A converters can be tested by a dual of the FFT test, using a digital sine wave input and an analog spectrum analyzer.

APPENDIX

The uncertainty in the differential nonlinearity is the uncertainty in the width of the bin $\hat{V}_{i+1} - \hat{V}_i$. From (4.13),

$$\hat{V}_{i+1} - \hat{V}_i = - A \left\{ \cos\left(\frac{\pi CH(i+1)}{N_t} \right) - \cos\left(\frac{\pi CH(i)}{N_t} \right) \right\} \tag{A1}$$

$$= - A \left\{ \cos\left(\frac{\pi (CH(i) + H(i))}{N_t} \right) - \cos\left(\frac{\pi CH(i)}{N_t} \right) \right\}. \tag{A2}$$

$CH(i)$ is the total number of codes in bins 1 through i and $\Delta CH(i) = H(i+1)$ is the number of codes in bin $[i+1]$. Now define $F(X) = \cos \pi X/N_t$:

$$\hat{V}_{i+1} - \hat{V}_i = - A [F(CH(i) + \Delta CH(i)) - F(CH(i))] \tag{A3}$$

$$= \frac{- A [F(CH(i) + \Delta CH(i)) - F(CH(i))]}{\Delta CH(i)}$$

$$\cdot \Delta CH(i) \tag{A4}$$

$$\approx - A \frac{dF(CH(i))}{dCH(i)} \Delta CH(i) \tag{A5}$$

$$= \frac{A\pi \Delta CH(i)}{N_t} \sin\left(\frac{\pi CH(i)}{N_t} \right). \tag{A6}$$

$\Delta CH(i)$ and $CH(i)$ are random variables, but we can assume that $CH(i)$ is known since it only affects the integral nonlinearity, and this confidence interval is for the differentail nonlinearity. Thus, the random variable is

$\Delta CH(i)$ and $\hat{V}_{i+1} - \hat{V}_i$ is of the form

$$Y = A \frac{\pi}{N_t} \sin\left(\frac{\pi CH(i)}{N_t}\right) X. \qquad (A7)$$

Let the random variable $\Delta CH(i) = X$ and be distributed with mean μ_x and standard deviation σ_x with the following notation: $X \sim (\mu_x, \sigma_x)$. If $Y = aX + b$, then $Y \sim (a\mu_x + b, a\sigma_x)$.

$$\mu_y = a\mu_x + b = \left(A \frac{\pi}{N_t} \sin\left(\frac{\pi CH(i)}{N_t}\right)\right)\mu_x \qquad (A8)$$

$$\sigma_y = a\sigma_x = A \frac{\pi}{N_t} \sin\left(\frac{\pi CH(i)}{N_t}\right)\sigma_x. \qquad (A9)$$

Now the mean μ_x and standard deviation σ_x of the random variable $\Delta CH(i)$ are needed to find μ_y and σ_y.

Any given sample with either go in bin $[i]$ or it will not go in bin $[i]$. This is a two outcome, or Bernoulli trial, with binomial distribution characterized by mean $np(1 - p) \approx np$ since $p \ll 1$ and standard deviation $\sqrt{np}$. The total number of samples taken is $n = N_t$, and p is the probability that a sample goes in a bin. Thus, $\Delta CH(i) \sim B(np, \sqrt{np})$.

From (A8) and (A9),

$$\mu_y = pA\pi \sin\left[\frac{\pi CH(i)}{N_t}\right] \qquad (A10)$$

$$\sigma_y = \sqrt{p} \, A \frac{\pi}{\sqrt{N_t}} \sin\left[\frac{\pi CH(i)}{N_t}\right]. \qquad (A11)$$

If the number of samples is large, the binomial distribution can be approximated by a Normal or Gaussian distribution and

$$P\left[\mu_y - Z_{\alpha/2}\sigma_y \le \mu \le \mu_y + Z_{\alpha/2}\sigma_y\right] = 1 - \alpha \qquad (A12)$$

can be found for any choice of α. $Z_{\alpha/2}$ is the number of standard deviations which can be found from a tabulated listing of the standard normal distribution for any chosen alpha. Thus, the measured bit width μ_y, which is nominally 1 bit, lies within its true value with tolerance $Z_{\alpha/2}\sigma_y$ with $100(1 - \alpha)$ percent confidence. Thus, $Z_{\alpha/2}\sigma_y \le \beta\mu_y$. $\beta\mu_y$ is the tolerance to which the bit width is known. Substituting (A10) and (A11) for σ_y and μ_y,

$$\frac{Z_{\alpha/2}^2}{N_t\beta^2} \le p. \qquad (A13)$$

p is the probability of a sample going in a bin and is a function of the bin $[i]$, so the minimum p, $P(2^{n-1})$ corre-

sponding to a zero input or bin $[2^{n-1}]$ is used.

$$P(2^{n-1}) = \frac{1}{\pi}\left\{\sin^{-1}\left[\frac{V_{\text{ref}}}{2^n A}\right] - \sin^{-1}\left[-\frac{V_{\text{ref}}}{2^n A}\right]\right\}$$

$$= \frac{2}{\pi}\sin^{-1}\left[\frac{V_{\text{ref}}}{A2^n}\right]. \qquad (A14)$$

For $V_{\text{ref}} \approx A$, this reduces to $(2/\pi)$, $\sin^{-1}[1/2^n]$. For any reasonable value of n, the $\sin^{-1}$ argument is small, and $\sin^{-1}(x) \approx x$ so $p = P(2^{n-1}) = 1/\pi 2^{n-1}$. The condition is that

$$N_t \ge \frac{Z_{\alpha/2}^2 \pi 2^{n-1}}{\beta^2}. \qquad (A15)$$

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