# Design of SAR ADC for Low Power Applications

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# List of Abbreviations

| Symbols | Description |
|---|---|
| *ADC* | Analog-to-Digital Converter |
| *CMOS* | Complementary Metal Oxide Semiconductor |
| *DAC* | Digital-to-Analog Converter |
| *DFF* | D-Flip Flop |
| *DNL* | Differential Non-Linearity |
| *ENOB* | Effective Number of Bits |
| *FFT* | Fast Fourier Transform |
| *FOM* | Figure of Merit |
| *INL* | Integral Non-Linearity |
| *ISSCC* | International Solid-State Circuits Conference |
| *MIM* | Metal Insulator Metal |
| *MOM* | Metal Oxide Metal |
| *SAR* | Successive Approximation Register |
| *SFDR* | Spurious-Free Dynamic Range |
| *SNDR* | Signal-to-Noise-and-Distortion Ratio |
| *SNR* | Signal-to-Noise Ratio |

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# Chapter 1

# Introduction

## 1.1 Motivation

Analog-to-digital converters (ADCs) play a critical role in bridging the gap between the continuous analog world and the discrete digital domain. They function by transforming real-world, continuous-time signals (such as voltages or currents) into digital representations, enabling processing by digital circuits and microprocessors. This conversion process is fundamental in various applications, particularly those requiring the interaction between analog sensors and digital systems.

## Low-Power ADCs: A Necessity for Resource-Constrained Applications

The demand for low-power consumption in electronic devices is ever-increasing. This is especially true for applications such as:

**Bio-Electrical Interfaces:** Devices like pacemakers and neural implants rely on batteries or harvested energy (e.g., from body heat). Low-power ADCs ensure efficient conversion of biosignals without compromising battery life or implant functionality.

**Space Applications:** Power is a precious commodity in spacecraft, where solar panels or radioisotope thermoelectric generators (RTGs) provide limited energy. Low-power ADCs are crucial for on-board data acquisition and processing.

**Wireless Sensor Nodes:** These tiny, battery-powered devices collect and transmit data from their environment. Minimizing power consumption extends their operational lifetime and reduces the frequency of battery replacements.

Bioelectric signals are shown in Fig. 1.1 [1] , exhibit a relatively limited dynamic range, typically spanning tens of microvolts to millivolts. Additionally, their frequency spectrum is confined, usually falling below 10 kHz. These characteristics influence the selection of appropriate Analog-to-Digital Converters (ADCs) for processing such signals.

Considering these constraints, medium-resolution, low-speed ADCs are sufficient for bioelectric signal acquisition. This thesis focuses on the design of low-power ADCs optimized for this specific application. The target specifications aim to achieve a balance between moderate resolution (around 10 bits) and a sampling rate (around 1 Msps) suitable for use in medical implant devices.

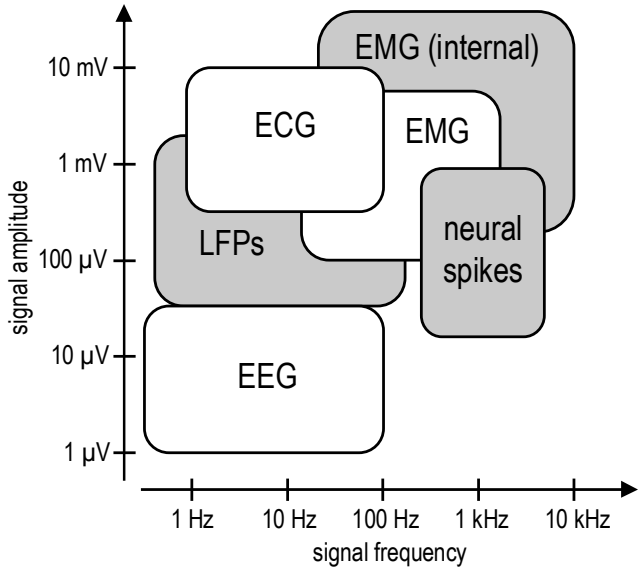


Figure 1.1: Approximate frequency content and amplitude distribution of common biopotentials recorded from the surface of the skin (white boxes) or internally (grey boxes).

## 1.2 Organization

The remainder of this thesis is organized as follows. Chapter 2 presents a concise introduction to the fundamental principles and operational characteristics of SAR ADC. It delves further into the individual building blocks that constitute a SAR ADC, exploring their functionalities and the relevant non-idealities associated with each block. These non-idealities can significantly impact the overall performance of the ADC and are crucial considerations for the design process. Chapter 3 focuses on the specific design choices made for the project. It details the architecture of the implemented SAR ADC and provides component sizing employed. Chapter 4 presents the simulation results obtained for the implemented SAR ADC design.

# Chapter 2

# Literature Review

Since low-power operation is paramount for this project, selecting an appropriate architecture for the ADC critically influences its overall performance. To make an informed decision, we examined the power consumption characteristics of existing nyquist ADCs. Fig. 2.1 depicts the power consumption of various ADC architectures plotted against their sampling rate (Nyquist rate). Similarly, Fig. 2.2 illustrates the power consumption plotted against the Signal-to-Noise and Distortion Ratio (SNDR) of the ADCs. The data presented in these figures is based on ADCs published in the International Solid-State Circuits Conference (ISSCC) proceedings between 1997 and 2024, as referenced in [2].

Based on the analysis of these figures, we observe the following trends: Successive Approximation Register (SAR) ADCs are typically well-suited for low-speed applications with medium-to-high resolution requirements due to their efficient power consumption characteristics. Pipelined ADCs dominate the medium-speed and medium-resolution range, offering a balance between speed and power. Flash ADCs and Time-Interleaved ADCs are often preferred for high-speed applications with lower resolution demands. However, they tend to be less power-efficient compared to SAR ADCs for the targeted application scope.

Considering the desired balance between speed and resolution in our project, Successive Approximation Register (SAR) ADCs emerge as the primary candidate architecture due to their superior power efficiency at the targeted performance range.

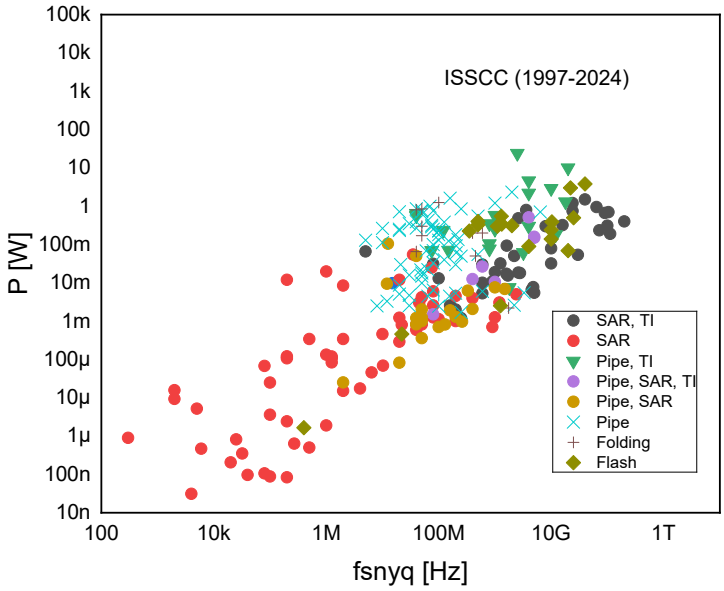


Figure 2.1: Power VS Nyquist Sampling Rate

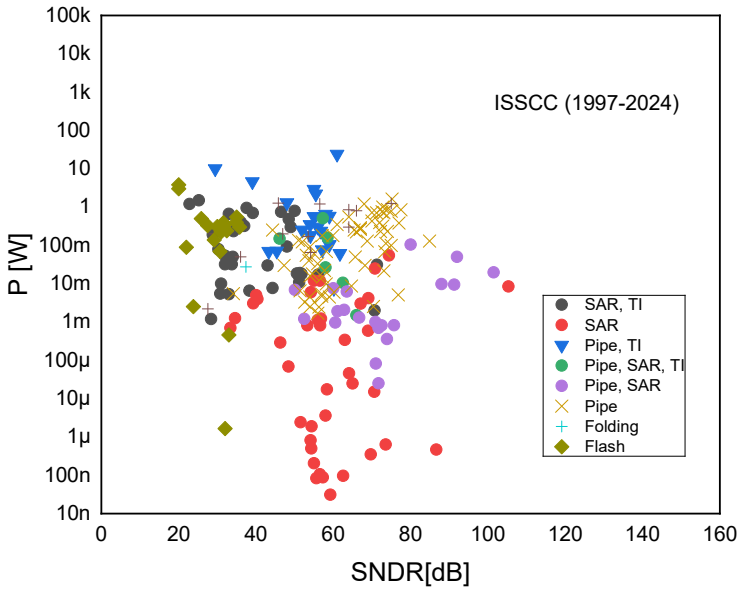


Figure 2.2: Power VS SNDR

## 2.1 SAR Architecture

The Successive Approximation Register (SAR) architecture is a well-established and widely employed technique for analog-to-digital conversion (ADC). Fig. 2.3 illustrates the basic architecture of a SAR ADC. To convert an analog input signal into a digital representation, ADCs perform three fundamental tasks: sampling, quantization, and comparison. In a SAR ADC, these tasks are accomplished sequentially by dedicated circuits:

**Sampling Circuit:** This circuit captures the analog input signal at a specific point in time and holds the sampled value for the duration of the conversion process.

**Capacitive Digital-to-Analog Converter (DAC):** This circuit generates a voltage reference based on a digital code. In a SAR ADC, the capacitive DAC typically uses binary-weighted capacitors to achieve this functionality.

**Comparator:** This circuit compares the voltage from the sampled analog input with the reference voltage generated by the capacitive DAC.

The SAR Logic plays a crucial role in controlling the operation of the capacitive DAC. It employs a binary search algorithm to iteratively refine the digital output code. The comparator compares the resulting DAC reference voltage with the sampled analog input. Based on the comparison result, the SAR logic adjusts the subsequent bits of the output code, converging on the digital representation that most closely approximates the analog input voltage. The final digital output code stored on the register represents the quantized value of the analog signal.

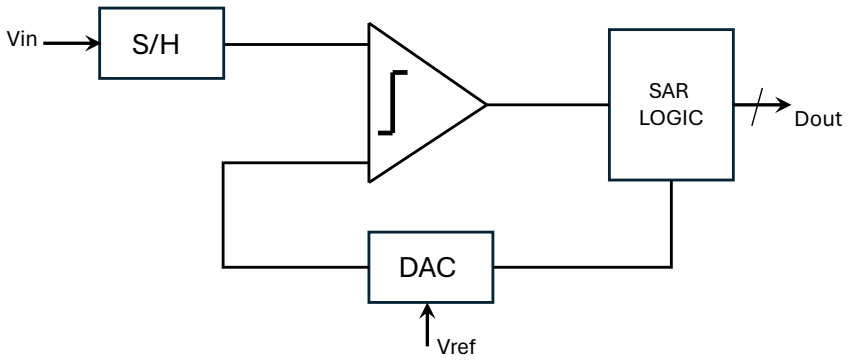


Figure 2.3: SAR ADC Block Diagram (single ended input)

### 2.1.1 Sample and Hold Circuit

Sampling circuit consists of a switch and a capacitor as shown in Fig. 2.4. Switch can be a single MOSFET (NMOS or PMOS) or Transmission gate (CMOS). MOS devices have on resistance which depends on gate-to-source voltage.

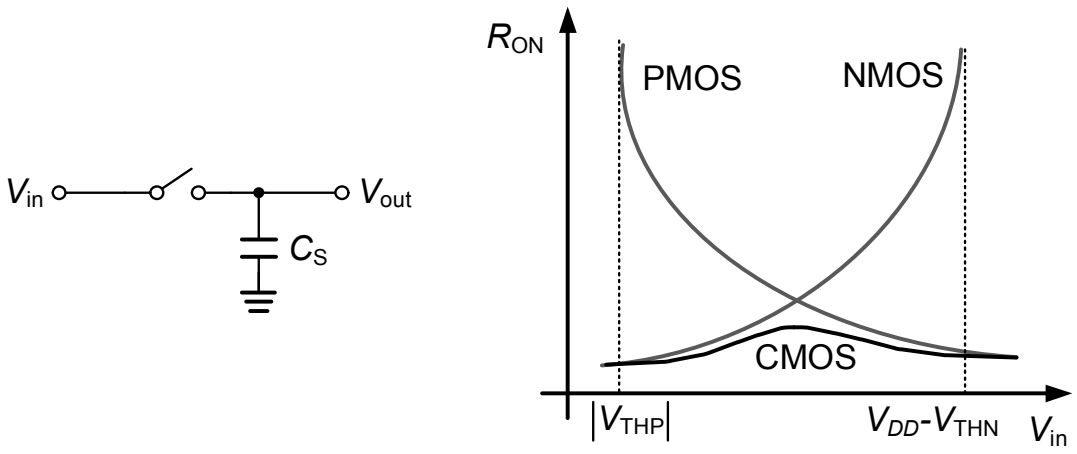


Figure 2.4: Sample and Hold Circuit with Switch 'on' resistance characteristics

The sampling circuit acts as a low pass filter, with bandwidth $f_{3,dB}$.

$$f_{3dB} = \frac{1}{2\pi R_{on} C_S} \tag{2.1}$$

From the transient response analysis, the sampled voltage error can be estimated. Assuming this error to be less than 1/2 LSB we can estimate time budget ($t_b$) to be allocated for sampling.

$$e^{-\frac{t_b}{R_{on}C_S}} < \frac{1}{2^{N+1}} \tag{2.2}$$

$$t_b > R_{on} \cdot C_S \cdot ln2 \cdot (N+1) \tag{2.3}$$

When switch is turned off Voltage droop is introduced by the leakage current of the switch, this becomes a critical source of error as the sampling rate becomes low. The subthreshold leakage current [6] of the transistor is the dominant leakage contributor to the switch, it is expressed as shown in Eq. (2.4).

$$I_{DS} = \mu C_{ox} \frac{W}{L} (n-1) V_T^2 e^{\frac{V_{GS}-V_{th}}{mV_T}} \times (1 - e^{-\frac{V_{DS}}{V_T}}) \tag{2.4}$$

Other non idealities exist for practical sample and hold circuits [7]. These are listed in the form of Table below.

| Non idealities | Source of Error | Occurrence | Solution |
|---|---|---|---|
| Charge injection | Channel Charge | Holding state | Slow clock edges |
| Clock Feedthrough | Parasitic capacitances | Holding state | Slow clock edges |
| Aperture error | Slow clock edges + Clock jitter | Transition state | Fast clock edges |
| Thermal noise | On Resistance of switch | Sampling state | Increase $C_s$ |

Table 2.1: Sample and Hold Non Idealities

The rms of Thermal noise for sampling circuit is given by,

$$V_{n,rms} = \sqrt{\frac{K_B T}{C_s}} \tag{2.5}$$

$K_B$ is the Boltzmann constant, T is the absolute temperature in kelvin. Assuming the thermal noise equal to quantization noise (assuming uniform Q.N.), the total noise power will be increased by a factor of two. Therefore SNR of ADC will be reduced by 3dB. Then the minimum value of sampling capacitor $C_s$ can be calculated by,

$$C_s = \frac{12 K_B T}{LSB^2} \tag{2.6}$$

### 2.1.2 Capacitive DAC

In SAR ADCs, capacitor arrays are preferred over resistive DACs for generating reference voltages. They are more easily fabricated with less mismatch errors and consume less power.

Capacitive DACs employ various architectures, including binary-weighted, thermometer-coded, and split-capacitor based designs. The selection of a particular architecture is primarily driven by considerations of die area, circuit complexity, and the extremity of component matching within the DAC.

#### 2.1.2.1 Binary weighted Capacitive DAC

The unit capacitor, denoted as $C_u$ , should be kept as small as possible for power saving. In practice, it is usually determined by the thermal noise and capacitor mismatch. From Eq. (2.6) we can find out $C_{u,n}$ as,

$$C_{u,n} = \frac{12 K_B T}{2^N \times LSB^2} \tag{2.7}$$

Statistically unit capacitor is modelled by nominal value of $C_u$ with standard deviation $\sigma_u$. Defining $\sigma_{u,r}$ as relative standard deviation of $C_u$. Then for a binary-weighted capacitor array, the worst-case standard deviation of differential nonlinearity (DNL) and integral nonlinearity (INL) occur at the MSB code transition due to the accumulation of the capacitor mismatch. Following the analysis in [8], they can be expressed as

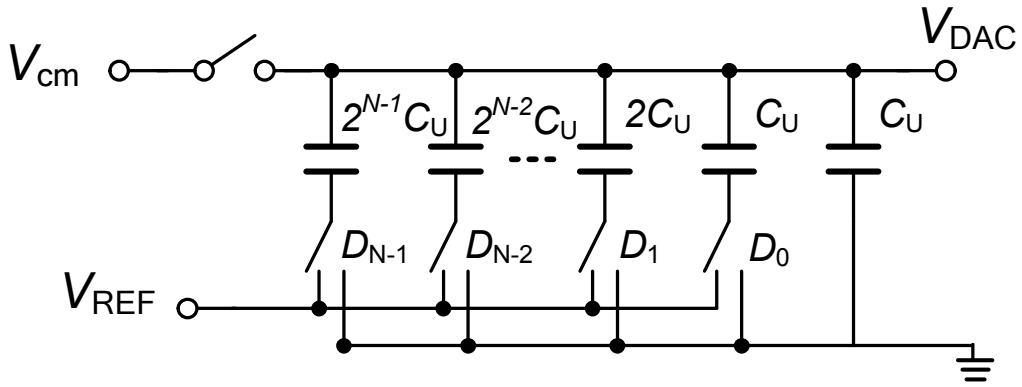


Figure 2.5: Binary weighted Capacitive DAC

$$\sigma_{DNL,max} = \sqrt{2^N - 1} \times \sigma_{u,r} \times LSB \tag{2.8}$$

$$\sigma_{INL,max} = \sqrt{2^{N-1}} \times \sigma_{u,r} \times LSB \tag{2.9}$$

The worst-case standard deviation of DNL is larger than that of INL, so we choose DNL as reference for yield estimation. For a typical metal-insulator-metal (MIM) capacitor relative mismatch is given as

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{K_\sigma}{\sqrt{A}} \tag{2.10}$$

$$C = K_C \cdot A \tag{2.11}$$

$\sigma\left(\frac{\Delta C}{C}\right)$ is the standard deviation of capacitor mismatch (It is $\sqrt{2}$ times greater than $\sigma_{u,r}$), $K_\sigma$ is the matching coefficient, A is the capacitor area, and $K_C$ is the capacitor density parameter. For high yield, it is necessary to maintain $3\sigma_{DNL,max} < 0.5$LSB. From solving earlier equations, we obtain a lower bound for the mismatch-limited unit capacitor.

$$C_{u,m} = 18 \cdot (2^N - 1) \cdot K_\sigma^2 \cdot K_C \tag{2.12}$$

For the differential configuration, the unit capacitance can be reduced by half than given by Eq. (2.12) while still satisfying the mismatch requirement. This is because the differential mode doubles the signal range but only increases $\sqrt{2}$ times of the error voltage introduced by the mismatch.

#### 2.1.2.2 Thermometer coded Capacitive DAC

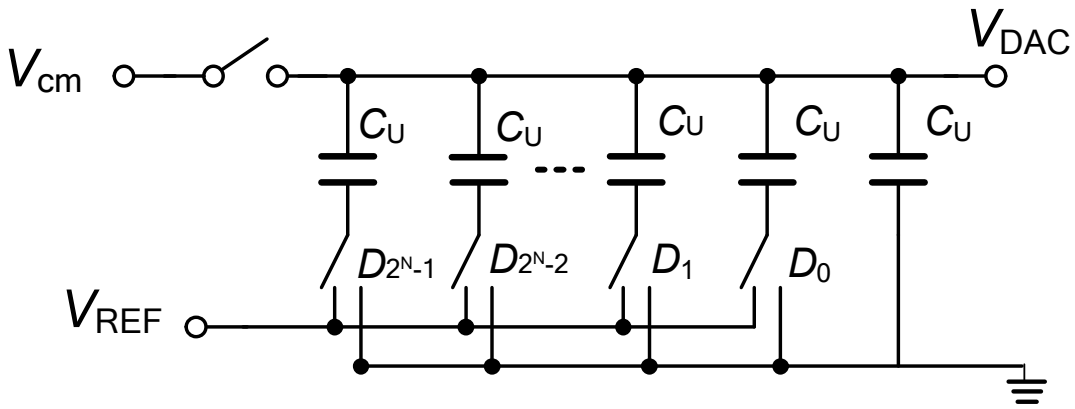


Figure 2.6: Thermometer coded Capacitor DAC

For a Thermometer-weighted capacitor array, the worst-case standard deviation of differential nonlinearity (DNL) and integral nonlinearity (INL) can be expressed as

$$\sigma_{DNL,max} = \sigma_{u,r} \times LSB \tag{2.13}$$

$$\sigma_{INL,max} = \sqrt{2^{N-1}} \times \sigma_{u,r} \times LSB \tag{2.14}$$

The worst-case standard deviation of INL is larger than that of DNL, so we choose INL as reference for yield estimation. Following the same procedure we obtain lower bound for the mismatch-limited unit capacitor.

$$C_{u,m} = 18 \cdot (2^{N-1}) \cdot K_\sigma^2 \cdot K_C \tag{2.15}$$

#### 2.1.2.3 Split Binary-weighted Capacitive DAC

The modified split-capacitor DAC array [5] is shown in Fig. 2.7 where a single unit capacitor is used as a bridge capacitor. This modification is used since it is difficult to realize fraction of unit capacitance as in normal split capacitor based DAC, which leads to nonlinear distortion. This topology induces the gain error of $\frac{1}{1-2^{-N}}$ , where N (Total resolution) = M (resolution of Main DAC) + S (resolution of sub-DAC). This error is linear and can be easily compensated through calibration techniques during post processing. From the analysis in [8], the mismatch limited unit capacitor is given by,

$$C_{u,m} = 18 \cdot (2^M - 1) \cdot 2^{2(N-M)} \cdot K_\sigma^2 \cdot K_C \tag{2.16}$$

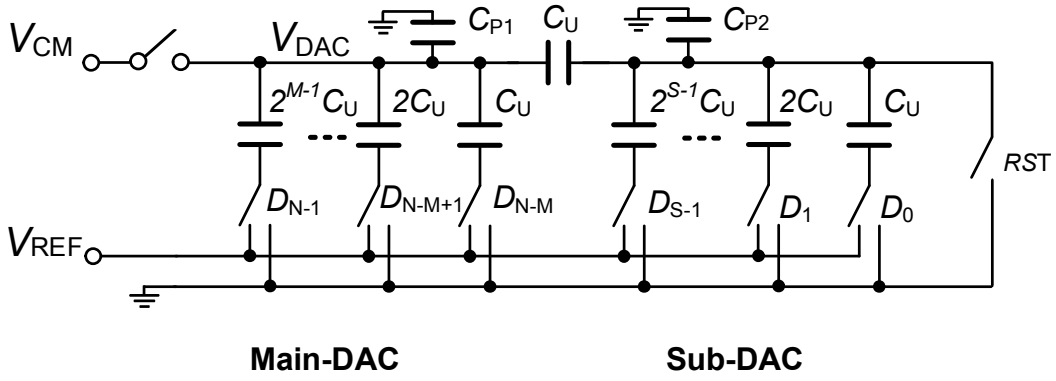


Figure 2.7: Modified split Binary-weighted Capacitor DAC

#### 2.1.2.4 Area Comparision

The number of unit capacitors [9] in a DAC is given by,

$$N_{C_U} = 2^M + 2^S - 1 + N_{Dummy} \tag{2.17}$$

$$N_{Dummy} = 4\left[\sqrt{2^M + 2^S - 1}\right] + 4 \tag{2.18}$$

The total capacitive array area is determined by the area of the single unit capacitor and the number of unit capacitors($N_{C_U}$). DRC rules and contacts add overhead to the unit capacitance area as shown in Fig. 2.8.

$$A_{C_{u,real}} = \left(\sqrt{A_{C_u}} + HO\right) \cdot \left(\sqrt{A_{C_u}} + VO\right) \tag{2.19}$$

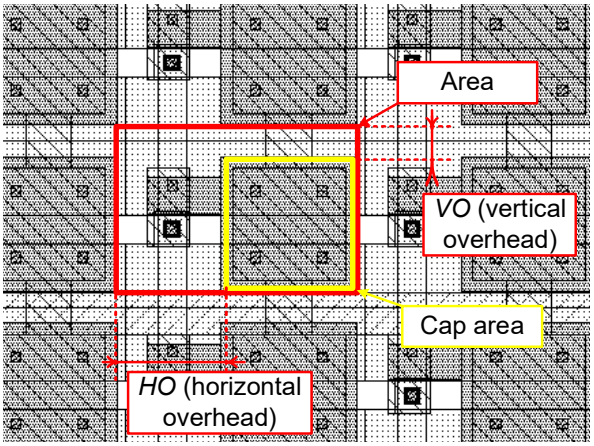


Figure 2.8: capacitor layout (MIM) with the overhead area for DRC and capacitor contacts

In Fig. 2.7 we see parasitic capacitances modeled as additional capacitors $C_{p1}$ and $C_{p2}$. The capacitance $C_{p2}$ has strong influence on the DAC linearity. In order to reduce its influence, the capacitance $C_{p2}$ needs to be as small as possible. It is composed of top plate parasitic capacitances in the sub DAC array and the top plate parasitic capacitance of the bridge capacitor. we can write expression for the output voltage of the DAC if the input code is B = $b_{N-1}...b_0$

$$C_{p2} = \alpha(C_{sum,sub} + C_B) = \alpha(\sum_{i=0}^{S-1} 2^i C_U + C_U) = \alpha 2^S C_U \tag{2.20}$$

$$\begin{aligned} V_{DAC}(B) = & \frac{C_U(\sum_{i=0}^{S-1} b_i 2^i C_U + \sum_{i=0}^{M-1} b_{i+S} 2^i C_U)}{C_{denom}} \cdot (V_{CM} - V_{ref}) + \\ & \frac{(C_{sum,sub} + C_{p2}) \sum_{i=0}^{M-1} b_{i+s} 2^i C_U}{C_{denom}} \cdot (V_{CM} - V_{ref}) \end{aligned} \tag{2.21}$$

$$where \quad C_{denom} = C_U(C_{sum,sub} + C_{sum,main} + C_{p1} + C_{p2}) + (C_{sum,sub} + C_{p2}) \cdot (C_{sum,main} + C_{p1})$$

$$LSB = \frac{C_U^2 \left(2^N - 1\right) + C_U C_{p2} \left(2^M - 1\right)}{C_{denom}} \cdot (V_{CM} - V_{ref}) \tag{2.22}$$

Using expressions (2.21) and (2.22) we can derive the expression for maximal differential nonlinearity due to parasitics for MSB code transistion as,

$$DNL_{max,par} = \frac{V_{DAC}(1000\cdots) - V_{DAC}(0111\cdots)}{LSB} - 1 = \frac{\left(C_U + C_{p2}\right)\left(2^N - 1\right)}{C_U(2^N - 1) + C_{p2}(2^M - 1)} - 1 \tag{2.23}$$

From the above expression we see that by reducing the number of capacitors in the Main DAC array it leads to the increased nonlinearity. Hence we need to modify yield expression from $3\sigma_{DNL,max} < 0.5$LSB to $3\sigma_{DNL,max} < 0.5$LSB -$DNL_{max,par}$. This leads to change in equation (2.16),

$$C_{u,m} = 18 \cdot (2^M - 1) \cdot 2^{2(N-M)} \cdot K_\sigma^2 \cdot K_C \cdot \left(\frac{0.5}{0.5 - DNL_{max,par}}\right)^2 \tag{2.24}$$

| **Type of DAC [10bit]** | $K_\sigma$=1%$\mu m$, $K_C$=1$fF/\mu m^2$, $\alpha$=0%. $C_{U,m}$ = | $N_{C_U}$ |
|---|---|---|
| Binary weighted | 1.84fF | 1155.94 |
| Thermometer coded | 0.92fF | 1155.94 |
| Split Capacitor (M=S=5) | 57.14 fF | 98.75 |

Table 2.2: Mismatch Summary of DAC architectures

Among the architectures in Table 2.2, the thermometer-coded DAC boasts the smallest unit capacitor value ($C_U$) and the lowest total area ($A_{C_{total}}$). However, it comes at the cost of higher switching complexity and the additional requirement for thermometer-to-binary converters. Furthermore, the minimum achievable capacitance ($C_{min}$) on the technology node imposes a limitation on this architecture.

Both binary-weighted and split-capacitor DACs share the same number of switches, making them more attractive from an implementation standpoint. To evaluate their area efficiency in terms of unit capacitor utilization we introduce $R_U$ ,

$$R_U = \frac{A_{C_{U,sc}}}{A_{C_{U,bw}}} = \frac{(2^M - 1)\cdot 2^{2(N-M)}}{(2^N - 1)} \times \left(\frac{0.5}{0.5 - DNL_{max,par}}\right)^2 \tag{2.25}$$

Total Capacitance Area ratio AR(M) is given by,

$$AR(M) = \frac{A_{sc}}{A_{bw}} = \frac{\left(\sqrt{A_{C_{U,bw}} R_U} + HO\right)\left(\sqrt{A_{C_{U,bw}} R_U} + VO\right)}{\left(\sqrt{A_{C_{U,bw}}} + HO\right)\left(\sqrt{A_{C_{U,bw}}} + VO\right)} \times \frac{N_{CU,sc}}{N_{CU,bw}} \tag{2.26}$$

To identify the effect of parasitics on area efficiency of split capacitor topology, we plot Eq. (2.26) for different values of alpha with three different overhead values ($0.1\sqrt{A_{C_{U,bw}}}$, $0.25\sqrt{A_{C_{U,bw}}}$,$0.5\sqrt{A_{C_{U,bw}}}$) for a 10-bit DAC.

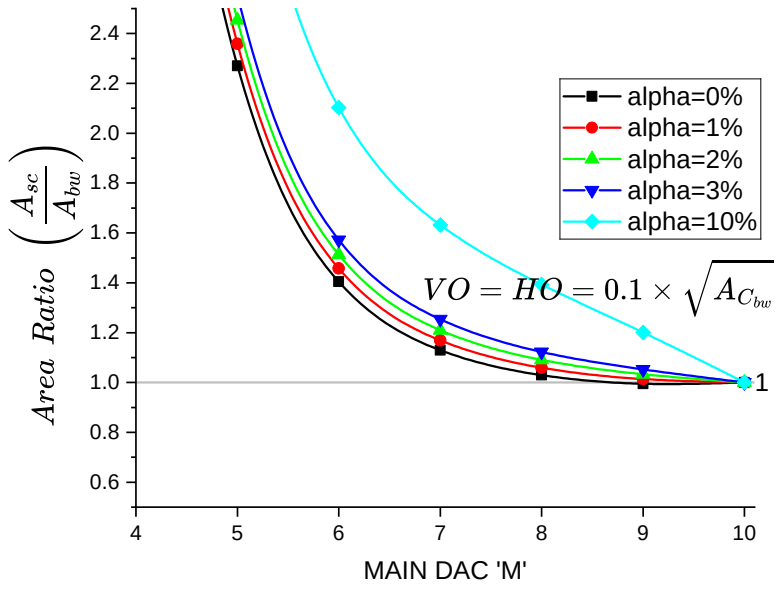


Figure 2.9: Plot of area ratio vs 'M' with overhead = 10%

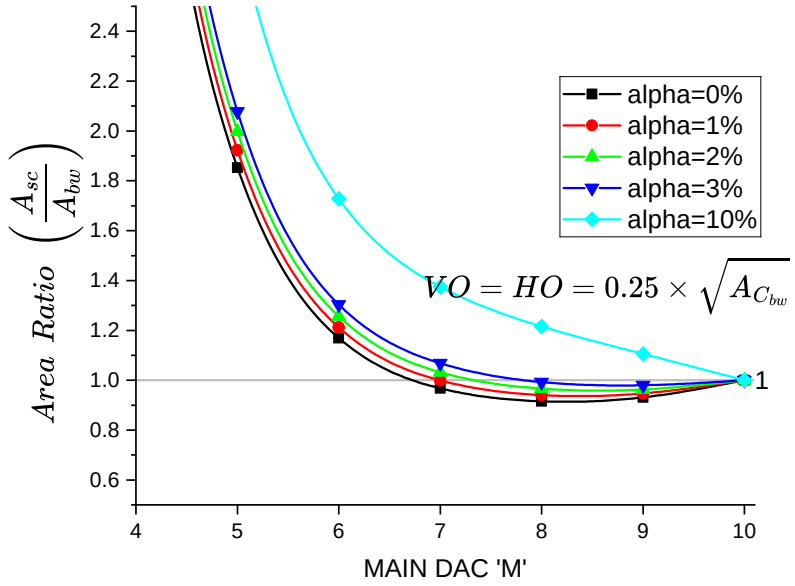


Figure 2.10: Plot of area ratio vs 'M' with overhead = 25%

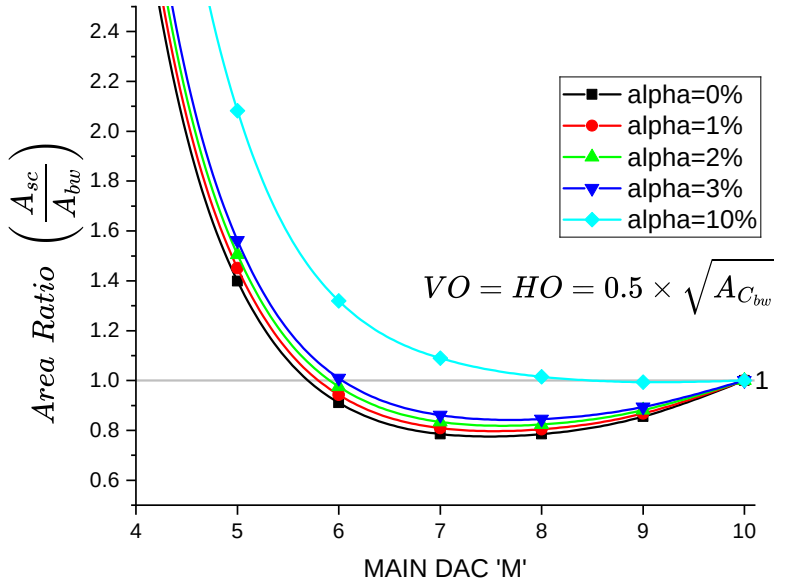


Figure 2.11: Plot of area ratio vs 'M' with overhead = 50%

#### 2.1.2.5 Monotonic Switching Scheme

Traditional SAR ADC's used binary weighted DAC's with bottom plate sampling where the input common mode is kept constant throughout the conversion phase. In 2010, Liu [3] proposed monotonic switching scheme with top plate sampling. In monotonic switching, the input common mode gets gradually pulled to supply or ground depending on upwards or downwards switching. Fig. 2.12 shows how voltage on DAC varies over time for conventional switching and monotonic switching. Following Liu, modifications to monotonic scheme were presented [4, 10] to improve the energy efficiency and area reduction even further.

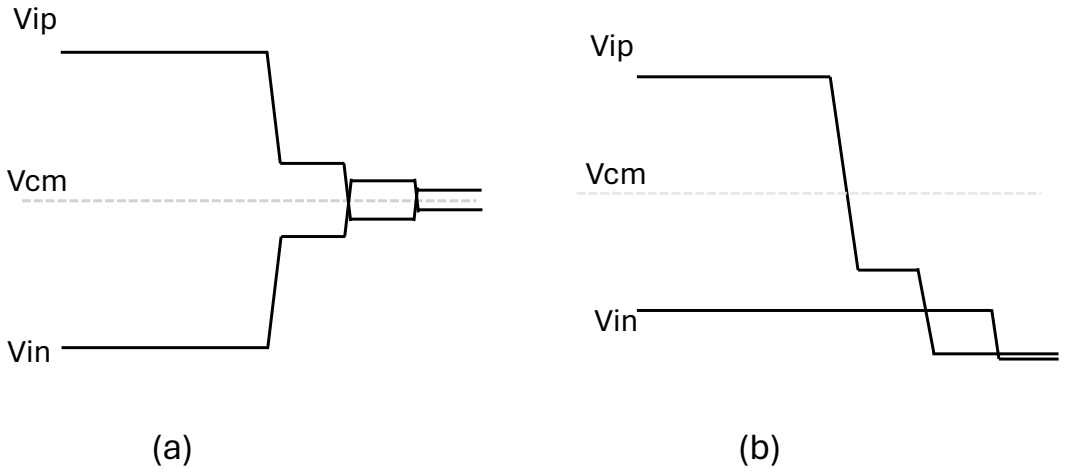


Figure 2.12: (a) conventional switching procedure (b) monotonic switching procedure

### 2.1.3 Dynamic Comparator

Fig. 2.13 shows schematic of dynamic comparator [3]. In the monotonic switching method for DAC, the voltage on top plate of the capacitors drops towards ground. Thus, the comparator input voltages are reduced, tending to zero volts. For this reason, it is necessary that the comparator be designed with a PMOS differential pair. When clock is logic high, outputs OUTP and OUTN are reset to logic high. When the clock signal is at low logic level, the differential input signal at inputs Vin and Vip charge the latch output node and the latch force one output to the high logic level and the other to the low logic level according to the differential input signal. The outputs OUTP and OUTN are directly connected to a NAND gate, thus forming the Valid signal. Therefore, when the clock is logic low, the Valid signal is set logic high and enables asynchronous control.

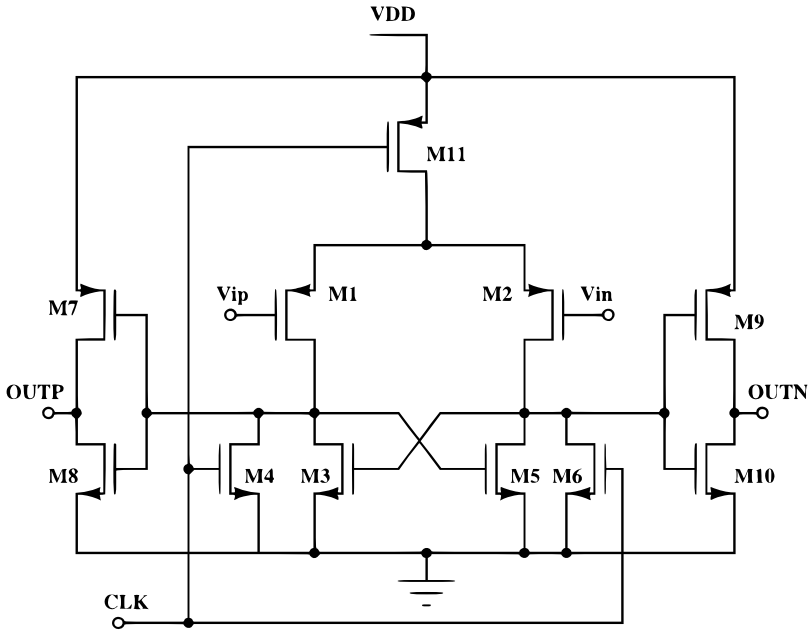


Figure 2.13: Dynamic comparator schematic

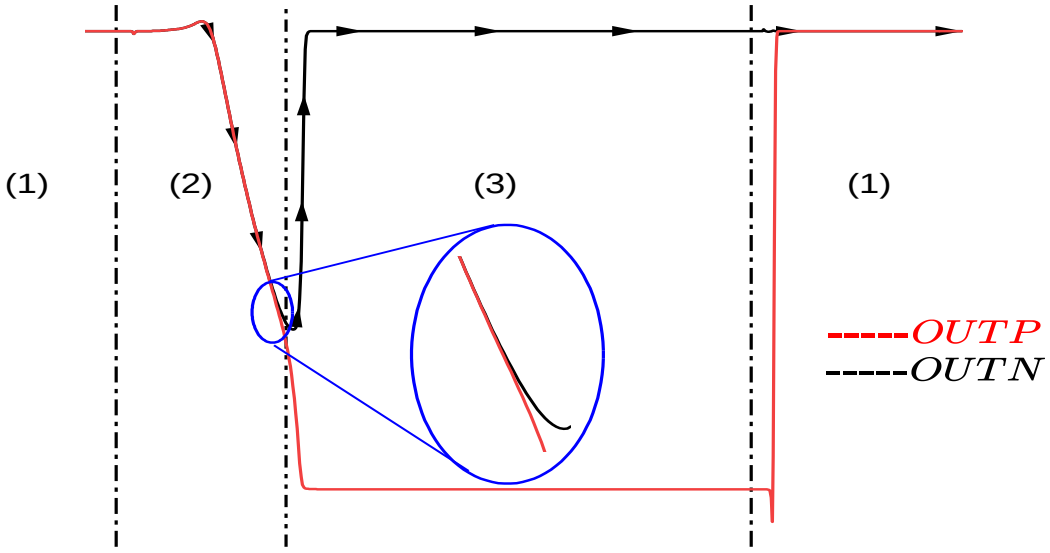


Figure 2.14: Phases of comparator operation

The working of comparator can be summarized in three phases. They are namely (1) Reset Phase, (2) Sensing or Amplification Phase, (3) Regeneration Phase.

**Reset Phase:** When the clock signal (CLK) is high, the comparator *resets* its outputs to a high state. This ensures a clean starting point for the subsequent sensing phase.

**Sensing (Amplification) Phase:** During this phase, the differential pair of transistors within the comparator amplifies the difference between the two input voltages ($V_{ip}$ and $V_{in}$). This amplification stage allows for easier detection of small voltage differentials.

**Regeneration Phase:** Once the sensing phase is complete, the cross-coupled NMOS transistor pair within the comparator utilizes positive feedback to pull the output nodes decisively to either a high or low state. This regeneration phase creates a clear and stable output voltage based on the amplified voltage difference from the sensing phase.

Dynamic comparators offer advantages like low power consumption, high speed, and high sensitivity over static comparators. However, they are not without limitations and suffer from several non-idealities that can impact their performance. These non-idealities include offset voltage, device noise, kickback noise, hysteresis, and metastability.

#### 2.1.3.1 Offset Voltage

This is a constant voltage difference present at the comparator's input even when the ideal input voltages are equal. There are mainly two types of offset voltages in the comparator: 1) offset voltage from the mismatch in transistor (static offset); 2) offset voltage from the mismatch in the parasitic capacitor loads (dynamic offset).

**Process Variation Offset**:- This offset arises from mismatches in transistor characteristics due to process variations during chip fabrication. These mismatches can include differences in transistor current gain factors ($\beta$) and threshold voltages ($V_{th}$). Increasing the transistor size is a well-known technique to mitigate this type of offset i.e. by improving the matching characteristics of the transistors.

**Parasitic Capacitance Mismatch Offset**:- This offset voltage stems from imbalances in parasitic capacitances associated with the comparator design. The load capacitor mismatch is a particularly critical contributor to this type of offset. Notably, studies have shown that a mere 1 fF imbalance in the output capacitance of a simplified latch model [11] (comprising a cross-coupled inverter pair) can lead to significant offset voltages in the range of tens of millivolts. This offset voltage is more affected by the relative capacitance mismatch ($\Delta C/C$) than the absolute difference $\Delta C$. At output nodes, additional capacitors with good matching properties can be added to reduce the relative mismatch. This comes with the added cost of area, speed, and power consumption.

#### 2.1.3.2 Device Noise

Thermal noise generated by the transistors and flicker noise inherent to semiconductor devices contribute to random fluctuations in the comparator's output. This noise can cause unwanted switching events or jitter in the output signal (Fig. 2.15). It primarily acts during sensing phase. Using larger transistors and proper layout techniques can help reduce noise.

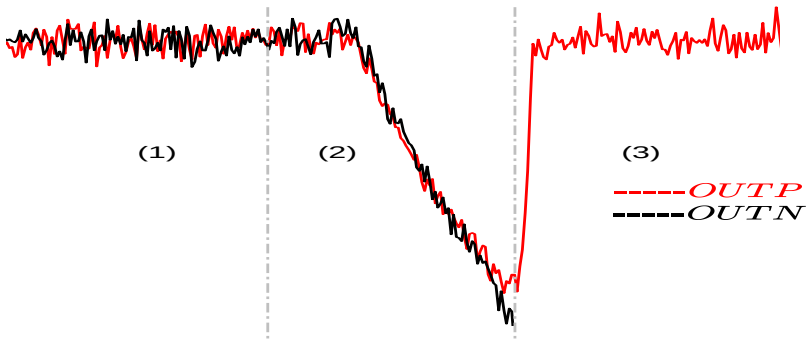


Figure 2.15: Effect of Noise on Comparator operation

#### 2.1.3.3 Kickback Noise

Kickback noise arises during the dynamic comparator's switching process ( i.e. when the comparator changes state to reset state). This switching event involves a rapid change in the internal voltage levels within the comparator. As a result, a transient current spike can be injected into the input nodes. This current spike, caused by the redistribution of channel charge within the transistors, creates temporary voltage fluctuations at the comparator's input. Mitigation techniques can be employed to minimize the impact of kickback noise in dynamic comparators. These techniques include utilizing a pre-amplifier stage before the main comparator to amplify the differential input voltage, reducing the relative impact of the transient current spike. Additionally, charge pump-based elimination techniques [12] can be implemented to actively cancel out the kickback noise current before it reaches the input nodes.

#### 2.1.3.4 Hysteresis

This refers to the non-zero difference between the rising and falling thresholds of the comparator's input voltage. In simpler terms, the voltage required to switch the comparator output high might be slightly different from the voltage needed to switch it low. Hysteresis can be beneficial in some applications to avoid noise-induced switching, but it can also introduce errors in critical timing circuits.

#### 2.1.3.5 Metastability

Metastability is the phenomenon where a latch (bistable element) requires an indeterminate amount of time to generate a valid output. The metastability in a dynamic latch comparator occurs when the differential input signal is so small that the latch does not have enough time to produce a well-defined logic levels, which might be interpreted differently by succeeding gates, leading to substantial conversion error.

### 2.1.4 SAR Control Logic

Conventional SAR ADCs often rely on synchronous control logic. This approach utilizes two distinct clock sources: a sample clock and a high-speed conversion clock. The synchronous control logic generates the necessary control signals based on these clock sources. However, this method suffers from a speed penalty. It allocates equal time slots for each conversion cycle, which is determined by the worst-case delay experienced by small differential signals. This one-size-fits-all approach can lead to wasted time in situations where the actual signal comparison is faster.

Asynchronous control logic offers a significant improvement in ADC speed. Unlike the synchronous approach, it generates the high-speed conversion clock dynamically based on feedback from the comparator. This feedback mechanism allows the conversion clock to adapt to the actual speed of the comparison process. As a result, asynchronous control logic eliminates the need for pre-defined time slots based on worst-case scenarios, leading to faster overall conversion times. Fig. 2.16 shows the schematic of asynchronous SAR control logic [3]. $Clks, ext$ is the external sample clock which acts as active high reset to control signals. $Clkc$ is comparator control clock (high speed converter clock), valid is the signal generated by nanding outputs of comparator.

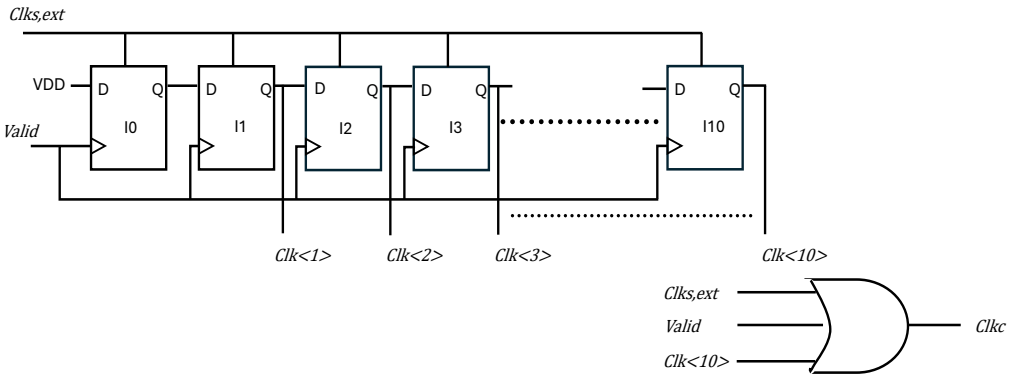


Figure 2.16: Asynchronous SAR Control Logic Schematic

Upon generation, the control signal initiates the conversion by instructing the dedicated DAC control logic (Fig. 2.18) to begin its switching operations. At the rising edge of $clk <$

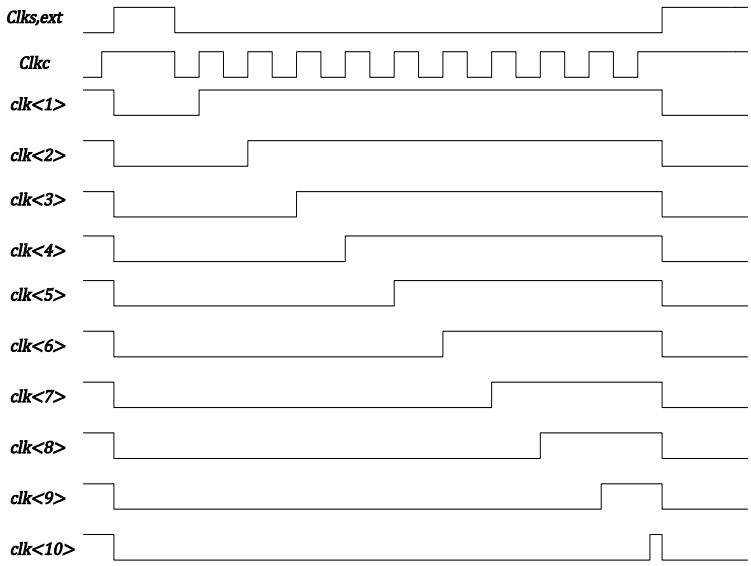


Figure 2.17: Asynchronous SAR Control Logic Timing Diagram

$i>$, D-flip-flop samples the comparator output. If the output is high, the relevant capacitor is switched from $V_{ref}$ to ground. If the output is low, the relevant capacitor is kept connected to $V_{ref}$. At the falling edge of $clk<i>$, all capacitors are reconnected to $V_{ref}$. The delay buffer guarantees that $clk<i>$ triggers the *AND* gate after the output of the D flip-flop.

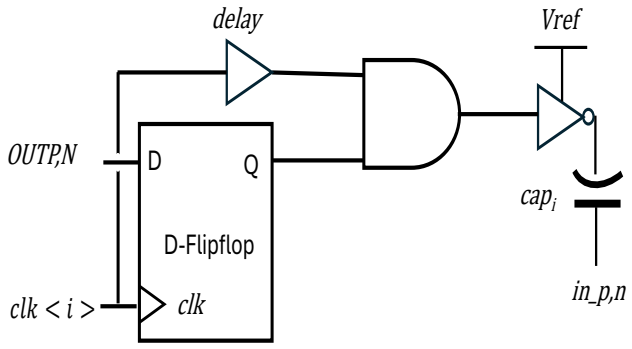


Figure 2.18: DAC Control logic

## 2.2 Summary

This chapter delved into the realm of Analog-to-Digital Converters (ADCs), with a particular focus on their energy efficiency. We began by surveying different ADC architectures and their efficiency trade-offs.

To gain a deeper understanding of a prominent architecture, the Successive Approximation Register (SAR) ADC, we examined its individual building blocks. The chapter explored the role of the Sample and Hold (S&H) circuit, highlighting its responsibility in capturing the analog input voltage and storing it on the top plate of the capacitive DAC.

Furthermore, we delved into a detailed analysis of the track bandwidth limitations, noise contributions, and other non-idealities associated with the switches used in the SAR ADC. Moving on to the Capacitive DAC subsection, the chapter provided a derivation-based approach to selecting the most suitable DAC architecture based on area efficiency. Additionally, potential switching procedures within the DAC were explored.

The chapter then shifted its focus to the dynamic comparator, a crucial element in the SAR ADC. We examined its operational principles and the various impairments that can affect its performance. Finally, the chapter concluded by exploring the concept of asynchronous control logic in the context of SAR ADCs.

# Chapter 3

# Design

## 3.1 Selection of Unit Capacitor

For our differential binary-weighted DAC topology, the expression for the mismatch-limited unit size capacitance can be written as,

$$C_{u,m} = 9 \cdot (2^N - 1) \cdot K_\sigma^2 \cdot K_C \tag{3.1}$$

In the TSMC 65LP technology node, two primary capacitor options are available: Metal-Insulator-Metal (MIM) and Metal-Oxide-Metal (MOM) capacitors. For this design, we opted to utilize MOM capacitors due to their favorable capacitance density. To optimize the MOM capacitor we performed 1000 Monte Carlo runs for capacitance with mismatch variations (using the following parameters NV=6, NH=6, w=0.1um, s=0.1um, bottom metal layer = 3, Top metal layer = 5, Area$\approx (1.1\mu m)^2$).

We found $\sigma_{u,r}$=0.32%, $K_C$=1.9fF/$\mu m^2$. Now $\sigma\left(\frac{\Delta C}{C}\right)$= $2 \times \sigma_{u,r}$= 0.65% (taken 2 times instead of $\sqrt{2}$). Therefore $K_\sigma$ = $0.65\% \times 1.1\mu m$ = $0.715\%\mu m$ .Substituting these values,

$$C_{u,m} = 9 \times (2^{10} - 1) \times 0.00715^2 \times 1.9fF = 0.894fF \tag{3.2}$$

From noise analysis (with $V_{i,range} = 0.8V$), we have

$$C_{u,n} = \frac{12K_BT}{2^N \times LSB^2} = 0.0795fF \tag{3.3}$$

The minimum unit MOM capacitance $C_{min}$ that can be fabricated in the TSMC 65LP node is 2.3fF. If we choose to use the binary weighted topology we need to pay extra power penality for the extra capacitance. Also if we try to use Split Capacitor based topology, main DAC size 'M' and the parasitics of sub DAC '$\alpha$' determine the unit capacitor size. We decided to use the ERMS DAC topology specified in [10], which is a binary weighted scheme where reference is reduced to C-2C dummy capacitor. It enables extra 1-bit resolution with same binary weighted structure. we choose to use mimimum capacitance $C_u = C_{min} = 2.3fF$ (with specifications NV=6, NH=6, w=0.1um, s=0.1um, bottom metal layer = 3, Top metal layer = 5) for ERMS DAC.

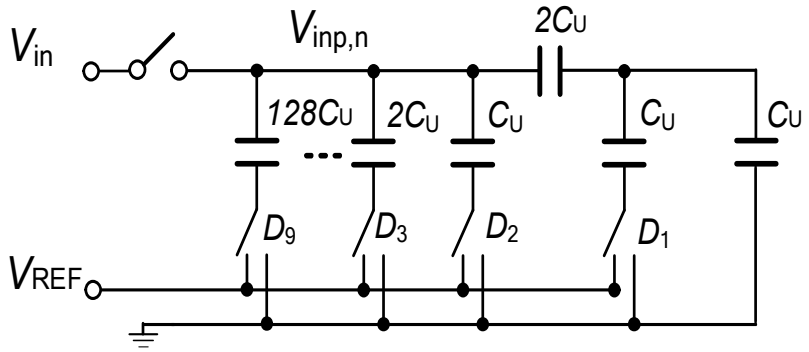


Figure 3.1: ERMS DAC

## 3.2 Design of Sample and Hold Circuit

For this design we choose $t_b$ for sampling to be equal to 15 % of sampling time($t_{sample}$=1$\mu$ sec). From previous section we found out $C_u$=2.3fF. Total capacitance on single DAC is 259 $\times C_u \approx$ 600fF. Substituting these values in Eq. (2.3),

$$t_b > R_{on} \cdot C_S \cdot ln2 \cdot (N+1) \tag{3.4}$$

$$R_{on} < \frac{t_b}{C_S \cdot ln2 \cdot (N+1)} \approx 32.8K\Omega \tag{3.5}$$

We chose bootstrapped switch implemented in [13] with following sizing (here CLK is Clks,ext and CLKB is its complement),

| **Component Parameters** | Width($\mu m$) | Length($\mu m$) |
|---|---|---|
| $M_{1-4}$ | 0.2 | 0.06 |
| MP5, MP6 | 0.2 | 0.06 |
| $M_7$ | 0.2 | 0.06 |
| $M_8 (R_{on} = 1.86K\Omega)$ | 0.8 | 0.06 |
| $M_{9-12}$ | 0.2 | 0.12 |
| MN6 | - | - |
| $C_1$,$C_2$ $(nmos - varactor)$ | 1 | 1 |

Table 3.1: Bootstrapped switch component sizes

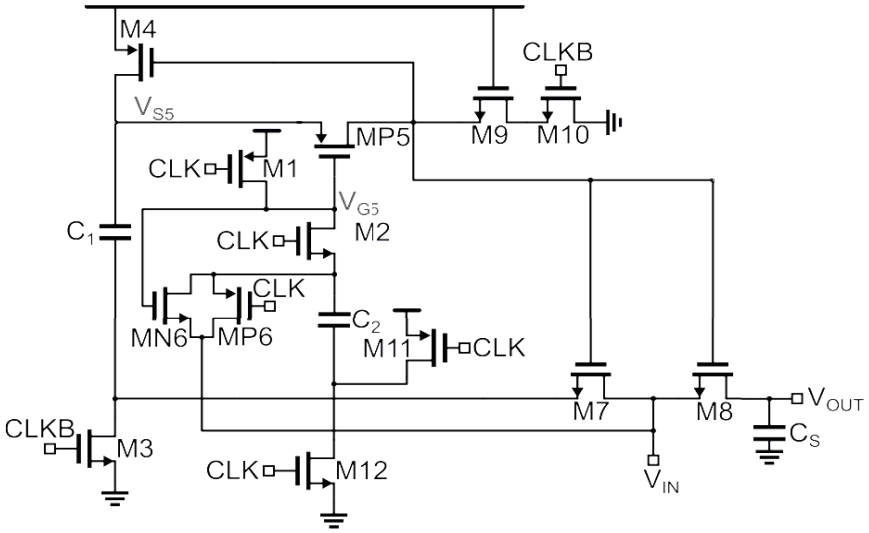


Figure 3.2: Bootstrapped switch Topology

## 3.3 Design of Comparator

The schematic for the dynamic comparator implemented is shown in Fig. 3.3. This topology was chosen as it has a better noise performance over a conventional strong arm latch. The size of the PMOS differential pair M3, M4 has a significant impact on controlling input referred noise and static offset. But increasing the size of M3,M4 indefinitely, causes power penality, since it increases node capacitances of X,Y. It also increases dynamic offset at lower common mode voltages.

The sizing of comparator components are presented in Table 3.2.

| **Component Parameters** | Width($\mu m$) | Length($\mu m$) |
|---|---|---|
| $M_1$ (low Vth) | 3.2u | 0.2 |
| $M_2$ | 0.4 | 0.2 |
| $M_{3,4}$ | 0.8 | 0.2 |
| $M_{5,6}$ | 0.4 | 0.2 |
| $M_{7,8}$ | 0.2 | 0.2 |
| $Inv_{1,2}$ (PMOS) high Vth | 0.36 | 0.06 |
| $Inv_{1,2}$ (NMOS) high Vth | 0.12 | 0.06 |

Table 3.2: Comparator component sizes

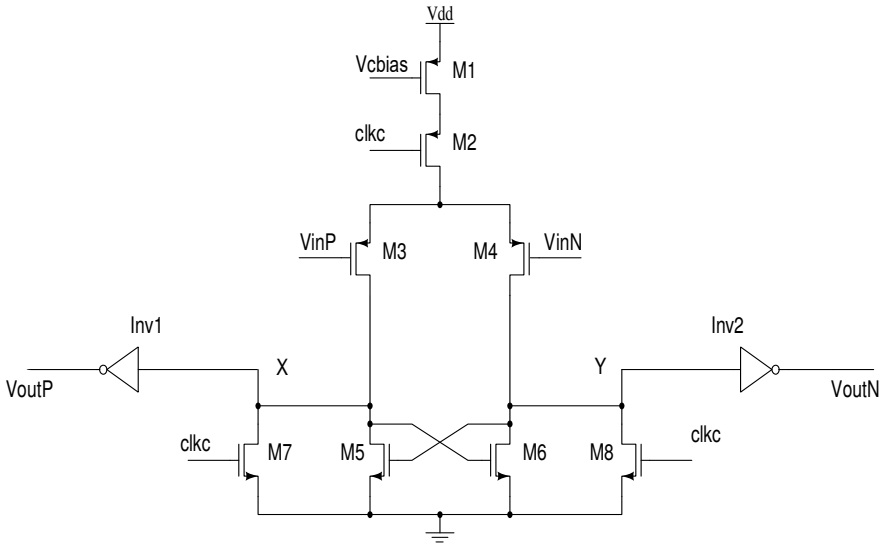


Figure 3.3: Dynamic Comparator with current source

Metastability can occur when the compared voltage difference is not sufficiently large enough to resolve the bit in designated time slot. The glitches in clkc will introduce this error. It can also occur when voltage across Top plate is not properly settled during conversion(DAC settling error). Following modification as shown in Fig. 3.4 is implemented to address this issue. Here multiplexer acts as breaking the feedback loop, when switch is sampling voltage onto top plate of capacitor array. During conversion loop is closed and delay block provides sufficient delay for settling of DAC. The implemented delay cell (CERO) is presented in [14], which has faster rise and fall times compared to traditional current starved inverter based delay cells. The comparator consumes a static current when the decision is completed as opposed to conventional strong arm latch. The delay from *valid* to *valid_delay* has to be the least possible delay at the rising edge of valid signal. Having lesser delay between rising edge of valid and rising edge of clkc helps in reducing the power consumption of the comparator.

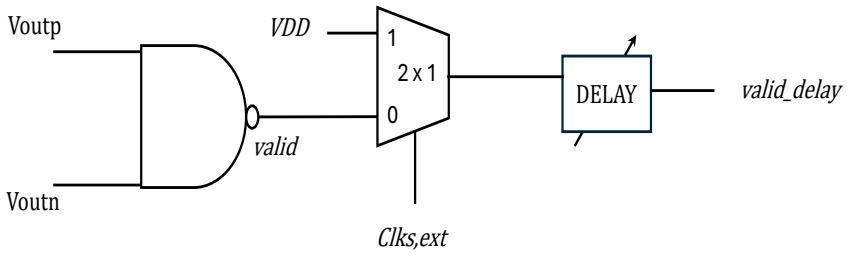


Figure 3.4: Modifications to address metastability during conversion

## 3.4 D-Flipflops and DAC switches

For the D-Flipflops, we chose transmission gate based flipflop (TG) for its reliability and simpler structure. All the gates of flipflops are implemented using high Vth MOS with minimum size width=0.12$\mu m$ and length= 0.06$\mu m$. All PMOS use stacking of 2 transistors with minimum size.

Unit inverter (DAC switches): PMOS: 480n/60n (standard Vth), NMOS: 480n/60n (standard Vth). These inverter units are scaled appropriately to obtain all of the switches.

# Chapter 4

# Simulation Results

Supply Voltage = 0.8V.

## 4.1 Comparator

Noise of the comparator has been simulated by pss/pnoise method. From the noise summary of cadence tool it was observed that flicker noise of the input differential pair and the regenerative pair are major noise contributors (they add upto 91% contribution).

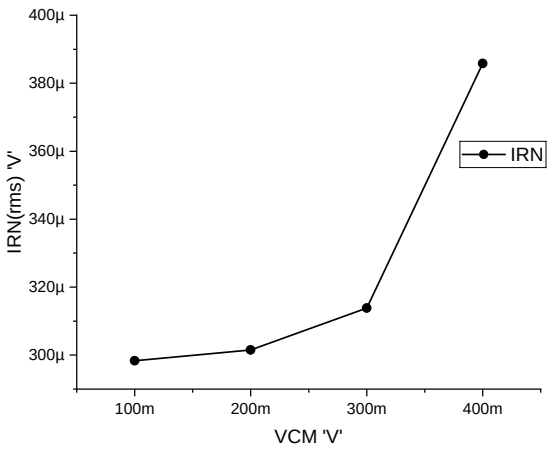


Figure 4.1: Comparator noise performance

The extraction of the offset stress values for both upward ($V_{R,offset}$) and downward ($V_{F,offset}$) directions was made from a Monte Carlo simulation with 200 runs (process and mismatch) by using the Smart-Resettable SAR method presented in [15]. The verilogA code for its implementation is reproduced in Appendix A. Testbench is shown in Fig. 4.2. The search range

is chosen to be -50mV to 50mV (differential ended input). The worst case offset values are observed (Table. 4.1) at lowest common mode voltage(VCM= 0V).

| Parameter | mean | $\sigma$ |
|---|---|---|
| $V_{F,offset}$ | 1.82 $mV$ | 5.62 $mV$ |
| $V_{R,offset}$ | 1.82 $mV$ | 5.62 $mV$ |

Table 4.1: Comparator input referred offset due to process and mismatch

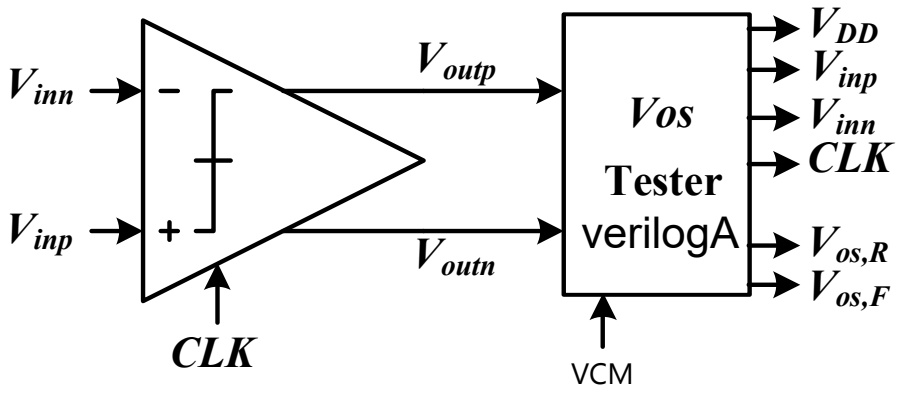


Figure 4.2: Offset Testbench schematic

## 4.2 SAR ADC Dynamic Performance

To evaluate the dynamic performance of the designed ADC, spectral test was conducted across all process corners. A sinusoidal input voltage with near full-scale output was applied. The input signal characteristics are as follows:

Amplitude: 350 mV (700 mV peak-to-peak differential amplitude)

Frequency: 147.5 kHz ( = $\frac{151}{1024} \times 1MHz$)

Common mode voltage: 400 mV

For obtaining spectra of digital output, transient noise analysis was performed. This analysis incorporates the noise characteristics of active devices within the design and setting the FMAX to 10 MHz (20 times the maximium signal bandwidth). The results obtained from all process corners are presented in Table 4.2, along with the processed output spectra (FFT with 1024 points) of the digital signal.

| **Parameter** | TT | FS | FF | SF | SS |
|---|---|---|---|---|---|
| Power ($\mu W$) | 1.374 | 1.207 | 1.11 | 1.34 | 1.404 |
| ENOB (bits) | 8.82 | 9.08 | 8.8 | 8.76 | 8.81 |
| SNR (dB) | 55.18 | 56.58 | 55.3 | 54.62 | 54.99 |
| SNDR (dB) | 54.88 | 56.44 | 54.73 | 54.54 | 54.794 |
| SFDR (dBc) | 66.76 | 69.47 | 65.7 | 65.9 | 66.13 |

Table 4.2: Dynamic performance results

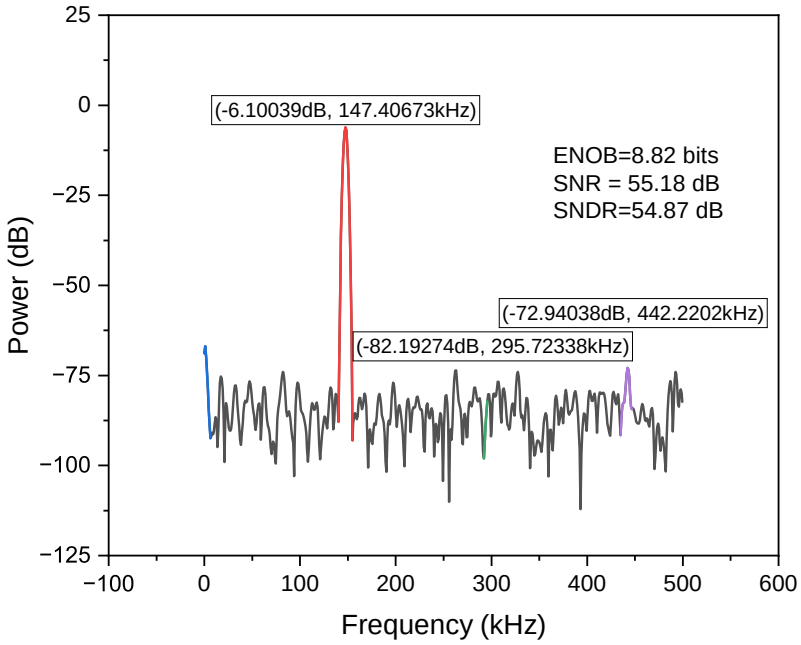


Figure 4.3: Output Spectra for TT corner

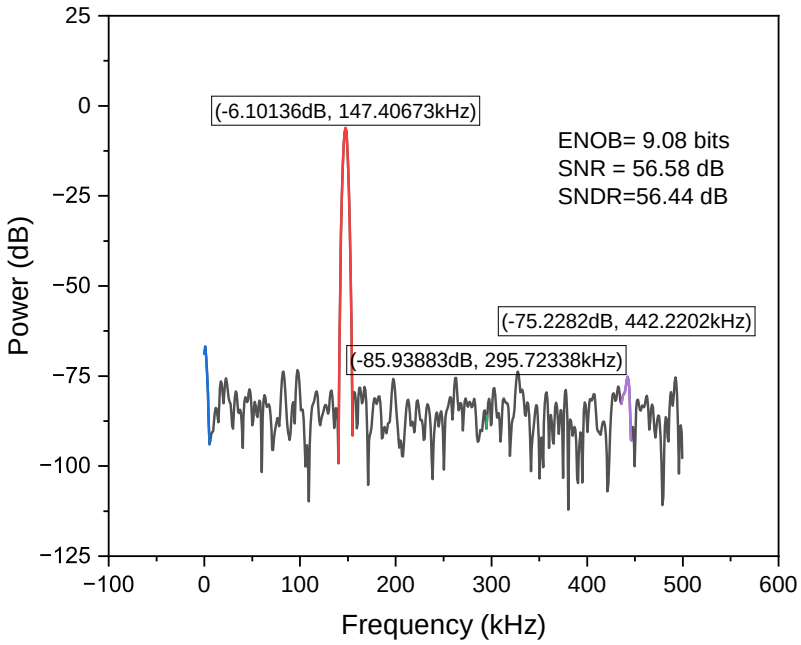


Figure 4.4: Output Spectra for FS corner

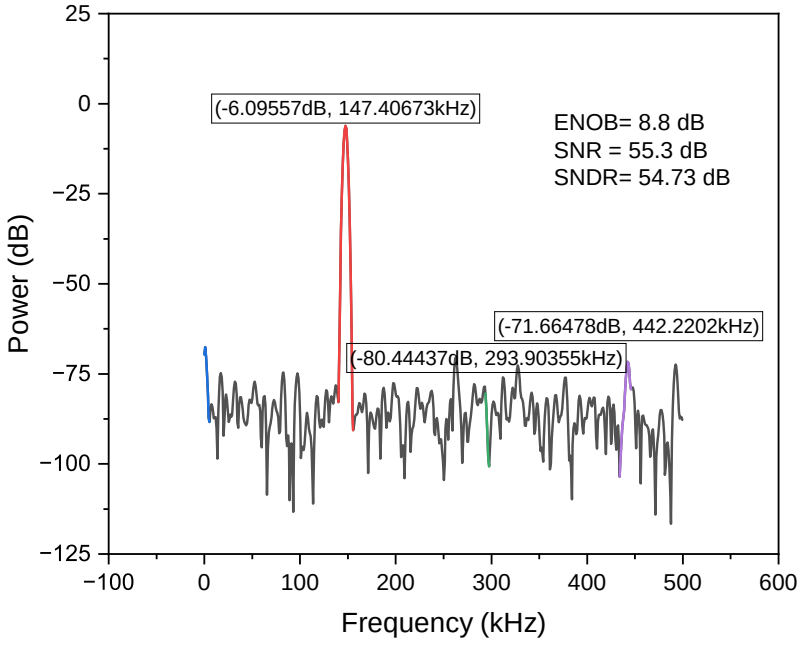


Figure 4.5: Output Spectra for FF corner

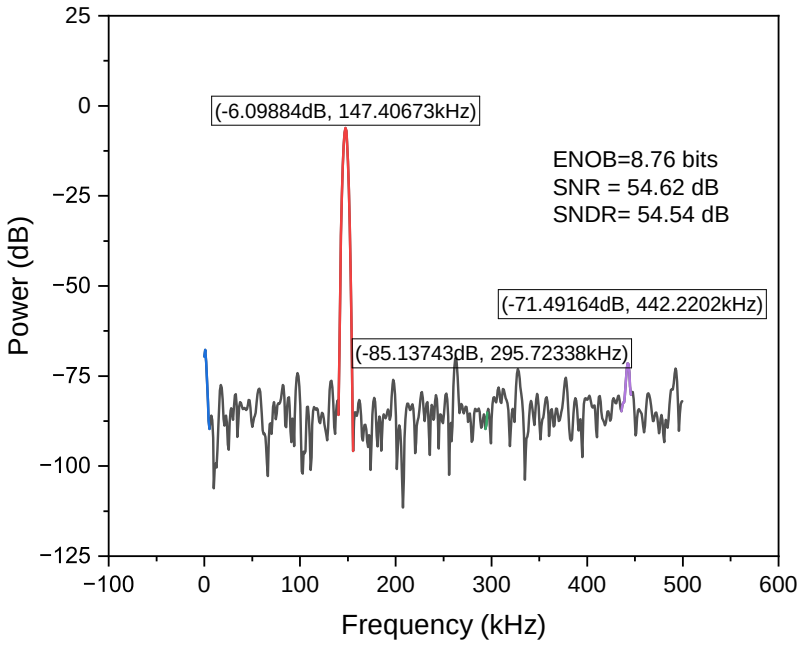


Figure 4.6: Output Spectra for SF corner

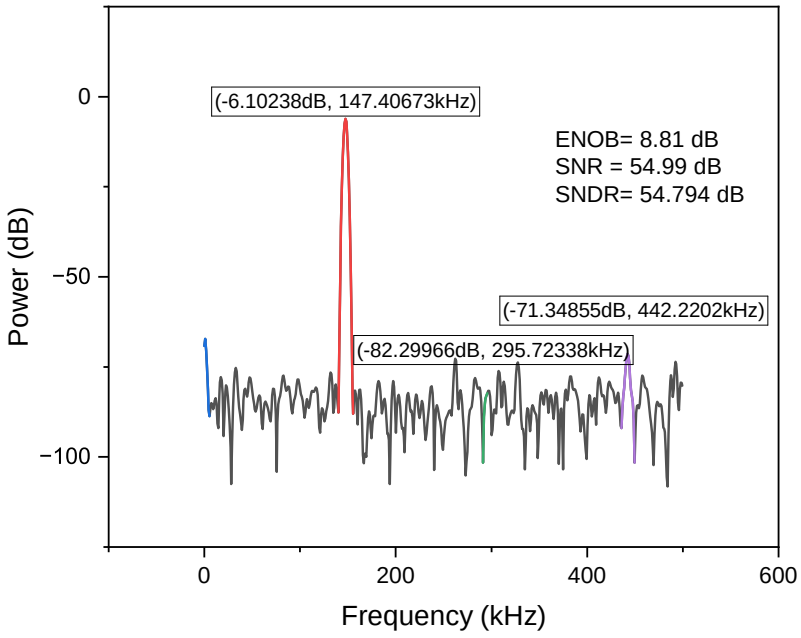


Figure 4.7: Output Spectra for SS corner

# Conclusion

The implemented design achieved an average power consumption of $1.28\mu W$. This project investigated the design and performance of a particular dynamic comparator. A key challenge identified was the high offset voltage, particularly at low common mode voltages. As referenced in [16], this offset degrades the SNDR by introducing distortion into the converted signal. To address this issue in future work, exploring offset calibration techniques is recommended.

From the dynamic performance of the implemented ADC, we identify noise as a key contributor to ENOB. One approach to enhance SNR could involve increasing the overall capacitance of the DAC and the size of the comparator itself. However, this strategy comes with trade-offs. Increased capacitance and comparator size can lead to higher power consumption and a larger chip area footprint. Future work should involve a more in-depth analysis of these trade-offs to determine the optimal configuration for specific application requirement.

# Appendix A

# VerilogA code for offset Tester Block

```
// VerilogA for VOS Tester

`include "constants.vams"
`include "disciplines.vams"

// code conventions:
// 1: positive/true/yes/rising/max/
// 0: negative/false/no/falling/min/
// UPPER_CASE: parameters {except VCMI - external common mode}
// lower_case: variables

module SRSAR (VCMI,VDDA, CLK, VINP, VINN,
VOUTP, VOUTN, VOS_R, VOS_F);

input VCMI,VOUTP, VOUTN;
output VDDA, CLK, VOS_R, VOS_F;

electrical VCMI,VDDA, CLK, VINP, VINN,
VOUTP, VOUTN, VOS_R, VOS_F;

// comparator supply voltage
parameter real VDD=0.8 from (0:100];

// comparator CM input (for diff input)
// or comparator DC VINN (for SE input)
real  VCM;

// comparator min diff input voltage
parameter real VIN_MIN=-50m from [-VDD:0];

// comparator max diff input voltage
```

```
parameter real VIN_MAX= 50m from [0:VDD];

// comparator high output voltage
parameter real VOUT_HIGH=VDD from [0:VDD];

// comparator low output voltage
parameter real VOUT_LOW=0 from [-VDD: VDD];

// is comparator input differential?
parameter integer DIFF_IN=0 from [0:1];

// is comparator output differential?
parameter integer DIFF_OUT = 1 from [0:1];
// clock period

parameter real TCLK = 100n from (0:1];
// rise time
parameter real TR=0.1n from [0:TCLK/2);
// fall time
parameter real TF=0.1n from [0: TCLK/2);
// clock active edge (1:rising, 0:falling)

// the active edge fires the comparison
// input is updated and output is checked
// just before the non-active edge

parameter integer CLK_EDGE = 1 from [0:1];
// no. of SAR bits
parameter integer NBIT=20 from [4:20];

// real variables by default init to zero
// current clock state (0 or 1)
integer clk_state;

// small delay to avoid race
real td = TCLK / 100;

// start in reset state
integer reset_state=1;


// comparator input is modeled as diff
// input direction (1:rising 0: falling)

integer vind_dir = 1;
// range of diff input
```

```
real vind_range;
// vind SAR value (ignores reset)
real vind_sar_val;

// vind value (SAR or reset value)
real vind_val;
// comparator positive input (active signal)

real vinp_val;
// comparator negative input (active signal
// for diff input and DC for SE input).

real vinn_val;
// comparator output threshold
real voutd_th;

// comparator output is modeled as diff
real voutd_val;
// detect low-to-high output transition
integer l2h_event = 0;

// detect high-to-ow output transition
integer h21_event = 0;

// counter used for SAR
integer count;
// measured Vos, rising

real vos_r_val;
// measured Vos,falling

real vos_f_val;

analog begin

V(VDDA) <+ VDD;
voutd_th=(DIFF_OUT == 1) ?  (VOUT_HIGH + VOUT_LOW)/2
            : (VOUT_HIGH + VOUT_LOW)/2;
// for SE output connect VOUTN to GND
voutd_val = V(VOUTP, VOUTN);

VCM = V(VCMI);


@(initial_step) begin
```

```
// init clock so 1st edge will be active
clk_state = (CLK_EDGE==1)?0:1;
vind_range = VIN_MAX - VIN_MIN;
count = 1;
vind_sar_val = VIN_MIN + vind_range/pow(2,count);
vind_val = VIN_MIN;
vinp_val = (DIFF_IN == 1) ? VCM + vind_val/2
                : VCM + vind_val;
    // Set positive comparator input based on differential mode
vinn_val = (DIFF_IN == 1) ? VCM - vind_val/2
                : VCM;
    // Set negative comparator input based on differential mode
end
// Trigger code block at half clock period
//(assumes 50% duty cycle)
@(timer (TCLK/2,TCLK/2)) begin
  clk_state = !clk_state; // Toggle clock state

  // Update vind and check voutd_val only on
  //non-active clock edge (to avoid glitches)
  if (clk_state != CLK_EDGE) begin
    if (reset_state == 1) begin // During reset state
      vind_val = vind_sar_val; // Apply next SAR value
      reset_state = 0;
end
       // Exit reset state
    else begin                  // During SAR conversion
      if (count == 0) $finish_current_analysis;
      // Terminate simulation
      else if (count < NBIT) begin
      // Continue SAR conversion
        count = count + 1;
      // Increment SAR counter
        if (voutd_val > voutd_th) begin
      // If comparator output exceeds threshold
vind_sar_val = vind_sar_val - vind_range/pow(2,count);
// is vind in the rising test?
    if (vind_dir == +1)
// reset to VIN_MIN before
// jumping down to avoid hys
reset_state = 1;

        end         // vind should jump up

   else begin
                vind_sar_val = vind_sar_val +
```

```
                vind_range/pow(2,count);

                // is vind in the falling test?
                if (vind_dir == 0)

                // reset to VIN_MAX before
                // jumping up to avoid hys
                reset_state = 1;
   end
end

// end of SAR for rising/falling test
      else if (count == NBIT) begin

// retain or remove SAR LSB
        if (voutd_val > voutd_th)

             vind_sar_val= vind_sar_val-
             vind_range/pow(2,count);
        if (vind_dir == +1) begin

             vos_r_val = vind_sar_val;
              // switch from rising to falling
             vind_dir = 0;
             // reset count
             count = 1;
             // init SAR value
             vind_sar_val = VIN_MIN +
             vind_range/pow(2,count);
            // init reset value
             vind_val= VIN_MAX;
            // go to reset state
             reset_state =1;
        end
        else if (vind_dir == 0) begin
             vos_f_val = vind_sar_val;
            // resetting count is the done flag
             count = 0;

        end
     end
     if (reset_state ==  1)
            // reset state: assign reset value
        vind_val = (vind_dir == 1) ? VIN_MIN: VIN_MAX;

    else
```

```
            / SAR state: assign vind SAR value
        vind_val= vind_sar_val;

     end
  end
     vinp_val = (DIFF_IN == 1) ? VCM + vind_val/2
     : VCM + vind_val;
     vinn_val = (DIFF_IN == 1) ? VCM - vind_val/2
     : VCM;

end


V(CLK) <+ transition( clk_state*VDD, td , TR , TF ) ;
V(VINP) <+ transition( vinp_val , td , TR , TF );
V(VINN) <+ transition( vinn_val , td , TR , TF );
V(VOS_R) <+ vos_r_val ;
V(VOS_F) <+ vos_f_val ;
end
endmodule
```

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