bit resolution can be achieved at somewhat lower yield. It is believed by the authors that more careful control of photolithographic processing would result in very high yield at the 10-bit level and significant yield at even higher resolutions.

ACKNOWLEDGMENT

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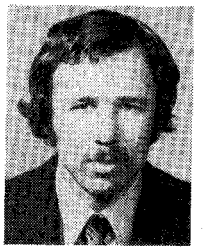

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All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques—Part II

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Abstract—**This two-part paper describes two different techniques for performing analog-to-digital (A/D) conversion compatibly with standard single-channel MOS technology. In the first paper, the use of a binary weighted capacitor array to perform a high-speed successive approximation conversion was discussed.**

This second paper describes a two-capacitor successive approximation technique, which, in contrast to the first, requires considerably less die area, is inherently monotonic in the presence of capacitor ratio errors, and which operates at somewhat lower conversion rate. Factors affecting accuracy and conversion rate are considered analytically. Experimental results from a monolithic prototype are presented; a resolution of eight bits was achieved with an A/D conversion time of 100 μs. Used as a digital-to-analog (D/A) converter, a settling time of 13.5 μs was achieved. The estimated total die size for a completely monolithic version including logic is 5000 mil^2.

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I. INTRODUCTION

AS DISCUSSED in Part I [9] of this paper, widespread application of techniques for digital processing of analog signals has been hindered by the unavailability of inexpensive functional blocks for analog-to-digital (A/D) conversion. Traditional approaches to A/D conversion have required the simultaneous implementation of high-performance analog circuits, such as operational amplifiers, and of digital circuitry

for counting, control, and data storage. Consequently, current A/D converter realizations have tended to be multiple-chip approaches [1] wherein the advantages offered by bipolar and MOS fabrication technologies are separately exploited.

In contrast, the charge-redistribution A/D conversion technique to be described in this paper requires a minimum number of precision components and is realizable on a single low-cost MOS chip.[1] Compared with the weighted capacitor technique described in Part I [9], the technique requires only two equal grounded capacitors of moderate value [11]. As a result, it can be realized in a relatively small die area compared with the weighted capacitor approach. On the other hand, ultimate resolution of this technique is sensitive to parasitic capacitances associated with the switch transistors, and the conversion rate is lower for a given clock rate because of the conversion algorithm required. The technique is thus most suitable when moderate conversion rate and moderate resolution are required in a small die area.

II. Serial D/A Converter

A simplified schematic diagram of a serial digital-to-analog (D/A) converter (DAC) circuit is shown in Fig. 1. Capacitors C_1 and C_2 are nominally of equal value. Conversion is accomplished serially by considering the least significant bit (LSB) d_1 first. Capacitor C_1 is precharged either to the reference voltage V_R by a momentary closure of S_2 if $d_1 = 1$ or to ground through S_3 if $d_1 = 0$. Simultaneously, C_2 is discharged to ground through S_4. With S_2, S_3, and S_4 open switch S_1 is then closed momentarily to redistribute the charge, and the resulting capacitor voltages are

$$V_1(1) = V_2(1) = \frac{d_1}{2} V_R . \tag{1a}$$

Holding the charge on C_2, the precharging of C_1 is repeated, this time considering the next least significant bit d_2. After redistribution the capacitor voltages are

$$V_1(2) = V_2(2) = \frac{1}{2}\left(d_2 + \frac{d_1}{2}\right) V_R . \tag{1b}$$

The process continues in this fashion, and at the end of K redistributions the existing charge on C_2 is divided by two and a charge increment corresponding to

$$\frac{d_K}{2} V_R \tag{1c}$$

is added. Therefore, for a K-bit D/A conversion the voltage on the capacitor is

$$V_1(K) = V_2(K) = \sum_{i=1}^{K} \frac{2^i d_i}{2^{K+1}} V_R \tag{1d}$$

which is the desired output. A total of K precharge steps and K redistributions are required to complete a K-bit D/A conversion. The conversion sequence for the input word 1101 is illustrated in Fig. 2.

[1] Patent pending.

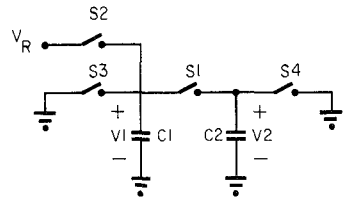

Fig. 1. Serial charge–redistribution digital-to-analog (D/A) converter.

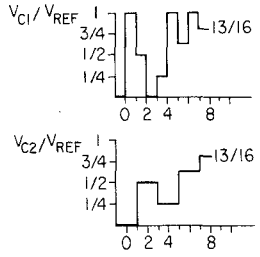

Fig. 2. Illustration of D/A conversion sequence for the input word 1101.

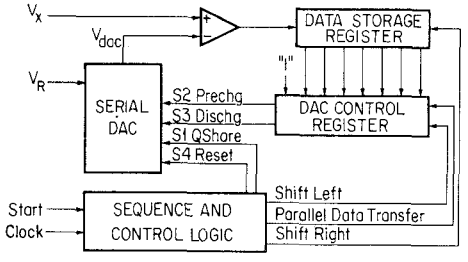

Fig. 3. Complete analog-to-digital (A/D) converter.

III. Successive Approximation A/D Converter

With the addition of a voltage comparator, storage registers, and sequencing logic the serial DAC can be used to construct a successive approximation A/D converter (ADC), as shown in Fig. 3. For an A/D conversion, the most significant bit (MSB) a_N must be determined first.[2] The control logic then takes on a particularly simple form since the DAC input string at any given point in the conversion is just the previously encoded word taken LSB first. For example, consider a point during the A/D conversion in which the first K MSB's have been decided. To decide the $(K+1)$th MSB, a $(K+1)$-bit word is formed in the DAC Control Register by adding a "1" as the LSB to the K-bit word already encoded in the Data Storage Regsiter. A $(K+1)$-bit D/A conversion then establishes the value of a_{N-K} by comparison with the unknown voltage V_X. The bit is stored in the Data Storage Register and the next serial D/A conversion is started. The conversion sequence is detailed in Table I, and Fig. 4 illustrates a 4-bit A/D conversion

[2] The jth bit is denoted d_j in a D/A conversion and a_j in an A/D conversion.

TABLE I
SUCCESSIVE APPROXIMATION A/D CONVERSION SEQUENCE

D/A Conversion Number	DAC Input Word						Comparator Output	No. of Charging Steps
	d_1	d_2	d_3	...	d_{N-1}	d_N		
1	1	--	--	...	--	--	a_N	2
2	1	a_N	--	...	--	--	a_{N-1}	4
3	1	a_{N-1}	a_N	...	--	--	a_{N-2}	6
...	...	...	...	...	...	...	...	...
N	1	a_2	a_3	...	a_{N-1}	a_N	a_1	2N
							TOTAL..	N(N+1)

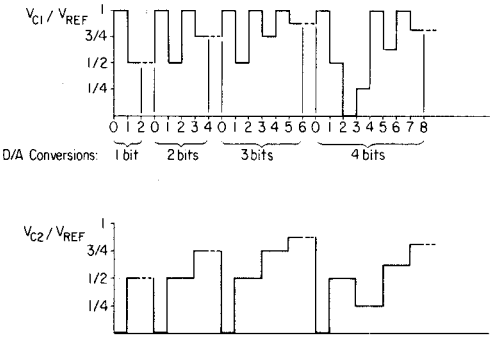

Fig. 4. Illustration of A/D conversion sequence for V_X/V_R = 13/16.

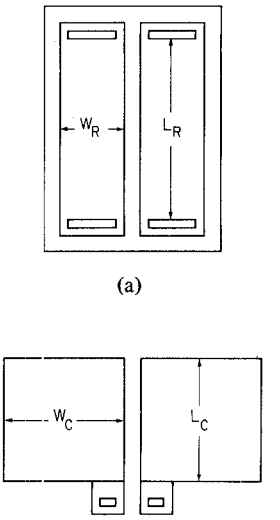

Fig. 5. Surface geometries for integrated passive components. (a) Resistor pair. (b) Capacitor pair.

TABLE II
CHARACTERISTICS OF INTEGRATED RESISTORS AND CAPACITORS

Component	Fabrication technique	Standard Deviation Matching	Derived σ_X (μm)	Temperature Coefficient (ppm/°C)	Voltage Coefficient (ppm/V)
Resistors	Diffused (W=40 μm)	$\pm$ 0.23% [2]	0.1	+1500 [2]	-200 *
	Ion-implanted (W=40 μm)	$\pm$ 0.12% [2]	0.05	+400 [2]	-800 **
Capacitors	MOS (t_{OX}=0.1 μm L= 10 mils N^+ substrate)	$\pm$ 0.06% ***	0.1	26	-10

for V_X = 13/16 V_R. Altogether $N(N+1)$ charging steps are required for an N-bit A/D conversion. The total A/D conversion time also includes N comparator settling times.

IV. ACCURACY CONSIDERATIONS IN MONOLITHIC PASSIVE COMPONENTS

In a successive approximation ADC it is necessary to generate accurate fractions of the reference voltage to establish the value of the bits $a_1, \cdots, a_N$. These fractions are obtained in an integrated circuit with resistor or capacitor dividers or by scaling of active device geometries. The relatively poor matching of active device characteristics, however, makes it difficult to achieve accurate voltage or current ratios over a wide range of values and operating conditions. For this reason voltage or current ratios are normally defined through fractions of passive components.

A major source of component mismatches in integrated circuits are uncertainties in photolithographic edge definition. For a pair of nominally identical resistors, as shown in Fig. 5(a), an edge uncertainty in the resistor length (ΔL) and width (ΔW) results in a mismatch

$$\frac{\Delta R}{R} = \frac{\Delta L}{L_R} - \frac{\Delta W}{W_R}. \tag{2}$$

The limited range of sheet resistances available in integrated resistors usually demands fairly large length-to-width (L/W) ratios. Hence

$$\frac{\Delta R}{R} \cong -\frac{\Delta W}{W_R}. \tag{3}$$

For a pair of nominally identical capacitors, as shown in Fig. 5(b), the mismatch due to edge uncertainties is

$$\frac{\Delta C}{C} = \frac{\Delta L}{L_C} + \frac{\Delta W}{W_C}. \tag{4}$$

Since the capacitance value is determined by the capacitor area (as opposed to L/W ratio for resistors) the freedom exists to optimize capacitor geometries to reduce the mismatch sensitivity to uncertainties in edge definition. Thus for a given area it is possible to have $L_C \simeq W_C > W_R$. Hence

$$\frac{\Delta C}{C} < \frac{\Delta R}{R}. \tag{5}$$

One further consideration with regard to mismatch error is the effect of oxide thickness gradients for large capacitor areas. As discussed in Part I [9], layout of the capacitors about a common centroid minimizes the effect of long-range gradients in oxide thickness.

Table II lists published matching data on integrated resistors [2] and measured data on MOS capacitors. The data suggest a standard deviation edge uncertainty of approximately 0.1 μm. Also listed in the table are voltage and temperature coef-

ficients on these components. The data indicate that in all of these aspects MOS capacitors over highly doped silicon offer an attractive alternative for the generation of accurate voltage ratios for monolithic A/D conversion.

V. Factors Limiting Linearity and Offset

In a practical implementation of the D/A converter presented in Section II the output voltage will have the form:

$$V'(K) = V(K) + V'_\epsilon \tag{6}$$

where $V(K)$ is the ideal voltage level given in (1d), and V'_ϵ is an error voltage. The primary sources of error are: feedthrough voltages ($V_{f\epsilon}$), capacitor mismatches ($V_{m\epsilon}$), voltage and temperature coefficients of capacitance ($V_{V\epsilon}$ and $V_{T\epsilon}$), and leakage currents ($V_{L\epsilon}$).

For an A/D converter, the input offset of the voltage comparator (V_{OS}) contributes an additional error component. The total error voltage for an ADC can be expressed as a sum:

$$V_\epsilon = V_{f\epsilon} + V_{m\epsilon} + V_{V\epsilon} + V_{T\epsilon} + V_{L\epsilon} + V_{OS}. \tag{7}$$

In order to keep the worst case conversion error below the converter resolution the following condition must be maintained:

$$\max |V_\epsilon| < \frac{V_R}{2^{N+1}} \tag{8}$$

for N bits.

A. Mismatches

For a mismatch ΔC between capacitors C_1 and C_2

$$\Delta C \equiv C_2 - C_1 \tag{9a}$$

and letting

$$C \equiv (C_1 + C_2)/2 \tag{9b}$$

an analysis of the precharge and charge redistribution sequence outlined in (1) indicates an error voltage

$$V_{m\epsilon} = \frac{\Delta C}{4C} \sum_{i=1}^{N} \frac{N - i - 1}{2^N} 2^i d_i V_R. \tag{10}$$

The worst cases occur when $d_N = 1$ and $d_i = 0$ for $i \neq N$ or vice versa. At these points, the mismatch error voltage is

$$V_{m\epsilon} \simeq \pm \frac{\Delta C}{4C} V_R \tag{11}$$

and at the $(01 \cdots 1)$ to $(10 \cdots 0)$ transition a discontinuity occurs with magnitude

$$\frac{\Delta V_{m\epsilon}}{V_R} \simeq \frac{\Delta C}{2C}. \tag{12}$$

An extrapolation of the data in Table II indicates that a capacitance value of 25 pF for C_1 and C_2 is adequate for an 8-bit converter.

B. Feedthrough

The asymmetry introduced into the circuit by the nonlinear capacitances associated with the charge-sharing MOS transistor switch results in a net feedthrough error voltage during redistribution. With respect to the circuit in Fig. 6, after application of a pulse to the gate of the transistor the resulting capacitor voltages are

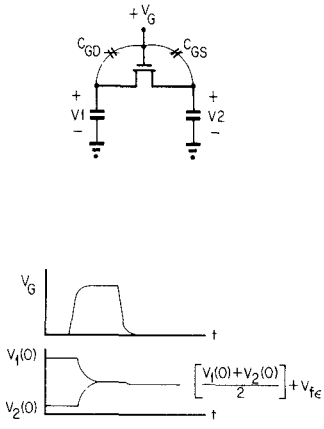

Fig. 6. Feedthrough error voltage during charge redistribution.

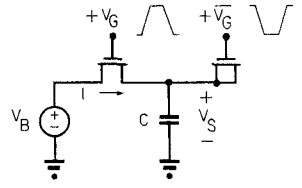

Fig. 7. Charge-canceling device for feedthrough compensation.

$$V_1 = V_2 = \frac{V_1(0) + V_2(0)}{2} + V_{f\epsilon 1}. \tag{13}$$

The feedthrough error voltage can be reduced by reading the capacitor voltages only after the gate voltage has been returned to zero. In this manner, the negative falltime feedthrough partially cancels the positive risetime feedthrough, but an exact cancellation is not achieved. The magnitude of this error component is proportional to the channel capacitance of the MOS transistor C_0 and inversely proportional to the sum of the charge-sharing capacitors

$$V_{f\epsilon 1} \propto \frac{C_0}{(C_1 + C_2)}. \tag{14}$$

An additional feedthrough error component is caused by the precharge transistors. After a capacitor has been charged to V_R or to ground, a negative feedthrough error voltage is introduced during the falltime of the gate voltage. In this case, the addition of a "charge-canceling" device [3], as shown in Fig. 7, reduces the net precharge feedthrough error voltage to approximately the same level as the feedthrough error voltage during charge redistribution. The charge-canceling transistor is a dummy device with the drain and source short-circuited to prevent dc current flow and with one-half the channel area of the precharge devices. The voltage applied at the gate of the charge-canceling device is the complement of the precharge transistor voltage. Since charge-redistribution divides the voltage equally between the two capacitors, the cumulative feed-

through error voltage is halved after each redistribution. Thus the maximum total feedthrough error voltage is approximately twice the worst case value of V_{fe}. In view of (14), therefore, the allowable error constrains the size of the MOS transistor switches in relation to the charge-sharing capacitors. This restriction, in turn, limits the magnitude of the charging currents and thus determines conversion speed. For $C_1 = C_2 = 25$ pF and a channel length $L = 7$ μm, a device W/L ratio of 10 produces a worst case cumulative feedthrough error voltage under 10 mV, for $V_R = 5$ V and gate voltages of 10 V. The charging time under these conditions is approximately 800 ns. These parameters are in agreement with simulations using the program ISPICE [4].

C. Capacitor Voltage and Temperature Variations

To characterize the error voltage due to capacitor nonlinearities, let

$$\alpha = \gamma_V^C = \frac{1}{C}\frac{\partial C}{\partial V}$$

where γ_V^C is the effective voltage coefficient of the MOS capacitors. The charge-sharing capacitors then have the form:

$$C_1 = C(1 + \alpha V_1) \tag{15a}$$

and

$$C_2 = C(1 + \alpha V_2). \tag{15b}$$

Here it is assumed that the nonlinearity is small enough that the higher order terms in $C(V)$ can be neglected. After precharging the capacitors to $V_1(0)$ and $V_2(0)$ and charge redistribution to a final voltage $V(f)$, we have:

$$V(f)\,2C\,\{1 + \alpha V(f)\} = C\,\{V_1(0) + V_2(0) + \alpha V_1^{\,2}(0) + \alpha V_2^{\,2}(0)\}. \tag{16}$$

Solving for $V(f)$ in the worst case, when $V_1(0) = V_R$ and $V_2(0) = 0$, then

$$V(f) \cong \frac{V_1(0) + V_2(0)}{2} + \frac{\alpha}{4} V_R. \tag{17}$$

Hence

$$V_{Ve} \cong \frac{1}{4}\gamma_V^C V_R. \tag{18}$$

Consideration of the data listed in Table II indicates that for a heavily doped ($5 \times 10^{20}\,\mathrm{cm}^{-3}$) lower capacitor plate the resulting error voltage due to capacitor nonlinearities is negligible. Moreover, since γ_T^C is also very small, temperature gradients of several degrees have a minimal effect on the capacitor voltages after redistribution.

D. Leakage Currents

With respect to conversion errors caused by leakage currents, a calculation for $C_1 = C_2 = 25$ pF indicates that 10 nA of leakage current will produce a voltage loss of 10 mV over 24 μs. Since room-temperature leakage currents in the order of 10 pA/mil^2 are typical in MOS circuits this source of error is also negligible and will allow operation at temperatures up to at least 100°C.

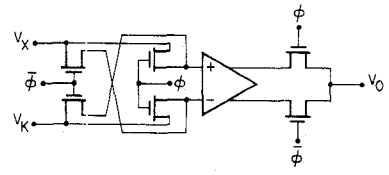

Fig. 8. Circuit for offset cancellation by subtraction.

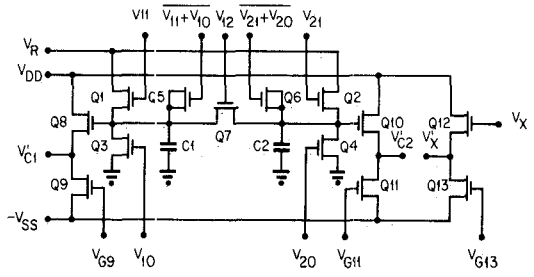

Fig. 9. Circuit schematic of monolithic DAC.

E. Offset Voltage

MOS transistor differential pairs exhibit substantial input offset voltages, typically in the order of 100 mV [5]. Several offset compensation schemes have been proposed [6], [7]. The problem of cancellation of offset voltage in MOS comparators was discussed in Part I of this paper [9], and by other authors. These techniques involve storage of the offset voltage of the comparator as a whole or the individual stages thereof on capacitors during a sample period prior to the conversion itself. As discussed in Part I, effective input offset voltages of less than 5 mV are readily achieved experimentally with this technique.

An alternative approach which is readily implementable in an MOS integrated circuit is illustrated in Fig. 8. Two conversion sequences are required to cancel the offset voltage. During the first A/D conversion pulse Φ is high and an offset voltage V_{OS} is encoded with the voltage difference $V_X - V'(K)$. On the second A/D conversion Φ is low, the input terminals of the comparator are inverted, and the comparator output is taken from the complementary output terminal. The encoded bits now include a contribution of $-V_{OS}$ to the difference $V_X - V'(X)$. The two binary words are added and divided by 2 to null out the offset voltage. Although this approach requires twice the conversion time, it can be used to cancel simultaneously the effect of capacitor mismatches. The mismatch error can be compensated by precharging all bits onto capacitor C_1 on the first conversion, and onto C_2 on the second conversion. The resulting mismatch errors are equal in magnitude and opposite in sign. The subsequent addition and division by 2 therefore also cancels the mismatch error component.

VI. Experimental Results

To verify experimentally the feasibility of the conversion technique, the two-capacitor DAC was fabricated by a five-mask n-channel aluminum-gate process. Fig. 9 is a schematic diagram of the D/A converter circuit, and Fig. 10 is a photo-

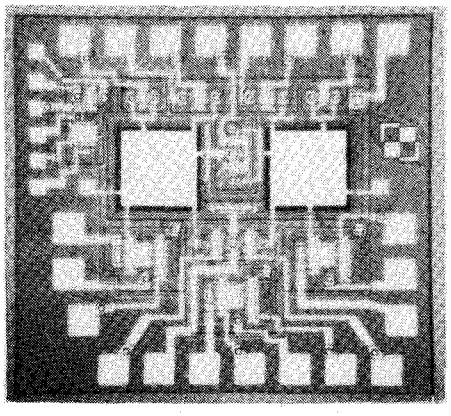

Fig. 10. Photomicrograph of experimental DAC.

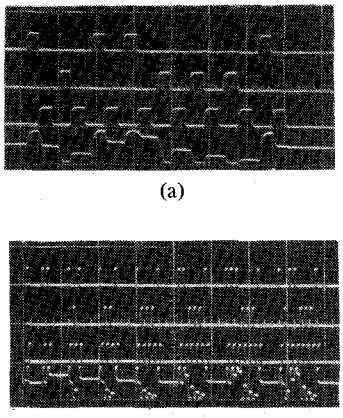

Fig. 11. Oscilloscope photographs of conversion sequence. (a) D/A conversion input word 10001101. Top to bottom: V_{11}, V_{10}, V_{12}, V'_{C1}. Vertical: 20 V/div (except V'_{C1}, 5 V/div). Horizontal: 2 μs/div. (b) A/D conversion output word 10001101. Top to bottom: V_{11}, V_{10}, V_{12}, V'_{C1}. Vertical: 20 V/div (except V'_{C1}, 5 V/div). Horizontal: uncalibrated (8 div $\simeq$ 100 μs).

micrograph of the 8-bit experimental die. The total chip size is 48 X 52 mil^2.

All transistors were designed with a nominal channel length $L = 7$ μm and an oxide thickness of 1000 Å. The switch devices, $Q1$–$Q4$ and $Q7$, were assigned a $W/L = 10$ based on feedthrough error considerations. The charge-canceling devices $Q5$ and $Q6$ have $W/L = 5$. The source followers $Q8$–$Q11$ are output buffers for the capacitor voltages. Source follower $Q12$–$Q13$ are included to level shift the voltage V_X to the same level as the DAC output voltage. The pull-down devices $Q9$, $Q11$, and $Q13$ have $W/L = 10$ and are biased in saturation. A quiescent current of 200 μA flows through these devices to drive a 10-pF load capacitance. The pull-up transistors $Q8$, $Q10$, and $Q12$ have $W/L = 15$. No offset-cancellation circuitry was included on the chip. The gate terminals of the pull-down transistors are taken off-chip to permit offset nulling. The feasibility of offset cancellation has been verified separately as discussed in Part I [9]. The integrated DAC was tested in a successive approximation ADC test circuit following the configuration shown in Fig. 3. Approximately 40 bits of shift register plus decoding gates were implemented with TTL logic. A bipolar integrated circuit was used for the voltage comparator.

The oscilloscope photographs in Fig. 11(a) and (b) correspond to an 8-bit D/A and A/D conversion, respectively. The control waveforms include a 5-μs time interval after each D/A conversion to take into account the estimated settling time of an MOS differential voltage comparator. The settling time estimate is based on computer simulation of a cascade of three differential pairs, each with a voltage gain of 10. The D/A conversion time for 8 bits is 13.5 μs and the total A/D conversion time is 100 μs. The A/D conversion time is the sum of a 1-bit D/A time, 2-bit, etc., up to 8 bits, plus assorted comparator and logic delays.

Fig. 12 includes a plot of the error voltage for an 8-bit ADC versus input voltage. The error has been defined as the difference in the measured transition points from the ideal staircase transfer function to eliminate the inherent quantization distortion from the error description. The maximum error is 9 mV which is less than $\frac{1}{2}$ LSB for a reference voltage of 5.120 V.[3]

[3]This voltage level was chosen for convenience to make 1 LSB = 20 mV.

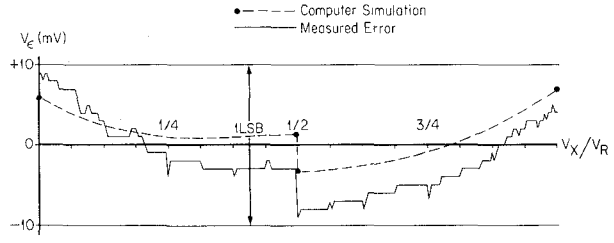

Fig. 12. Error voltage versus input voltage for the A/D converter.

The general features of this error curve can be explained in terms of the error components also shown in Fig. 12. A masking misalignment on the chip was observed which reduced the gate-source overlap capacitance of transistors $Q1$ and $Q2$ by approximately 15 percent. Since the capacitance components of the charge-canceling devices $Q5$ and $Q6$ are unchanged, this misalignment results in a net positive error voltage on $C1$ and $C2$ when the most significant bits are "1." The masking misalignment also causes a reduction in the gate-drain overlap capacitance of $Q3$ and an increase in the gate-drain overlap capacitance of $Q4$. The change in the capacitances of $Q3$ and $Q4$ causes a net positive error voltage on $C1$ and $C2$ when the most significant bits are "0." A third error component arises from the mismatch between capacitors $C1$ and $C2$, which results in a discontinuity of one-half the value of the capacitor mismatch at the $(011\cdots1)$ to $(100\cdots0)$ transition. The composite diagram of the three error components shown in Fig. 12 is based on computer simulations and is in general agreement with the measured error curve.

Of the three error components isolated above the first two can be minimized by a self-aligned process or, alternatively, with a mask layout which is more tolerant to masking misalignments. The mismatch error can be compensated along with the input offset voltage of the comparator with the two-conversion approach previously described. The most important source of error in the circuit, therefore, is the feedthrough error voltage.

TABLE III
PERFORMANCE CHARACTERISTICS OF EXPERIMENTAL ADC

Resolution	8 Bits
Conversion Time	100 μs
Power Supplies	+10v,-5v
Input Range	0-5v

VII. CONCLUSIONS

An MOS compatible A/D conversion technique utilizing charge redistribution on equal capacitors has been developed. For a given level of resolution, the technique can be realized in considerably less area than in the case of a weighted capacitor technique. The principal reason for this is that fabrication of precisely ratioed capacitors requires that the large valued capacitors be made up of many small elements, and the use of such techniques as dummy metal strips. These geometrical requirements enlarge the capacitor array by approximately a factor of 2 compared to the area required for two equal capacitors adding up to the same total capacitance. While the total amount of capacitance required to achieve a given level of resolution using the 2-capacitor approach is roughly the same as in the weighted approach for the same resolution, the capacitance can be realized in a much smaller area.

An experimental 8-bit D/A converter was fabricated in *N*-channel metal gate MOS technology. This was used in an experimental A/D converter, and the experimental evidence gathered indicates that the 8-bit level of resolution can readily be achieved with the circuit and capacitors used. The observed performance is summarized in Table III. With an improved layout to minimize sensitivity of feedthrough to mask alignment, and with a common centroid geometry for the capacitors, the area required to achieve 8-bit resolution in a complete single chip A/D converter would be approximately 5000 mil^2.

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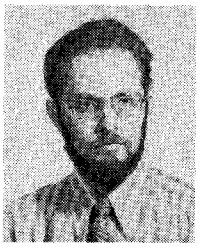

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