An 80dB-SNDR 98dB-SFDR Noise-Shaping SAR ADC with Duty-Cycled Amplifier and Digital-Predicted Mismatch Error Shaping

Hanyue Li, Yuting Shen, Haoming Xin, Eugenio Cantatore and Pieter Harpe
Integrated Circuits Group, Eindhoven University of Technology, Eindhoven, The Netherlands
Email: h.li2@tue.nl

***Abstract*—This paper presents a low-power and high-linearity noise-shaping SAR ADC that employs a duty-cycled amplifier and a mismatch error shaping technique. The power-efficient duty-cycled amplifier with 18x gain and two passive integrators provide 2nd-order noise shaping to improve in-band noise attenuation. Mismatch error shaping with a two-level digital prediction scheme is used to 1st-order shape the capacitive DAC mismatch errors without sacrificing the input signal range. The proposed ADC is fabricated in 65 nm CMOS technology and achieves 80 dB peak SNDR and 98 dB peak SFDR in a 31.25 kHz bandwidth, leading to a Schreier FoM of 176.3 dB.**

Keywords—noise-shaping SAR ADC, mismatch error shaping, duty-cycled amplifier, high linearity

I. Introduction

Low-power, low-speed and high-linearity analog-to-digital converters (ADCs) are in high demand for biomedical, instrumentation and other sensor applications in this Internet-of-Things era. The noise-shaping successive approximation register (NSSAR) ADC is a promising candidate to meet these requirements. As a hybrid implementation of ΣΔ ADC and SAR ADC, the NSSAR ADC inherits both high-resolution and low-power merits from the original ADC architectures. Therefore, it draws the attention of circuits designers and continuously advances the frontier of ADC performance in recent years [1-7].

The basic NSSAR ADC structure is a SAR ADC with an extra loop filter applied to the residue signal to achieve noise shaping. By reusing the capacitive digital-to-analog converter (DAC) in the SAR ADC as the feedback DAC in the noise-shaping loop, the NSSAR ADC can directly obtain the residue information after each SAR conversion and therefore reduces the DAC hardware cost compared to a conventional ΣΔ ADC. At the same time, it is favourable to use fewer active components in the loop filter for a given noise transfer function (NTF), to minimize power and noise overhead. On top of the hardware cost considerations, the NSSAR ADC also brings the benefits of multi-bit quantization, as the SAR ADC resolution is usually in the order of 8 to 12 bits. The multi-bit quantizer leads to improved stability, reduced sensitivity to integrator non-linearity, and lower oversampling ratio (OSR) and/or lower filter-order for a given signal-to-quantization-noise-ratio (SQNR). However, the linearity of an NSSAR ADC is limited by the mismatch of the multi-bit DAC. This paper proposes two solutions: firstly, a duty-cycled amplifier is used to increase the residue gain compared to prior-art, which results in a more aggressive NTF. Secondly, a simplified two-level digital-predicted mismatch error shaping scheme is used to shape DAC mismatch out-of-band in an efficient way.

The paper is organized as follows: Section II describes the overall ADC architecture and its operation. Section III details the design of the duty-cycled amplifier together with a duty-cycled bias circuit. Section IV explains the mismatch error shaping (MES) principle and highlights the advantages of the proposed digital prediction scheme. Section V shows the measured results and conclusions are drawn in Section VI.

II. System Overview

The key point of the NSSAR ADC is its loop filter. Both passive and active loop filters are used in recent NSSAR ADC publications. Passive loop filters [7] leverage charge sharing between capacitors to realize the integration function. They are simple to design but introduce extra sampling noise in each integration action and cannot achieve a sharp NTF due to the leaky integrators. As a result, the DAC capacitor values required to suppress the sampling noise become larger, and the final power efficiency is in general worse than active counterparts. Active loop filters [2][6] consist of amplifiers cascaded with passive integrators to provide a more effective in-band noise suppression. In this way, a higher-order NTF can be realized with fewer active components. Moreover, the passive integrator noise is attenuated by the preceding amplifier, becoming negligible.

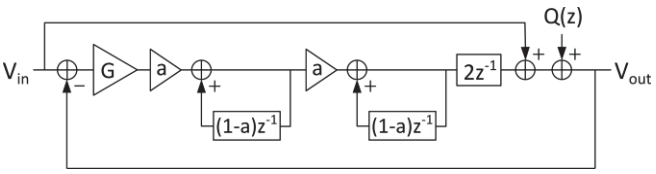

Fig. 1. Signal diagram of the proposed NSSAR ADC.

This work uses the active loop filter structure shown in Fig. 1. Q(z) represents the quantization error of the SAR ADC. After quantization, the residue (V_{in}-V_{out}) is fed to the loop filter, which is composed of an amplifier with gain G and two identical passive integrators. Figure 2 shows the circuit level implementation. The main blocks of this ADC are a differential 10-bit binary-scaled DAC with 1-bit redundancy, an amplifier, two slices of load capacitors C_{RES} for the amplifier, two integration capacitors C_{INT1} and C_{INT2}, a comparator and logic control. The frequency of the external sampling clock φ_{SAMP} is 1 MHz and the ADC has an OSR of 16. After the sampling moment, the DAC is first reset by φ_{RST} (as will be explained in Section IV). When all 11 bits are resolved, the amplifier is enabled by φ_{AMP} and the amplified residue voltage from the SAR conversion is stored on C_{RES}. The 1st passive integration between C_{RES} and C_{INT1} takes place subsequently by φ_{INT1}. After that, the two C_{RES} capacitors which now contain the integrated residue are split

ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC) | 978-1-6654-3751-6/21/$31.00 ©2021 IEEE | DOI: 10.1109/ESSCIRC53450.2021.9567748

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on July 14,2023 at 04:13:56 UTC from IEEE Xplore. Restrictions apply.

to the positive and negative side and perform the 2nd integration with C_{INT2} during φ_{INT2}, as shown in Fig. 2(b). Since C_{INT2} is in series with $C_{DAC,p}$ and $C_{DAC,n}$, it will implement the summation of V_{in} with the integrated residue in front of the quantizer, which is shown in Fig. 1. By placing two C_{INT2} capacitors in series with the DAC, the effective gain of the loop filter is further increased by 2. Besides, this connection avoids the use of a multi-input-pair comparator and gets rid of the extra comparator noise brought by the second input pair [7]. The DAC outputs are connected to V_{CM} during the 2nd integration phase to avoid signal-dependent charge injection at the end of the integration phase. The offset requirements for the amplifier and comparator are also relaxed, because both offsets will reside on C_{INT2} after the modulator is stable, lowering the maximum amplifier output range.

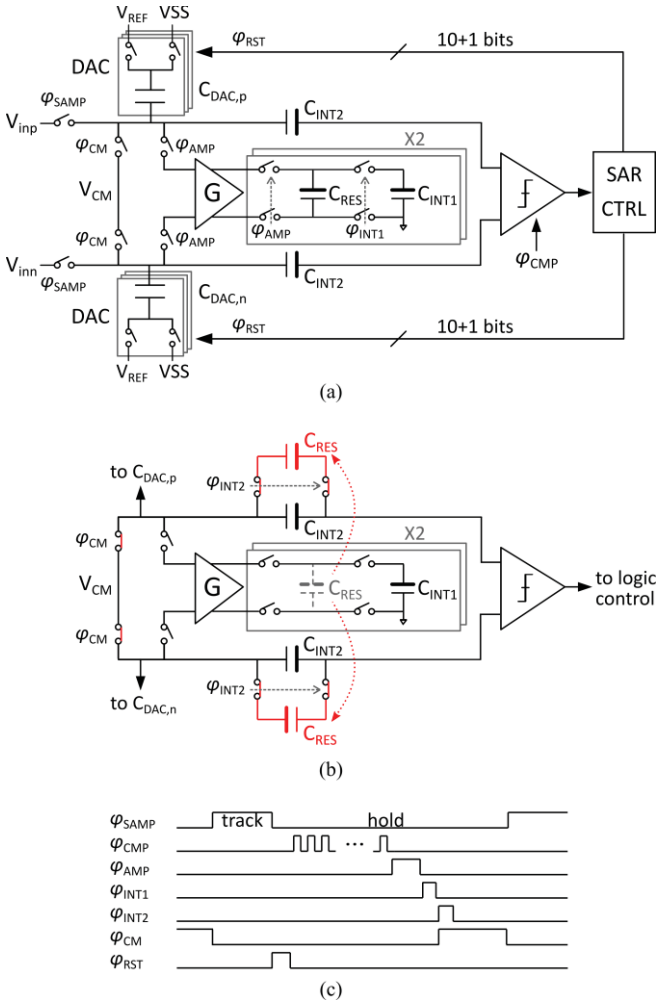

Fig. 2. (a) Proposed NSSAR ADC. (b) The 2nd integration phase. (c) Timing diagram.

A sharper NTF and higher in-band noise suppression can be obtained by increasing the amplifier gain G, but larger gain may cause instability. In this work, C_{INT1} is equal to C_{INT2}, and both are 3 times C_{RES} ($C_{INT1} = C_{INT2} = 3C_{RES} = 75$ fF), resulting in a coefficient a = ¼ in Fig. 1. The maximum amplifier gain to ensure stability is 23, and the nominal gain is set to 18 to account for PVT variations. The in-band noise attenuation is 30 dB, which is 3 dB higher than in [1] and 8 dB higher than in [2] (both using a similar loop filter structure), assuming the same OSR of 16x. The nominal NTF can be expressed as $(1-1.5z^{-1}+0.56z^{-2}) / (1+0.75z^{-1}+0.56z^{-2})$, hence a 2nd-order shaping is achieved.

III. Duty-Cycled Amplifier

Dynamic amplifiers are often used due to their efficiency. However, their gain is limited by the allowed output common mode headroom, which is determined by the supply voltage. For instance, the dynamic amplifier in [2] has a gain of 13.3x, which is not enough for the proposed ADC. Therefore, a duty-cycled amplifier is adopted in this work, as shown in Fig. 3(a). This amplifier has an inverter-based input stage to boost transconductance, and switches to enable duty-cycling. The DC gain of this amplifier is designed to be 40x and the required 18x gain can be obtained by controlling the enable time to achieve incomplete settling. The common mode feedback (CMFB) of the amplifier is implemented by splitting the bottom tail current source and connecting their gates to the output nodes. This CMFB approach is suitable here, because the design does not require an accurate output common mode and the differential output range of the amplifier is only ±200 mV. The linearity of the amplifier is also not very critical, because the amplifier input only consists of the noise signal: amplifier non-linearity will thus only result in a slight increase in noise floor, but will not produce signal distortion.

Duty-cycled amplifiers have been used in prior ADC works, but the current consumption associated with the bias current generation is usually neglected. In this work, a duty-cycled constant-g_m bias circuit is also developed to provide the bias voltage V_b for the amplifier, as shown in Fig. 3(b). The start-up circuit is not drawn for simplicity. On top of the decoupling capacitors between the gate of the current mirror and supply/ground, another decoupling capacitor C_b (2 pF) is added to further stabilize V_b during duty-cycling. The control clocks φ_{BCLK1} and φ_{BCLK2} are derived from the asynchronous SAR logic and are only enabled once per 16 sampling clock cycles. The bias circuit is disabled in the other cycles, while the voltage V_b is kept by C_b. In this way, the consumption of the bias generator is reduced to a small fraction of the amplifier power.

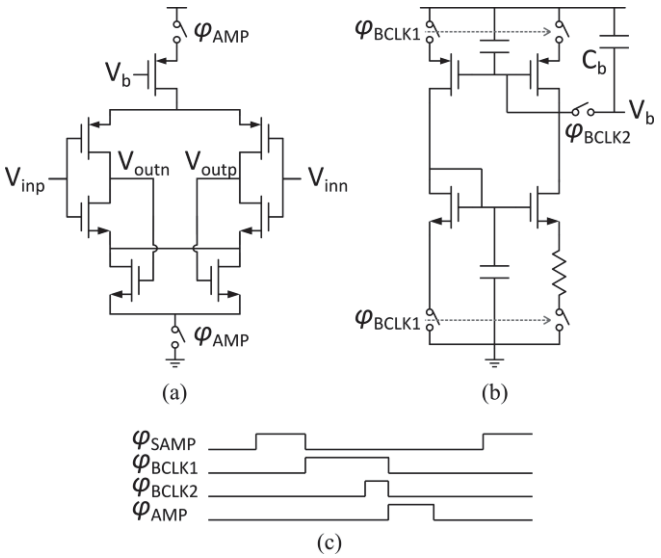

Fig. 3. (a) Duty-cycled amplifier. (b) Duty-cycled bias circuit. (c) Timing for the amplifier and bias circuit.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on July 14,2023 at 04:13:56 UTC from IEEE Xplore. Restrictions apply.

IV. Mismatch Error Shaping

A. Principle of MES

An effective method to deal with DAC mismatch in an oversampled SAR ADC is mismatch error shaping (MES) [1]. Figure 4 shows the principle of MES. During the SAR conversion, the DAC generates the reference voltage, modelled as an ideal DAC voltage V_{DAC} and a mismatch error E(n), for the comparator. After the SAR conversion is finished, the MSB control bit is reset immediately, but the LSBs control bits (D_{n-1}, …, D_1, D_0, as shown in Fig. 5) are held until the sampling of the next input signal. After the sampling phase, the DAC LSBs (MSB-1 to LSB) are reset, which equivalently adds the ideal DAC LSB voltage V_{LSBs} and the mismatch error E(n-1) from the previous sample to the current input. By altering the reset timing in this way and subtracting the additional V_{LSBs} in the digital domain, mismatch errors are 1st-order shaped [1]. However, because V_{LSBs} has a theoretical range between $-½V_{REF}$ and $+½V_{REF}$, over range may occur at the input of the converter as indicated in Fig. 4.

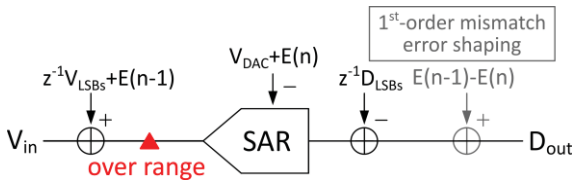

Fig. 4. Principle of the 1st-order MES and its over range problem.

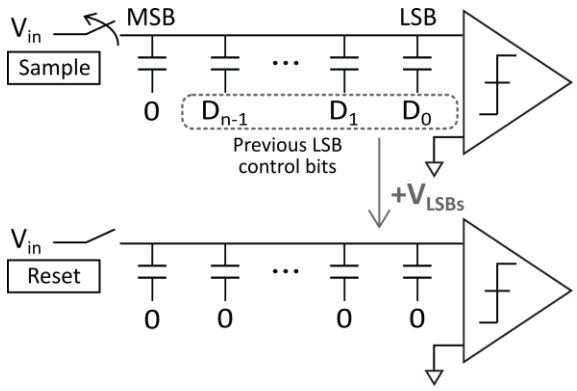

Fig. 5. The DAC switching sequence for MES proposed in [1].

B. Digital prediction scheme

To deal with the over range problem in MES, [1] only applies MES to capacitors from MSB-3 downwards and uses data weighted averaging (DWA) for the first 3 MSB capacitors. Reference [3] proposed a digital prediction scheme to detect the over range occurrence and compensate it. The main idea is that, in an oversampled system, the current ADC output can be used as a rough guess for the next input sample of the ADC. Therefore, the actual input (after reset of the LSBs) can be estimated from the available ADC output information. Using this estimate, the MSB capacitor in [3] is split into two separate capacitors, which are pre-set according to the estimate before sampling to compensate the V_{LSBs} shift. However, this method still requires DWA to mitigate the MSB capacitors' mismatch.

This work improves the method described in [3] by introducing a two-level over range detection scheme, as shown in Fig. 6 and Fig. 7. The estimated next ADC input D_P is calculated by adding the first 3 bits (MSB to MSB-2) from the current ADC output code D_{out} and the first 2 bits from the current SAR output code D_{LSBs}. To provide MSB compensation, a split switching scheme is used in the DAC. By judging if D_P is greater or less than zero, the MSB capacitors are pre-set to '11' or '00' before the track phase. Therefore, an extra compensation voltage V_{comp} can be obtained by resetting the MSB capacitors after the sampling moment. The tri-level prediction scheme in [3] works similarly, but when D_P is between $-V_{det}$ and V_{det} (V_{det} = $⅓V_{REF}$), the MSB capacitor does not switch and provides V_{comp} = 0 V. In this case, the mismatch between MSB capacitors (C_L and C_R in Fig. 7) is not completely shaped and will limit the final performance. The proposed two-level detection scheme, instead, ensures that the MSB capacitors are always involved in the over range compensation and that their mismatch is also shaped. The minimum OSR required for reliable prediction is 6, which is slightly higher than that required for the tri-level prediction. As alternative, an analog detection scheme was proposed in [8], but it needs an additional comparison cycle and complicates the logic. In this work, because it is sufficient to determine only the MSB of D_P for the polarity prediction, the prediction circuit is simple and does not need full adders.

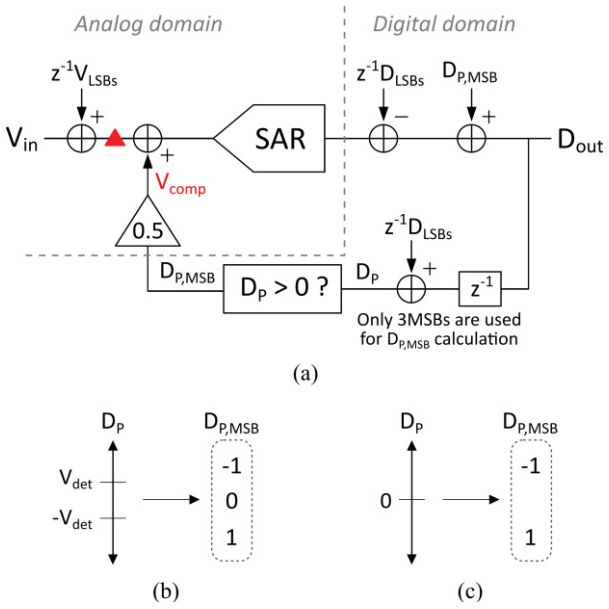

Fig. 6. (a) Principle of the MES with digital prediction. (b) Tri-level prediction scheme proposed in [3]. (c) Two-level prediction scheme in this work.

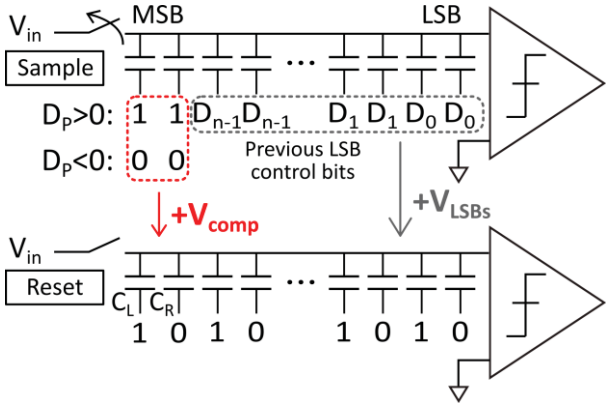

Fig. 7. DAC switching sequence in the proposed MES with two-level digital prediction.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on July 14,2023 at 04:13:56 UTC from IEEE Xplore. Restrictions apply.

V. Measurement Results

The prototype is fabricated in a 65 nm CMOS technology. The area of the ADC is 0.043 mm^2, as shown in Fig. 8. Thanks to MES, the DAC capacitance is reduced to 1 pF per side. It is only limited by noise requirements and occupies less than half of the total area. Except for the sampling clock, other logic blocks (SAR logic, MES prediction logic, NS logic to generate all the clocks shown in Fig. 2 and Fig. 3) are implemented on-chip.

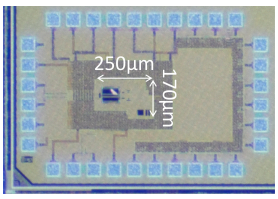

Fig. 8. Die photo.

Figure 9 shows the measured spectrum without and with MES at an input signal frequency of 946.07 Hz and a sampling frequency of 1 MS/s. After enabling MES, the SNDR and SFDR improve from 66 dB to 80 dB and from 69 dB to 98 dB, respectively. The odd-order harmonics caused by DAC mismatch are reduced greatly. Figure 10 shows the ADC performance over input signal power and input frequency. The dynamic range (DR) of this ADC is 81.4 dB.

Table I presents a performance summary and comparison to state-of-the-art NSSAR ADCs. Only NSSAR ADCs with on-chip DAC mismatch calibration/correction are shown here for a fair comparison. There are other works that achieve better figure-of-merit (FoM) [5][6], but the DAC calibration is done off-chip and its cost is not included in the calculation. Compared to the reports in the table, this work achieves a relatively high loop-filter order, comparable SFDR and FoMs, a minimum DAC capacitance, and a simple architecture.

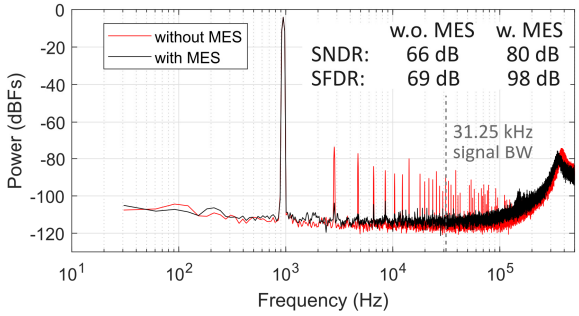

Fig. 9. Measured spectrum without and with MES (Hamming window, 10x averaging).

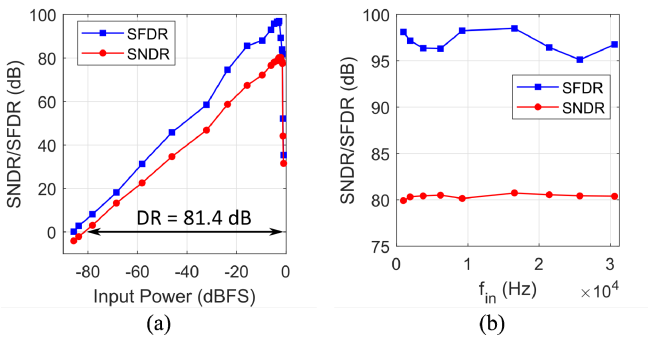

Fig. 10. Measured SNDR and SFDR vs. (a) input power and (b) input frequency.

TABLE I. Benchmark with Other Works

	[1]		[2]	[3]		[4]	This work
Technology	55 nm		28 nm	40 nm		28 nm	65 nm
Supply [V]	1.2		1	1.1		1.8/1.1	1.2
Loop filter order	1		1	1		3	2
SAR resolution	12		10	13		12	10
Fs [MS/s]	1		132	2		1	1
BW [kHz]	1	4	5000	40	10	20	31.25
Cap mismatch solution	1st-order MES + DWA		DWA	2nd-order MES + DWA		DEM + dither	1st-order MES
DAC cap per side	2.4 pF		1.6 pF	N.A.		N.A.	1 pF
SNDR [dB]	101	96.1	81.3	90.5	95.3	93.95	80
SFDR [dB]	105.1	105.1	92.2	102.2	102.2	108.0	98
Power [µW]	15.7		480	67.4		493.1	7.3
FoMw [fJ/c.s.]	85.6	37.6	5.1	30.8	70.8	302.6	14.3
FoMs [dB]	179.0	180.2	181.5	178.2	177.0	170.0	176.3
Area [mm^2]	0.072		0.0049	0.061		0.116	0.043

VI. Conclusions

The NSSAR ADC proposed in this paper uses a duty-cycled amplifier together with a duty-cycled bias generator inside the loop filter. As a result, it provides higher gain and achieves stronger in-band noise attenuation in a power-efficient way. Furthermore, a two-level digital-predicted MES technique solves the DAC mismatch problems while preventing over range, with little hardware cost. Thanks to these techniques, the ADC reaches 80 dB SNDR and 98 dB SFDR in a 31.25 kHz bandwidth while consuming 7.3 µW.

Acknowledgements

This work with project number 16594 is financed by the Dutch Research Council (NWO).

References

[1] Y.-S. Shu, L.-T. Kuo and T.-Y. Lo, "An oversampling SAR ADC with DAC mismatch error shaping achieving 105dB SFDR and 101dB SNDR over 1kHz BW in 55nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 458–459.

[2] C.-C. Liu and M.-C. Huang, "A 0.46 mW 5MHz-BW 79.7 dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter," in *ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 466–467.

[3] J. Liu, et al., "A 40kHz-BW 90dB-SNDR noise-shaping SAR with 4× passive gain and 2nd-order mismatch error shaping," in *ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 158–160.

[4] K. Obata, et al., "A 97.99 dB SNDR, 2 kHz BW, 37.1 µW noise-shaping SAR ADC with dynamic element matching and modulation dither effect," in *proc. VLSI Symp.*, 2016, pp. 1–2.

[5] J. Liu, D. Li, Y. Zhong, X. Tang and N. Sun, "A 250kHz-BW 93dB-SNDR 4th-order noise-shaping SAR using capacitor stacking and dynamic buffering," in *ISSCC Dig. Tech. Papers*, Feb. 2021, pp. 369–371.

[6] T.-H. Wang, R. Wu, V. Gupta and S. Li, "A 13.8-ENOB 0.4pF-C_{IN} 3rd-order noise-shaping SAR in a single-amplifier EF-CIFF structure with fully dynamic hardware-reusing kT/C noise cancelation," in *ISSCC Dig. Tech. Papers*, Feb. 2021, pp. 374–376.

[7] Y.-Z. Lin, C.-Y. Lin, S.-C. Tsou, C.-H. Tsai and C.-H. Lu, "A 40MHz-BW 320MS/s passive noise-shaping SAR ADC with passive signal-residue summation in 14nm FinFET," in *ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 330–332.

[8] Y. Shen, H. Li, H. Xin, E. Cantatore and P. Harpe, "A low-cost 0.98µW 0.8V oversampled SAR ADC with pre-comparison and mismatch error shaping achieving 84.5dB SNDR and 103dB SFDR," in *proc. CICC*, 2021, pp. 1–2.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on July 14,2023 at 04:13:56 UTC from IEEE Xplore. Restrictions apply.