18.5 A Self-Calibrated Pipeline ADC with 200MHz IF-Sampling Frontend

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In cellular base stations, a recent trend is to digitize multiple channels with a single ADC, even directly from IF. Thus, there is increasing demand for ADCs with wide dynamic range, particularly high SFDR, and capability of sampling signals up to 200MHz frequency. This 13b 50MSample/s pipeline ADC, fabricated in a 0.35µm BiCMOS (SiGe) process, incorporates digital self-calibration and achieves 76.5dB SFDR at 194.2MHz input dissipating 715mW from a 2.9V supply.

Figure 18.5.1 shows the block diagram of the ADC. The wideband frontend S/H circuit feeds a pipeline ADC, which consists of two calibrated 2.5b stages followed by nine 1.5b stages and a 2b flash and gives 15 output bits, the two least significant of which are used for calibration. The stage output bits are first processed by an RSD correction circuitry after which the calibration coefficients are applied. Synchronization between the S/H and the pipeline is realized with a DLL. An on-chip state machine controls the ADC during the calibration cycle. The calibration algorithm is implemented off-chip with an FPGA circuit. Fully-differential circuitry is used throughout the design. To minimize the effect of thermal noise the maximum signal swing is set as high as 3.8Vpp differential.

At high signal frequencies the ADC performance is predominantly set by the front-end S/H circuit, which is an SC amplifier with programmable gain of 1 or 2. In the unity-gain mode, the circuit acts as a flip-around S/H circuit, while the gain of 2 mode is realized by splitting the sampling capacitor in two and connecting one half into feedback and the other to the signal ground in the hold phase. The total sampling capacitance is 10pF, which leaves enough margin to the 13b target resolution for the noise contribution of the opamp and the ADC.

The sampling linearity is determined almost solely by the input switch device, the signal-dependent on-resistance and parasitic capacitances of which being the distortion sources. To improve linearity, the bootstrapped MOS switch shown in Figure 18.5.2 is used. Unlike in a typical realization, the gate voltage of the switch transistor (MS) does not track the input voltage, but rather the average of the input and the output voltages. This reduces the distortion when the signal current produces a voltage drop over the on-resistance, which is unavoidable with a large-amplitude IF signal. The bulk voltage of the switch transistor also tracks the signal, reducing the bulk effect and keeping the voltage over the nonlinear junction capacitances almost constant, which is essential for low distortion. The signal-dependent charge injection is minimized by the bottom plate sampling technique and is further reduced by bootstrapping in the sampling switch. Bootstrapped switches are also employed in the first two pipeline stages.

From the opamp, high gain and wide bandwidth are required simultaneously with low noise and maximal output voltage swing to obtain fast and accurate settling with a high SNR. The two-stage BiCMOS opamp, shown in Figure 18.5.3, utilizes an all-nMOS-npn signal path and cascode compensation to achieve wide bandwidth, a telescopic first stage to obtain low noise and high DC-gain, and a rail-to-rail output stage to maximize the output signal swing. The capacitive level shifting, employed between the opamp stages, is virtually noiseless and does not require a bias current, but requires fairly large capacitors to prevent signal attenuation. Separate CMFB loops are used for the first and the second stage, both realized with the traditional SC circuit. Since in the pipeline stages the opamp does not have to be unity-gain stable, the compensation capacitor is made smaller to gain more close-loop bandwidth. In the latter stages, the amplifier is also scaled down due to the smaller load.

In IF-sampling low clock jitter is essential and thus noise coupling to the clock signal must be minimized. The circuit has a differential clock buffer for bringing in the clock signal from a crystal oscillator. To avoid the noise contribution of a clock generator, the sampling clock is taken directly after the buffer, while a conventional clock generator produces the non-overlapping signals for the other switches in the S/H. The clocks of the pipeline stages are synchronized to the sampling clock with a DLL.

A high-resolution stage in the front of the pipeline ADC provides linearity improvement as well as power savings in the subsequent stages [1]. However, each additional bit in the first stage halves its feedback factor and doubles the comparator accuracy requirement. By having two medium-resolution front-end stages the noise contribution of the subsequent stages is similarly reduced allowing scaling in the backend stages, the amplifier and comparator specifications being still reasonable.

To achieve the 13b resolution with high yield, digital self-calibration, developed from Reference [2], is utilized. A simplified schematic of the MDACs employing the calibration method is shown in Figure 18.5.4. In the 2.5b stage on the left, the error attached to each reference unit capacitor is measured separately with the backend stages. The stage under calibration samples the analog ground voltage and in the hold mode the capacitor being measured is connected to $\pm V_{ref}$, while the extra calibration capacitor is connected to opposite V_{ref} and other capacitors to ground. The purpose of the extra capacitor is to bring the MDAC output to the voltage range of normal operation. Following the switching scheme of the stage, correction coefficients for the stage output codes and the offset are cumulatively calculated from the capacitor errors. The stored coefficients are added to the output during the normal operation.

The first two 1.5b stages of the backend pipeline are actually used as amplifiers during the calibration, which allows enhancing resolution of the measurement by a factor of four simply by doubling the stage gain. This is accomplished by halving the MDAC feedback capacitor during the calibration, as shown in Figure 18.5.4.

The circuit is measured with an LC resonator for isolating the SC load from the signal source. The uncalibrated INL is ±7.1LSB improving to ±3.0LSB after the calibration. In Figure 18.5.5, a spectrum obtained with a 194.2MHz signal shows 76.5dB SFDR. A timing error in the digital delay line produced random bit errors, which raises the noise floor and limits the SNDR below 55dB. The performance is summarized in Figure 18.5.6 and the die micrograph is shown in Figure 18.5.7.

References:

[1] L. Singer et al., "A 12b 65MSample/S CMOS ADC with 82dB SFDR at 120MHz," ISSCC Digest Technical Papers, pp. 38-39, Feb. 2000.

[2] S.-H. Lee, B.-S. Song, "Digital-Domain Calibration for Multistep Analog-to-Digital Converters," IEEE J. Solid-State Circuits, vol. 27, pp. 1679-1688, Dec. 1992.

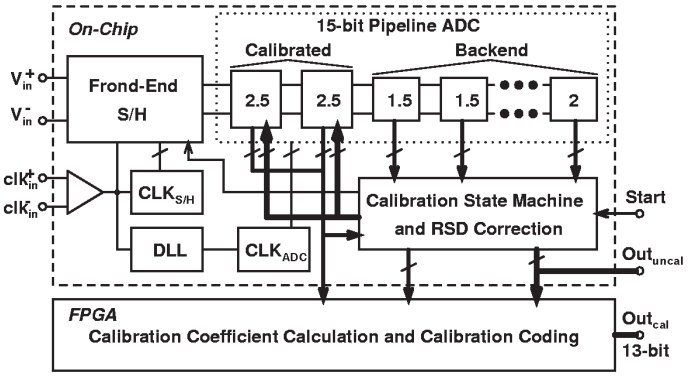

Figure 18.5.1: Block diagram.

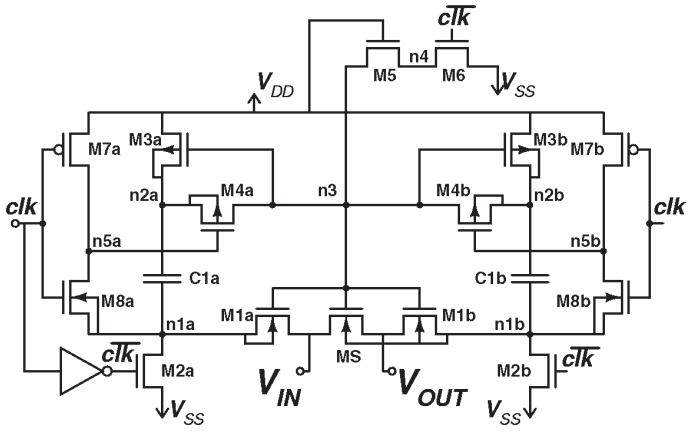

Figure 18.5.2: Double-side bootstrapped input switch.

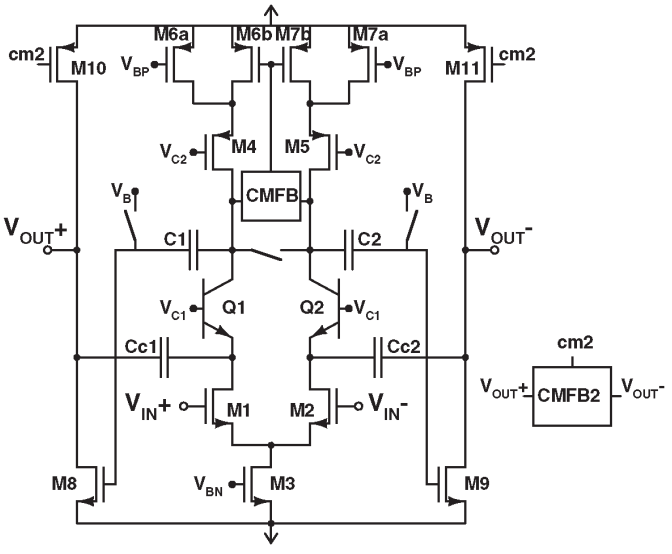

Figure 18.5.3: BiCMOS opamp.

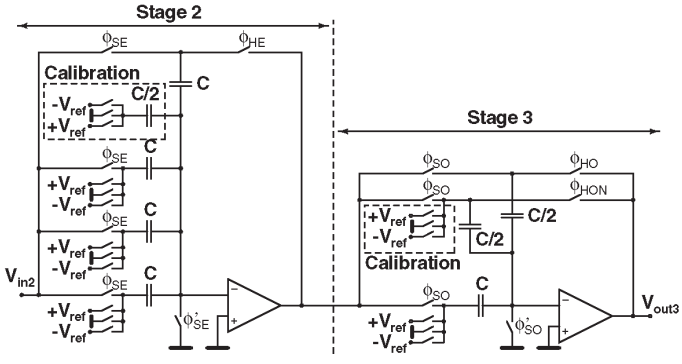

Figure 18.5.4: Principle of calibration: stage3 is used as an amplifier when stage2 errors are being measured.

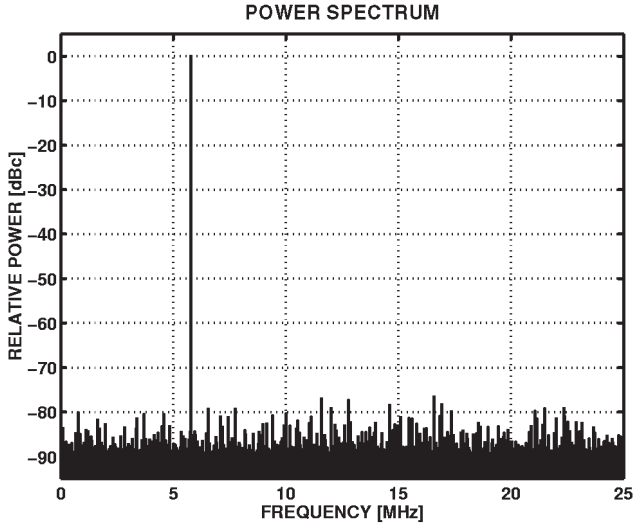

Figure 18.5.5: Down converted spectrum with —1-dBFS, 194.2MHz signal.

Resolution	13b
Sample Rate	50MSample/s
Input Voltage (differential)	3.8Vpp
Input Bandwidth	200MHz
DNL / INL (calibrated)	±1.0 / ±3.0LSB
SFDR (at 200MHz)	76.5dB
Power Dissipation at 2.9V	715mW
Die Area	6.0mm^2
Technology	0.35µm BiCMOS(SiGe)

Figure 18.5.6: Summarized performance.

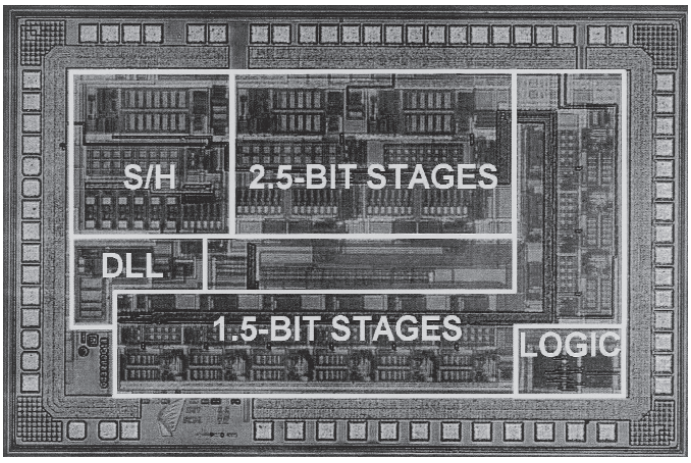

Figure 18.5.7: 13b 50MSample/s pipeline ADC die micrograph.