V_{CM}-based monotonic capacitor switching scheme for SAR ADC

Zhangming Zhu, Yu Xiao and Xiaoli Song

A novel energy-efficient V_{CM}-based monotonic capacitor switching scheme for successive approximation register (SAR) analogue to-digital converters (ADCs) is proposed. Based on the third reference voltage V_{CM} and monotonic capacitor switching procedure, the proposed switching scheme achieves 97.66% less switching energy and 75% less number of capacitors over the conventional architecture, resulting in the most energy-efficient switching scheme among the reported switching sequences.

Introduction: In SAR ADCs, the primary sources of power consumption are capacitor arrays, the comparator, and digital circuits. With the advanced technology and supply voltage scaling, the digital power dissipation is becoming lower. The fully dynamic comparator is often used owing to its good power efficiency. Therefore, the power of capacitor arrays dominates the overall power consumption of SAR ADCs. Recently, several energy-efficient switching schemes have been developed to reduce the power of capacitor arrays. Compared to conventional architecture [1], the set and down [2], V_{CM}-based [3], and new tri-level switching scheme [4] reduces the switching energy by 81.26, 87.54, and 96.89%, respectively. In this Letter, a more energy-efficient V_{CM}-based monotonic capacitor switching procedure is presented. By using the level shift technique after the MSB is determined and the V_{CM}-based monotonic switching procedure for LSBs comparison, the switching energy and number of capacitors have been significantly reduced.

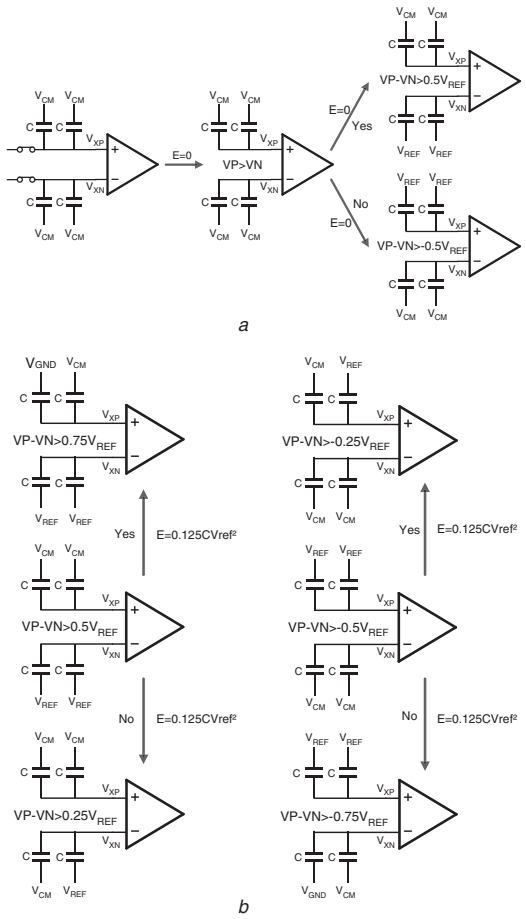

Fig. 1 *V_{CM}-based monotonic capacitor switching scheme of 3-bit ADC*

V_{CM}-based monotonic capacitor switching scheme: To explain the proposed scheme, a 3-bit differential SAR ADC is used. The scheme can be performed in two phases: the MSB phase and next 2 bits phase, as shown in Figs. 1*a* and *b*. In Fig. 1*a*, the differential input signal is sampled on the top-plates of two capacitor arrays via sampling switches, and simultaneously the bottom-plates of capacitors are connected to the common-mode voltage V_{CM} which is designed to be half of V_{REF}. Next, the sampling switches are turned off and the comparator performs the first comparison without consuming any switching energy. Once the MSB is obtained, the bottom-plates of the capacitor array which samples the lower input voltage are reconnected to V_{REF} and the other capacitor array remains unchanged. Thus, the voltage of capacitors on the lower voltage potential side is level-shifted by $0.5V_{REF}$. This operation consumes no switching energy. After the MSB comparison, the different reference voltages will be chosen for the differential capacitor arrays, as shown in Table 1. If MSB = 1, the positive and negative reference voltages on the V_{XP} side will be V_{CM} and V_{GND}. On the other side, the positive and negative reference voltages will be V_{REF} and V_{CM}. Then the ADC performs the monotonic capacitor switching procedure for the following successive approximation operation.

Table 1: Different reference voltages are chosen for differential capacitor arrays according to first comparison result

	MSB = 1		MSB = 0	
Differential input	V_{XP} side	V_{XN} side	V_{XP} side	V_{XN} side
Positive reference	V_{CM}	V_{REF}	V_{REF}	V_{CM}
Negative reference	V_{GND}	V_{CM}	V_{CM}	V_{GND}

As shown in Fig.1*b*, according to the comparator output, the corresponding bit-capacitor on the higher voltage potential side is switched from V_{CM} to ground or from V_{REF} to V_{CM} and the other one remains unchanged. The ADC repeats the procedure until the LSB is decided. During the monotonic switching procedure, there is only one capacitor switch for each bit cycle, resulting in less switching activity and lower energy. Figs. 2*a* and *b* show the successive approximation waveforms of the set and down switching scheme and the proposed method, respectively. As shown in Fig. 2*b*, the proposed switching scheme reduces the common-mode voltage variation by 50% compared to the set and down switching procedure. The common-mode voltage of the proposed switching scheme will gradually approach the V_{CM}.

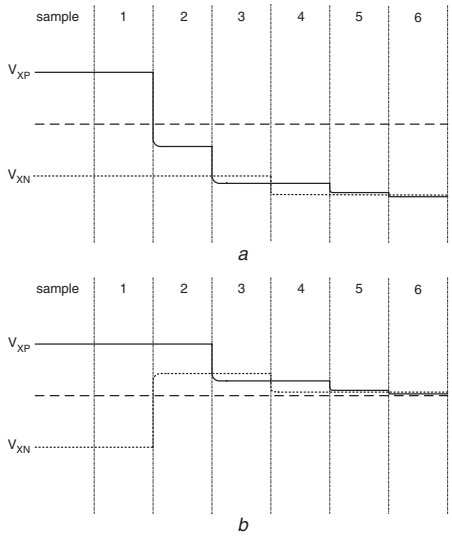

Fig. 2 *Waveform of set and down switching scheme, and waveform of V_{CM}-based monotonic capacitor switching scheme*

a Set and down switching scheme
b V_{CM}-based monotonic capacitor switching scheme

Table 2: Comparison of switching schemes

Switching scheme	Average switching energy (CV^2_{REF})	Energy saving	Area reduction
Set and down	255.5	Reference	Reference
V_{CM}-based	170.17	33.4%	0
New tri-level	42.41	83.4%	50%
Proposed	31.88	87.1%	50%

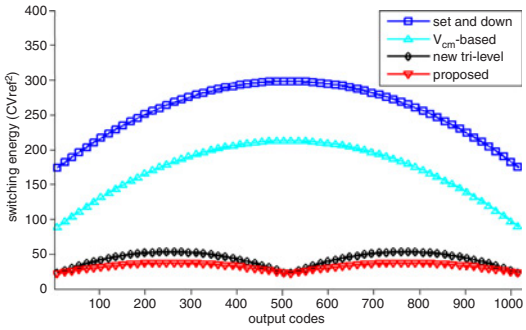

Fig. 3 *Switching energy against output codes*

Switching energy analysis: The behaviour simulations of a 10-bit differential SAR ADC were performed to compare the average switching energy for previously reported switching schemes and the proposed V_{CM}-based monotonic capacitor switching scheme. Table 2 summarises the features of different schemes. The average switching energy for the set and down switching scheme equals $255.5CV_{REF}^2$, while the proposed switching scheme only consumes $31.875CV_{REF}^2$. The proposed method requires 87.1% less switching energy than that of the set and down one. The V_{CM}-based and new tri-level switching scheme provide only 33.4 and 83.4% reduction, respectively. Furthermore, the proposed scheme achieves 50% capacitor area saving with respect to the set and down switching procedure. Fig. 3 shows a comparison of switching energy for the several switching schemes against the output code. The proposed scheme achieves the best power efficiency. For an N-bit SAR ADC, the average switching energy for the proposed switching scheme can be derived as:

$$E_{avg} = \sum_{i=1}^{N-2} (2^{N-i-5}) CV_{REF}^2 \quad (1)$$

Linearity: The minimum value of the unit capacitor is usually determined by the capacitor mismatch, assuming the unit capacitor is modelled with a nominal value of C_u and a standard deviation of σ_u. Since the V_{CM}-based monotonic switching scheme determines the first two MSBs mismatch-independently, the worst case DNL occurs at $1/4V_{FS}$ and $3/4V_{FS}$. Considering an N-bit DAC with the differential architecture, $2 \times (2^{N-2} - 1)C_u$-elements are switched when the two code transitions occur, with an LSB of $2C_u$, leading to a σ_{DNL} of:

$$\sigma_{DNL,MAX} = \frac{\sqrt{2 \times (2^{N-2} - 1)}\sigma_u}{2C_u} \quad (2)$$

Compared to the set and down switching scheme, the request of matching between unit capacitors is relaxed by a factor of $\sqrt{2}$.

Conclusion: An energy-efficient V_{CM}-based monotonic capacitor switching scheme for a SAR ADC is proposed. The three reference voltage levels and monotonic capacitor switching scheme result in a low power and area-efficient SAR ADC. The proposed switching scheme provides the lowest switching energy among the published switching schemes and also has relaxed capacitor matching requirements.

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One or more of the Figures in this Letter are available in colour online.

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