# The High-Speed Low-Power Dynamic Comparator



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**Abstract**. This paper comments on four works for the optimization of comparator design. Today, with the development of integrated circuits, the requirements for comparators about low power, low delay, few offset voltage, and low noise are highly desirable. Specifically, these works made progress in the conventional comparator, which comprises a preamplifier and a latch. They also solved some problems, such as decreasing power and delay. Some works employ a positive feedback cross-coupled pares to provide a larger gain in the preamplifier, use PMOS switch transistors to accelerate the definition phase, or a double-tail architecture to increase the latch regeneration speed. Other work designs a charge pump to improve speed.

## 1. Introduction

In two high-speed parallel ADCs, a high-speed comparator is the main factor limiting the max samples of ADCs and the power consumptions. The performance of the comparator is based on speed, precision, and power consumption, in the ideal condition. However, the delay between the output and the input of the comparator is inevitable due to response time and settling time which support the comparator to work properly. So, reducing the delay is the main purpose of improving the performance of ADCs.

Some works made progress among the conventional comparators. The first is that Samaneh Babayan-Mashhadi and his team members substitute the classic structure of single-tail with a kind of double-tail structure to increase the latch regeneration speed. As to the second one, Ata Khorami and Mohammad Sharifkhani demonstrate a low-power comparator. PMOS is provided as input of the latch stage and the cross-coupled circuit is used for the preamplifier. The third one, YAO WANG et al., present a novel comparator with the latching stage using divided gate-biasing, providing a much faster speed and lower energy consumption.

Moreover, a novel innovation is designed by Haoyu Zhuang and his teammates. They add a charge pump to the conventional Miyahara's comparator, which is used in the bootstrap switch, increasing the actual voltage of the latch, thus increasing the regeneration speed. It decreases the delay compared to conventional Miyahara', but it can still be improved since the power consumption increases.

This paper describes the design, progress, and innovation based on the conventional comparator. The paper is organized as follows. Section Ⅱ introduces the conventional comparator. The innovations are discussed in Section Ⅲ, and finally, Section Ⅳ concludes the paper.

## 2. Conventional dynamic comparator

The schematic diagram of the conventional dynamic comparator is shown in Fig.1.The operation of the comparator is as follows [1]. During the reset phase, the CLK equals 0, and Mtail is off. Both Outn and Outp start to work and are charged. In the comparison phase, Outp and Outn, which have been pre-charged, will start to discharge with different discharging rates depending on the VINN and VINP

The delay of the comparator is comprised of two times delays, which are t0 and tlatch. As given in Fig1. The CL is the comparator load, Itail is the function of input common-mode voltage (Vcm) and VDD. Also, β1,2 is the input transistors' current factor, so the delay is obtained as:

$$t_{delay} = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4|V_{thp}|\,\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right) \quad (1)$$

This structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. However, a needed sufficiently high supply voltage, and only one current path are the disadvantages.

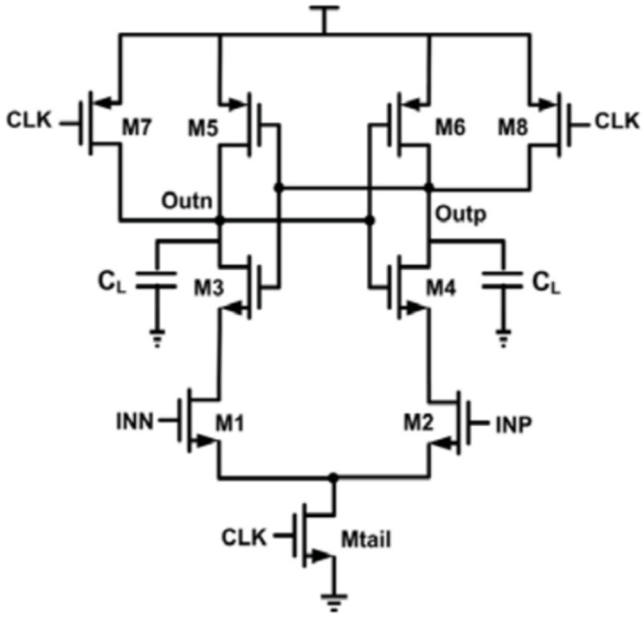



Fig.1 Conventional comparator

## 3. Proposed comparator

### *3.1. double-tail dynamic comparator*

Samaneh Babayan-Mashhadi and his teammates design a low-power double-tail comparator in 2014. The schematic of the conventional double-tail dynamic comparator is shown in Fig.2(a). This comparator can operate at lower supply voltages due to its topology. The double tail structure can enable a large current in the latching stage and a wider Mtail2, which leads to the fast latching independent of the input common-mode voltage and a small current in the input stage used for low offset [2]. Also, a shielding between input and output is provided by the intermediate stage results in the reduced value of kickback noise. Similar to the conventional dynamic comparator, the total delay of the comparator is achieved as follows:

$$t_{delay} = 2\frac{C_{Lout}V_{thn}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}}\ln\left(\frac{V_{DD}\cdot I_{tail2}^2\cdot C_{L,fn(p)}}{8\,V_{thn}^2\cdot C_{Lout}\,g_{mR1,2}g_{m1,2}\,\Delta V_{in}}\right) \quad (2)$$

However, the performance of the conventional double-tail comparator can still be improved since it can obtain a more optimal delay. To optimize the conventional comparator, a novel comparator is designed, and Fig.2(b). demonstrates the schematic diagram of the proposed novel dynamic double-tail

comparator. It is based on the double-tail structure due to the better performance in low-voltage applications. Increasing ΔVfn/fp to improve the latch regeneration is the main design idea. To achieve this goal, two measures are operated. The first is that two control transistors are added in a cross-coupled manner. The second is two added nMOS switches, Msw1 and Msw2, which can avoid static power consumption because they can emulate the operation of the latch and increase the fn and fp's voltage difference.

The operation of the proposed comparator is as follows. During the reset phase, fn and fp nodes are pulled to VDD by M3 and M4, and the intermediate stage transistors MR1, MR2 reset both latch outputs to the ground. In the decision-making phase, fn and fp start to drop with different rates according to the voltages. Unlike in conventional double-tail dynamic comparator that ΔVfn/fp is just the function of input transistor transconductance and input voltage difference, in the proposed comparator when one fn/fp nodes is discharging faster, the other one will be pulled back to VDD. By doing this, ΔVfn/fp increases exponentially, and the latch regeneration time will be reduced.

In summary, the delay of the proposed comparator is reduced for two factors. Firstly, it increases the initial output voltage difference at the beginning of the regeneration, defined as ΔV0. What's more, the effective transconductance gmeff is enhanced because one of fn and fp will charge up back to the VDD and turn on one of the intermediate stage transistors. So the total delay of the proposed comparator follows the formula:

$$t_{delay} = 2\frac{V_{thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \times \ln\left(\frac{V_{DD}/2}{4V_{thn}|V_{thp}|\frac{g_{mR1,2}}{I_{tail2}}\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}}\exp\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,fn(p)}}\right)}\right) \quad (3)$$

The proposed comparator utilizes the inner positive feedback in double-tail operation and finally strengthens the latch regeneration, improving low supply voltages.

The proposed comparator and the conventional comparator are all designed in 0.18um CMOS technology with VDD=1.2V. Fig.3 displays the post-layout simulation results of the delay and the energy per conversion of the mentioned dynamic comparators versus supply voltage variation [3]. As seen from the simulation, the delay is significantly reduced in low-voltage supplies, which means the proposed comparator can be used in the lower supply voltages to consume the same power as the conventional one.

Fig.4 presents the simulated performance as a function of input common voltage. It's apparent that the double-tail comparator is less affected by the variation of the input common-mode voltage than the conventional one. Fig.5 illustrates the dependence of the comparator delay on power supply level at various differential input voltages. The larger the differential input voltage, the smaller the comparator delay. Fig.6 shows the simulated delay of the comparator versus differential input voltage under different conditions of input common-mode voltage at VDD=1.2V. When the Vcm is a fixed value, the delay decreased as differential input voltage increased, and the delay is dependent on the variation of common-mode voltage.

In summary, the method used to decide important parameters and emulate them provides new ideas for us to optimize the comparator.

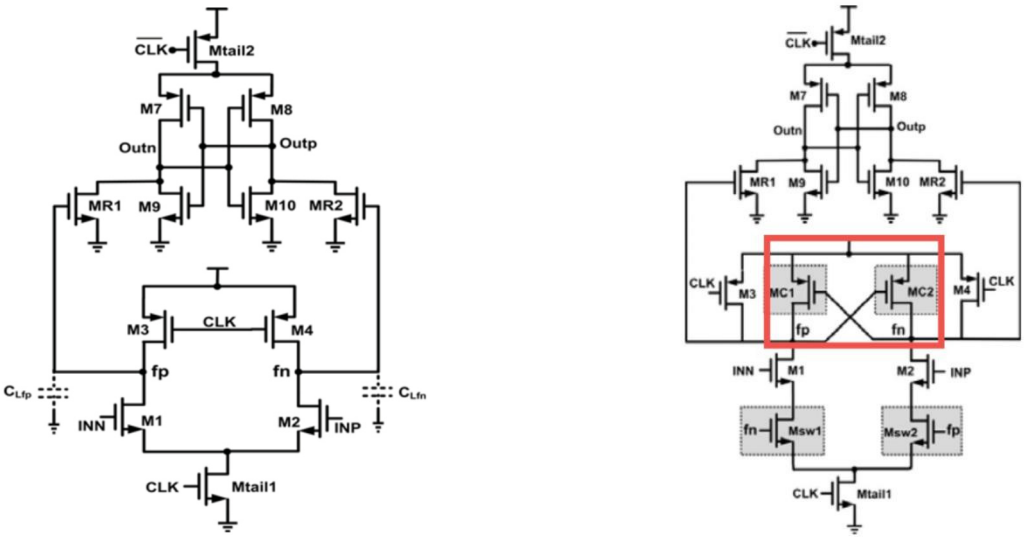



Fig.2 Double-tail dynamic comparator; (a) conventional double-tail dynamic comparator (b) proposed double-tail dynamic comparator

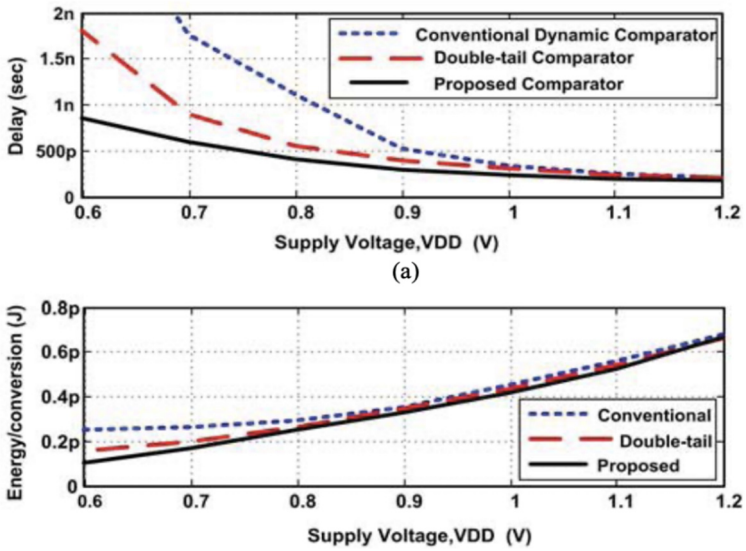



Fig.3 The post-layout simulation results of the delay and the energy per conversion

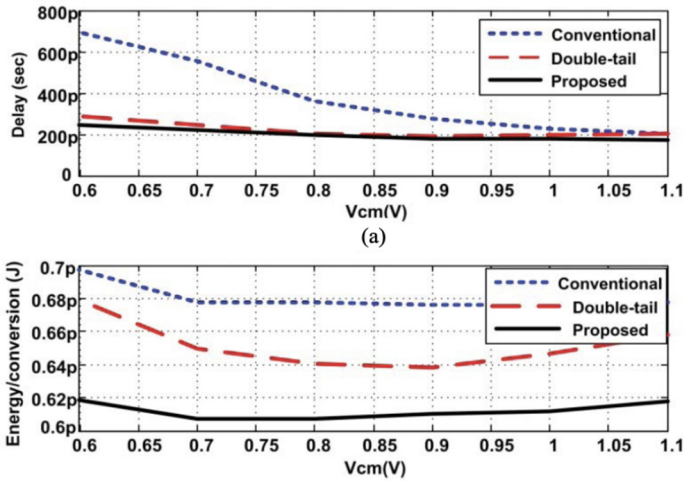



Fig.4 The simulated performance as a function of input common-voltage

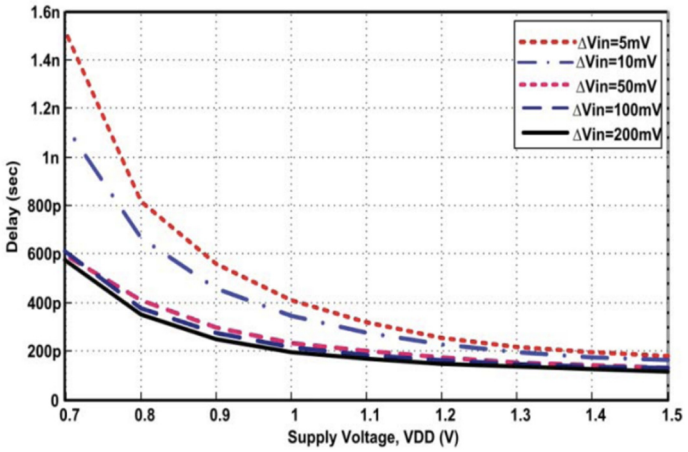



Fig.5 The dependence of the comparator delay on power supply level at various differential input voltages

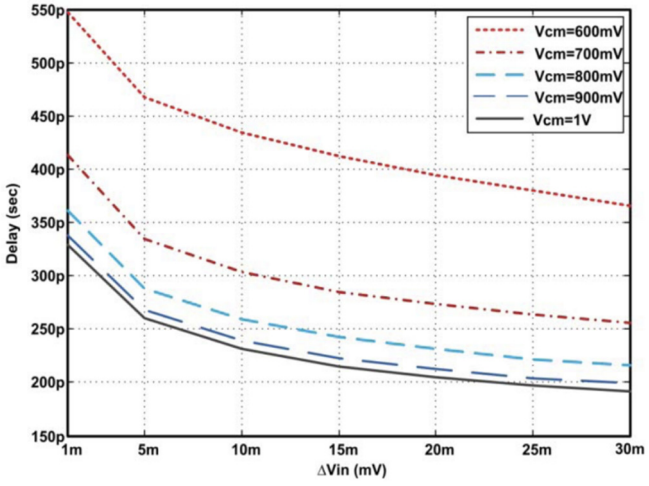



Fig.6 The simulated delay of the comparator versus differential input voltage under different conditions of input common-mode voltage at VDD=1.2V

*3.2. a low-power high-speed comparator for precise applications*

Ata Khorami and Mohammad Sharifkhani demonstrated a low-power comparator in which PMOS is provided as input of the latch stage. A cross-coupled circuit is used for the preamplifier.

Fig.7 is the circuit of the proposed comparator. During the reset phase, the clk, clkb1, and clkb2 are kept logic '1' to provide GND with output voltage which belongs to the preamplifier and latch [3]. During the evaluation phase, first, clk and clkb1 switch to logic '0' to open the preamplifier, which charges parasitic capacitors of O1+ and O1- nodes variously.

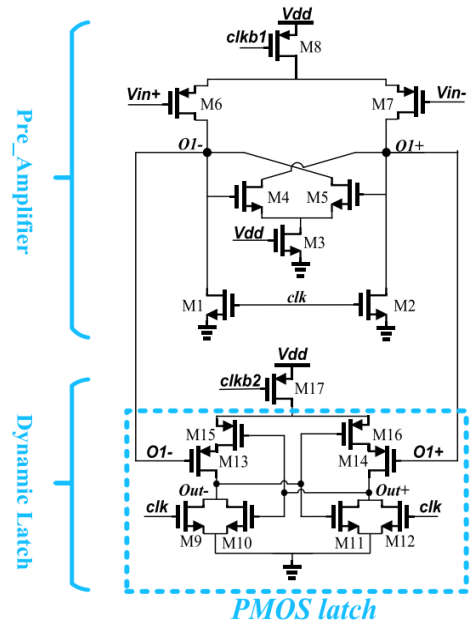



Fig.7 The circuit of the proposed comparator.

Referred to the proposed comparator, two innovations are a cross-coupled circuit (Fig.8) and a latch with input PMOS transistors(Fig.9). The following is a detailed description of these innovations.

Firstly, the innovation about the cross-coupled circuit is below. During the evaluation phase, due to M4 and M5 are largely in the subthreshold region, the differential voltage is slightly increasing by the cross-coupled circuit. And the common-mode voltage has a decline providing a significant drive to the input PMOS latch stage. The impact of the latch on the input-referred offset voltage is removed by growing Vidl [3]. Therefore, the cross-coupled circuit achieves enough delay to provide the minimum required preamplification to reach a given speed and latch offset elimination. Detailed data analysis of offset is below.

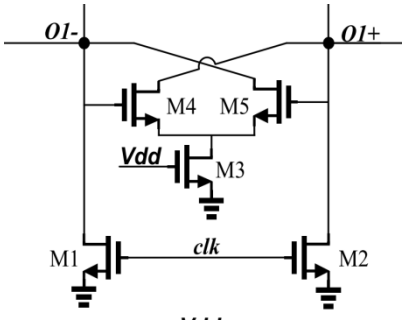



Fig.8 Failure characteristics of specimen SJ2

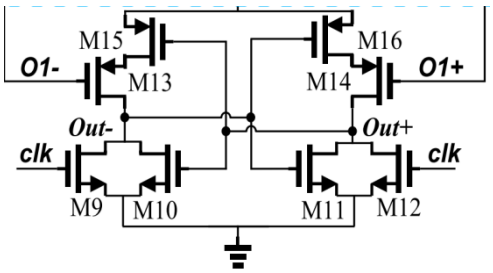



Fig.9 A latch with input PMOS transistors.

The latch delay is described as：

$$t_{latch} = \tau_{inv} \times \ln\left(\frac{VDD-GND}{V_{idl}}\right) + \frac{K_{latch}}{(VDD-V_{cml}-V_{thp})^2} \tag{4}$$

Vcml is the input common-mode voltage of latch (Vcml =(VO1++VO1-)/2). Vidl is the differential voltage of the latch (Vidl =VO1++VO1-). The two figures are all from the preamplifier stage. Then they can be figured in the following formulas

$$\begin{cases} V_{cml} = \frac{V_{O1+}+V_{O1-}}{2} = \frac{I\times\frac{t_{amp}}{C}}{1+\alpha\left(\frac{t_{amp}}{C}\right)}, I = I_1 + I_2 \\ V_{cml} = V_{O1+} - V_{O1-} = \frac{I\times\frac{t_{amp}}{C}}{1-\alpha\left(\frac{t_{amp}}{C}\right)}, I = I_2 - I_1 \end{cases} \tag{5}$$

Because the α term of the conventional comparator is equal to 0, the proposed method is bigger. Consequently, a lower Vcml and higher Vidl can be achieved. So, a fast speed is realistic according to formula (4).

To prove the results of derivations, this paper designs a sample of the proposed comparator to achieve an offset voltage with 2mV. Using the formula about the delay, Vcml and Vidl get an illustration (Fig.10) about simulation and analytical derivations in the delay of the proposed comparator versus Vcm, which verifies the analytical derivations doping out an exact delay.And the delay is stable in Vcm = 0.2v - 0.5v and Vcm = 1.0v - 1.4v ,in which the former is lower than latter. After that, a decreasing trend about the delay changing with Vid about simulation and analytical derivations when Vcm is equal to 1.1v can be concluded in Fig.11. According to the definition of offset voltage, if an input difference voltage of up to VOS is applied to the comparator, after amplified, VO1++VO1-. Therefore, Fig.12 illustrates the offset voltage versus Vcm about simulation and analytical derivations. The result is that the two lines almost coincide.

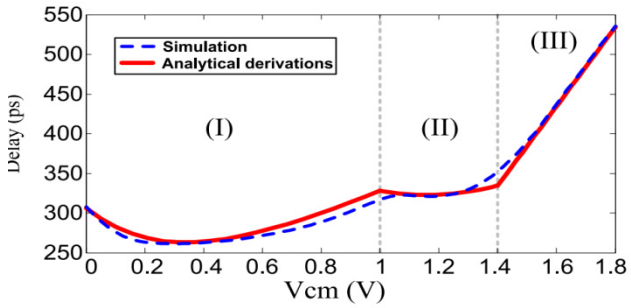



Fig.10 The delay of the proposed comparator changing with Vcm.

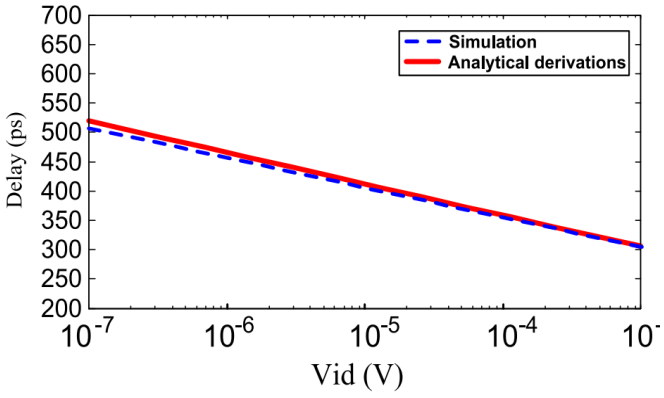



Fig.11 The delay changing with Vid.

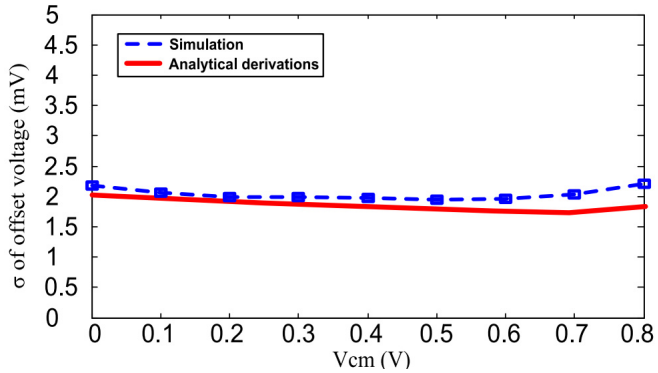



Fig.12 The offset voltage versus Vcm.

### *3.3. A Low-Power High-Speed Dynamic Comparator with a Transconductance-Enhanced Latching Stage*

YAO WANG et al. have presented a novel comparator with a latching stage using divided gate-biasing to provide a much faster speed and lower energy consumption.

Referred to the proposed comparator (as Fig.13 shown), in the reset phase, M0, M1, M4, and M5 are in the strong-inversion region compared with other cross-coupled structures that have two transistors in the cut-off region and the other two in the strong-inverter region.

A more effective transconductance can be concluded in the comparison phase, which has a higher regeneration speed. What's more, lower energy consumption is made because of a shorter metastable period in the inverters provided by a speed-up comparison.

According to the proposed comparator [4], a significant decline in delay and energy consumption will be achieved with the new latching stage. In fact, it can be achieved by improving the effective transconductance at the start of the comparison phase.

The latching delay of two cross-coupled inverters is given by

$$t_{latch} = \frac{C_{OUT}}{g_{m,eff}} \cdot \ln \frac{\Delta V_{out}}{\Delta V_0} = \frac{C_{OUT}}{g_{m,eff}} \cdot \ln \frac{V_{DD}/2}{\Delta V_0} \tag{6}$$

The total delay is described as

$$t_{latch} = \frac{V_{THN} C_{OUT} \cdot 2\mu_P C_{OX} \frac{W_1}{L_1}}{g_{m,eff}^2} = \frac{C_{OUT}}{g_{m,eff}} \cdot \ln \frac{V_{DD}/2}{\Delta V_0} \tag{7}$$

According to this formula, to lower tdelay, the higher gm and lower COUT should be chosen. The effect of VDD can't be concluded directly, so the result of the simulation would be represented later.

This paper cited postlayout simulated delay of comparators of [5] and [6] in contrast with proposed and conventional comparators and illustrated the relationship of postlayout simulated delay and Vcm (VDD=1.2v; Vid=50mv) in Fig.14.Additionally, Fig.15 shows the relationship between energy consumption and Vcm. Evidently, the delay, which is the minimum in the Vcm=1.0v, is slower than the proposed comparator by 150 ps. And the energy consumption, which is the minimum in the Vcm between 1.0v and 1.2v, is considerable to [6] but clearly lower than the conventional comparator and [5].

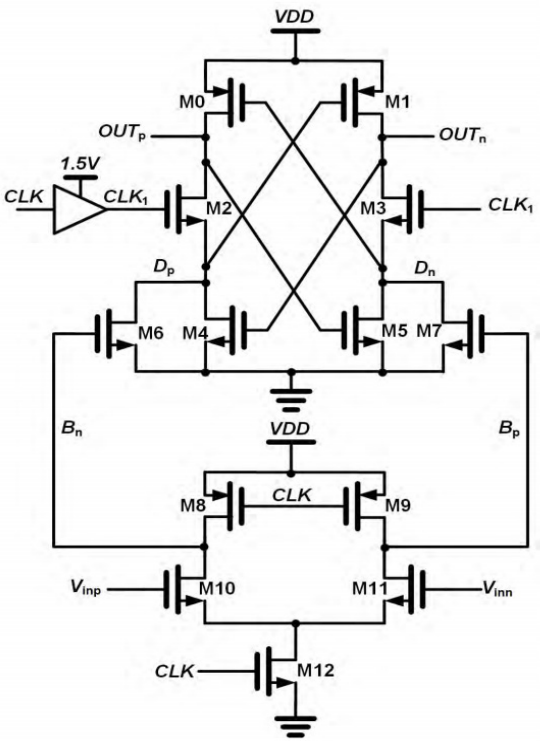



Fig.13. The proposed comparator

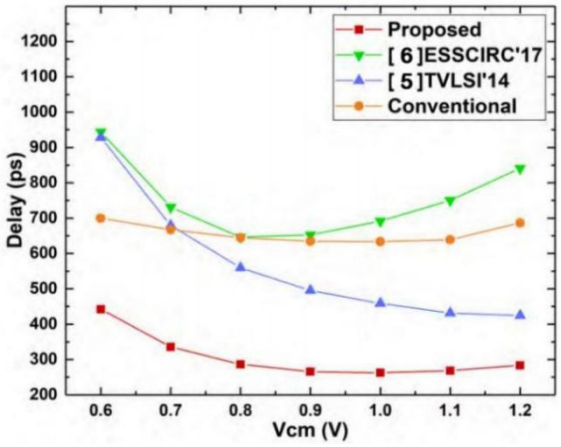



Fig.14. The relationship of postlayout simulated delay.

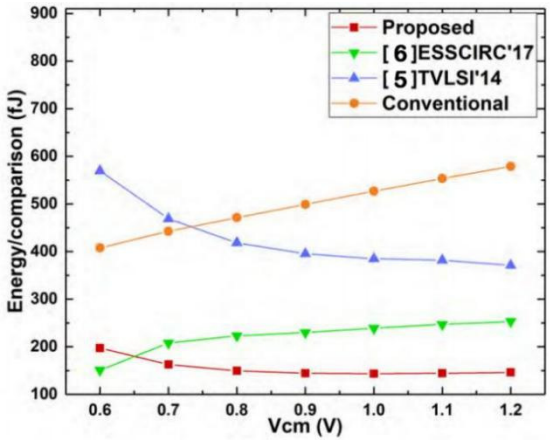



Fig.15. The relationship of energy consumption and Vcm

Simulation results in Fig.16 and Fig.17 show the delay and energy consumption versus VDD(Vid=50mv; Vcm=VDD-0.1v).Fig.16 shows that the proposed comparator is a better fit for low-voltage and low-power applications due to the greatly lower delay and energy consumption than other comparators. In this paper, the proposed chooses VDD=1.2v.

Based on the above, low delay and energy consumption can be achieved when VDD=1.2V. Therefore, Fig.4 illustrates the dependence of delay in the difference in input voltage (VDD=1.2v) and the multiple input common-mode voltage. For the multiple of input common-mode voltage ranging 0.7-1.1v, the delay remains stable and declines along with the decrease of the differential voltage.

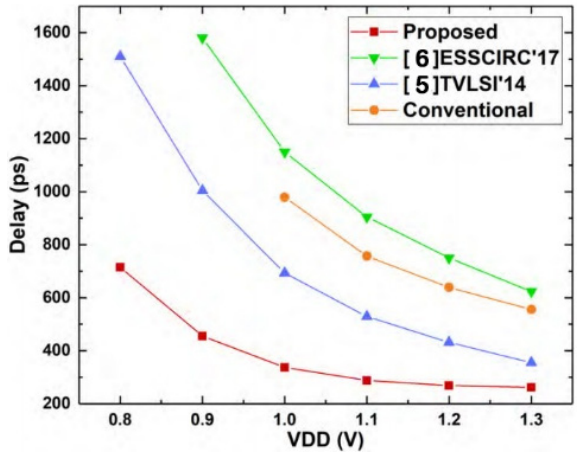



Fig.16 The delay versus VDD

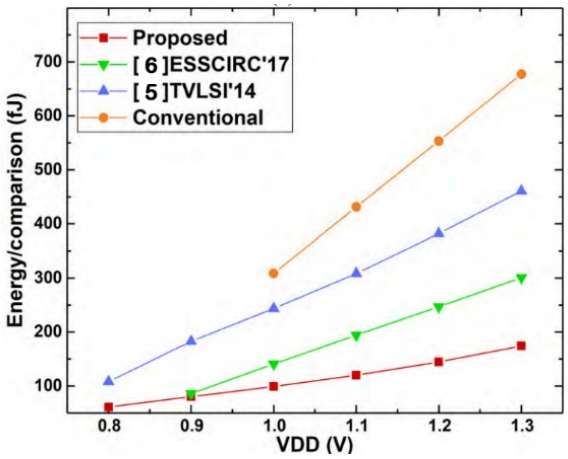



Fig.17 Energy consumption versus VDD

Based on the above, low delay and energy consumption can be achieved when VDD=1.2V. Therefore, Fig.18 illustrates the dependence of delay in the difference in input voltage (VDD=1.2v) and the multiple input common-mode voltage. For the multiple of input common-mode voltage ranging 0.7-1.1v, the delay remains stable and declines along with the decrease of the differential voltage.

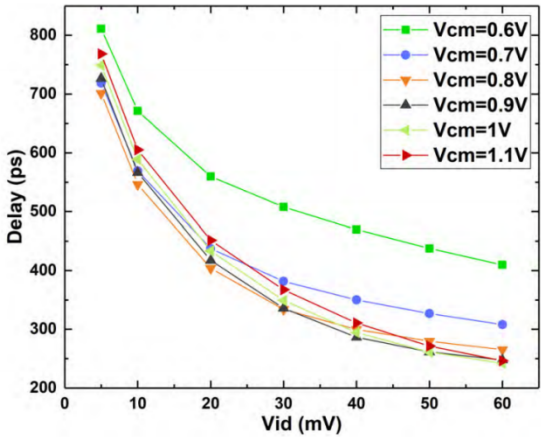



Fig.18 Post layout simulated delay versus Vid.

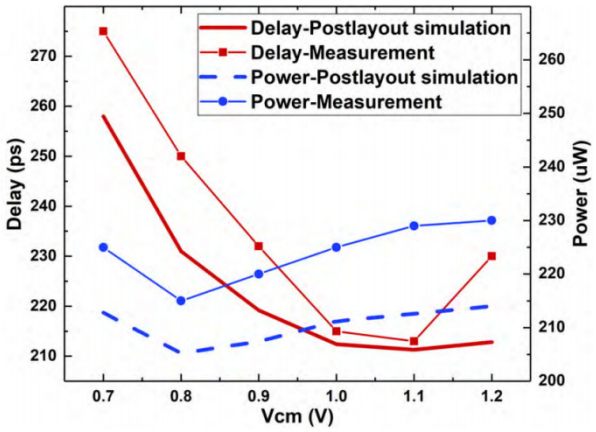



Fig.19 The delay and power versus Vcm.

The demonstration about the simulation and measurement of delay and power versus Vcm(Vid=0.1v, VDD=1.2v,f=2GHz) is represented in Fig.19. It can be concluded that the delay is under 275ps, and the consumption of power is about 225μW with the input common-mode voltage ranging 0.7-1.2v. The trend of experimental results is basically the same as the simulated results. But there is a constant error because of the methods and devices of measurement. In conclusion, such a high speed and low power consumption are realistic in the proposed comparator.

*3.4. a novel comparator with a charge pump based on the conventional Miyahara's comparator*

Haoyu Zhuang and his teammates design a voltage comparator 60% faster than the Miyahara's by using a charge pump in 2020.

The schematic of the conventional Miyahara's comparator is shown in Fig.20. It has three phases: the reset phase, the amplification phase, and the regeneration phase. The operation of the comparator is described as follows. DIP and DIN are reset to VDD in the reset phase, while OUTP, OUTN, QP, and QN are reset to GND. And in the amplification phase, DIP and DIN fall, while OUTP, OUTN, QP, and

QN rise. M10 and M11 are turned on in the regeneration phase so that the comparison result can be generated.

Based on the analysis, we can conclude that the input-referred noise can be reduced by increasing the input pair transconductance and the integration time [7]. So, new technology is applied to the conventional Miyahara's comparator, which can greatly improve the comparison speed and will not degrade the noise performance.

The proposed comparator based on the comparator above-mentioned is shown in Fig. 21. It just has one modification compared to the classic one, a charge pump connected to the VTOP. So, the VTOP is equal to VDD at CLK=0 and is slightly larger than VDD at CLK=1. Besides, the bulk of M6~M9 is also connected to the VTOP to make sure their bulk-source voltage is not negative. The operation of the proposed comparator is similar to Miyahara's comparator. In the reset phase, all the sources are reset. In the amplification phase, CLK's rise contributes to the rising of VTOP, which makes the second-stage amplification phase turn on earlier than conventional Miyahara's comparator, which helps accelerate the comparison speed of the proposed comparator.

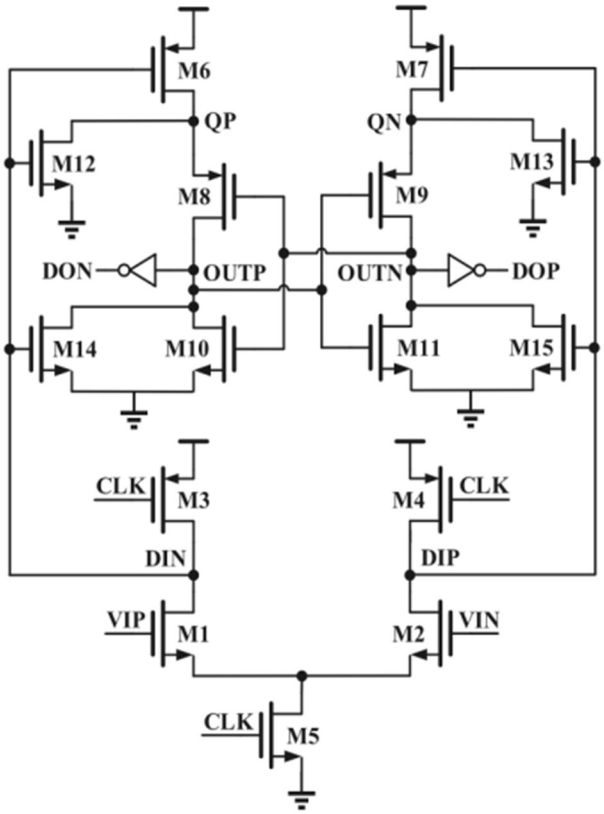



Fig.20 Miyahara's comparator

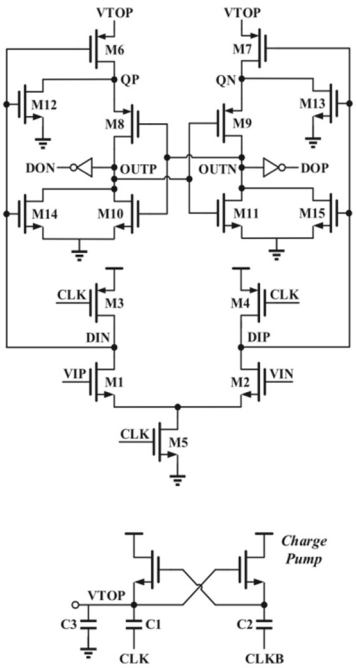


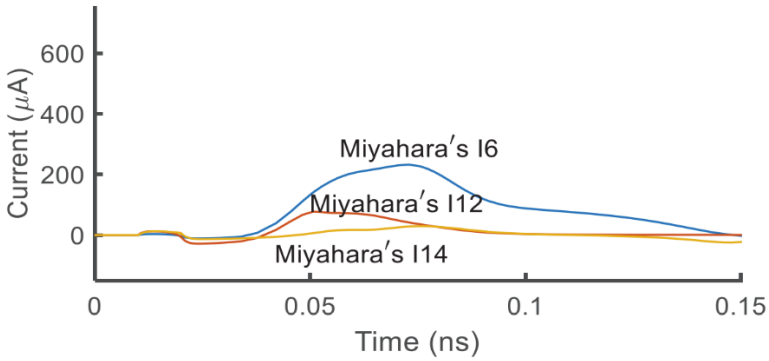

Fig.21 The novel comparator based on Miyahara's comparator

Meanwhile, the current at the beginning of the second-stage amplification is much larger than Miyahara's comparator. Fig. 22 displays the comparison of the current in both comparators. As can be seen, the current in the proposed comparator is about 3 times larger, which is caused by the earlier start of the second-stage amplification and the larger current in M12 and M13. The faster rise of OUTP and OUTN in the proposed comparator accelerates the comparison speed.

The larger current also increases the latch transconductance, which cancels out the penalty in the noise performance due to the reduced integration time caused by the earlier start of the second-stage amplification.

The proposed comparator is designed in the same as conventional Miyahara's comparator. Fig.23 shows the measured power consumption versus the differential input voltage. The conclusion is that the power of the proposed comparator is larger by 47% than Miyahara's comparator due to the larger voltage the proposed comparator works at.

Fig.24 shows the measured delay versus the differential input voltage and figures out that the delay of the proposed comparator is 60% smaller than Miyahara's comparator.



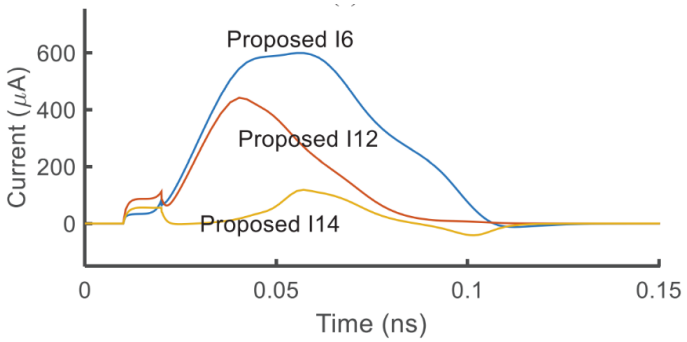



Fig.22 The comparison of the current in both of the comparators

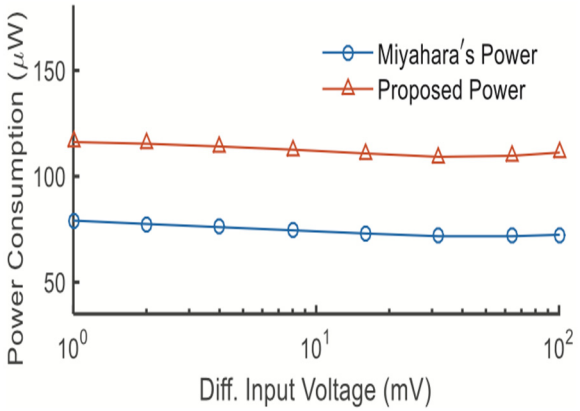



Fig.23Measured power consumption versus the differential input voltage

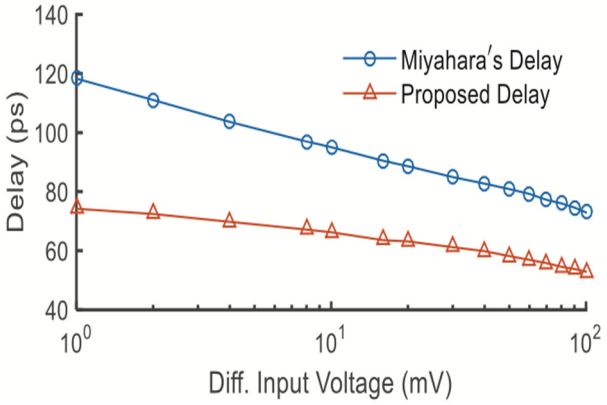



Fig.24 The measured delay versus the differential input voltage

Table.1 lists the process of the performance of the comparator. The delay and power consumption are greatly reduced, but the offset and kickback noise are almost remained unchanged. Under the 180nm technique, there are some different technologies. The new double-tail dynamic comparator designed in 2014 can reduce the power consumption and delay. The comparator in 2018 uses the input of the latch and the cross-coupled circuit while the comparator in 2019 uses the separated gate-biasing cross-coupled transistors to substitute the conventional cross-coupled inverter structure. It can be concluded that the delay [8] of 2014 is greater than that of 2019, the power consumption is much higher than that of 2019. Under the 40nm technique, it greatly increases the speed without needing extra calibration for

comparator offset. Through Table I, it can be found that the power consumption has been greatly reduced compared to the previous design. However, the optimization of the circuit still needs to consider some factors involved in the noise, delay, power, and offset voltage [9, 10].

Table.1 The performance of dynamic comparator

| Parameter | CDC | CDDC | 2014 | 2018 | 2019 | 2020 |
|---|---|---|---|---|---|---|
| CMOS technology （nm） | 180 | 180 | 180 | 180 | 180 | 40 |
| Supply voltage (V) | 0.8 | 0.6 | 1.2 | 1.1 | 1.2 | 0.5 |
| clock frequency (GHz) | 0.9 | 1.8 | 0.5 | 0.5 | 0.5 | 1 |
| Delay time (ps) | 940 | 358 | 550 | 370 | 268.6 | 84 |
| Offset (mv) | — | 7.91 | 7.8 | 2 | 7.3 | — |
| power consumption per conversion (μw) | — | — | 329 | 230 | 72.2 | 115 |
| kickback noise （mv） | 51.3 | 5.3 | 43 | — | — | — |

*CDC and CDD stand for Conventional Dynamic Comparator, Conventional Double-tail Dynamic Comparator, respectively

## 4. Conclusion

In summary, four dynamic comparators are given to improve circuit performance.

From the analytical expressions, a new dynamic comparator is proposed by Samaneh Babayan-Mashhadi, and the power consumption and delay time are significantly reduced. These are improvements to the circuit structure, thereby optimizing the performance of the comparators to a certain extent. The main idea of Ata Khorami and Mohammad Sharifkhani is PMOS transistors used at the input of the latch and the cross-coupled circuit to keep the common-mode voltage of the preamplifier outputs at a low level. Yao Wang put forwards separated gate-biasing cross-coupled transistors instead of the conventional cross-coupled inverter structure in the latching stage, significantly decreasing the delay and energy consumption.

And there is an innovation to optimize the comparator. Haoyu Zhuang designs an extra charge pump based on the classic Miyahara's two-stage comparator to improve voltage, decrease the delay, and not degrade the noise performance. But its comparator offset causes the offset of the entire SAR ADC.

Generally, through the study of four papers, we can have more ways to deal with design problems in future design work. However, the noise is still a problem. Therefore, many critical factors are considered when designing dynamic comparators.

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