A Review on SAR ADC’s

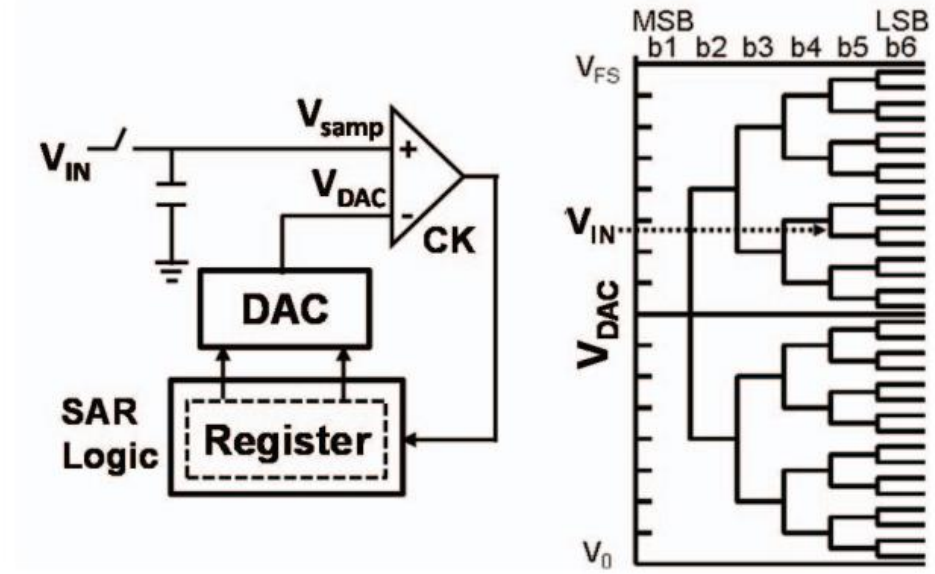


Fig. 1. SAR-ADC diagram and its time trellis operation

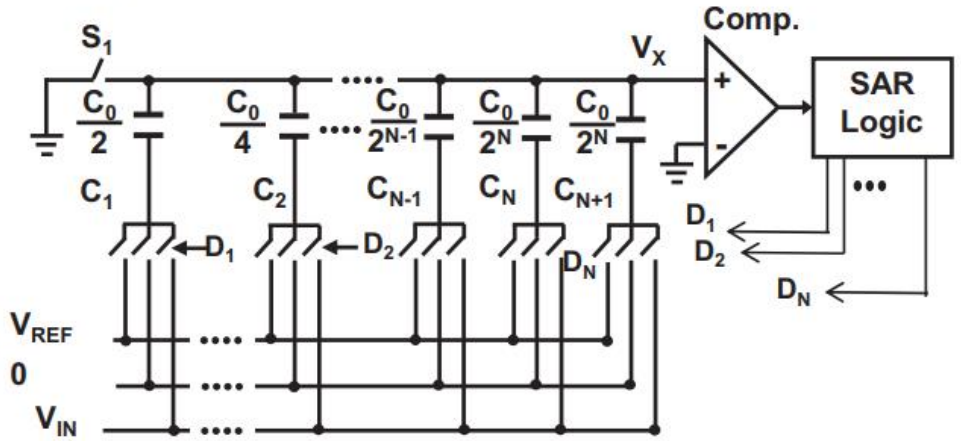


Fig. 2. Charge redistribution SAR-ADC

ADVANTAGES:

(+)Low power consumption!

(+)MOM capacitor

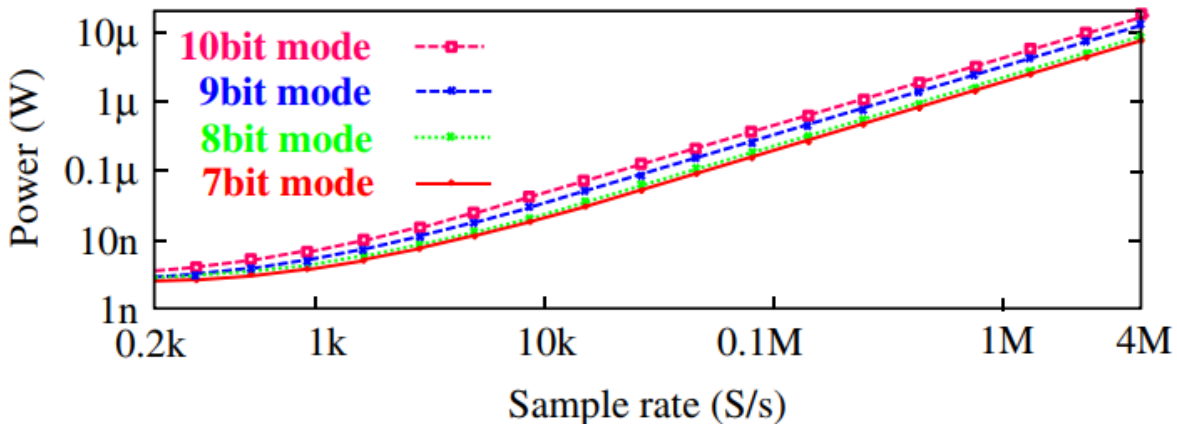
(Good Layout density & Matching accuracy [10-bit])

DISADVANTAGES:

(-)Higher conversion time (n+2 or 3 cycles).

(-)Limited precision

(Comparator Decision Error, Noise and Capacitor/DAC Matching)



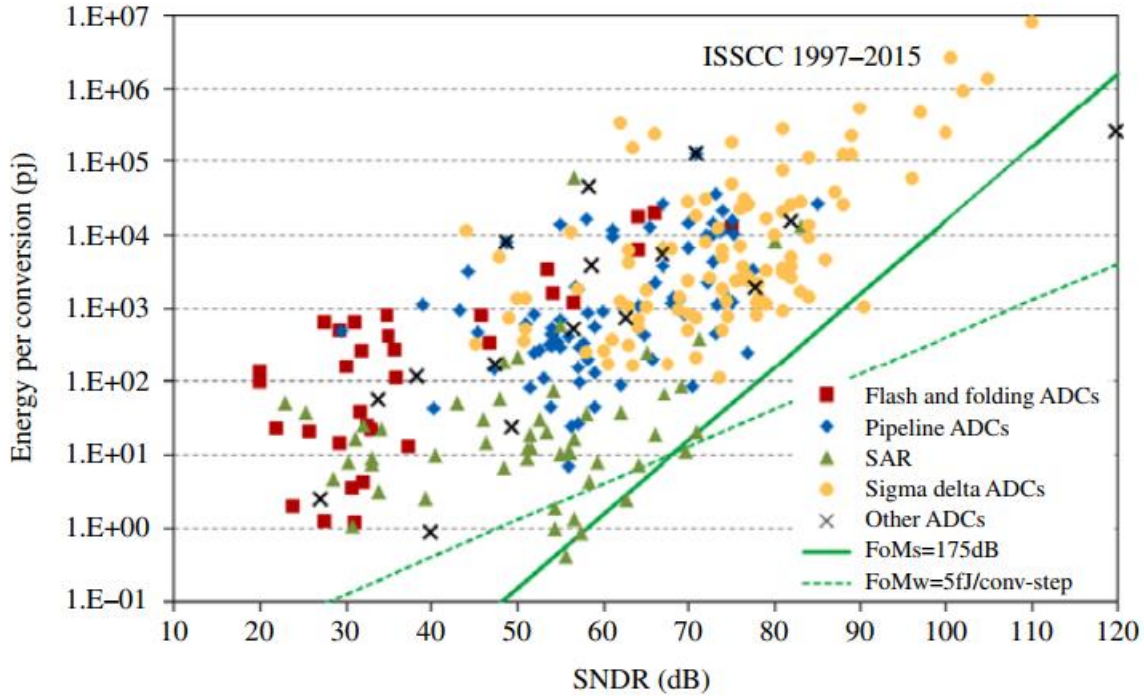
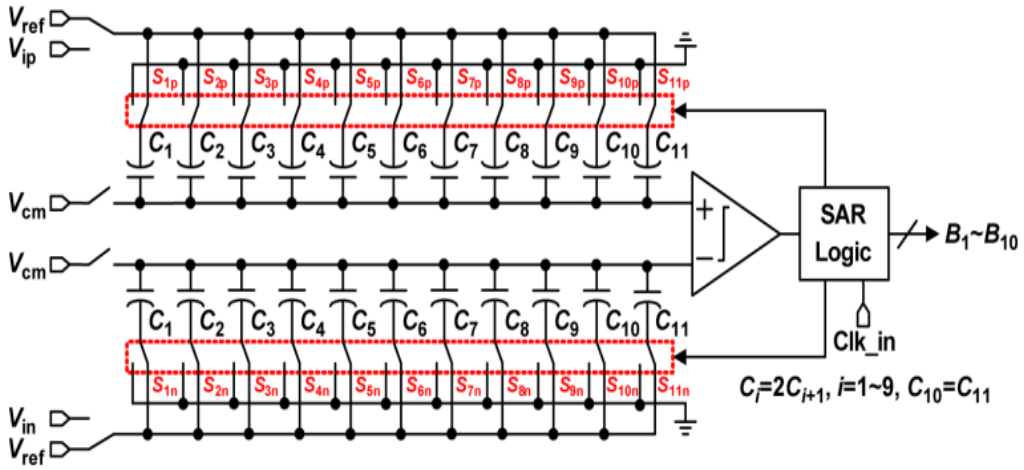


Fig. 3. Power efficiency (*P/fs*) vs. SNDR with ADC architecture. (Modified from B. Murmann "ADC Performance Survey 1997-2015," [Online] http://web.stanford.edu/~murmann/adcsurvey.html)

Ref: - https://github.com/bmurmann/ADC-survey

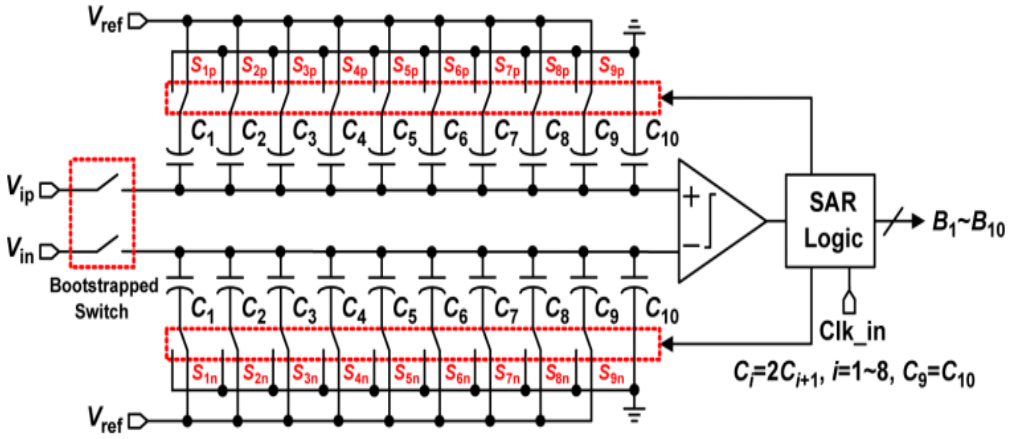


Conventional Switching SAR ADC

-> At sampling phase bottom plate of capacitor Charged to Vip/in. Top plates reset to Vcm.

-> During Comparison, C1 switched to Vref and rest to Gnd. If Vip > Vin, B1 =1 else B1=0.

-> Similarly other comparisons are performed.



Monotonic Switching SAR ADC

-> Switching procedure can be upwards or Downwards.

-> Samples Vip/in onto top plate of capacitor via switches. Bottom plates are reset to Vref.

-> During Comparison, the capacitor on higher Potential is switched to gnd.

-> Similarly other comparisons are performed.

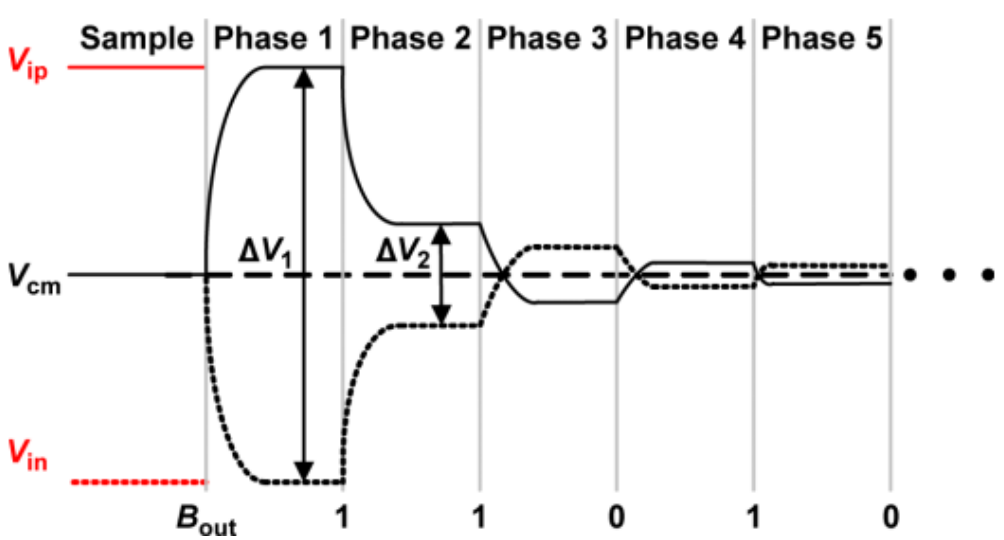


Fig. Conventional Switching Procedure

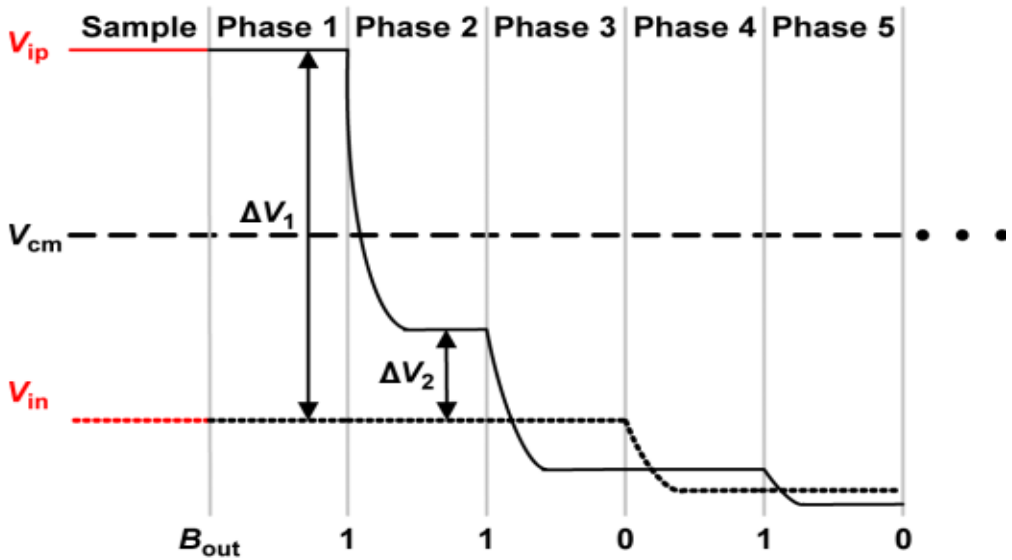


Fig. Monotonic Switching Procedure

Operation speed improvement

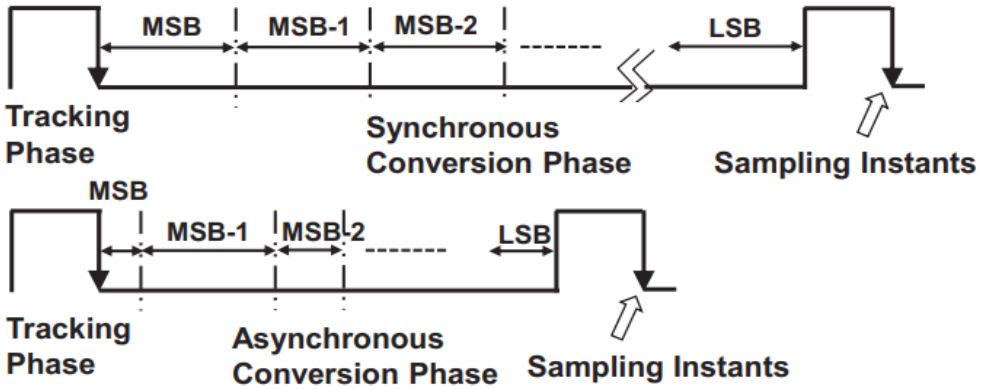


Fig. 4. Asynchronous SAR-ADC control (Proposed,2006)

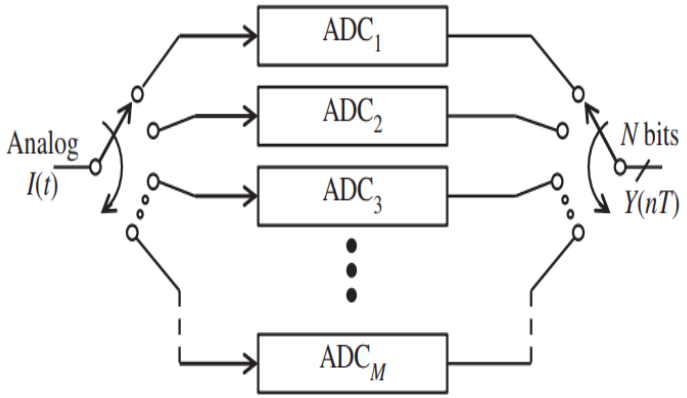


Fig.5. Time Interleaving (Use of Sub SAR ADC's)

Difficulty- Performance of interleaving.
(offset, gain & timing mismatch)

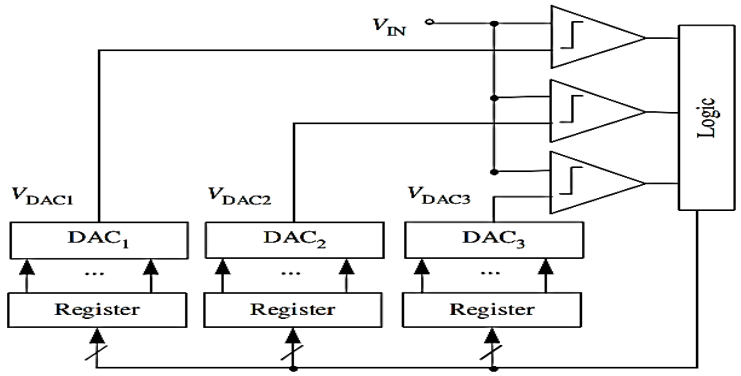


Fig. 6. 2-Bit per cycle conversion SAR ADC (Multi cycle)

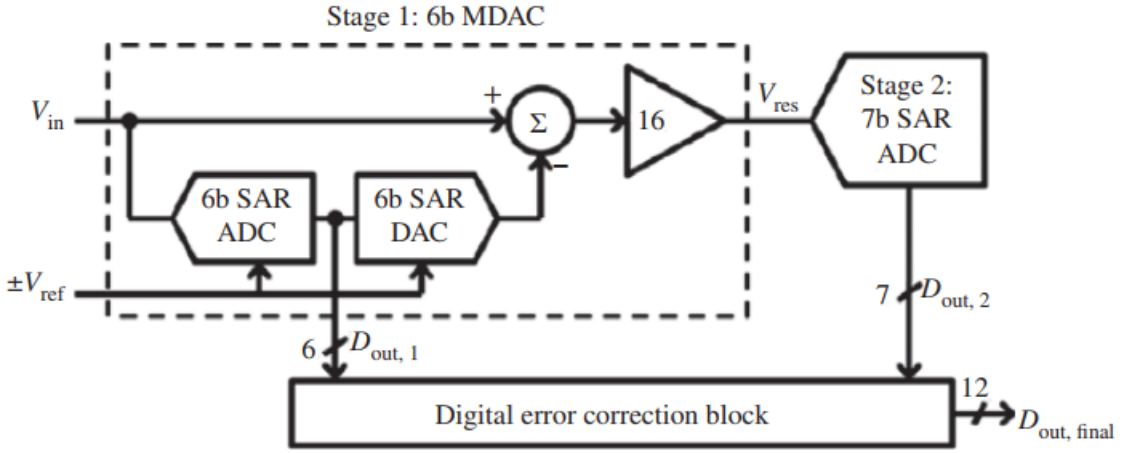


Fig. 7. Pipelined SAR ADC (Sub-ranging)

*Ref- RECENT PROGRESS ON CMOS SUCCESSIVE APPROXIMATION ADCS. **(MATSUURA)**

Limited Resolution & Precision improvement (Nyquist sampling)

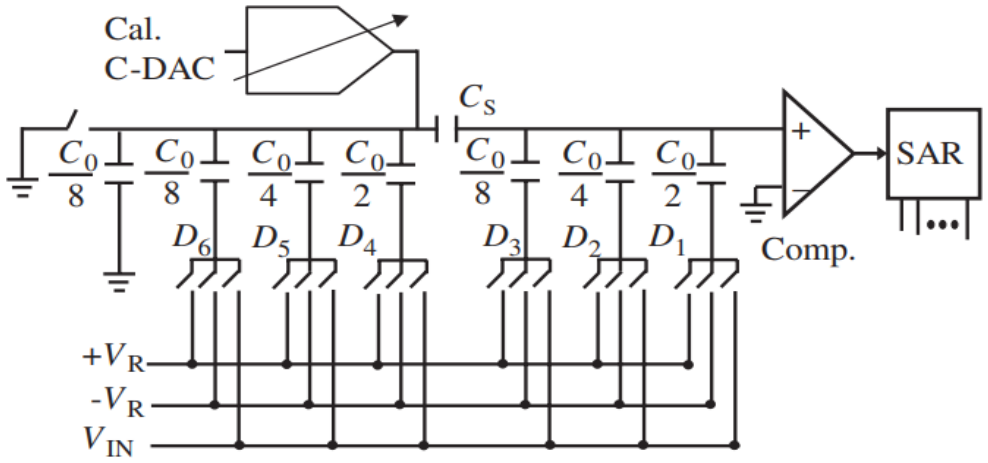


Fig. 8. Split Capacitor + Error Correction!

Parasitics causes mismatches to binary weights

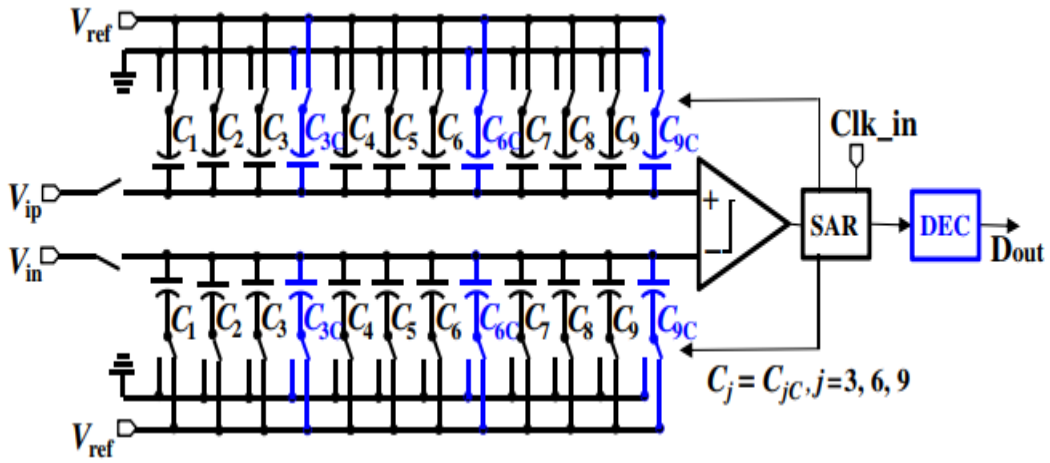


Fig.9. Binary Scale Redundant Capacitor Array + DEC

Accounts only comp. decision errors (Not mismatch errors)

Limited Resolution & Precision improvement (By Oversampling)

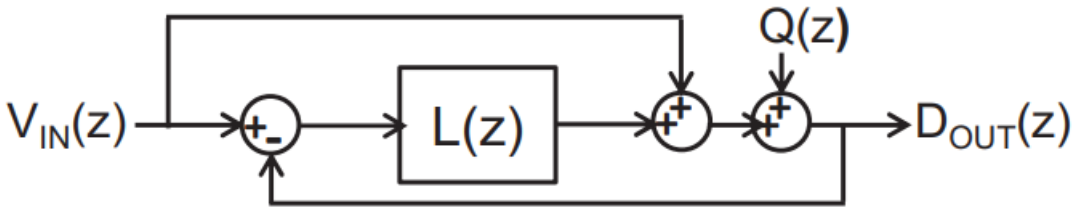
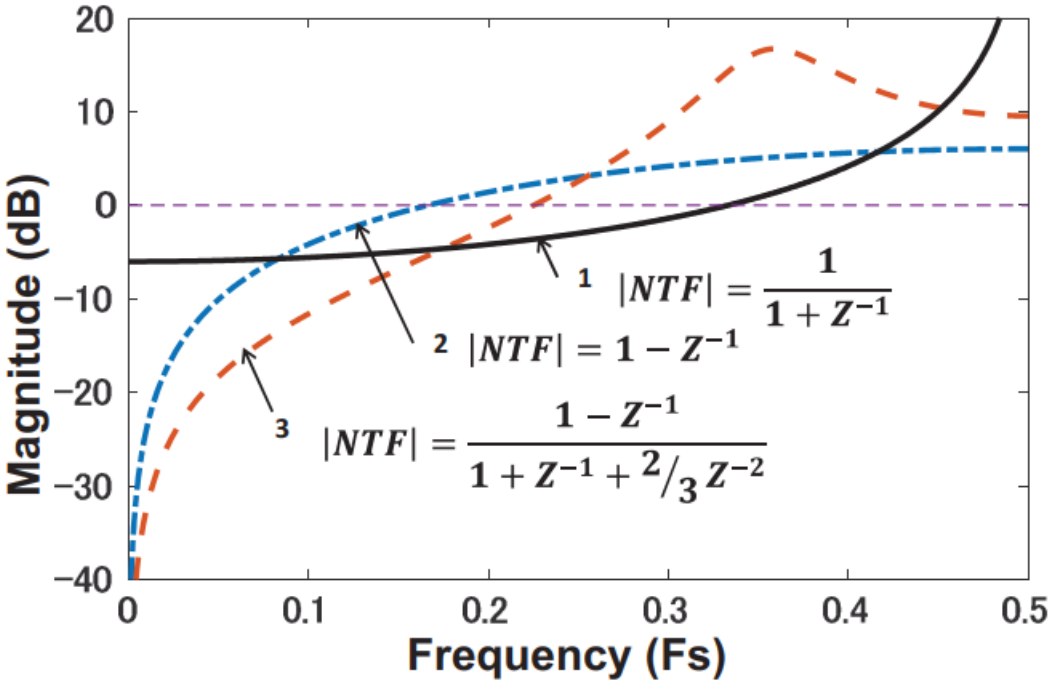
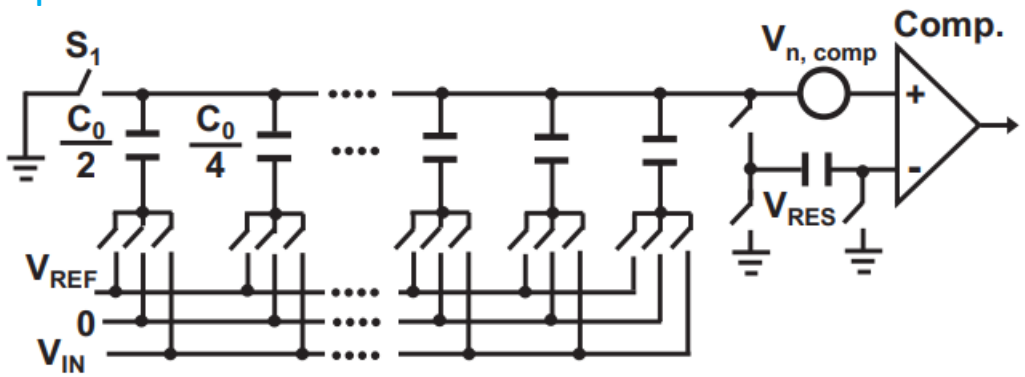


Fig. 10. SFD of Noise-shaping SAR ADC



*Ref -J.A. Fredenberg & Y.-S. Shu papers (ISSCC)

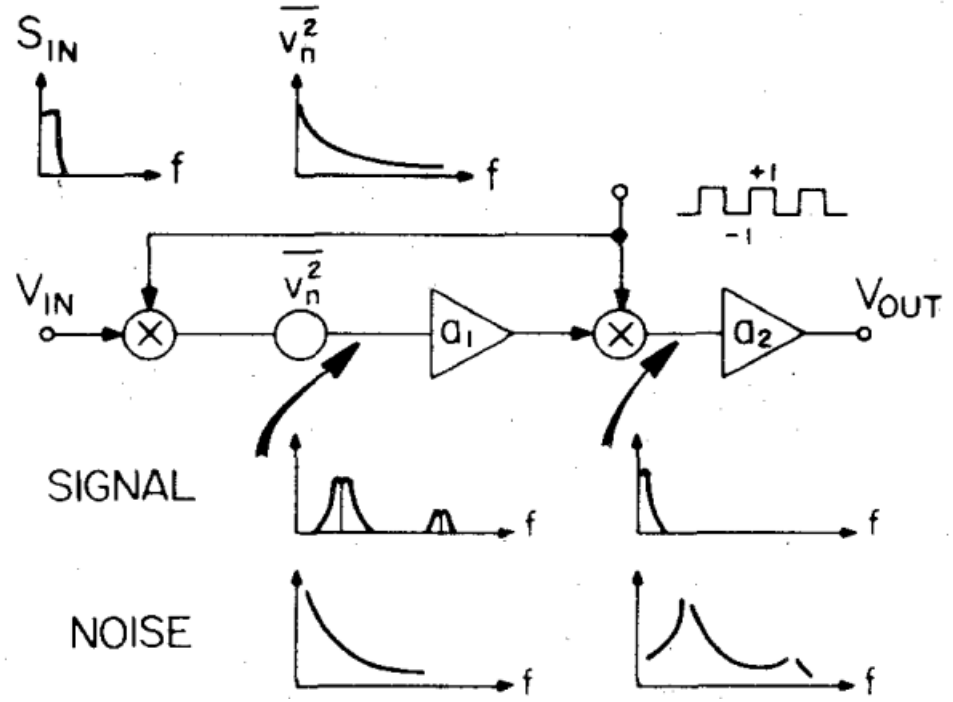
(+)Good for suppressing comparator Thermal and Quantization noise by distributing it over wider spectrum.



1) Delayed residue ($L(Z)= z^{-1}$)
2) Integrator ($L(Z)= z^{-1}/(1-z^{-1})$)
3) FIR-IIR filter

Limited Resolution & Precision improvement (By Oversampling)

modulate harmonic distortion and flicker noise out of signal bandwidth



Ref- A Low-Noise Chopper-Stabilized Differential Switched-Capacitor Filtering Technique (P.R. Gray,1982)

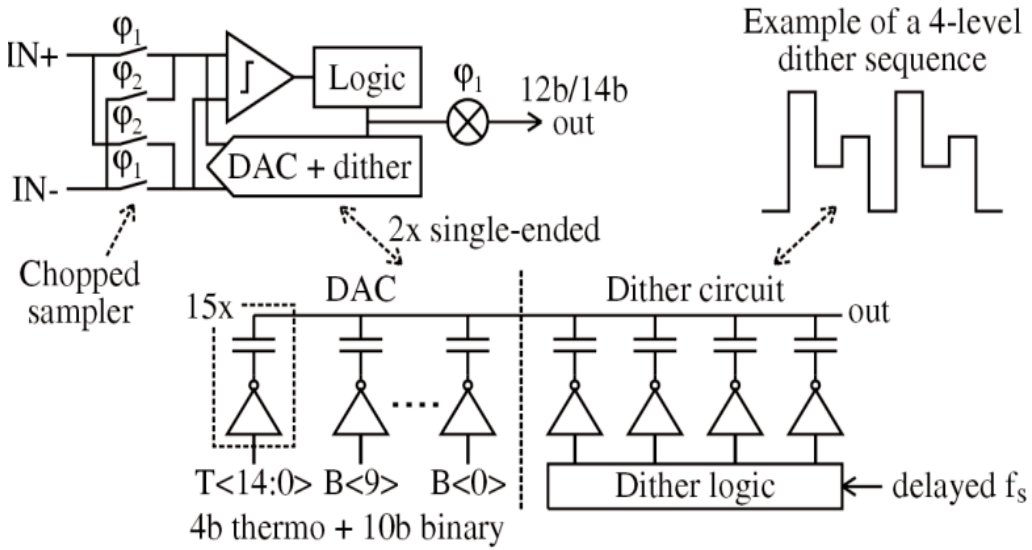


Fig. 11. Chopper Stabilization and Dither Logic*

Dithering randomizes Q.N. making it more uniform

Here it provides SNDR improvement (from mismatch!)

*Ref - **An Oversampled 12/14b SAR ADC with Noise Reduction and Linearity Enhancements Achieving up to 79.1dB SNDR (ISSCC, Pieter Harpe)**

Limited Resolution & Precision improvement (By Oversampling)

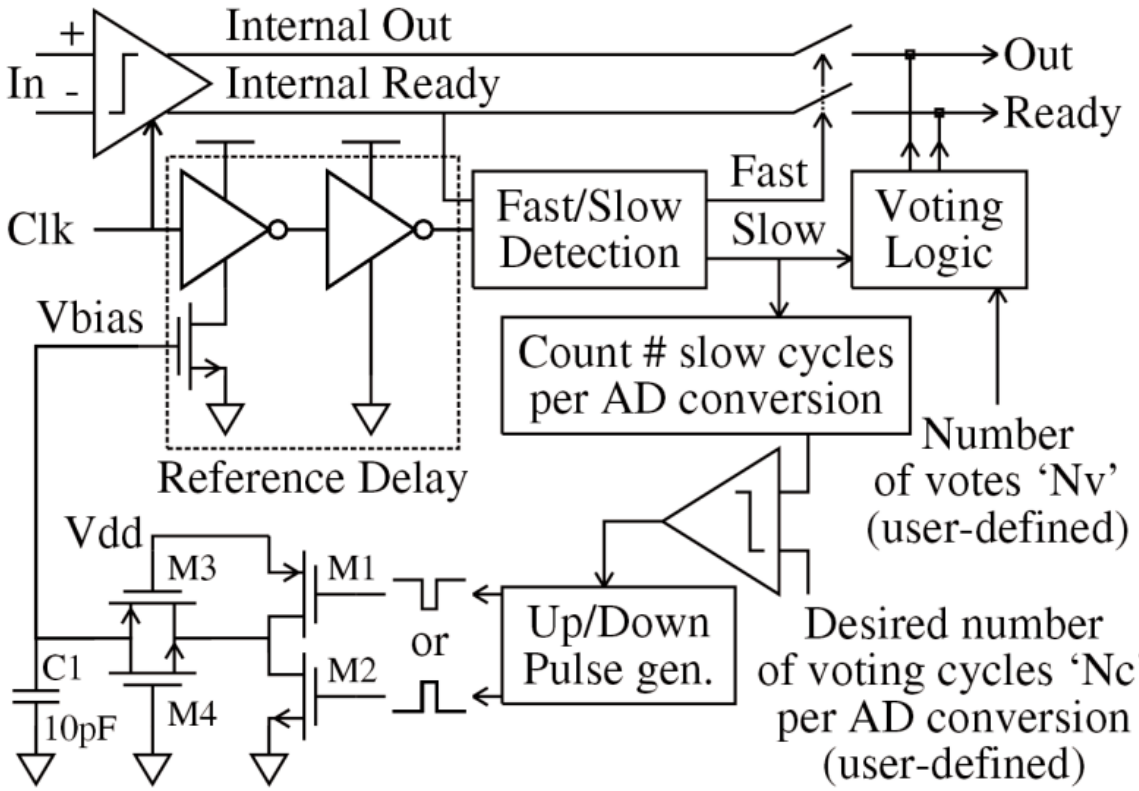


Fig. 12. CL programmable Data Driven Noise reduction (DDNR) Technique

*Ref - **An Oversampled 12/14b SAR ADC with Noise Reduction and Linearity Enhancements Achieving up to 79.1dB SNDR (ISSCC, Pieter Harpe)**

Limited Resolution & Precision improvement (By Oversampling)

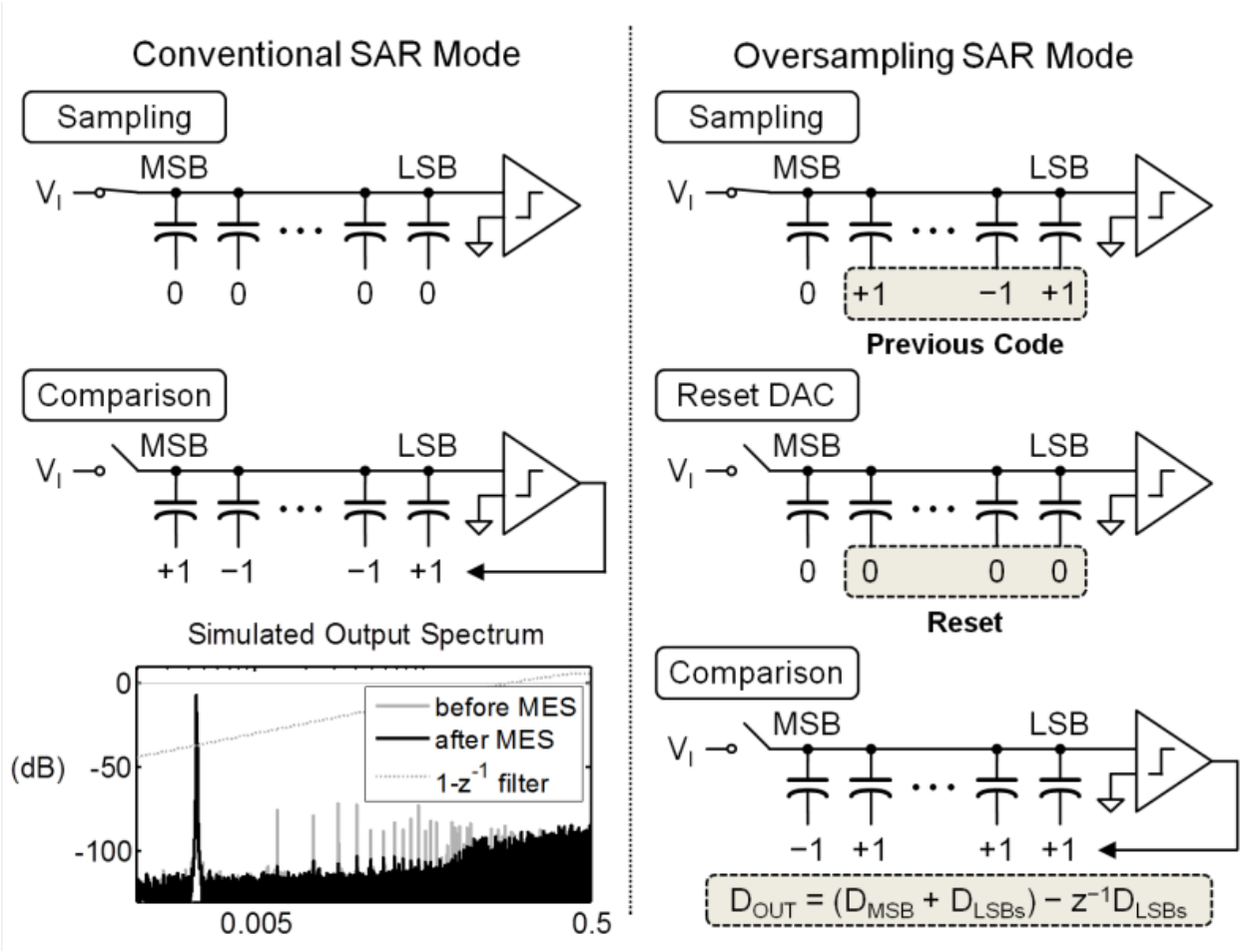


Fig. 13. DAC Mismatch Error Shaping (MES)

(-) input range reduction (DR reduced by 6dB)

Need for i/p range compensation techniques

-> DWA
-> Prediction
-> Detection (**Analog,2023 P. Harpe**)

*Ref - **An Oversampling SAR ADC with DAC Mismatch Error Shaping Achieving 105dB SFDR and 101dB SNDR over 1kHz BW in 55nm CMOS (Y.-S. Shu)**

Current Trends:-

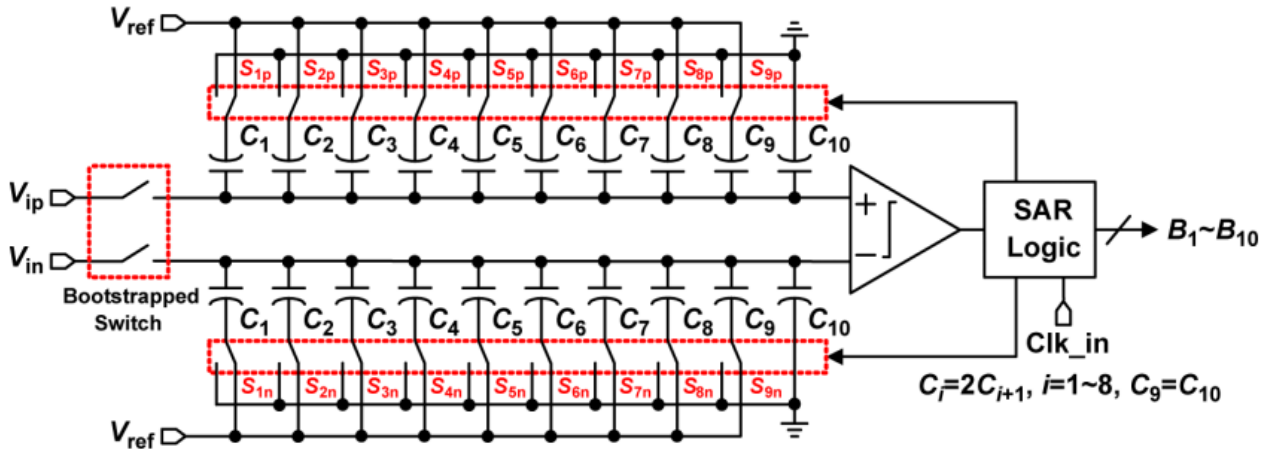
-> Mixing and matching with improvements of techniques discussed so far.

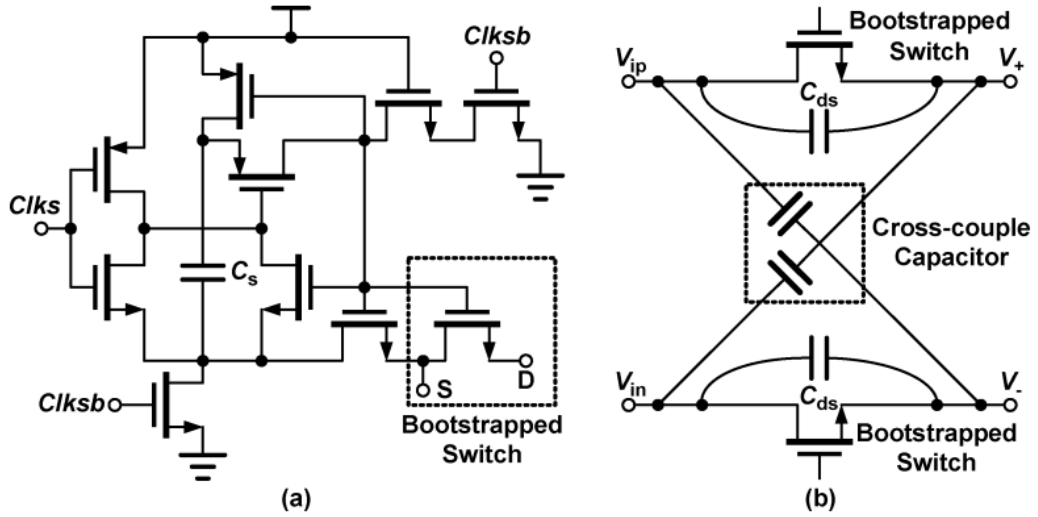
A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure

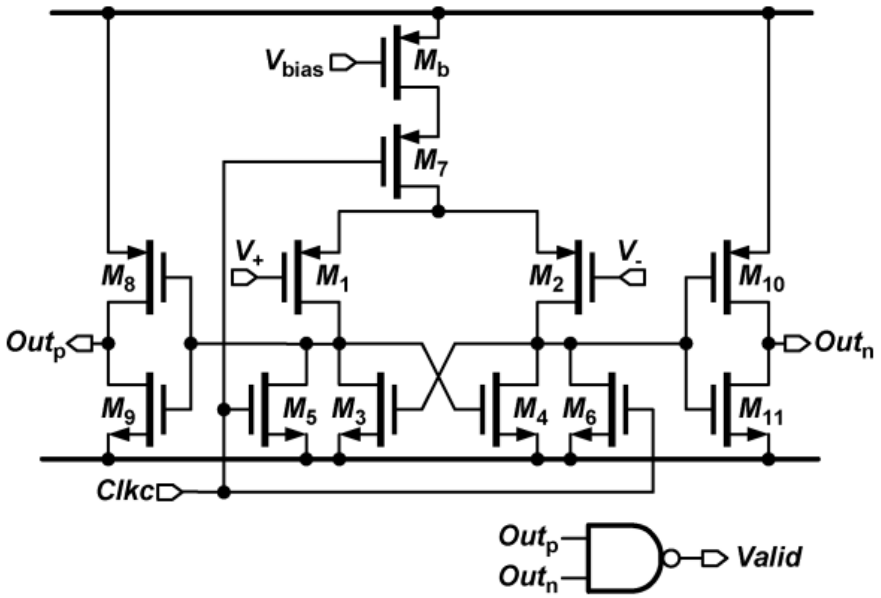
Chun-Cheng Liu, *Student Member, IEEE*, Soon-Jyh Chang, *Member, IEEE*,
Guan-Ying Huang, *Student Member, IEEE*, and Ying-Zu Lin, *Student Member, IEEE*

Building Blocks

- Bootstrapped Switches
- Comparator
- Control Logic
- DAC Capacitor Array







Bootstrapped Switch

-> constant VGS (turn on)

(Eliminates Sampling distortion)

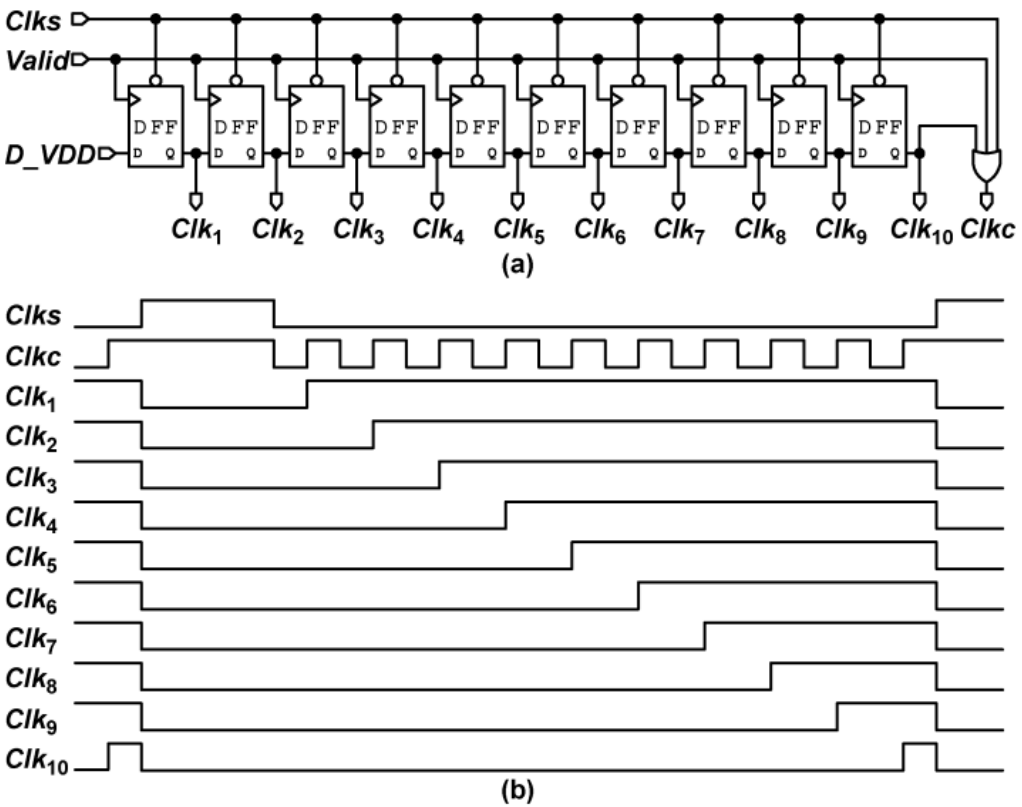
-> reduces effect of Capacitive Coupling(turn off)

Dynamic Comparator

-> Clkc low (compares)

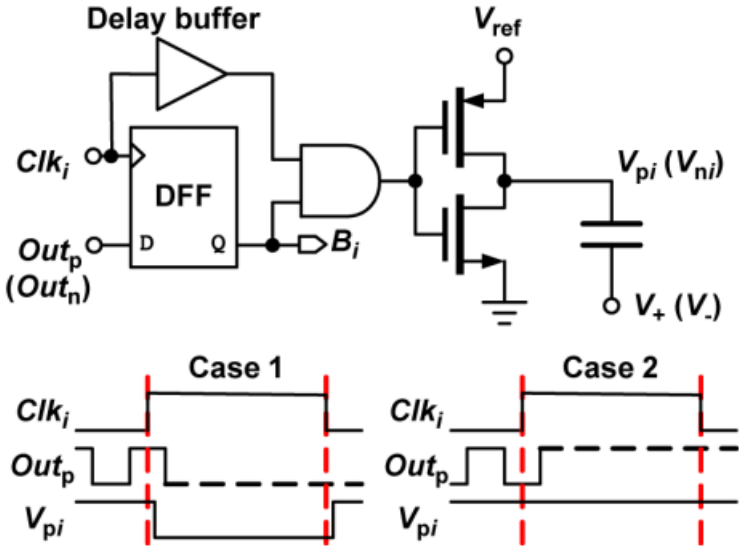
-> Clkc high (o/p's reset to High)

-> Generates a Valid signal



Control signals

Asynchronous Control signal Generation



DAC Control Logic

-> At ↑edge (clk_i), sampling of comparator o/p

-> If O/p is High Cap_i switched from VREF to gnd and vice-versa.

-> At ↓edge(clk_i) all Cap's are reconnected to VREF.