An Ultra-Low Power High-Order Temperature-Compensated CMOS Voltage Reference

Arthur Campos de Oliveira[1,*], David Cordova[2,†], Hamilton Klimach[1,‡] and Sergio Bampi[1,§]
[1]Federal University of Rio Grande do Sul, Porto Alegre, Brazil
[2]IMS Laboratory, Bordeaux, France
[*]oliveira.arthurc@gmail.com, [†]david.cordova@ims-bordeaux.fr, [‡]hamilton.klimach@ufrgs.br, [§]bampi@inf.ufrgs.br

***Abstract*—This work presents an ultra-low power low-voltage high-order temperature-compensated voltage reference. The proposed circuit is based on the self-cascode MOSFET (SCM) and explores the dependence of the threshold voltage (V_T) with the transistor dimensions. The SCM is biased by the leakage current of a zero-V_T transistor for PSRR improvement. The proposed circuit is composed only of 3 transistors. The high-order temperature compensation is achieved through a bulk-driven scheme. Additionally, the proposed high-order compensation also attenuates the mismatch variability of the voltage reference. Post-layout simulation results for a standard 130 nm CMOS process are presented. A voltage reference of 90.5 mV with a 1 ppm/°C temperature coefficient (TC) is achieved at typical corner. The circuit can operate at a minimum supply voltage as low as 0.3 V while consuming 43.7 pW at room temperature.**

***Keywords*—Voltage reference, high-order, subthreshold circuit, picowatt, ultra-low power, ultra-low voltage.**

I. Introduction

A voltage reference is a circuit responsible for providing at its output voltage that is almost independent of process, supply voltage and temperature variations. Since its first practical implementation, several other structures were proposed [1]–[7]. Traditional bandgap references present the adequate performance for many applications, but their power consumption usually is at µW range, where today's Wireless Sensor Networks (WSNs) requirements are at nW to pW range [8].

A common approach to achieve low-power operation is to use devices with different threshold voltages (V_T) biased in the subthreshold region to obtain at the output a reference that is proportional to their V_T difference [1], [6], [7]. However, this leads to a large spread of both voltage reference and TC values due to the different doping process of distinct threshold devices.

For this reason, in this work, we explore the dependence of V_T with respect to transistor dimensions [2]–[4] to achieve distinct V_T using the same type of devices. High-order temperature compensation is achieved by feeding back the voltages through their bulk terminals. This approach also attenuates the mismatch variability of the voltage reference. The proposed high-order 3-Transistor voltage reference can operate at a minimum supply voltage of 0.3 V while consuming 43.7 pW at room temperature and achieves a TC of only 1 ppm/°C.

The rest of the paper is organized as follows: Section II presents the circuit description. Section III describes the design methodology of the SCM and the proposed scheme for mismatch variability attenuation. The post-layout simulation results are presented in Section IV. Finally, Section V presents the conclusions.

II. Circuit Description

The schematics of the proposed 3-Transistor voltage reference is shown in Fig. 1(a). The three transistors that compose the circuit are operating in weak inversion. Transistors M_1 and M_2 are triple-well devices (isolated bulk) and form the SCM, and M_3 is a zero-V_T transistor which serves as current source biasing the SCM with its leakage current. Distinct V_T of the SCM using the same type of transistors are achieved through the dependence of V_T with the transistor dimensions. Therefore, a voltage reference that is the weighted difference between M_1 and M_2 V_T's is obtained. High-order temperature compensation is achieved by feeding back V_X and V_{REF} voltages through the bulk terminals of M_1 and M_2.

According to the Unified Current Control Model (UICM) [9], the drain current can be described as function of a forward (I_F) and a reverse (I_R) current

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{1}$$

where $I_S = I_{SQ}\mathrm{S}$, S is the ratio of the width (W) and channel length (L) of the transistor. i_f and i_r are the forward and reverse normalized currents or inversion coefficients, and $I_{SQ} = \mu C'_{ox} n \frac{\phi_t^2}{2}$ is the specific current, which is process related, where n represents the subthreshold slope factor, C'_{ox} is the gate capacitance per unit area, and $\phi_t = kT/q$ is the thermal voltage. The relationship between the normalized currents and voltages is given by

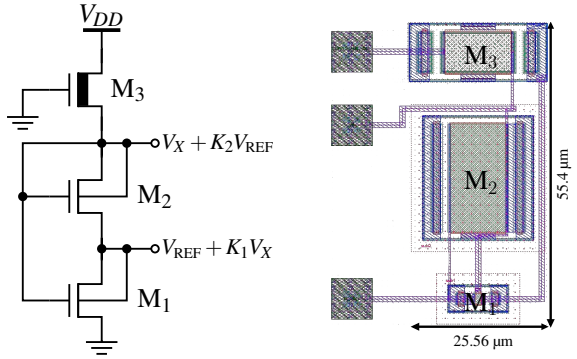
$$\frac{V_G - V_T - nV_{S(D)}}{n\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{2}$$

where V_G, V_S and V_D are the gate, source and drain voltages referenced to the bulk terminal. V_T is the threshold voltage.

From expressions (1) and (2), the drain current of the NMOS transistor operating in WI ($i_f \ll 1$) is given by

$$I_D = 2eI_S \exp\left(\frac{V_G - V_T}{n\phi_t}\right)\left[\exp\left(\frac{-V_S}{\phi_t}\right) - \exp\left(\frac{-V_D}{\phi_t}\right)\right] \tag{3}$$

where for $V_D \geq 3 \sim 4\phi_t$ the drain current becomes almost independent of the drain voltage.



(a) (b)

Fig. 1. Schematics of the proposed circuit (a) its layout (b).

Considering that all transistors in Fig. 1(a) operate in weak inversion ($i_f \ll 1$), are saturated ($i_r = 0$) and $V_{DS} \geq 3 \sim 4\phi_t$, their drain currents are given by

$$I_{D1} = 2eI_{S1}\exp\left(\frac{V_X - V_{T1} + V_{REF}(n_1 - 1)}{n_1\phi_t}\right) \quad (4)$$

$$I_{D2} = 2eI_{S2}\exp\left(\frac{n_2V_X - V_{T2} - n_2V_{REF}}{n_2\phi_t}\right) \quad (5)$$

$$I_{D3} = 2eI_{S3}\exp\left(\frac{-n_3V_X - V_{T3}}{n_3\phi_t}\right) \quad (6)$$

V_{REF} is mainly defined by transistors M_1 and M_2. Since $I_{D1} = I_{D2}$ and $n_1 \approx n_2 \approx n$, V_{REF} is given by

$$V_{REF} = \frac{1}{2n-1}\left[V_{T1} - V_{T2} + (n-1)V_X + n\phi_t \ln\left(\frac{I_{S2}}{I_{S1}}\right)\right] \quad (7)$$

Transistors M_1 and M_3 form the equivalent of a 2-Transistor voltage reference [1], which means that the voltage V_X will be given by their gate-to-source voltage difference. Through $I_{D1} = I_{D3}$:

$$V_X = \frac{n_3V_{T1} - n_1V_{T3}}{n_1n_3 + n_3} + \left(\frac{n_1 - 1}{n_1 + 1}\right)V_{REF} + \left(\frac{n_1}{n_1 + 1}\right)\phi_t \ln\left(\frac{I_{S3}}{I_{S1}}\right) \quad (8)$$

From (7) and (8) one can see that the high-order compensation is achieved by feeding back both V_{REF} and V_X through the bulk terminals of M_1 and M_2, making possible to achieve high-order compensation to either V_{REF} or V_X voltages. Due their magnitude, one can conclude that V_X has more impact on V_{REF} than the opposite, i.e., $K_1 > K_2$ (Fig. 1(a)). In the case of this work, the circuit is designed for the high-order compensation of V_{REF}, but the same can also be achieved for V_X.

By replacing (8) in (7), and defining $\beta = \frac{n(n+3)-2}{n+1}$, $\xi = \frac{n_3(n+1)}{n-1}$ and $\theta = \frac{n(n-1)}{n+1}$ the voltage reference is now given by

$$V_{REF} = \frac{V_{T1} - V_{T2}}{\beta} + \frac{n_3V_{T1} - nV_{T3}}{\beta\xi} + \phi_t \ln\left(\frac{I_{S2}^{\frac{n}{\beta}} I_{S3}^{\frac{\theta}{\beta}}}{I_{S1}^{\frac{n+\theta}{\beta}}}\right) \quad (9)$$

Thus, the proposed circuit provides at its output the weighted difference between the V_T of M_1 and M_2 transistors, as shown by the first term of (9). The second term of V_{REF} appears as the high-order compensation coming from V_X, where V_{REF} is compensated through the third term by adjusting S_1, S_2 and S_3 ratios.

It is important to note that since in the model used the transistor terminals are referenced to the bulk, (9) includes the variation of V_T due to body-effect.

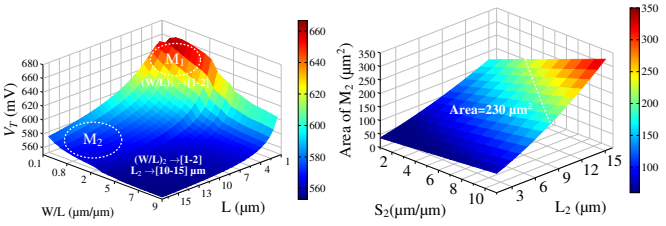
III. High-Order 3-Transistor Voltage Reference

A. Design of the SCM

Different than previous works, in the proposed voltage reference distinct V_T using the same type of transistor are achieved through its dependence with the transistor dimensions. Since the goal of this design is low-power operation, the choice of the transistor type is made between the two high-V_T transistors in the process used. As presented in [4], the low-power transistor presented both lowest normalized temperature slope (α_{V_T}) and the wider V_T variation from W_{MIN}/L_{MIN} to W_{MAX}/L_{MAX}, making it the preferable choice.

The variation of V_T with respect to W and L for the low-power transistor of a standard 130 nm CMOS process in shown in Fig. 2(a). As can be seen, L is the major contributor for the V_T variation, while V_T becomes dependent only of L for larger values of W. As stated before, V_{REF} is generated mainly by the difference between the V_T of M_1 and M_2. Therefore, the $V_{T1} > V_{T2}$ condition needs to be guaranteed. From Fig. 2(a), to obtain a high V_T value transistor M_1 must be sized with small values of both W and L (W/L between 1 to 2). On the other hand M_2 is sized taking into account the following:

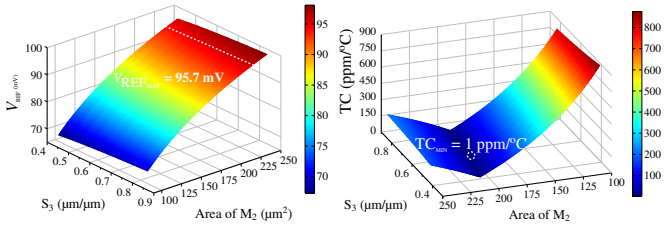
- $L_2 \gg L_1$, which guarantee $V_{T1} > V_{T2}$.
- To prevent charging damage in the polysilicon, the maximum oxide area for any single gate transistor in the 130 nm process used in this work has to be less than 230 µm^2.
- To guarantee an efficient layout area while $(W\times L)_2 \leq$ 230 µm^2, a range of $(W/L)_2$ = [1-2] with L_2 = [10-15] µm is defined, as shown by Fig. 2(b).



(a) V_T dependence with respect to W and L. (b) Maximum M_2 area.

Fig. 2. V_T and M_2 area boundaries.

The maximum value of V_{REF} is limited by the maximum M_2 area as shown by Fig. 3(a), which results in a maximum voltage reference value of 95.7 mV. This value is used to defined the minimum supply voltage for proposed circuit. Since to guarantee saturation $V_{DS} \geq 4\phi_t$, $V_{DD_{MIN}} = V_{DS3} + V_{DS2} + V_{REF_{MAX}}$, resulting in a minimum supply voltage of approximately 300 mV.



(a) Maximum value of V_{REF} for W_1=2µm and L_1=1µm.

(b) TC as function of S_3 and M_2 area for L_2 = 10 µm.

Fig. 3. Max V_{REF} and minimum TC sizing.

Through the range defined to S_2 and using L_2 as starting point, the circuit is designed to achieve the lowest TC as possible. For a fixed value of $(W/L)_1$=2µm/1 µm, the TC is dependent of both S_2 and S_3 ratios. From Fig. 2(a), V_T becomes almost independent of L for values greater than 10 µm, thus defining L_2 = 10 µm. Fig. 3(b) shows the TC dependence with respect to S_3 and M_2 area. In these conditions, S_2 has the major impact in the TC where the high-order compensation is achieved through the fine adjustment of S_3. As shown in Fig. 3(b), a minimum TC of 1 ppm/°C is achieved with S_2=2 and S_3=0.645.

B. Mismatch Variability Attenuation

From the previous considerations on the design of the SCM, one can conclude that M_1 is the major contributor to the mismatch variability of V_{REF} due its small W and L. With this in mind, the proposed bulk driven scheme also attenuates the mismatch variability caused by M_1 when compared to the conventional approach.

Suppose a positive (negative) ΔV_{T1} due to mismatch. This would also cause a positive (negative) variation of both V_{REF} and V_X voltages. But due to the magnitude and the definition of both voltages the impact of a given ΔV_{T1} variation is much greater in V_{REF} than on V_X, i. e., $|\Delta V_{T1}| \rightarrow |\Delta V_{REF}| > |\Delta V_X|$. The dependence of V_T with respect to the source-to-bulk voltage (V_{SB}) can be expressed as [9]

$$V_T = V_{T0} + (n-1)V_{SB} \tag{10}$$

where V_{T0} is the threshold voltage at zero V_{SB} voltage. Thus, a positive (negative) ΔV_{T1} would cause a increase (decrease) on V_{SB2} voltage and consequently increasing (decreasing) V_{T2}. In summary, the proposed scheme attenuates the mismatch variability of V_{REF} by making V_{T2} follow a V_{T1} variation.

IV. Post-Layout Simulation Results

The proposed voltage reference is designed using a standard 130 nm CMOS process. Fig. 1(b) shows the layout of the proposed circuit occupying an active silicon area of 0.0012 mm^2. M_1 and M_2 are triple-well low-power transistors. Post-layout simulation results for the temperature behavior of V_{REF} is presented by Fig. 4, which shows V_{REF} and V_X voltages optimized for the -20 °C to 85 °C range, defined as the conventional approach [4], and its sum, with $K < 1$, resulting in the high-order compensation. From typical simulations, the

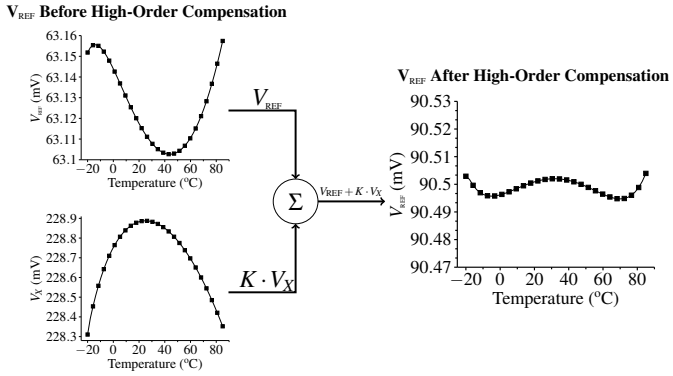
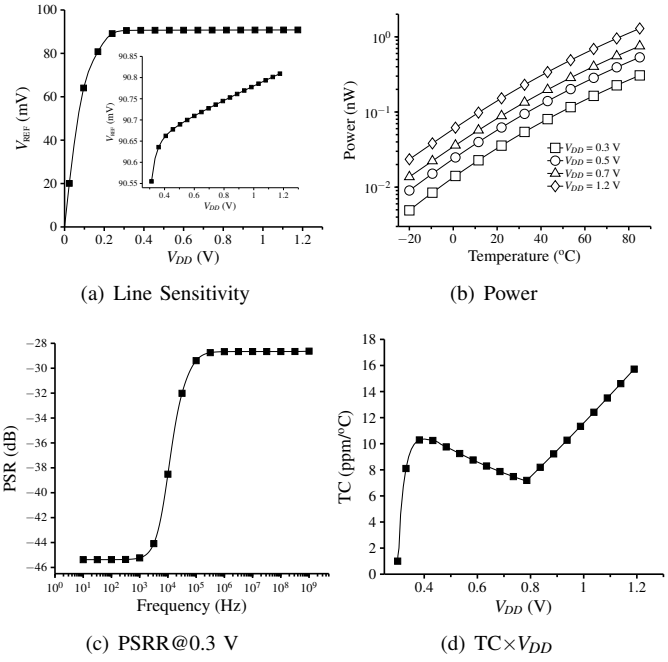


Fig. 4. Temperature behavior of the proposed high-order voltage reference.

conventional circuit presented a TC of 8 ppm/°C while the proposed circuit achieves a minimum TC of 1 ppm/°C at 300 mV of supply voltage with an average value of 90.5 mV.



(a) Line Sensitivity

(b) Power

(c) PSRR@0.3 V

(d) TC×V_{DD}

Fig. 5. Post-layout performance of the proposed circuit.

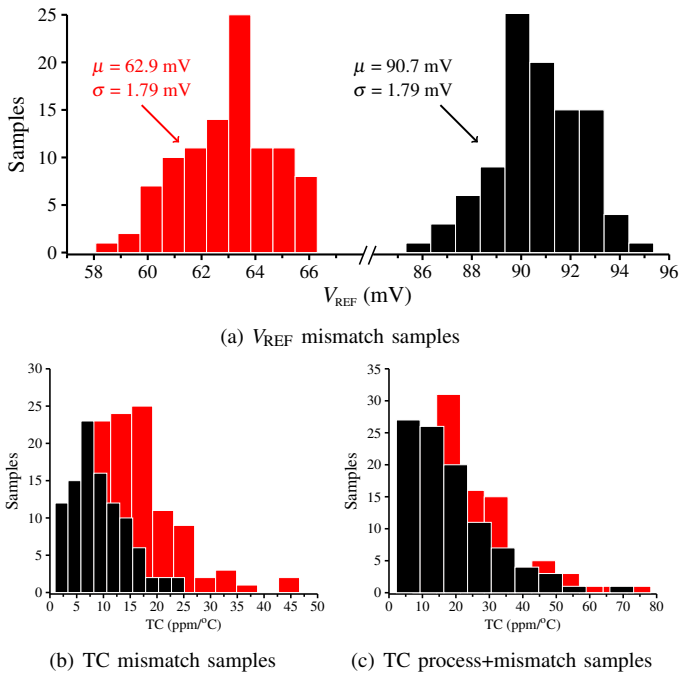
The line sensitivity (LS) obtained from 0.3 V to 1.2 V is 0.4 %/V as presented by Fig. 5(a). The circuit consumes 43.7 pW at 0.3 V supply and 27 °C, and reaches a maximum of 1.3 nW at 1.2 V and 85 °C, as shown by Fig. 5(b). At 0.3 V the circuit achieves a PSR of -45.3 dB at 100 Hz and -28.6 dB for higher frequencies, as shown by Fig. 5(c). The dependence of TC with respect to V_{DD} is presented by Fig. 5(d), where it presents a minimum TC of 1 ppm/°C at 0.3 V and a maximum 16 ppm/°C at 1.2 V.

The sensitivity to process and mismatch variability of the conventional and proposed circuits are presented in Fig. 6. The mismatch variability is presented by Fig. 6(a), where for the conventional implementation the circuit presents a σ/μ = 2.85 % while the proposed circuit presented a σ/μ = 1.98 %. As the results show, the proposed scheme makes

TABLE I
COMPARISON BETWEEN OUR WORK AND RECENT PICOWATT VOLTAGE REFERENCES.

Specification	[1]$^{a,+}$	[2]$^{+}$	[3]*	[4]*	[5]$^{+}$	[6]$^{+,a}$	[7]*	**This Work***	Unit
Technology	0.13	0.18	0.13	0.13	0.18	0.18	0.18	**0.13**	µm
Temp. Range	-20-80	0-120	0-120	-25-125	-40-85	0-100	0-125	**-20-85**	°C
Supply Voltage	0.5-3	0.15-1.8	0.3-1.2	0.3-1.2	1.2-2.2	1.4-3.6	0.45-3.3	**0.3-1.2**	V
Power@room temp.	29.5	26.1	7	18.5	114	35	93	**43.7**	pW
V_{REF}	176	17.69	85	62	986.2	1.25	248	**90.5**	mV
TC	29	1462.4	31.1^{b}	31.5^{b}	48-124	31	15	**18**^{b}	ppm/°C
LS	0.036	2.03	0.417	0.06	0.38	0.31	0.217	**0.4**	%/V
PSR@100 Hz	-51	-64	-18	-64	-42	-41	-36	**-45.3**	dB
Area	0.0093	0.0012	0.001	0.0007	0.0048	0.0025	0.002	**0.0012**	mm^2

^{a}After trimming; ^{b}Process+Mismatch Mean; $^{+}$Experimental; *Simulation



(a) V_{REF} mismatch samples

(b) TC mismatch samples

(c) TC process+mismatch samples

Fig. 6. Variability results for the conventional (red) and the proposed (black) 3-transistor voltage reference @ 0.3 V.

the spread of the voltage reference stay the same while its mean was increased, resulting in a 30% attenuation of the mismatch variability coefficient. These results validate the proposed mismatch attenuation scheme.

Considering mismatch variations, a mean TC of 9.3 ppm/°C is achieved for the proposed circuit while the conventional achieved a mean of 17 ppm/°C. When considering both process and mismatch variations, once again the proposed circuit presented a lower mean TC (18 ppm/°C) compared to the conventional approach (26 ppm/°C). In both cases, the spread of the TC in the proposed circuit was reduced.

Table I presents the comparison of the proposed circuit with the state-of-the-art picowatt voltage references. The proposed circuit presents one of the lowest minimum supply voltages, being the lowest the presented by [2] due to its small voltage reference value. Regarding the power consumption and LS, the circuit achieved reasonable performance within ultra-low-power systems requirements. Considering both process and mismatch variation, it presented the lowest TC mean without trimming. And it is also competitive among the prior state-of-the-art when the occupied silicon area is considered. To the best of our knowledge, the proposed circuit is the first high-order compensated voltage reference operating at pW consumption range.

V. CONCLUSION

This paper presented a high-order 3-transistor pW voltage reference. The voltage reference was obtained through the dependence of the threshold voltage with respect to the transistor dimensions, providing a first-order compensation, while the high-order compensation was achieved by feeding back the voltages through the transistors bulk terminal. Besides providing high-order compensation, the proposed approach also attenuates the mismatch variability of the voltage reference. The low-power and low-voltage operation of the proposed circuit and its small TC makes it a suitable choice for fully-integrated temperature sensors to be used in ultra-low power systems.

REFERENCES

[1] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," *IEEE JSSC*, vol. 47, no. 10, pp. 2534–2545, Oct 2012.

[2] D. Albano, F. Crupi, F. Cucchi, and G. Iannaccone, "A Sub-*kT/q* Voltage Reference Operating at 150 mV," *IEEE TVLSI*, vol. 23, no. 8, pp. 1547–1551, Aug 2015.

[3] A. C. de Oliveira, J. G. Caicedo, H. D. Klimach, and S. Bampi, "0.3 V supply, 17 ppm/°C 3-transistor picowatt voltage reference," in *2016 IEEE 7th LASCAS*, Feb 2016, pp. 263–266.

[4] D. Cordova, A. C. de Oliveira, P. Toledo, H. Klimach, S. Bampi, and E. Fabris, "A 0.3 V, High-PSRR, Picowatt NMOS-Only Voltage Reference using Zero-V_T Active Loads," in *2016 29th SBCCI*, Sept 2016, pp. 1–6.

[5] Q. Dong, K. Yang, D. Blaauw, and D. Sylvester, "A 114-pW PMOS-only, trim-free voltage reference with 0.26% within-wafer inaccuracy for nW systems," in *2016 IEEE Symp. VLSI*, June 2016, pp. 1–2.

[6] I. Lee, D. Sylvester, and D. Blaauw, "A Subthreshold Voltage Reference With Scalable Output Voltage for Low-Power IoT Systems," *IEEE JSSC*, vol. PP, no. 99, pp. 1–7, Jan 2017.

[7] A. C. de Oliveira, D. Cordova, H. Klimach, and S. Bampi, "A 0.45 V, 93 pW Temperature-Compensated CMOS Voltage Reference," in *2017 IEEE 8th LASCAS*, Feb 2017.

[8] T. Jang *et al.*, "FOCUS: Key Building Blocks and Integration Strategy of A Miniaturized Wireless Sensor Node," in *ESSCIRC*, Sept 2015, pp. 257–262.

[9] M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*. Cambridge University Press, 2010.