Charge Injection in Analog MOS Switches

GEORGE WEGMANN, STUDENT MEMBER, IEEE, ERIC A. VITTOZ, SENIOR MEMBER, IEEE, AND FOUAD RAHALI

Abstract—**Charge injection in MOS analog switches, also called pass transistors or transmission gates, is approached by using the continuity equation. Experimental results show the negligible influence of substrate current which leads to a unidimensional model. An easy-to-handle simplified model is deduced and its predictions compared to the injections obtained by measurements. It is shown that this model, which can be used to implement various strategies to reduce charge injection, is valid in any realistic situation.**

I. Introduction

MOST modern analog MOS circuits include an elementary sample-and-hold circuit that combines a sampling switch, implemented by at least one transistor, with a holding capacitor. The major limitation to the accuracy of this circuit is the disturbance of the sampled voltage when the transistor is turned off. One cause is noise, which results in random sequences of small perturbations. The other is charge injection due to carriers released from the channel and to coupling through gate-to-diffusion overlap capacitances.

This problem had been identified in the very first publications on switched-capacitor circuits [1], where first-order compensations were already proposed. A model based on the circuit of Fig. 1, to which most practical charge injection problems can be reduced, was derived and resulted in a universal chart [2]–[4]. This model allows one to choose and implement the best possible design strategy for any given situation. It has been rederived first with a zero signal source resistance [5] and then for the general case [6], [7], with exactly the same results.

The purpose of this paper is to validate this model by providing physical support, theoretical proof, and experimental evidence and to define its limits of validity.

The analysis assumes a symmetrical transistor and a linear variation of the gate voltage V_G (with respect to the bulk) between ON and OFF values $V_{G\,\mathrm{ON}}$ and $V_{G\,\mathrm{OFF}}$, as shown in Fig. 2 for an n-channel transistor. The effective gate threshold voltage V_{TE} will be assumed to depend linearly on the input voltage V_{in}, according to

$$V_{TE} = V_{T0} + n_0 V_{\mathrm{in}} \tag{1}$$

where V_{T0} is the threshold voltage for $V_{\mathrm{in}} = 0$ and $n_0 = 1 + \gamma/\sqrt{\Phi_f}$. γ is the usual body effect parameter and Φ_f the Fermi level. The constant slope during switching off is

$$a = (V_{G\,\mathrm{ON}} - V_{TE})/t_{\mathrm{FALL}} \tag{2}$$

where t_{FALL} is the time needed for the gate voltage to reach the threshold voltage V_{TE}.

Further assumptions are equilibrium before switching off and

$$t_{\mathrm{FALL}} \gg R_{\mathrm{in}} C_1 \tag{3}$$

which allows one to neglect the effect of the signal source during switching off.

Other important values are the total gate capacitance C_G, which includes both overlap capacitances C_{OV} and the total charge Q_{tot} released at switching off

$$Q_{tot} = C_G (V_{G\,\mathrm{ON}} - V_{TE}). \tag{4}$$

This charge increases if the transistor is widened to reduce

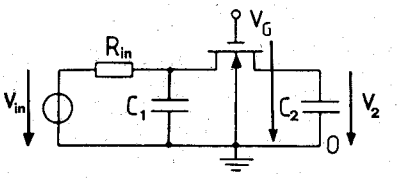

Fig. 1. Circuit for charge injection analysis (pass transistor).

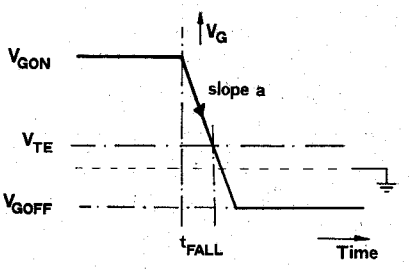

Fig. 2. Definition of the applied gate voltage for an n-channel transistor. V_G is assumed to decrease linearly with time from its ON value $V_{G\,\mathrm{ON}}$ to its OFF value $V_{G\,\mathrm{OFF}}$. Effective threshold V_{TE} is reached after fall time t_{FALL}.

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G. Wegmann and F. Rahali are with the Electronics Laboratory, Swiss Federal Institute of Technology (EPFL), CH-1007 Lausanne, Switzerland.

E. A. Vittoz is with the Centre Suisse d'Electronique et de Microtechnique S.A. (CSEM), Maladière 71, CH-2000 Neuchâtel 7, Switzerland.

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the transfer time constant. It can be pointed out that this charge is a linear function of V_{TE}, and thus a linear function of V_{in} as far as (1) is valid. It results in a linear dependence of charge injection with V_{in}, which has been confirmed experimentally [8].

The longest time needed by mobile charges to reach one end of the channel is proportional to

$$T_0 = n_0 L^2 / \{\mu(V_{G\,ON} - V_E)\} \qquad (5)$$

where μ is the carrier mobility and L the effective channel length [9], [10]. By switching off the transistor the mobile charges of the inversion charge layer are shared between drain, source, and substrate and change the value of the voltage across the capacitors. The fraction of charge ΔQ_2 of the total channel charge released onto the holding capacitor C_2 causes an error voltage of

$$\Delta V_2 = \Delta Q_2 / C_2. \qquad (6)$$

This error voltage limits the accuracy of high-performance analog CMOS circuits as they need large transistors (which entails a high channel charge) and small capacitors to reduce the transfer time constant.

The prediction of the error voltage ΔV_2 in the general case of Fig. 1 will be based on the following qualitative physical description of the charge injection phenomenon in the MOS transistor. A rapid variation of the gate voltage causes a variation of the surface potential as the amount of mobile charges cannot change instantaneously. The surface potential induces an immediate variation of the depletion width, which compensates the excessive charge. Equilibrium corresponding to the new gate voltage is reached by the subsequent charge flow to drain and source. A fraction of the charge in the channel escapes to the substrate leading to charge pumping [11]–[13], which is due to trapping at the interface and to recombination in the channel and into the substrate.

The fact that a part of the channel charge does not flow back to the drain or source has to be analyzed.

II. Charges Leaking to the Substrate

Measurements of the collected charge at the drain and source (Q_{inj}) as a function of the gate OFF voltage $V_{G\,OFF}$ and the fall time t_{FALL} are represented in Fig. 3 for an n-channel device. Long transistors have been chosen to allow measurements with T_0/t_{FALL} larger than 1, corresponding to a short fall time situation.

At long fall times (the switch-off time is longer than the channel transit time), nearly all the channel charge of the transistor is collected by the drain or source and even a low voltage $V_{G\,OFF}$ does not change the amount of injected charge. The inversion charge layer can follow the gate voltage variation. When the gate voltage V_G reaches V_{TE}, most of the channel charge has already been injected and the total injected charge Q_{inj} at drain and source does not vary with $V_{G\,OFF}$.

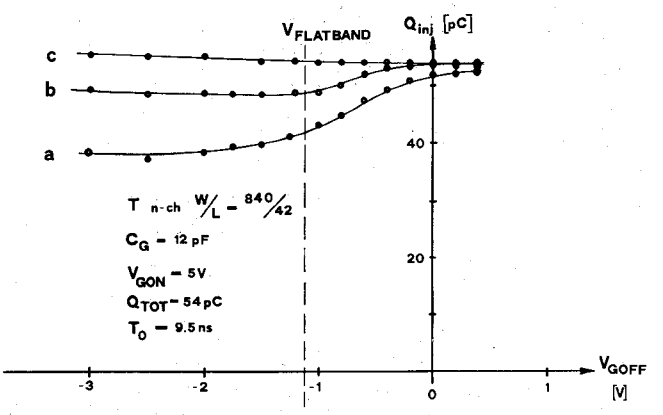

Fig. 3. Measured total charge injected Q_{inj} at drain and source as a function of the gate OFF voltage $V_{G\,OFF}$. N-channel with $W/L = 840/42$, $C_G = 12$ pF, $V_{TE} = 0.5$ V, $V_{G\,ON} = 5$ V, $Q_{tot} = 54$ pC, and $T_0 = 9.5$ ns. Different fall times t_{FALL} are considered: (*a*) $t_{FALL}/T_0 = 0.63$, (*b*) $t_{FALL}/T_0 = 2.4$, and (*c*) $t_{FALL}/T_0 = 42$.

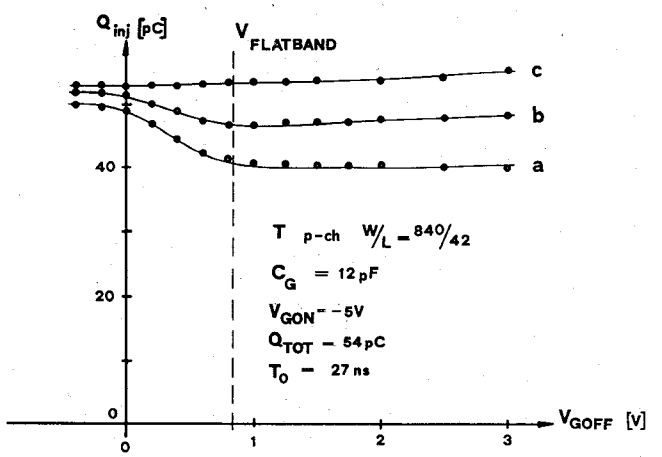

Fig. 4. Measured total charge injected Q_{inj} at drain and source as a function of the gate OFF voltage $V_{G\,OFF}$. P-channel with $W/L = 840/42$, $C_G = 12$ pF, $V_{TE} = -0.45$ V, $V_{G\,ON} = -5$ V, $Q_{tot} = 54$ pC, and $T_0 = 27$ ns. Different fall times t_{FALL} are considered: (*a*) $t_{FALL}/T_0 = 0.22$, (*b*) $t_{FALL}/T_0 = 0.85$ and (*c*) $t_{FALL}/T_0 = 15$.

At short fall times, an increase of the charges flowing into the substrate is observed while $V_{G\,OFF}$ decreases until the flat-band voltage is reached. These charges going to the substrate reduce the total amount of injected charge at the drain and source. Beyond flat-band voltage V_{FB}, charge injection remains constant. The physical explanation is that most of the channel charge has not yet flown back to the drain and source when the gate voltage V_G reaches V_{TE}. If V_G is reduced further, most of the mobile charges will be prevented from escaping to the substrate by the surface potential barrier. This barrier is progressively lowered when $V_{G\,OFF}$ is reduced, which explains why an increasing proportion of the channel charge escapes to the substrate. Therefore Q_{inj} is progressively reduced and saturation is reached when $V_{G\,OFF}$ is approximately equal to the flat-band voltage V_{FB}, which eliminates the barrier.

Fig. 4 shows an equivalent situation for a p-channel transistor.

Measurements with more realistic short-channel lengths did not allow us to show such dependences because the short fall time conditions could not be achieved experi-

mentally and because the dependences were merged by the injections due to the overlap capacitances.

Summarizing, if the fall time is longer than the channel transit time T_0 and the gate OFF voltage $V_{G\,\mathrm{OFF}}$ is just slightly smaller than the threshold voltage V_{TE}, then the substrate current is negligible. In the practical case of short transistors, as used for pass transistors, which have a very short-channel transit time T_0, one can assume that the charges lost through the substrate can be neglected.

III. Models

A. General Model

The flow of mobile charges in the channel can be expressed using the continuity equation [14]:

$$\frac{\partial n(x,y,t)}{\partial t} = \frac{1}{q}\operatorname{div}(J(x,y)) + G - U \tag{7}$$

where $J(x,y)$ stands for the current density, q for the elementary charge, and $n(x,y,t)$ for the carrier density. y refers to the axis along the channel and x to the one perpendicular to it, into the substrate. G and U stand for the generation and recombination rate, respectively.

It has been shown in Section II that the charge leaking to the substrate due to mobile carriers is within a few percents in practical cases. Therefore it can be assumed that the current density $J(x,y)$ depends only on y and that $(U-G)=0$. Using the simple linear expression between the induced channel charge density Q_{si} and the quasi-Fermi level Φ_n of the mobile charges

$$Q_{si} = C_{OX}(V_G - V_{T0} - n_0\Phi_n) \tag{8}$$

where C_{OX} is the gate oxide capacitance per unit area, and introducing the relation between the quasi-Fermi level and the current density $J(y,t)$, one can transform the continuity equation (7) into (9)

$$\frac{\partial}{\partial t}Q_{si}(y,t) = \frac{\mu}{n_0 C_{ox}}\frac{\partial}{\partial y}\left[Q_{si}(y,t)\frac{\partial}{\partial y}Q_{si}(y,t)\right] \tag{9}$$

where

$$Q_{si}(y,t) = -\int qn(x,y,t)\,dx$$

Q_{si} is a unknown function of time and y only which we have to calculate.

The boundary conditions may be expressed if the terminating impedances on the drain and source side are specified. Using the sample-and-hold circuit of Fig. 1 they can be expressed as follows (assuming that C_{OV} is equal to zero):

$$-\frac{\mu W}{n_0 C_G}Q_{si}\frac{\partial Q_{si}}{\partial y}\bigg|_{\text{source}} = C_1\frac{dV_1}{dt} \tag{10a}$$

$$+\frac{\mu W}{n_0 C_G}Q_{si}\frac{\partial Q_{si}}{\partial y}\bigg|_{\text{drain}} = C_2\frac{dV_2}{dt} \tag{10b}$$

where W is the channel width.

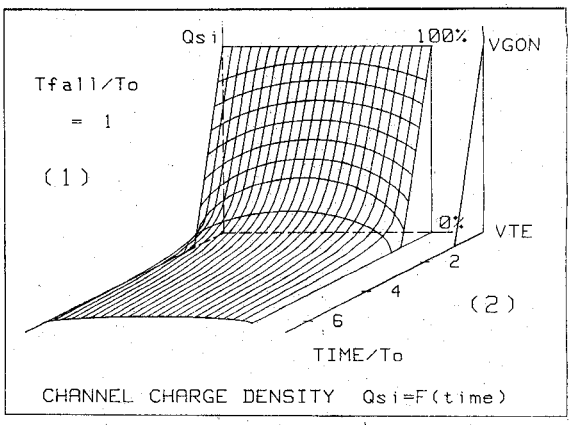

Fig. 5. Evolution of the minority-carrier density along the channel as a function of time and position for a fall time $t_{\mathrm{FALL}}/T_0 = 1$. $C_2/C_1 = 10$, $C_1 = 10\ C_G$, and $C_2 = 100\ C_G$.

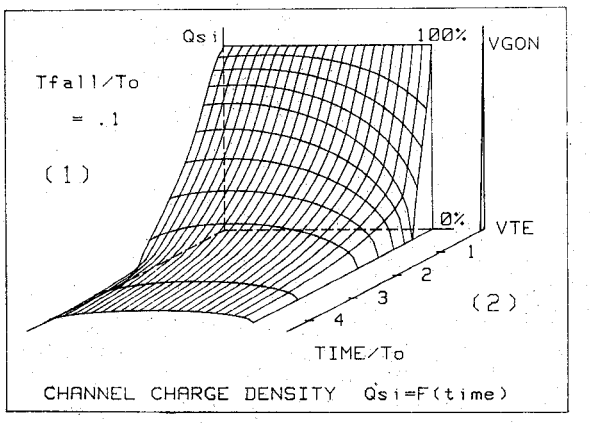

Fig. 6. Evolution of the minority-carrier density along the channel in the case of a asymmetrical situation as a function of time and position for a short fall time $t_{\mathrm{FALL}}/T_0 = 0.1$. $C_2/C_1 = 10$, $C_1 = 0.01\ C_G$, and $C_2 = 0.1\ C_G$.

The nonlinear and nonstationary differential equation (9) may be solved numerically using the finite-element method coupled with the simple Runge–Kutta method [15].

From the numerical solution $Q_{si}(y,t)$ one can find the variation of the quasi-Fermi level along the channel using (2) and derive the charge injection values at drain and source by integrating (10).

The evolution of the mobile charge density $Q_{si}(y,t)$ along the channel (y axis) as a function of time and position is shown in Figs. 5–7.

At short fall times (Fig. 5) the mobile charges follow a curved profile with a higher conductance in the center of the channel than at both extremities, because those in the center do not have enough time to flow to the drain or source. The resulting electric field in the channel pushes the carriers to each side. As soon as pinch-off is reached at both ends the terminal impedances have no influence anymore. If this occurs early enough half the total channel charge is collected by the source and drain.

A nonsymmetrical electric field along the channel (Fig. 6) may only be obtained with a very short fall time and with a value of C_1 or C_2 much smaller than the gate

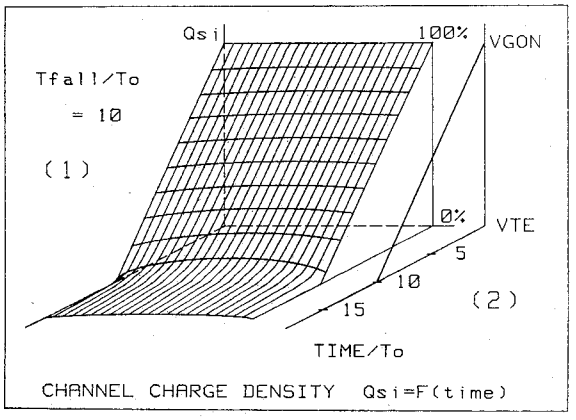

Fig. 7. Evolution of the minority-carrier density along the channel as a function of time and position for a long fall time $t_{FALL}/T_0 = 10$. $C_2/C_1 = 10$, $C_1 = 10\ C_G$, and $C_2 = 100\ C_G$.

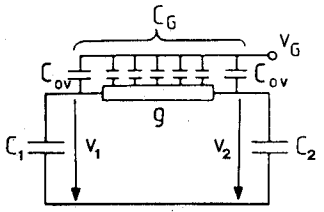

Fig. 8. Model of the channel for charge injection analysis. Substrate current is assumed to be negligible.

capacitance C_G. However, it does not correspond to any practical case.

Long fall times will be considered in the next section.

B. Simplified Modelization (Electrical Model)

Fig. 7 shows that for long fall times with

$$t_{FALL} \gg T_0 \tag{11}$$

and large enough capacitor values

$$C_1 \text{ and } C_2 \gg C_G \tag{12}$$

the profile is homogenous all along the channel. The channel conductance can therefore be represented as a time variable conductance g

$$g[V_G(t)] = \beta(V_G(t) - V_{TE}) = \beta(V_{G\,ON} - at - V_{TE}) \tag{13}$$

with $\beta = (W/L)\mu C_{OX}$, while the gate voltage V_G is higher than the effective threshold voltage. For a gate voltage lower than the effective threshold voltage V_{TE} the channel conductance is assumed to be equal to zero, which means that weak inversion effects are neglected. Thus, the transistor can be represented as a time-variable conductance g associated with the distributed gate oxide capacitance and the two overlap capacitances C_{OV}, as shown in Fig. 8 [2], [4]. Drain and diffusion capacitances are included in C_1 and C_2.

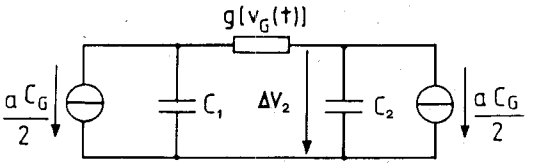

Fig. 9. Final simplified model for charge injection analysis.

If conditions (11) and (12) are satisfied, the variation with time of the surface potential at any point of the channel is negligible with respect to that of the gate. Thus the linear decrease of V_G with slope a across the distributed gate capacitance C_G is equivalent to a constant current source of total value (aC_G) flowing symmetrically to both ends. This leads to the final model of Fig. 9.

Resolving this circuit yields the following normalized differential equation:

$$dV/dT = (T - B)[(1 + C_2/C_1)V + 2TC_2/C_1] - 1 \tag{14}$$

where the normalized factors are

$$V = \Delta V_2 / \left[(C_G/2)\sqrt{(a/\beta C_2)}\right] \tag{15a}$$

$$T = t/\sqrt{(C_2/a\beta)} \tag{15b}$$

$$B = (V_{G\,ON} - V_{TE})\sqrt{(\beta/aC_2)}\,. \tag{15c}$$

The numerical solution for different values of the capacitor ratio C_2/C_1 by integrating (14) during the switch-off time ($0 < T < B$) leads to the diagram of Fig. 10 representing the charge injection ratio $\Delta Q_2/Q_{tot}$ as a function of the characteristic switching parameter B [2]. This diagram shows that for small values of B, equirepartition of charge is obtained independently of capacitance ratio C_2/C_1. For large values of B, which are reached if the fall time is very long, voltage equilibrium is approached asymptotically, which yields a charge repartition proportional to C_2/C_1. For intermediate cases, corresponding to most realistic situations, the charge repartition strongly depends on the switching parameter B.

The effect of nonsymmetrical overlap capacitances has to be taken into account because for short transistors (as used for pass transistors) their difference ΔC_{OV} can be an important fraction of the total gate capacitance. Therefore the two symmetrical current sources of a value of $aC_G/2$ on each side (Fig. 9) have to be replaced by one of a value of $a(C_G + \Delta C_{OV})/2$ and by one of $a(C_G - \Delta C_{OV})/2$.

Assuming that the charge redistribution is not affected by a small variation of B, a first-order correction can be obtained by adding the charge difference due to the asymmetrical overlap capacitances leading to

$$\Delta V_{2\text{asymmetrical}} = \Delta V_2(1 \pm \Delta C_{OV}/C_G) \tag{16}$$

where the positive sign corresponds to the case of larger overlap capacitance on side 2.

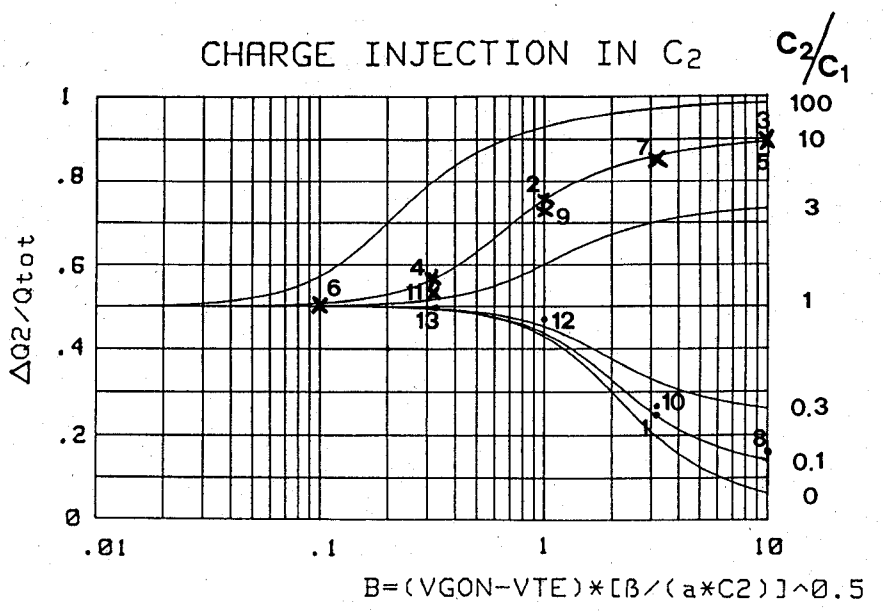

Fig. 10. Normalized diagram showing the amount of charge injected in C_2 as a function of switching parameter $B = (V_{G\,ON} - V_{TE})[\beta/(aC_2)]$ 0.5 and capacitance ratio C_2/C_1. Various points calculated from the numerical model for marginal situations (see Table I) are reported for $C_2/C_1 = 10$ (×) and $C_2/C_1 = 0.1$ (○). None of the points showing visible discrepancy (7–13) corresponds to a realistic case.

TABLE I
VARIOUS POINTS CALCULATED FOR DIFFERENT VALUES OF C_2/C_G AND t_{FALL}/T_0 IN THE CASE OF $C_2/C_1 = 10$ AND $C_2/C_1 = 0.1$

No.	T_{FALL}/T_0	C_2/C_G	C_2/C_1	COMMENTS
1	100	10	0.1	
2	100	100	10	
3	100	1	10	
4	10	100	10	FIGURE 7
5	10	0.1	10	
6	1	100	10	FIGURE 5
7	1	0.1	10	
8	1	0.01	0.1	
9	0.1	0.1	10	FIGURE 6
10	0.1	0.01	0.1	
11	0.01	0.1	10	
12	0.01	0.01	0.1	
13	0.001	0.1	0.1	

In summary, the parameters of this simplified model are the gate voltage $V_{G\,ON}$, the effective threshold voltage V_{TE} (which includes the effect of the substrate modulation according to (1)), the slope a of the gate voltage, the value of the capacitor C_2, the ratio C_2/C_1, the transfer parameter β of the transistor, and the difference of the overlap capacitances ΔC_{OV}.

To check the importance of conditions (11) and (12) for the validity of this simplified model, various points corresponding to various values of t_{FALL}/T_0 and C_2/C_G were calculated numerically with (9) and (10). Some of these points are given in Table I and reported in the diagram of Fig. 10. It can be seen that the correspondence is perfect for all points satisfying (11) and (12) (only points 1, 2, and 4 of this category have been reported for the sake of clarity). Even when the conditions are only marginally fulfilled (points 3 and 5–7), results still agree within a few percent. All the points for which a large discrepancy is observed correspond to nonrealistic situations.

At short fall times the channel is quickly pinched off and is no longer homogenous as assumed in the simplified model. However, the fact that the channel conductance is not uniform does not influence the equal sharing of the channel charge to drain and source predicted by the model for small values of B, but only the time needed to evacuate all the mobile charges from the device.

IV. EXPERIMENTAL RESULTS

The experimental verification was carried out by measuring the circuit of Fig. 1. To increase the accuracy of the measurements and to reduce parasitics, a guard box, large transistors, and load capacitors were used. Each measurement point is the mean value of over 200 samples, which reduces the effect of added noise, especially for low injections.

All device parameters were individually measured. Care was taken to respect the conditions discussed in Section II for negligible charge flow to the substrate. Calibration of the total channel charge was obtained for each measurement by connecting the drain to the source. The precision of the measurements is estimated to be within a few percent in the worst cases.

The influence of all the parameters mentioned before has been separately tested. In Fig. 11 the experimental

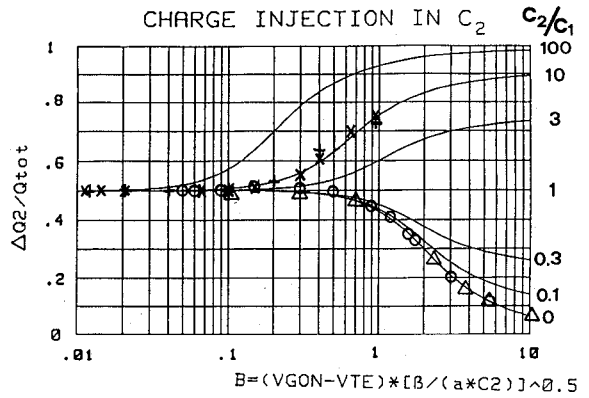

Fig. 11. Measured injections for symmetrical transistors. 1) N-channel, $W/L = 10000/22$, $C_G = 79$ pF, $V_{TE} = 0.5$ V, $C_2/C_1 = 0$, and $C_2 = 39.3$ nF. Gate ON voltage $V_{GON} = 2$ V (○); gate ON voltage $V_{GON} = 3.5$ V (△). 2) P-channel, $W/L = 840/42$, $C_G = 12$ pF, $V_{TE} = -0.45$ V, $C_2/C_1 = 10$, $C_2 = 27.3$ nF, and $C_1 = 2.9$ nF. Gate ON voltage $V_{GON} = -5$ V (X, +). The slope a is the independent variable.

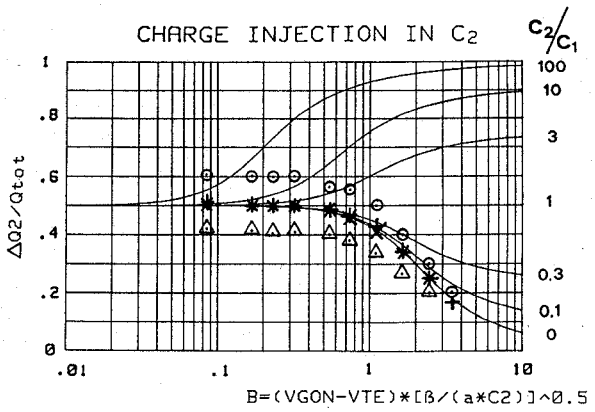

Fig. 12. Measured injections for asymmetrical overlap capacitances $\Delta C_{OV}/C_G = \pm 0.17$. P-channel, $W/L = 1000/10$, $C_G = 6$ pF, $V_{TE} = -0.45$ V, $C_2/C_1 = 0$, $C_2 = 2.9$ nF, and $V_{GON} = -5$ V. C_{OV} larger on C_2 side: measured (○); after correction with (16) (+). C_{OV} smaller on C_2 side: measured (△); after correction with (16) (×). The slope a is always the independent variable.

results for an n-channel ($W/L = 10000/22$ and $C_2/C_1 = 0$) and a p-channel ($W/L = 840/42$ and $C_2/C_1 = 10$) are reported.

Fig. 12 shows the experimental results for a ratio $C_2/C_1 = 0$ and a p-channel transistor ($W/L = 1000/10$) having a large asymmetry of overlap capacitances ($\Delta C_{OV}/C_G = 0.17$). After correcting by (16), a good agreement is obtained with the theoretical curve, which demonstrates the validity of this equation.

Several other measurements have been carried out by using other transistors and other capacitances. Where it was possible the experiments were made with p- and n-channel transistors of the same dimensions. All results show a good correlation with the theoretical curves.

V. Conclusions

Charge injection has been approached using numerical modeling to support a simplified model, which allows designers to predict the amount of charge injection as a function of different parameters. It has been shown theoretically and experimentally that this model remains valid in any practical situation, as long as the amount of charge leaking to the substrate is negligible. For short fall times ($t_{FALL} \ll T_0$) this must be ensured by avoiding gate OFF voltage values that are much lower than threshold V_{TE}. Experimental results obtained by varying the different parameters agreed with the injections obtained by the models. The simplified model concentrates all the relevant parameters in an injection diagram (Fig. 10) and allows one to predict quickly the amount of charge injection in order to decide on a possible strategy.

A first strategy is to choose C_1 much larger than C_2 (very low impedance of the signal source) and the switching parameter B much larger than 1, so that all the charges released into C_2 flow back into C_1 during the decay of the gate voltage and ΔQ_2 tends to zero (some easily calculable additional charge is due to the coupling through overlap capacitances after switching off). The drawback is the long time needed for switching off.

A second possibility is to equilibrate the values of both capacitors [16]. By symmetry, half the channel charge flows in each capacitor and can be compensated by half-sized dummy switches that are switched on when the main switch is blocked [1].

A third solution eliminates the need for equal capacitor values by choosing a value of B much smaller than 1, which also ensures equipartition of the total charge. Charge compensation can be achieved using a single half-sized dummy switch.

If the switch is implemented with a pair of complementary transistors controlled by complementary clock signals, the two types of charge released may partially compensate each other. This kind of compensation is not very efficient since it depends on the input voltage V_{in} and since no real matching exists between p- and n-channel transistors. In addition, the residual charge injection can be shown to depend on the timing and skew of the two complementary clocks, which may translate jitter into amplitude noise [17]. A good procedure is therefore to turn off completely the first transistor before switching off the second. The problem can then easily be reduced to that of a single switch.

In any case, the unavoidable mismatch and the uncertainty of the parameters limit the achievable compensation of charge injection. To ensure the best possible compensation, the dummy switches must have the same configuration and be as close as possible to the main switch. Such carefully implemented compensation allows one to reduce charge injection by one, maybe two orders of magnitude. Further improvements require special circuit techniques, such as full differential implementation and active compensation by low-sensitivity auxiliary input [3], [18], [19].

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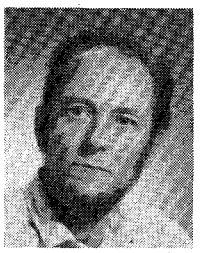
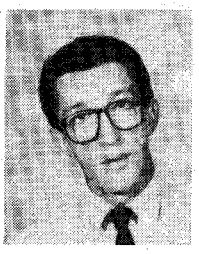
George Wegmann (S'82) was born in Bergamo, Italy, on May 20, 1960. He received the M.S. degree in electrical engineering from the Swiss Federal Institute of Technology, Lausanne (EPFL), in 1985.

Since 1985 he has been a Research Assistant at EPFL, where he is currently working towards the Ph.D. degree on the subject of micropower analog CMOS circuits.



Eric A. Vittoz (A'63–M'72–SM'87) was born in Lausanne, Switzerland, on May 9, 1938. He received the M.S. and Ph.D. degrees in electrical engineering from the Federal Institute of Technology in Lausanne, Switzerland (EPFL) in 1961 and 1969, respectively.

After spending one year as a Research Assistant, he joined the Centre Electronique Horloger S.A. (CEH), Neuchâtel, Switzerland, in 1962, where he became involved in micropower integrated circuit developments for watches, while preparing a thesis in the same field. In 1971 he became Vice-Director of CEH, supervising advanced developments in electronic watches and other micropower systems. Since 1984 he has been Director of the Centre Suisse d'Electronique et de Microtechnique S.A., which was created by merging CEH laboratories with other institutes, where he is in charge of the Division of Circuits and System Design. His field of personal research interest is the design of low-power analog circuits in CMOS technologies. Since 1975 he has also been lecturing and supervising student work in integrated circuit design at EPFL, where he became Titular Professor in 1982.



Fouad Rahali was born in Oran, Algeria, on July 23, 1955. He received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology, Lausanne (EPFL), in 1978 and 1984, respectively.

From 1978 to 1984 he was a Research Assistant at the Electronics Laboratory of the EPFL, where he become involved in simulation of semiconductor devices. He presented his Ph.D. dissertation on the numerical simulation of MOS transistors. From 1984 to 1986 he was lecturing on the physics of semiconductors and electronics at Oran University, Algeria, where he became the Research Supervisor in the Department of Physics. Since 1986, he has been with the Electronics Laboratory of EPFL as Research Associate.