# A 0.7V 7-to-10bit 0-to-2MS/s Flexible SAR ADC for Ultra Low-Power Wireless Sensor Nodes

Pieter Harpe[1,2], Guido Dolmans[1], Kathleen Philips[1], Harmke de Groot[1]
[1] Holst centre and imec, Eindhoven, The Netherlands
[2] Eindhoven University of Technology, Eindhoven, The Netherlands

***Abstract*— This paper presents a flexible SAR ADC in 90nm CMOS for wireless sensor nodes. By supporting resolutions from 7 to 10bit and sample rates from DC to 2MS/s, this design can be used for a variety of applications such as sensor interfacing and receiver frontends. Flexibility is achieved by a reconfigurable comparator and a reconfigurable DAC. Compared to prior art, this work substantially improves power-efficiency and enables low-voltage operation by employing a pseudo-differential DAC switching scheme, offset compensation and simplified asynchronous logic control. The measured chip achieves power-efficiencies of 2.8-6.6fJ/conversion-step at 2MS/s and 0.7V supply. The FOM is maintained down to kS/s-range as the leakage is only 2nW.**

## I. Introduction

Wireless sensor nodes for a.o. EEG, ECG, temperature and pressure monitoring require ultra low-power ADCs for both the sensor-readout interface and for the wireless communication frontend. However, each situation has different requirements for accuracy and bandwidth. For example, a wireless sensor node for ECG monitoring may have two ADCs: one for reading out the ECG sensor, and one for the wireless communication. While the first one may need 10bit resolution at 8kS/s [1], the second one could have 8bit resolution but it requires a sample rate of several MS/s [2]. Commonly, different ADC designs would be used for these two cases in order to maximize the performance. To save design time and to reduce costs, this work proposes a SAR ADC with a wide range of flexibility (7 to 10bit resolution and sample rates from DC up to 2MS/s), such that it can cover various applications with a single design.

Furthermore, since the available energy in autonomous wireless sensor nodes is limited and it may be produced by local energy harvesters with a limited output voltage, the ADC needs very good power-efficiency and the ability to operate at a reduced supply (sub-1V). While SAR ADCs with flexible resolution and speed have been proposed before [3], [4], either their power-efficiency is not competitive to optimized point solutions or they lack the ability to operate at supplies below 1V. For these reasons, this work extends [4] by enabling low-voltage operation (0.7V) while maintaining sufficient speed (2MS/s) and by improving the power-efficiency by about 2×. The low-voltage operation is enabled mostly by an improved DAC scheme, while the conversion accuracy is further enhanced by redundancy in the conversion algorithm and comparator offset correction.

Section II introduces the flexible ADC, Section III shows the measurement results and Section IV concludes this work.

## II. Flexible SAR ADC

Fig. 1 shows the architecture of the flexible SAR ADC. The differential input voltage is sampled on the capacitor arrays inside the DAC. Clock boosting is used to enable operation at a reduced supply with sufficient bandwidth and linearity. The binary-scaled charge-redistribution DAC uses unit capacitors of 0.6fF, which are switched between GND and VDD. The small value of 0.6fF minimizes the power consumption while providing sufficient kT/C noise performance for all resolutions. The 3 MSBs of the DAC (b8 to b6) can be calibrated manually with 1LSB steps to compensate for mismatch errors. The asynchronous logic control resolves the bits of the output code based on self-synchronization [5]. Thus, this architecture requires only a sample-rate clock instead of an oversampled clock. The reference voltage for the DAC, the analog supply, and the digital supply all share a single pin on the chip, powered by an external 0.7V supply.

To implement flexibility in a power-efficient way, the DAC and the comparator are configurable dependent on the selected resolution (7, 8, 9 or 10bit). To save power in the DAC, the MSB capacitors are disabled and disconnected from the capacitor array for lower resolution settings. The reconfigurability of the comparator will be discussed in the following section.

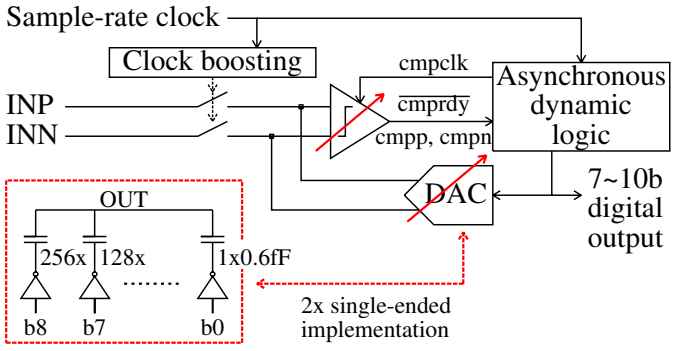


Fig. 1. Flexible asynchronous SAR ADC architecture.

### A. Reconfigurable Comparator

A reconfigurable dynamic comparator is implemented in this work [6], [4]. As in [5], the generated differential output ($cmpp$, $cmpn$) is accompanied by a ready-indication

978-1-4673-2213-3/12/$31.00 ©2012 IEEE

($\overline{cmprdy}$) for the asynchronous logic (Fig. 1). The accuracy (i.e. the noise level) of the comparator can be programmed for each resolution. Since the first stage dominates the power consumption and the input-referred noise (IRN), only this stage is made programmable. The implementation is shown in Fig. 2. Since the power of the first stage scales proportional to its load capacitance $C_{load}$, while the IRN scales with $\frac{1}{C_{load}}$, programming $C_{load}$ is sufficient to optimize the accuracy and power consumption for each mode. Control signals $b_{1,0}$ are used to digitally program $C_{load}$ by means of switching capacitors $C_{1,0}$. Since a large $C_{load}$ would reduce the speed of operation, the tail current is also made programmable: using control signal $b_2$, device $M_2$ can be enabled in parallel to $M_1$. With this structure, both the power consumption and the IRN-power can be programmed over a 4×-range. Since the comparator offset may be slightly dependent on the selected configuration, offset correction for the comparator is implemented inside the DAC as in [7].

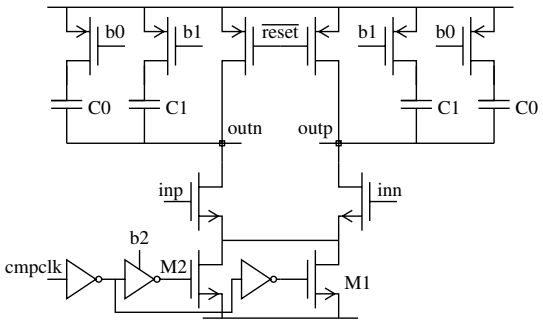


Fig. 2. Flexible preamplifier as used in the comparator.

### B. Two-Step Conversion for 9/10bit Settings

In the presented design, the power consumption is dominated by the comparator, as the power of the DAC and logic are strongly reduced thanks to the small capacitor elements and the asynchronous dynamic logic. As the comparator is noise limited, one could theoretically predict a 4× power increase for each additional bit in resolution, which would imply that the power-efficiency would be degraded for higher resolutions. For that reason, a two-step conversion process is used for the 9 and 10bit resolution modes as in [4], [8]. While a detailed explanation is given in [4], the basic principle for e.g. 10bit resolution is as follows: in a first phase, 8 SAR iterations are performed with the comparator at 8bit accuracy level. This saves power in the comparator, but it may introduce decision errors due to the IRN of the comparator, which is not sufficient for 10bit accuracy. To overcome these decision errors, redundancy is added in the second phase of the conversion: 3 instead of 2 SAR iterations are additionally performed, allowing decision errors up to ±2LSB from the first phase to be corrected. Furthermore, if the second phase is performed with the comparator set to 10bit accuracy, the overall conversion will be 10bit accurate, even though the majority of the conversion is performed at 8bit accuracy. In this way, power is saved while the final accuracy is not degraded.

The redundancy is simply implemented with an additional SAR iteration (11 instead of 10), while a digital adder is used to recombine the data from the 11 SAR iterations to a 10bit output code. A timing diagram of a 10bit conversion is shown in Fig. 3: since the logic is self-synchronized, only a single external clock edge is required for a complete conversion cycle. A total of 11 comparisons is performed. During the first 8 cycles, the comparator is set to a low-accuracy setting, characterized by three parameters: *Offset1*, *Bias1* and *Load1* that define the offset correction, bias current and load capacitance of the comparator, respectively. After completion of the first 8 iterations, the comparator needs to be switched instantaneously to a high-accuracy setting (with parameters *Offset2*, *Bias2* and *Load2*). Therefore, two digital registers are implemented on-chip, each holding one of the required configuration settings. A multiplexer is used to switch automatically from low to high-accuracy after the first 8 iterations are completed.

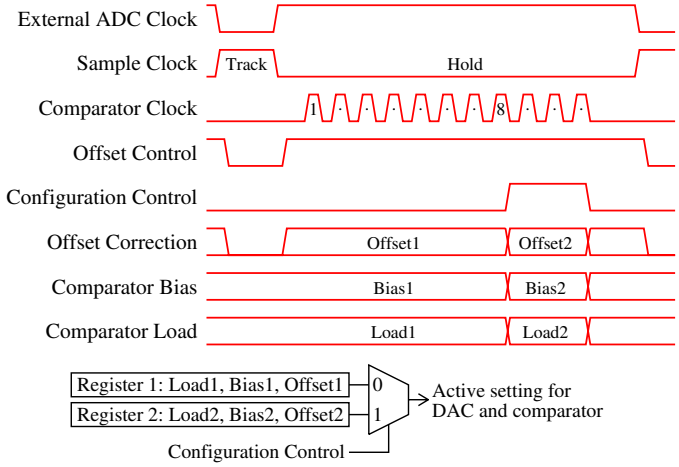


Fig. 3. Two-step conversion process and instantaneous reconfiguration.

### C. Pseudo-Differential DAC Switching Scheme

While a differential DAC is implemented (Fig. 1), it is used in a pseudo-differential way similar to [9]: after each comparator decision, either the positive-side or the negative-side capacitor is switched from GND to VDD, dependent on the comparator result. Since the DAC is only activated after each comparator decision and an update after the last iteration is not useful, a 9bit DAC is sufficient for 10bit ADC resolution, which saves power and chip area. Due to the pseudo-differential switching scheme, the transient voltages at the sampled nodes develop as in Fig. 4: the difference settles to zero during the SAR algorithm, but the common-mode gradually increases since the capacitors are always switching from GND to VDD. This is a desirable effect since it will gradually increase the common-mode level applied to the first stage of the comparator (Fig. 2). Since that stage is based on a NMOS input-pair, this leads to an increased speed of operation, which is especially useful in view of the reduced supply voltage. As a drawback, the variation in common-mode could introduce errors due to the signal-dependent offset from

the comparator. However, this effect is alleviated automatically by the redundancy in the two-step conversion process, which can overcome these variations within certain budget (±2LSB).

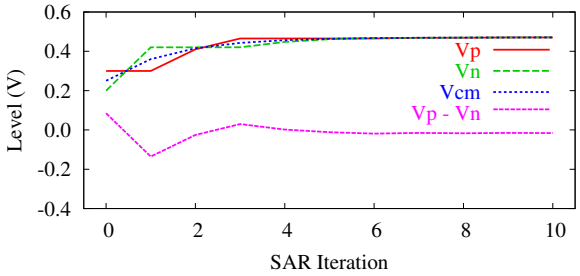


Fig. 4. DAC voltages during the SAR iterations.

### D. Asynchronous Dynamic Logic

As in previous work [5], [4], the logic in this ADC is implemented with asynchronous dynamic logic. However, it is simplified to further reduce the power consumption while it is also adjusted to support the new DAC switching scheme. The logic of a single bit slice (for bit $k$), implementing one SAR iteration, is shown in Fig. 5, while a timing diagram is given in Fig. 6. Following the numbers in Fig. 6, the operation is

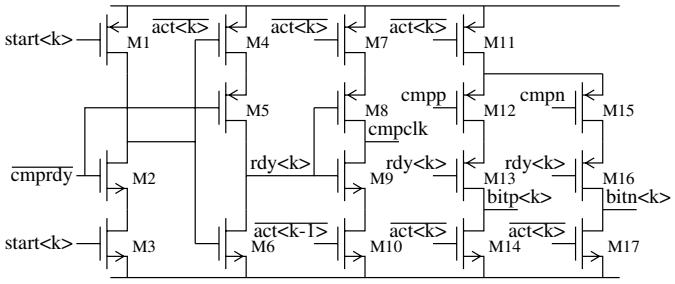


Fig. 5. Asynchronous dynamic logic implementation of a bit-slice.

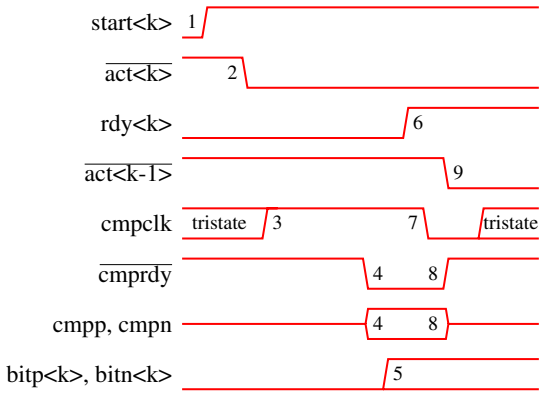


Fig. 6. Timing diagram for a single bit-slice.

as follows: the slice is enabled by a *start*<*k*> signal from the previous slice (1), which causes the active signal $\overline{act}$<*k*> to go low through $M_{2,3}$ (2). Through $M_{7,8}$, *cmpclk* is now activated (3), which will activate the comparator. When the comparator is ready (4), the result is stored by switching either *bitp*<*k*> or *bitn*<*k*> (5). Also, *rdy*<*k*> will go high through $M_5$ (6) to indicate that this iteration is finished. This will reset the comparator (7, 8) and it will enable the next slice (9).

While previous asynchronous dynamic logic needed various transistor sizes for reliable performance [5], this work uses minimum-size devices only, thereby saving power and reducing complexity. Moreover, as shown in Fig. 6, the *cmpclk* output of this cell is in high-impedance when the cell is not active. In this way, the 11 *cmpclk* outputs from the 11 bit slices can be connected together immediately instead of being combined through additional combinational logic, hence further simplifying the logic.

## III. Measurement Results

Fig. 7 shows the realized ADC in 90nm CMOS, which occupies 0.047mm$^2$ including decoupling capacitors. For all

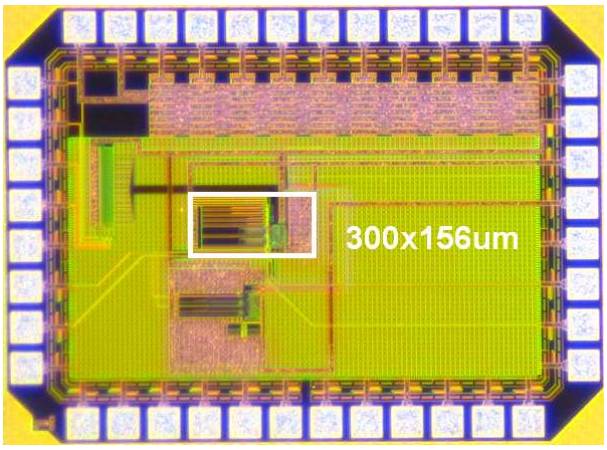


Fig. 7. Die photo of the ADC in 90nm CMOS.

resolution modes, the ADC operates up to 2MS/s with a 0.7V supply. 8 test-chips were calibrated and measured. The chip with the worst INL performance was selected for all measurements in this paper. The INL and DNL for 10bit mode are shown in Fig. 8, reaching an INL of 0.68LSB and a DNL of 0.50LSB.

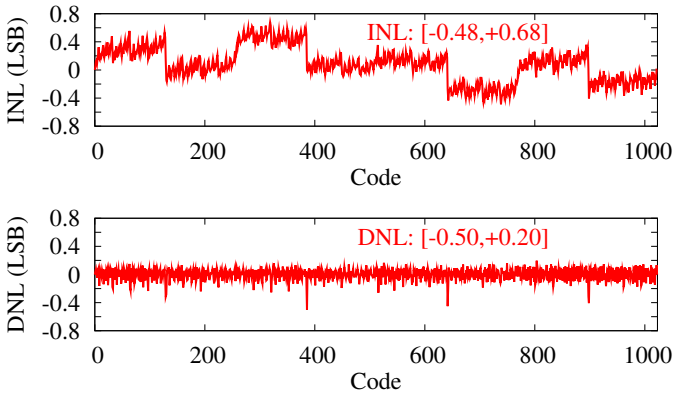


Fig. 8. Measured INL and DNL.

An example spectrum for 10bit mode is shown in Fig. 9, achieving an SFDR above 72dB and an ENOB of 9.30bit. Fig. 10 shows the ENOB versus signal frequency for the different resolutions, reaching up to 9.30bit with an ERBW beyond Nyquist in all cases. The measured power consumption (Fig. 11) scales proportional to the sample rate, down to a leakage level of 2nW.

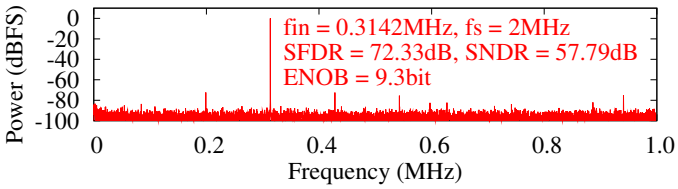


Fig. 9. Measured spectrum at 0.7V supply and 2MS/s.

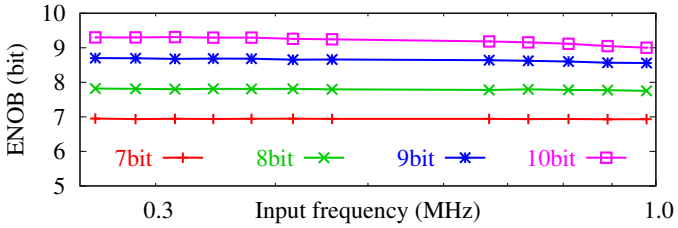


Fig. 10. Measured ENOB at 0.7V supply and 2MS/s for the different modes.

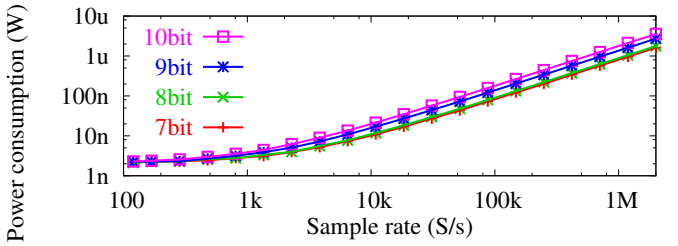


Fig. 11. Measured power consumption at 0.7V supply for the different modes.

Considering the example scenarios from the introduction: for an ECG readout at 10bit resolution with 8kS/s, this ADC consumes 16nW, and for a wireless frontend at 8bit resolution and 2MS/s, this ADC consumes 1.77$\mu$W.

Table I summarizes the measured performance. Using the FOM:

$$FOM = \frac{Power}{2^{ENOB} \cdot \min(f_s, 2ERBW)} \ ,$$

power efficiencies from 2.8 to 6.6fJ/conversion-step are achieved, depending on the selected resolution.

Compared to previous point solutions and flexible designs ([6], [10], [3], [4], [11]), this work achieves very good power-efficiency for all four resolution modes as shown in Table I and Fig. 12. Moreover, it also achieves a relatively high sample rate given the sub-1V supply. Compared to previous work [4], this design improves the power-efficiency by more than 2$\times$ thanks to the reduced supply, the optimized DAC and the comparator offset correction.

TABLE I

MEASURED PERFORMANCE SUMMARY AND COMPARISON.

| | [6] | [10] | [3] | [4] | This work | | | |
|---|---|---|---|---|---|---|---|---|
| Technology (nm) | 65 | 40 | 65 | 90 | 90 | | | |
| Area (mm$^2$) | 0.026 | 0.011 | 0.212 | 0.047 | 0.047 | | | |
| Supply (V) | 1 | 0.5 | 0.50~0.55 | 1.1 | 0.7 | | | |
| Fsample (MS/s) | 1 | 1.1 | 0.06~0.02 | 4 | 2 | | | |
| Resolution (bit) | 10 | 8 | 5~10 | 7~10 | 7 | 8 | 9 | 10 |
| Range ($V_{pp}$) | 2.0 | - | 1.0~1.1 | 1.45~1.36 | 0.9 | 0.9 | 0.9 | 0.9 |
| INL (LSB) | 2.2 | 0.6 | 0.07~0.57 | 0.17~0.42 | 0.16 | 0.35 | 0.33 | 0.68 |
| DNL (LSB) | 0.5 | 0.6 | 0.11~0.58 | 0.20~0.45 | 0.31 | 0.68 | 0.31 | 0.50 |
| ENOB (bit) | 8.75 | 7.5 | 4.77~8.84 | 6.97~9.40 | 6.94 | 7.81 | 8.70 | 9.30 |
| Power ($\mu$W) | 1.9 | 1.2 | 0.234~0.206 | 8.22~17.44 | 1.61 | 1.77 | 2.72 | 3.56 |
| FOM (fJ/c.step) | 4.4 | 6.3 | 143.4~22.4 | 16.4~6.5 | 6.6 | 3.9 | 3.3 | 2.8 |

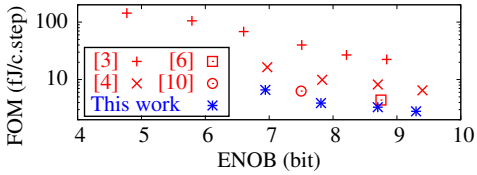


Fig. 12. Performance comparison: FOM versus ENOB.

## IV. CONCLUSION

In this work, a power-efficient flexible SAR ADC was presented. Supporting 7 to 10bit resolution and sample rates from DC up to 2MS/s at 0.7V supply, this design is suitable for applications such as wireless sensor nodes. The prototype in 90nm occupies 0.047mm$^2$ and achieves a FOM of 2.8-6.6fJ/conversion-step, which confirms that a highly flexible design can achieve state-of-the-art power efficiency at the same time.

## REFERENCES


[1] N. van Helleputte, et al., "A 160$\mu$A biopotential acquisition ASIC with fully integrated IA and motion-artifact suppression," *ISSCC Dig. Tech. Papers*, pp. 118 – 119, Feb. 2012.

[2] M. Vidojkovic, et al., "A 2.4GHz ULP OOK single-chip transceiver for healthcare applications," *ISSCC Dig. Tech. Papers*, pp. 458 – 459, Feb. 2011.

[3] M. Yip and A. P. Chandrakasan, "A resolution-reconfigurable 5-to-10b 0.4-to-1V power scalable SAR ADC," *ISSCC Dig. Tech. Papers*, pp. 190 – 191, Feb. 2011.

[4] P. Harpe, Y. Zhang, G. Dolmans, K. Philips, and H. de Groot, "A 7-to-10b 0-to-4MS/s flexible SAR ADC with 6.5-to-16fJ/conversion-step," *ISSCC Dig. Tech. Papers*, Feb. 2012.

[5] P. Harpe, C. Zhou, Y. Bi, N. van der Meijs, X. Wang, K. Philips, G. Dolmans, and H. de Groot, "A 26 $\mu$W 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585 – 1595, July 2011.

[6] M. van Elzakker, et al., "A 10-bit charge-redistribution ADC consuming 1.9$\mu$W at 1MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007 – 1015, May 2010.

[7] P. Harpe, B. Busze, K. Philips, and H. de Groot, "A 0.47-1.6mW 5bit 0.5-1GS/s time-interleaved SAR ADC for low-power UWB radios," in *proc. ESSCIRC*, Sept. 2011, pp. 147 – 150.

[8] V. Giannini, et al., "An 820$\mu$W 9b 40MS/s noise-tolerant dynamic-SAR ADC in 90nm digital CMOS," *ISSCC Dig. Tech. Papers*, pp. 238 – 239, Feb. 2008.

[9] B. Verbruggen, M. Iriguchi, and J. Craninckx, "A 1.7mw 11b 250ms/s 2x interleaved fully dynamic pipelined SAR ADC in 40nm digital CMOS," *ISSCC Dig. Tech. Papers*, pp. 466 – 467, Feb. 2012.

[10] A. Shikata, et al., "A 0.5V 1.1MS/sec 6.3fJ/conversion-step SAR-ADC with tri-level comparator in 40nm CMOS," in *IEEE Symp. on VLSI Circuits*, June 2011, pp. 262 – 263.

[11] B. Murmann. (2012, Mar.) ADC performance survey 1997 - 2012. [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html