An Ultra-Low Power CMOS Subthreshold Voltage Reference

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***Abstract*—A voltage reference circuit operating with nanopower consumption has been proposed in this paper. There are only two current branches in the core circuit. The simulation results show that the average output reference voltage is 0.257V, and the line sensitive is 6.9ppm/V in a supply voltage range from 0.6V to 2V. Resulting from the approximated consideration of body effect, a temperature coefficient of 2.5ppm/°C is achieved in a temperature range from -20°C to 80°C. The power consumption is minimized to 1.5nW at room temperature while the power supply rejection ratio is -40dB at 100Hz and -29dB at 10MHz.**

Keywords-subthreshold; temperature compensation; ultra low power; voltage reference; CMOS analog circuit

I. INTRODUCTION

The portable mobile devices are prevailing in people's daily life. Due to the high efficiency of dc-dc converter and the advancement of the CMOS technology, the circuit could operate with lower supply voltage, and the quiescent current becomes bottleneck for the portable terminals to extend the battery run time. Based on the fact that the threshold voltage (V_{TH}) of MOSFETs with different gate oxide thickness in the same technology exhibit different temperature characteristic, two nanopower CMOS voltage references were presented in [1] and one power consumption was 22nW. Also there were several subthreshold voltage references proposed with the same principle [2], [3]. The simplest structure was developed in [2], of which the power consumption was decreased to 2.6nW and about one order of magnitude lower than [1]. However, all circuits aforementioned at least had three current branches, including one current generator and one active load, which impeded the minimization of quiescent current.

In this paper, an ultra-low power subthreshold voltage reference is presented, the current generator and the active load are merged into one branch, resulting in only two branches in core circuit. The precise parameters of temperature compensation could be obtained by the body effect approximation In order to verify the performance of proposed voltage reference, a simulation based on SMIC 0.18μm CMOS technology has been carried out. The results demonstrate that this circuit exhibits low temperature coefficient (TC) and low power consumption.

II. PROPOSED CIRCUIT AND OPRERATING PRINCIPLE

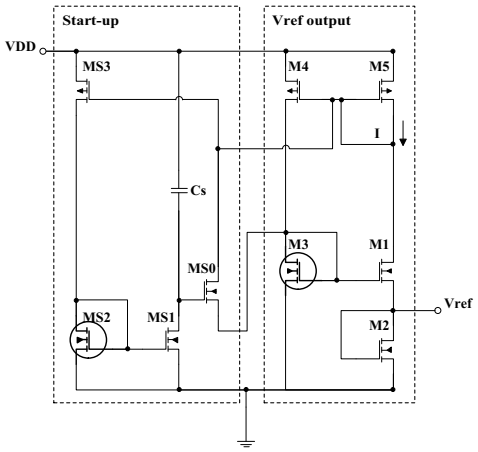

Figure 1. The schematic of Proposed subthreshold voltage reference

The proposed subthreshold voltage reference circuit consists of a start-up circuit and a reference voltage (V_{ref}) output circuit, as showed in Fig. 1. In Vref output circuit, all MOSFETs work in subthreshold region. N-type MOSFETs (NMOS) M1~3 are used to generate V_{ref}. P-type MOSFETs (PMOS) M4 and M5 form a subthreshold current mirror providing the same ratio of current in each branch. A start-up circuit is used to ensure the normal operation condition could always be achieved. All transistors in proposed voltage reference are standard V_{TH} MOSFETs, except for MS2 and M3, which are high V_{TH} (HVT) MOSFETs. Since the substrate of NMOS should be connected to ground for N-well technology, body effect exists in V_{TH} of M1.

A. Temperature Compensation

According to I-V characteristic of NMOS operating in subthreshold region [4], when drain-source voltage V_{DS} is 4 times larger than thermal voltage V_T, one obtains that

$$I = \mu_n C_{ox} (\eta - 1) \frac{t_{ox3}}{t_{ox1}} \frac{K_{N1} K_{N2}}{K_{N3}} V_T^{\,2} \exp\left(\frac{V_{TH3} - V_{TH1}^{\,*} - V_{TH2}}{\eta V_T} \right). \quad (1)$$

Where μ_n is the carrier mobility, C_{ox} is the gate-oxide capacitance that equals the ratio of the dielectric permittivity of silicon dioxide ε_{ox} and the gate oxide thickness t_{ox}. η is the

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subthreshold slop factor and $K_N=(W/L)_N$ is the aspect ratio of NMOS while the thermal voltage $V_T=\kappa_B T/q$, where κ_B is the Boltzmann constant, T is the absolute temperature and q is the elementary charge, threshold voltage with body effect V_{TH}^* could be expressed as [5]

$$V_{TH}^* = V_{TH} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right). \quad (2)$$

Where γ is the body-effect constant, Φ_F is the Femi potential of substrate, V_{SB} is the source-bulk voltage. If V_{SB} = 0, then $V_{TH}^*=V_{TH}(T_0)+k(T-T_0)$ [6], where T_0 is the reference temperature, negative constant k is the TC of V_{TH}. According to the parameters of SMIC 0.18μm CMOS technology and BSIM 3v3 model, $2\Phi_F\approx0.8V$ is always larger than V_{SB} in this circuit and the second term in (2) could be approximated as $(\eta-1)V_{SB}$ [4], [7]. Therefore, (2) could be rewritten as

$$V_{TH}^* = V_{TH}(T_0) + k(T-T_0) + (\eta-1)V_{SB}. \quad (3)$$

From (1) and (3), V_{ref} is given by

$$V_{ref} = V_{GS2} = \frac{1}{\eta}\left[\Delta V_{TH} + \Delta k(T-T_0)\right] + V_T \ln\frac{t_{ox3}}{t_{ox1}}\frac{K_{N1}}{K_{N3}}. \quad (4)$$

Where, $\Delta V_{TH}(T_0)=V_{TH3}(T_0)-V_{TH1}(T_0)$, $\Delta k=k_3-k_1$. Setting $\partial V_{ref}/\partial T=0$, an output reference voltage independence of temperature V_{ref0} can be achieved on condition that

$$\frac{K_{N1}}{K_{N3}} = \frac{t_{ox1}}{t_{ox3}}\exp\left(\frac{-\Delta k q}{\kappa_B \eta}\right). \quad (5)$$

B. Additional Performance Discussion

Some additional calculation can help to optimize the proposed circuit performance.

Substituting (5) into (4), one obtains that

$$V_{ref0} = \frac{1}{\eta}\left[\Delta V_{TH}(T_0) - \Delta k T_0\right]. \quad (6)$$

From (6), we can find that V_{ref0} mainly depends on $\Delta V_{TH}(T_0)$. The parameters of technology used in this design are listed as follows: $V_{TH3}(T_0)=0.659V$, $V_{TH1}(T_0)=0.39V$, $t_{ox3}=6.65*10^{-09}m$, $t_{ox1}=3.87*10^{-09}m$, $k_3=-1.08mV/K$, $k_1=-0.85mV/K$, $\eta=1.25$ and $\kappa_B/q=0.085mV$, then $V_{ref0}=0.27V$ and $K_{N1}/K_{N3}=5.1$ could be easily obtained.

When a zero TC of V_{ref} is satisfied, a current I_0 is given by

$$I_0 = \mu_n C_{ox}(\eta-1)K_{N2}V_T^2 \exp\left(\frac{V_{ref0}}{\eta V_T}\right). \quad (7)$$

From the expression of I_0, the quiescent current decreases with reducing the aspect ratio of M2. In order to reduce the power consumption, a small aspect ratio of M2 should be set (i.e., $K_{N2}=1μm/10μm$).

Since supply voltage is described as

$$V_{DD} \geq V_{GS1} + V_{ref0} + |V_{GS5}|. \quad (8)$$

A large enough channel width W of transistors should be set to get a minimal V_{DD}, and we, roughly set $K_{N1}=100μm/5μm$ and $K_{N3}=19μm/5μm$.

III. SIMULATION RESULTS

In order to evaluate the performance of the proposed voltage reference and validate the design procedure, a series of simulations are carried out with the aid of SPICE simulator using SMIC 0.18μm Mixed Signal/RF technology.

To study the dependence of the output voltage on process variation, Monte Carlo simulations are performed assuming related process parameters obey a Gaussian distribution condition on the typical process corner and room temperature. The results for 300 runs are depicted in Fig. 2 and Fig. 3. The mean value of the output voltage μ is 257.3mV and the standard deviation σ is 3.4mV, the coefficient of variation σ/μ is 1.3%. There are 285 samples whose TC is lower than 8ppm/°C, while 4 samples higher than 11ppm/°C. The average TC is 4 ppm/°C.

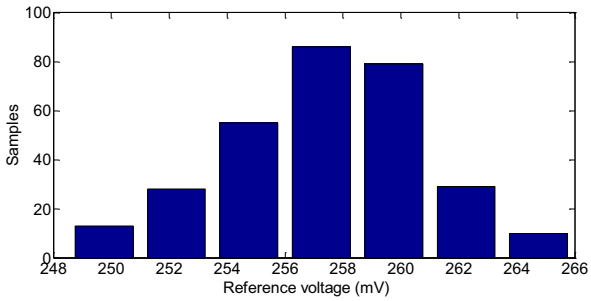

Figure 2. Monte Carlo simulation distribution of V_{ref} at 27°C.

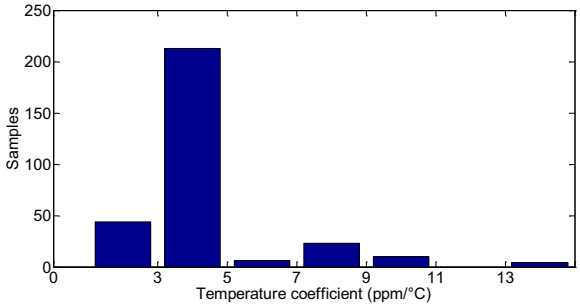

Figure 3. Monte Carlo simulation distribution of TC.

The temperature dependence of V_{ref} and total current consumption are showed in Fig. 4 and Fig. 5, respectively. In the temperature range from -20°C to 80°C, V_{ref} has a difference of 0.065mV. The current consumption varies from 0.57nA to 8.58nA with the supply voltage of 0.6V and a total power consumption of 1.5nW is achieved at room temperature. When V_{DD}=1.8V, TC increases to 23.5ppm/°C and the maximum power consumption is 16.3nW.

The minimum supply voltage is about 0.6V because V_{GS1} is limited to 0.16V, which is the same as $|V_{GS5}|$. Fig. 6 shows the output voltage of the reference has a difference of 2.6mV with the supply voltage ranging from 0.6V to 2V at room

temperature, which implies the line sensitivity is 6.9ppm/V. Fig. 7 shows that the power supply rejection ratio (PSRR) is -40dB at frequency 100Hz and -29dB at 10MHz at room temperature with supply voltage of 0.6V and without any filtering capacitor.

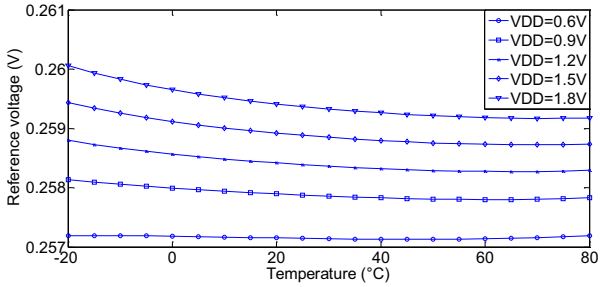

Figure 4. Temperature dependence of output voltage.

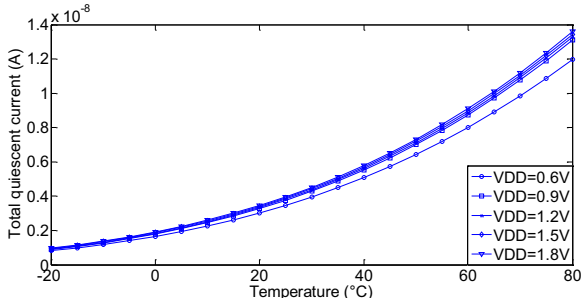

Figure 5. Temperature dependence of total quiescent current.

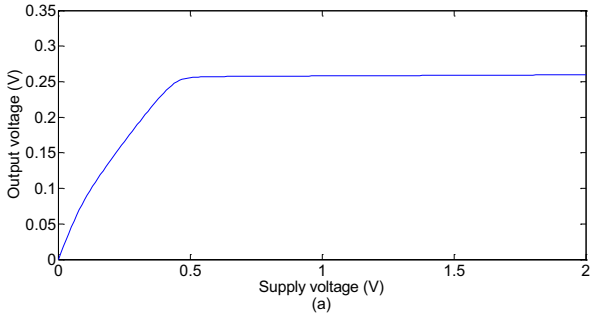

Figure 6. Supply voltage dependence of output voltage.

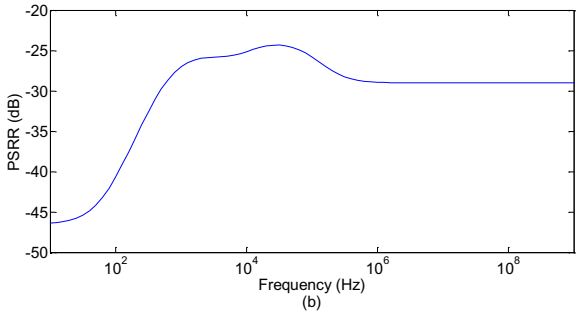

Figure 7. PSRR of proposed voltage reference circuit, for V_{DD}=0.6V.

After TC optimization, the aspect ratio of MOSFETs is adjusted slightly and the main characteristics of the proposed voltage reference are showed in Table I. The error between the initial values and the adjusted ones of the aspect ratio is negligible while the average of V_{ref} is 0.257V, about 13mV lower than manually calculated. This error is mainly caused by the variability of η. The results demonstrate that the proposed subthreshold voltage reference has a good temperature coefficient with an ultra-low power supply.

TABLE I. THE ASPECT RATIO OF MOSFETS AND THE RESULTS OF SIMULTATION

The aspect ratio		**Simulation**	
MOSFETs	***W/L (μm)***	***Items***	***This work***
M1	100/5	Technology (μm)	0.18
M2	1/10	Temperature coefficient (ppm/°C)	2.5@(-20~80)°C
M3	18.5/5	Supply current (nA)	2.6@0.6V
M4	100/5	Line sensitivity (ppm/V)	6.9@(0.6~2)V
M5	100/5	PSRR (dB)	-40@100Hz -29@10MHz

IV. CONCLUSION

An ultra-low power consumption voltage reference has been proposed and simulated in 0.18μm technology. There are only two branches in the proposed circuit. Utilizing approximation of body effect, the parameters used to circuit design are obtained easily. The results of simulation show that a temperature coefficient of 2.5ppm/°C and power consumption of 1.5nW are achieved, which makes the proposed voltage reference suitable for nanopower applications.

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