A 1.8-65 fJ/conv.-step 64 dB SNDR Continuous Time Level Crossing ADC Exploiting Dynamic Self-Biasing Comparators

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***Abstract*—This work presents a power-efficient level crossing ADC designed to digitize sparse signals. It uses dynamically self-biased comparators, which require minimal current when the input voltage is far from a decision threshold. It also uses a DAC architecture which avoids the signal attenuation commonly present in prior level crossing ADC works, improving the achievable SNDR. The prototype is designed and implemented in a 65-nm CMOS technology, and occupies an area of 0.0045 mm². In a 20 kHz bandwidth, the LC-ADC achieves a 64 dB SNDR. Thanks to the proposed techniques a power efficiency of up to 1.8 fJ/conv.-step is achieved for sinusoidal inputs. For sparse biopotential signals a FoMw as low as 0.9 fJ/conv.-step was measured. This makes the prototype interesting for e.g. biomedical applications that make use of spike-based processing.**

***Index Terms*—Continuous time (CT), dynamic biased comparator, event-driven, level crossing (LC) analog-to-digital converter (ADC)**

I. INTRODUCTION

IMPROVING battery life is an important factor in enabling new applications for biomedical insertable and implantable devices. Various biopotentials, such as electromyography (EMG), electrocardiography (ECG) or extracellular action potentials (EAP) signals, contain short bursts of activity followed by long periods of inactivity. Using a traditional Nyquist approach, the input signal is sampled and digitalized based on the maximum expected frequency. This means that during periods of inactivity, the input signal is still sampled at the same high frequency, generating unnecessary data. Converting, transmitting and processing these samples can be inefficient when taking the energy consumption of these tasks into account.

A Level Crossing Analog to Digital Converter (LC-ADC) is able to take advantage of the sparsity of the input signal by only converting signal changes. This means that the number of generated samples is proportional to the signal activity, reducing the amount of required data samples, and the energy needed for their transmission and processing, as was demonstrated e.g. for ECG acquisition in [1]. Additional advantages of Continuous Time (CT) LC-ADCs include an alias free spectrum, an SNDR that exceeds the theoretical limit of conventional Nyquist ADCs with the same resolution in amplitude [2] and lower EMI emissions due to the clockless operation [3].

The LC-ADC has made its way into numerous applications, and can be integrated in a continuous-time (CT) and discrete-time (DT) system. A CT LC-ADC is especially interesting when the front-end, the processor and data transmission are not clocked. A DT LC-ADC on the other hand is better suited for interfacing with clocked systems. Thanks to its event-driven nature, an LC-ADC is an especially good fit for Spiking Neural Network (SNN) processors, which is a class of machine learning networks that are triggered by events [4]. A fully clockless system incorporating a CT LC-ADC with an SNN and asynchronous body channel communication was demonstrated in [5]. In [6] an LC-ADC is used to compress the data generated by sensors that mimic the human skin. In [7]-[9], an LC-ADC is used as a wake-up detector for a more power-hungry system when activity is detected.

While an LC-ADC is effective in compressing the data for various applications, its energy efficiency (>100fJ/conv.-step [11]-[16]) is typically poor when compared to more conventional ADCs, such as SAR ADCs (< 1fJ/conv.-step [17]). One of the root causes of the poor energy efficiency is that the comparators cannot be clocked in a CT LC-ADC, as it is a completely clockless system. In this paper, we propose comparators that are able to dynamically adjust their bias to the input level in order to improve the power efficiency of CT LC-ADCs. This work is extending a previous report [10], by presenting results from a new chip implementation, which provides several improvements compared to [10]. The prototype proposed here targets a 20 kHz bandwidth, and an ENOB better than 10 bits, which is sufficient to digitize most physiological signals. The rest of this paper is organized as follows. Section II reviews the operation of a conventional LC-ADC, and Section III explains the proposed self-biased comparator concept. The circuit level implementation is elaborated in Section IV, and the measurement results of the prototype are presented in Section V. Finally, in Section VI we discuss the advantages and limitations of LC-sampling followed by the conclusion in Section VII.

II. LC-ADC ARCHITECTURE REVIEW

An LC-ADC operates by detecting when the input signal

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crosses a level, as shown in Fig. 1(a). When a crossing is detected, an up or down event is generated, signifying that the input has changed by 1LSB. One of the advantages that a LC-ADC has over a Nyquist ADC is that it can exceed the theoretical limit given by

$$SNDR = 6.02 \cdot N + 1.76, \quad (1)$$

where N is the number of bits of the DAC [18], which is due to the amplitude quantization error. An LC-ADC relies on providing information on the time when a level crossing occurs. Therefore, the error introduced can better be modelled as an error in time, δ, instead of amplitude, limiting the SNDR to [10]

$$SNDR = -20\log_{10}(\delta \times f_{SIG}) - 11.2, \quad (2)$$

where f_{SIG} is the signal bandwidth, and δ is the difference in time between the ideal and measured level crossing. By decreasing the timing error, the limit described by (1) can be exceeded.

When high speed is required, LC-ADC implementations similar to flash ADCs have been proposed [13]. However, to achieve state-of-the-art power efficiency, the architecture shown in Fig 1(b) is preferred. This architecture has been used and described in [12], [14] and [19], and therefore its operation is only briefly summarized here.

From the input voltage V_{in} (Fig. 1(b)), the closest DAC level is subtracted, generating a residue voltage between ±1LSB. If the amplitude of the residue voltage exceeds 1LSB, this is detected by either the upper or lower comparator. This event updates the up/down counter, bringing the residue voltage again between ±1LSB. Note that all circuits in Fig. 1(b) are event-driven (so their power scales with activity), except for the comparators, which need to operate continuously. Hence, the consumption of the comparators is typically the bottleneck for the power consumption of an LC-ADC.

In prior works, the comparators have been implemented using either CT comparators [11], [12], [14], [20], [21], or using DT comparators [15], [16]. The CT comparators are usually implemented using class A, open-loop amplifiers. Due to the static bias current used in the amplifiers, they continuously use considerable energy. Recent DT works have demonstrated better efficiency by using clocked comparators [15], [16]. This allows for the comparator to consume only dynamic power, which helps with concentrating the energy in the decision moment. However, the energy efficiency of DT LC-ADCs remains lower than conventional Nyquist ADCs due to the high sampling speed required to minimize the timing error, as described in (2). Additionally, using DT comparators makes it more difficult to take advantage of the sparsity of the input signal, since extra circuitry is required to adapt the comparison rate to the input activity. Some techniques have been proposed in [16] and [23] to tackle this issue, but the energy efficiency remains orders of magnitude worse than Nyquist ADCs (> 100 fJ/conv.-step).

In [12], it was shown that the efficiency of a CT LC-ADC can be improved by using a comparator with relaxed noise performance to detect if the residue voltage is closer to +LSB or -LSB, and another high-performance comparator which detects if a level crossing occurs. In this work, we take this concept a step further, and propose a new CT self-biased comparator to design a CT LC-ADC with state-of-the-art power efficiency.

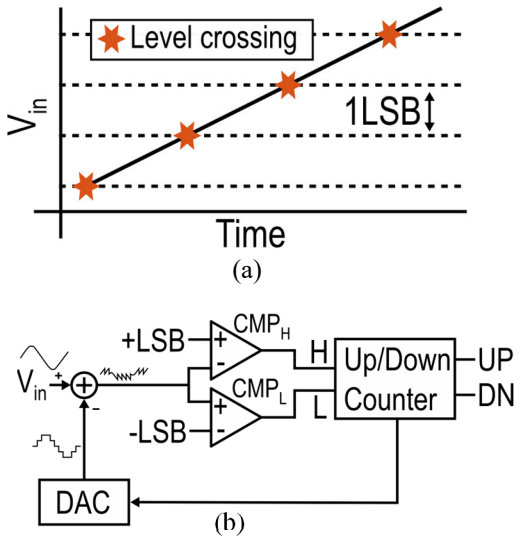


Fig. 1 (a) Time domain operation. (b) Block diagram of an LC-ADC [10].

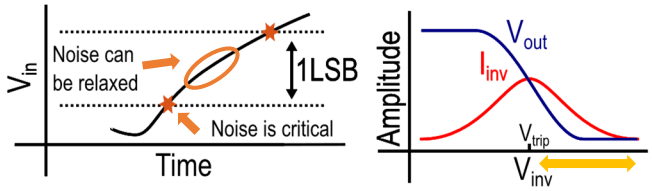
III. Dynamic Self-Biasing Comparator

A. Concept

A significant amount of energy could be saved when the residue voltage is not close to a decision threshold, since the noise performance of the comparator can be relaxed, without falsely triggering an up (UP) or down (DN) event. This means that in those regions, the power consumption of the comparator could be lowered, as shown in Fig. 2(a).

A CMOS inverter consumes maximum power, providing maximum gain and minimum input-referred noise when it is biased in its trip point, while the power consumption lowers when moving away from the trip point. This behavior makes it ideal to dynamically change the noise performance of the comparator. If an inverter is biased in such a way that the level crossing occurs at its trip point, it is possible to spend most of the energy only close to the decision moment.

However, a change of 1LSB at the input of an inverter is typically not sufficient to significantly change the power consumption of the inverter. To maximize efficiency, it is desirable that a 1LSB change of the input voltage completely saturates the inverter output, since this causes a significant drop in the inverter current as shown in Fig. 2(b). This is achieved here by adding a pre-amplifier in front of the inverter, together forming the comparator architecture. Contrary to prior CT comparator implementations where the bias current is constant (Fig. 3(a)), in this work the pre-amplifier bias current is generated by mirroring the current of the inverter (Fig. 3(b)). In this way, the comparator consumes a small current when the inverter is far from its trip point, and a much larger bias current when the inverter is near the trip point (i.e. at a level-crossing).



(a) (b)

Fig. 2: (a) Noise performance requirements at different input signal levels, (b) transfer characteristic of an inverter (blue line), its current consumption I_{inv} (red line) and interval of the characteristics used for the current mirroring (yellow).

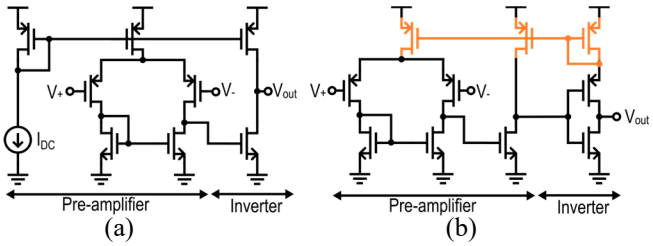


Fig. 3: (a) Conventional and (b) proposed concept of the comparators [10].

Hence, when the input approaches a level crossing, the current in the pre-amplifier increases, lowering its input-referred noise. The implementation shown in Fig. 3(b) is sensitive to PVT variations. Techniques to increase the robustness of the proposed concept are discussed in Section IV.B.

B. Noise, power and gain tradeoffs

In Fig. 4 results are shown based on a simple model of Fig. 3(b), to demonstrate the impact of the gain G of the pre-amplifier on its input-referred noise and bandwidth. It is assumed that a linearly increasing voltage V_{in} is applied to the input of the comparator, starting from 0 V at t = 0 ms, and causing a level crossing at t = 1 ms (Fig. 4(a)), when the input voltage is 1LSB, i.e. $V_{in} = V_{LSB}$. The increasing input voltage results in an exponential increase of the inverter current I, as the inverter is biased in sub-threshold. The inverter input voltage is $G \cdot V_{in}$, thus the inverter current in any moment can be estimated as

$$I = I_0 e^{G \cdot V_{in}}, \tag{3}$$

where I_0 is a suitable pre-factor. As the inverter current is mirrored to the pre-amplifier, (3) also describes the pre-amplifier bias current. The maximum pre-amplifier current I_{max} can be calculated in the same way to be

$$I_{max} = I_0 e^{G \cdot V_{LSB}}. \tag{4}$$

Combining equations (3) and (4) one can write that

$$\frac{I}{I_{max}} = \frac{e^{G \cdot V_{in}}}{e^{G \cdot V_{LSB}}}. \tag{5}$$

This equation is plotted in top panel of Fig. 4(b).

Assuming the thermal noise of the input transistor pair to be the dominant noise source in the pre-amplifier, and supposing the ratio between transconductance and bias current to be constant, which is approximately true in weak inversion, it can

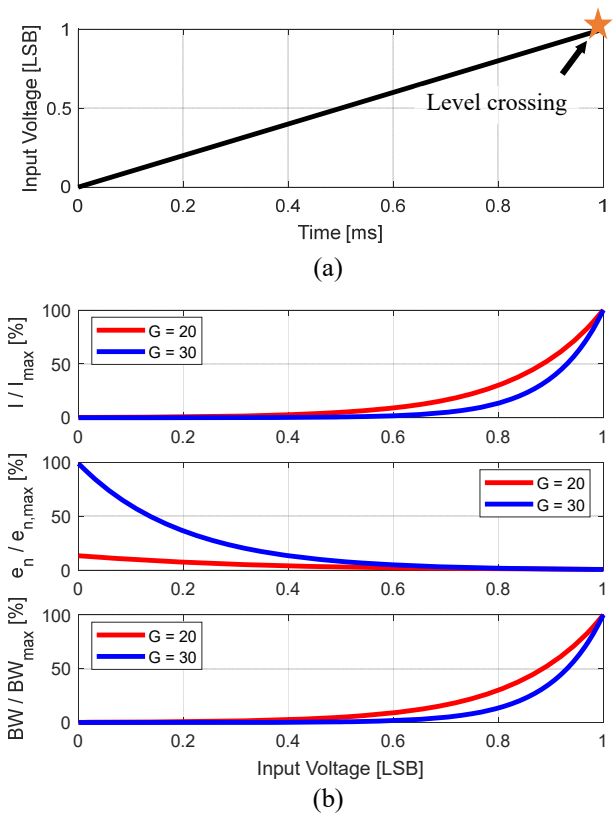


Fig. 4: Results which show the effect of a linearly rising input signal in time (a) on the pre-amplifier bias current I, input-referred amplitude spectral density of the noise e_n, and bandwidth BW, considering two different gains G of the pre-amplifier (b).

be estimated that

$$\frac{e_n}{e_{n,max}} = \frac{\sqrt{I_{min}}}{\sqrt{I}}, \tag{6}$$

where e_n is the input-referred amplitude spectral density of the comparator noise when the current I flows in the pre-amplifier, and $e_{n,max}$ is its maximum value, which is observed at the minimum preamplifier biasing current I_{min}. Equation (6) is shown in Fig. 4(b), middle panel.

Transistor-level simulations show that the dominant pole of the comparator is at the output of the pre-amplifier. The pole frequency is proportional to the the inverse of the pre-amplifier output resistance and, thus, it is proportional to the actual bias current I. Therefore, one can write

$$\frac{BW}{BW_{max}} = \frac{I}{I_{max}}, \tag{7}$$

where BW_{max} is the maximum pre-amplifier bandwidth, which is achieved for the maximum bias current I_{max}. This equation is plotted in the lowest panel of Fig. 4(b) and shows that the speed at which the comparator is enabled decreases for a higher pre-amplifier gain.

Due to the finite bandwidth of the pre-amplifier and inverter, the effect of the comparator noise does not only depend on the noise added in the decision moment, but also on the noise added to the system in the past. However, thanks to the averaging

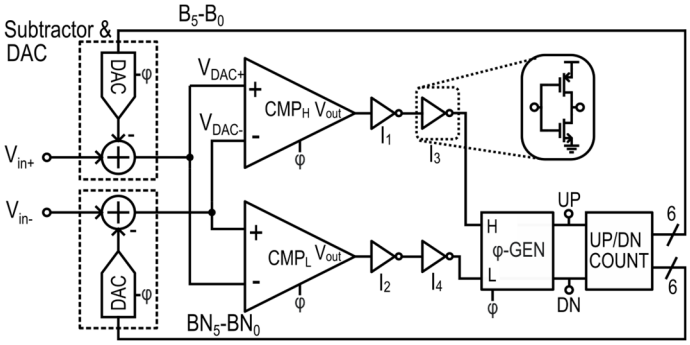


Fig. 5: System overview of the implemented design.

provided by the finite system bandwidth, the noise close to the decision moment has a stronger effect on the accuracy of the decision than the noise added much before the decision. This allows the noise requirements of the pre-amplifier before the decision moment to be relaxed.

When the gain of the pre-amplifier is increased, the current increases more sharply near the level crossing. Thanks to this, the average current consumption is decreased. This reduction in current comes at the cost of higher input-referred noise, and illustrates the tradeoff between the reduction in power and the noise of the pre-amplifier. Accordingly, if the gain of the pre-amplifier is too large, the input-referred noise before a level crossing is increased excessively (Fig. 4(b)). This impacts the level-crossing detection, degrading the SNDR due to the aforementioned noise averaging. On the other hand, if the gain is chosen too small, the dynamic self-biasing is less effective, which diminishes the power savings. A good tradeoff for the gain was found to be 20 V/V according to simulations.

IV. Circuit Implementation

The system architecture of the proposed LC-ADC is shown in Fig. 5. It is a differential implementation of Fig. 1(b), which makes the ADC more robust to variations of the input common-mode voltage. The input is continuously tracked using a capacitive 6-bit DAC, which also provides a suitable voltage shift to keep V_{DAC+} and V_{DAC-} within the reference voltage $V_{CM} \pm$ ½LSB. This simplifies the design of the comparator CMP proposed in this work, as it only needs to handle a small input voltage range. To ensure that the comparator output achieves a rail-to-rail voltage swing, two extra CMOS inverters are cascaded after the CMP blocks (I_1-I_4). When a level crossing is detected, the corresponding UP/DN event is generated and the asynchronous up/down counter updates the DAC to bring V_{DAC+} and V_{DAC-} voltage within $V_{CM} \pm$ ½LSB again. The UP/DN event also triggers a reset phase φ, which is used to charge the DAC to the new voltage level.

A. Subtractor and DAC

The 6-bit DAC and subtractor serve two important functions in an LC-ADC. First, due to the continuous-time nature of the LC-ADC, it should track the input voltage continuously. Secondly, it must provide a voltage shift such that the residue voltage is kept between ±1LSB. In order to relax the noise requirements of the comparators, it is important to avoid signal attenuation.

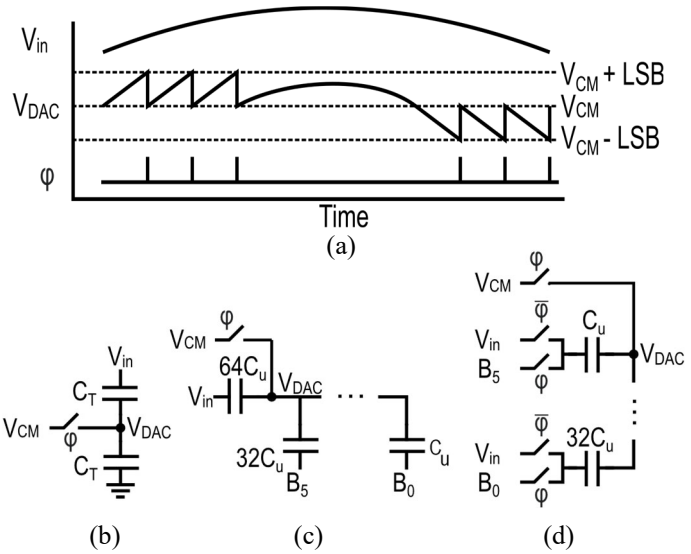


Fig. 6: Timing diagram of a DAC (a), and different implementations of a capacitive DAC using a 1-bit (b), N-bit (c) or the proposed approach (d).

Two different implementations of a capacitive DAC for LC-ADCs can be found in literature. The timing diagram of both approaches is the same, and is shown in Fig. 6(a). When a change of 1LSB is detected, φ is asserted and 1LSB is subtracted. The implementations are shown in Fig. 6(b) and Fig. 6(c), and are commonly referred to as a 1-bit [20] and N-bit DAC [22], respectively. For the 1-bit DAC, the switch closes when the input crosses the value $V_{CM} \pm$ ½V_{LSB}, resetting the DAC back to V_{CM}. An advantage of this approach is the capability of handling input voltages greater than V_{DD}. If there is no delay between the input crossing ±LSB and the resetting of the DAC capacitor, then exactly 1LSB is subtracted. However, if there is a delay, the input can change, introducing an error that depends on the slope of the input. As a consequence, a signal dependency on the loop delay is introduced, leading to a tight requirement for the comparator speed.

In the N-bit architecture, the output node is controlled by the DAC control bits B_5-B_0. This means that the voltage shift that the DAC provides is independent of the input signal, overcoming the limitation of the 1-bit DAC topology. One of the main disadvantages of the N-bit DAC is that more digital logic and thus more power is required to control the DAC. However, since the power consumption is typically dominated by the comparators for sparse inputs, the N-bit approach has been chosen here.

In the conventional implementation of the N-bit DAC for LC-ADCs (Fig. 6(c)), the tracking function and the voltage shift are provided by different capacitors. In order to be able to provide the required maximum voltage shift of $\pm V_{CM}$, the capacitance of the input tracking capacitor C_{in} should be equal to the total capacitance of the capacitor array. However, since the input tracking capacitor C_{in} forms a capacitive divider with the capacitor array, the input amplitude is halved. This input signal attenuation at V_{DAC} is detrimental to the ADC

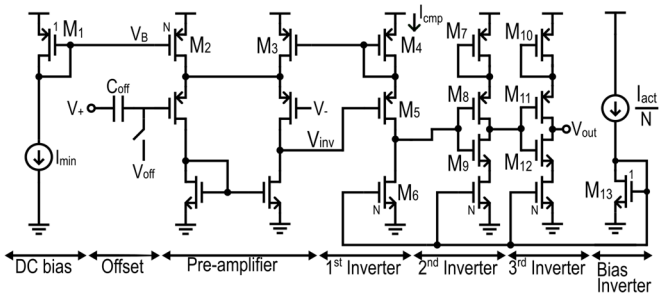


Fig. 7: Implementation of the comparators CMP_H and CMP_L.

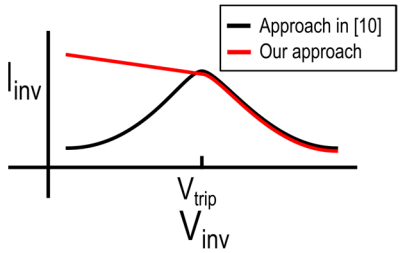


Fig. 8: Comparison of the current profile of the inverter for the approach described in [10] and our proposed approach.

performance and negatively affects the noise requirement of the comparator. To mitigate this shortcoming, we propose here to use one capacitor to do both the input signal tracking, and to provide the required voltage shift (Fig. 6(c)). This approach prevents the signal attenuation. It also gives an additional benefit, since the capacitance seen from the input is reduced. Indeed, the input is connected to a capacitor in series with the input of the comparator and thus only drives a small parasitic capacitance, while in the one-bit (Fig. 6(b)) and traditional N-bit DAC (Fig. 6(c)) implementations, a larger capacitance to ground is seen from the input node. The solution shown in Fig. 6(d) allows thus to relax the requirements on the electronics driving the input of the ADC.

The proposed DAC (Fig. 6(d)) works as follows: after every UP or DN event φ is asserted, charging the capacitors to

$$Q = \sum_{i=0}^{5} C_u \cdot 2^i (B_i - V_{CM}), \quad (8)$$

where B_i is 0 or V_{DD}, depending on the DAC code. After φ is set low again, all the capacitors in the array are connected in parallel, and the capacitors provide a voltage shift ΔV of

$$\Delta V = \frac{\sum_{i=0}^{5} B_i 2^i}{\sum_{i=0}^{5} 2^i} - V_{CM}. \quad (9)$$

Eq. (9) reveals that the proposed DAC topology can indeed shift the input voltage between ± V_{CM}, and thus the input range is not compromised if V_{CM} is chosen to be ½V_{DD}.

B. Comparator

The complete transistor implementation of the CMP blocks in Fig. 5 is shown in Fig. 7. It is based on the concept explained in Section III, but some additional elements are added to improve the robustness of the circuit.

Firstly, the current flowing through a standard CMOS inverter at its trip point is sensitive to process variations: according to simulations this current varies indeed by two orders of magnitude over the process corners in the Si-CMOS technology used to implement the design. To tackle this variability, the inverter is biased with the current I_{act} via the current mirror M_6, M_{13}. When the input signal moves away from a level crossing, the inverter saturates, pushing M_6 into the cut-off region. In our initial implementation [10], the inverter was implemented using a CMOS inverter, which complicated the design of the current mirror. In this work, we instead opted for a common source architecture for the first inverter (Fig. 7). This means that the current profile shown in Fig. 2(b) is not valid anymore for the architecture discussed in this work, but instead the asymmetric profile shown in Fig. 8 is applicable. This is not a problem since it can be guaranteed, suitably choosing the inversions in the signal path, that the first inverter always operates to the right of the trip point, where the current is reduced.

The loop created by feeding back the inverter current to the pre-amplifier should be fast to react to changes in the input. According to small signal post-layout simulations, the bandwidth of the pre-amplifier is 4 MHz at the trip point, which is enough to avoid SNDR degradation. Additionally, a high loop gain is not required since the accuracy of the loop does not impact the resolution of the ADC. For these reasons, the open loop gain is designed to be smaller than one, guaranteeing a fast response and stable loop.

Secondly, the offset of the two comparators CMP_H and CMP_L introduces an error. This is typically removed through calibration [12], [14], [20]. In this work, the offset is calibrated by adding a voltage shift to one of the comparator inputs, provided by charging C_{off} (Fig. 7). This requires a one-time, foreground calibration of the comparator to find the voltage V_{off} which minimizes the offset voltage of the comparators. Afterwards, the capacitor C_{off} is reset to V_{off} during every reset phase φ, recharging the capacitor to provide the correct offset.

The calibration ensures that at the crossing of a level, the output of the comparator (i.e. third inverter (Fig. 7)) operates at its trip point. However, if there is large variability between the inverters, the first inverter may be far from its trip point when the third inverter is at its trip point. This could push M_6 out of saturation, leading to poor control of the current in the first inverter and in the pre-amplifier. While an exact replica of the first inverter would help matching the trip points, due to the asymmetry of the current profile shown in Fig. 8 this is not possible as the 2nd or 3rd inverter would draw their maximum current when not at a level crossing. To be able to turn off the second and third inverter, M_9 and M_{12} are added. The trip points of the three inverters are still matched since at the trip point, M_4, M_5, M_7, M_8, M_{10} and M_{11} all have $V_{gs} = V_{ds}$. Since these transistors are all matched and are biased with the same current, their bias voltages (and thus the trip points) will match too. This minimizes systematic errors and improves the uniformity of the trip points. Additionally, thanks to the gain provided in the pre-amplifier, the input-referred variation of the trip point compared to its nominal value has a reduced influence on the comparator.

Finally, the current of the first inverter is continuously sensed by M_4 and copied to the pre-amplifier using M_3. When the first

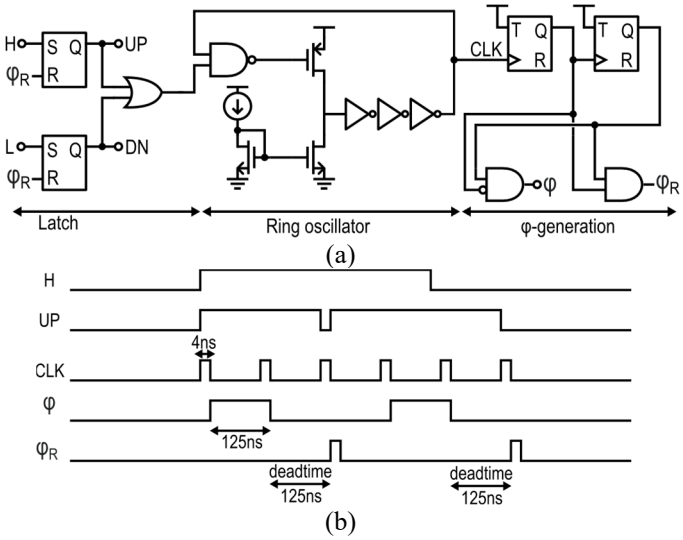


Fig. 9: Block diagram of the LC-ADC digital logic used for the control signal generator (a), and time waveforms of the control signals (b).

inverter saturates, it is important that the pre-amplifier remains properly biased. For this reason, a small bleeding current (I_{min} = 5 nA) is also mirrored by M_1-M_2 to bias the pre-amplifier. This current also helps maintaining sufficient bandwidth when the inverter is far from its trip point.

C. Digital logic

The digital logic consists of two blocks. The first block handles the UP, DN and φ generation. The second block contains a 6-bit asynchronous ripple counter which is used to control the DAC.

The implementation of the first block is shown in Fig. 9(a), and the corresponding time waveforms are shown in Fig. 9(b). When a comparator output goes high (corresponding to the L or H signal for the DN and UP events, respectively), the corresponding SR-latch is set and the reset phase is initiated. The UP and DN signals are the ADC outputs. The delay between the rising edge of L or H and the rising edge of UP or DN is negligible, hence, the digital circuitry has negligible impact on the noise performance of the ADC.

It is possible that the residue voltage falls outside the ±1LSB window, e.g. at the startup of the ADC. This means that multiple count events are required to bring the residue voltage inside the ±1LSB window again. When UP or DN is high, the current-starved ring oscillator is enabled to generate CLK and control the duration of the reset phase φ (Fig. 9). The number of falling edges of CLK are counted using two cascaded T-latches. At the first falling edge of CLK, signal φ goes high, while φ goes low at the second falling edge. At the third falling edge, φ_R goes high, and the circuit attempts to reset the SR latches. If L or H is still high after the dead time between the second and third falling edge, UP or DN remains high and the cycle repeats until L and H are both low. The dead time gives the comparators sufficient time to change state.

The period of the current starved ring oscillator (Fig. 9(a)) determines for how long the reset signal φ is high (Fig. 9(b)).

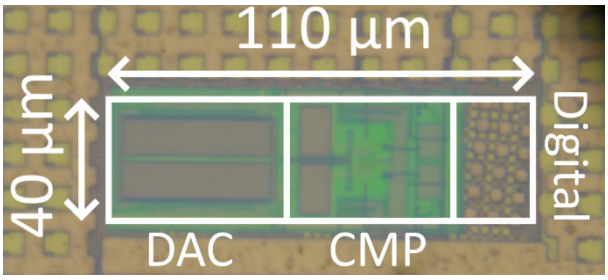


Fig. 10: Chip micrograph of the proposed LC-ADC.

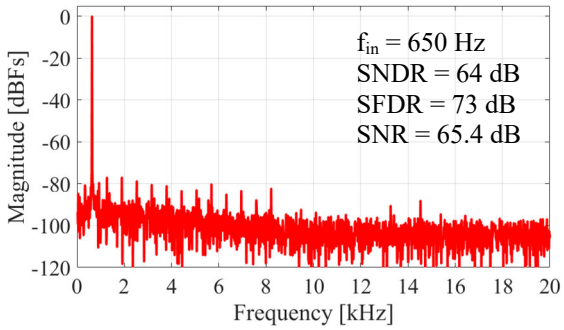


Fig. 11: Output spectrum obtained for a 650 Hz full-scale sinusoidal input.

On one hand, this period should be long enough to allow the DAC capacitors and C_{off} (Fig. 7) to settle. On the other hand, since two oscillation periods determine the shortest time between consecutive up or down events, it should be short enough to avoid limiting the speed of the ADC. According to simulations, this means that a duration between 10 ns and 125 ns is acceptable in the designed ADC, and thus tight control of this period is not required.

V. Measurement Results

The proposed ADC is fabricated in a 65-nm CMOS process. The active area is approximately 0.0045 mm^2 and consists of all the blocks shown in Fig. 5. The micrograph of the chip is provided in Fig. 10. The digital and analog supply voltages are both 1.2 V. The digital output of the ADC is sampled using an oscilloscope. In order to use the standard approach based on the Fast Fourier Transform (FFT) for signal spectrum analysis and SNDR calculation, spline interpolation is used on the output events [13].

Due to an issue with the layout of the DAC, the MSB capacitor is not well-matched to the other capacitors of the DAC. This problem has been corrected in the interpolation process, using a one-time software calibration for the MSB capacitor only. The required correction value is the same for the 5 measured samples, indicating a systematic error due to the layout of the MSB capacitor.

A. Accuracy

The measured output spectrum for a full scale ($2.2V_{pp}$) 650 Hz sinusoidal input is shown in Fig. 11. It achieves an SNDR of 64 dB, and an SFDR of 73 dB. The SNDR is calculated by integrating the noise and distortion inside the bandwidth of

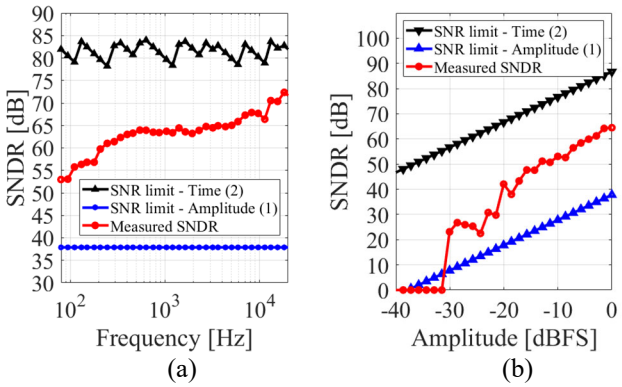


Fig. 12: SNDR vs. (a) frequency, and (b) amplitude of the input.

20 kHz. The UP and DN pulses are acquired at a sampling frequency of 50 MHz.

The measured dynamic performance of the ADC (Fig. 12(a)) plots the SNDR for different input signal frequencies obtained for a full-scale sinusoidal input. It shows an increase of the SNDR up to 70dB when the harmonics fall outside the bandwidth. At low frequencies the SNDR drops, because the time between events becomes large enough for the DAC leakage to affect the SNDR. This is a common effect in CT LC-ADCs, also reported in [12] and [22]. It is assumed that the input activity is high enough such that this is not an issue for our application. Nevertheless, this shortcoming could be mitigated by adding a dither signal to the input [24].

To prevent the SNDR from being limited by the time resolution of the acquisition system, the sampling speed of the oscilloscope is set to 1.25 GHz for measurements at 20 kHz. This sampling frequency generates too much data to capture enough periods for lower frequency sinusoidal inputs. For this reason, the oscilloscope sampling frequency has been adapted to the frequency of the input signal, keeping the SNR due to the time quantization error, calculated according to Eq. (2), always higher than 75dB. The sampling frequency is thus varied from 5 MHz to 1.25 GHz. The limit due to a timing error, as given by (2) is plotted for reference (Fig. 12(a) (black line)). Fig. 12(a) reveals also that the ADC is indeed able to exceed the theoretical SNDR limit (blue line) due to the amplitude resolution, as given by (1).

Fig. 12(b) shows the SNDR as a function of the input amplitude, which is measured for a 650 Hz sinusoidal input using a sample rate of 50 MHz. When the input amplitude is smaller than 1LSB, the input does not cross any levels and thus the SNDR drops to zero. The limits due to time and amplitude quantization have again been included as a reference.

B. Power Consumption

The comparator currents as a function of input voltage expressed in LSBs are shown in Fig. 13. They have been measured by disabling the counter, and by keeping the DAC code constant. This makes it possible to change the comparator input voltage by sweeping the ADC input voltage. Fig. 13 shows that when the comparator input voltage is around 0 V, i.e. far away from a level crossing, the comparator current is

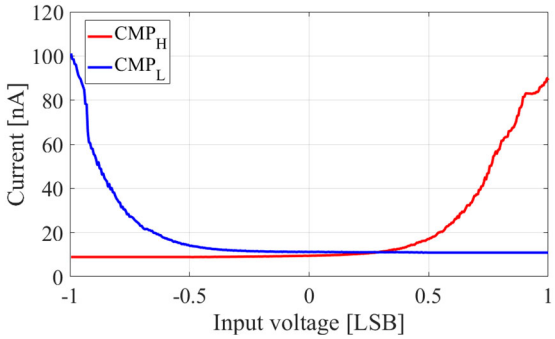


Fig. 13: Current of the comparators CMP_H and CMP_L as a function of their input voltages.

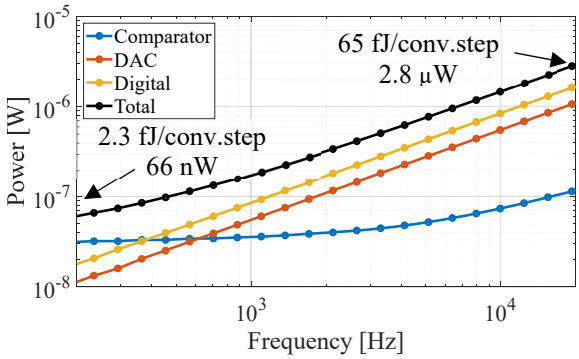


Fig. 14: Measured LC-ADC power consumption vs input signal frequency for a full-scale sine input.

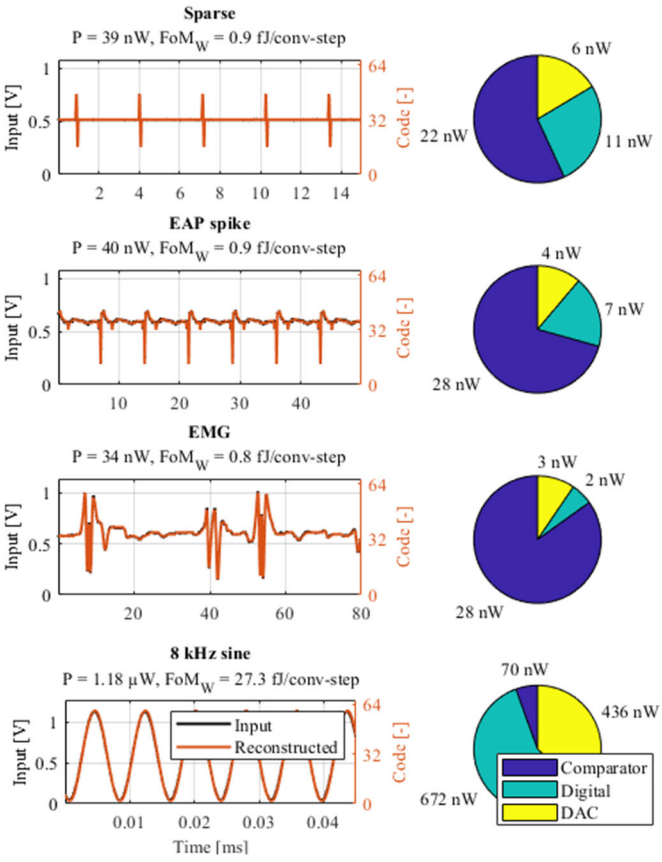


Fig. 15: Measured power and FoM_W for different input signal types and system power consumption breakdown. The FoM_W is calculated based on a SNDR of 64 dB.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE WITH STATE OF THE ART LC-ADCS

	This work	[10] VLSI'23	[11] TCAS-II'18	[12] TBioCAS'13	[13] JSSC'17	[14] JSSC'13	[5] JSSC'22	[15] JSSC'20	[16] ESSCIRC'22
Technology (nm)	65	65	180	180	65	130	40	28	40
Comparator	CT	CT	CT	CT	CT	CT	CT	DT	DT
Supply	1.2	1.2	0.55-1	0.8	1.0	0.8	1.0	1.0	0.5/1
Area (mm^2)	0.0044	0.005	0.0144	0.045	0.3	0.36	0.007	0.0126	0.012
Peak SNDR (dB)	64*	61.4	37.3	49	59.9	54	59.5	53.53	64.4**
Peak ENOB (bit)	10.3	9.9	5.9	7.8	9.7	8.7	9.6	8.6	10.4
Reconstruction method	Spline	Spline	3rd to 6th order polynomial	3rd to 6th order polynomial	Spline	Test DAC	N.A.	N.A.	N.A.
Bandwidth (kHz)	20	16	1	3.3	20,000	20	N.A.	1420	15
Full-Scale Input (V_{pp})	2.2	1.9	0.5	1.6	0.6	0.56	N.A.	1.0	0.9
Power consumption	66 nW – 2.8 µW	76 nW – 9.9 µW	4.4 nW – 186 nW	313 nW – 582 nW	30 mW	3-9 µW	34 µW	150 µW-205 µW	5.38 µW
FoM_W (fJ/conv.step.)	1.8 - 65	3-320	35-4500	206-383	930	180-550	N.A.	140-186	138

* Uses off-chip calibration to correct for MSB mismatch ** Uses off-chip calibration for DAC mismatch

10 nA, which is controlled by I_{min} of Fig. 7. As the DAC voltage approaches +1LSB or -1LSB, the current in one of the comparators rises exponentially, while the current in the other comparator remains low. This confirms the strong dependency of the comparator power on its input voltage.

The power consumption measured for a full-scale sinusoidal input at different frequencies is shown in Fig. 14. As the frequency increases, the number of level crossings per second rises, increasing the digital and DAC power consumption. For benchmarking it is common to use the FoM_W, defined as

$$FoM_W = \frac{P}{2^{ENOB} \cdot 2 \cdot F_{BW}}. \quad (10)$$

Since the FoM_W depends on the input signal, according to the normal practice in LC-ADCs the FoM_W for sinusoidal inputs is calculated using the ENOB, the achieved bandwidth and the power at the minimum and maximum frequency. The proposed CT LC-ADC achieves an SNDR of 64 dB, ENOB of 10.3 bit and a bandwidth of 20 kHz. The highest power is measured at 20 kHz, where the ADC consumes 2.8 µW, which corresponds to an efficiency of 65 fJ/conv.-step. The best FoM_W is measured at 230 Hz, where the SNDR is 62 dB and the power is 66 nW, resulting in a FoM_W = 1.8 fJ/conv.-step.

To show the energy efficiency of the LC-ADC in various application scenarios, the power is measured for different input signals, and the results are provided in Fig. 15. For an exemplary sparse input, an EAP and an EMG signal the energy efficiency is about 0.9 fJ/conv.-step. On the other hand, for an 8 kHz sinusoidal input (Fig. 15), the efficiency is 27.3 fJ/conv.-step due to the increased amount of up and down events. One should notice that the use of the dynamic self-biasing of the comparators is fundamental to improve the energy efficiency for sparse input signals, and could be further optimized as for these signals the comparator power is still dominant.

The performance of this LC-ADC is benchmarked against other state-of-the-art LC-ADCs in Table I. This work achieves a very competitive SNDR and the smallest area. Thanks to the dynamically biased comparators, the proposed CT LC-ADC also achieves the highest energy efficiency for sparse inputs, as highlighted by the best reported FoM_W so far.

VI. DISCUSSION

As can be seen from Table I, the energy efficiency of LC-ADCs depends strongly on the properties of the input signal. This makes the optimal choice of ADC architecture also dependent on the application. The most common choice for a low-power and medium-resolution ADC is a SAR ADC. However, in some specific applications, an LC-ADC can be more power efficient.

For example, to perform the spike sorting in [10], a relatively high time resolution is needed, which for a SAR ADC translates to a high sampling speed. The prototype here described achieves a temporal resolution of 250 ns, defined as the shortest time between two consecutive up or down events. This corresponds to a sampling speed of 4 MHz for the SAR ADC. If we scale the power consumption of [17] assuming a FoM_W of 0.35 fJ/conv.-step, then the SAR ADC would consume 1.7 µW. As shown in Fig. 15, for a sparse input this ADC consumes 40 nW, which is more than 40x lower than the power used by a SAR ADC. To preserve energy efficiency in the complete system, the LC-ADC should be interfaced to an asynchronous processor, such as the SNN described in [6], or send data using a communication protocol which does not require time discretization, such as e.g. the body channel communication used in [10] or a UWB transmitter [26].

Indeed, as it has been shown in [25], time quantization would add a significant penalty to the overall power consumption. This is due to the fact that LC-ADCs typically require a very low time uncertainty, as can be seen from (2), which translates into a high sampling rate if the system is synchronous. Since clock generation is typically not included in the calculation of

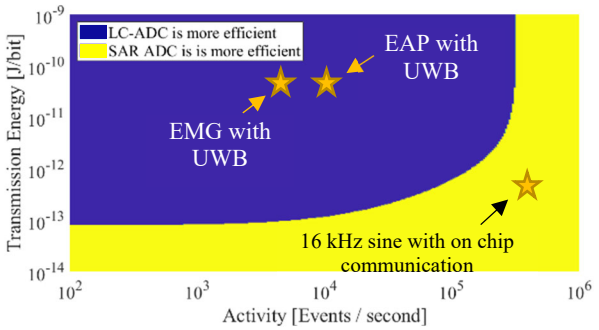


Fig. 16: Comparison between SAR and LC-ADC in terms of total used power, as function of transmission energy and signal activity. The most efficient architecture is the SAR within the yellow region and LC-ADC in the blue region.

FoM_W, this provides an unrealistic advantage in the benchmark of LC-ADCs when compared to SAR ADCs if time discretization is required. One way to show this using the FoM_W is to consider a scenario where a SAR ADC and the proposed LC-ADC are operated with the same clock frequency. To achieve a 20 kHz bandwidth, the SAR ADC requires a clock frequency of 40 kHz. To keep 64 dB SNDR for the LC-ADC, a maximum frequency of 7 Hz can be processed according to (2) when clocked at the time accuracy that is provided by a 40 kHz clock. For a sinusoidal input of such a slow frequency, the required power is 40 nW. By combining these results, the calculated FoM_W would be as high as 2.2 pJ/conv.-step, highlighting the importance of asynchronous processing when opting for a CT LC-ADC.

In order to visualize the tradeoff between signal activity and power consumption, Fig. 16 can be used. Here we consider both the energy for the ADC conversion and the one needed for the transmission of the converted signal. In this way, we can appreciate the potential advantage in the data compression that the LC-ADC can provide.

The total power for a SAR ADC is assumed to be

$$P_{tot,SAR} = P_{SAR} + E_{TX} \cdot N \cdot f_s, \qquad (11)$$

where N is the number of bits, f_s is the sampling speed and E_{TX} is the energy needed to transmit one bit, which is typically between 0.1 pJ/bit for on chip communication, and 1 nJ/bit for wireless data communication. In Fig. 16 we suppose that N = 10 and f_s is 40 kHz. From [17], it is estimated that for a SAR with similar ENOB and bandwidth to our LC-ADC, the total required power P_{SAR} is 14 nW. The total power for an LC-ADC and transmission is calculated as

$$P_{tot,LC} = P_{DC,LC} + activity \cdot (E_{TX} + E_{event}), \qquad (12)$$

where $P_{DC,LC}$ is the static power of the LC-ADC, which is 40 nW for the prototype here described. The activity is measured in events per second. Finally, E_{event} is the energy consumed for processing one up or down event, which is 1.1 pJ in the proposed prototype.

Fig. 16 shows for which combination of signal activity and transmission energy the LC-ADC or SAR ADC achieves the lowest power consumption. The region depicted in blue shows where the LC-ADC is more energy-efficient, while the yellow region indicates where the SAR ADC is more efficient. The plot shows that when the activity of the signal is high, or the energy needed for transmission is low, a SAR ADC is preferred. On the other hand, when the data transmission is expensive in terms of energy, the data compression inherently provided by the LC-ADC approach can provide better energy efficiency.

A few application examples are shown in Fig. 16. The activity of the input signal has been calculated for the EMG and EAP signal shown in Fig. 15, which are 5k and 10k events per second, respectively. If the data is transmitted using an UWB transmitter, such as the one presented in [26], it is indeed advantageous to use an LC-ADC instead of a SAR ADC (provided that the data processing will not require time quantization, as is often possible for biomedical signals). On the other hand, when the activity is high, such as for a full-scale 16 kHz sine wave using on-chip communication, a SAR ADC achieves a better efficiency.

VII. Conclusion

This work presents a novel level crossing ADC achieving state-of-the-art performance. To improve the energy efficiency of the converter, we have proposed the use of a comparator, which dynamically adapts the bias current depending on how close the input is to the crossing of a level. Moreover, a new DAC architecture is proposed to remove the signal attenuation from which conventional DAC architectures suffer. Thanks to these innovations, the energy efficiency of this work and its precursor [10] has been improved by 10x over the most energy-efficient LC-ADC previously reported [11]. This prototype is useful in applications that can make use of the data compression inherently offered by an LC-ADC for processing sparse signals and can be useful to lower the total energy needed at system level for conversion and transmission, especially when data transmission costs a significant amount of power. Additionally, this prototype is especially useful to convert sparse signals, whenever time quantization is not needed for further processing, such as for feature extraction using an SNN. Therefore this prototype enables improved energy efficiency in applications that can make use of spike-based processing.

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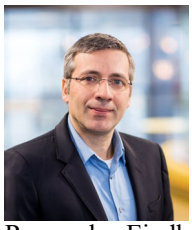

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