11.1 An Oversampled 12/14b SAR ADC with Noise Reduction and Linearity Enhancements Achieving up to 79.1dB SNDR

Pieter Harpe, Eugenio Cantatore, Arthur van Roermund

Eindhoven University of Technology, Eindhoven, The Netherlands

Autonomous wireless sensor nodes for cloud networks require ultra-low-power electronics. In particular, sensor readout interfaces need low-speed high-precision ADCs for capturing, e.g., bio-potential signals, environmental information, or interactive multimedia. For these applications, state-of-the-art SAR ADCs can provide highly power-efficient solutions (<10fJ/conversion-step) but with limited accuracy (SNDR <63dB) [1,2]. Alternatively, $\Delta\Sigma$ ADCs offer higher precision at the cost of lower efficiency (e.g. 84dB SNDR with 54fJ/conversion-step [3]). This work bridges the existing performance gap by extending the accuracy of low-power SAR ADCs to SNDRs in the order of 70-to-80dB. Feedback-controlled data-driven noise reduction [1], oversampling, chopping [4] and dithering [5] techniques are combined to increase both SNR and linearity in a power-efficient way. Various ADC modes are supported by making these techniques individually programmable, thereby extending the application range.

The 12b/14b SAR ADC is shown in Fig. 11.1.1. The asynchronous architecture allows the use of a single external clock at the sample-rate frequency. While nominally 14b, the 2-LSB cycles can be disabled to provide a 12b mode at lower power. The unit element in the differential capacitive DAC equals 0.55fF, leading to a total sampling capacitance of 9pF per side. This results in 88dB kT/C-related SNR at 0.8V supply for a rail-to-rail input. The 4 MSBs are thermometer-encoded to save switching energy. As 14b matching cannot be achieved intrinsically with such small capacitors, chopping and dithering are applied in combination with oversampling to improve the linearity.

Apart from suppressing DC offset and 1/f noise, chopping also modulates distortion components. Thus, by chopping at half the sampling rate and using oversampling, also the dominant even-order distortions are moved out of the signal bandwidth. This helps in particular to counteract the even-order distortions due to mismatch in the thermometer-encoded MSBs. The implementation of this scheme can be done with little power overhead (Fig. 11.1.1): the sampling clock f_s is divided by a factor of two, and two boosted clocks $\varphi1$, $\varphi2$ are generated to drive the NMOS sampling switches that also implement the input chopping. While requiring two clock boosters, each of them operates at half the sample rate; thus it does not increase the overall power consumption. The output chopping is performed in the digital domain and is implemented with a MUX that selects the output data either from the non-inverted or from the inverted output of the SAR register.

Whereas chopping cancels out even-order distortions, it does not reduce the odd-order terms. Due to the small unit capacitors, undesirable layout parasitics especially influence the binary-scaled LSBs as these parasitics are usually not perfectly binary-scaled. The thermometer bits are less prone to this problem as they re-use identical layouts rather than scaled ones. To reduce the distortion related to the binary part of the DAC, dithering is applied to randomize these errors (Fig. 11.1.1). A deterministic dither sequence with 4 or 16 levels is injected at the input of the ADC after sampling but before the actual AD conversion. The dither logic is a simple counter to create the desired fixed sequence, and a 4-capacitor DAC adds the actual sequence to the sampling node. As the dither is a deterministic pattern, it results in spurious tones at multiples of $f_s/4$ or $f_s/16$, dependent on the selected length of the sequence. In combination with oversampling, these tones will be outside the critical baseband. Therefore, it is possible to use large-range dither without requiring dither subtraction after the ADC. The dither range is set to approximately 700 LSB to average over all 10b of the binary array rather than over the LSBs only. The power consumption of the dither circuit is dominated by its capacitors. Since these are a small fraction of the total DAC capacitance (about 4%), the power consumption is similarly low.

Next to linearity, power-efficient low-noise performance is a second requisite to enable efficient high-precision SAR ADCs. While oversampling helps to improve SNR, the required 4× speed per 6dB improvement is rather costly. As the comparator is the dominant contributor for overall noise, a power-efficient data-driven noise reduction (DDNR) technique is applied to the comparator as shown in Fig. 11.1.2 [1]. In brief, the noise reduction is selectively done on the noise-critical bit-cycles by voting on multiple repetitive comparator decisions. The selection is done by triggering a reference delay cell together with the comparator. For large input signals that are not noise-critical, the comparator generates an output before the reference delay, and the decision is immediately provided to the SAR logic. In case the comparator is slow, which indicates a small input level that could be corrupted by noise, the decision is taken several times and the voting logic produces the majority value as the final output. The amount of noise reduction depends on two parameters: first, the number of votes (Nv) used in the voting process, as a higher number results in better noise averaging; and second, the number of voting cycles (Nc) per conversion. For example, when voting is only applied in the most noise-critical case, Nc equals 1. When voting is also applied in the second-most noise-critical case, Nc equals 2 and additional noise reduction is achieved. In [1], the number of votes Nv is fixed to 5 while the number of voting cycles Nc is manually set by tuning the bias voltage V_{bias} that controls the reference delay. For that reason, the approach is not autonomous and sensitive to PVT variations.

This work introduces a feedback loop around the DDNR method to enable reliable autonomous operation (Fig. 11.1.2). Moreover, the noise reduction is digitally programmable by setting the two critical parameters Nv and Nc. Nv is simply used in the digital voting logic to count the number of repetitive decisions. Nc is used to control the reference delay by means of a feedback loop that drives V_{bias}. The actual number of voting cycles is determined by counting the number of times a slow, noise-critical decision is detected during a conversion. This number is compared against the desired value Nc. Dependent on the comparison result V_{bias} is either increased or decreased by a charge or discharge pulse on C_1 through M_1, M_2. To achieve a slow time-constant in the loop without needing an excessively large capacitor C_1, transistors M_3 and M_4 are added. These transistors are biased in sub-threshold and thus create a large RC constant for the loop.

The implemented ADC occupies 0.18mm^2 in a 65nm CMOS technology (Fig. 11.1.7) and operates at 0.8V supply. Out of 5 measured samples, the chip with the lowest SNDR was selected for the measurements presented in this paper. Figure 11.1.3 shows the measured impact of the various enhancement techniques. In 14b mode at 128kS/s with 16× oversampling and f_{in} = 169.22Hz, the application of chopping, 16-level dithering and DDNR improves the SFDR by about 8dB and the SNDR by about 6dB. The figure also shows the measured programmability of the DDNR at 10kS/s. The input-referred noise (IRN) of the ADC reduces while the power consumption increases as more votes are used or more voting cycles are allowed during the conversion. In 12b mode, the IRN improvement is limited by the quantization noise. Figure 11.1.4 shows the measured INL and DNL for 12b and 14b mode without chopping, dithering and oversampling. The measured SFDR and SNDR versus input frequency are given in Fig. 11.1.5 for Nyquist-rate 12b/14b operation as well as 4×/16× oversampled 14b operation. The detailed settings and measured results for these 4 modes are summarized in Fig. 11.1.6 together with a comparison to prior art. The power-efficient enhancement techniques enable reaching an SNDR between 67.8dB and 79.1dB, dependent on the selected mode. This is relatively high as compared to previous low-power SAR ADCs [1,2]. Moreover, all 4 modes of operation achieve state-of-the-art power-efficiencies in both Walden and Schreier-based FoMs as compared to ADCs with similar SNDRs [6].

References:

[1] P. Harpe, E. Cantatore, and A. van Roermund, "A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with Data-Driven Noise Reduction," *ISSCC Dig. Tech. Papers*, pp. 270–271, Feb. 2013.

[2] C.-Y. Liou and C.-C. Hsieh, "A 2.4-to-5.2fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with Charge-Average Switching DAC in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 280–281, Feb. 2013.

[3] A.P. Perez, E. Bonizzoni, and F. Maloberti, "A 84dB SNDR 100kHz Bandwidth Low-Power Single Op-Amp Third-Order $\Delta\Sigma$ Modulator Consuming 140μW," *ISSCC Dig. Tech. Papers*, pp. 478 – 479, Feb. 2011.

[4] K.-C. Hsieh and P. Gray, "A Low-Noise Chopper-Stabilized Differential Switched-Capacitor Filtering Technique," *ISSCC Dig. Tech. Papers*, pp. 128–129, Feb. 1981.

[5] R.A. Wannamaker, *et al.*, "A Theory of Nonsubtractive Dither," *IEEE Trans. on Signal Processing*, pp. 499–516, Feb. 2000.

[6] B. Murmann, "ADC Performance Survey 1997-2013," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html, June 2013.

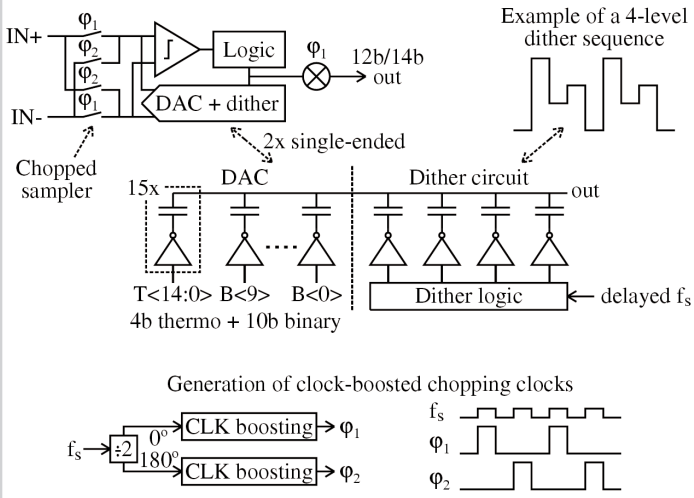

Figure 11.1.1: 12b/14b SAR ADC with chopping, dithering and segmented DAC.

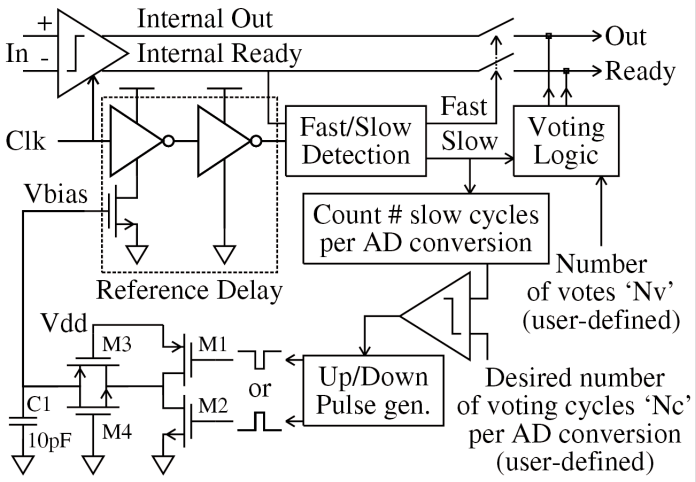

Figure 11.1.2: Closed-loop programmable Data-Driven Noise Reduction (DDNR) technique.

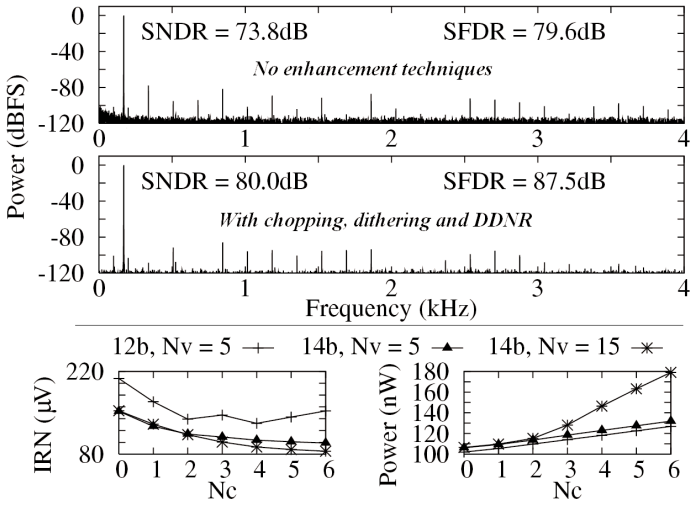

Figure 11.1.3: Spectrum without and with enhancement techniques, and influence of DDNR on IRN and power consumption.

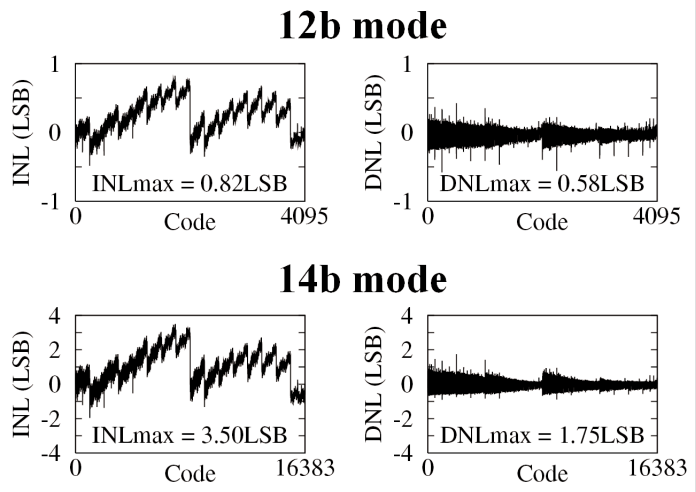

Figure 11.1.4: INL and DNL for 12b and 14b mode (without chopping, dithering and oversampling).

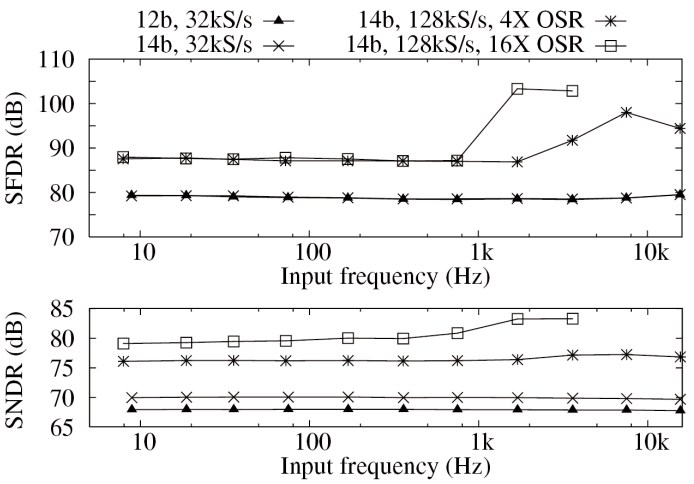

Figure 11.1.5: SFDR and SNDR versus input frequency for the different modes.

	[1]	[2]	[3]	This work			
Technology (nm)	65nm	90nm	180nm	65nm			
Area (mm²)	0.076	0.042	0.492	0.18			
Supply voltage (V)	0.6	0.4	1.5	0.8			
Resolution (bit)	12	10	-	12	14	14	14
Sample rate (kS/s)	40	500	3200	32	32	128	128
Oversampling ratio	-	-	16	-	-	4x	16x
Bandwidth (kHz)	20	250	100	16	16	16	4
#votes Nv, #cycles Nc	5, -	-	-	5, 2	5, 4	5, 4	5, 4
Chopping	-	-	-	Off	Off	On	On
Dithering	-	-	-	Off	Off	4-level	16-level
Power (μW)	0.097	0.5	140	0.310	0.352	1.367	1.370
INL (LSB)	1.90	0.5	-	0.82	3.50	-	-
DNL (LSB)	0.97	0.3	-	0.58	1.75	-	-
SFDR (dB)	68.8	81.3	96.0	78.4 *	78.5 *	86.9 *	87.1 *
SNDR (dB)	62.5	54.3	84.0	67.8 *	69.7 *	76.1 *	79.1 *
FOMW (fJ/conv.step)	2.2	2.4	54.0	4.8 *	4.4 *	8.2 *	23.2 *
FOMS (dB)	175.7	171.3	172.5	174.9 *	176.3 *	176.8 *	173.8 *

* Worst value across entire bandwidth

Figure 11.1.6: Performance summary and comparison.

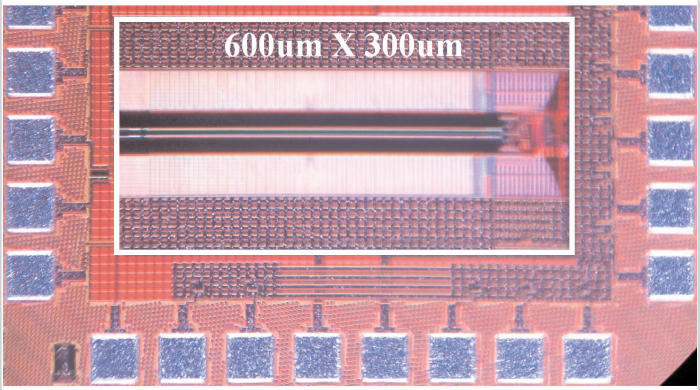

Figure 11.1.7: Die photo of the ADC in 65nm CMOS.

978-1-4799-0920-9/14/$31.00 ©2014 IEEE