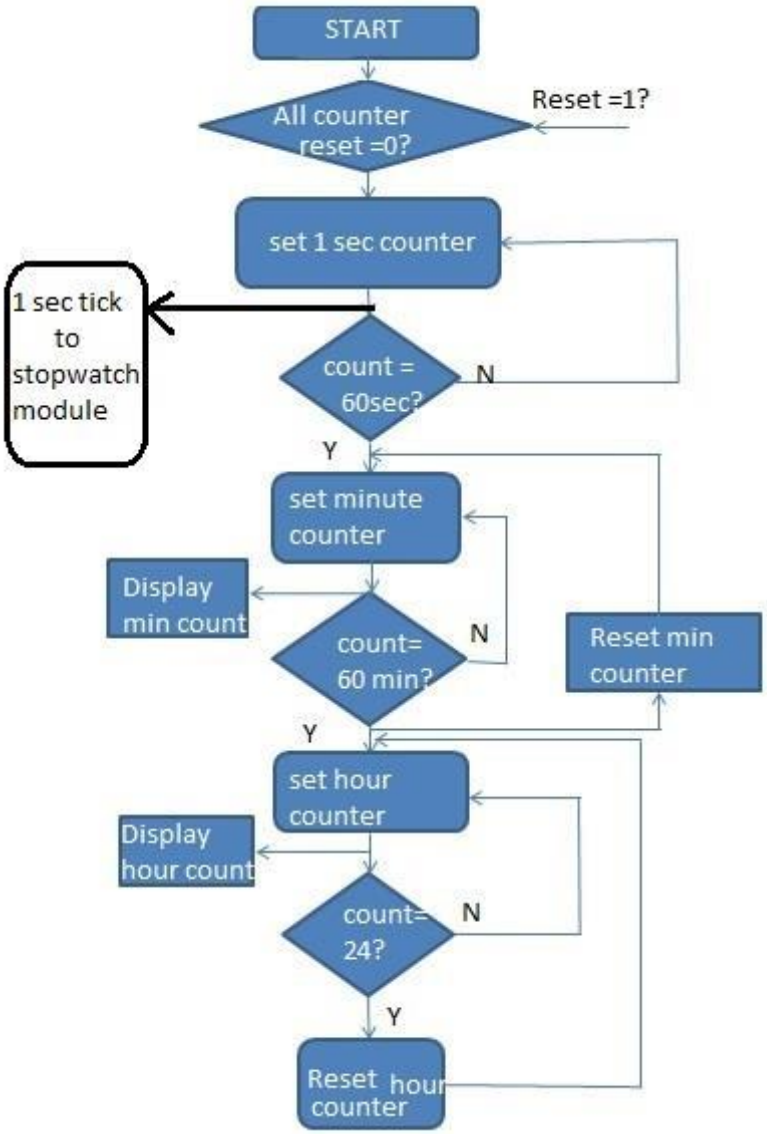

Flow chart of digital clock

Table 1 : Comparison of parameter for concurrent and sequential code .

S. No	Parameters	Concurrent Code	Sequential Code
A	***Device utilization report***		
1	Number of slices	87	88
2	Number of slice flip flop	80	80
3	Number of 4 input LUTs	170	173
B	***Timing report***		
1	Maximum frequency(MHz)	162.136	139.782
2	Minimum input required time after clock(nsec)	5.009	6.036
3	Maximum output required time before clock(nsec)	8.046	8.934
4	Maximum combinational path delay(nsec)	8.957	9.934
C	***Memory usage(kilobytes)***	263536	263568
D	***Power report***		
	Static power(mWatt)	33.59	81.53
2	Dynamic power (mWatt)	0.00	0.00
3	Total power(mWatt)	33.59	81.53