PSoC® Creator™
Project Datasheet for SmartMotorControl

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1 Overview

The Cypress PSoC 6 is a family of 32-bit devices with the following characteristics:

- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals such as PWM, UART, SPI and I2C
- Analog subsystem that includes 12-bit SAR ADC, comparators, op amps, CapSense, LCD drive and more
- Several types of memory elements, including SRAM and flash
- Programming and debug system through Serial Wire Debug (SWD)
- High-performance 32-bit ARM Cortex-M4 core with a nested vectored interrupt controller (NVIC)
- Flexible routing to all pins

Figure 1 shows the major components of a typical PSoC 62 series member PSoC 6 device. For details on all the systems listed above, please refer to the PSoC 6 Technical Reference Manual .

Figure 1. PSoC 62 Device Series Block Diagram

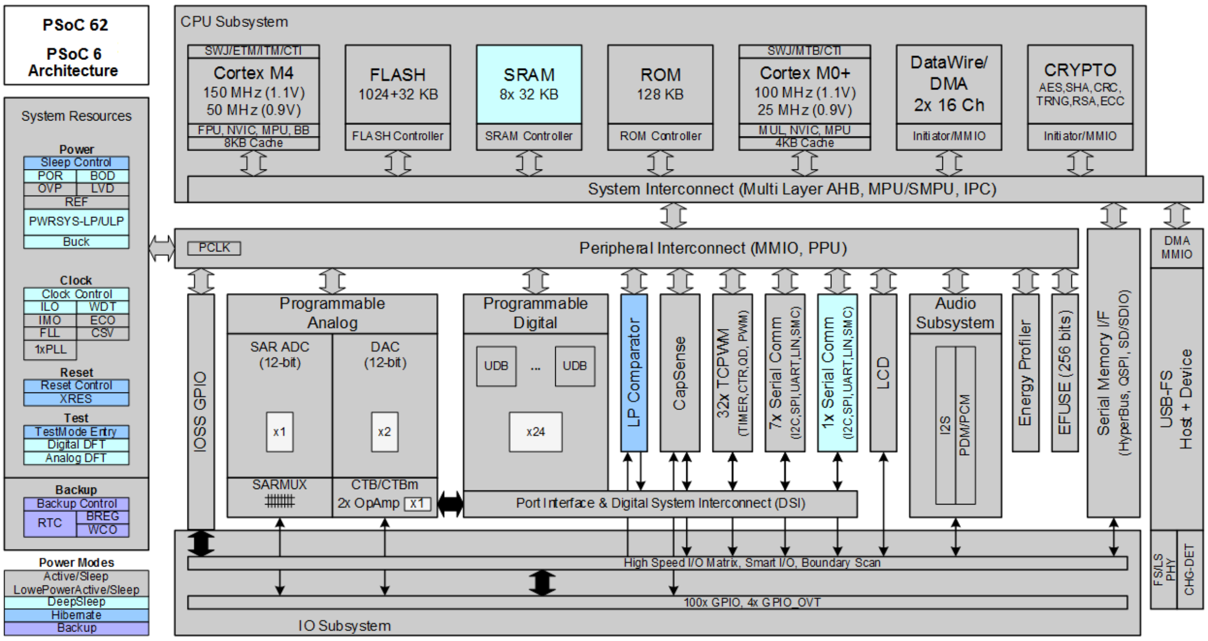


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C6247BZI-D54
Package Name	124-BGA
Family	PSoC 6
Series	PSoC 62
Max CPU speed (MHz)	150
Flash size (kB)	1024
SRAM size (kB)	288
Vdd range (V)	1.7 to 3.6
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

Table 2. Device Resources

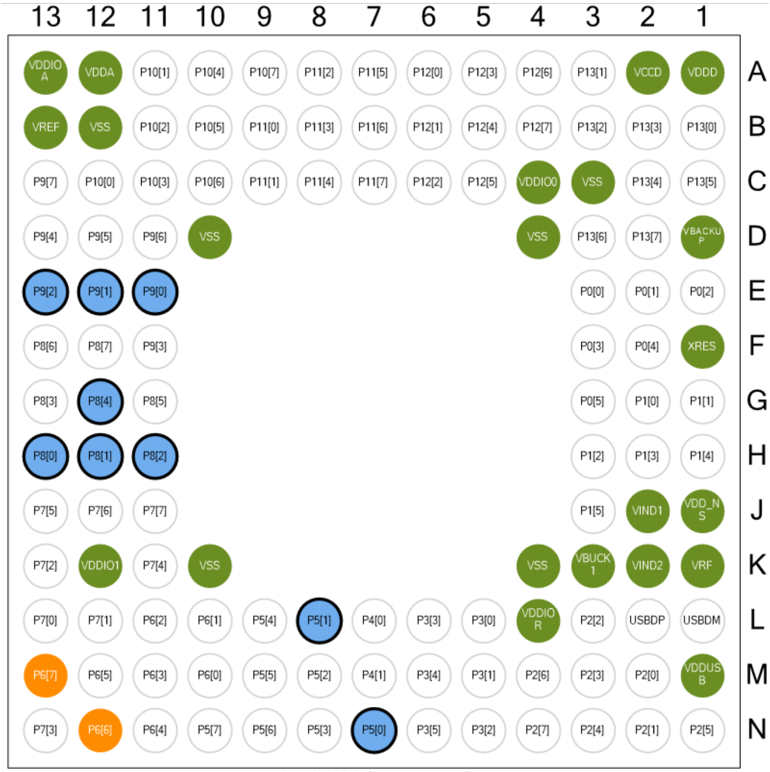
Resource Type	Used	Free	Max	% Used
Digital Clocks	0	8	8	0.00 %
Crypto Accelerator	0	1	1	0.00 %
Interrupts [CM0+]	5	27	32	15.63 %
Interrupts [CM4]	3	144	147	2.04 %
IO	11	91	102	10.78 %
Interprocessor Communication	0	16	16	0.00 %
MCWDT	0	2	2	0.00 %
CapSense	0	1	1	0.00 %
Energy Profiler	0	1	1	0.00 %
Real Time Clock	0	1	1	0.00 %
I2S	0	1	1	0.00 %
PDM/PCM	0	1	1	0.00 %
SCB	2	7	9	22.22 %
Serial Memory Interface	0	1	1	0.00 %
USB	0	1	1	0.00 %
DMA Channels	0	32	32	0.00 %
LCD	0	1	1	0.00 %
SmartIO	0	2	2	0.00 %
TCPWM	4	28	32	12.50 %
UDB				
Macrocells	0	96	96	0.00 %
Unique P-terms	0	192	192	0.00 %
Total P-terms	0			
Datapath Cells	0	12	12	0.00 %
Status Cells	0	12	12	0.00 %
Control Cells	0	12	12	0.00 %
7-Bit IDAC	0	2	2	0.00 %
Continuous Time DAC	0	1	1	0.00 %
LP Comparator	0	2	2	0.00 %
Opamp	0	2	2	0.00 %
Sample and Hold	0	1	1	0.00 %
SAR ADC	0	1	1	0.00 %

Resource Type	Used	Free	Max	% Used
DieTemp Sensor	0	1	1	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



	13	12	11	10	9	8	7	6	5	4	3	2	1
A	VDDIOA	VDDA	P10[1]	P10[4]	P10[7]	P11[2]	P11[5]	P12[0]	P12[3]	P12[6]	P13[1]	VCCD	VDDD
B	VREF	VSS	P10[2]	P10[5]	P11[0]	P11[3]	P11[6]	P12[1]	P12[4]	P12[7]	P13[2]	P13[3]	P13[0]
C	P9[7]	P10[0]	P10[3]	P10[6]	P11[1]	P11[4]	P11[7]	P12[2]	P12[5]	VDDIO0	VSS	P13[4]	P13[5]
D	P9[4]	P9[5]	P9[6]	VSS						VSS	P13[6]	P13[7]	VBACKUP
E	P9[2]	P9[1]	P9[0]								P0[0]	P0[1]	P0[2]
F	P8[6]	P8[7]	P9[3]								P0[3]	P0[4]	XRES
G	P8[3]	P8[4]	P8[5]								P0[5]	P1[0]	P1[1]
H	P8[0]	P8[1]	P8[2]								P1[2]	P1[3]	P1[4]
J	P7[5]	P7[6]	P7[7]								P1[5]	VIND1	VDD_NS
K	P7[2]	VDDIO1	P7[4]	VSS						VSS	VBUCK1	VIND2	VRF
L	P7[0]	P7[1]	P6[2]	P6[1]	P5[4]	P5[1]	P4[0]	P3[3]	P3[0]	VDDIOR	P2[2]	USBDP	USBDM
M	P6[7]	P6[5]	P6[3]	P6[0]	P5[5]	P5[2]	P4[1]	P3[4]	P3[1]	P2[6]	P2[3]	P2[0]	VDDUSB
N	P7[3]	P6[6]	P6[4]	P5[7]	P5[6]	P5[3]	P5[0]	P3[5]	P3[2]	P2[7]	P2[4]	P2[1]	P2[5]

CY8C6247BZI-D54
124-BGA
(bottom view)

2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode
1	VDDD	VDDD	Power	
2	VCCD	VCCD	Power	
3	P13[1]	GPIO [unused]		
4	P12[6]	GPIO [unused]		
5	P12[3]	GPIO [unused]		
6	P12[0]	GPIO [unused]		
7	P11[5]	GPIO [unused]		
8	P11[2]	GPIO [unused]		
9	P10[7]	GPIO [unused]		
10	P10[4]	GPIO [unused]		
11	P10[1]	GPIO [unused]		
12	VDDA	VDDA	Power	
13	VDDIOA	VDDIOA	Power	
14	P13[0]	GPIO [unused]		
15	P13[3]	GPIO [unused]		
16	P13[2]	GPIO [unused]		
17	P12[7]	GPIO [unused]		
18	P12[4]	GPIO [unused]		
19	P12[1]	GPIO [unused]		
20	P11[6]	GPIO [unused]		
21	P11[3]	GPIO [unused]		
22	P11[0]	GPIO [unused]		
23	P10[5]	GPIO [unused]		
24	P10[2]	GPIO [unused]		
25	VSS	VSS	Power	
26	VREF	VREF	Dedicated	
27	P13[5]	GPIO [unused]		
28	P13[4]	GPIO [unused]		
29	VSS	VSS	Power	
30	VDDIO0	VDDIO0	Power	
31	P12[5]	GPIO [unused]		
32	P12[2]	GPIO [unused]		
33	P11[7]	GPIO [unused]		
34	P11[4]	GPIO [unused]		
35	P11[1]	GPIO [unused]		
36	P10[6]	GPIO [unused]		
37	P10[3]	GPIO [unused]		
38	P10[0]	GPIO [unused]		
39	P9[7]	GPIO [unused]		
40	VBACKUP	VBACKUP	Power	
41	P13[7]	GPIO [unused]		
42	P13[6]	GPIO [unused]		
43	VSS	VSS	Power	
49	VSS	VSS	Power	
50	P9[6]	GPIO [unused]		

Pin	Port	Name	Type	Drive Mode
51	P9[5]	GPIO [unused]		
52	P9[4]	GPIO [unused]		
53	P0[2]	GPIO [unused]		
54	P0[1]	GPIO [unused]		
55	P0[0]	GPIO [unused]		
63	P9[0]	DcMotorSpeed	Dgtl Out	Strong drive
64	P9[1]	DirectionInput1	Software In/Out	Strong drive
65	P9[2]	DirectionInput2	Software In/Out	Strong drive
66	XRES	XRES	Dedicated	
67	P0[4]	GPIO [unused]		
68	P0[3]	GPIO [unused]		
76	P9[3]	GPIO [unused]		
77	P8[7]	GPIO [unused]		
78	P8[6]	GPIO [unused]		
79	P1[1]	OVT IO [unused]		
80	P1[0]	OVT IO [unused]		
81	P0[5]	GPIO [unused]		
89	P8[5]	GPIO [unused]		
90	P8[4]	ServoPositionControl	Dgtl Out	Strong drive
91	P8[3]	GPIO [unused]		
92	P1[4]	OVT IO [unused]		
93	P1[3]	OVT IO [unused]		
94	P1[2]	OVT IO [unused]		
102	P8[2]	LidarMotorSpeed	Dgtl Out	Strong drive
103	P8[1]	\LidarUart:tx\	Dgtl Out	Strong drive
104	P8[0]	\LidarUart:rx\	Dgtl In	HiZ analog
105	VDD_NS	VDD_NS	Power	
106	VIND1	VIND1	Dedicated	
107	P1[5]	OVT IO [unused]		
115	P7[7]	GPIO [unused]		
116	P7[6]	GPIO [unused]		
117	P7[5]	GPIO [unused]		
118	VRF	VRF	Power	
119	VIND2	VIND2	Dedicated	
120	VBUCK1	VBUCK1	Power	
121	VSS	VSS	Power	
127	VSS	VSS	Power	
128	P7[4]	GPIO [unused]		
129	VDDIO1	VDDIO1	Power	
130	P7[2]	GPIO [unused]		
131	USBDM	USB IO [unused]		
132	USBDP	USB IO [unused]		
133	P2[2]	GPIO [unused]		
134	VDDIOR	GPIO [unused], Power		
135	P3[0]	GPIO [unused]		
136	P3[3]	GPIO [unused]		
137	P4[0]	GPIO [unused]		
138	P5[1]	\ExternalUart:tx\	Dgtl Out	Strong drive
139	P5[4]	GPIO [unused]		
140	P6[1]	GPIO [unused]		
141	P6[2]	GPIO [unused]		
142	P7[1]	GPIO [unused]		

Pin	Port	Name	Type	Drive Mode
143	P7[0]	GPIO [unused]		
144	VDDUSB	VDDUSB	Power	
145	P2[0]	GPIO [unused]		
146	P2[3]	GPIO [unused]		
147	P2[6]	GPIO [unused]		
148	P3[1]	GPIO [unused]		
149	P3[4]	GPIO [unused]		
150	P4[1]	GPIO [unused]		
151	P5[2]	GPIO [unused]		
152	P5[5]	GPIO [unused]		
153	P6[0]	GPIO [unused]		
154	P6[3]	GPIO [unused]		
155	P6[5]	GPIO [unused]		
156	P6[7]	GPIO [unused]	Dgtl In	Res pull down
157	P2[5]	GPIO [unused]		
158	P2[1]	GPIO [unused]		
159	P2[4]	GPIO [unused]		
160	P2[7]	GPIO [unused]		
161	P3[2]	GPIO [unused]		
162	P3[5]	GPIO [unused]		
163	P5[0]	\ExternalUart:rx\	Dgtl In	HiZ analog
164	P5[3]	GPIO [unused]		
165	P5[6]	GPIO [unused]		
166	P5[7]	GPIO [unused]		
167	P6[4]	GPIO [unused]		
168	P6[6]	GPIO [unused]	Dgtl In	Res pull up
169	P7[3]	GPIO [unused]		

Abbreviations used in Table 3 have the following meanings:

- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- HiZ analog = High impedance analog
- Res pull down = Resistive pull down
- Res pull up = Resistive pull up

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode
P0[0]	55	GPIO [unused]		
P0[1]	54	GPIO [unused]		
P0[2]	53	GPIO [unused]		
P0[3]	68	GPIO [unused]		
P0[4]	67	GPIO [unused]		
P0[5]	81	GPIO [unused]		
P1[0]	80	OVT IO [unused]		
P1[1]	79	OVT IO [unused]		
P1[2]	94	OVT IO [unused]		
P1[3]	93	OVT IO [unused]		
P1[4]	92	OVT IO [unused]		
P1[5]	107	OVT IO [unused]		
P10[0]	38	GPIO [unused]		
P10[1]	11	GPIO [unused]		
P10[2]	24	GPIO [unused]		
P10[3]	37	GPIO [unused]		
P10[4]	10	GPIO [unused]		
P10[5]	23	GPIO [unused]		
P10[6]	36	GPIO [unused]		
P10[7]	9	GPIO [unused]		
P11[0]	22	GPIO [unused]		
P11[1]	35	GPIO [unused]		
P11[2]	8	GPIO [unused]		
P11[3]	21	GPIO [unused]		
P11[4]	34	GPIO [unused]		
P11[5]	7	GPIO [unused]		
P11[6]	20	GPIO [unused]		
P11[7]	33	GPIO [unused]		
P12[0]	6	GPIO [unused]		
P12[1]	19	GPIO [unused]		
P12[2]	32	GPIO [unused]		
P12[3]	5	GPIO [unused]		
P12[4]	18	GPIO [unused]		
P12[5]	31	GPIO [unused]		
P12[6]	4	GPIO [unused]		
P12[7]	17	GPIO [unused]		
P13[0]	14	GPIO [unused]		
P13[1]	3	GPIO [unused]		
P13[2]	16	GPIO [unused]		
P13[3]	15	GPIO [unused]		
P13[4]	28	GPIO [unused]		
P13[5]	27	GPIO [unused]		
P13[6]	42	GPIO [unused]		
P13[7]	41	GPIO [unused]		
P2[0]	145	GPIO [unused]		

Port	Pin	Name	Type	Drive Mode
P2[1]	158	GPIO [unused]		
P2[2]	133	GPIO [unused]		
P2[3]	146	GPIO [unused]		
P2[4]	159	GPIO [unused]		
P2[5]	157	GPIO [unused]		
P2[6]	147	GPIO [unused]		
P2[7]	160	GPIO [unused]		
P3[0]	135	GPIO [unused]		
P3[1]	148	GPIO [unused]		
P3[2]	161	GPIO [unused]		
P3[3]	136	GPIO [unused]		
P3[4]	149	GPIO [unused]		
P3[5]	162	GPIO [unused]		
P4[0]	137	GPIO [unused]		
P4[1]	150	GPIO [unused]		
P5[0]	163	\ExternalUart:rx\	Dgtl In	HiZ analog
P5[1]	138	\ExternalUart:tx\	Dgtl Out	Strong drive
P5[2]	151	GPIO [unused]		
P5[3]	164	GPIO [unused]		
P5[4]	139	GPIO [unused]		
P5[5]	152	GPIO [unused]		
P5[6]	165	GPIO [unused]		
P5[7]	166	GPIO [unused]		
P6[0]	153	GPIO [unused]		
P6[1]	140	GPIO [unused]		
P6[2]	141	GPIO [unused]		
P6[3]	154	GPIO [unused]		
P6[4]	167	GPIO [unused]		
P6[5]	155	GPIO [unused]		
P6[6]	168	GPIO [unused]	Dgtl In	Res pull up
P6[7]	156	GPIO [unused]	Dgtl In	Res pull down
P7[0]	143	GPIO [unused]		
P7[1]	142	GPIO [unused]		
P7[2]	130	GPIO [unused]		
P7[3]	169	GPIO [unused]		
P7[4]	128	GPIO [unused]		
P7[5]	117	GPIO [unused]		
P7[6]	116	GPIO [unused]		
P7[7]	115	GPIO [unused]		
P8[0]	104	\LidarUart:rx\	Dgtl In	HiZ analog
P8[1]	103	\LidarUart:tx\	Dgtl Out	Strong drive
P8[2]	102	LidarMotorSpeed	Dgtl Out	Strong drive
P8[3]	91	GPIO [unused]		
P8[4]	90	ServoPositionControl	Dgtl Out	Strong drive
P8[5]	89	GPIO [unused]		
P8[6]	78	GPIO [unused]		
P8[7]	77	GPIO [unused]		
P9[0]	63	DcMotorSpeed	Dgtl Out	Strong drive
P9[1]	64	DirectionInput1	Software In/Out	Strong drive
P9[2]	65	DirectionInput2	Software In/Out	Strong drive
P9[3]	76	GPIO [unused]		

Port	Pin	Name	Type	Drive Mode
P9[4]	52	GPIO [unused]		
P9[5]	51	GPIO [unused]		
P9[6]	50	GPIO [unused]		
P9[7]	39	GPIO [unused]		
USBDM	131	USB IO [unused]		
USBDP	132	USB IO [unused]		

Abbreviations used in Table 4 have the following meanings:

- Dgtl In = Digital Input
- HiZ analog = High impedance analog
- Dgtl Out = Digital Output
- Res pull up = Resistive pull up
- Res pull down = Resistive pull down

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
\ExternalUart:rx\	P5[0]	Dgtl In
\ExternalUart:tx\	P5[1]	Dgtl Out
\LidarUart:rx\	P8[0]	Dgtl In
\LidarUart:tx\	P8[1]	Dgtl Out
DcMotorSpeed	P9[0]	Dgtl Out
DirectionInput1	P9[1]	Software In/Out
DirectionInput2	P9[2]	Software In/Out
GPIO [unused]	P5[4]	
GPIO [unused]	P7[2]	
GPIO [unused]	P7[4]	
GPIO [unused]	P3[0]	
GPIO [unused]	P3[3]	
GPIO [unused]	P2[2]	
GPIO [unused]	P4[0]	
GPIO [unused]	P7[3]	
GPIO [unused]	P8[5]	
GPIO [unused]	P8[6]	
GPIO [unused]	P9[3]	
GPIO [unused]	P8[7]	
GPIO [unused]	P7[6]	
GPIO [unused]	P7[5]	
GPIO [unused]	P7[7]	
GPIO [unused]	P8[3]	
GPIO [unused]	P0[3]	
GPIO [unused]	P6[1]	
GPIO [unused]	P2[1]	
GPIO [unused]	P2[4]	
GPIO [unused]	P2[7]	
GPIO [unused]	P6[5]	
GPIO [unused]	P6[7]	Dgtl In
GPIO [unused]	P2[5]	
GPIO [unused]	P3[2]	
GPIO [unused]	P5[7]	
GPIO [unused]	P6[4]	
GPIO [unused]	P6[6]	Dgtl In
GPIO [unused]	P3[5]	
GPIO [unused]	P5[3]	
GPIO [unused]	P5[6]	
GPIO [unused]	P2[0]	
GPIO [unused]	P2[3]	
GPIO [unused]	P2[6]	
GPIO [unused]	P6[2]	
GPIO [unused]	P7[1]	
GPIO [unused]	P7[0]	

Name	Port	Type
GPIO [unused]	P3[1]	
GPIO [unused]	P5[5]	
GPIO [unused]	P6[0]	
GPIO [unused]	P6[3]	
GPIO [unused]	P3[4]	
GPIO [unused]	P4[1]	
GPIO [unused]	P5[2]	
GPIO [unused]	P10[5]	
GPIO [unused]	P10[2]	
GPIO [unused]	P13[5]	
GPIO [unused]	P11[0]	
GPIO [unused]	P12[1]	
GPIO [unused]	P11[6]	
GPIO [unused]	P11[3]	
GPIO [unused]	P11[4]	
GPIO [unused]	P11[1]	
GPIO [unused]	P10[6]	
GPIO [unused]	P11[7]	
GPIO [unused]	P13[4]	
GPIO [unused]	P12[5]	
GPIO [unused]	P12[2]	
GPIO [unused]	P12[4]	
GPIO [unused]	P12[0]	
GPIO [unused]	P11[5]	
GPIO [unused]	P11[2]	
GPIO [unused]	P12[3]	
GPIO [unused]	P0[5]	
GPIO [unused]	P13[1]	
GPIO [unused]	P12[6]	
GPIO [unused]	P13[3]	
GPIO [unused]	P13[2]	
GPIO [unused]	P12[7]	
GPIO [unused]	P13[0]	
GPIO [unused]	P10[7]	
GPIO [unused]	P10[4]	
GPIO [unused]	P10[1]	
GPIO [unused]	P13[6]	
GPIO [unused]	P10[0]	
GPIO [unused]	P0[2]	
GPIO [unused]	P9[7]	
GPIO [unused]	P13[7]	
GPIO [unused]	P9[6]	
GPIO [unused]	P9[5]	
GPIO [unused]	P9[4]	
GPIO [unused]	P10[3]	
GPIO [unused]	P0[4]	
GPIO [unused]	P0[0]	
GPIO [unused]	P0[1]	
LidarMotorSpeed	P8[2]	Dgtl Out
OVT IO [unused]	P1[4]	
OVT IO [unused]	P1[5]	
OVT IO [unused]	P1[3]	
OVT IO [unused]	P1[1]	

Name	Port	Type
OVT IO [unused]	P1[2]	
OVT IO [unused]	P1[0]	
ServoPositionControl	P8[4]	Dgtl Out
USB IO [unused]	USBDP	
USB IO [unused]	USBDM	

Abbreviations used in Table 5 have the following meanings:

- Dgtl In = Digital Input
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Allow but warn

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD (serial wire debug)
Embedded Trace (ETM)	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

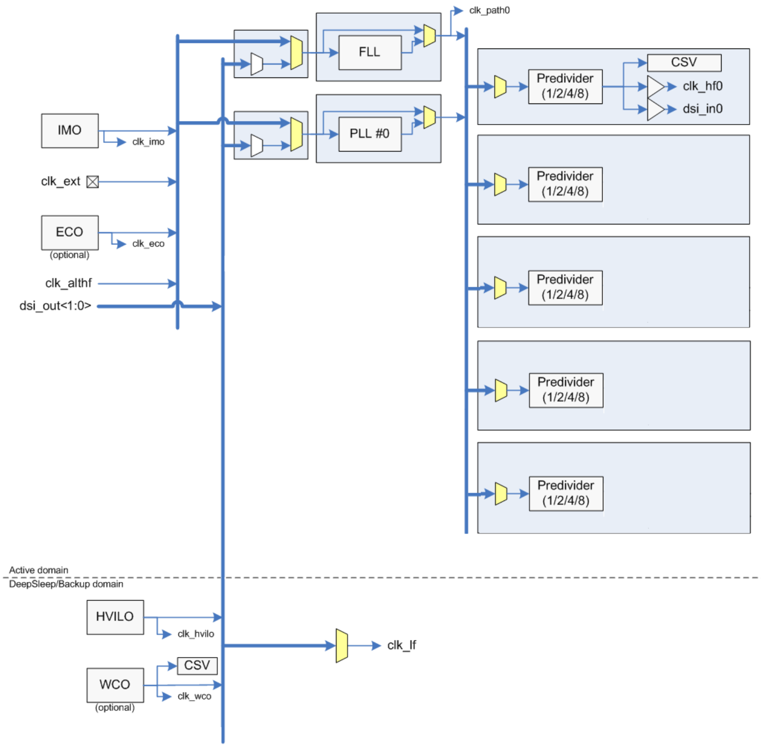
Name	Value
Power Mode	1.1V LDO Linear Regulator
External PMIC Output	Disabled
vBackup Source	VDDD
VBACKUP (V)	3.3
VDD_NS (V)	3.3
VDDA (V)	3.3
VDDD (V)	3.3
VDDIO0 (V)	3.3
VDDIO1 (V)	3.3
VDDIOA (V)	3.3
VDDIOR (V)	3.3
VDDUSB (V)	3.3
Variable VDDA	False

4 Clocks

The clock system includes these clock resources:

- Multiple internal clock sources:
  - 8 MHz Internal Main Oscillator (IMO) ±1%
  - 32 kHz Internal Low Speed Oscillator (ILO) ±30% output
  - 32.768 kHz Precision Internal Low Speed Oscillator (PILO) ±2% output
- Internal FLL and PLL can be used to increase frequency generated by HF clock sources
- Source clocks, FLL, and PLL can be used to drive 5 separate HF clocks
- HFCLK0 can be used to drive peripherals and UDBs
- LFCLK is typically used for DeepSleep wakeup timer

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
Clk_HF0	NONE	FLL	100 MHz	100 MHz	±2.4	True	True
FLL	NONE	PathMux0	100 MHz	100 MHz	±2.4	True	True
Clk_Fast	NONE	Clk_HF0	100 MHz	100 MHz	±2.4	True	True
Clk_Slow	NONE	Clk_Peri	50 MHz	50 MHz	±2.4	True	True
Clk_Peri	NONE	Clk_HF0	50 MHz	50 MHz	±2.4	True	True
Clk_Pump	NONE	FLL	25 MHz	25 MHz	±2.4	True	True
PathMux4	NONE	IMO	8 MHz	8 MHz	±1	True	True
Clk_Timer	NONE	IMO	8 MHz	8 MHz	±1	True	True
IMO	NONE		8 MHz	8 MHz	±1	True	True
PathMux0	NONE	IMO	8 MHz	8 MHz	±1	True	True
PathMux1	NONE	IMO	8 MHz	8 MHz	±1	True	True
PathMux3	NONE	IMO	8 MHz	8 MHz	±1	True	True
PathMux2	NONE	IMO	8 MHz	8 MHz	±1	True	True
Clk_Bak	NONE	Clk_LF	32 kHz	32 kHz	±10	True	True
Clk_LF	NONE	ILO	32 kHz	32 kHz	±10	True	True
Clk_AltSysTick	NONE	Clk_LF	32 kHz	32 kHz	±10	True	True
ILO	NONE		32 kHz	32 kHz	±10	True	True
PILO	NONE		32.768 kHz	? MHz	±2	False	False
ExtClk	NONE		24 MHz	? MHz	±0	False	False
Clk_HF1	NONE	FLL	? MHz	? MHz	±0	False	False
WCO	NONE		32.768 kHz	? MHz	±0.015	False	False
Clk_HF3	NONE	FLL	? MHz	? MHz	±0	False	False
Clk_HF2	NONE	FLL	? MHz	? MHz	±0	False	False
PLL0	NONE	PathMux1	100 MHz	? MHz	±0	False	False
Clk_HF4	NONE	FLL	? MHz	? MHz	±0	False	False
ECO	NONE		24 MHz	? MHz	±0	False	False
DigSig1	NONE		? MHz	? MHz	±0	False	False
DigSig2	NONE		? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

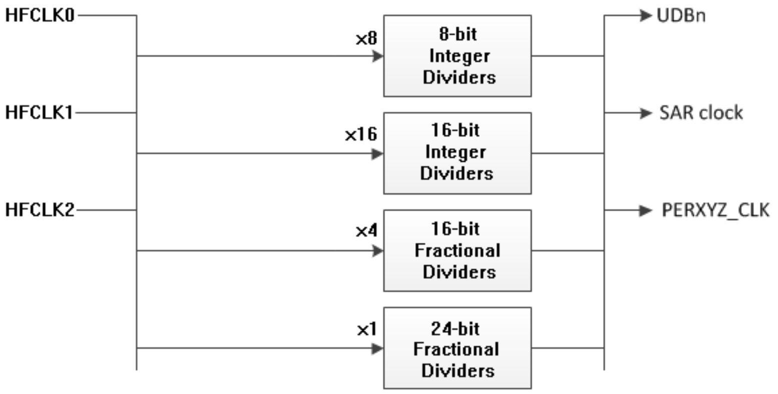


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
ExternalUart_-SCBCLK	UNKNOWN	Clk_Peri	1.382 MHz	1.389 MHz	±2.4	True	True
LidarUart_-SCBCLK	UNKNOWN	Clk_Peri	1.382 MHz	1.389 MHz	±2.4	True	True
LidarMotorC-lock	UNKNOWN	Clk_Peri	1 MHz	1 MHz	±2.4	True	True
SpeedClock	UNKNOWN	Clk_Peri	1 MHz	1 MHz	±2.4	True	True
ServoClock	UNKNOWN	Clk_Peri	1 MHz	1 MHz	±2.4	True	True
Clock	UNKNOWN	Clk_Peri	1 kHz	1 kHz	±2.4	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 6 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CySysClkImo API routines
  - CySysClkIlo API routines
  - CySysClkEco API routines
  - CySysClkWco API routines
  - CySysClkWrite API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	CortexM0p Vector	CortexM0p Priority	CortexM4 Vector	CortexM4 Priority	Deep Sleep Wakeup Capable
LidarUart_SCB_IRQ	45			45	7	No
ExternalUart_SCB_IRQ	46			46	7	No
OneMsInterrupt	90			90	7	No

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 6 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 6 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

This design has no flash protection specified; all blocks are unprotected.

For more information on Flash memory and protection, please refer to:

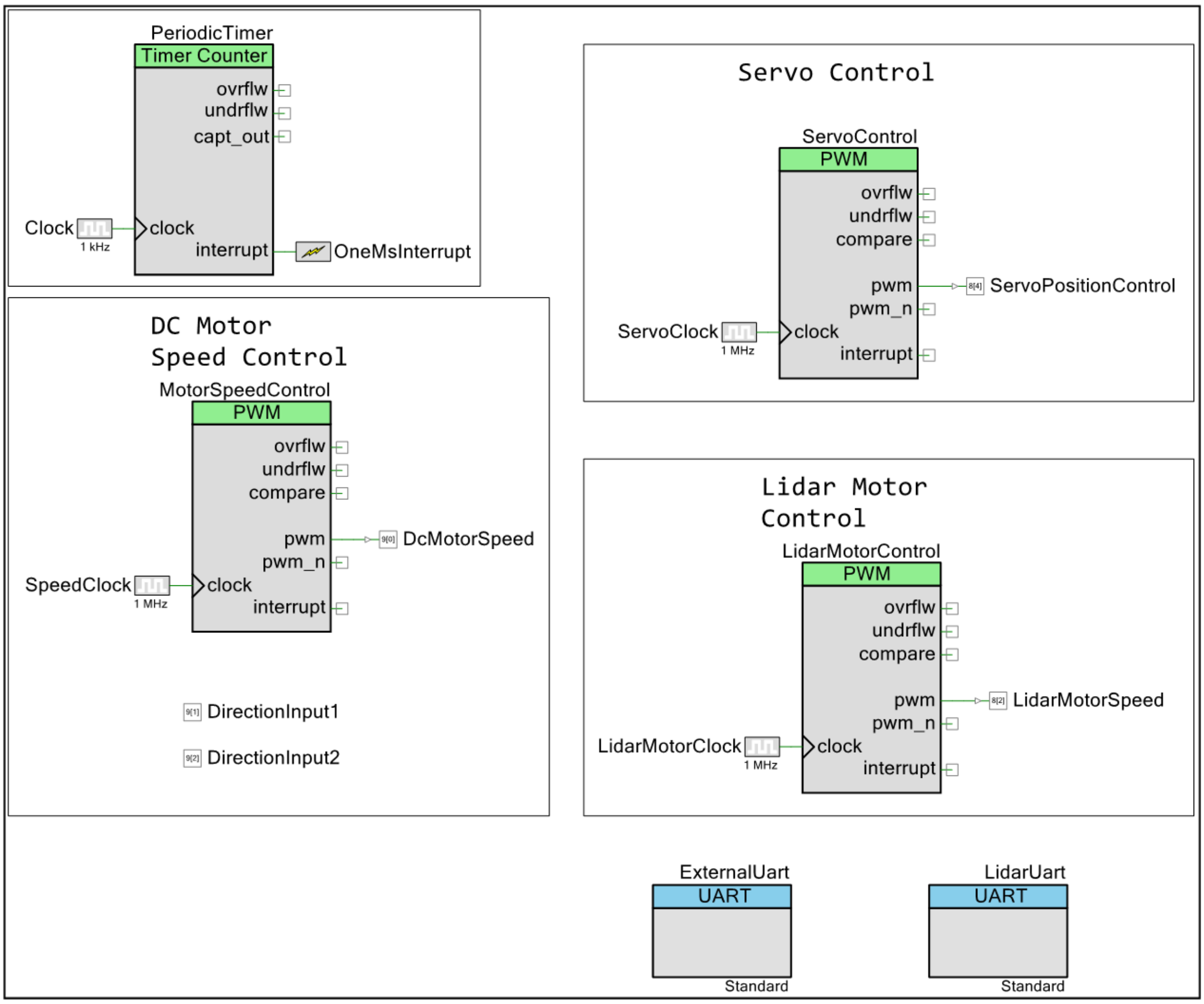
- Flash Protection chapter in the PSoC 6 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CySysFlash API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance ExternalUart (type: SCB_UART_PDL_v2_0)
- Instance LidarMotorControl (type: TCPWM_PWM_PDL_v1_0)
- Instance LidarUart (type: SCB_UART_PDL_v2_0)
- Instance MotorSpeedControl (type: TCPWM_PWM_PDL_v1_0)
- Instance PeriodicTimer (type: TCPWM_Counter_PDL_v1_0)
- Instance ServoControl (type: TCPWM_PWM_PDL_v1_0)

8 Components

8.1 Component type: SCB_UART_PDL [v2.0]

8.1.1 Instance ExternalUart

Description: UART (SCB) communications interface
Instance type: SCB_UART_PDL [v2.0]
Datasheet: online component datasheet for SCB_UART_PDL

Table 12. Component Parameters for ExternalUart

Parameter Name	Value	Description
Baud Rate (bps)	115200	This parameter specifies the baud rate in bps. The actual baud rate may differ based on the available clock frequency and Component settings. Range: 1 - 1000000 bps.
Bit Order	LSB First	This parameter defines the direction in which the serial data is transmitted. When set to the MSB first, the most-significant bit is transmitted first. When set to the LSB first, the least-significant bit is transmitted first.
Break Signal Bits	11	This parameter specifies the break width in bits. The range: 7-16.
Com Mode	Standard	This parameter defines the sub-mode of UART as: Standard, SmartCard or IrDA.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
CTS	false	This parameter enables the cts input.
Data Width	8 bits	This option defines the width of a single data element in bits. The range: 4-9.
Drop on Frame Error	false	This parameter determines if the data is dropped from the RX FIFO on a frame error event.
Enable Clock from Terminal	false	This parameter allows choosing between an internally configured clock (by the component) or an externally configured clock (by the user) for the component operation.
Enable Digital Filter	false	This parameter applies a digital 3-tap median filter to the UART input lines.
Interrupt	Internal	This parameter allows choosing between Internal and External placement of the Interrupt Component.

Parameter Name	Value	Description
Oversample	12	This parameter defines how many Component clocks oversample the selected baud rate. The range: 8 - 16 (except IrDA mode). The oversample values are predefined for IrDA mode.
Parity	None	This parameter defines the functionality of the parity bit location in the transfer as None, Odd or Even.
RTS	false	This parameter enables the rts output.
RX Output	false	This parameter enables the RX trigger output terminal (rx_dma) of the component. This terminal must be connected to the DMA trigger input or left unconnected.
Show UART Terminals	false	This parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins or SmartIO component.
Stop Bits	1	This parameter defines the number of stop bits.
TX Output	false	This parameter enables the TX trigger output terminal (rx_dma) of the component. This terminal must be connected to the DMA trigger input or left unconnected.
TX/RX Mode	TX + RX	This parameter enables the receiver or transmitter functionality or both simultaneously.
TX-Enable	false	This parameter enables TX_EN output.
User Comments		Instance-specific comments.

8.1.2 Instance LidarUart

Description: UART (SCB) communications interface
Instance type: SCB_UART_PDL [v2.0]
Datasheet: online component datasheet for SCB_UART_PDL

Table 13. Component Parameters for LidarUart

Parameter Name	Value	Description
Baud Rate (bps)	115200	This parameter specifies the baud rate in bps. The actual baud rate may differ based on the available clock frequency and Component settings. Range: 1 - 1000000 bps.

Parameter Name	Value	Description
Bit Order	LSB First	This parameter defines the direction in which the serial data is transmitted. When set to the MSB first, the most-significant bit is transmitted first. When set to the LSB first, the least-significant bit is transmitted first.
Break Signal Bits	11	This parameter specifies the break width in bits. The range: 7-16.
Com Mode	Standard	This parameter defines the sub-mode of UART as: Standard, SmartCard or IrDA.
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
CTS	false	This parameter enables the cts input.
Data Width	8 bits	This option defines the width of a single data element in bits. The range: 4-9.
Drop on Frame Error	false	This parameter determines if the data is dropped from the RX FIFO on a frame error event.
Enable Clock from Terminal	false	This parameter allows choosing between an internally configured clock (by the component) or an externally configured clock (by the user) for the component operation.
Enable Digital Filter	false	This parameter applies a digital 3-tap median filter to the UART input lines.
Interrupt	Internal	This parameter allows choosing between Internal and External placement of the Interrupt Component.
Oversample	12	This parameter defines how many Component clocks oversample the selected baud rate. The range: 8 - 16 (except IrDA mode). The oversample values are predefined for IrDA mode.
Parity	None	This parameter defines the functionality of the parity bit location in the transfer as None, Odd or Even.
RTS	false	This parameter enables the rts output.
RX Output	false	This parameter enables the RX trigger output terminal (rx_dma) of the component. This terminal must be connected to the DMA trigger input or left unconnected.

Parameter Name	Value	Description
Show UART Terminals	false	This parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins or SmartIO component.
Stop Bits	1	This parameter defines the number of stop bits.
TX Output	false	This parameter enables the TX trigger output terminal (rx_dma) of the component. This terminal must be connected to the DMA trigger input or left unconnected.
TX/RX Mode	TX + RX	This parameter enables the receiver or transmitter functionality or both simultaneously.
TX-Enable	false	This parameter enables TX_EN output.
User Comments		Instance-specific comments.

8.2 Component type: TCPWM_Counter_PDL [v1.0]

8.2.1 Instance PeriodicTimer

Description: This component implements a Timer/Counter using the TCPWM hardware block
Instance type: TCPWM_Counter_PDL [v1.0]
Datasheet: online component datasheet for TCPWM_Counter_PDL

Table 14. Component Parameters for PeriodicTimer

Parameter Name	Value	Description
Capture Input	Disabled	This parameter determines if a Capture terminal is displayed on the schematic
Clock Prescaler	Divide by 1	Divides down the input clock
Compare or Capture	Capture	Selects the mode for the compare capture register
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Count Direction	Up	Selects the direction the counter counts
Count Input	Disabled	Determines if a count input is needed and how that input is registered
Interrupt Source	Overflow/Underflow	Selects which events can trigger an interrupt
Period	32768	Sets the period of the Timer/Counter. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
Reload Input	Disabled	Determines if a reload input is needed and how the reload signal input is registered
Resolution	16-bits	Selects the size of the counter

Parameter Name	Value	Description
Run Mode	Continuous	If Continuous is selected counter runs forever. If One Shot is selected counter runs for one period and stops
Start Input	Disabled	Determines if a start input is needed and how that input is registered
Stop Input	Disabled	Determines if a stop input is needed and how that input is registered
User Comments		Instance-specific comments.

8.3 Component type: TCPWM_PWM_PDL [v1.0]

8.3.1 Instance LidarMotorControl

Description: This component implements a PWM using the TCPWM hardware block
Instance type: TCPWM_PWM_PDL [v1.0]
Datasheet: online component datasheet for TCPWM_PWM_PDL

Table 15. Component Parameters for LidarMotorControl

Parameter Name	Value	Description
Clock Prescaler	Divide by 1	Divides down the input clock
Compare 0	0	Sets the compare value. When the count value equals the compare the compare output pulses high. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Count Input	Disabled	Determines if a count input is needed and how that input is registered
Enable Compare Swap	false	When selected the compare register is swapped between compare 0 and compare 1 on the next OV/UN after the swap is registered
Enable Period Swap	false	If checked the periods will be swapped at the next OV/UN when a swap event has been registered
Interrupt Source	None	Selects which events can trigger an interrupt
Invert PWM Output	false	If checked the main PWM output is inverted
Invert PWM_n Output	false	If checked the main PWM_n output is inverted
Kill Input	Disabled	Determines how the kill input behaves
Kill Mode	Stop on Kill	Determines what the kill signal does to the PWM

Parameter Name	Value	Description
Period 0	100	Sets the period of the counter. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
PWM Alignment	Left Aligned	Selects which direction the PWM counts in. Left = Up, Right = Down, Center/Asymmetric = Up/Down
PWM Mode	PWM	Selects the PWM mode of operation
PWM Resolution	16-bits	Selects the width of the PWM
Reload Input	Disabled	Determines if a reload input is needed and how the reload signal input is registered
Run Mode	Continuous	If Continuous is selected counter runs forever. If One Shot is selected counter runs for one period and stops
Start Input	Disabled	Determines if a start input is needed and how that input is registered
Swap Input	Disabled	This input controls when compare and period swaps occur
User Comments		Instance-specific comments.

8.3.2 Instance MotorSpeedControl

Description: This component implements a PWM using the TCPWM hardware block
Instance type: TCPWM_PWM_PDL [v1.0]
Datasheet: online component datasheet for TCPWM_PWM_PDL

Table 16. Component Parameters for MotorSpeedControl

Parameter Name	Value	Description
Clock Prescaler	Divide by 1	Divides down the input clock
Compare 0	0	Sets the compare value. When the count value equals the compare the compare output pulses high. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Count Input	Disabled	Determines if a count input is needed and how that input is registered
Enable Compare Swap	false	When selected the compare register is swapped between compare 0 and compare 1 on the next OV/UN after the swap is registered

Parameter Name	Value	Description
Enable Period Swap	false	If checked the periods will be swapped at the next OV/UN when a swap event has been registered
Interrupt Source	None	Selects which events can trigger an interrupt
Invert PWM Output	false	If checked the main PWM output is inverted
Invert PWM_n Output	false	If checked the main PWM_n output is inverted
Kill Input	Disabled	Determines how the kill input behaves
Kill Mode	Stop on Kill	Determines what the kill signal does to the PWM
Period 0	100	Sets the period of the counter. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
PWM Alignment	Left Aligned	Selects which direction the PWM counts in. Left = Up, Right = Down, Center/Asymmetric = Up/Down
PWM Mode	PWM	Selects the PWM mode of operation
PWM Resolution	16-bits	Selects the width of the PWM
Reload Input	Disabled	Determines if a reload input is needed and how the reload signal input is registered
Run Mode	Continuous	If Continuous is selected counter runs forever. If One Shot is selected counter runs for one period and stops
Start Input	Disabled	Determines if a start input is needed and how that input is registered
Swap Input	Disabled	This input controls when compare and period swaps occur
User Comments		Instance-specific comments.

8.3.3 Instance ServoControl

Description: This component implements a PWM using the TCPWM hardware block
Instance type: TCPWM_PWM_PDL [v1.0]
Datasheet: online component datasheet for TCPWM_PWM_PDL

Table 17. Component Parameters for ServoControl

Parameter Name	Value	Description
Clock Prescaler	Divide by 1	Divides down the input clock
Compare 0	0	Sets the compare value. When the count value equals the compare the compare output pulses high. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).

Parameter Name	Value	Description
Config Data in Flash	true	Controls whether the configuration structure is stored in flash (const, true) or SRAM (not const, false).
Count Input	Disabled	Determines if a count input is needed and how that input is registered
Enable Compare Swap	false	When selected the compare register is swapped between compare 0 and compare 1 on the next OV/UN after the swap is registered
Enable Period Swap	false	If checked the periods will be swapped at the next OV/UN when a swap event has been registered
Interrupt Source	None	Selects which events can trigger an interrupt
Invert PWM Output	false	If checked the main PWM output is inverted
Invert PWM_n Output	false	If checked the main PWM_n output is inverted
Kill Input	Disabled	Determines how the kill input behaves
Kill Mode	Stop on Kill	Determines what the kill signal does to the PWM
Period 0	100	Sets the period of the counter. Range: 0-65535 (for 16 bit resolution) or 0–4294967295 (for 32 bit resolution).
PWM Alignment	Left Aligned	Selects which direction the PWM counts in. Left = Up, Right = Down, Center/Asymmetric = Up/Down
PWM Mode	PWM	Selects the PWM mode of operation
PWM Resolution	16-bits	Selects the width of the PWM
Reload Input	Disabled	Determines if a reload input is needed and how the reload signal input is registered
Run Mode	Continuous	If Continuous is selected counter runs forever. If One Shot is selected counter runs for one period and stops
Start Input	Disabled	Determines if a start input is needed and how that input is registered
Swap Input	Disabled	This input controls when compare and period swaps occur
User Comments		Instance-specific comments.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
    - Software base types
    - Hardware register types
    - Compiler defines
    - Cypress API return codes
    - Interrupt types and macros
- Registers
    - The full PSoC 6 register map is covered in the PSoC 6 Registers Technical Reference Manual
    - Register Access chapter in the System Reference Guide
        - CY_GET API routines
        - CY_SET API routines
- System Functions chapter in the System Reference Guide
    - General API routines
    - CyDelay API routines
    - CyVd Voltage Detect API routines
- Power Management
    - Power Supply and Monitoring chapter in the PSoC 6 Technical Reference Manual
    - Low Power Modes chapter in the PSoC 6 Technical Reference Manual
    - Power Management chapter in the System Reference Guide
        - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
    - CyWdt API routines