

## 1.2 III WHAT IS A MICROPROCESSOR?

In the late 1960s, the CPU was designed with discrete logic gates. As semiconductor technology advanced, it was possible to fabricate more than thousand gates on a single silicon chip—this came to be known as *Large-scale integration*. As technology moved from Small-scale Integration to Large-scale Integration, it became possible to build a whole CPU with its related timing functions on a single chip. This came to be known as *Microprocessor*. A computer that is designed using a microprocessor as its CPU, is known as a Microcomputer.

Intel Corporation announced the first 4 bit microprocessor 4004 in 1971. The number of bits refer to the number of binary digits that the microprocessor can manipulate in one operation. Soon after this, Intel developed an 8 bit microprocessor 8080 in 1974. The 8085 microprocessor that followed 8080, had few more additional features compared to 8080 architecture. The instruction sets of 8080 and 8085 are practically the same. The 8085 microprocessor has an 8 bit data bus, so it can read data from or write data to memory or I/O ports only 8 bit at a time. It has a 16 bit address bus, so it can address any one of  $2^{16}$  or 65,536 memory locations. It operates with 3MHz clock signal. The limitations of 8085 microprocessor are

- It operates with low speed
- Less powerful addressing mode and instruction set
- Limited number of 8 bit general purpose registers
- Low memory (64 Kbytes) addressing capability

Because of these limitations, Intel Corporation announced the first 16 bit microprocessor 8086 in 1978. The 8086 microprocessor has 16 bit data bus and 20 bit address bus. It can read or write data to memory or I/O ports either 16 bit or 8 bit at a time and it can address any one of 1,048,576 ( $2^{20}$ ) memory locations. Subsequently, Intel developed 16 bit processors such as 8088, 80186, 80188 and 80286. The Intel 8088 has the same instruction set and arithmetic unit as the 8086. It has 8 bit data bus and 20 bit address bus and can read or write data to memory or I/O devices only 8 bit of data at a time. 80186 and 80188 are an improved version of 8086 and 8088 respectively. Both the processors have a few additional instruction sets compared to 8086 instruction set. 80286 is an improved version of 80186. It is designed to be used as CPU in multitasking computers. It operates in real and virtual addressing mode. Later, in 1985, Intel developed 32 bit microprocessor 80386. The 80386 can address directly up to 4 gigabytes of memory. Intel's second generation of 32 bit microprocessor 80486 was available in the year 1989. Intel introduced a third generation 80586 (Pentium processor) in 1998. Motorola, Zilog, etc. also developed 8 bit, 16 bit and 32 bit Microprocessors. Microprocessors have been widely used after their invention. However, the following limitations of the microprocessor led to the invention of the microcontroller.

- A microprocessor requires external memory to execute a program.
- A microprocessor cannot be directly interfaced with I/O devices. Peripheral chips are needed to interface I/O devices.

### SECTION REVIEW |||

1. The 8085 microprocessor has \_\_\_\_\_ bit data bus and \_\_\_\_\_ bit address bus.
2. List the limitations of the 8085 microprocessor.
3. The 8088 microprocessor has \_\_\_\_\_ bit data bus and \_\_\_\_\_ bit address bus.
4. The 80386 is a \_\_\_\_\_ bit microprocessor.
5. List the limitations of microprocessor.

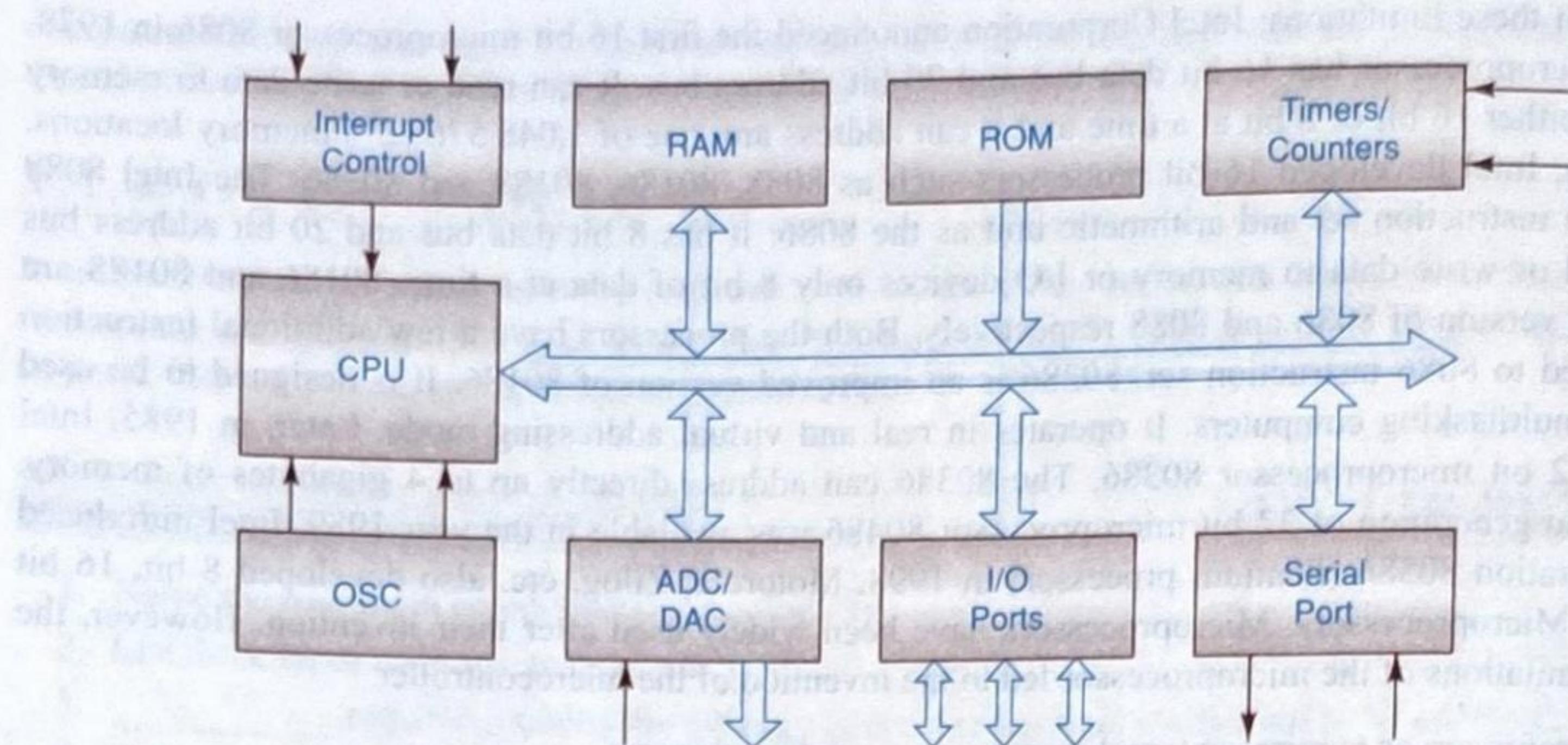
## 1.3 III WHAT IS A MICROCONTROLLER?

As technology moved from LSI to VLSI, it became possible to build the microprocessor, memory and I/O devices on a single chip. This came to be known as the 'Microcontroller.'

A microcontroller contains a microprocessor and also one or more of the following components.

- Memory
- Analog to Digital (A/D) converter
- Digital to Analog (D/A) converter
- Parallel I/O interface
- Serial I/O interface
- Timers and Counters

Figure 1.5 shows the block diagram of a typical microcontroller, which is a true computer on-chip. The first 4 bit microcontroller was developed by different companies like Hitachi, National, Toshiba, etc. Soon after this, 8 bit microcontrollers were developed by Intel, Motorola, Zilog, Philips, Microchip technology, etc.



**Figure 1.5** Block diagram of a typical microcontroller

### 1.3.1 APPLICATIONS OF MICROCONTROLLER

Microcontrollers have been widely used in home appliances such as refrigerators, washing machines and microwave ovens. It is used in displays, printers, keyboards, modems, charge card phones and also in automobile engines, etc. as controllers.

### 1.3.2 COMMERCIAL MICROCONTROLLER DEVICES

A brief overview of some commercial microcontrollers, PIC microcontrollers, Intel microcontrollers and Atmel microcontrollers is given in this section. Microcontrollers must be selected depending on the needs of a given application. Table 1.1 lists the various microcontrollers with important features like on-chip memory, number of timers, DMA, A/D converter and UART.

**TABLE 1.1** *Microcontrollers with important features*

Device	Register Memory On-chip (bytes)	On-chip program memory ROM/EPROM	Speed MHz	No. of timers/ Counters	No. of I/O lines	On-chip Peripherals
8031 (MCS51-family)	128	ROM less	12	2	32	UART
8051 (MCS51-family)	128	4K ROM	12	2	32	UART
8052 (MCS51-family)	256	8K ROM	12	3	32	UART

(Contd)



# THE 8051 MICROCONTROLLER

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## Learning Objectives

After you have completed this chapter, you should be able to

- Explain the features of the 8051 microcontroller
- Explain the architecture of the 8051 microcontroller
- Explain the pin diagram of the 8051 microcontroller
- Explain the memory organisation of the 8051 microcontroller
- Define the stack and explain its uses
- Explain the additional features of the 8052 microcontroller

### 2.1 III FEATURES OF 8051

A microcomputer is a computer implemented on a very large scale integration chip. The 8051 is the first microcontroller of the MCS-51 family, introduced by Intel Corporation at the end of the 1980s. The 8051 family with its many enhanced members enjoys the largest market share, estimated to be about 40%, among the various microcontroller architectures. The architecture and pin diagram of the 8051 are presented in this chapter. The block diagram of the 8051 microcontroller is as shown in Fig. 2.1.

The salient features of the 8051 microcontroller are given below:

- 8 bit CPU
- On-chip clock oscillator
- 4 Kbytes of on-chip program memory
- 256 bytes of on-chip data random access memory

- 64 Kbytes of program memory address space
- 64 Kbytes of data memory address space
- 32 bidirectional I/O lines can be either used as four 8 bit ports or 32 individually addressable I/O lines
- Two 16 bit timers/counters
- 16 bit address bus multiplexed with port 0 and port 2 and 8 bit data bus multiplexed with port 0
- Full duplex asynchronous receiver transmitter
- Five-vector interrupt structure with two priority levels

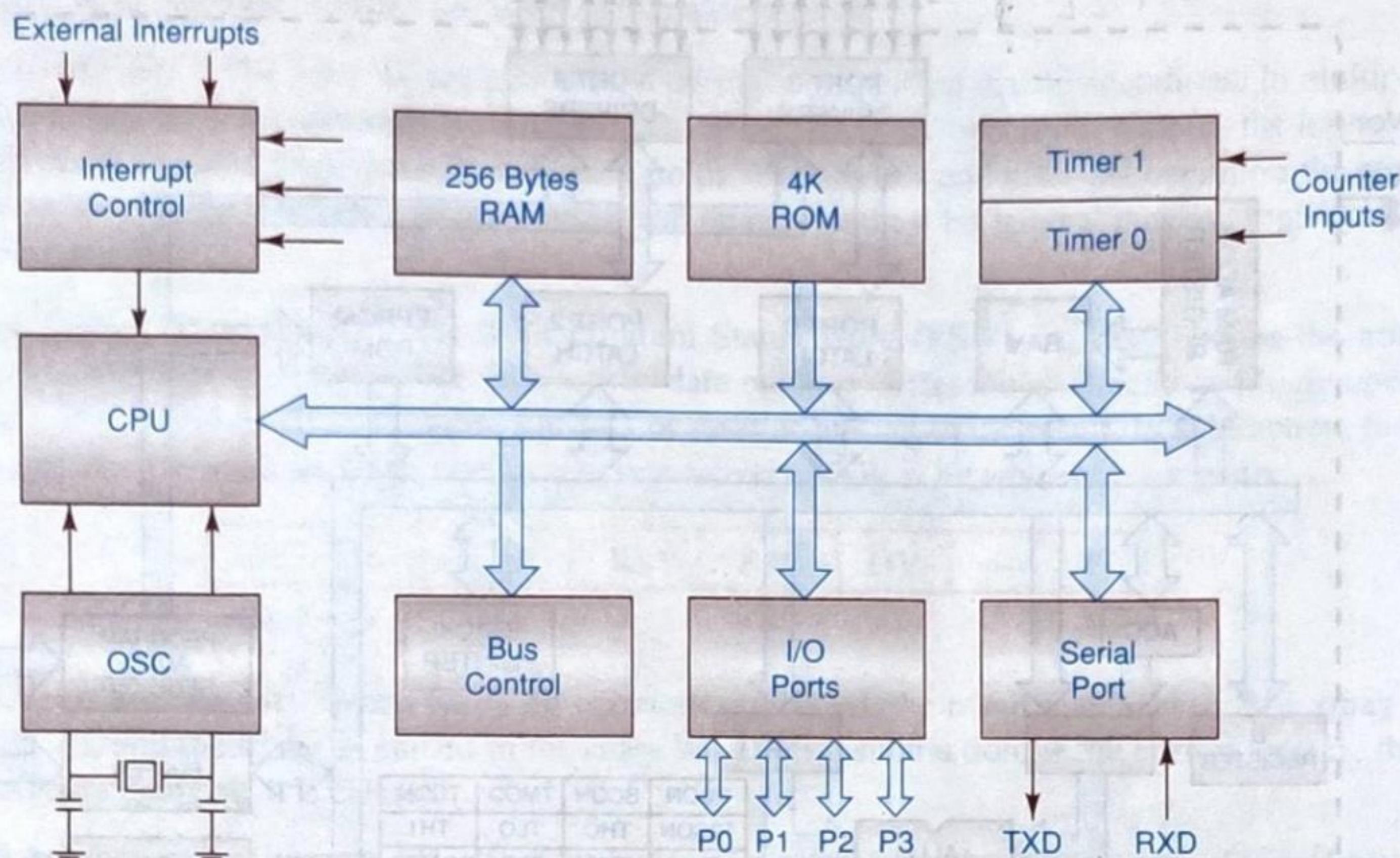


Figure 2.1 Block diagram of 8051 Microcontroller

## 2.2 III ARCHITECTURE OF 8051

Figure 2.2 shows a functional block of the internal operations of an 8051 microcontroller. The 8051 includes an 8 bit CPU, memory, four 8 bit I/O ports, two timers/counters and a Universal Asynchronous Receiver Transmitter (UART).

### 2.2.1 PROCESSOR

The processor includes arithmetic and logic unit, instruction decoder and timing generation unit, Accumulator (A or Acc), B register and status register.

**Arithmetic and Logic Unit** The Arithmetic and Logic Unit (ALU) performs the computing functions. The accumulator is an 8 bit register. In arithmetic and logical operations, one of the operands is in 'A' register. After the arithmetic/logical operations, are performed, the result is stored in 'A' register and this affects various flags namely Carry (C), Auxiliary Carry (AC), Overflow (O), and Parity (P) of status register.

**Instruction Decoder and Control** The instruction decoder and control are parts of the timing and control unit. When an instruction is fetched from program memory, it is loaded in the instruction register. The decoder decodes the instruction and establishes the sequence of events to follow. The instruction register is not programmable and cannot be accessed through any instruction. The timing generation and control unit synchronises all the microcontroller operations with the clock and generates control signals necessary for communication between the processor and peripherals.

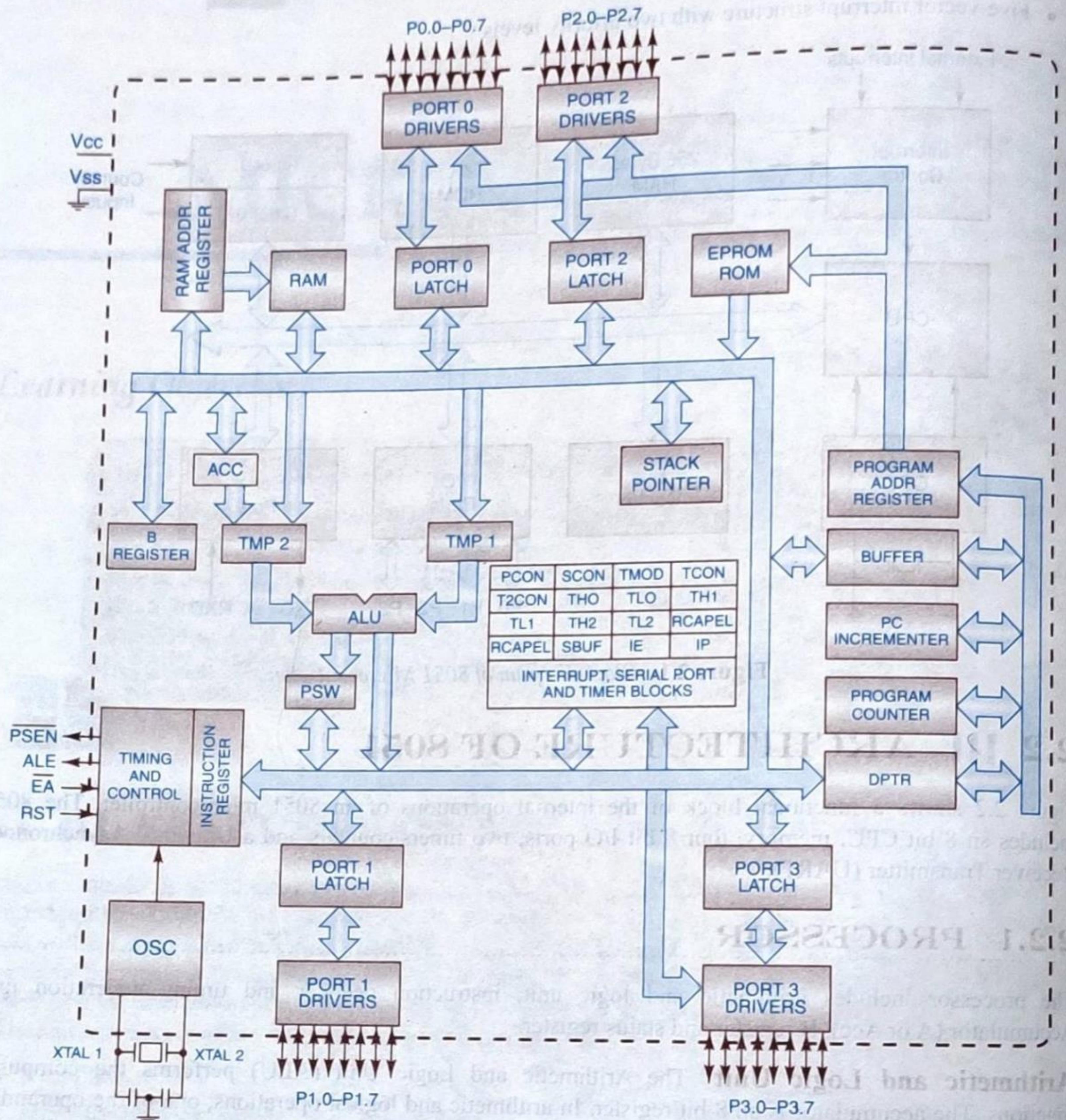


Figure 2.2 Functional block diagram of 8051 (Courtesy Intel)

## CPU Registers

**'A' Register (E0H)** Similar to any Intel microprocessor, the 8051 has an 8 bit A and in the instruction, it is referred as 'A'. The accumulator is used in all arithmetic and logical operations and has direct connection to ALU. One of the operands is stored in the accumulator. After the operation is performed, the result is stored in the A. In multiplication operation, one of the 8 bit operands is stored in 'A' register. After the operation, it stores the lower byte of the result in 'A' register. In division operation, it holds an 8 bit dividend and after the operation, the quotient is stored in the accumulator. It is also used in indexed addressing mode to access information from program memory. 'A' is bit addressable register.

**'B' Register (F0H)** The 8 bit 'B' register is used during multiply and divide operations. In multiplication operation, one of the 8 bit operands is stored in 'B' register. After the operation, it stores the higher byte of the result in 'B' register. In division operation, it holds 8 bit divisor and after the operation the remainder is stored in 'B' register. For other instructions, it can be used as an 8 bit general purpose register. 'B' is bit addressable register.

**Program Status Word (D0H)** The 8 bit Program Status Word (PSW) register contains the arithmetic status of the ALU and the bank selects bits for the data memory. After the arithmetic and logic operations, the C, AC, P, and O flags of PSW register are set or reset according to the result. In subtraction, the C and AC bits operate as borrow and digit borrow flag respectively. PSW is bit addressable register

CY	AC	F0	RS1	RS0	OV	---	P
Bit 7				Bit 0			

**Bit 7: Carry/borrow bit** When two 8 bit operands are added, the result may exceed 8 bit (may exceed 255 or FF H), and the 9<sup>th</sup> bit is copied in the carry bit. During subtraction, if the borrow occurs, the carry bits is set and otherwise, it is cleared.

**Bit 6: Auxiliary carry/borrow bit** This bit indicates a carry from the lower nibble (lower 4 bit) during 8 bit addition. If auxiliary carry flag is set, it means there is a carry from 3<sup>rd</sup> to 4<sup>th</sup> bit position. In subtraction, if there is a borrow from 4<sup>th</sup> bit to 3<sup>rd</sup> bit position, then AC is set, else it is cleared.

**Bit 5: F0** Flag 0 is available to the user for general purpose.

**Bit 4-3: RS1:RS0** Register Bank Select bits

11 = Selects register bank 3

10 = Selects register bank 2

01 = Selects register bank 1

00 = Selects register bank 0

Each bank contains eight 8 bit registers

**Bit 2: OV** OV flag is used to detect errors in signed arithmetic operations. When two signed numbers are added, if the result exceeds the destination, overflow flag is set, else it is reset. OV is set, if there is a carry from D6 to D7, but no carry from D7, or if there is a carry from D7 but no carry from D6 to D7.

**Bit 1: Undefined flag**

**Bit 0: Parity flag** P flag is set, if the result contains an even number of 1 bit, else it is reset, if the result contains an odd number of 1 bit.

**Stack Pointer (81 H)** Stack Pointer is an 8 bit register. It contains the address of the data item on the top of the stack. It is incremented before the data is stored. While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialised to 07H after a reset. The operation and instruction associated with the stack will be discussed in detail in Chapter 3.

**Data Pointer (DPH-83 H and DPL-82 H)** The Data Pointer (DPTR) consists of two 8 bit registers—a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16 bit address. It is used to furnish address information for internal and external program memory and for external data memory.

**Program Counter** Program Counter (PC) is a 16 bit register. The 16 bit program counter specifies the address of the next instruction to be executed. After reset, the PC will be set to 0000H and the CPU will start executing the first instruction stored at program memory location 0000H. The 8051 fetches the instruction one byte at a time and after fetching, it increments the PC by 1.

## 2.2.2 MEMORY

The 8051 devices have 4 Kbytes on-chip program memory and 256 bytes of on-chip data random access memory. The program memory is used to hold the start up program that will be executed when the 8051 is powered up. The 8051's on-chip data random access memory is organised as follows:

First 128 bytes:	00H to 1FH	Register Banks
	20H to 2FH	Bit Addressable RAM
	30H to 7FH	General Purpose Registers
Next 128 bytes:	80H to FFH	Special Function Registers

The 256 bytes of internal memory are organised as shown in Fig. 2.3. Data memory is divided into two groups of memory size 128 bytes each. In the first 128 bytes, the user data can be stored in register banks, bit addressable RAM and in general purpose registers. The next 128 bytes are special function registers.

**Register Banks (00H to 1FH)** The lowest 32 bytes are grouped into four banks of eight registers. RS1 and RS0 of (bit 4-3) program status word select the bank. Each bank contains 8 general purpose registers R0–R7 (R0, R1, R2, R3, R4, R5, R6, and R7). These registers are similar to the general-purpose registers of the microprocessor. These registers are used in instructions such as:

ADD A, R2; adds the value contained in R2 to the accumulator

If RS1 = 0 and RS0 = 0, Bank 0 is selected, and then R2 is the memory location 02H of the Internal RAM. The following instruction has the same effect as the above instruction.

ADD A, 02H

**Bit Addressable RAM (20H to 2FH)** The 8051 supports a special feature which allows access to bit variables. The bit addressable area of the RAM is just 16 bytes of internal RAM located between 20H and 2FH. This is where individual memory

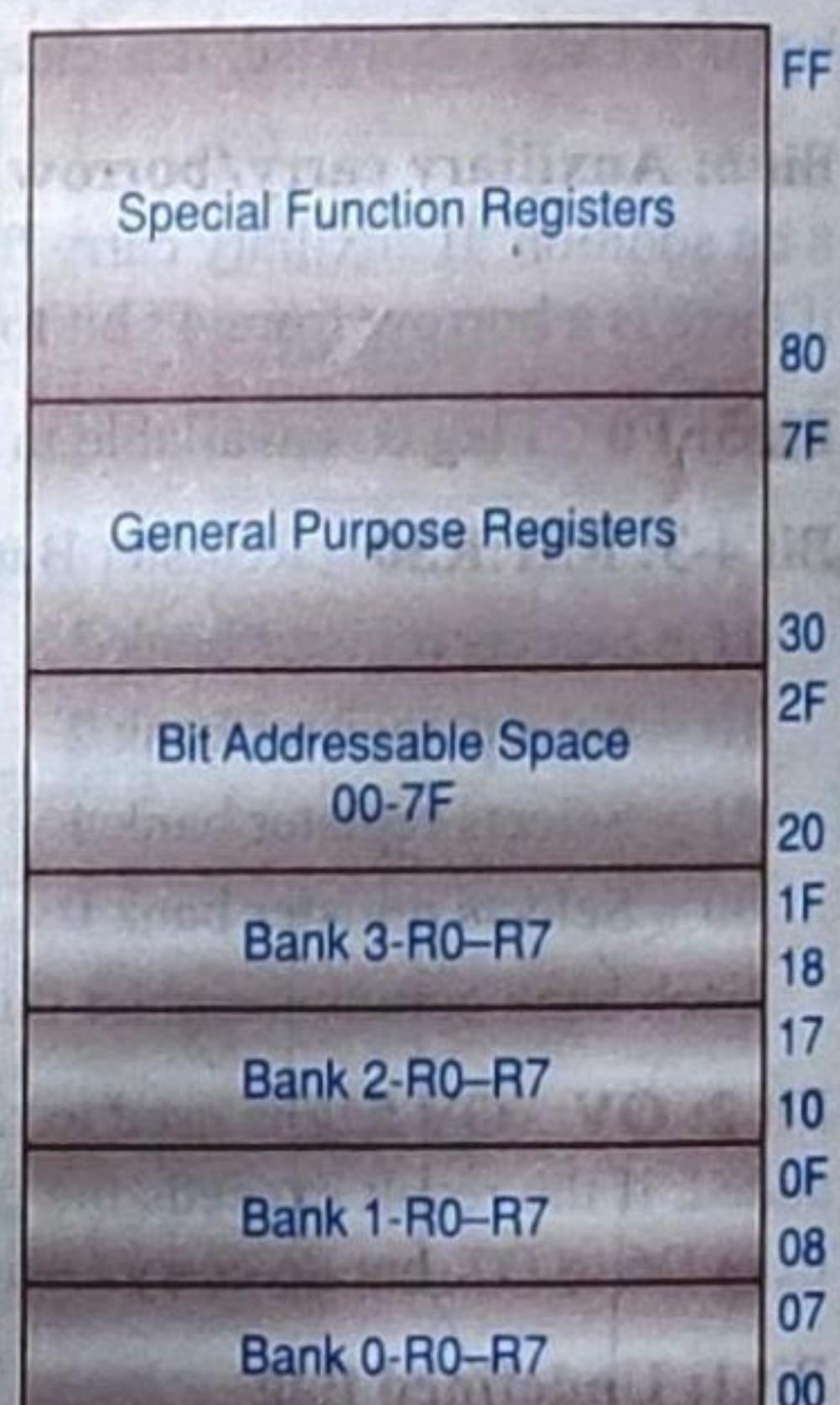


Figure 2.3 Internal RAM organisation

bits in internal RAM can be set or cleared. In total, there are 128 bits; addressed 00H to 7FH. Bit variables can have a value of 0 or 1.

A bit variable can be set with a command such as SETB and cleared with a command such as CLR. Example instructions are:

SETB 25H	; sets the bit 25H (becomes 1)
CLR 25H	; clears the bit 25H (becomes 0)

### Note

1. Bit 25H is actually bit 5 of internal RAM location 24H.
2. Bit addressing can also be performed on some of the SFR registers, which will be discussed later on.

**TABLE 2.1** Bit address of internal RAM

Byte Address	Bit Address	Byte Address	Bit Address
	7-0		7 - 0
2F	7F-78	27	3F-38
2E	77-70	26	37-30
2D	6F-68	25	2F-28
2C	67-60	24	27-20
2B	5F-58	23	1F-18
2A	57-50	22	17-10
29	4F-48	21	0F-08
28	47-40	20	07-00

**General Purpose RAM (30H to 7FH)** These 80 bytes of internal RAM memory are available for general-purpose data storage. Access to this area of memory is fast as compared to access to the main memory, and instructions with single byte operands use this area for storage. However, the system stack uses these 80 bytes and in practice, little space is left for general storage. The general purpose RAM can be accessed using direct or indirect addressing modes.

**SFR Register** The SFR registers are located within the internal memory in the address range 80H to FFH, as shown in Fig. 2.3. Not all locations within this range are defined. Each SFR has a very specific function. They have an address (within the range 80H to FFH) and a name, which reflects the purpose of the SFR. Although 128 bytes of the SFR address space is defined, yet only 21 SFR registers are defined in the standard 8051. Undefined SFR addresses should not be accessed, as this might lead to some unpredictable

results. Note that some of the SFR registers are bit addressable. SFRs are accessed just like normal internal RAM locations. CPU and internal peripheral modules use special function registers for controlling the desired operation of the device. The special function registers contain input and output ports, control register for interrupts, timers, serial ports, etc. as shown in Table 2.2.

### 2.2.3 DIGITAL I/O PORT AND PERIPHERALS

It contains four 8 bit parallel ports, named as port 0, port 1, port 2, and port 3. Ports are used to send or receive the data. Each bit of the port can be configured as an input or an output and also port 0 is used as low order address and data pins (AD0–AD7), Port 2 is used as high order address pins (A8–A15) and port 3 is used by timers, serial port, external interrupt and for sending control signals (RD, WR) to external data memory. It contains two versatile timers—timer 0 and timer 1. Both are 16 bit timers/counters and each timer consists of two 8 bit registers. It supports serial data transmission using universal asynchronous receiver transmitter.

**TABLE 2.2** *Special function registers (Courtesy Intel)*

Symbol	Name	Address
*ACC	Accumulator	E0H
*B	B Register	F0H
*PSW	Program Status Word	D0H
SP	Stack Pointer	81H
DPTR	Data Pointer 2 Bytes	
DPL	Low Byte	82H
DPH	High Byte	83H
*P0	Port 0	80H
*P1	Port 1	90H
*P2	Port 2	A0H
*P3	Port 3	B0H
*IP	Interrupt Priority Control	B8H
*IE	Interrupt Enable Control	A8H
TMOD	Timer/Counter Mode Control	89H
*TCON	Timer/Counter Control	88H
TH0	Timer/Counter 0 High Byte	8CH
TL0	Timer/Counter 0 Low Byte	8AH
TH1	Timer/Counter 1 High Byte	8BH
TL1	Timer/Counter 1 Low Byte	8DH
*SCON	Serial Control	98H
SBUF	Serial Data Buffer	99H
PCON	Power Control	87H

\*bit addressable

**SECTION REVIEW**

1. The 8051 has 64 Kbyte of program memory address space.
2. The 8051 has 5 number of vector interrupts with 2 priority levels.
3. In division operation, an 8 bit divisor is stored in B register.
4. In division operation, A register is used to store quotient.
5. OV flag detects errors in signed arithmetic operations.
6. AC flag is set, if there is a borrow from fourth bit to third bit.
7. Stack pointer is a 8 bit register.
8. Stack pointer is initialised to 07H after reset.
9. Bit 1 of program status word is undefined flag.
10. PC 16 bit register contains the address of program and external data memory.
11. 20H location to 2FH location is bit addressable space in internal RAM.
12. The 8051 contains 4 number of register banks and each register bank contains 8 number of 8 bit registers.
13. List bit addressable registers in the 8051 microcontroller.
14. Name any five byte-addressable registers.
15. RD and WR control signals are used to interface external data memory.
16. In the 8051, maximum power dissipation rating is 1W.

**2.3 PIN DIAGRAM OF 8051**

The 8051 microcontroller is a 40 pin DIP as shown in Fig. 2.4. The crystal frequency is the basic clock frequency of the microcontroller. The 8051 requires a +5V single power supply and is designed for 1 MHz minimum clock frequency to 16 MHz maximum clock frequency. A brief discussion of these pins is given in this section.

**Vcc (Pin no 40)** Vcc pin is connected to +5 V power supply with rated current 125 mA. In 8051, maximum power dissipation rating is 1 W.

**Vss (Pin no 20)** Vss pin is connected to Ground reference.

**XTAL2 (Pin no 18)** The output of the crystal oscillator circuit is connected as shown in Fig. 2.5. 30 pF disc capacitors are recommended when 12 MHz quartz crystals is used. In case of external clock, clock is connected to XTAL2.

**XTAL1 (Pin no 19)** The input of the crystal oscillator circuit is connected to XTAL1. In case of external clock, this pin is connected to ground.

1	P1.0	V	40
2	P1.1	Vcc	39
3	P1.2	P0.0	38
4	P1.3	P0.1	37
5	P1.4	P0.2	36
6	P1.5	P0.3	35
7	P1.6	P0.4	34
8	P1.7	P0.5	33
9	RST	P0.6	32
10	P3.0/RXD	P0.7	31
11	P3.1/TXD	EA	30
12	P3.2/INT0	ALE	29
13	P3.3/INT1	PSEN	28
14	P3.4/T0	P2.7/A15	27
15	P3.5/T1	P2.6/A14	26
16	P3.6/WR	P2.5/A13	25
17	P3.7/RD	P2.4/A12	24
18	XTAL2	P2.3/A11	23
19	XTAL1/CLKIN	P2.2/A10	22
20	Vss	P2.1/A9	21

Figure 2.4 Pin diagram of 8051

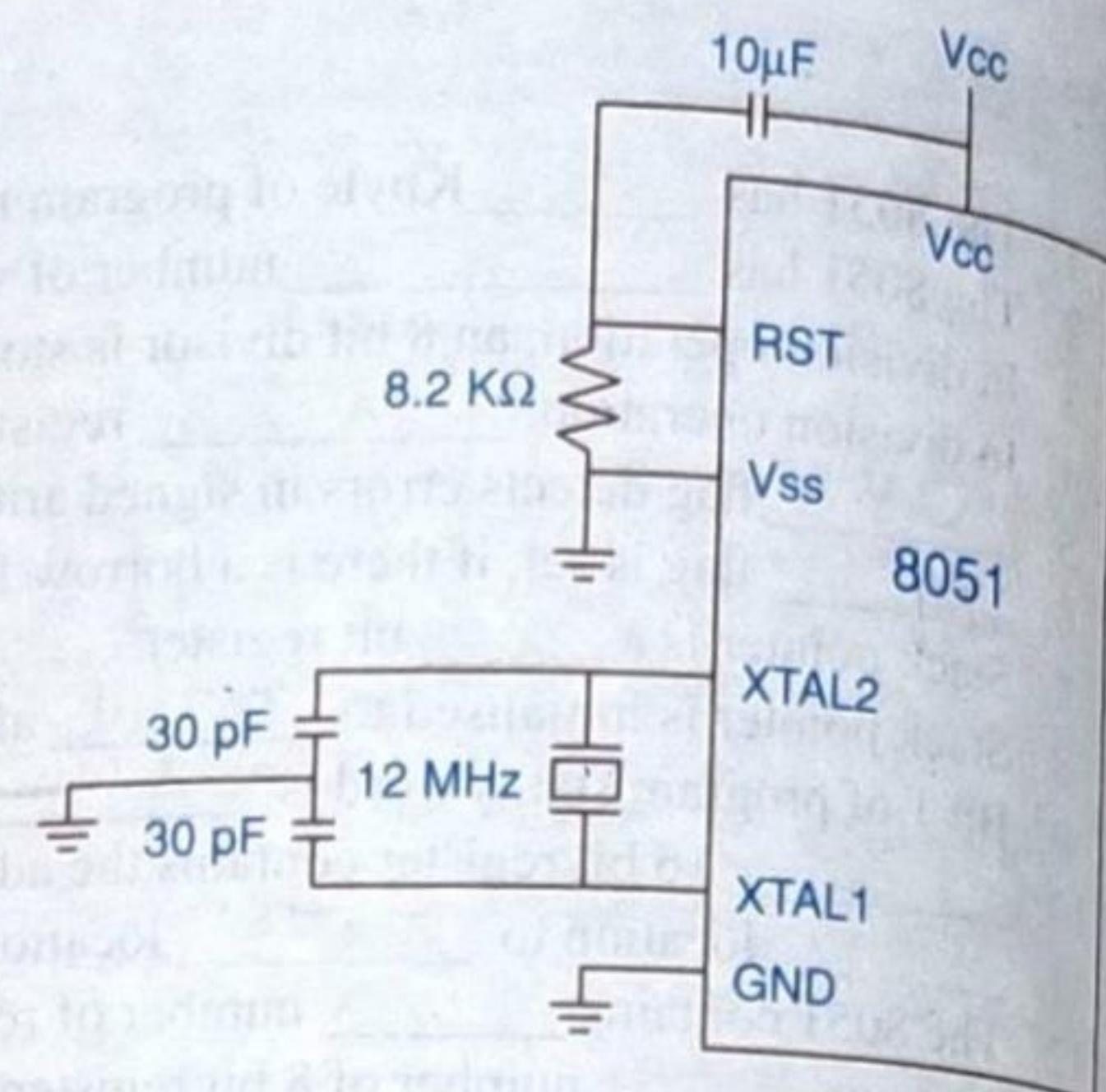
*RST (Pin no 9) If active high*

**RST (Pin no 9)** The microcontroller provides a reset mechanism to establish initial conditions. The special function registers and few CPU registers must be initialised before the microcontroller can operate properly.

Reset circuit is as shown in Fig. 2.5. For resetting 8051, RST pin is made high for two machine cycles (24 oscillator periods). Table 2.3 lists the SFRs and their reset values.

**Port 0 (Pins 32-39)** Port 0 serves as true bi-directional I/O port, and also as low order address and data bus for external memory.

**Port 1 (Pins 1-8)** Port 1 has no dual functions. It serves as quasi bi-directional 8 bit I/O port.



**Figure 2.5** 8051 connected to 12 MHz crystal and reset circuit

**TABLE 2.3 Reset values of the SFRs**

SFR	Reset Value
PC	0000H
ACC	00H
B	00H
PSW	00H
SP	07H
P0-P3	FFH
TMOD	00H
TCON	00H
TH0	00H
TL0	00H
TH1	00H
TL1	00H
SCON	00H
IP	xxx00000B
IE	0xx00000B
PCON	0xxxxxxxB

x-unknown

**Port 2 (Pins 21-28)** Port 2 is also an 8 bit quasi bi-directional I/O port. The alternate use of port 2 is to serve as high order address bus for external memory.

**Port 3 (Pins 10-17)** Port 3 is also an 8 bit quasi bi-directional I/O port. The alternate functions of port 3 are related to external interrupts, serial ports, timers and read/write control signals for external data memory. Table 2.4 lists the alternate functions of port 3.

**ALE (Pin 30)** *for demultiplexing* Address latch enable pin is used to demultiplex AD0-AD7 of port 0. This is a positive going pulse generated every time during external memory access. This signal is used primarily to latch low order address from the multiplexed bus and generate a separate set of eight address lines A0-A7 as shown in Fig. 2.6. *for demultiplexing* *to read off chip ROM content*

**PSEN (Pin 29)** Program strobe signal is the output control signal. It remains low while fetching external program memory. During the internal program execution, the condition of this pin is high.

**EA (Pin 31)** If external access (EA) pin is held high, it selects internal program memory

$\overline{EA} = 1 \rightarrow$  Store prog  
on chip from  
 $\overline{EA} = 0 \rightarrow$  store externally

for address 0000H to 0FFFH. Beyond this address (1000H to FFFFH), it selects external program memory as shown in Fig. 2.8(a). Else if this pin is held low, it selects only external program memory for address 0000H to FFFFH.

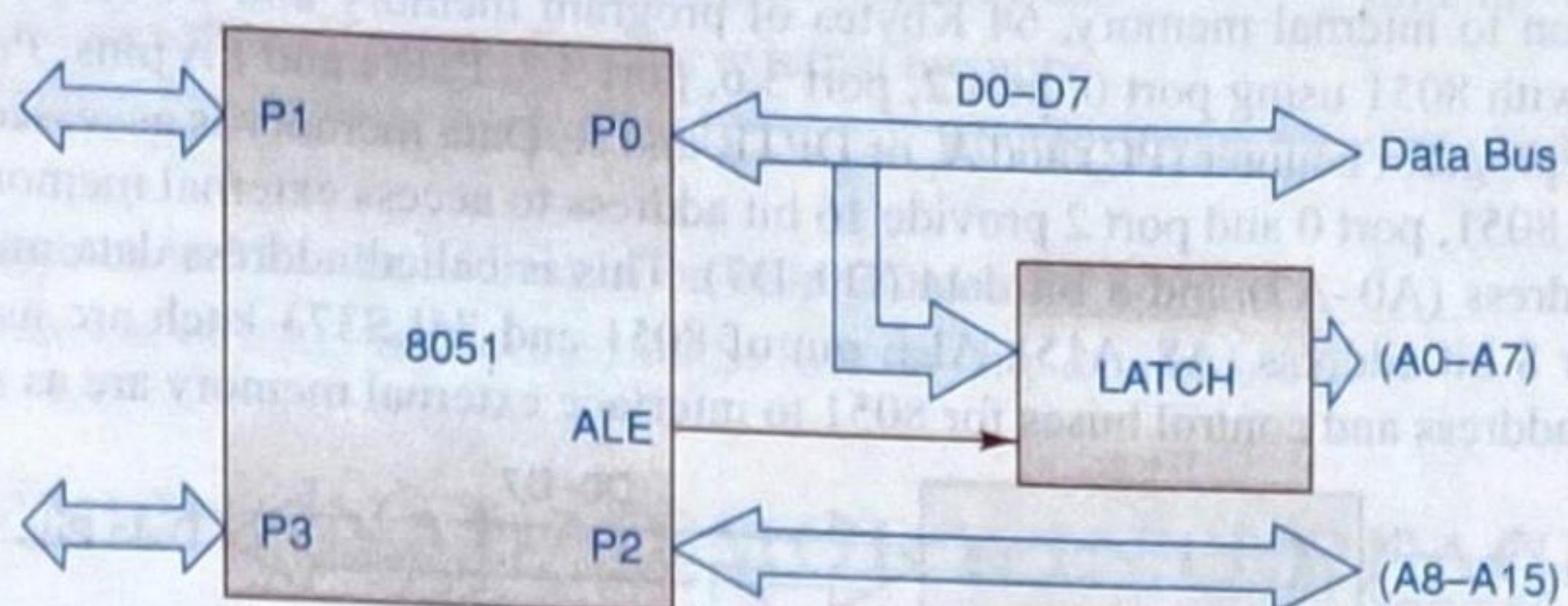


Figure 2.6 Data and address multiplexing using ALE

TABLE 2.4

Alternate functions of port 3

P3.0	Pin 10	RXD (serial input port)
P3.1	Pin 11	TXD (serial output port)
P3.2	Pin 12	$\overline{\text{INTO}}$ (external interrupt 0)
P3.3	Pin 13	$\overline{\text{INTI}}$ (external interrupt 1)
P3.4	Pin 14	T0 (timer/counter 0 external input)
P3.5	Pin 15	T1 (timer/counter 1 external input)
P3.6	Pin 16	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	Pin 17	$\overline{\text{RD}}$ (external data memory read strobe)

### SECTION REVIEW |||

30 pF

- In an oscillator circuit, 10 nF disc capacitor is recommended when 12 MHz crystal is used.
- After reset, the value of P0-P3 will be FFH.
- Port 1 port has no dual functions.
- Port 3 port contains control signals for external data memory.
- ALE (pin 30) pin is used to demultiplex AD0-AD7.
- 0000H to 0FFFH is the address of internal program memory.
- The 8051 contains 2 external interrupts.
- Port 3 port serves as low order address bus and Port 2 port serves as high order address bus for external memory.
- For resetting 8051, RST pin is made high for 24 oscillator periods.  
(2 machine cycles)

## 2.4 III MEMORY ORGANISATION

The 8051 devices have 4 Kbytes of on-chip program memory and 256 bytes of on-chip data random access memory. In addition to internal memory, 64 Kbytes of program memory and 64 Kbytes of data memory can be interfaced with 8051 using port 0, port 2, port 3.6, port 3.7, PSEN and EA pins. Program memory is accessed using the program counter (PC) and A, or DPTR and A. Data memory is accessed using DPTR, R0 and R1 register. In 8051, port 0 and port 2 provide 16 bit address to access external memory. Port 0 provides the lower 8 bit address (A0–A7) and 8 bit data (D0–D7). This is called address/data multiplexing. Port 2 provides the upper 8 bit address (A8–A15). ALE pin of 8051 and 74LS373 latch are used to demultiplex AD0–AD7. Data, address and control buses for 8051 to interface external memory are as shown in Fig. 2.7.

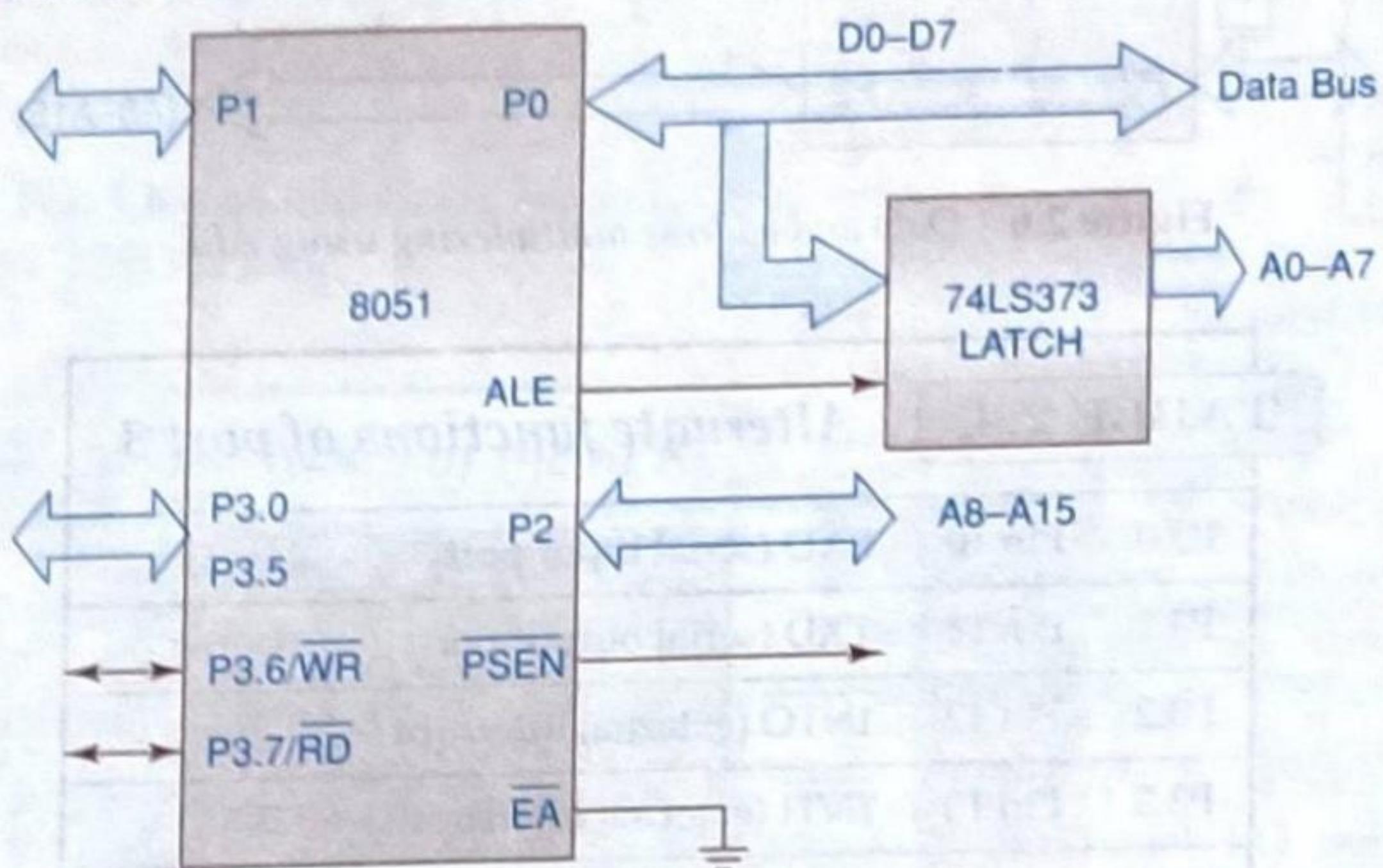


Figure 2.7 Data bus, address bus and control signals of 8051

When EA is connected to the ground, 8051 fetches instructions from external ROM by using PSEN. Then, the address of external ROM is 0000H to FFFFH. When EA is connected to Vcc, then it fetches instructions from on-chip ROM 4 Kbytes. The address of on-chip ROM is 0000 to 0FFFH. For address 1000H to FFFFH, it fetches instructions from external ROM. In this mode, 60 Kbytes of external ROM can be interfaced with 8051 microcontroller as shown in Fig. 2.8(a). The data can be stored both in internal and 64 Kbytes of external data memory as shown in Fig. 2.8(b).

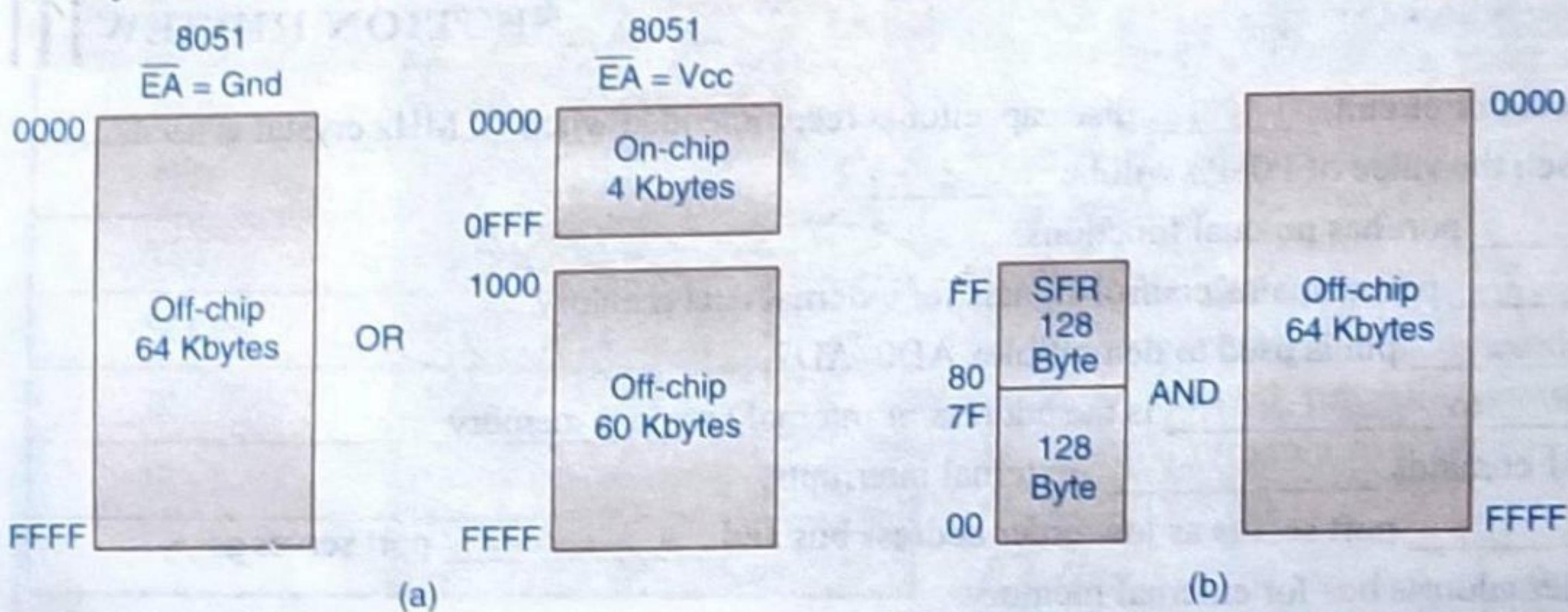


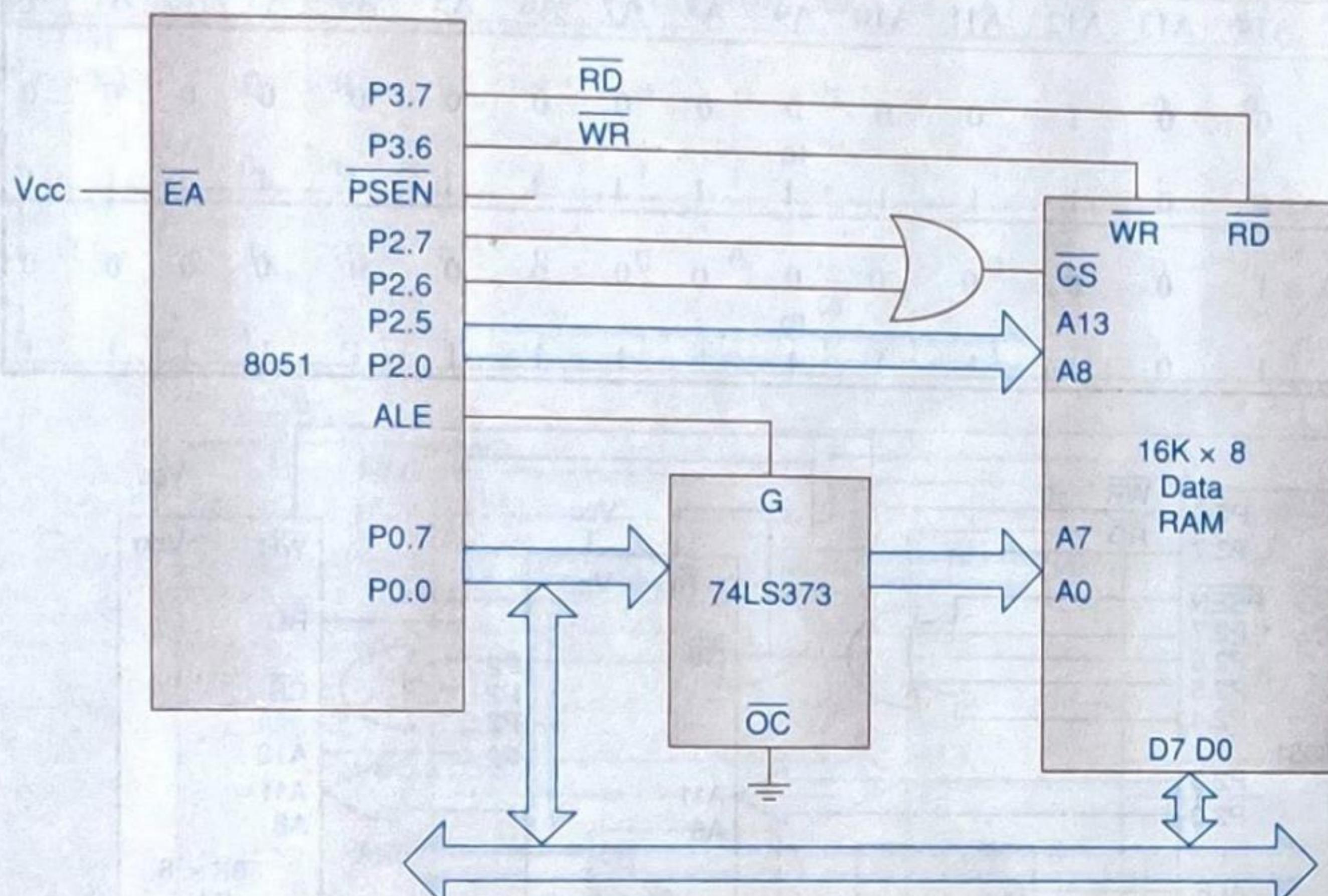
Figure 2.8(a) On-chip and off-chip program Rom, (b) On-chip and off-chip data memory

**SECTION REVIEW**

1. The 8051 device has \_\_\_\_\_ on-chip program memory and \_\_\_\_\_ on-chip data memory.
2. List the control signals used to interface the external memory.
3. \_\_\_\_\_ Kbytes of program memory and \_\_\_\_\_ Kbytes of data memory can be interfaced to 8051.
4. If  $\overline{EA}$  is connected to Vcc, the address of on-chip ROM is \_\_\_\_\_ to \_\_\_\_\_.
5. \_\_\_\_\_ number of bytes is allocated for SFR in on-chip data memory.

## **2.5 III EXTERNAL MEMORY INTERFACING**

The 8051 devices have only 256 bytes of on-chip data random access memory. In applications where large amount of data random access memory is required, the external data random access memory is interfaced with 8051. Address, data,  $\overline{RD}$  (P3.7) and  $\overline{WR}$  (P3.6) pins are used to interface data RAM. P3.7 and P3.6 are connected to  $\overline{RD}$  and  $\overline{WR}$  pins of data RAM as shown in Fig. 2.9.



**Figure 2.9 Connection to external data RAM**

The memory chip requires 14 address lines (A13–A0) to decode  $16384 \times 8$  registers. The remaining address lines—A15 and A14 pin—are connected through OR gate to  $\overline{CS}$  pin of external data RAM. When the address lines A15 and A14 are low, then external data RAM is selected. The address of external data RAM is 0000H to 3FFFH. Since  $\overline{EA}$  is connected to Vcc, internal program memory is selected for address 0000H to 0FFFH.

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