X

S. No.	Name of the Experiment		Date of Experiment	Remarks
1	Emp-1> Intro do lab	1-2	4/02/25	
2	Enp-2> V-I relation in Diode	3-5	11/2/25	
3	Exp-3> Amplipien Circuit using OPAMP 741	6-8	18/2/25	
4	Exp-4> LOGIC GATES	9-10	22/2/25	
5	Exp-5> Implementation using NAND gate	11-12	26/2/25	

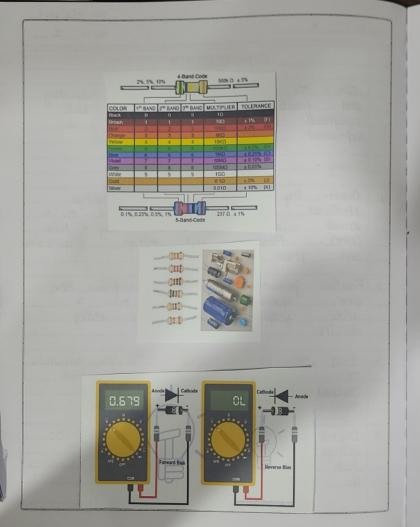


Dual Power Supply



Measuring voltage, resistance, or Measuring high current low current (less than 200mA) (up to 10A)

L	Expt. No
[Expourment - 1
	oim - To introduce the electronics lateratory and familiarize students with traic equipments and components used in experiment.
_	Theory -
1.	Cathode Ray Oscilloscope (CRO): Displays electrical signals as waveforms on a screen using a cathode - ray - tube (CRT). Measures peak valtage, prequence and phase differences.
	Function generator: Generater wareforms like sine, square & triangle over a wide frequency range for testing circuits.
5.	Dual DC power dupply: Provider adjustable DC voltage & current (max 2A) with Constant accurent / voltage mades & overload protection.
1	Digital Multimeter (DMM): Measures AC/DC voltage, currents, nesistance and itests diades / continuity. Displays reading on ACD.
	Teacher's Signature



T.	No 1	Page No. 2
Expt.	No.	rage No
5.	Resistors: - Resist amount slow, in ohm (-1). Values are by colou codes. Capacitors: - Stores energy in field $J_0 _W$ 2 plates dependent dielectric	measured
6.	Copacitors:- Stores energy in Jield John 2 plates Asperot dislectric	a electric
	Diodes: - Allow current in Jeans to block in Jeverse to	
8.	Trapsistors:- Three terminal devi that amplify on switch curr a small base current.	ices ents wing
	Teacher's Signature	

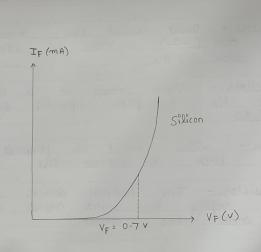


Fig-1> Formard Dias of

Expt. No. 2

Page No. 5

Result

Supply Voltage	Vp	ID	Va	
0.7 V	0589 V			
1.6 V	0.555 V			
1.5 V	0.585V			
1.6 V	0.592 V			
2.0 V	0.665V			
2.5 V	0.621 V			
3.0 V	0.632V			
3.5 V	6.640V			

Precautions:

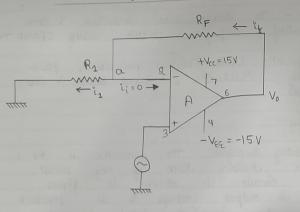
0	Connections	should	be	done	Carchilla
O	Readings	shall	be	moted	carebully
0	Proper	connection	,		
	,				

Teacher's Signature _

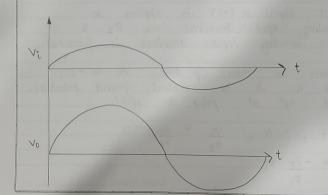
	Date 13/2/25
Exp	r. No &
	Experiment - 3
	voim - To design an inverting & non inverting amperieu circuit using OPAMP 741.
	Equipment - CRO, Function generation, power upply, Multimeter, Bread Board & CRO probes.
	Theory
->	Inverting Emplijien: The invertex is the basic building block of any circuit. The circuit is shown in figure. Vo is output voltage & in feedback to the inverting input terminal through RF & R1 metwork.
	Input signal vi (ac) is applied to inverting input terminal via R1 & mon inverting input terminal is Grounded.
	Assume an Ideal Op Amp. Ds vs = 0; mode a is at visitual Ground potential. Nodal eg ⁿ at point a yields.
	$V_0 = -R_E V_0^2$
	R°

Expt. No.

Non-inverting Amplifier



Apput & Output Waveforms



2>	Non - inverting somplifier: - When ac is applied and circuit provides input signal without inverting it, such a arcuit is called mon - inverting amplifier
	and circuit provides input signal without
	inventing it, such a circuit is called
	mon - inverting amplifier.
	us yeur, voltage at mode of is vi, same as in put voltage applied to
	is sero, voltage at mode of its vi
	same as input voltage applied to
	mon-inverting input terminal. RF & R1
	yours a potential divider.
	The state of the s
	1 = 1, Vi = Vo-vi, Vi + Vi = Vo
	R ₁ R _F R ₁ R _F R _F

Yo =	11+	RF (, V _c
	L	Ra	

Observations

(i)	Inve	edina	Samplifie	المال			
S.no	Resistors		Input		output	Grain	
	RL	RF	Voltage	Freq	Valtage		
1.	1ke	10KA	10 mV	IKH2	100 mV	-16	
2.	150		20 mV	1KH2	-200 mV	-10	
3.	1KI	loka	30 mV	1KH Z	-300 mV	-10	
4.	1KD	IOKS	40 my	1KHZ	-400 mV	-10	
5.	1KA	10 KA	50 mV	1KH2	-500 mV	-10	
6.	1KA	1042	60 m V	IKHZ	-600 mV	-10	
7.	1KA	10150	70 mV	1542	-700 my	-10	
				0			

Page No. 8

(ii)	Non-	Invoting	Amplifier
			•

S.mo	no Resistors		s Anput		Output		Gain
	RL	RF	Voltage	Forequency	Vo	Itage	
1	1 KD	10KV	10 mV		110	mV	+11
2	IKR	IOKS	20 mV		220	mV	tu
3	152	loks	30 mV		330	mν	tii
4	IKA	1012	40 mV		440	mV	til
5	IKS	1042	50 mV		550	mV	+()
6	IKD	IOKS	60 mV		660	mV	t11
7	IKI	1015-52	76 mv		770	m٧	+11

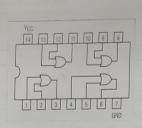
Calculations & Result:

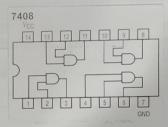
Precautions -

- All Connections should be done carefully Avoid excessive input signals Ensure proper polarity

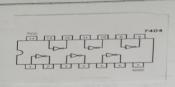
Conclu	Lion- Tr	ne or	berûmen	t succ	ess bull	y demo	ensterate	١
	pundi					eating		
mon	inverting	am	blikier	using		OPAME		
		1	0	0		,,,,		

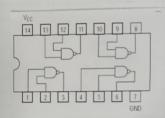
Teacher's Signature ____

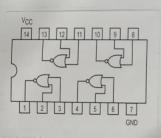




		Date 22/2/25
xpt. No4		Page No9
	Experiment -	4
Aim - To very gates (OR, justing their	AND, NOT.	th tables of logic, NAND, NOR, XOR),
Apparatus - NAND). Br. Power supply,	Logic Gater I eadboard, Cor Push Butto	Cs (eg:- 7400 for meeting Wires,
Procedure &	Table :-	
OR GATE - T	South Table	
Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1
AND GATE -	Touth Table	
doput		Output
A	В	У
0	0	0
0	1	0
1	0	0

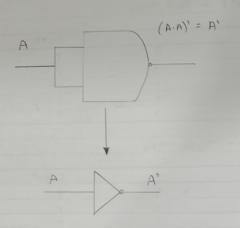






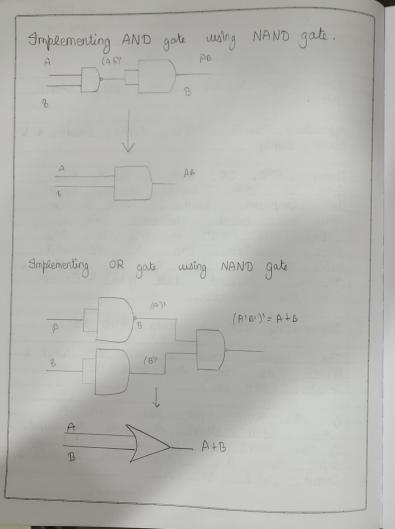
t. No4		Page No	
NAND GATE	- Truth Table		
Input		OUTPUT	
A	В	y	
0	0	1	
0		1	
1	0		
1	1	0	
	1	Cathar	
NOR Gate - To	ieuth Table		
	1	Catput	
1 A	ieuth Table	Catput	
Anput A	ieuth Table	Catput	

Input		Output
A	В	Y
0	0	0
0	1	1
1	0	1
1	1	0



Simplementing NOT gate using NAND gate

	Date 26 2 25
Expt. No.	5 Page No
	Eaperiment - 5
Aim:- Gate	Design & implementation using NAND
Power	atus:- Connecting Wixes, Glates, Bradboard & Supply
Gates Gates Using Theore	i- AND, OR, NOT is called tasic as their logical operation correct simplified further. NAND & NOR are called universal Gates as g only NAND are only Nak, any function can be uniplemented. NAND are NOR Gates & De Morgan's ems, different tasic Gates & Ex-ae are scalized
The	Higure shows 2 ways un which a gate can be used as an
the 2>0 un but	All NAND input tins connect to input signal A gives an output ne NAND input kin in connected to signal A, while others to logic 1. (Nill be A'. Teacher's Signature



Expt. N	No 5 Page No 12
11)	Implementing AND gate using NAND gate
1	An AND gate can be supplaced by a NAND gates as shown in figure.
	Implementing OR gate using NAND gate
	An OR gate con be supplaced by NAND Gates as shown in figure.
	Result: Using the procedures mentioned before, we can use NAND gate.
	Teacher's Signature