MANIPAL UNIVERSITY
JAIPUR
(University under Section 2(f) of the UGC Act)

FIRST STATE PRIVATE UNIVERSITY IN RAJASTHAN
A+ NAAC
3.28 SCORE

B.TECH FIRST YEAR

ACADEMIC YEAR: 2023-2024

COURSE NAME: EES

COURSE : ELECTRICAL AND ELECTRONICS SYSTEMS

LECTURE SERIES NO : 01 (ONE)

CREDITS : 4

MODE OF DELIVERY :

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PROPOSED DATE OF DELIVERY:

MANIPAL UNIVERSITY
JAIPUR

VISION
Global Leadership in Higher Education and Human Development

MISSION
- Be the most preferred University for innovative and interdisciplinary learning
- Foster academic, research and professional excellence in all domains
- Transform young minds into competent professionals with good human values

VALUES
Integrity, Transparency, Quality,
Team Work, Execution with Passion, Humane Touch

BIPOLAR JUNCTION TRANSISTORS

- The transistor is a three-layer semiconductor device consisting of either two n- and one p- type layers of material or two p- and one n- type layers of material.
- The former is called an npn transistor, while the latter is called a pnp transistor
- So, there are two types of BJT-

  i) pnp transistor ii) npn transistor

BIPOLAR JUNCTION TRANSISTORS

In each transistor following points to be noted-

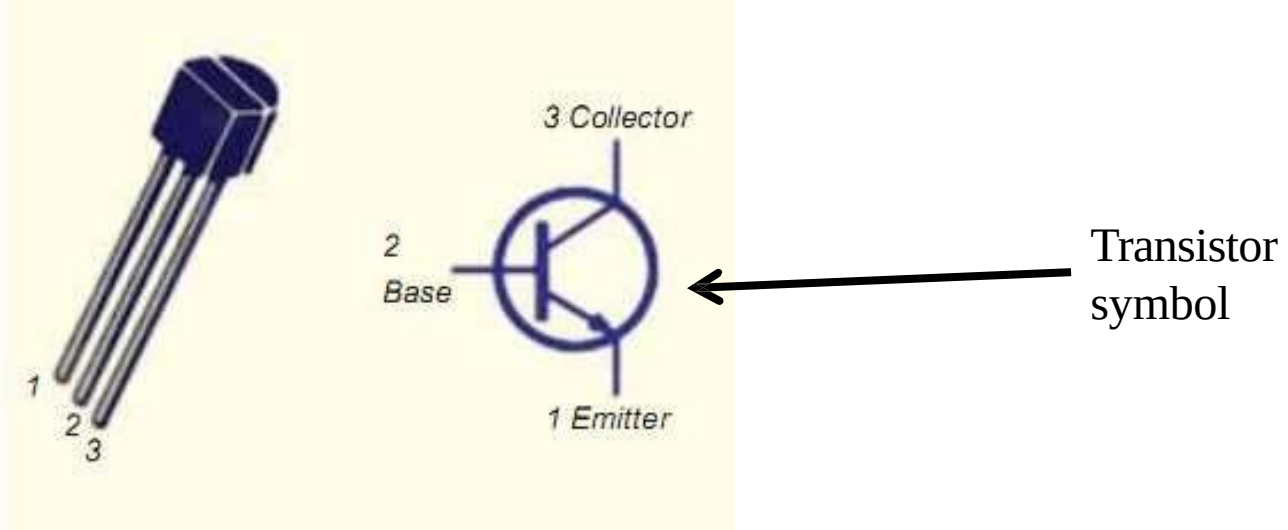
i) There are two junction, so transistor can be considered as two diode connected back to back.

ii) There are three terminals.

iii) The middle section is thin than other.

NAMING OF TRANSISTOR TERMINALS

- Transistor has three section of doped semiconductor.
- The section one side is called “emitter” and the opposite side is called “collector”.
- The middle section is called “base”.



NAMING OF TRANSISTOR TERMINALS

1) *Emitter:*
   - The section of one side that supplies carriers is called emitter.
   - Emitter is always forward biased wr to base so it can supply carrier.
   - For “npn transistor” emitter supply holes to its junction.
   - For “pnp transistor” emitter supply electrons to its junction.

NAMING OF TRANSISTOR TERMINALS

2) Collector:

- The section on the other side that collects carrier is called collector.
- The collector is always reversed biased wr to base.
- For “npn transistor” collector receives holes to its junction.
- For “pnp transistor” collector receives electrons to its junction.

NAMING OF TRANSISTOR TERMINALS

3) Base:

- The middle section which forms two pn junction between emitter and collector is called Base.

SOME IMPORTANT FACTORS TO BE REMEMBERED-

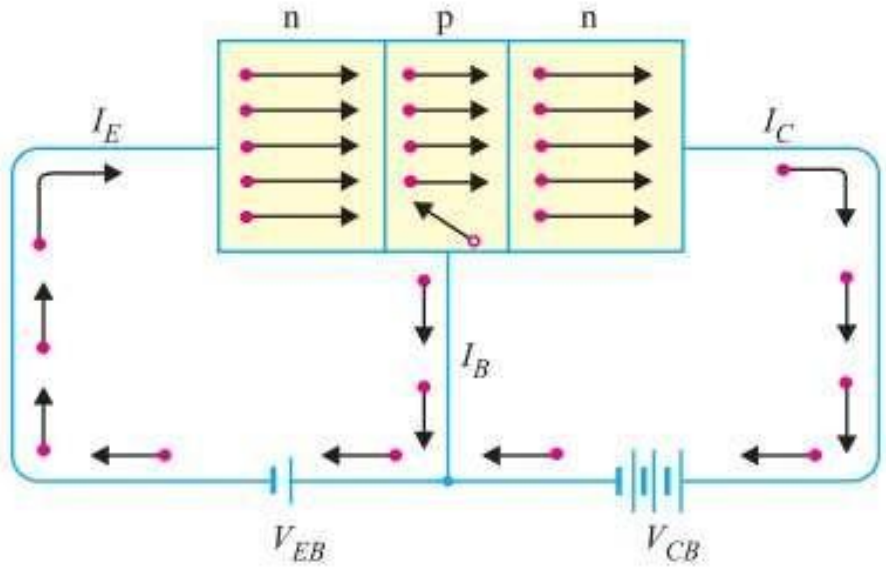
- The transistor has three region named emitter, base and collector.
- The Base is much thinner than other region.
- Emitter is heavily doped so it can inject large amount of carriers into the base.
- Base is lightly doped so it can pass most of the carrier to the collector.
- Collector is moderately doped.

SOME IMPORTANT FACTORS TO BE REMEMBERED-

- The junction between emitter and base is called emitter-base junction(emitter diode) and junction between base and collector is called collector-base junction(collector diode).
- The emitter diode is always forward biased and collector diode is reverse biased.
- The resistance of emitter diode is very small (forward) and resistance of collector diode is high (reverse).

TRANSISTOR OPERATION

1) Working of npn transistor:



✓Forward bias Is applied to emitter-base junction and reverse bias is applied to collector-base junction.

✓The forward bias in the emitter-base junction causes electrons to move toward base. This constitute emitter current, I_E.

TRANSISTOR OPERATION

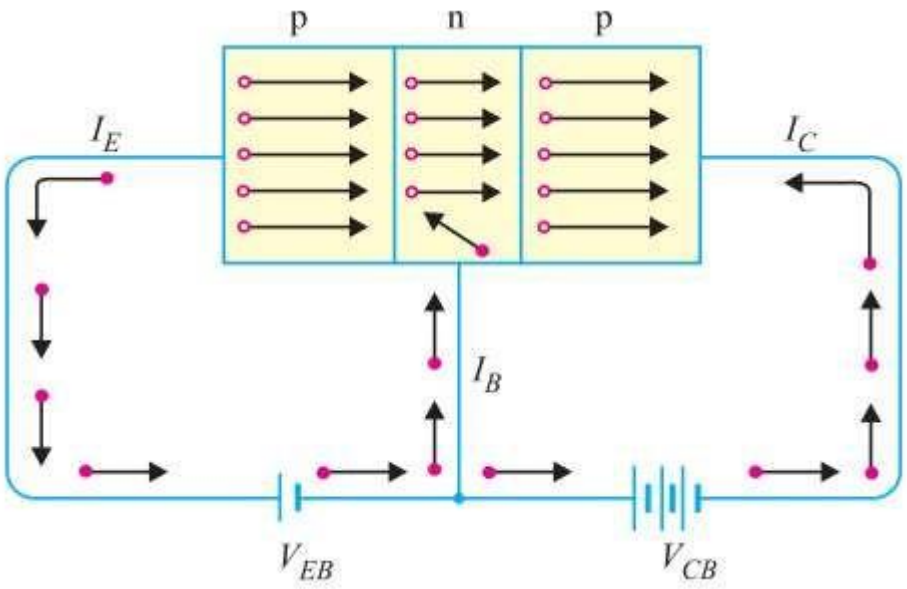
1) Working of npn transistor:

- ✓ As this electrons flow toward p-type base, they try to recombine with holes. As base is lightly doped only few electrons recombine with holes within the base.
- ✓ These recombined electrons constitute small base current.
- ✓ The remainder electrons crosses base and constitute collector current.

$$I_E = I_B + I_C$$

TRANSISTOR OPERATION

2) Working of pnp transistor:



✓Forward bias is applied to emitter-base junction and reverse bias is applied to collector-base junction.

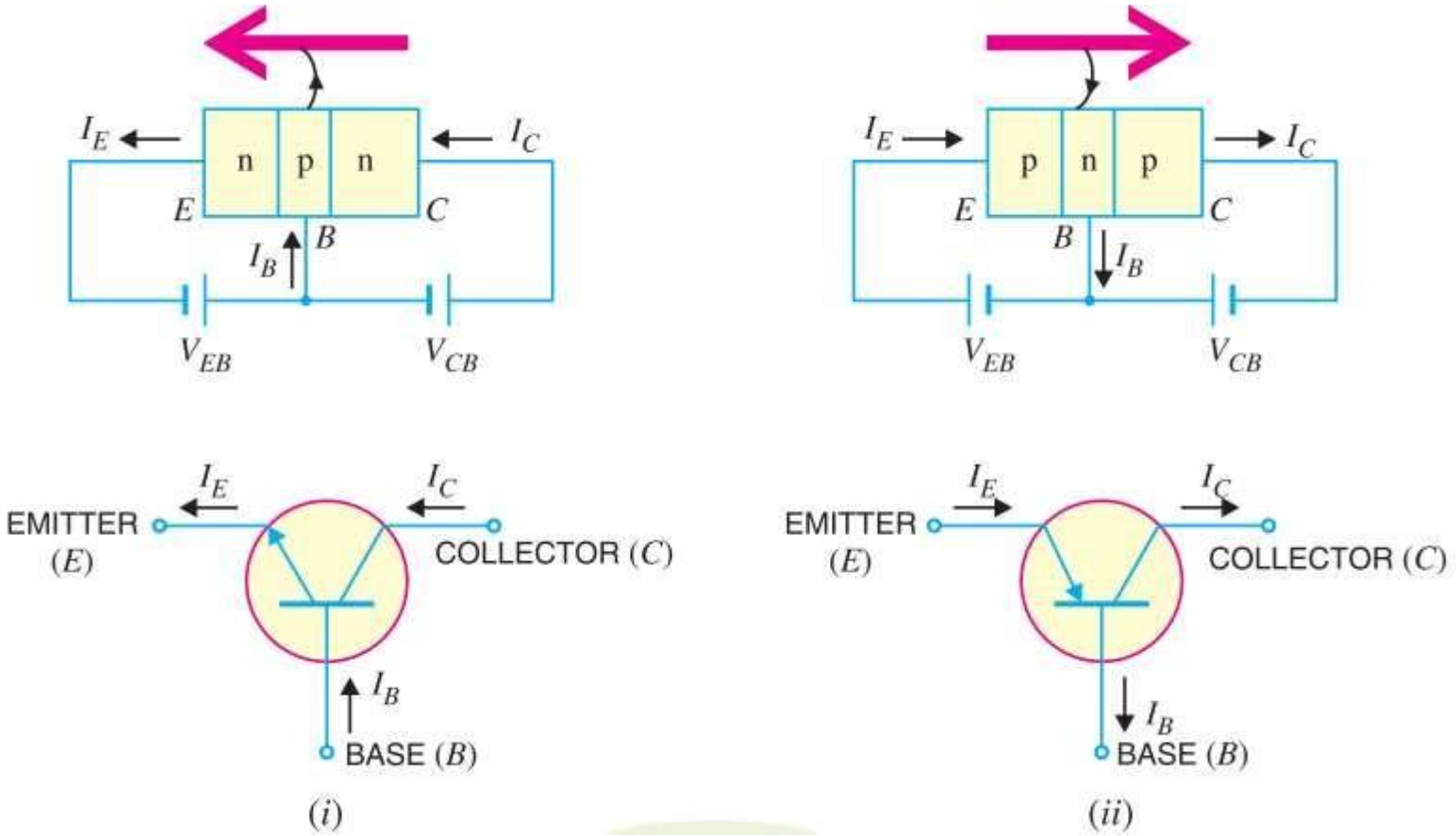
✓The forward bias in the emitter-base junction causes holes to move toward base. This constitute emitter current, I_E

TRANSISTOR OPERATION

2) Working of pnp transistor:

- ✓ As this holes flow toward n-type base, they try to recombine with electrons. As base is lightly doped only few holes recombine with electrons within the base.
- ✓ These recombined holes constitute small base current.
- ✓ The remainder holes crosses base and constitute collector current.

TRANSISTOR SYMBOL



TRANSISTOR OPERATING MODES

- Active Mode
  - Base- Emitter junction is forward and Base- Collector junction is reverse biased.
- Saturation Mode
  - Base- Emitter junction is forward and Base- Collector junction is forward biased.
- Cut-off Mode
  - Both junctions are reverse biased.

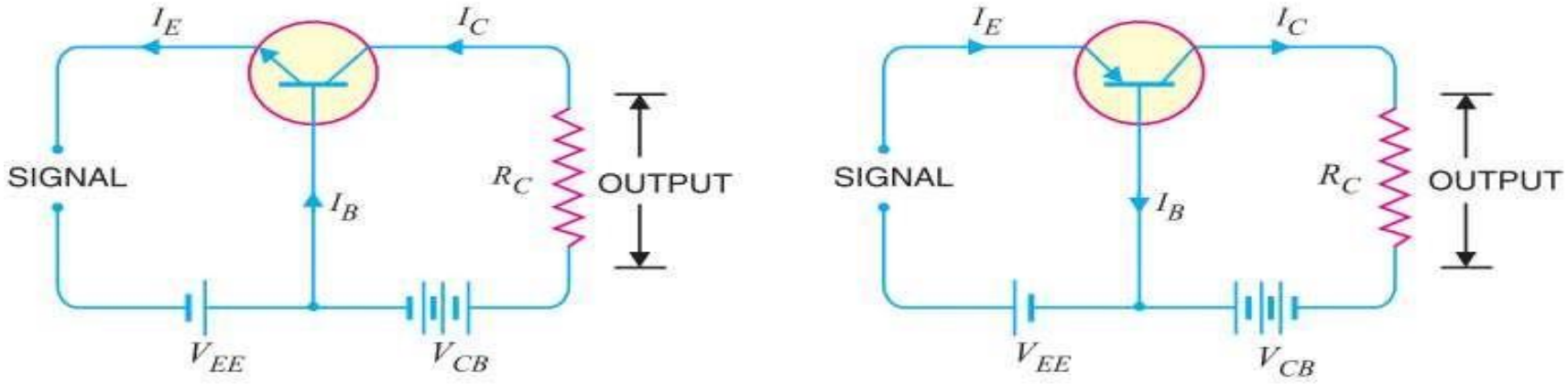
TRANSISTOR CONNECTION

- Transistor can be connected in a circuit in following three ways-

1) Common Base
2) Common Emitter
3) Common Collector

COMMON BASE CONNECTION

- The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration.



- First Figure shows common base npn configuration and second figure shows common base pnp configuration.

COMMON BASE CONNECTION

- Current amplification factor (α) :

  The ratio of change in collector current to the change in emitter current at constant V_{CB} is known as current amplification factor, α.

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \; at \text{ constant} V_{CB}$$

→ Practical value of α is less than unity, but in the range of 0.9 to 0.99

EXPRESSION FOR COLLECTOR CURRENT

→Total emitter current does not reach the collector terminal, because a small portion of it constitute base current. So,

$$I_E = I_C + I_B$$

→Also, collector diode is reverse biased, so very few minority carrier passes the collector-base junction which actually constitute leakage current,I_{CBO} .

→ So, collector current constitute of portion of emitter current αI_E and leakage current I_{CBO} .

$$I_C = \alpha I_E + I_{CB0}$$

EXPRESSION FOR COLLECTOR CURRENT

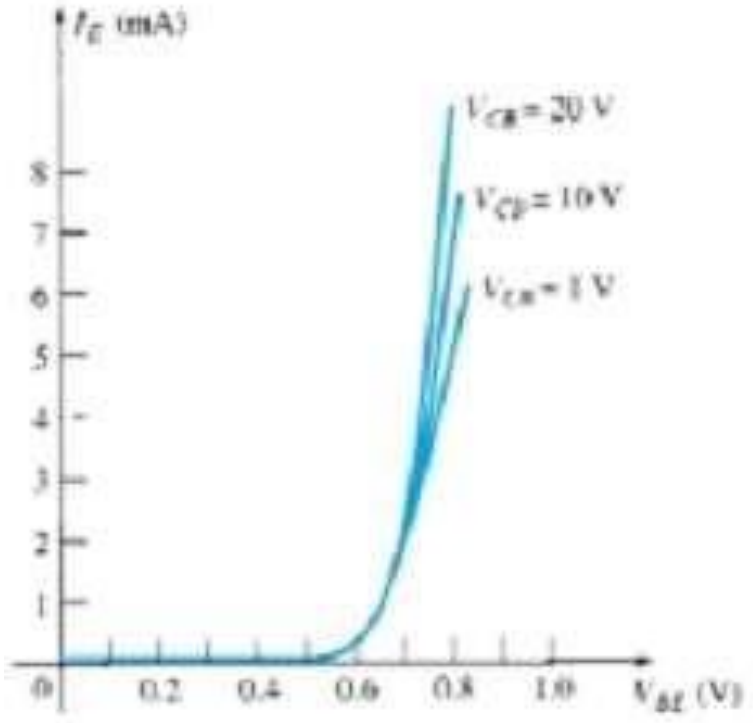
$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{I_{CBO}}{1 - \alpha}$$

CHARACTERISTICS OF COMMON BASE CONFIGURATION

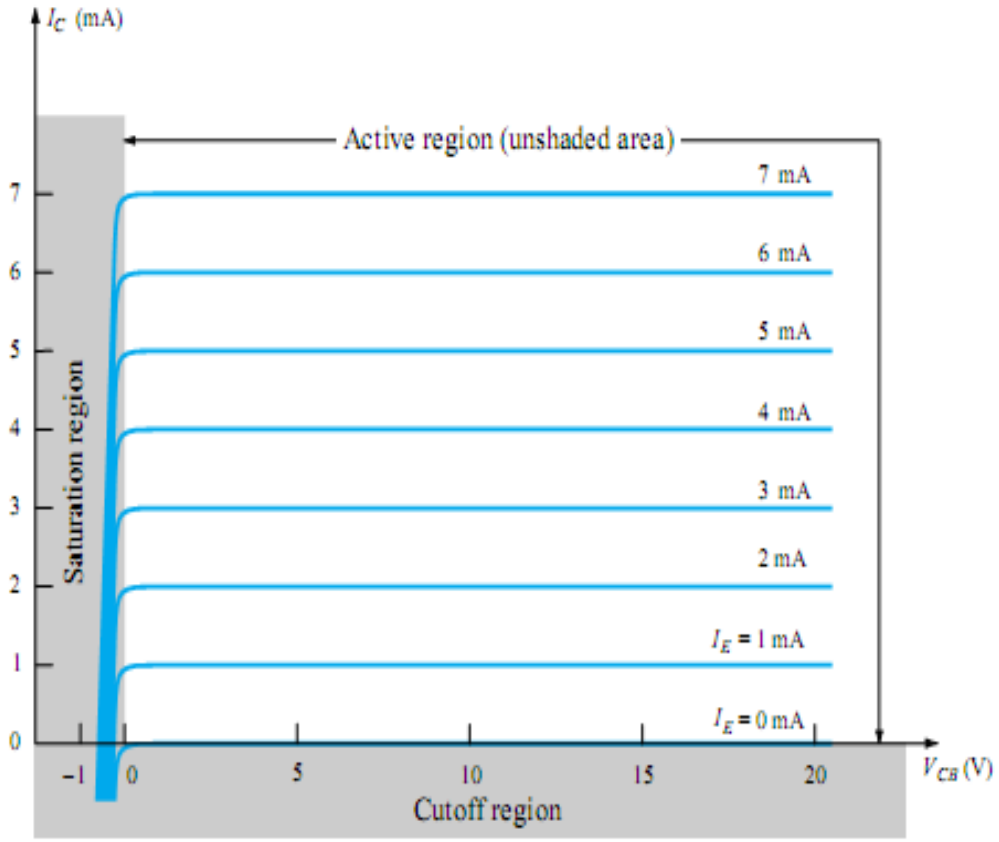
- Input Characteristics:



- V_{BE} vs I_E characteristics is called input characteristics.
- I_E increases rapidly with V_{BE}. It means input resistance is very small.
- I_E almost independent of V_{CB}.

CHARACTERISTICS OF COMMON BASE CONFIGURATION

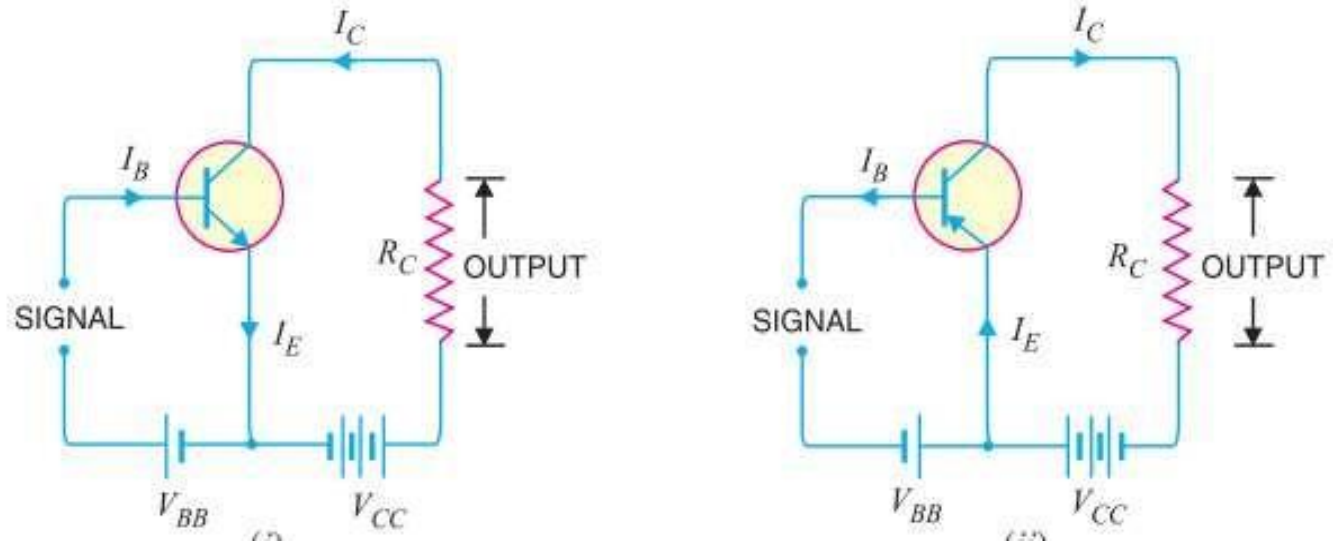
Output Characteristics:



- V_{Bc} vs I_c characteristics is called output characteristics.
- I_C varies linearly with V_{Bc} ,only when V_{Bc} is very small.
- As, V_{Bc} increases, I_C becomes constant.

COMMON EMITTER CONNECTION

- The common-emitter terminology is derived from the fact that the emitter is common to both the input and output sides of the configuration.



- First Figure shows common emitter npn configuration and second figure shows common emitter pnp configuration.

COMMON EMITTER CONNECTION

- Base Current amplification factor (β) :
- In common emitter connection input current is base current and output current is collector current.
- The ratio of change in collector current to the change in base current is known as base current amplification factor, β.

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

- Normally only 5% of emitter current flows to base, so amplification factor is greater than 20. Usually this range varies from 20 to 500.

RELATION BETWEEN β AND α

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$I_E = I_B + I_C$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C}$$

$$\beta = \frac{\Delta I_C / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{\alpha}{1 - \alpha}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

EXPRESSION FOR COLLECTOR CURRENT

$$I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_B + I_C = I_B + (\alpha I_E + I_{CBO})$$

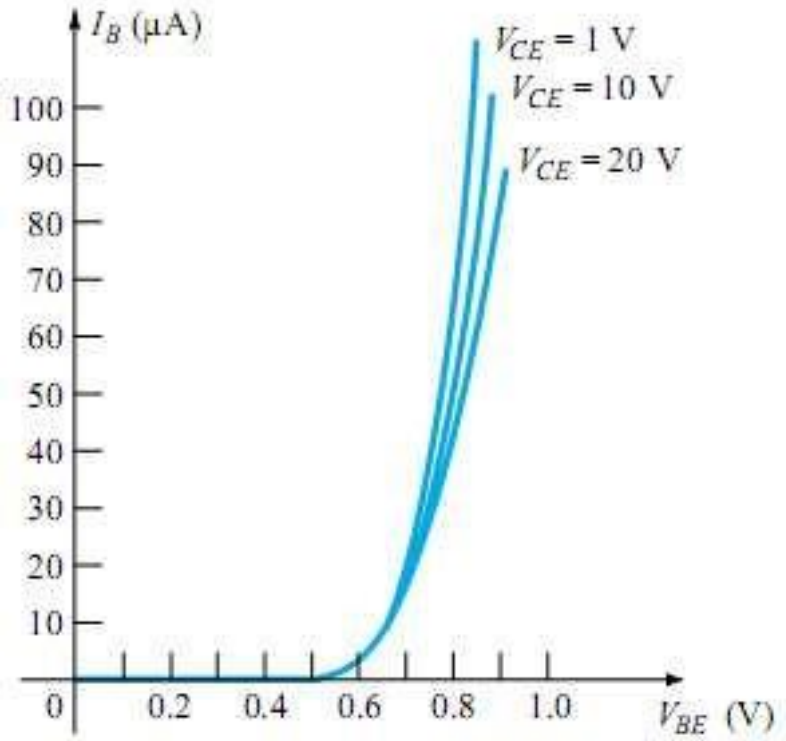
$$I_E(1-\alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

$$I_C \; ; \quad I_E = *(\beta + 1) I_B + (\beta + 1) I_{CBO}$$

CHARACTERISTICS OF COMMON EMITTER CONFIGURATION

- <u>Input Characteristics:</u>



→V_{BE} vs I_B characteristics is called input characteristics.

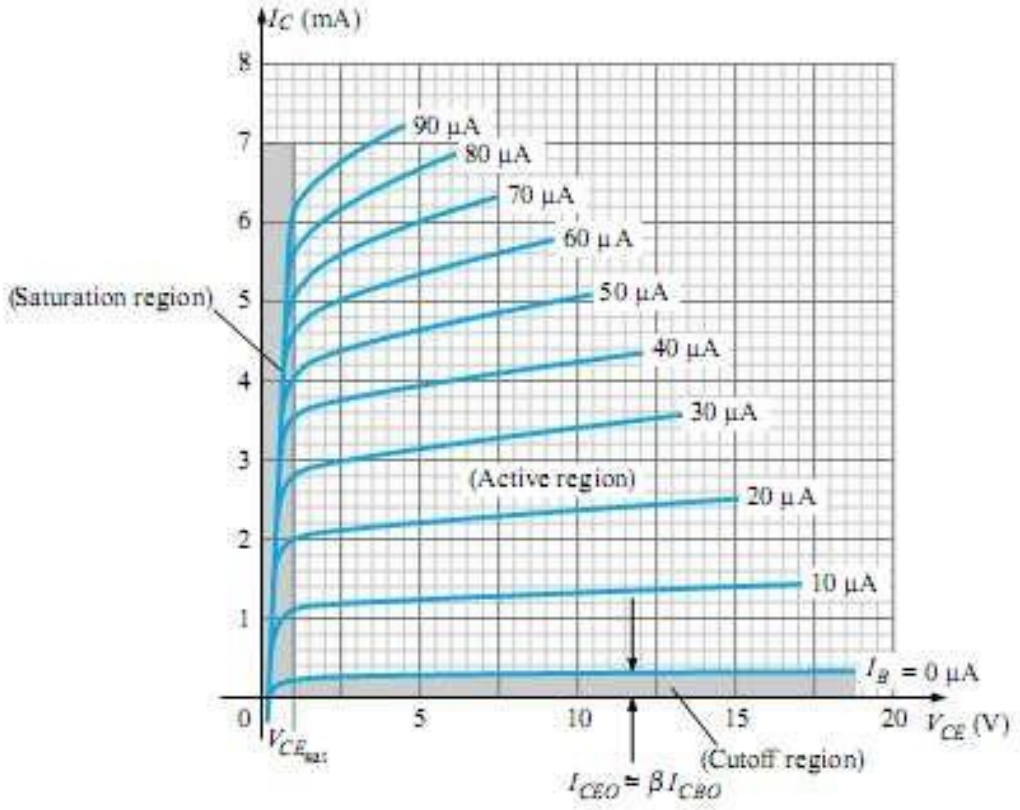
→ I_B increases rapidly with V_{BE} . It means input resistance is very small.

→ I_E almost independent of V_{CE}.

→I_B is of the range of micro amps.

CHARACTERISTICS OF COMMON EMITTER CONFIGURATION

- <u>Output Characteristics:</u>



- V_{CE} vs I_c characteristics is called output characteristics.
- I_C varies linearly with V_{CE} ,only when V_{CE} is very small.
- As, V_{CE} increases, I_C becomes constant.

EXPRESSION FOR COLLECTOR CURRENT

$$I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_B + I_C = I_B + (\alpha I_E + I_{CBO})$$

$$I_E(1-\alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

$$I_C \; ; \quad I_E = *(\beta + 1) I_B + (\beta + 1) I_{CBO}$$

$$\beta = \frac{\alpha}{1-\alpha} \quad \therefore \quad \beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{1}{1-\alpha}$$

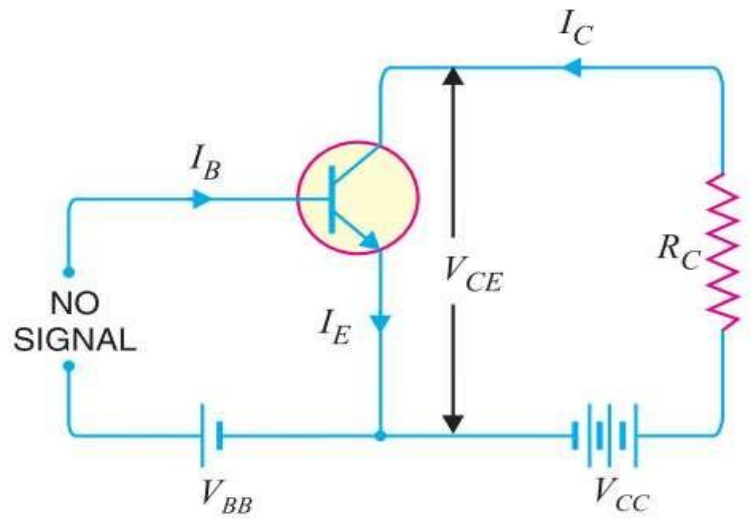
COMPARISON OF TRANSISTOR CONNECTION

S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (about 100 Ω)	Low (about 750 Ω)	Very high (about 750 kΩ)
2.	Output resistance	Very high (about 450 kΩ)	High (about 45 kΩ)	Low (about 50 Ω)
3.	Voltage gain	about 150	about 500	less than 1
4.	Applications	For high frequency applications	For audio frequency applications	For impedance matching
5.	Current gain	No (less than 1)	High (β)	Appreciable

TRANSISTOR LOAD LINE ANALYSIS

- In transistor circuit analysis it is necessary to determine collector current for various V_{CE} voltage.
- One method is we can determine the collector current at any desired V_{CE} voltage, from the output characteristics.
- More conveniently we can use load line analysis to determine operating point.

TRANSISTOR LOAD LINE ANALYSIS



- Consider common emitter npn transistor ckt shown in figure.
- There is no input signal.
- Apply KVL in the output ckt-

$$V_{CE} = V_{CC} - I_C R_C$$

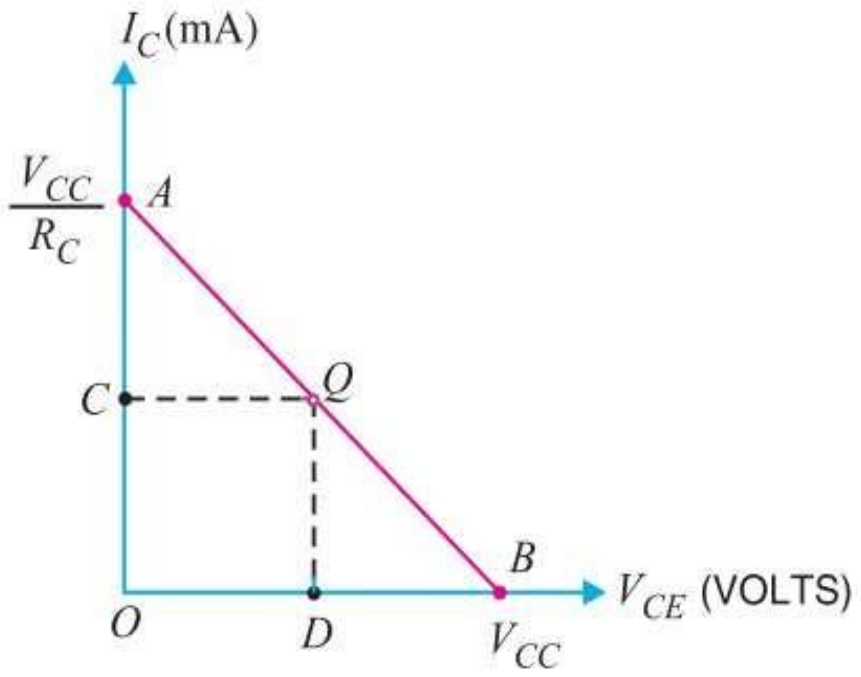
(*i*) When the collector current $I_C = 0$, then collector-emitter voltage is maximum and is equal to V_{CC} *i.e.*

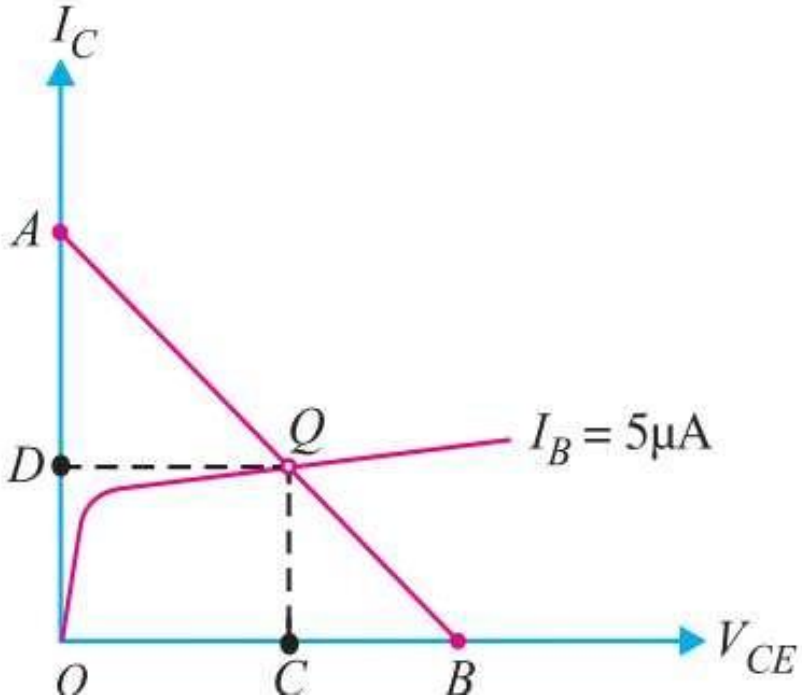
$$\text{Max. } V_{CE} = V_{CC} - I_C R_C$$
$$= V_{CC} \qquad (\because I_C = 0)$$

When collector-emitter voltage $V_{CE} = 0$,

$$V_{CE} = V_{CC} - I_C R_C$$
$$0 = V_{CC} - I_C R_C$$
$$\text{Max. } I_C = V_{CC}/R_C$$

TRANSISTOR LOAD LINE ANALYSIS

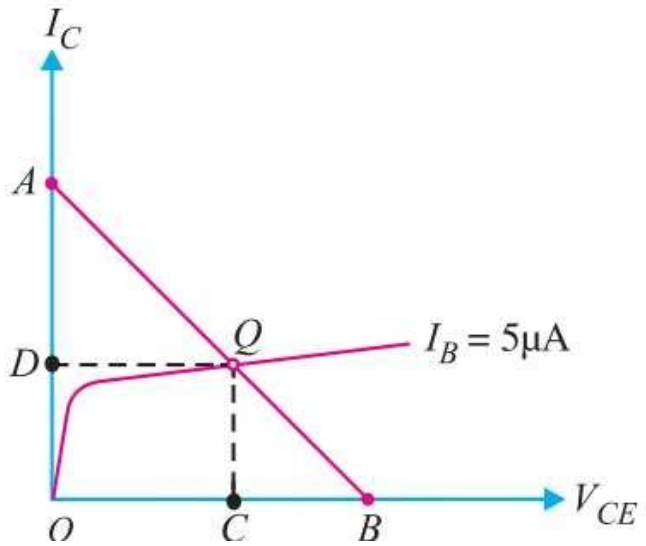




OPERATING POINT

The zero signal values of I_C and V_{CE} are known as the **operating point.**

- It is called operating point because variation of I_C takes place about this point.
- It is also called quiescent point or Q-point.

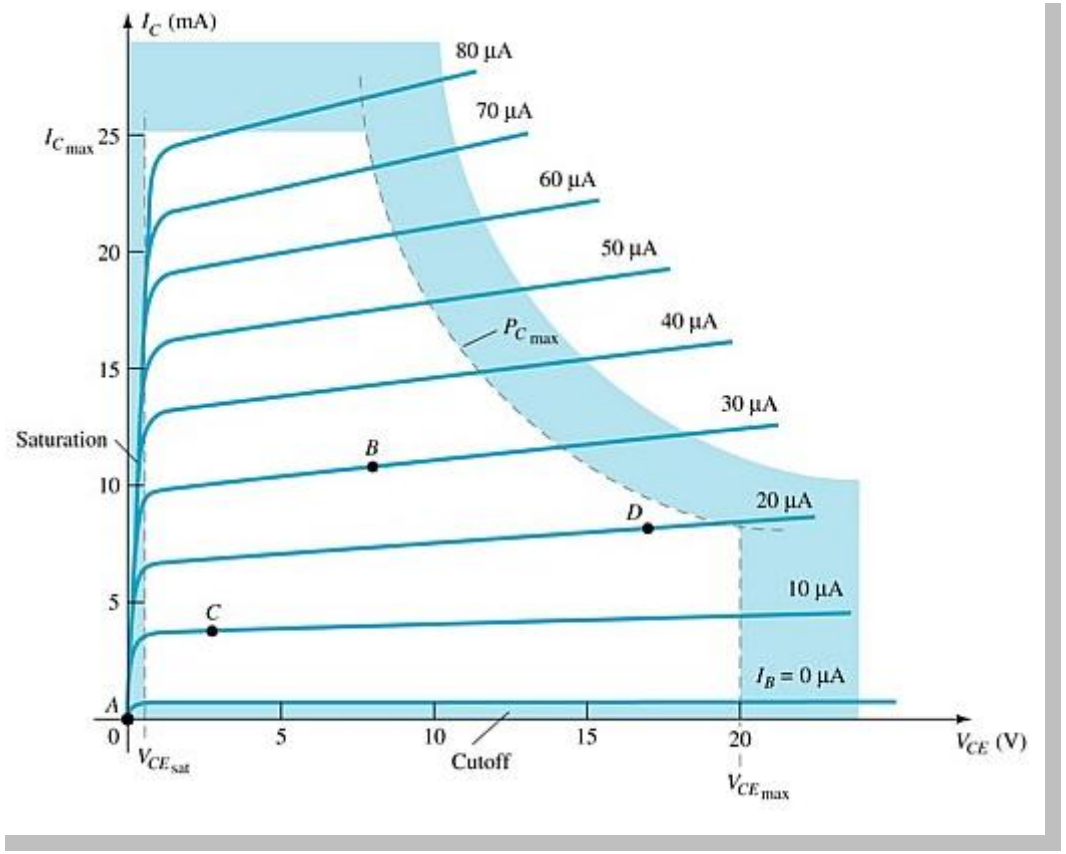


Biasing

Biasing: The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.

OPERATING POINT

The DC input establishes an operating or *quiescent point* called the *Q-point*.



THE THREE STATES OF OPERATION

- **Active or Linear Region Operation** **Base–Emitter junction is forward biased Base–Collector junction is reverse biased**

- **Cutoff Region Operation**

  Base–Emitter junction is reverse biased

- **Saturation Region Operation**

  Base–Emitter junction is forward biased Base–Collector junction is forward biased

No matter what type of configuration a transistor is used in, the basic relationships between the currents are always the same, and the base-to- emitter voltage is the threshold value if the transistor is in the “on” state

$$V_{BE} = 0.7V$$

$$I_E = (\beta + 1)I_B \cong I_C$$

$$I_C = \beta I_B$$

- The operating point defines where the transistor will operate on its characteristics curves under dc conditions.
- For linear (minimum distortion) amplification, the dc operating point should not be too close to the maximum power, voltage, or current rating and should avoid the regions of saturation and cutoff.

DC BIASING CIRCUITS

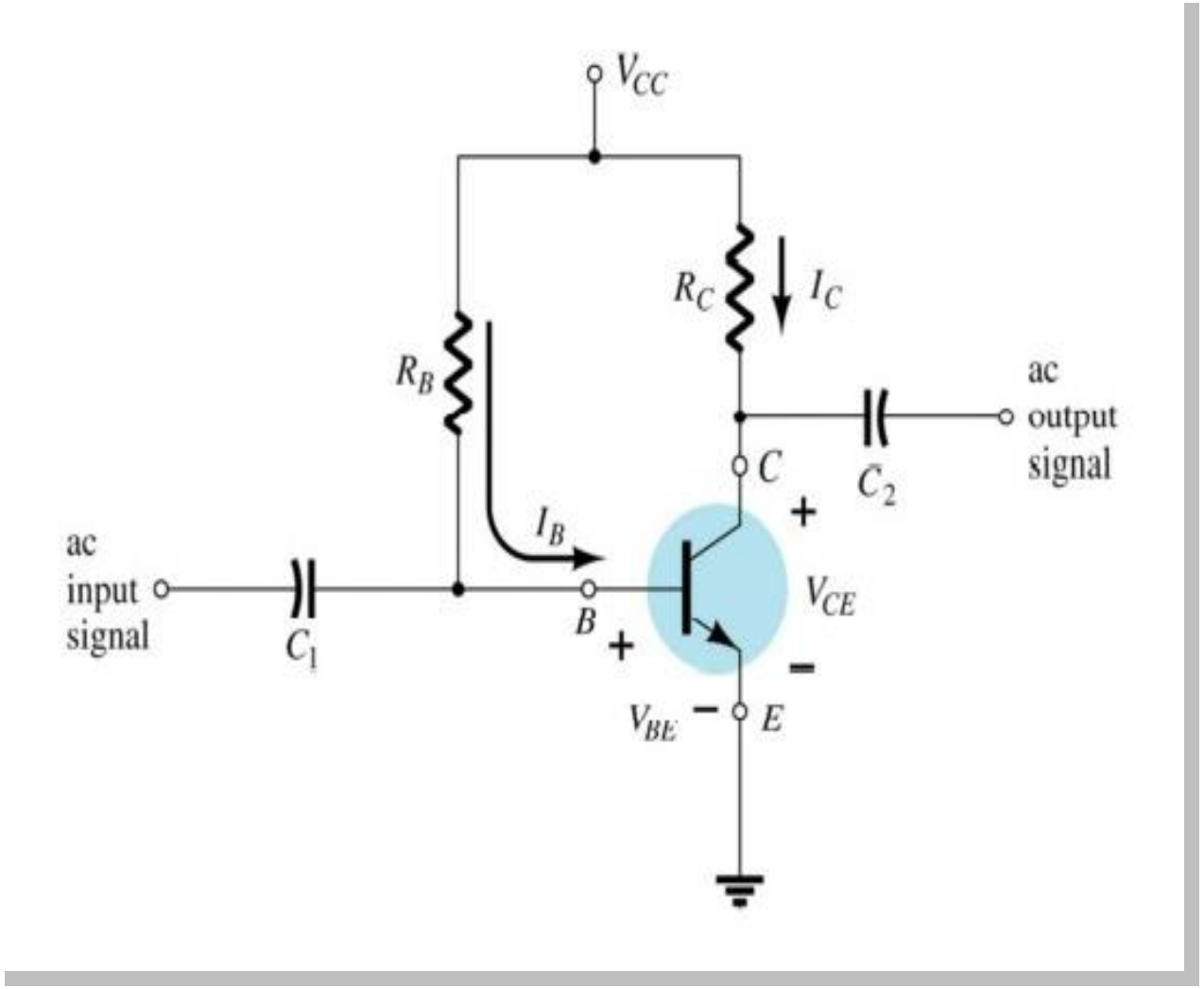
- **Fixed-bias circuit**
- **Emitter-follower bias circuit**
- **Voltage divider bias circuit**

I. FIXED BIAS

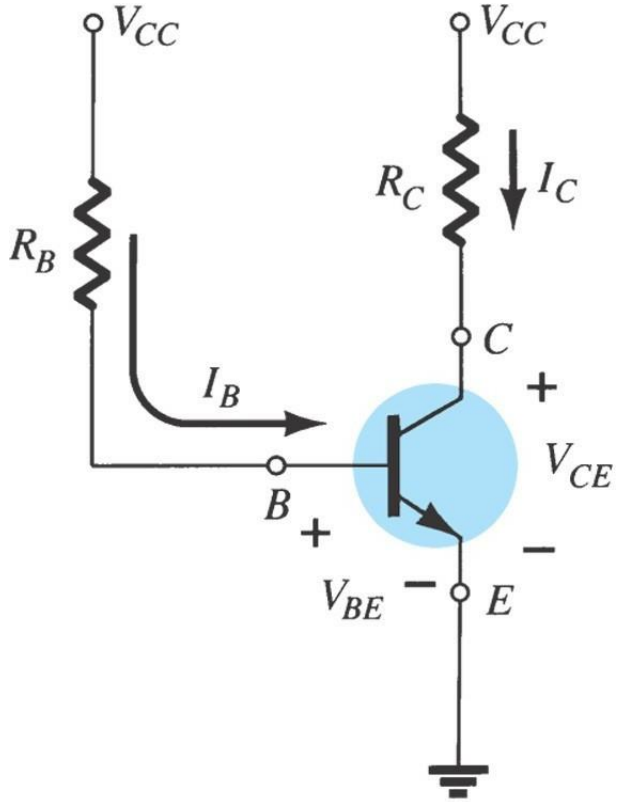
- The fixed-bias configuration is the simplest of transistor biasing arrangements, but it is also quite unstable

- For most configurations the dc analysis begins with a determination of the base current

- For the dc analysis of a transistor network, all capacitors are replaced by an open-circuit equivalent



Fixed-bias circuit



The dc equivalent circuit of the fixed bias circuit where the capacitor is replaced with an open-circuit

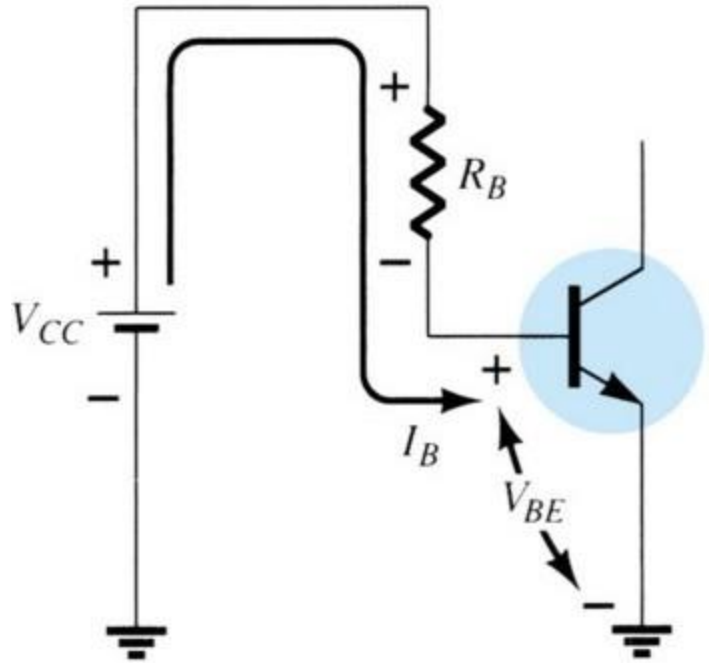
THE BASE-EMITTER LOOP

From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



COLLECTOR-EMITTER LOOP

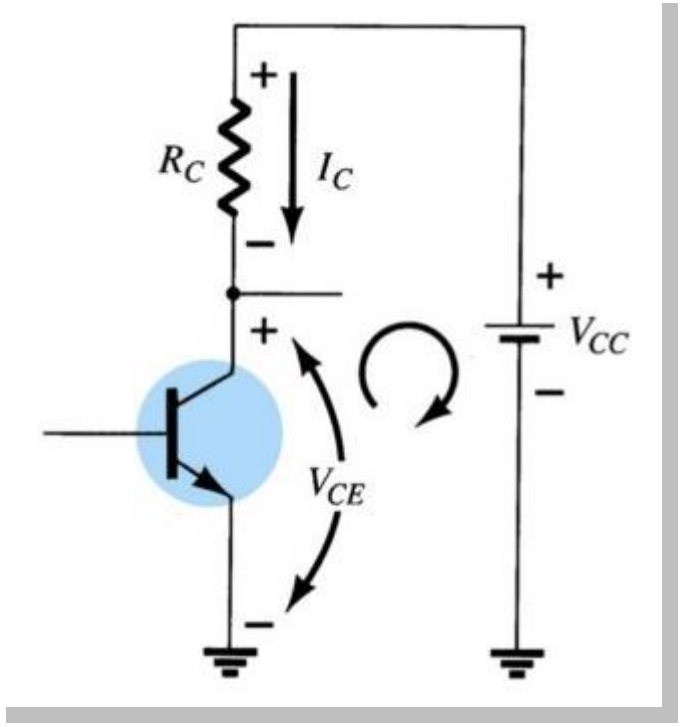
Collector current:

$$\mathbf{I_C = \beta I_B}$$

From Kirchhoff's voltage law:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

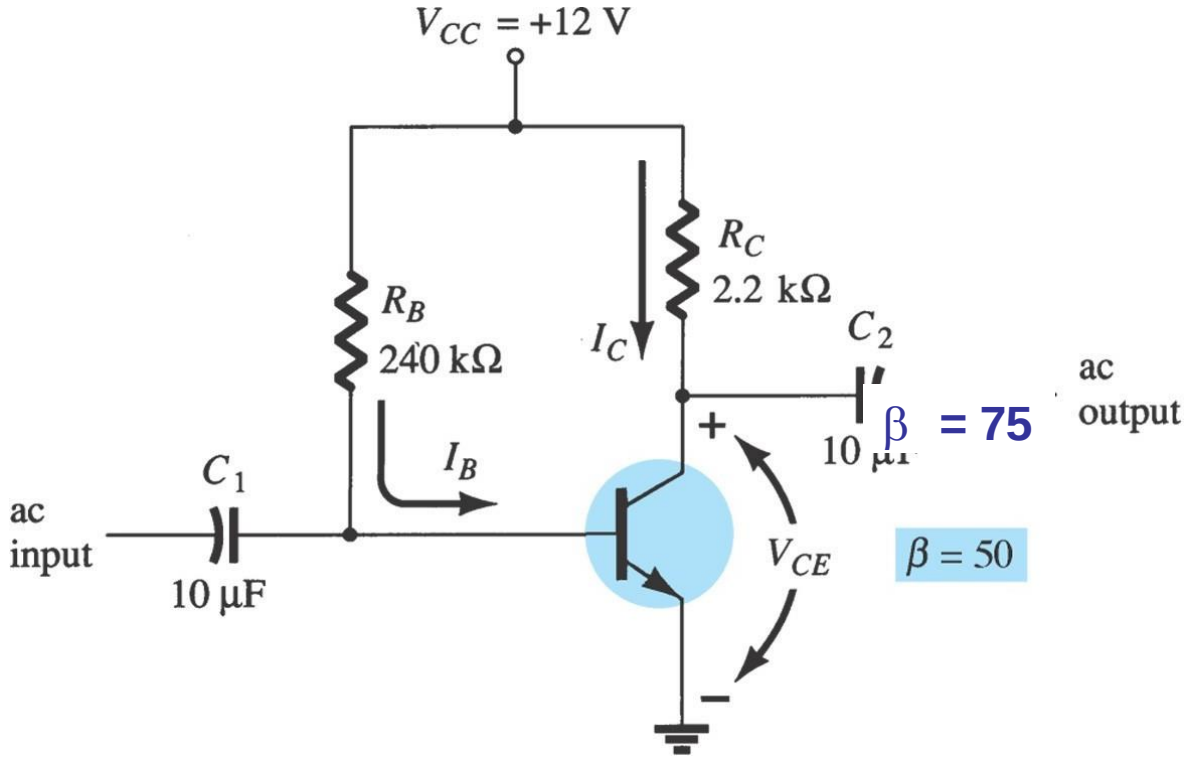
$$\mathbf{V_{CE} = V_{CC} - I_C R_C}$$



EXAMPLE:

Determine the following for the fixed-bias configuration of the figure shown:

(a) I_{BQ} and I_{CQ} (b) V_{CEQ} (c) V_B and V_C (d) V_{BC}



SATURATION

- Saturation conditions are normally avoided because the base-collector junction is no longer reverse – biased and the output amplified will be distorted.

- For a transistor operating in the saturation region, the current is a maximum value for the particular design. Change the design and the corresponding saturation level may rise or drop

- The highest collector current saturation level is defined by the maximum as provided by the specification sheet.

SATURATION

When the transistor is operating in saturation, current through the transistor is at its *maximum* possible value.

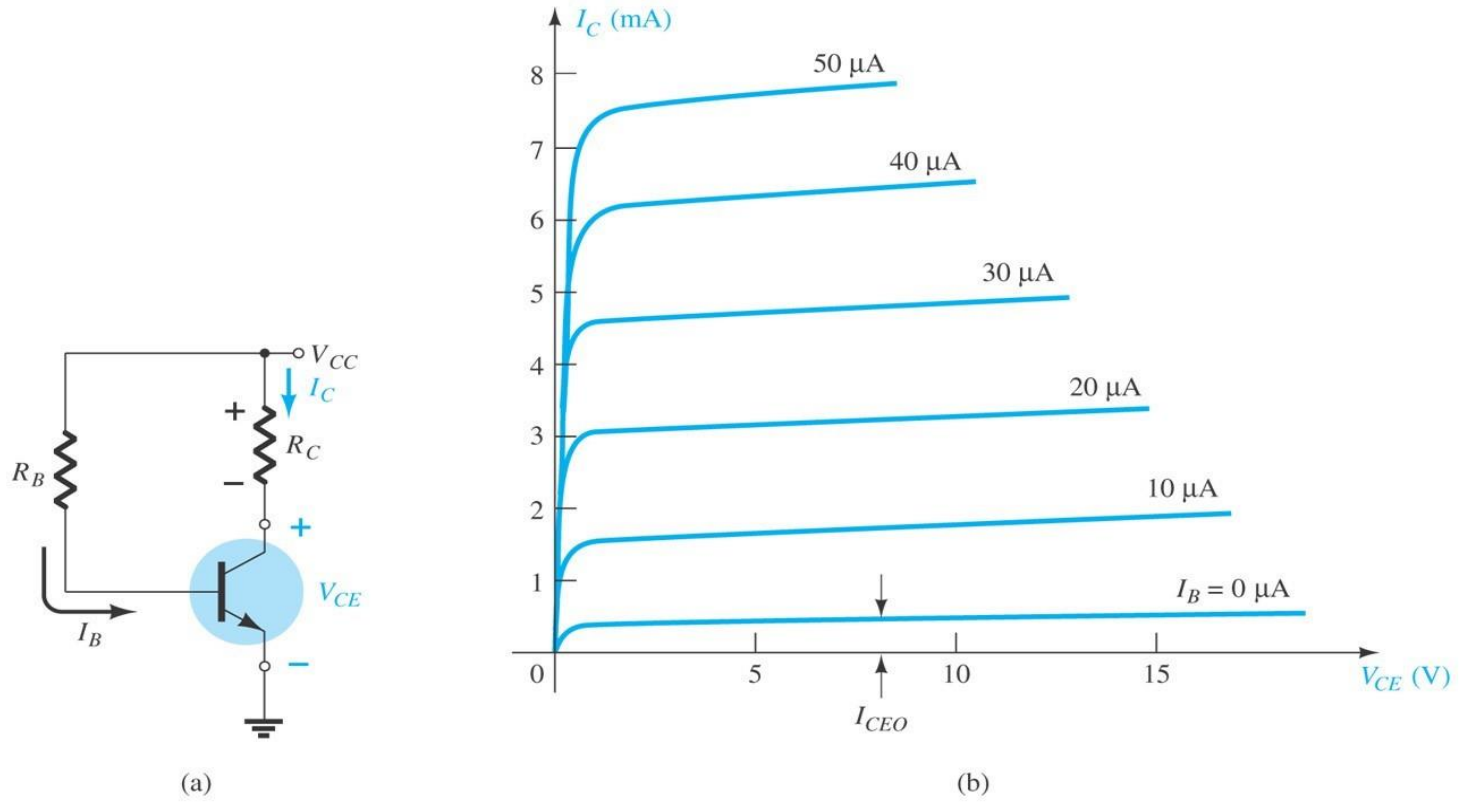
$$I_{C\,sat} = \frac{V_{CC}}{R_C}$$

$$V_{CE} \cong 0\ V$$

In the previous example, the saturation level for the network is given by:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{12V}{2.2k\Omega} = 5.45mA$$

LOAD LINE ANALYSIS



The variables I_C and V_{CE} are related by the equation:

$$V_{CE} = V_{CC} - I_C R_C$$

LOAD LINE ANALYSIS

The end points of the load line are:

I_{Csat}

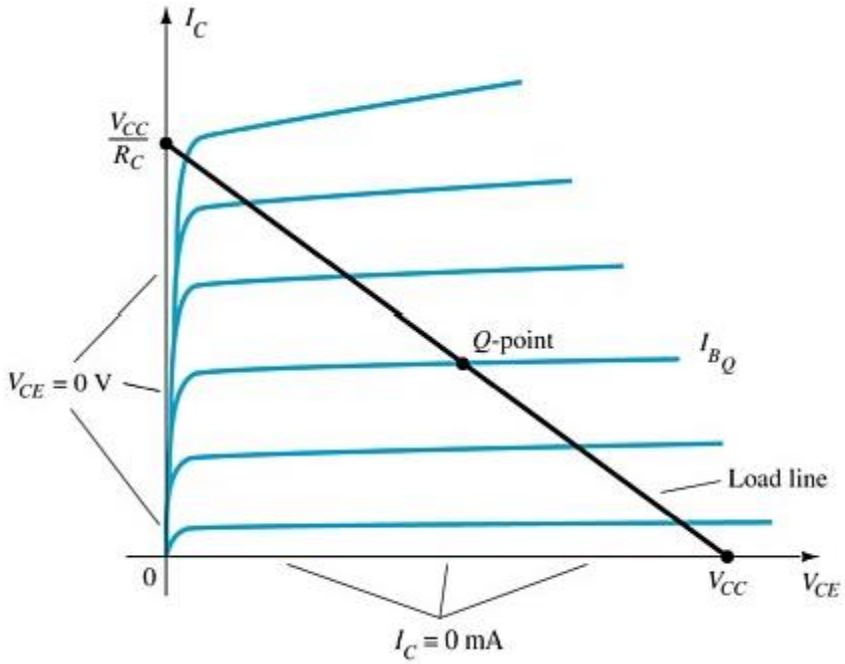
$V_{CE} = 0$ V

$I_C = V_{CC} / R_C$

$V_{CEcutoff}$

$I_C = 0$ mA

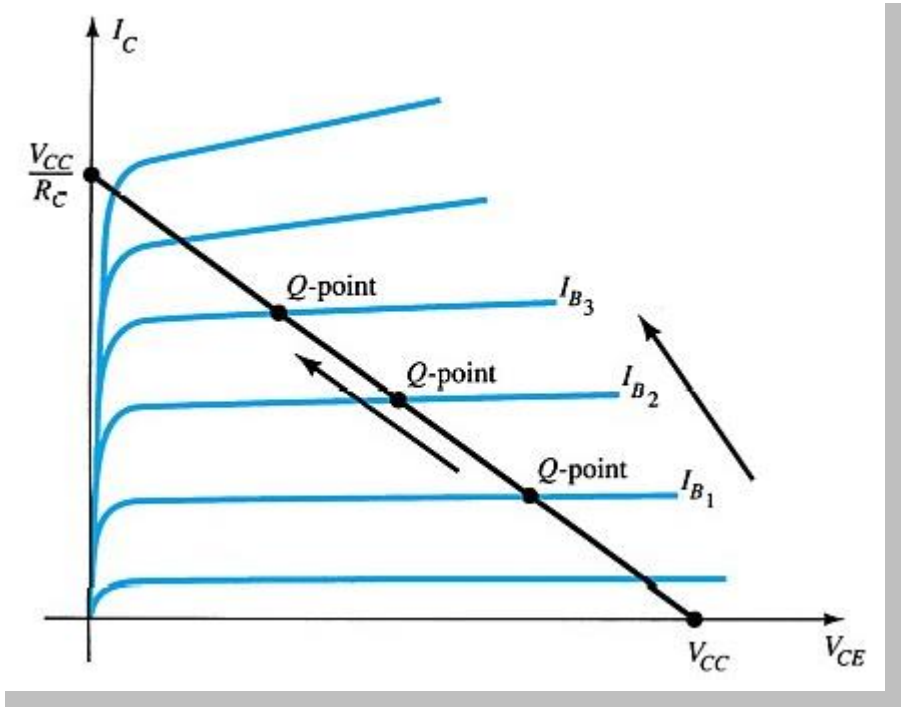
$V_{CE} = V_{CC}$



The *Q*-point is the operating point:

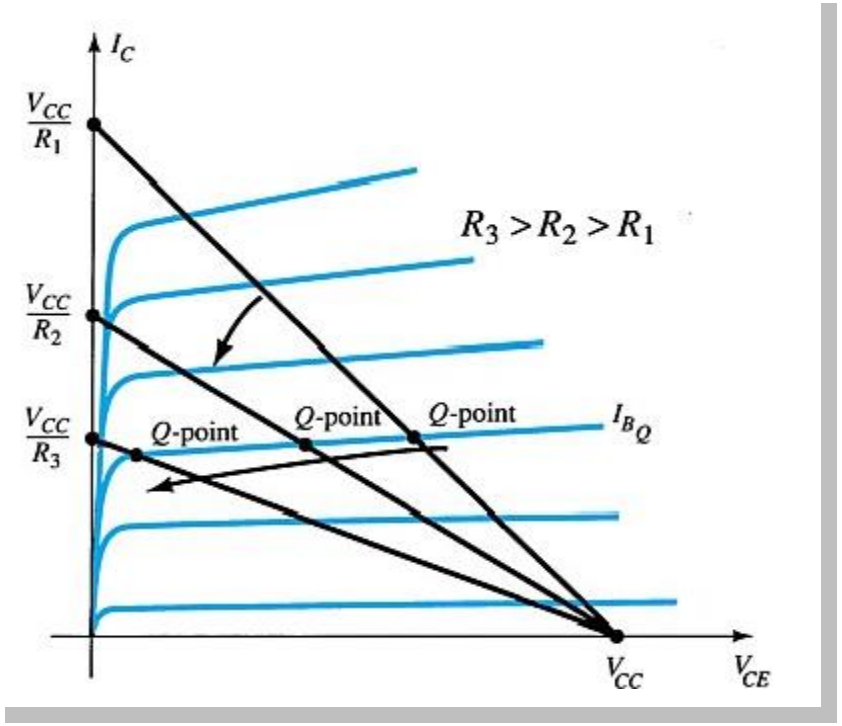
- where the value of R_B sets the value of I_B
- that sets the values of V_{CE} and I_C

CIRCUIT VALUES AFFECT THE Q-POINT



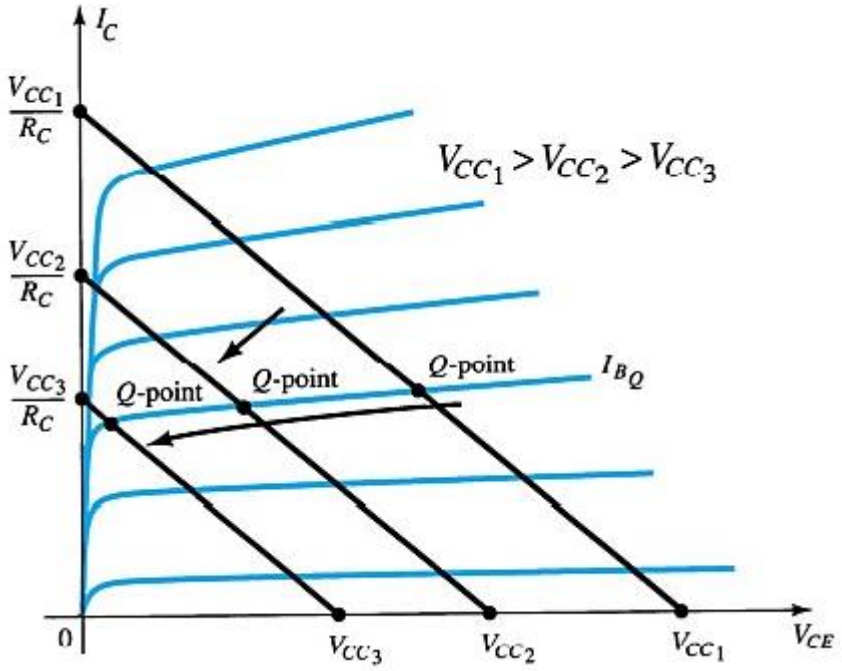
[Movement of the Q-point with increasing level of I_B]

CIRCUIT VALUES AFFECT THE Q-POINT



[Effect of an increasing level of R_C on the load line the *Q*-point]

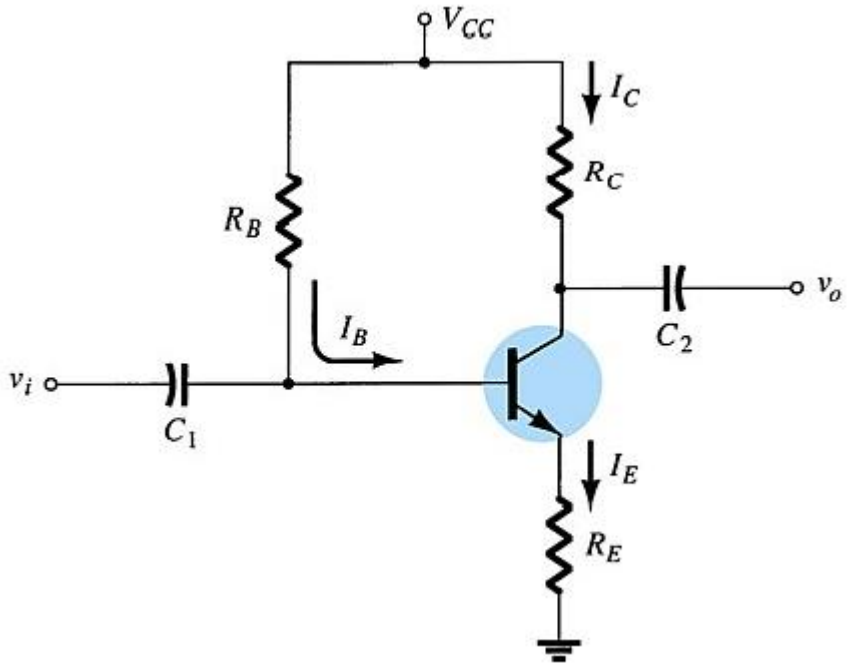
CIRCUIT VALUES AFFECT THE Q-POINT



[Effect of lower values of V_{CC} on the load line the *Q*-point]

II. EMITTER-STABILIZED BIAS CIRCUIT

Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.



BASE-EMITTER LOOP

From Kirchhoff's voltage law:

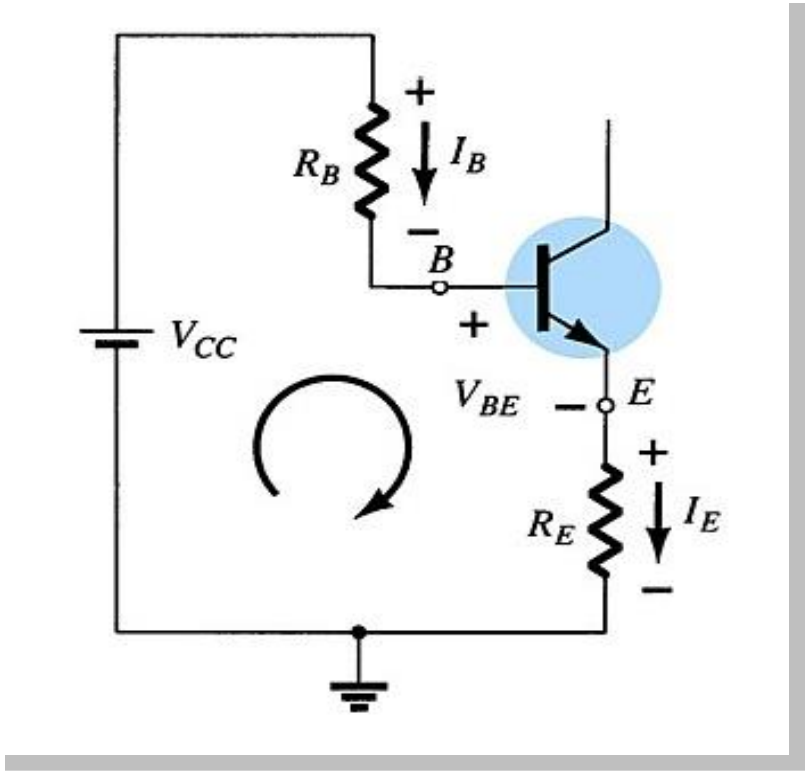
$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$:

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

Solving for I_B:

$$\mathbf{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}}$$



COLLECTOR-EMITTER LOOP

From Kirchhoff's voltage law:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \cong I_C$:

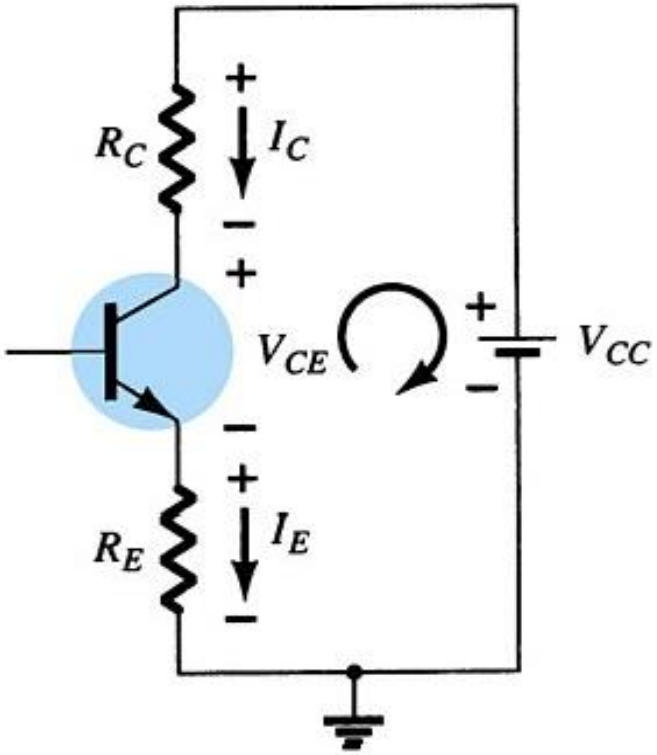
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Also:

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C \quad V_B = V_{CC} -$$

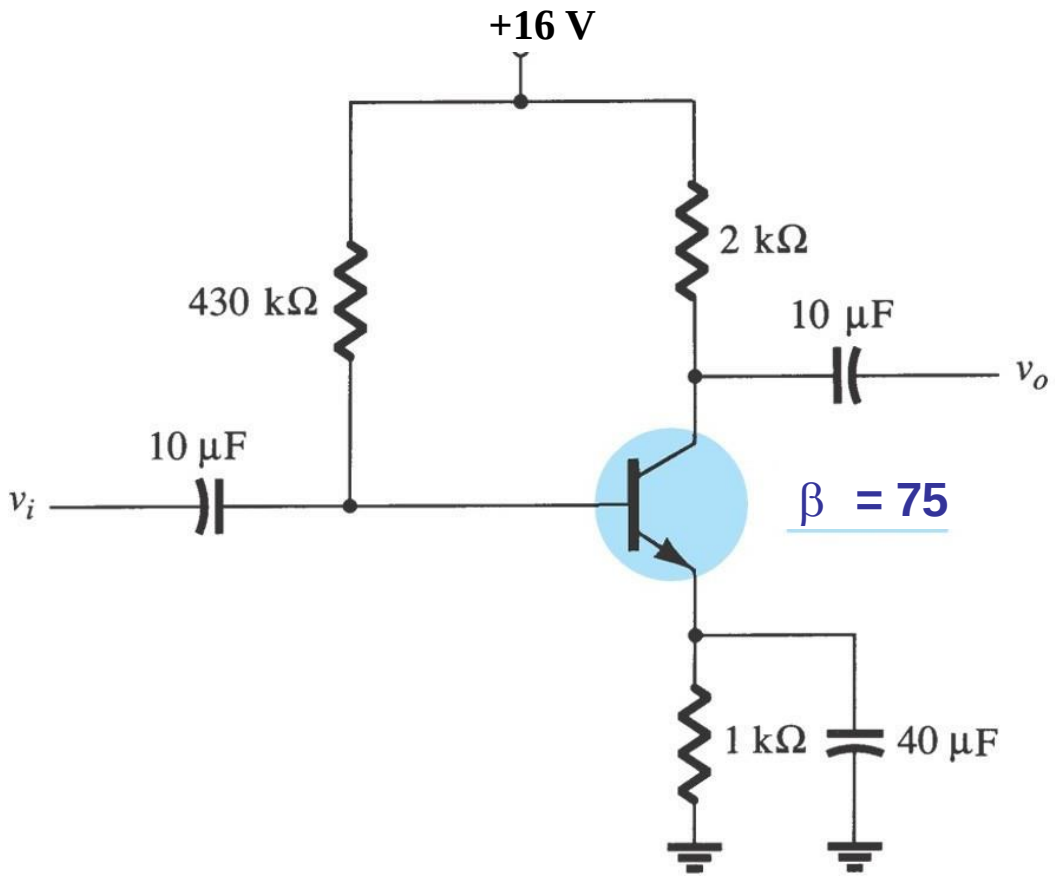
$$I_R R_B = V_{BE} + V_E$$



EXAMPLE:

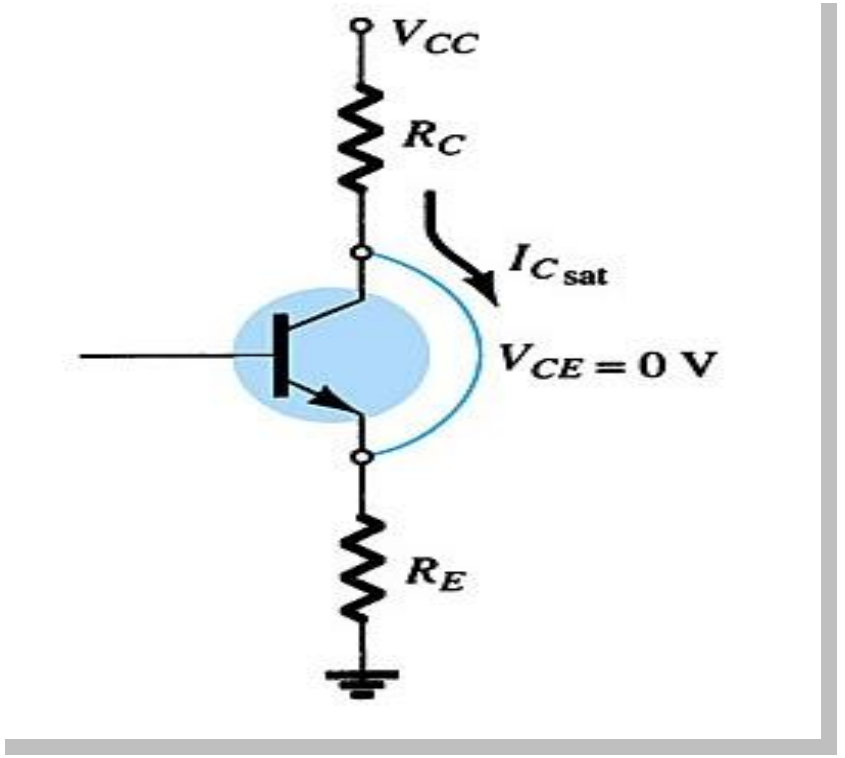
Determine the following for the emitter bias network of the figure shown:

(a) I_B (b) I_C (c) V_{CE} (d) V_C (e) V_E (f) V_B (g) V_{BC}



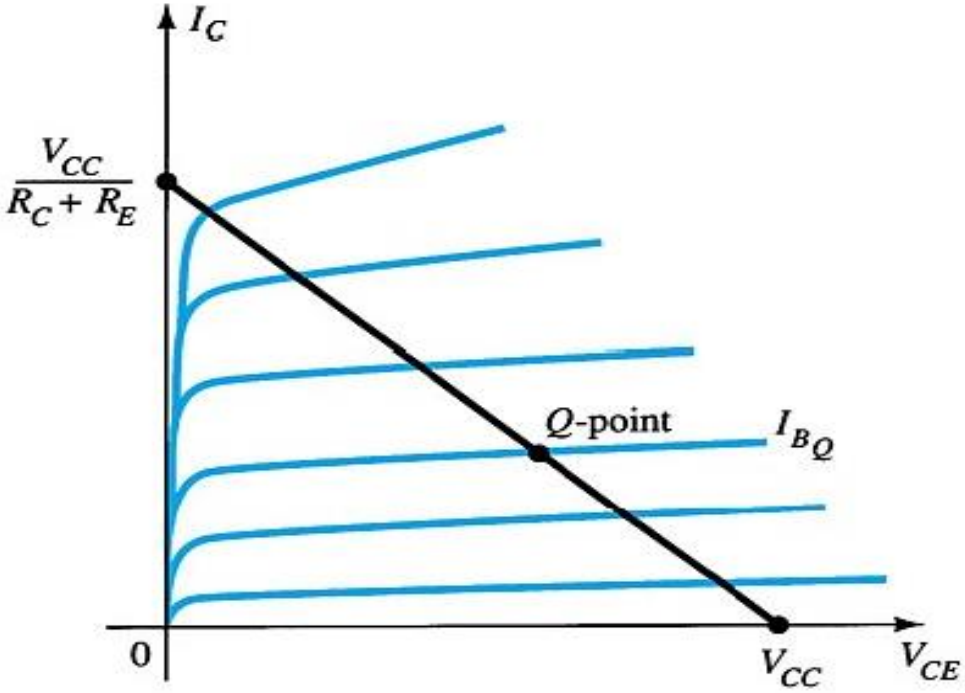
SATURATION LEVEL

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$



LOAD-LINE ANALYSIS

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



The endpoints can be determined from the load line.

$V_{CEcutoff}$:

$V_{CE} = V_{CC}$

$I_C = 0$ mA

I_{Csat}:

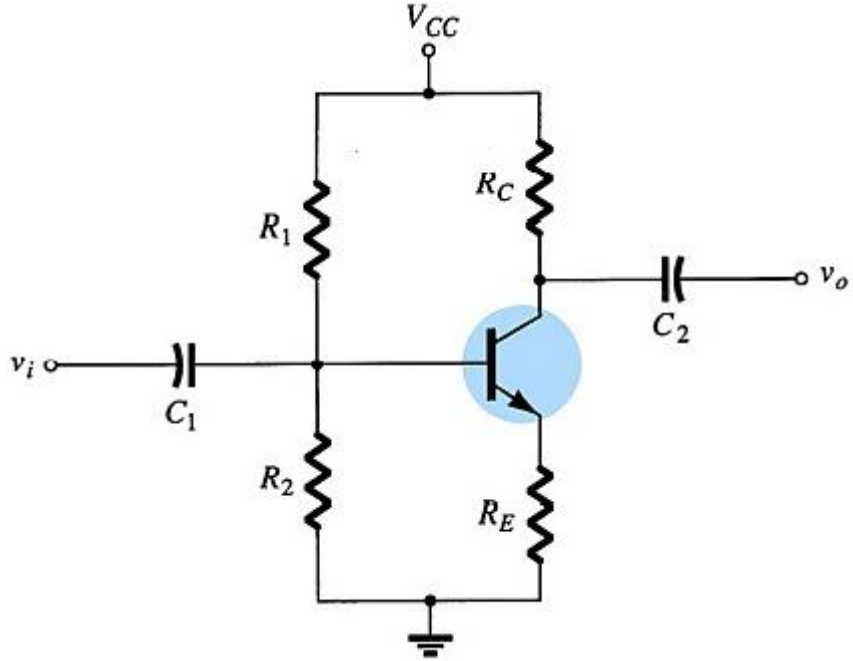
$V_{CE} = 0$ V

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

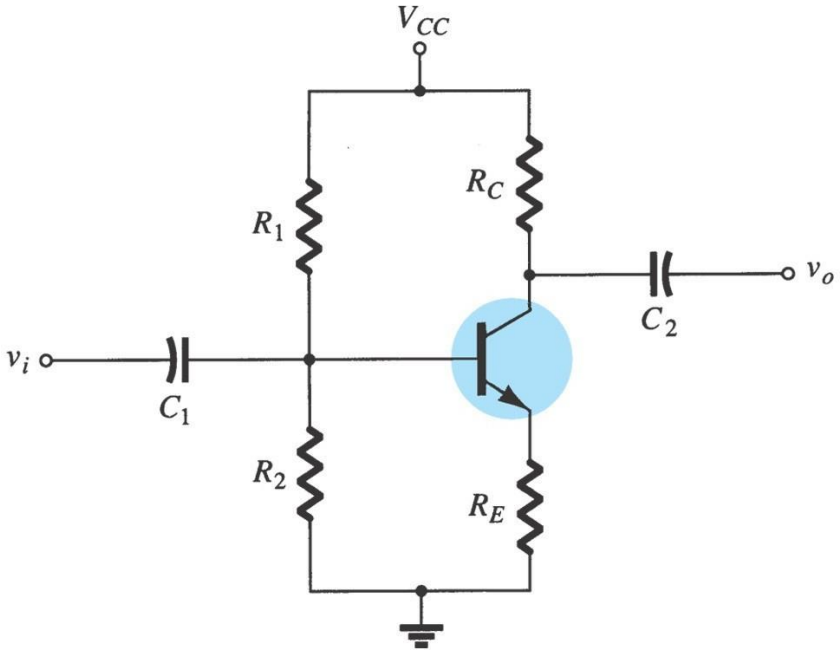
III. VOLTAGE DIVIDER BIAS

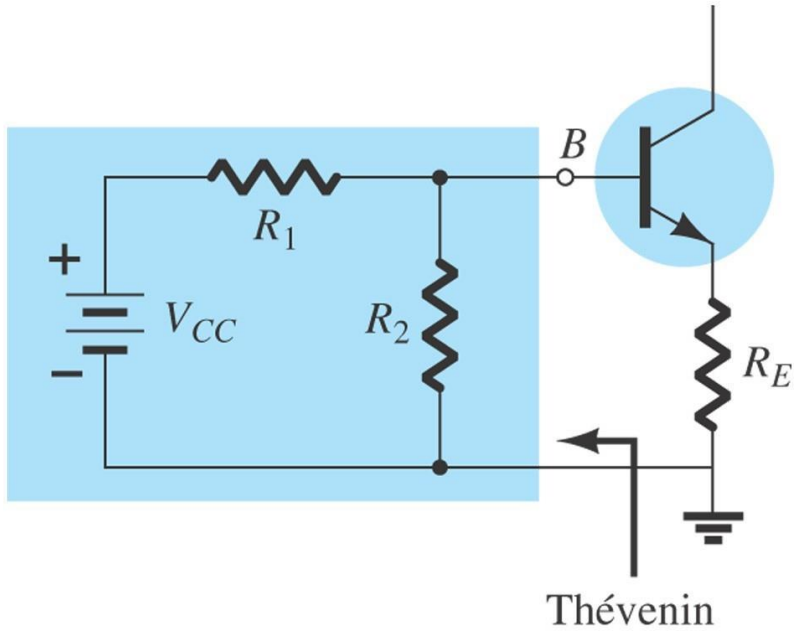
This is a very stable bias circuit.

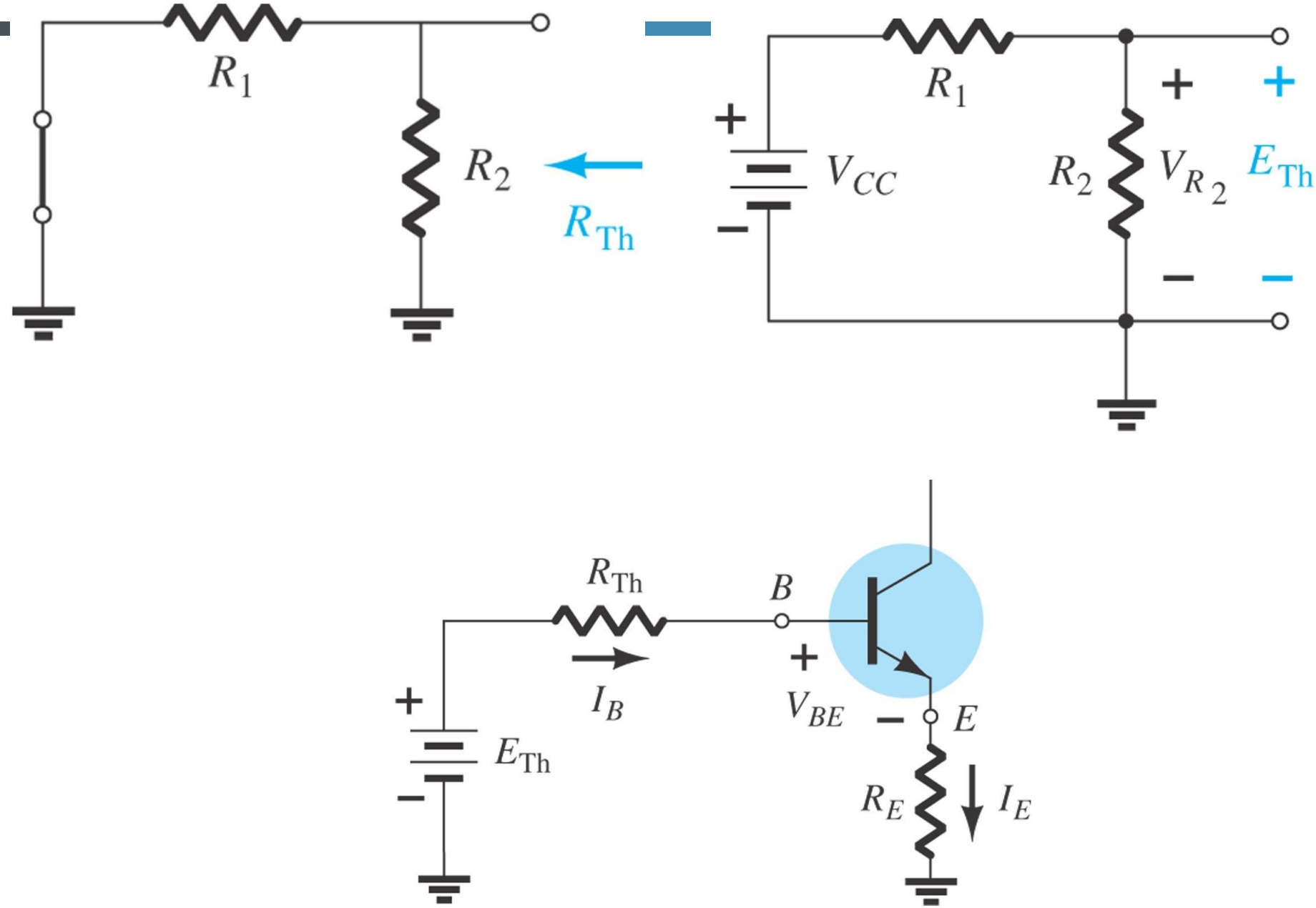
The currents and voltages are nearly independent of any variations in β.



EXACT ANALYSIS:






R_1
R_2
R_{Th}
V_{CC}
R_1
R_2
V_{R_2}
E_{Th}
R_{Th}
B
I_B
V_{BE}
E
E_{Th}
R_E
I_E

$$R_{Th} = R_1 \| R_2 \qquad E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Applying Kirchhoff's voltage law in the clockwise direction in the Thevenin network,

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$ (Substituting $I_E = (\beta+1) I_B$)

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

VOLTAGE DIVIDER BIAS ANALYSIS

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$

$$I_C = 0mA$$

Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0V$$

Q: In a common base connection, current amplification factor is 0.9. If the emitter current is 1mA, determine the value of base current.

Sol:

$$\text{Here, } \alpha = 0.9, \quad I_E = 1\ \text{mA}$$

$$\text{Now} \qquad \alpha = \frac{I_C}{I_E}$$

$$\textit{or} \qquad I_C = \alpha I_E = 0.9 \times 1 = 0.9\ \text{mA}$$

$$\text{Also} \qquad I_E = I_B + I_C$$

$$\therefore \qquad \text{Base current, } I_B = I_E - I_C = 1 - 0.9 = \mathbf{0.1\ mA}$$

Q: In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50 µA. Find the total collector current. Given that α = 0.92.

Sol:

$$\text{Here, } I_E = 1\ \text{mA}, \alpha = 0.92, \quad I_{CBO} = 50\ \mu\text{A}$$

$$\therefore \qquad \text{Total collector current, } I_C = \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3}$$

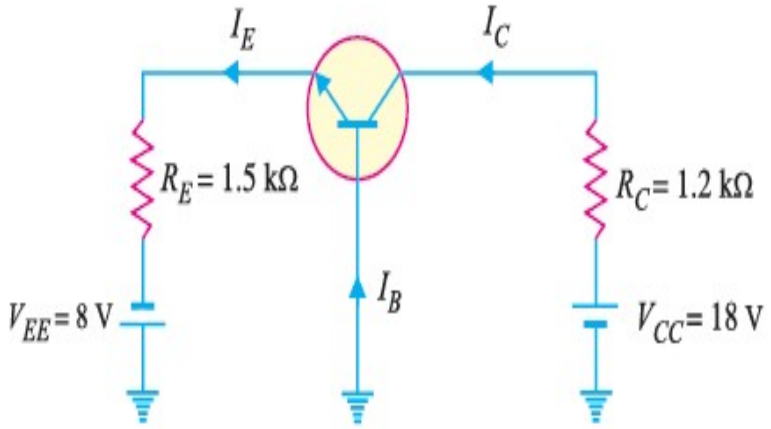
$$= 0.92 + 0.05 = \mathbf{0.97\ mA}$$

Q: For the common base circuit shown in Fig. determine I_C and V_{CB} . Assume the transistor to be of silicon.

- **Solution :**

Since the transistor is of silicon, V_{BE} = 0.7V.

Applying Kirchhoff's voltage law to the emitter side loop, we get,



$$V_{EE} = I_E R_E + V_{BE}$$

$$\text{or} \quad I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{8V - 0.7V}{1.5\ \text{k}\Omega} = 4.87\ \text{mA}$$

$$\therefore \quad I_C \simeq I_E = \mathbf{4.87\ mA}$$

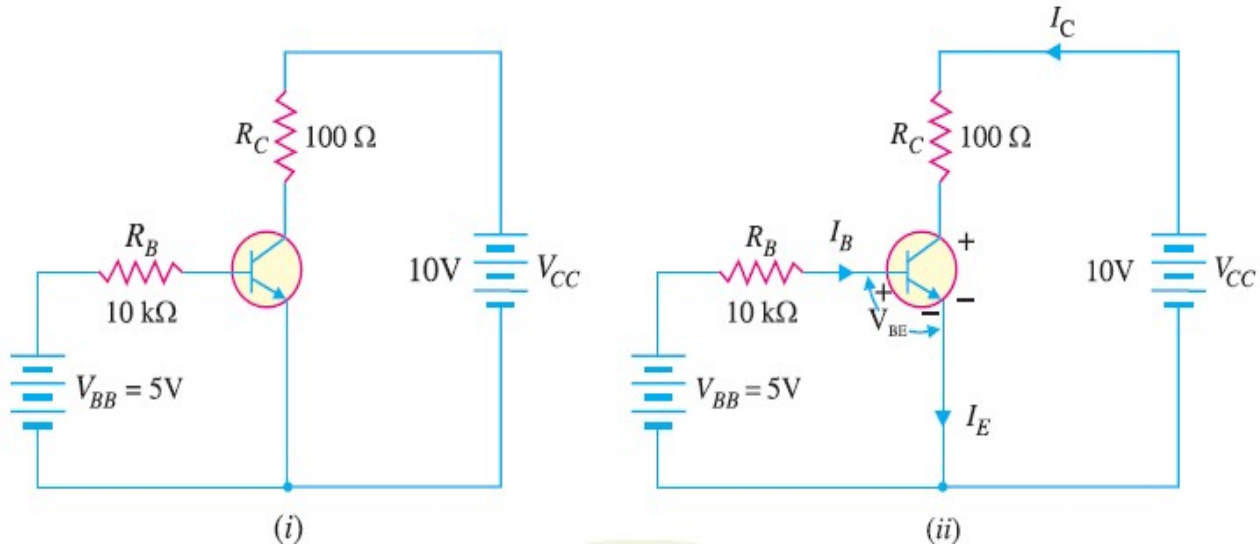
$$V_{CC} = I_C R_C + V_{CB}$$

$$\therefore \quad V_{CB} = V_{CC} - I_C R_C$$

$$= 18\ \text{V} - 4.87\ \text{mA} \times 1.2\ \text{k}\Omega = \mathbf{12.16\ V}$$

Determine V_{CB} in the transistor circuit shown in Fig. (i). The transistor is of silicon and has β = 150.

- **Solution :**



Applying Kirchhoff's voltage law to base-emitter loop, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

or $$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5\text{V} - 0.7\text{V}}{10\ k\Omega} = 430\ \mu\text{A}$$

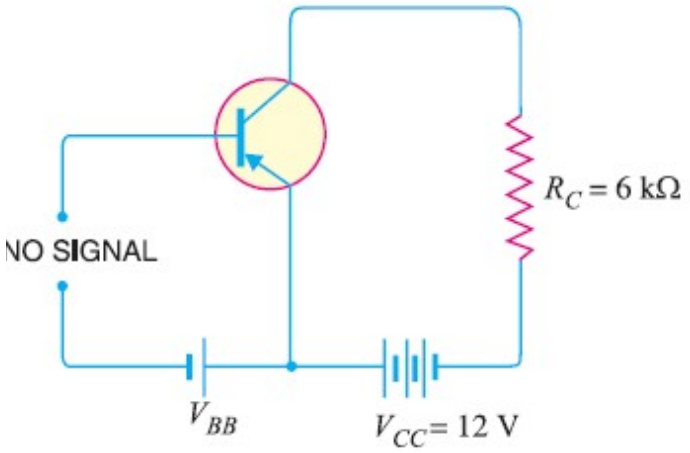
$\therefore$ $$I_C = \beta I_B = (150)(430\ \mu\text{A}) = 64.5\ \text{mA}$$

Now $$V_{CE} = V_{CC} - I_C R_C$$
$$= 10\text{V} - (64.5\ \text{mA})\ (100\Omega) = 10\text{V} - 6.45\text{V} = 3.55\text{V}$$

We know that : $$V_{CE} = V_{CB} + V_{BE}$$

$\therefore$ $$V_{CB} = V_{CE} - V_{BE} = 3.55 - 0.7 = \mathbf{2.85V}$$

Q: In the circuit diagram shown in Fig., if V_{CC} = 12V and R_C = 6 kΩ, draw the d.c. load line. What will be the Q point if zero signal base current is 20μA and β = 50 ?



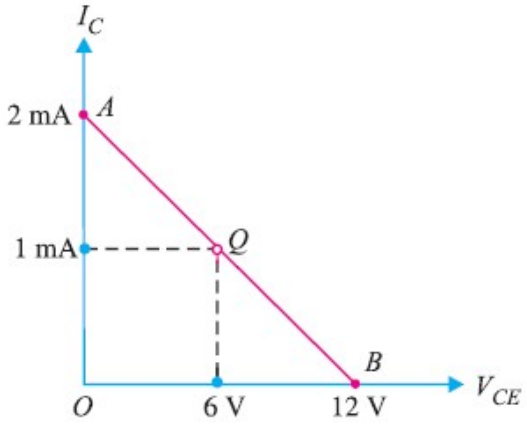
The collector-emitter voltage V_{CE} is given by :

$$V_{CE} = V_{CC} - I_C R_C$$

When $I_C = 0$, $V_{CE} = V_{CC} = 12$ V. This locates the point B of the load line.

When $V_{CE} = 0$, $I_C = V_{CC} / R_C = 12\ V/6\ k\Omega = 2$ mA.

This locates the point A of the load line. By joining these two points, load line AB is constructed as shown



Zero signal base current, $I_B = 20\ \mu A = 0.02$ mA

Current amplification factor, $\beta = 50$

$\therefore$ Zero signal collector current, $I_C = \beta I_B = 50 \times 0.02 = 1$ mA

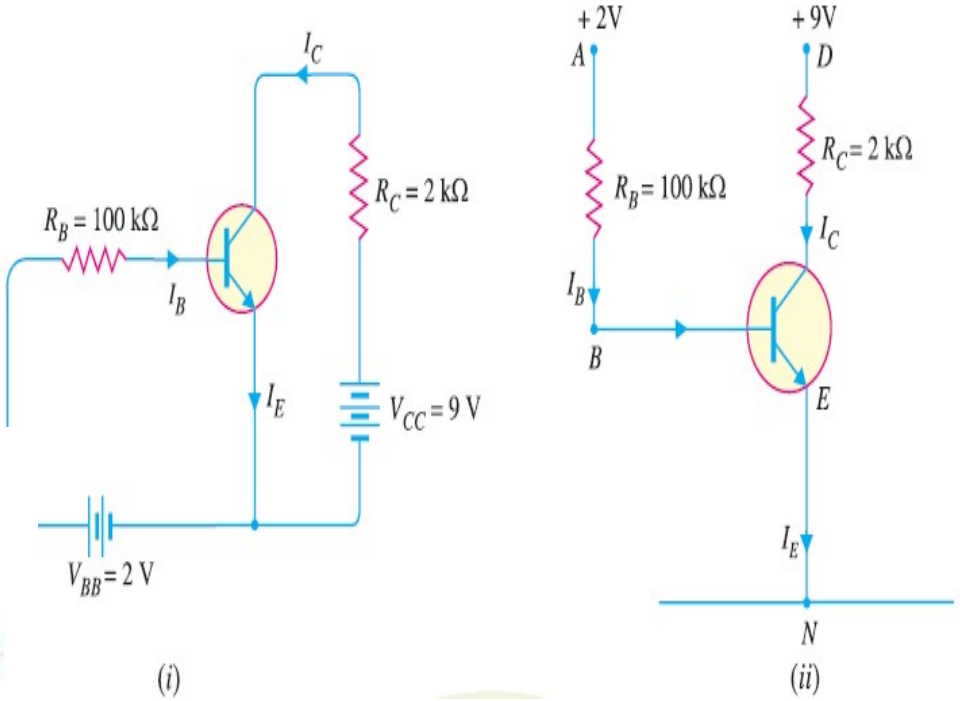
Vce=Vcc-IcRc
Vce=12-1ma.6k=6v

Q. Fig. below shows biasing with fixed bias method. (i) Determine the collector current I_C and collector-emitter voltage V_{CE}. Neglect small base-emitter voltage. Given that β = 50.

- Solution:

In the circuit shown in Fig. 2 (i), biasing is provided by a battery V_{BB} (= 2V) in the base circuit which is separate from the battery V_{CC} (= 9V) used in the output circuit.

The same circuit is shown in a simplified way in Fig. 2 (ii). Here, we need show only the supply voltages, + 2V and +9V. It may be noted that negative terminals of the power supplies are grounded to get a complete path of current.



$$I_B R_B + V_{BE} = 2\ \text{V}$$

As V_{BE} is negligible,

$$\therefore \quad I_B = \frac{2\text{V}}{R_B} = \frac{2\text{V}}{100\ \text{k}\Omega} = 20\ \mu\text{A}$$

$$\text{Collector current, } I_C = \beta I_B = 50 \times 20\ \mu\text{A} = 1000\ \mu\text{A} = 1\ \text{mA}$$

Applying Kirchhoff's voltage law to the circuit *DEN*, we get,

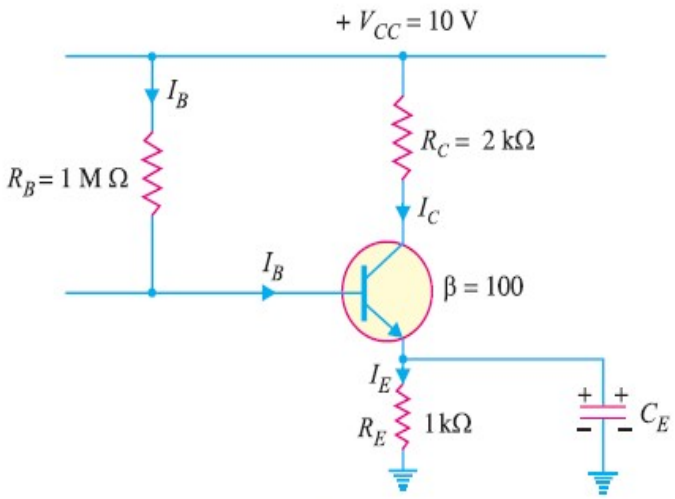
$$I_C R_C + V_{CE} = 9$$

$$\textit{or} \quad 1\ \text{mA} \times 2\ \text{k}\Omega + V_{CE} = 9$$

$$\text{or} \quad V_{CE} = 9 - 2 = 7\ \text{V}$$

Q- Fig. below shows that a silicon transistor with β = 100 is biased by base resistor method. Draw the d.c. load line and determine the operating point.

Solution : Applying Kirchhoff 's voltage law to the base side and taking resistances in kΩ and currents in mA, we have,



$$V_{CC} = I_B R_B + V_{BE} + I_E \times 1$$

or $$10 = 1000\, I_B + 0 + (I_C + I_B)$$

or $$10 = 1000\, I_B + (\beta I_B + I_B)$$

or $$10 = 1000\, I_B + (100\, I_B + I_B)$$

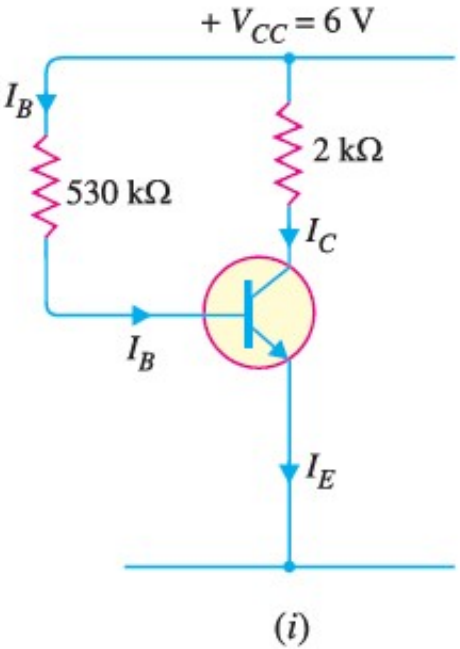
or $$10 = 1101\, I_B$$

$\therefore$ $$I_B = 10/1101 = \mathbf{0.0091\ mA}$$

$$I_C = \beta I_B = 100 \times 0.0091 = \mathbf{0.91\ mA}$$

$$I_E = I_C + I_B = 0.91 + 0.0091 = \mathbf{0.919\ mA}$$

Qu.- Calculate the values of three currents in the circuit shown in Fig



(i)

Solution : D.C. load line

Referring to Fig. (i), $V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0$, $V_{CE} = V_{CC} = 6$ V. This locates the first point B (OB = 6V) of the load line on collector-emitter voltage axis as shown in Fig. 3 (ii).

When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 6V/2\ k\Omega = 3$ mA.

This locates the second point A (OA = 3mA) of the load line on the collector current axis. By joining points A and B, d.c. load line AB is constructed as shown in Fig ii.

For Q point :

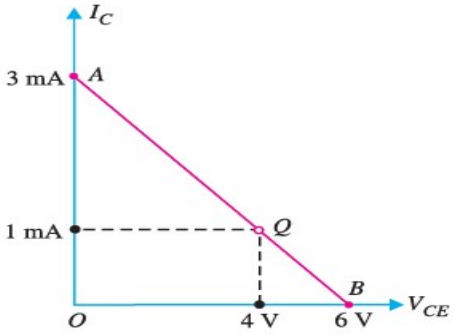
$$I_B R_B + V_{BE} = V_{CC}$$

or
$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{(6 - 0.7)\ \text{V}}{530\ \text{k}\Omega} = 10\ \mu\text{A}$$

$\therefore$ Collector current, $I_C = \beta I_B = 100 \times 10 = 1000\ \mu\text{A} = 1\ \text{mA}$

Collector-emitter voltage, $V_{CE} = V_{CC} - I_C R_C = 6 - 1\ \text{mA} \times 2\ \text{k}\Omega = 6 - 2 = 4\ \text{V}$

$\therefore$ Operating point is **4 V, 1 mA.**



(ii)