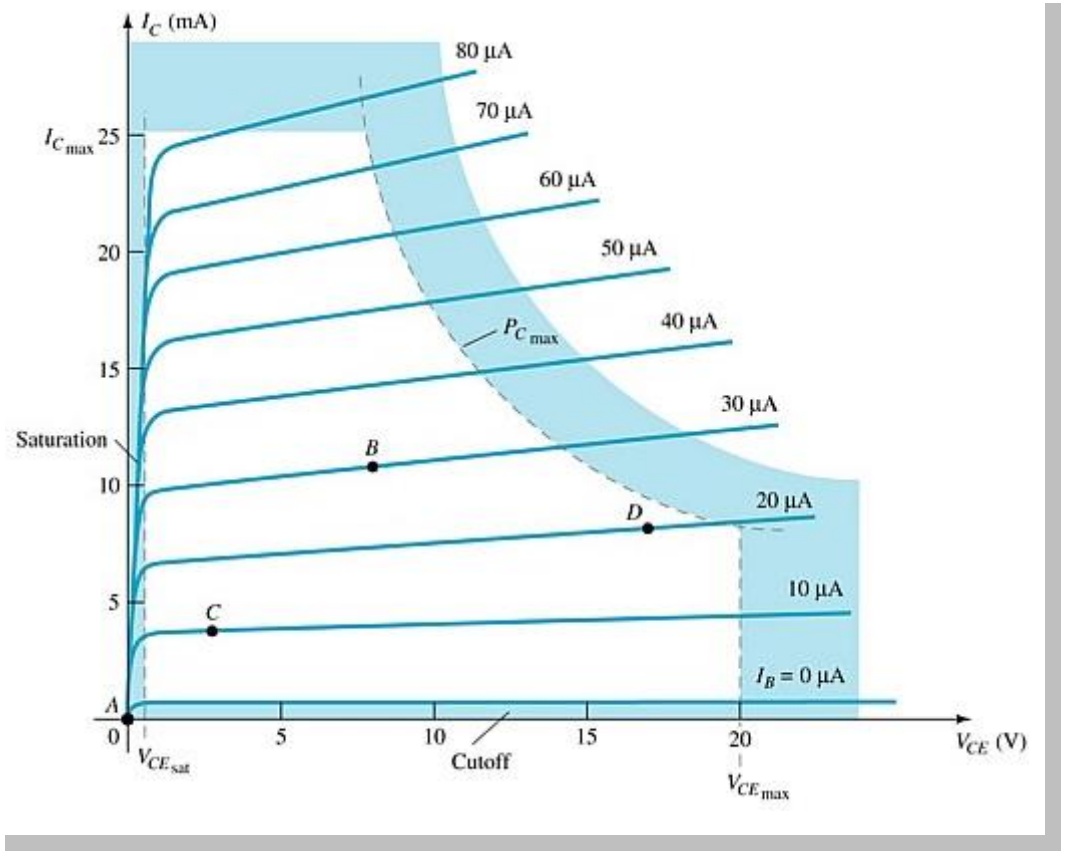
Biasing

Biasing: The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.

OPERATING POINT

The DC input establishes an operating or *quiescent point* called the *Q-point*.



THE THREE STATES OF OPERATION

- **Active or Linear Region Operation** **Base–Emitter junction is forward biased Base–Collector junction is reverse biased**

- **Cutoff Region Operation**

  Base–Emitter junction is reverse biased

- **Saturation Region Operation**

  Base–Emitter junction is forward biased Base–Collector junction is forward biased

No matter what type of configuration a transistor is used in, the basic relationships between the currents are always the same, and the base-to- emitter voltage is the threshold value if the transistor is in the “on” state

$$V_{BE} = 0.7V$$

$$I_E = (\beta + 1)I_B \cong I_C$$

$$I_C = \beta I_B$$

- The operating point defines where the transistor will operate on its characteristics curves under dc conditions.
- For linear (minimum distortion) amplification, the dc operating point should not be too close to the maximum power, voltage, or current rating and should avoid the regions of saturation and cutoff.

DC BIASING CIRCUITS

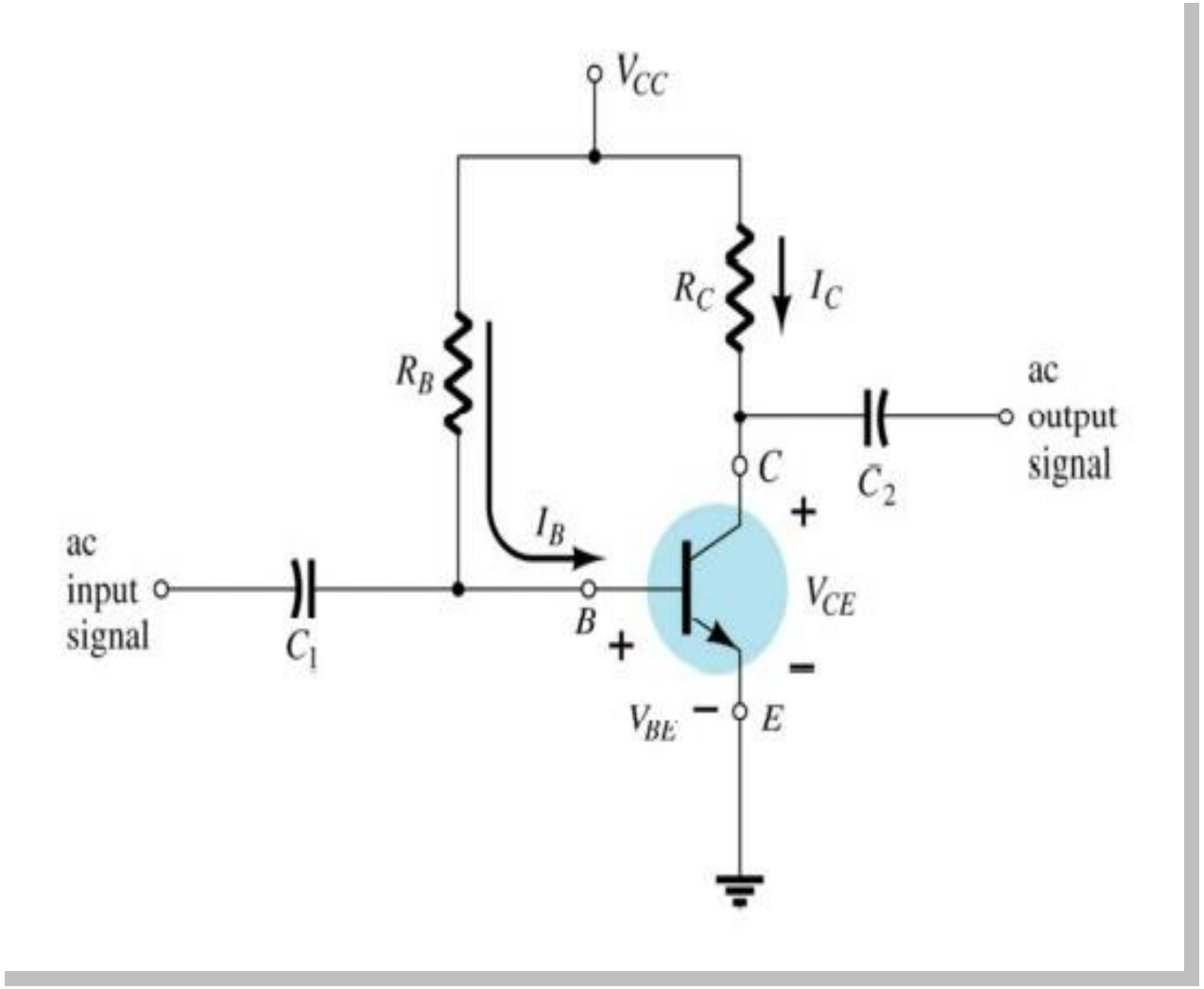
- **Fixed-bias circuit**
- **Emitter-follower bias circuit**
- **Voltage divider bias circuit**

I. FIXED BIAS

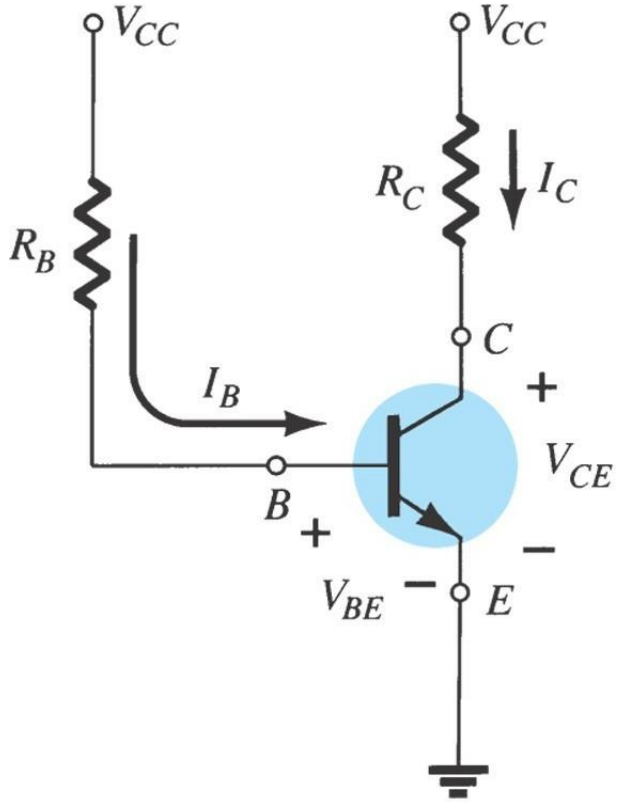
- The fixed-bias configuration is the simplest of transistor biasing arrangements, but it is also quite unstable

- For most configurations the dc analysis begins with a determination of the base current

- For the dc analysis of a transistor network, all capacitors are replaced by an open-circuit equivalent



Fixed-bias circuit



The dc equivalent circuit of the fixed bias circuit where the capacitor is replaced with an open-circuit

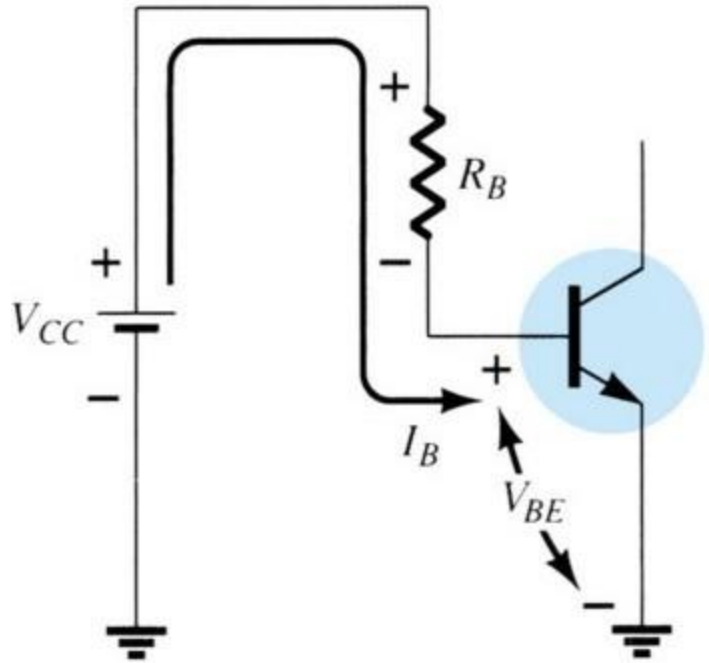
THE BASE-EMITTER LOOP

From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



COLLECTOR-EMITTER LOOP

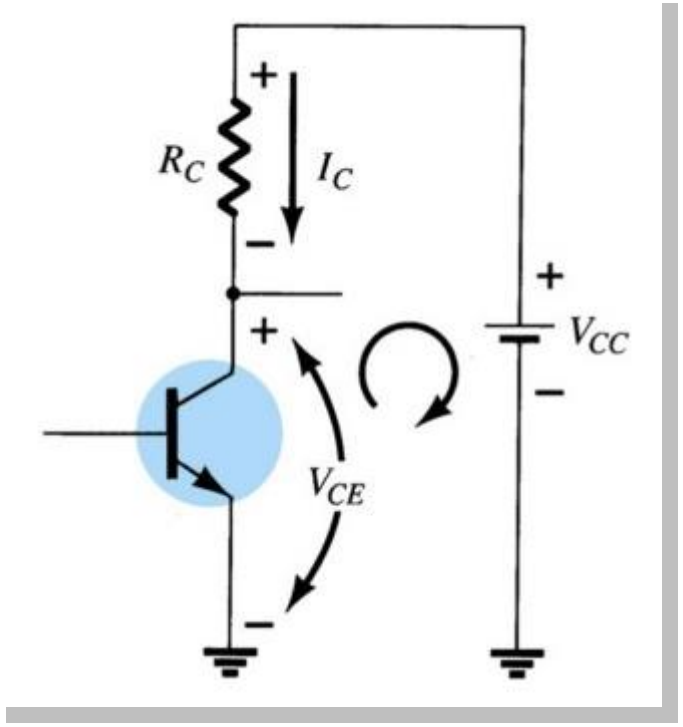
Collector current:

$$\mathbf{I_C = \beta I_B}$$

From Kirchhoff's voltage law:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

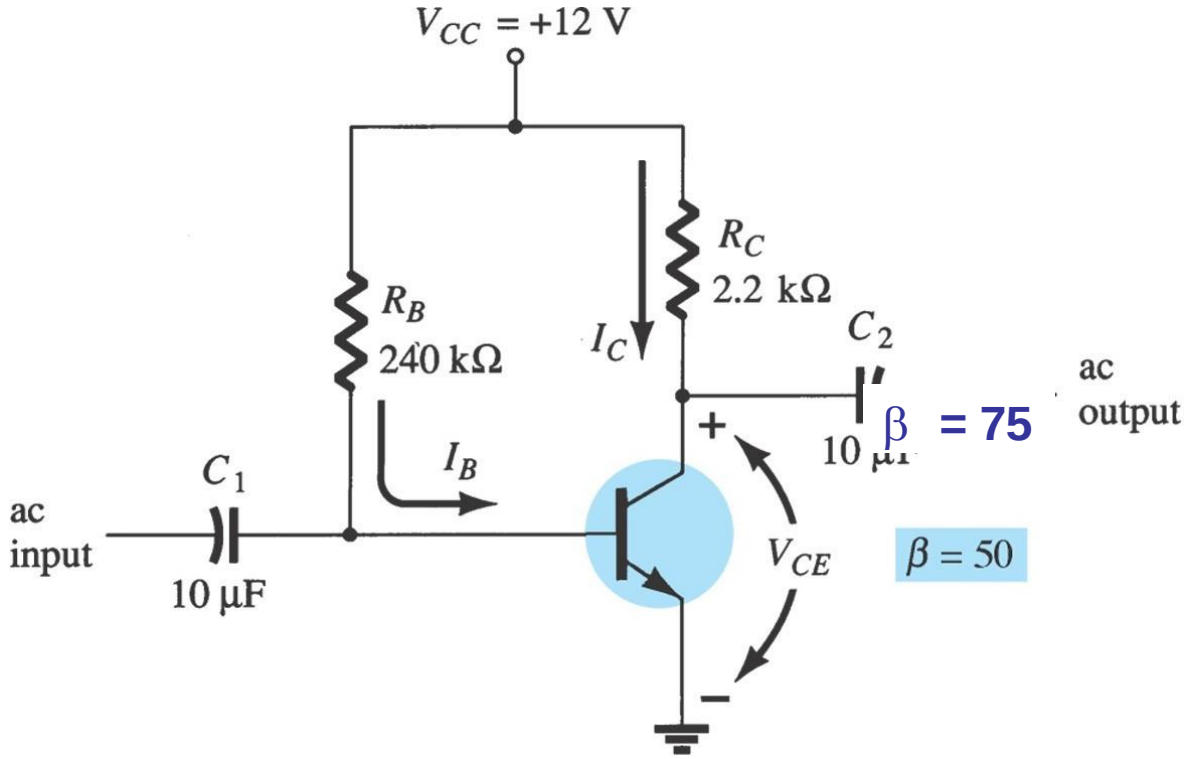
$$\mathbf{V_{CE} = V_{CC} - I_C R_C}$$



EXAMPLE:

Determine the following for the fixed-bias configuration of the figure shown:

(a) I_{BQ} and I_{CQ} (b) V_{CEQ} (c) V_B and V_C (d) V_{BC}



SATURATION

- Saturation conditions are normally avoided because the base-collector junction is no longer reverse – biased and the output amplified will be distorted.

- For a transistor operating in the saturation region, the current is a maximum value for the particular design. Change the design and the corresponding saturation level may rise or drop

- The highest collector current saturation level is defined by the maximum as provided by the specification sheet.

SATURATION

When the transistor is operating in saturation, current through the transistor is at its *maximum* possible value.

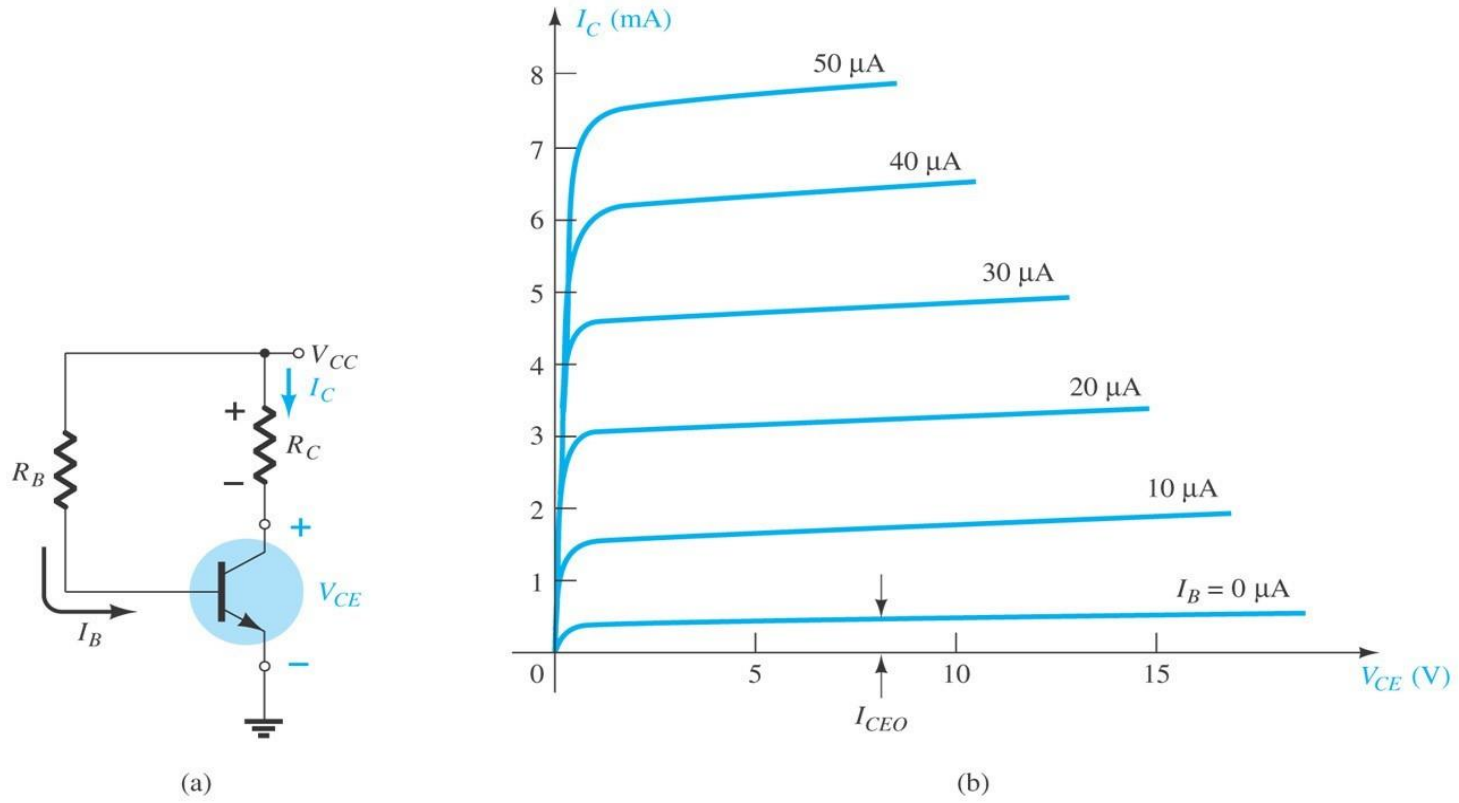
$$I_{C\,sat} = \frac{V_{CC}}{R_C}$$

$$V_{CE} \cong 0\ V$$

In the previous example, the saturation level for the network is given by:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{12V}{2.2k\Omega} = 5.45mA$$

LOAD LINE ANALYSIS



The variables I_C and V_{CE} are related by the equation:

$$V_{CE} = V_{CC} - I_C R_C$$

LOAD LINE ANALYSIS

The end points of the load line are:

I_{Csat}

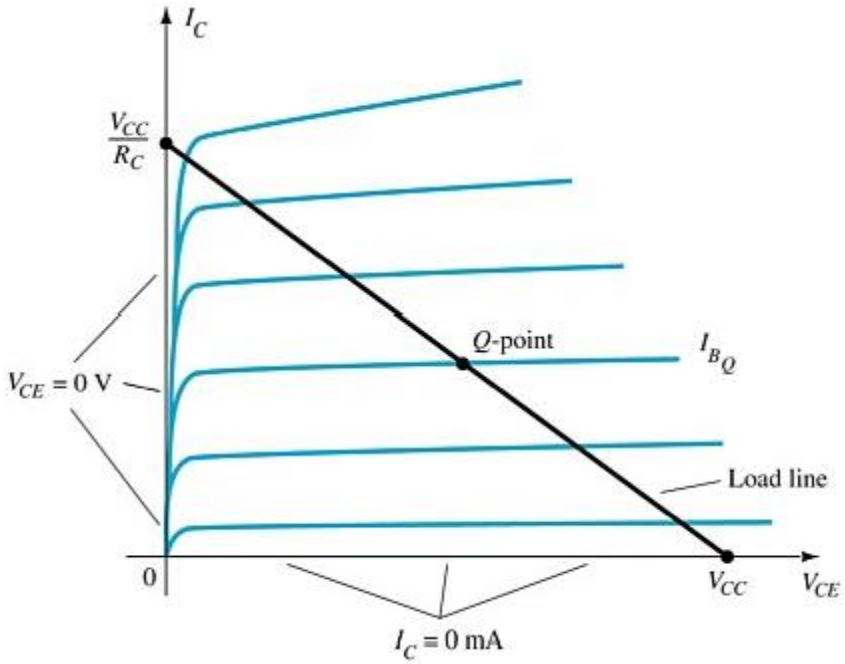
$V_{CE} = 0$ V

$I_C = V_{CC} / R_C$

$V_{CEcutoff}$

$I_C = 0$ mA

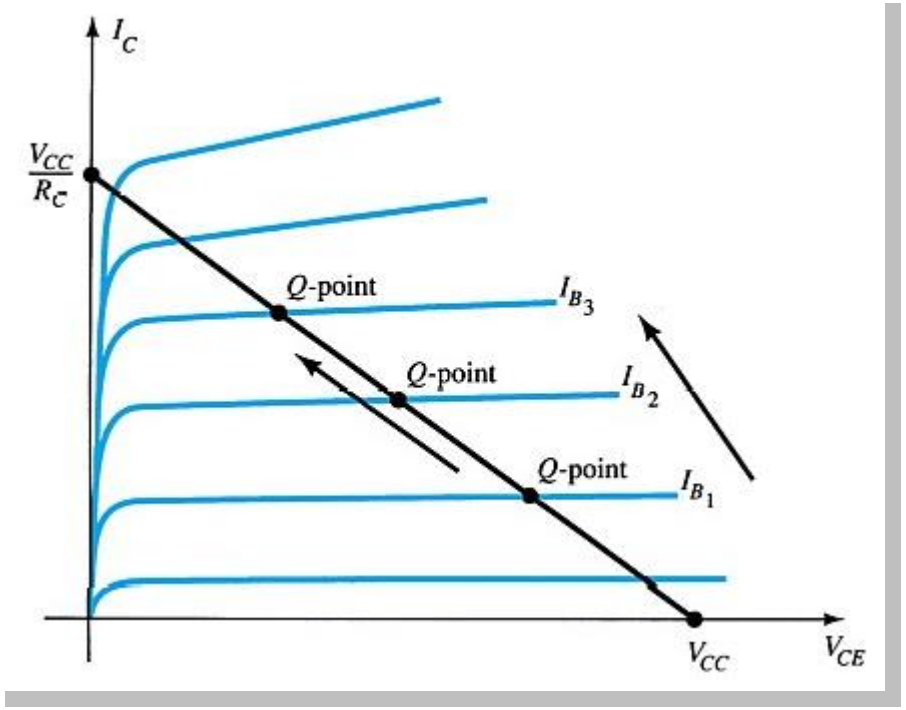
$V_{CE} = V_{CC}$



The *Q*-point is the operating point:

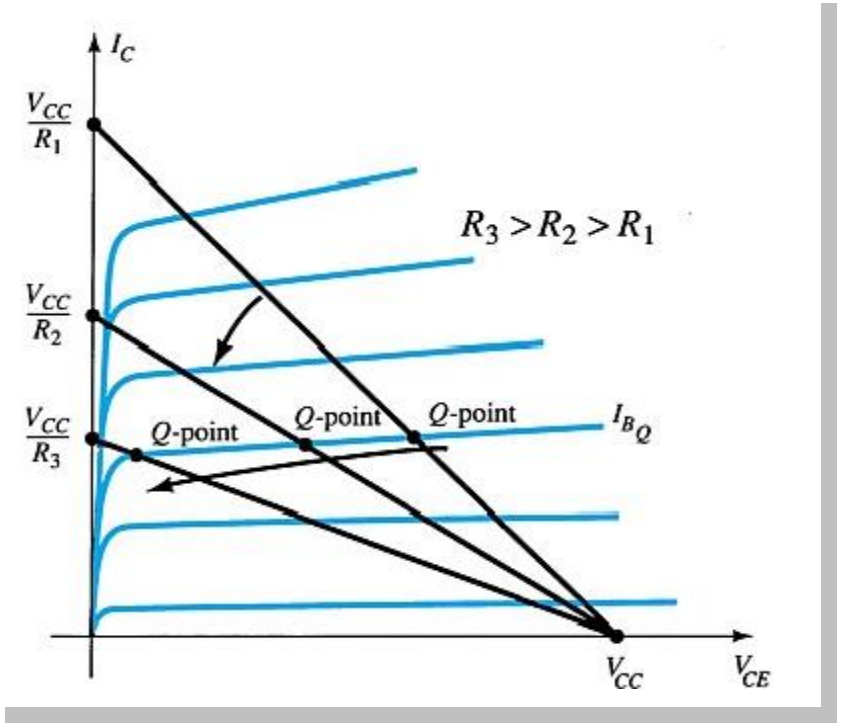
- where the value of R_B sets the value of I_B
- that sets the values of V_{CE} and I_C

CIRCUIT VALUES AFFECT THE Q-POINT



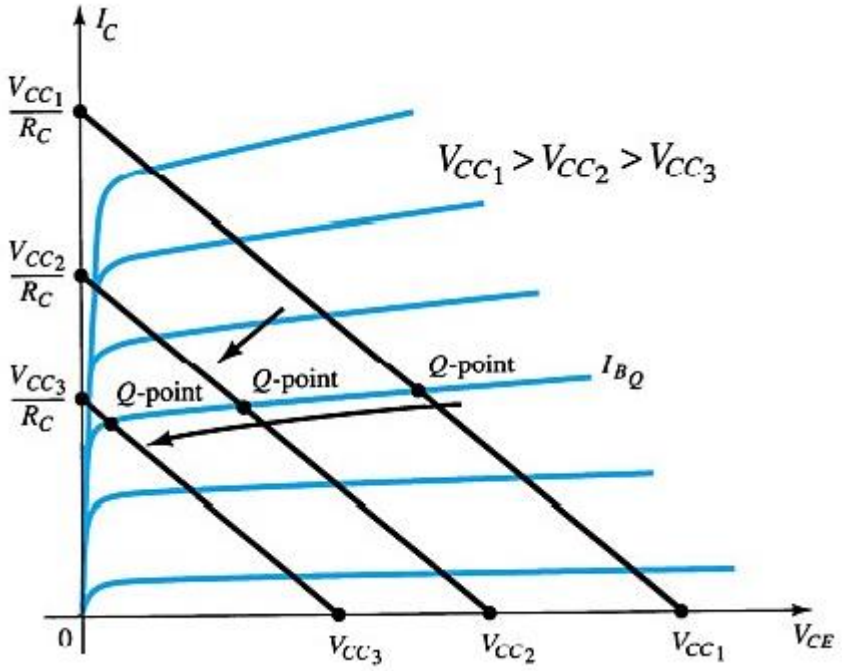
[Movement of the Q-point with increasing level of I_B]

CIRCUIT VALUES AFFECT THE Q-POINT



[Effect of an increasing level of R_C on the load line the *Q*-point]

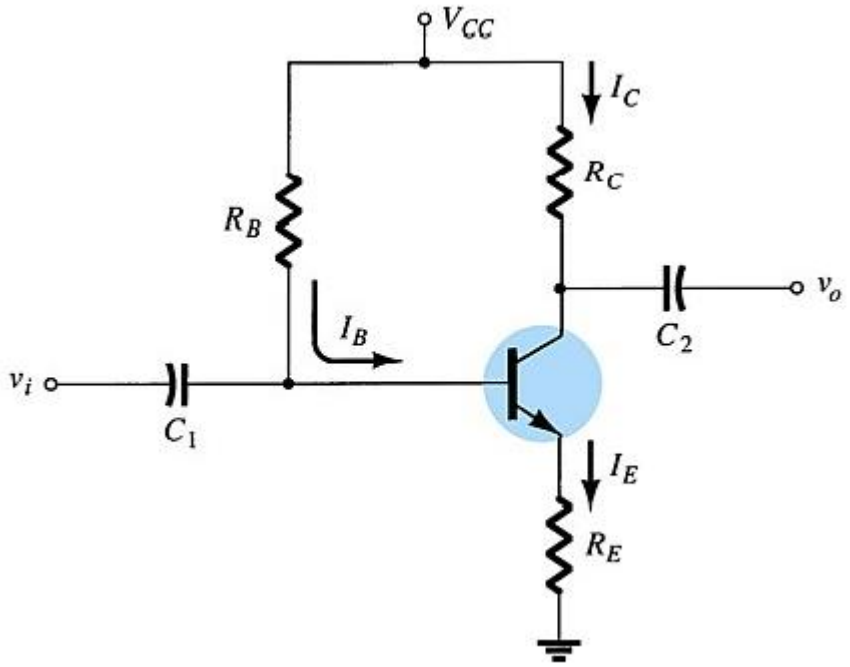
CIRCUIT VALUES AFFECT THE Q-POINT



[Effect of lower values of V_{CC} on the load line the *Q*-point]

II. EMITTER-STABILIZED BIAS CIRCUIT

Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.



BASE-EMITTER LOOP

From Kirchhoff's voltage law:

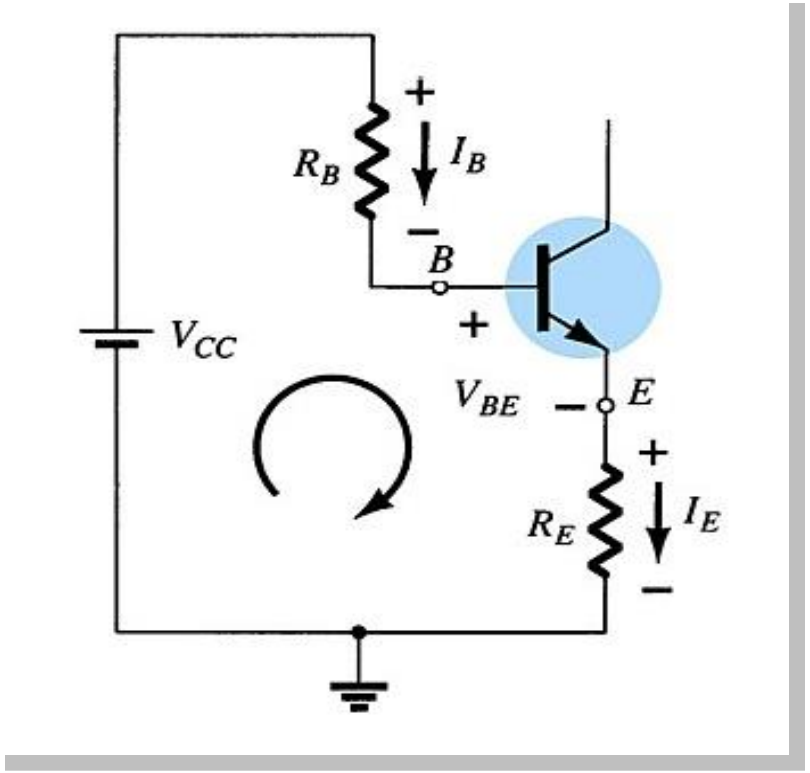
$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$:

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

Solving for I_B:

$$\mathbf{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}}$$



COLLECTOR-EMITTER LOOP

From Kirchhoff's voltage law:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \cong I_C$:

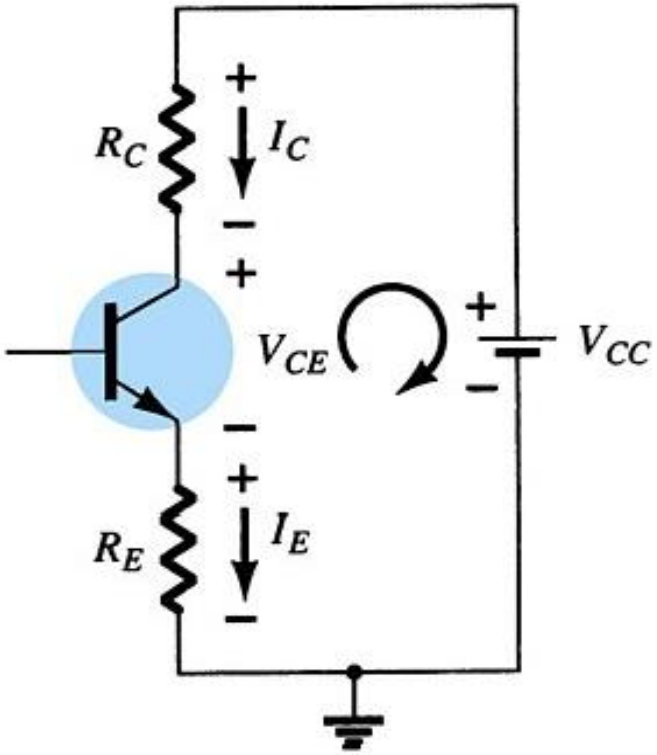
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Also:

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C \quad V_B = V_{CC} -$$

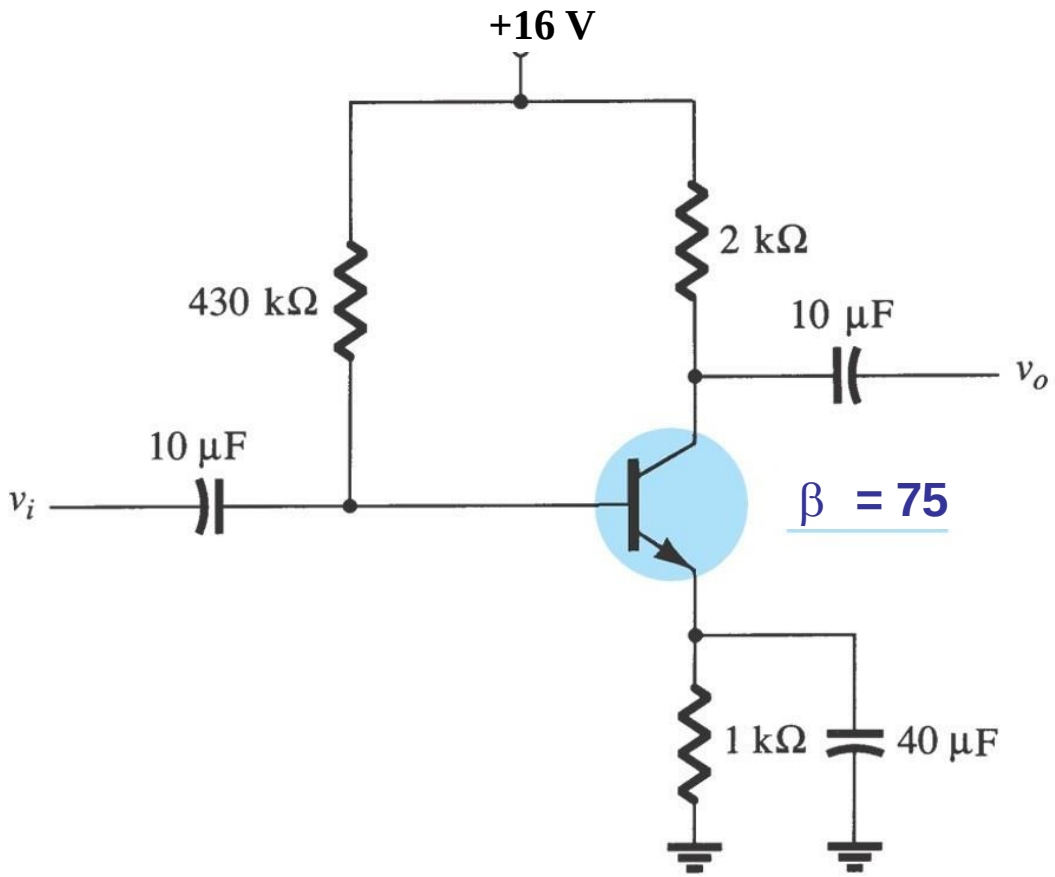
$$I_R R_B = V_{BE} + V_E$$



EXAMPLE:

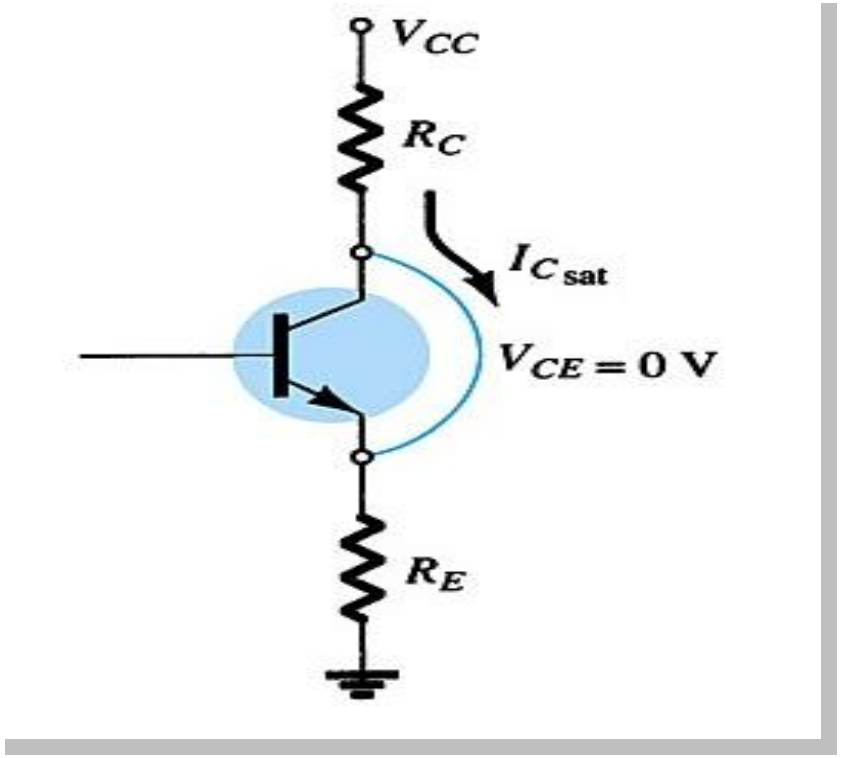
Determine the following for the emitter bias network of the figure shown:

(a) I_B (b) I_C (c) V_{CE} (d) V_C (e) V_E (f) V_B (g) V_{BC}



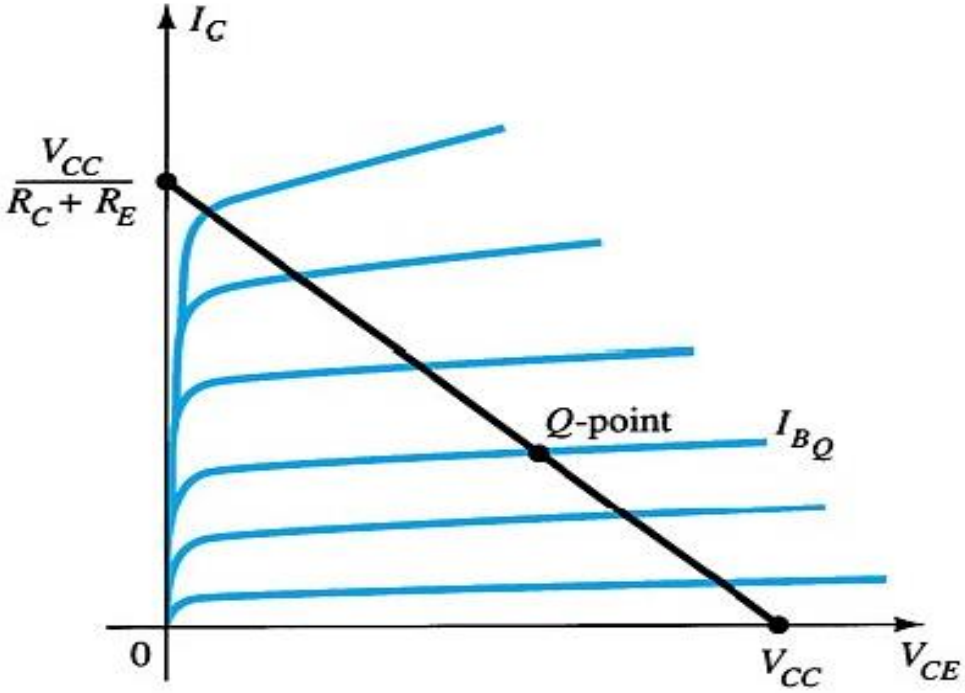
SATURATION LEVEL

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$



LOAD-LINE ANALYSIS

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



The endpoints can be determined from the load line.

$V_{CEcutoff}$:

$V_{CE} = V_{CC}$

$I_C = 0$ mA

I_{Csat}:

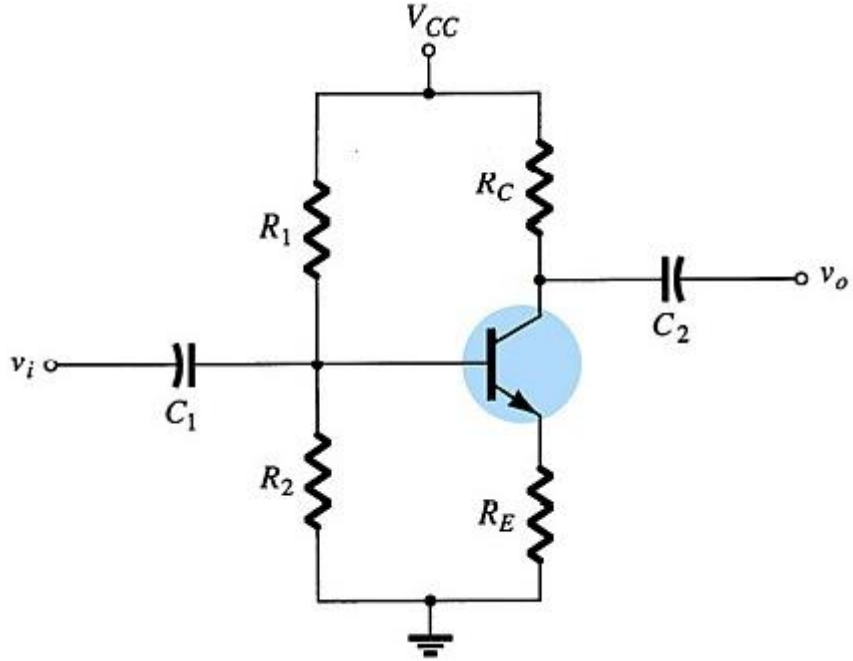
$V_{CE} = 0$ V

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

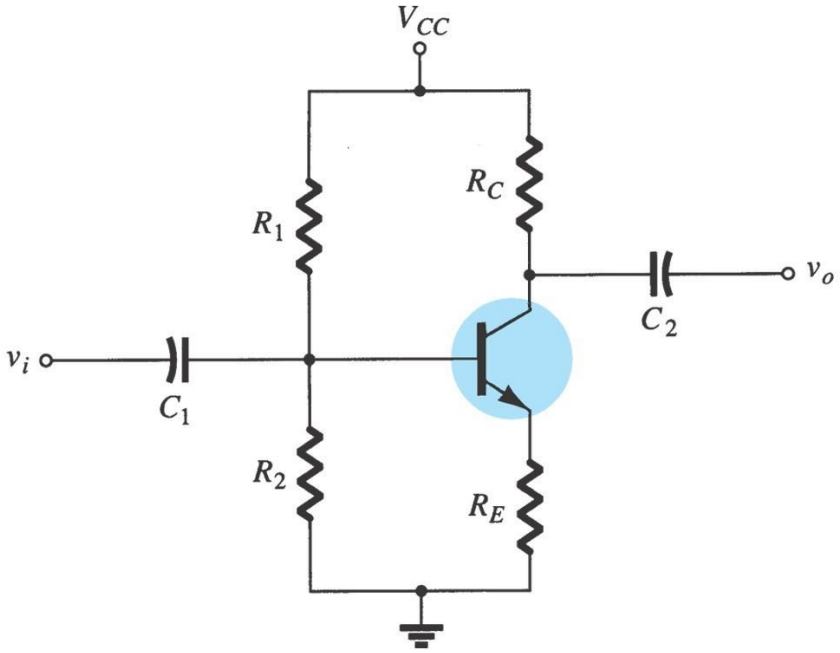
III. VOLTAGE DIVIDER BIAS

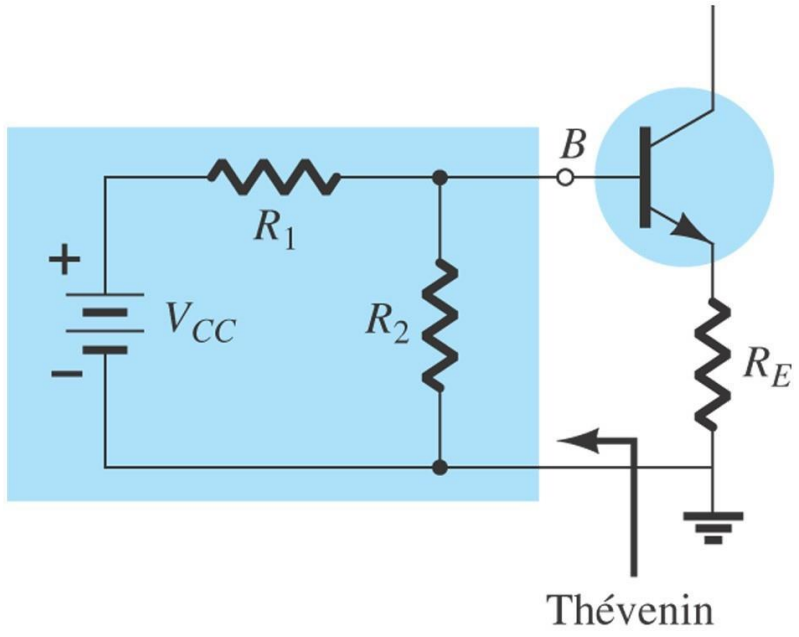
This is a very stable bias circuit.

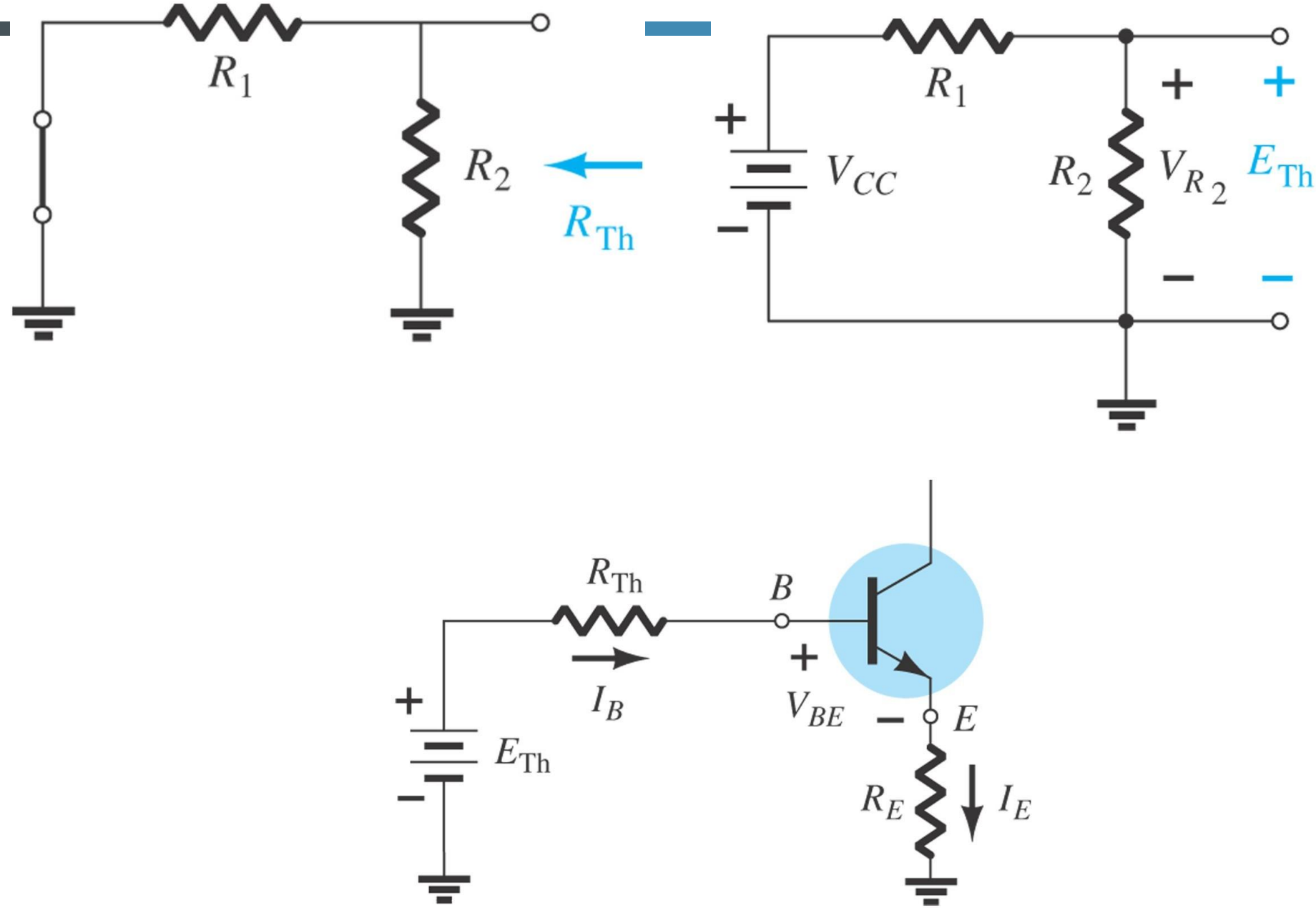
The currents and voltages are nearly independent of any variations in β.



EXACT ANALYSIS:






R_1
R_2
R_{Th}
V_{CC}
R_1
R_2
V_{R_2}
E_{Th}
R_{Th}
B
I_B
V_{BE}
E
E_{Th}
R_E
I_E

$$R_{Th} = R_1 \| R_2 \qquad E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Applying Kirchhoff's voltage law in the clockwise direction in the Thevenin network,

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$ (Substituting $I_E = (\beta+1) I_B$)

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

VOLTAGE DIVIDER BIAS ANALYSIS

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$

$$I_C = 0mA$$

Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0V$$