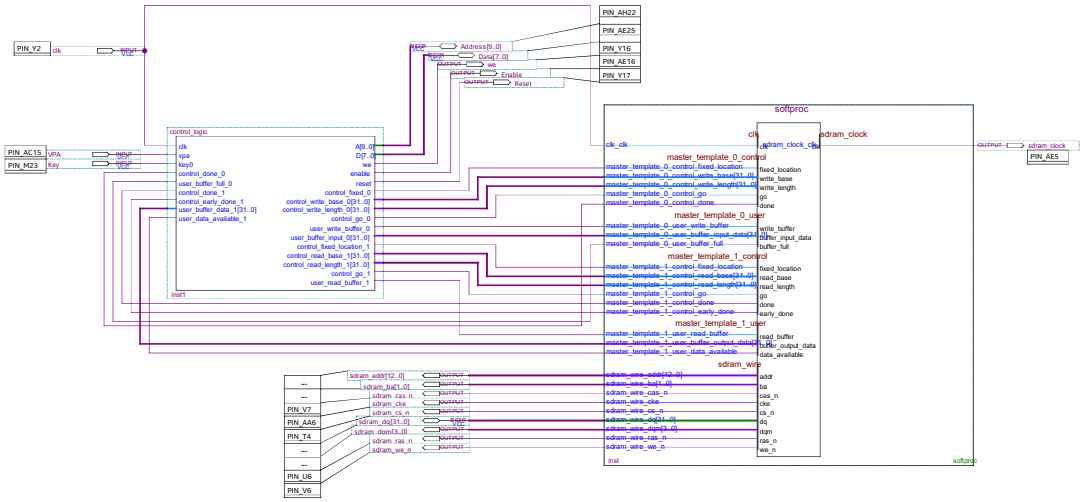
PIN_Y2
clk
PIN_AC15
VPA
PIN_M23
Key
control_logic
clk
vpa
key0
control_done_0
user_buffer_full_0
control_done_1
control_early_done_1
user_buffer_data_1[31..0]
user_data_available_1
A[9..0]
D[7..0]
we
enable
reset
control_fixed_0
control_write_base_0[31..0]
control_write_length_0[31..0]
control_go_0
user_write_buffer_0
user_buffer_input_0[31..0]
control_fixed_location_1
control_read_base_1[31..0]
control_read_length_1[31..0]
control_go_1
user_read_buffer_1
inst1
Address[9..0]
Data[7..0]
we
Enable
Reset
PIN_AH22
PIN_AE25
PIN_Y16
PIN_AE16
PIN_Y17
softproc
clk
clk_clk
sdram_clock_clk
sdram_clock
master_template_0_control
master_template_0_control_fixed_location
master_template_0_control_write_base[31..0]
master_template_0_control_write_length[31..0]
master_template_0_control_go
master_template_0_control_done
master_template_0_user
master_template_0_user_write_buffer
master_template_0_user_buffer_input_data[31..0]
master_template_0_user_buffer_full
master_template_1_control
master_template_1_control_fixed_location
master_template_1_control_read_base[31..0]
master_template_1_control_read_length[31..0]
master_template_1_control_go
master_template_1_control_done
master_template_1_control_early_done
master_template_1_user
master_template_1_user_read_buffer
master_template_1_user_buffer_output_data
master_template_1_user_data_available
sdram_wire
sdram_wire_addr[12..0]
sdram_wire_ba[1..0]
sdram_wire_cas_n
sdram_wire_cke
sdram_wire_cs_n
sdram_wire_dq[31..0]
sdram_wire_dqm[3..0]
sdram_wire_ras_n
sdram_wire_we_n
fixed_location
write_base
write_length
go
done
write_buffer
buffer_input_data
buffer_full
fixed_location
read_base
read_length
go
done
early_done
read_buffer
buffer_output_data
data_available
addr
ba
cas_n
cke
cs_n
dq
dqm
ras_n
we_n
inst
softproc
OUTPUT
sdram_clock
PIN_AE5
sdram_addr[12..0]
sdram_ba[1..0]
sdram_cas_n
sdram_cke
sdram_cs_n
sdram_dq[31..0]
sdram_dqm[3..0]
sdram_ras_n
sdram_we_n
PIN_V7
PIN_AA6
PIN_T4
PIN_U6
PIN_V5