

多重等脉宽调制触发区事件源的配置

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摘要

为了确定特殊TZ事件源,用脉宽输出(PWM)对多触发区(TZ)响应的应用日益受到挑战。

这份应用报告描述的内容是:当多重TZ事件在一个PWM通道出现时,如何配置等脉宽调制 以确认TZ事件源。

在应用报告里讨论的项目源代码都能在: http://www-s.ti.com/sc/techlit/spraar4.zip 下载到。

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1 TZ介绍

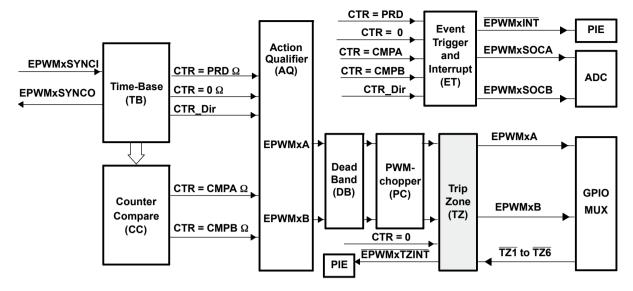


图1.TZ子模块

每个等脉宽调制模块都连接了六个来自通用输入/输出(GPIO) MUX的TZn信号(TZ1到TZ6)。这些信号显示出错误或者触发情况,所以当错误发生时ePWM输出可编程响应。

1.1 触发区子模块的作用

TZ子模块的主要功能:

- 触发输入TZ1到TZ6容易添加到任何一个ePWM模块中
- 在错误情况下,输出EPWMxA和EPWMxB能被强制到一下状态中:

 - 低
 - 高阻抗
 - 不反映
- 在主要的小型电路或者过流环境下支持单出错操作(OSHT)
- 在限流工作情况下支持周期出错操作
- 每个触发区输入脚能定位到单出错操作和周期出错操作
- 在任何一个触发区管脚都能产生中断
- 支持软件受迫出错
- 如果不需要触发区域子模块能被完全旁路

2 多触发区面临的问题

每个ePWM输出(EPWMxA和EPWMxB)都能被任何或者所有六个TZn输入(TZ1到TZ6)获得。由于每一个选定的TZ类型(稳态的或者周期的)只有一个TZ标记,所以如果多重TZ在单个ePWM输出中TZ源不能被确定。一种解决办法就是允许所有的TZ中断。

当所有TZ共享PIE组2,代码能通过读取OIEFR2去确定哪个TZ标记到中断服务列队中。问题是从PIE获取中断指针时,硬件会自动清除PIEIFRx.y位,并且其发生在进入ISR前,所以TZ源标记会丢失。*TMS320x280,2801x,2804x系统控制和中断参考手册列出了硬件中断响应的流程图*。



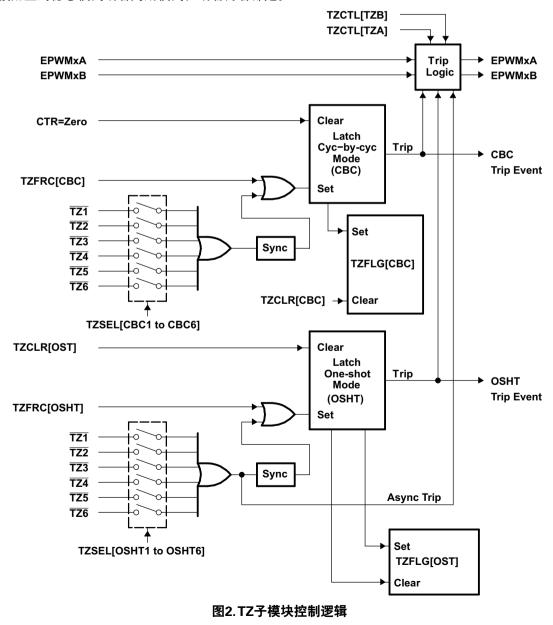
3 确定TZ源

为了在多TZ中配置一个脉宽调制通道到触发状态,允许同样的TZ为了另一个PWM通道分配独立TZ给PWM通道。这让TZFLG位为了其他PWM通道去确定TZ源。在TZCTL寄存器中用户能配置TZ事件而在PWM通道中没有任何动作。这个解决方案避免获取TZ时间时需要扩展电路。

如果扩展获取TZ事件已经准备可用,与TZ管脚共用的GPIO输入能被读取确定逻辑层。例如,TMS320F2808设备,TZI与GPIO12共用一个管脚,TZ2与GPIO13共用一个管脚,等等。类似的例子可以在TMS320F2809, TMS320F2808, TMS320F2806, TMS320F2802, TMS320F2801, TMS320C2802, TMS320C2801和TMS320F2801x DSP的GPIO多路中断图解中看到(SPRS230)。

3.1 为单个ePWM输出开通多触发区

图2是设计在每一个ePWM模块中的TZ控制逻辑图。注意所有六个TZ在两个ePWM通道中都可用。每个TZ能被配置到稳态模式或者周期模式,或者两者都是。



多重等脉宽调制触发区事件源的配置



TZSEL寄存器允许每个TZ对一个单ePWM可用。由于多TZ可用,但CBC或者OSHT触发事件发生,如图3触发时间设置了相对应的TS中断标志,cBC-TZFLG或者OSHT-TZFLG。这些标示能被用来产生一个响应TZ事件的中断。在OSR代码中,一个首要的任务就是确定那个TZ事件引发了中断。

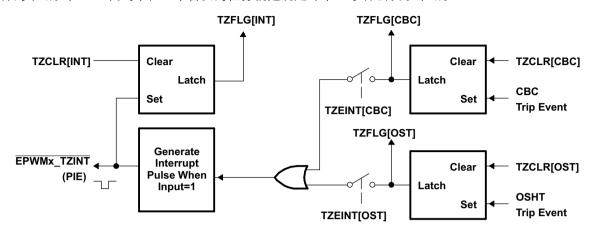


图3.TZ子模块中断逻辑

还有,这个错误事件在选定的ePWM通道中导致一个特定的动作,如表1注意EMPWMxA和EPWMxB已经在他们各自响应错误事件的动作中分开控制。

位	名称	值	描述
15-4	预留		预留
3-2	TZB		当一个触发事件发生,在EPWMxB输出中会发生以下动作,它的TZ管脚能产生的一个在
			TMS320x280x, 2801x, 2804x系统控制和中断参考手册中定义的寄存器动作(SPRU712)。
			高阻抗(WPWMxB=高阻抗状态)
		00	强制EPWMxB到高阻抗状态
		01	强制EPWMxB到低阻抗状态
		10	EPWMxB中没有任何操作
		11	
1-0	TZA		当一个触发事件发生,在EPWMxA输出中会有以下动作。它的TZ管脚能发生一个
			在TMS320x280x, 2801x, 2804x系统控制和中断参考指南中定义的TZSEL寄存器动作
			(SPRU712)。
		00	高阻抗(EPWMxA=高阻抗状态)
		01	强制EPWMxA到高阻抗状态
		10	强制EPWMxA到低阻抗状态
		11	EPWMxA中没有任何操作

表1.Tz控制寄存器区描述

3.2 确定TZ事件源

所面临的问题是当多重TZ事件可用时,确定特定TZ事件引起一个TZ相关中断。没有直接与特定TZ事件相关联的中断。但是,TZ事件和特定的ePWM模块相关联。比如,任何EPWMxA1允许TZ事件都能引起PIEIFR2.1的设置。如果PIEIER2.1被设置了,EPWM1_TZINT中断就会产生。但是中断源可能是任何六个TZn中的一个。



这个方案在附加ePWM模块中的单TZ事件是可用的。

除了配置一个PWM通道到多TZ触发状态外,还为另一个PWM通道允许同一个TZ分配一个单独TZ到PWM通道。这允许为另一个PWM通道检测TZFLG位能确定TZ源。在PWM通道中配置附加TZ事件在TZCTL寄存器中没有任何操作。

3.3 确定TZ事件源

这个例子显示的是如何实现在应用报告总描述的方法。总的来说,TZ的范例软件提供了28x整代或者部分外围代码包。在合格应用报告中,*C280x,C2801xC/C++头文件和外围例子*(SPRC191)都在F2808 eZdsp™中用到。

这些代码修正后允许六个ePWM1的TZn都可用,每个都被设置为在TZ事件发生时EPWM1A输出为高状态。 TZ2-56对EPWMs2-6都可用,由一个TZ对每个ePWM模块都可用和每个TZ配置到在发生TZ事件时没有任何 动作。ePWM1的TZ中断被修正以确定TZ事件源。

3.3.1 软件配置

这个部分讨论当六个TZz事件中任何一个发生时让EPWM1A强制转换到高状态的配置方法。 EPWM_TZINT发生时,检测TZFLG位ePWM1-5以确定TZ事件源。如果没有被设置,TZ6就是源。这个例子能检测TZ事件可配置的最大数目,但是配置可用更少的TZ事件例子也可以使用。

```
void InitEPwm1Example()
  // Enable allTZs as one shot trip sources
  EALLOW:
  EPwm1Regs.TZSEL.bit.OSHT1 = 1;
  EPwm1Regs.TZSEL.bit.OSHT2 = 1;
  EPwm1Regs.TZSEL.bit.OSHT3 = 1;
  EPwm1Regs.TZSEL.bit.OSHT4 = 1;
  EPwm1Regs.TZSEL.bit.OSHT5 = 1;
  EPwm1Regs.TZSEL.bit.OSHT6 = 1;
  // What do we want any of the TZs to do?
  EPwm1Regs.TZCTL.bit.TZA =TZ_FORCE_HI;
  EPwm1Regs.TZCTL.bit.TZB = TZ_NO_CHANGE;
  // EnableTZ interrupt on anyTZ event
  EPwm1Regs.TZEINT.bit.OST = 1;
  EDIS:
void InitEPwm2Example()
  // Enable TZ1 as one shot trip source
  EALLOW:
  EPwm2Regs.TZSEL.bit.OSHT2 = 1;
  // Do not impact PWM outputs on TZ event
  EPwm2Regs.TZCTL.bit.TZA =TZ_NO_CHANGE;
  EPwm2Regs.TZCTL.bit.TZB = TZ_NO_CHANGE;
  EDIS;
}
```

3.3.2 程序

用例子中的软件装载和实时运行在F2808 eZdsp中,增加一个可变EPWM1TZIntCount到可见窗口并不断更新这个窗口。

用示波器连接到F2808 eZdsp的P8连接脚#9的EPWM1A(和GPIO0共用)。注意EPWM1A的输出是激活的。你可以看到PWM 50%的占空比。



连接跳线的一段到位于p8-39的地,跳线的另一端连接到位于p8-37的TZ1(与GPIO12共用)。注意 EPWM1A的输出现在被强制到高电位,还有在观测窗口的EPwm1TZIntCount数值不断增长,这表示 ePWM1中断已经在TZ1被激活时开始工作。

现在对剩下的TZ进行重复测试

- 1. 用跳线连接P8-9到P8-17和TZ2(与GPIO13共享)
- 2. 用跳线连接P8-9到P8-5和TZ3(与GPIO14共享)
- 3. 用跳线连接P8-9到P8-22和TZ4 (与GPIO15共享)
- 4. 用跳线连接P8-9到P8-23和TZ5 (与GPIO16共享)
- 5. 用跳线连接P8-9到P8-24和TZ6 (与GPIO17共享)

这些测试用户都会看到epwm1a的输出都被强制到高位还有EPwm1TZIntCount的数值继续增加。

表2.T2808 eZdsp P8连接器

P8 Pin #	P8 Signal	P8 Pin #	
1	+ 3.3 V/+5 V /NC	2	+ 3.3 V/+5 V /NC
3	MUX_GPIO29	4	MUX_GPIO28
5	GPIO14	6	GPIO20
7	GPIO21	8	GPIO23
9	GPIO0	10	GPIO1
11	GPIO2	12	GPIO13
13	GPIO4	14	GPIO15
15	GPIO27	16	GPIO16
17	GPIO13	18	GPIO134
19	GND	20	GND
21	GPIO7	22	GPIO15
23	GPIO16	24	GPIO17
25	GPIO18	26	GPIO19
27	MUX_GPIO31	28	MUX_GPIO30
29	MUX_GPIO11	30	MUX_GPIO8
31	GPIO22/GPIO24	32	MUX_GPIO10
33	GPIO25	34	GPIO25
35	GPIO26	36	GPIO32
37	GPIO12	38	GPIO33
39	GND	40	GND



GPAMUX1/2 ⁽¹⁾ Register Bits	Default at Reset Primary I/O Function (GPxMUX1/2 bits = 0,0)	Peripheral Selection 1 ⁽²⁾ (GPxMUX1/2 bits = 0,1)	Peripheral Selection 2 (GPxMUX1/2 bits = 1,0)	Peripheral Selection 3 (GPxMUX1/2 bits = 1,1)
		GPAMUX	(1	
1-0	GPIO0	EPWM1A (O)	Reserved ⁽³⁾	Reserved ⁽³⁾
3-2	GPIO1	EPWM1B (O)	SPISIMOD (I/O)	Reserved ⁽³⁾
5-4	GPIO2	EPWM2A (O)	Reserved ⁽³⁾	Reserved ⁽³⁾
7-6	GPIO3	EPWM2B (O)	SPISOMID (I/O)	Reserved ⁽³⁾
9-8	GPIO4	EPWM3A (O)	Reserved ⁽³⁾	Reserved ⁽³⁾
11-10	GPIO5	EPWM3B (O)	SPICLKD (I/O)	ECAP1 (I/O)
13-12	GPIO6	EPWM4A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
15-14	GPI07	EPWM4B (O)	SPISTED (I/O)	ECAP2 (I/O)
17-16	GPIO8	EPWM5A (O)	CANTXB (O)	ADCSOCAO (O)
19-18	GPIO9	EPWM5B (O)	SCITXDB (O)	ECAP3 (I/O)
21-20	GPIO10	EPWM6A (O)	CANRXB (I)	ADCSOCBO (O)
23-22	GPIO11	EPWM6B (O)	SCIRXDB (I)	ECAP4 (I/O)
25-24	GPIO12	TZ1 (I)	CANTXB (O)	SPISIMOB (I/O)
27-26	GPIO13	TZ2 (I)	CANRXB (I)	SPISOMIB (I/O)
29-28	GPIO14	TZ3 (I)	SCITXDB (O)	SPICLKB (I/O)
31-30	GPIO15	TZ4 (I)	SCIRXDB (I)	SPISTEB (I/O)
		GPAMUX	2	
1-0	GPIO16	SPISIMOA (I/O)	CANTXB (O)	TZ5 (I)
3-2	GPIO17	SPISOMIA (I/O)	CANRXB (I)	TZ6 (I)

⁽¹⁾ The word *Reserved* means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should it be selected, the state of the pin is undefined and the pin may be driven. This selection is a reserved configuration for future expansion.

4 结论

这个应用报告显示出对单PWM通道使用多TZ技术能检测出特定的TZ源。

5 参考

- TMS320x28xx, 28xxx 增强脉冲宽度调制(ePWM) 模块参考手册 (SPRU791)
- TMS320x280x, 2801x, 2804x 系统控制和中断参考手册(SPRU712)
- TMS320F2809, TMS320F2808, TMS320F2806, TMS320F2802, TMS320F2801, TMS320C2802, TMS320C2801, and TMS320F2801x DSPs 数据手册(SPRS230)
- C280x, C2801x C/C++ 头文件外围范例(SPRC191)
- eZdsp 2808 技术参考(http://c2000.spectrumdigital.com/ezf2808/docs/2808_ezdspusb_techref_c.pdf)

⁽²⁾ GPXMUX1/2 refers to the appropriate MUX register for the pin, GPAMUX1, GPAMUX2 or GPBMUX1.

⁽³⁾ This table pertains to the F2808 device. Some peripherals may not be available in the 2809, 2806, 2802, or 2801 devices. For more details, see the pin descriptions.

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