TMS320F28x DSP External Interface (XINTF) Reference Guide

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External Interface (XINTF)

The external interface (XINTF) is a nonmultiplexed asynchronous bus, similar to the C240x external interface.

1 Functional Description

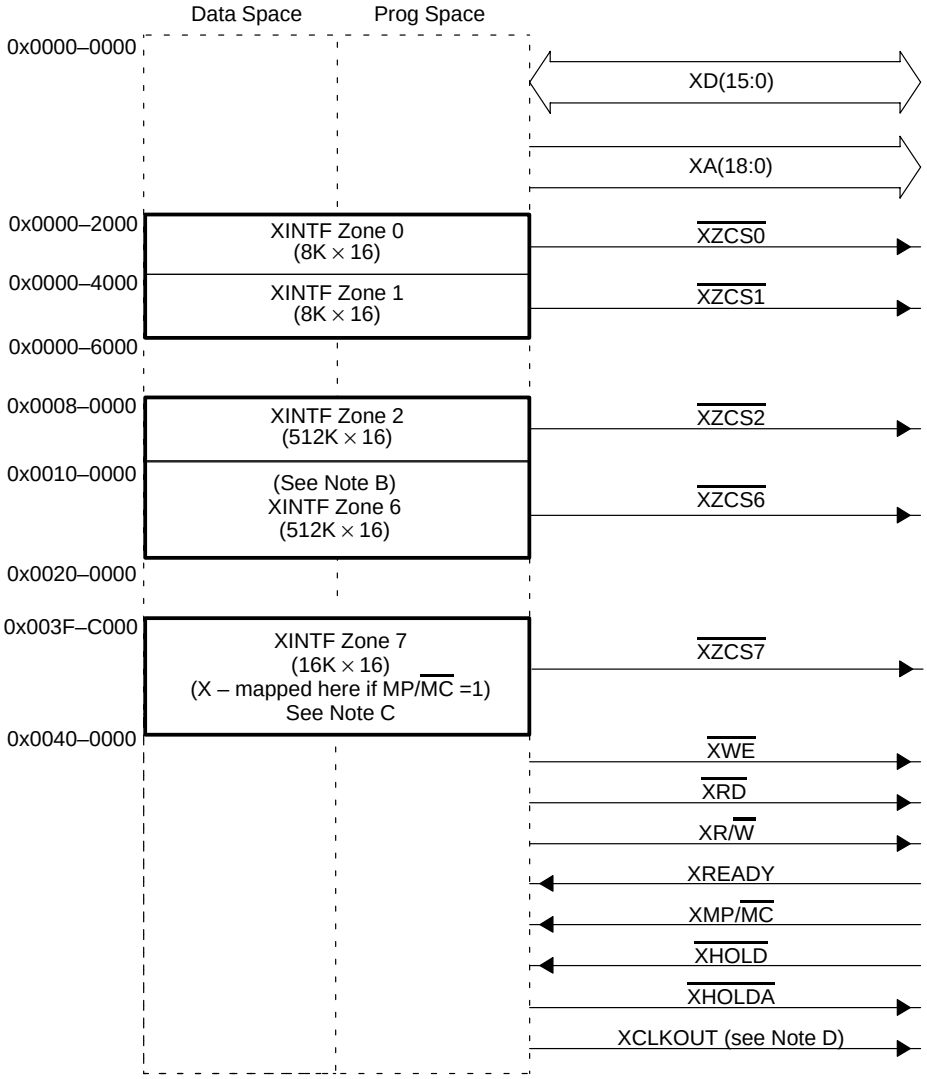
The XINTF on the TMS320F2812 is mapped into five fixed memory-mapped zones as defined in Figure 1.

Each of the 28x XINTF zones has a chip-select signal that is toggled when an access is made to that particular zone. On some devices the chip-select signals for two zones may be internally ANDed together to form a single shared chip select. In this manner, the same memory is connected to both zones or external decode logic can be used to separate the two.

Each of the five zones can also be programmed with a specified number of wait states, strobe signal set-up and hold timing. The number of wait states, set-up and hold timing is separately specified for a read access and a write access. In addition, each zone can be programmed for extending wait states externally using the XREADY signal or not. The programmable wait-state, chip-select and programmable strobe timing enables glueless interface to external memories and peripherals.

You specify the set-up/hold and access wait states for each XINTF zone by configuring the associated XTIMINGx registers. The access timing is based on an internal clock called XTIMCLK. XTIMCLK can be set to the same rate as the SYSCLKOUT or to one-half of SYSCLKOUT. The rate of XTIMCLK applies to all of the XINTF Zones. XINTF bus cycles begin on the rising edge of XCLKOUT and all timings and events are generated with respect to the rising edge of XTIMCLK.

Figure 1. External Interface Block Diagram (See Note A)



NOTES: A. Each zone can be programmed with different wait states, setup and hold timings, and is supported by zone chip selects (XZCS0AND1, XZCS2, XZCS6AND7), which toggle when an access to a particular zone is performed. These features enable glueless connection to many external memories and peripherals.

B. Zones 3 – 5 are reserved for future expansion.

C. The mapping of XINTF Zone 7 is dependent on the XMP/MC device input signal and the MP/MC mode bit (bit 8 of XINTCNF2 register). Zones 0, 1, 2, and 6 are always enabled.

D. XCLKOUT is also pinned out on the devices without the rest of the XINTF.

2 XINTF Configuration Overview

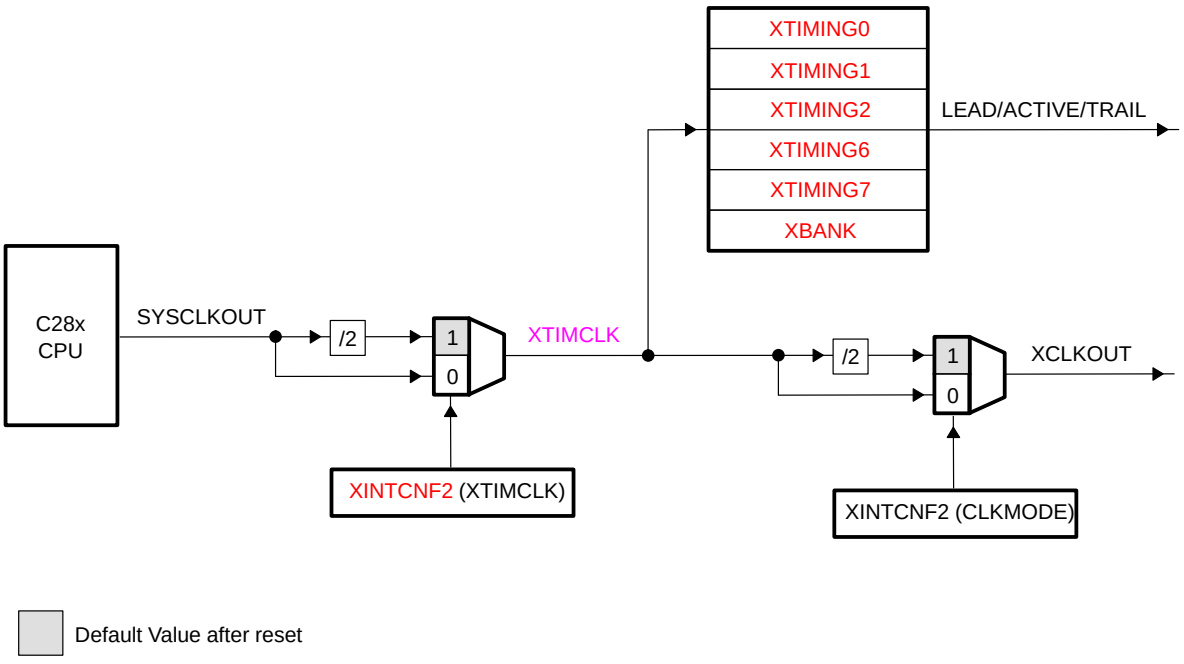
The following gives an overview of the various XINTF parameters that can be configured to fit particular system requirements. The exact configuration used depend on the operating frequency of the 28x device, switching characteristics of the XINTF, and the timing requirements of the external devices to which it is being interfaced. Detailed information on each of these parameters is given in the following sections.

Because a change to many of the XINTF configuration parameters will cause a change to the access timing, code that configures these parameters should not execute from the XINTF itself.

2.1 XINTF Clocking

There are two clocks used by the XINTF module. Figure 2 shows the relationship between these two clocks and the CPU clock, SYSCLKOUT.

Figure 2. Relationship Between XTIMCLK and SYSCLKOUT



2.1.1 Internal XINTF clock, XTIMCLK.

All accesses to all of the XINTF zones are based on the frequency of this clock. When configuring the XINTF, you need to determine the ratio required for the

internal XINTF clock, XTIMCLK, with respect to SYSCLKOUT. XTIMCLK can be configured to be either equal or ½ of SYCLKOUT by writing to the XTIMCLK bit in the XINTFCNF2 register.

By default XTIMCLK is one-half of SYSCLKOUT.

2.1.2 External clock out, XCLKOUT.

All XINTF accesses begin on the rising edge of XCLKOUT. In addition, external logic may be clocked off of XCLKOUT. The frequency of XCLKOUT can be configured as a ratio of the internal XINTF clock, XTIMCLK. XCLKOUT can be configured to be either equal or one-half of XTIMCLK by writing to the CLKMODE bit in the XINTFCNF2 register.

By default XTIMCLK is one-half of XTIMCLK, which in turn is one-fourth of the CPU clock, SYSCLKOUT.

2.2 Write Buffering

By default write access buffering is disabled. In most cases, to improve performance of the XINTF, you should enable write buffering. Up to three writes to the XINTF can be buffered without stalling the CPU. The write buffer depth is configured in the XINTCNF2 register.

2.3 XINTF access lead/active/trail wait state timing per zone.

An XINTF zone is a region of memory-mapped addresses that directly access the external interface. Any read or write access to an XINTF zone can be divided into the following three portions: Lead, Active, and Trail. The number of XTIMCLK cycle wait states for each portion of an access can be configured for each XINTF zone in the corresponding zone XTIMING register. Timing for read accesses can be configured separately from timing for write accesses. In addition, to facilitate connections to slow external devices the X2TIMING bit can be used to double the specified lead/active and trail wait states for a particular zone.

2.3.1 Lead period

During the lead portion, the chip-select signal for the zone being accessed is taken low and the address is placed on the address bus (XA). The total lead period, in XTIMCLK cycles can be configured in the zone's XTIMING register. By default, the lead period is set to the maximum six XTIMCLK cycles for both read and write accesses.

2.3.2 Active period

During the active period, the access to the external device is made. For a read access, the read strobe (XRD) is brought low and data is latched into the DSP.

For a write access, the write enable (XWE) strobe is brought low and data is placed on the data bus (XD). If the zone is configured to sample the XREADY signal, the external device can control the XREADY signal to further extend the active period beyond the programmed wait states.

The total active period for any access that does not sample XREADY is 1 XTIMCLK cycle plus the number wait states specified in the corresponding XTIMING register. By default, the active wait states are set to the 14 XTIMCLK cycles for both read and write accesses.

2.3.3 Trail period

The trail period serves as a hold time in which the chip-select signal remains low but the read and write strobes are brought back high. The total trail period, in XTIMCLK cycles can be configured in the zone's XTIMING register. By default the lead period is set to the maximum six XTIMCLK cycles for both read and write accesses.

Based on system requirements, the lead, active and trail wait state values can be configured to best fit the devices connected to a particular XINTF zone. The following should be considered when selecting the timing parameters:

- ❏ Minimum wait state requirements as described in section 3
- ❏ The timing characteristics of the XINTF, as described in the device data sheet
- ❏ The timing requirements of the external device
- ❏ Any additional delays between the 28x device and the external device

2.4 XREADY sampling for each zone.

By sampling XREADY, the external device can extend the active portion of the access. All of the XINTF zones on a device share the same XREADY input signal but each XINTF zone can individually be configured to either sample or ignore the XREADY signal. In addition, the sampling can be specified as synchronous or asynchronous for each zone.

- ❏ Synchronous sampling:

  If XREADY is sampled synchronously, then the XREADY signal must meet set-up and hold timing relative to one XTIMCLK edge before the end of the active period. That is, XREADY will be sampled one XTIMCLK cycle before the total lead + active cycles specified for the access

- ❏ Asynchronous sampling:

  If XREADY is sampled asynchronously, then the XREADY signal must meet set-up and hold timing relative to three XTIMCLK cycles before the

end of the active period. That is, XREADY will be sampled three XTIMCLK cycles before the total lead + active cycles specified for the access.

In both the synchronous and asynchronous case if the XREADY sample is found to be low, the active portion of the cycle is extended by one XTIMCLK cycle and XREADY is sampled again during the next XTIMCLK cycle. This pattern continues until XREADY is sampled high at which time the access will complete normally.

If a zone is configured to sample XREADY, then it is done so for both read and write accesses to that zone. By default each XINTF zone is configured to sample XREADY in the asynchronous mode. When using the XREADY signal the system designer should consider:

- Minimum XINTF wait state requirements as described in section 3. The minimum requirements are different when sampling XREADY in the synchronous mode vs the asynchronous mode.
- The timing characteristics of the XINTF, as described in the device data sheet
- The timing requirements of the external device
- Any additional delays between the 28x device and the external device

2.5 Bank switching.

When jumping from one XINTF zone to another XINTF zone, a slow device may require extra cycles in order to release the bus in time for another device to gain access. Bank switching allows you to specify a particular zone for which extra cycles will be added for any access that crosses into or out of the specified zone. The zone and number of cycles is configured in the XBANK register.

2.6 Effects of the XMP/$\overline{\text{MC}}$ signal on the XINTF

At reset the value of the XMP/$\overline{\text{MC}}$ pin is sampled and latched into the XINTF configuration register XINTFCNF2. The state of this pin at reset determines whether the boot ROM or XINTF zone 7 is enabled.

If, at reset, XMP/$\overline{\text{MC}}$ = 1 (microprocessor mode) then zone 7 is enabled and the reset vector is fetched from external memory. In this case you must be certain that the reset vector points to a valid memory location for code execution.

If, at reset, XMP/$\overline{\text{MC}}$ = 0 (microcomputer mode) then the boot ROM is enabled and XINTF zone 7 is disabled. In this case the reset vector is fetched from the internal boot ROM and XINTF zone 7 cannot be accessed.

After reset, the MP/$\overline{MC}$ mode can be changed by writing to the status bit in the XINTFCNF2 register. In this manner, a system can boot through the boot ROM and later software can set MP/MC to 1 to access zone 7.

3 Configuring Lead, Active, and Trail Wait States

XINTF signal timing can be tuned to match specific external device requirements such as setup and hold times for both read and write accesses. The timing parameters can be configured individually for each XINTF zone in the XTIMING registers. Each zone can also be configured to either ignore the XREADY signal or sample it. This allows you to maximize the efficiency of the XINTF based on the memory or peripheral being accessed.

Table 1 shows the relationship between the parameters that can be configured in the XTIMING registers and the duration of the pulse in terms of XTIMCLK cycles, tc(XTIM).

Table 1. Pulse Duration in Terms of XTIMCLK Cycles

Description		Duration (ns)	
		X2TIMING = 0	X2TIMING = 1
LR	Lead period, read access	XRDLEAD x tc(xtim)	(XRDLEADx2) x tc(xtim)
AR	Active period, read access	(XRDACTIVE+WS+1) x tc(xtim)	(XRDACTIVEx2+WS+1) x tc(xtim)
TR	Trail period, read access	XRDTRAIL x tc(xtim)	(XRDTRAILx2) x tc(xtim)
LW	Lead period, write access	XWRLEAD x tc(xtim)	(XWRLEADx2) x tc(xtim)
AW	Active period, write access	(XWRACTIVE+WS+1) x tc(xtim)	(XWRACTIVEx2+WS+1) x tc(xtim)
TW	Trail period, write access	XWRTRAIL x tc(xtim)	(XWRTRAILx2) x tc(xtim)

Notes: 1) tc(xtim) - Cycle time, XTIMCLK

2) WS refers to the number of wait states inserted by hardware when using XREADY. If the zone is configured to ignore XREADY (USEREADY= 0) then WS = 0.

Minimum wait-state configurations must be used for each zone's XTIMING register. These wait-state requirements are in addition to any timing requirements as specified by the device to which it is interfaced. For information on requirements for a particular device, see the data sheet for that device.

No internal device hardware is included to detect illegal settings.

If the XREADY signal is ignored (USEREADY = 0), then the following requirements must be met:

```
1. Lead:        LR >= tc(xtim)
                LW >= tc(xtim)
```

These requirements result in the following XTIMING register configuration restrictions:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Valid	≥ 1	≥ 0	≥ 0	≥ 1	≥ 0	≥0	0, 1

Examples of valid and invalid timings when not sampling XREADY:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid	0	0	0	0	0	0	0, 1
Valid	1	0	0	1	0	0	0, 1
Valid	≥ 1	≥ 0	≥0	≥ 1	≥ 0	≥0	0, 1

If the XREADY signal is sampled in the synchronous mode (USEREADY = 1,

READYMODE = 0), then the following requirements must be met:

```
1. Lead:        LR >= tc(xtim)
                LW >= tc(xtim)

2. Active:      AR >= 2 x tc(xtim)
                AW >= 2 x tc(xtim)
```

These requirements result in the following XTIMING register configuration restrictions:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Valid	≥ 1	≥ 1	≥0	≥ 1	≥1	≥0	0, 1

Examples of valid and invalid timings when using synchronous XREADY:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid	0	0	0	0	0	0	0, 1
Invalid	1	0	0	1	0	0	0, 1
Valid	1	1	0	1	1	0	0, 1

If the XREADY signal is sampled in asynchronous mode (USEREADY = 1, READYMODE = 1) , then the following requirements must be met:

```
3. Lead:        LR >= tc(xtim)
                LW >= tc(xtim)

4. Active:      AR >= 2 x tc(xtim)
                AW >= 2 x tc(xtim)

5. Lead+Active: LR+AR >= 4 x tc(xtim)
                LW+AW >= 4 x tc(xtim)
```

These requirements result in the following three possible XTIMING register configurations:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Valid	≥ 1	≥ 2	0	≥ 1	≥ 2	0	0, 1
Valid	≥ 2	≥ 1	0	≥ 2	≥ 1	0	0, 1
Valid	≥ 1	≥ 1	0	≥ 1	≥ 1	0	1

Examples of valid and invalid timings when using asynchronous XREADY:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid	0	0	0	0	0	0	0, 1
Invalid	1	0	0	1	0	0	0, 1
Invalid	1	1	0	1	1	0	0
Valid	1	1	0	1	1	0	1
Valid	1	2	0	1	2	0	0, 1
Valid	2	1	0	2	1	0	0, 1

Table 2 and Table 3 show the relationship between Lead/Active/Trail values and the XTIMCLK/X2TIMING modes.

Table 2. Relationship Between Lead/Trail Values and the XTIMCLK/X2TIMING Modes

Trail Value	XTIMCLK Mode	X2TIMING Mode	SYSCLKOUT Cycles	SYSCLKOUT Cycles
Formula	0	0	Lead Value * 1	Trail Value * 1
	0	1	Lead Value * 2	Trail Value * 2
	1	0	Lead Value * 2	Trail Value * 2
	1	1	Lead Value * 4	Trail Value * 4
0	X	X	Not a valid value (do not use)	0
1	0	0	1	1
	0	1	2	2
	1	0	2	2
	1	1	4	4
2	0	0	2	2
	0	1	4	4

Table 2. Relationship Between Lead/Trail Values and the XTIMCLK/X2TIMING Modes (Continued)

Trail Value	XTIMCLK Mode	X2TIMING Mode	SYSCLKOUT Cycles	SYSCLKOUT Cycles
	1	0	4	4
	1	1	8	8
3	0	0	3	3
	0	1	6	6
	1	0	6	6
	1	1	12	12

Table 3. Relationship Between Active Values and the XTIMCLK/X2TIMIN Modes

Active Value	XTIMCLK Mode	X2TIMING Mode	Total Active SYSCLKOUT Cycles (includes 1 implied active cycle)
Formula	0	0	Active Value * 1 + 1
	0	1	Active Value * 2 + 1
	1	0	Active Value * 2 + 2
	1	1	Active Value * 4 + 2
0	0	X	1 or Invalid if XREADY used (USEREADY = 1)
	1	X	2 or Invalid if XREADY used (USEREADY = 1)
1	0	0	2
	0	1	3
	1	0	4
	1	1	6
2	0	0	3
	0	1	5
	1	0	6
	1	1	10
3	0	0	4
	0	1	7

Table 3. Relationship Between Active Values and the XTIMCLK/X2TIMIN Modes(Continued)

Active Value	XTIMCLK Mode	X2TIMING Mode	Total Active SYSCLKOUT Cycles (includes 1 implied active cycle)
	1	0	8
	1	1	14
4	0	0	5
	0	1	9
	1	0	10
	1	1	18
5	0	0	6
	0	1	11
	1	0	12
	1	1	22
6	0	0	7
	0	1	13
	1	0	14
	1	1	26
7	0	0	8
	0	1	15
	1	0	16
	1	1	30

4 XINTF Registers

Table 4 shows the XINTF configuration registers. Modification of these registers will affect the timing of XINTF accesses and should be performed only by code running outside of the XINTF.

Table 4. XINTF Configuration and Control Register Mappings

Name	Address	Size (x16)	Description
XTIMING0	0x0000–0B20	2	XINTF Timing Register, Zone 0
XTIMING1	0x0000–0B22	2	XINTF Timing Register, Zone 1
XTIMING2†	0x0000–0B24	2	XINTF Timing Register, Zone 2
XTIMING6	0x0000–0B2C	2	XINTF Timing Register, Zone 6
XTIMING7	0x0000–0B2E	2	XINTF Timing Register, Zone 7
XINTCNF2‡	0x0000–0B34	2	XINTF Configuration Register
XBANK	0x0000–0B38	1	XINTF Bank Control Register
XREVISION	0x0000–0B3A	1	XINTF Revision Register

† XTIMING3, XTIMING4, XTIMING5 are reserved for future expansion and are not currently used.
‡ XINTCNF1 is reserved and not currently used.

The individual timing parameters can be programmed into the XTIMING registers described in Figure 3.

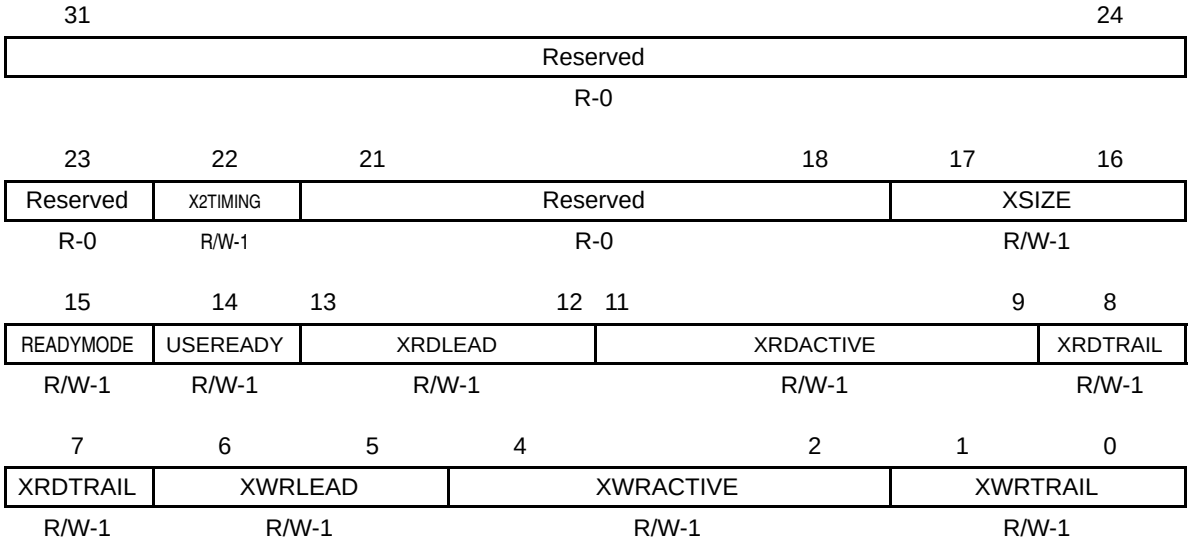
4.1 XINTF Timing Registers

Each XINTF zone has one timing register. Changes to this register will affect the timing of that particular zone. Changes to a zone's timing register should be made only by code executing outside of that zone.

Note: Timing Constraints

- ❑ Minimum wait-state requirements for different modes are shown in Section 2.
- ❑ The external device to which the 28x is interfaced may have additional timing constraints. See the vendor documentation for details.
- ❑ No logic is included to detect illegal settings.

Figure 3. XTIMING0/1/2/6/7 Register Layout



Note: R = Read; W = Write; -n = reset value

Bits	Name	Description
31–23	Reserved	
22	X2TIMING	This bit specifies the scaling factor of the XRDLEAD, XRDACTIVE, XRDTRAIL, XWRLEAD, XWRACTIVE, and XWRTRAIL values for the zone. 0 The values are scaled 1:1 1 The values are scaled 2:1 (doubled). This the default mode of operation on power up and reset.
21–18	Reserved	Reserved
17–16	XSIZE	These two bits must always be written to as 1, 1. Any other combination is reserved and will result in incorrect XINTF behavior. 0 0 Reserved – results in incorrect XINTF behavior 0 1 Reserved – results in incorrect XINTF behavior 1 0 Reserved – results in incorrect XINTF behavior 1 1 16-bit interface– the only valid combination
15	READYMODE	Sets the XREADY input sampling for the zone as synchronous or asynchronous. This bit is ignored if XREADY is not sampled (USEREADY = 0). 0 XREADY input is synchronous for the zone. 1 XREADY input is asynchronous for the zone.

Figure 3. XTIMING0/1/2/6/7 Register Layout (Continued)

Bits	Name	Description
14	USEREADY	Determines if accesses to the zone will sample or ignore the XREADY input signal. 0 The XREADY signal is ignored when accesses are made to the zone. 1 The XREADY signal can further extend the active portion of an access to the zone past the minimum defined by the XRDACTIVE and XWRACTIVE fields.
13–12	XRDLEAD	Two-bit field that defines the read cycle lead period for the zone, in XTIMCLK cycles, from 1, 2, 3 (if X2TIMING bit is 0) or 2, 4, 6 (if X2TIMING bit is 1). **Note:** See Section 3 for minimum constraints for different operating modes.

XRDLEAD		X2TIMING	Read Lead Period
0	0	X	Invalid
0	1	0	1 XTIMCLK cycle
		1	2 XTIMCLK cycles
1	0	0	2 XTIMCLK cycles
		1	4 XTIMCLK cycles
1	1	0	3 XTIMCLK cycles
		1	6 XTIMCLK cycles

Bits	Name	Description
11–9	XRDACTIVE	Three-bit field that defines the read cycle active wait-state period, in XTIMCLK cycles, from 0, 1, 2, 3, 4, 5, 6, 7 (if X2TIMING bit is 0) or 0, 2, 4, 6, 8, 10, 12, 14 (if X2TIMING bit is 1). **Notes:** 1) See Section 3 for minimum constraints for different operating modes. 2) The active period is, by default, 1 XTIMCLK cycle. Therefore, the total active period is (1 + XRDACTIVE) XTIMCLK cycles.

XRDACTIVE			X2TIMING	Read Active Period Waitstates
0	0	0	0	0
0	0	1	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles
0	1	0	0	2 XTIMCLK cycles
			1	4 XTIMCLK cycles
0	1	1	0	3 XTIMCLK cycles
			1	6 XTIMCLK cycles
1	0	0	0	4 XTIMCLK cycles
			1	8 XTIMCLK cycles
1	0	1	0	5 XTIMCLK cycles
			1	10 XTIMCLK cycles

Figure 3. XTIMING0/1/2/6/7 Register Layout (Continued)

Bits **Name** **Description**

XRDACTIVE			X2TIMING	Read Active Period Waitstates
1	1	0	0	6 XTIMCLK cycles
			1	12 XTIMCLK cycles
1	1	1	0	7 XTIMCLK cycles
			1	14 XTIMCLK cycles

8–7 XRDTRAIL Two-bit field that defines the read cycle trail period, in XTIMCLK cycles, from 0, 1, 2, 3 (if X2TIMING bit is 0) or 0, 2, 4, 6 (if X2TIMING bit is 1).

XRDTRAIL		X2TIMING	Read Trail Period
0	0	0	0
0	1	0	1 XTIMCLK cycle
		1	2 XTIMCLK cycles
1	0	0	2 XTIMCLK cycles
		1	4 XTIMCLK cycles
1	1	0	3 XTIMCLK cycles
		1	6 XTIMCLK cycles

6–5 XWRLEAD Two-bit field that defines the write cycle lead period, in XTIMCLK cycles, from 1, 2, 3 (if X2TIMING bit is 0) or 2, 4, 6 (if X2TIMING bit is 1).

Note: See Section 3 for minimum requirements for different operating modes.

XWRLEAD		X2TIMING	Write Lead Period
0	0	x	Invalid
0	1	0	1 XTIMCLK cycle
		1	2 XTIMCLK cycles
1	0	0	2 XTIMCLK cycles
		1	4 XTIMCLK cycles
1	1	0	3 XTIMCLK cycles
		1	6 XTIMCLK cycles

4–2 XWRACTIVE Three-bit field that defines the write cycle active wait-state period, in XTIMCLK cycles, from 0, 1, 2, 3, 4, 5, 6, 7 (if X2TIMING bit is 0) or 0, 2, 4, 6, 8, 10, 12, 14 (if X2TIMING bit is 1).

Notes: 1) See Section 3 for minimum requirements.

2) The active period is by default 1 XTIMCLK cycle. Therefore, the total active period is (1 + XWRACTIVE) XTIMCLK cycles.

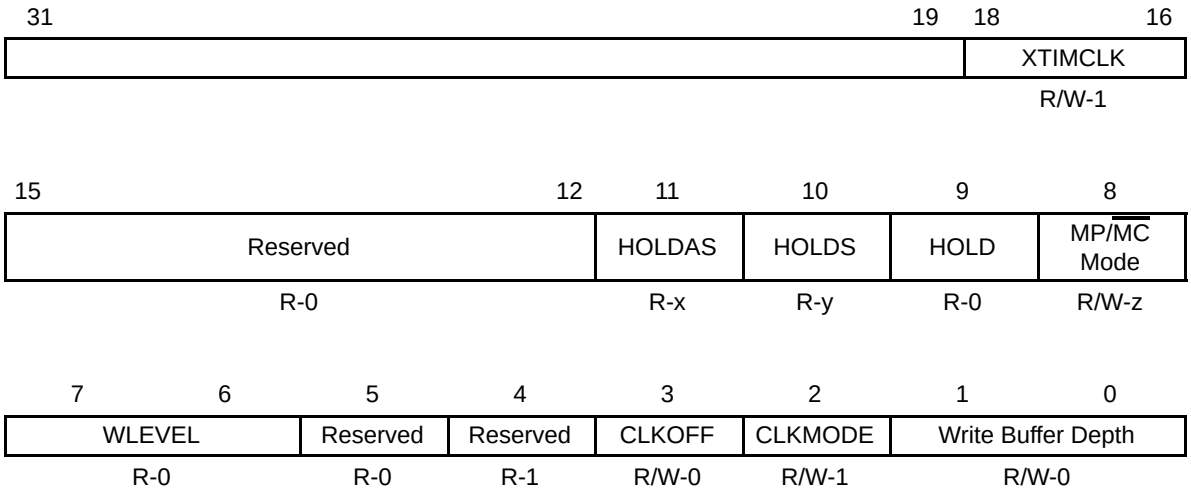
XWRACTIVE			X2TIMING	Write Active Period Wait States
0	0	0	x	0
0	0	1	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles

Figure 3. XTIMING0/1/2/6/7 Register Layout (Continued)

Bits	Name	Description				
		0	1	0	0	2 XTIMCLK cycles
					1	4 XTIMCLK cycles
		0	1	1	0	3 XTIMCLK cycles
					1	6 XTIMCLK cycles
		1	0	0	0	4 XTIMCLK cycles
					1	8 XTIMCLK cycles
		1	0	1	0	5 XTIMCLK cycles
					1	10 XTIMCLK cycles
		1	1	0	0	6 XTIMCLK cycles
					1	12 XTIMCLK cycles
		1	1	1	0	7 XTIMCLK cycles
					1	14 XTIMCLK cycles
1–0	XWRTRAIL	Two-bit field that defines the write cycle trail period, in XTIMCLK cycles, from 0, 1, 2, 3 (if X2TIMING bit is 0) or 0, 2, 4, 6 (if X2TIMING bit is 1).				
					X2TIMING	**Write Trail Period**
		0	0		x	0
		0	1		0	1 XTIMCLK cycle
					1	2 XTIMCLK cycles
		1	0		0	2 XTIMCLK cycles
					1	4 XTIMCLK cycles
		1	1		0	3 XTIMCLK cycles
					1	6 XTIMCLK cycles

4.2 XINTF Configuration Register

Figure 4. XINTCNF2 Register



Legend: R = Read; W = Write; -n = reset value; x = $\overline{\text{XHOLDA}}$ output; y = $\overline{\text{XHOLD}}$ input; z = XMP/$\overline{\text{MC}}$ input

Bits	Name	Description
31–19	Reserved	
18–16	XTIMCLK	These bits select the fundamental clock for the timing of lead, active and trail switching operations as defined by the XTIMING and XBANK registers: This setting affects all of the XINTF zones. Changes to the XTIMCLK ratio should be made only by code executing outside of the XINTF. 0 0 0 XTIMCLK = SYSCLKOUT/1 0 0 1 XTIMCLK = SYSCLKOUT/2 0 1 0 Reserved 0 1 1 Reserved 1 0 0 Reserved 1 0 1 Reserved 1 1 0 Reserved 1 1 1 Reserved
15–12	Reserved	Reserved

Figure 4. XINTCNF2 Register (Continued)

Bits	Name	Description
11	HOLDAS	This bit reflects the current state of the $\overline{\text{XHOLDA}}$ output signal. It can be read by the user to determine if the external interface is currently granting access to an external device. 0 $\overline{\text{XHOLDA}}$ output signal is low. 1 $\overline{\text{XHOLDA}}$ output signal is high.
10	HOLDS	This bit reflects the current state of the $\overline{\text{XHOLD}}$ input signal. It can be read by the user to determine if an external device is requesting access to the external bus. 0 $\overline{\text{XHOLD}}$ input signal is low. 1 $\overline{\text{XHOLD}}$ input signal is high.
9	HOLD	This bit grants a request to an external device that drives the $\overline{\text{XHOLD}}$ input signal and the $\overline{\text{XHOLDA}}$ output signal. 0 Automatically grants a request to an external device that is driving both the $\overline{\text{XHOLD}}$ input signal and the $\overline{\text{XHOLDA}}$ output signal low. 1 Does not grant a request to an external device that drives the $\overline{\text{XHOLD}}$ input signal low while the $\overline{\text{XHOLDA}}$ output signal stays high. If this bit is set while $\overline{\text{XHOLD}}$ and $\overline{\text{XHOLDA}}$ are both low (external bus accesses granted) then the $\overline{\text{XHOLDA}}$ signal is forced high (at the end of the current cycle) and the external interface is taken out of high-impedance mode. On a reset $\overline{\text{XRS}}$, this bit is set to zero. If, on a reset, the $\overline{\text{XHOLD}}$ signal is active-low, then the bus and all signal strobes must be in high-impedance state and the $\overline{\text{XHOLDA}}$ signal is also driven active-low. When HOLD mode is enabled and $\overline{\text{XHOLDA}}$ is active-low (external bus grant active) then the core can still execute code from internal memory. If an access is made to the external interface, then a not ready signal is generated and the core is stalled until the $\overline{\text{XHOLD}}$ signal is removed.
8	MP/$\overline{\text{MC}}$ Mode	On reset, this bit reflects the state of the XMP/$\overline{\text{MC}}$ input signal sampled at $\overline{\text{XRS}}$. You can modify the state of this bit by writing a 1 or a 0 to this location. This will be reflected on the XMP/$\overline{\text{MC}}$ output signal. This mode also affects ZONE 7 and Boot ROM mapping. All other zones ignore this bit. Changes to this bit should be made only by code executing outside of XINTF Zone 7. **Note:** The XMP/$\overline{\text{MC}}$ input signal state is ignored after reset. 0 Microcomputer state (XINTF ZONE 7 disabled, Boot ROM enabled). 1 Microprocessor state (XINTF ZONE 7 enabled, Boot ROM disabled).

Figure 4. XINTCNF2 Register (Continued)

Bits	Name	Description
7–6	WLEVEL	The current number of writes buffered are detectable as follows: 0 0 Empty 0 1 1 value currently in the write buffer 1 0 2 values currently in the write buffer 1 1 3 values currently in the write buffer The value in the write buffer may be 8-, 16-, or 32-bit data. **Note:** There may be a few cycles of delay from the time when a value enters the write buffer to the buffer level depth update.
5	Reserved	Reserved
4	Reserved	Reserved
3	CLKOFF	Turn XCLKOUT mode off. This is done for power savings and noise reduction. This bit is set to 0 on a reset. 0 XCLKOUT is enabled. 1 XCLKOUT is disabled.
2	CLKMODE Mode	XCLKOUT divide by 2 mode. All bus timings, irrespective of which mode is enabled, will start from the rising edge of XCLKOUT. The default mode of operation on power up and reset is /2 mode. Changes to the CLKMODE bit should be made only by code executing outside of the XINTF. 0 XCLKOUT is equal to XTIMCLK 1 XCLKOUT is a divide by 2 of XTIMCLK

Figure 4. XINTCNF2 Register (Continued)

Bits	Name	Description
1–0	Write Buffer Depth	The write buffer allows the processor to continue execution without waiting for XINTF write accesses to complete. The write buffer depth is selectable as follows:

0 0 No write buffering. The CPU will be stalled until the write completes on the XINTF.

Note: Default mode on reset ($\overline{\text{XRS}}$).

0 1 One write is buffered and the CPU will stall for the second write. The CPU is stalled until the write cycle begins on the XINTF (there could be a read cycle currently active on the XINTF).

1 0 Two writes are buffered and the CPU will stall for the third write. The CPU is stalled if a second write follows. The CPU will be stalled until the first write begins its cycle on the XINTF.

1 1 Three writes are buffered. The CPU is stalled if a fourth write follows. The CPU will be stalled until the first write begins its cycle on the XINTF.

Order of execution is preserved, e.g., writes are performed in the order they were accepted. The processor is stalled on XINTF reads until all pending writes are done and the read access completes. If the buffer is full, any pending reads or writes to the buffer will stall the processor.

The “Write Buffer Depth” can be changed; however, it is recommended that the write buffer depth be changed only when the buffer is empty (this can be checked by reading the “Write Buffer Level” bits). Writing to these bits when the level is not zero may have unpredictable results.

4.3 XBANK Register

Figure 5. XBANK Register

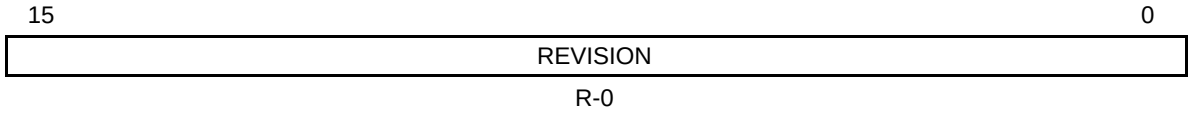
15	6	5	3	2	0
Reserved		BCYC		BANK	
R-0		R/W-1		R/W-1	

Bits	Name	Description
15:6	Reserved	
5:3	BCYC	These bits specify the number of XTIMCLK cycles to add between any consecutive access that crosses into or out of the specified zone, be it a read or write, program or data space. The number of XTIMCLK cycles can be 0 to 7. On a reset ($\overline{XRS}$) the value defaults to 7 XTIMCLK cycles (14 SYSCLKOUT cycles). 0 0 0 0 cycle 0 0 1 1 XTIMCLK cycle 0 1 0 2 XTIMCLK cycles 0 1 1 3 XTIMCLK cycles 1 0 0 4 XTIMCLK cycles 1 0 1 5 XTIMCLK cycles 1 1 0 6 XTIMCLK cycles 1 1 1 7 XTIMCLK cycles
2:0	BANK	These bits specify the XINTF zone for which bank switching is enabled, ZONE 0 to ZONE 7. At reset, XINTF Zone 7 is selected. 0 0 0 Zone 0 0 0 1 Zone 1 0 1 0 Zone 2 0 1 1 Reserved 1 0 0 Reserved 1 0 1 Reserved 1 1 0 Zone 6 1 1 1 Zone 7 (selected at reset by default)

4.4 XREVISION Register

The XREVISION register contains a unique number to identify the particular version of XINTF used in the product. For the 2812, this register will be configured as described in Figure 6.

Figure 6. XREVISION Register Layout



Bits	Name	Description
15–0	REVISION	Current XINTF Revision. For internal use/reference. Test purposes only. Subject to change.

5 Signal Descriptions

Table 5. XINTF Signal Descriptions

Name	I/O/Z	Description
XD(15:0)	I/O/Z	Bidirectional 16-bit data bus
XA(31:0)	O/Z	Address bus. The address is placed on the bus on the rising edge of XCLKOUT and held on the bus until the next access. Specific devices may not have all 32 address lines. See the data sheet for a specific device.
XCLKOUT	O/Z	Single output clock derived from the XTIMCLK to be used for on-chip and off-chip wait-state generation and as a general-purpose clock source. XCLKOUT is either the same frequency or 1/2 the frequency of XTIMCLK, as defined by the CLKMODE bit in the XINTCNF2 register. At reset XCLKOUT = 1/2 XTIMCLK XCLKOUT = 1/4 SYSCLKOUT
$\overline{\text{XWE}}$	O/Z	Active low write strobe. This signal is driven low on all bus modes and data size types. The write strobe waveform is specified, per zone basis, by the Lead, Active, Trail periods in the XTIMINGx registers.
$\overline{\text{XRD}}$	O/Z	Active low read strobe. This signal is driven low on all bus modes and data size types. The read strobe waveform is specified, per zone basis, by the Lead, Active, Trail periods in the XTIMINGx registers. **Note:** The $\overline{\text{XRD}}$ and $\overline{\text{XWE}}$ signals are mutually exclusive.
XR/$\overline{\text{W}}$	O/Z	Read/not write control. When high, this signal indicates a read cycle is active, when low, it indicates a write cycle is active. This signal is normally held high. The XR/$\overline{\text{W}}$ and $\overline{\text{XSTRB}}$ signals perform similar functions to the $\overline{\text{XRD}}$ and $\overline{\text{XWE}}$ signals. Generally, users opt to use the latter because they are cleaner and easier to use.
$\overline{\text{XZCS0}}$ $\overline{\text{XZCS1}}$ $\overline{\text{XZCS2}}$ $\overline{\text{XZCS6}}$ $\overline{\text{XZCS7}}$	0	Zone chip selects. These signals are active when an access to the addressed zone is performed. Some devices such as the F2812 have two zone chip-select signals internally ANDed to form one single chip select. See the data sheet for details.
XREADY	I	Indicates peripheral is READY to $\overline{\text{complete}}$ the access when asserted to 1. For each XINTF zone, this can be configured to be a synchronous or an asynchronous input. In synchronous mode, the XINTF interface block requires XREADY to be valid one XTIMCLK clock cycle before the end of the active period. In asynchronous mode, The XINTF interface block samples XREADY three XTIMCLK clock cycles before the end of the active period. XREADY is sampled at the XTIMCLK rate independent of the XCLKOUT mode.

Table 5. XINTF Signal Descriptions (Continued)

Name	I/O/Z	Description
$\overline{\text{XHOLD}}$	I	This signal, when active low, requests the XINTF to release the external bus (place all busses and strobes into high-impedance state). The XINTF releases the bus when any current access is complete and there are no pending accesses on the XINTF. This signal is an asynchronous input and is synchronized by XTIMCLK.
$\overline{\text{XHOLDA}}$	O/Z	This signal is driven active low, when the XINTF has granted an $\overline{\text{XHOLD}}$ request. All XINTF busses and strobe signals will be in a high-impedance state. This signal is released when the $\overline{\text{XHOLD}}$ signal is released. External devices should only drive the external bus when this signal is active low.
XMP/$\overline{\text{MC}}$	I	Switches between microprocessor and microcomputer mode. When high, Zone 7 is enabled on the external interface. When low, Zone 7 is disabled from the external interface, and on-chip memory (i.e., ROM) may be accessed instead. This signal is latched into the XINTCNF2 register on a reset ($\overline{\text{XRS}}$) and you can modify the state of this mode in software. **Note:** The state of the XMP/$\overline{\text{MC}}$ input signal is ignored after reset.

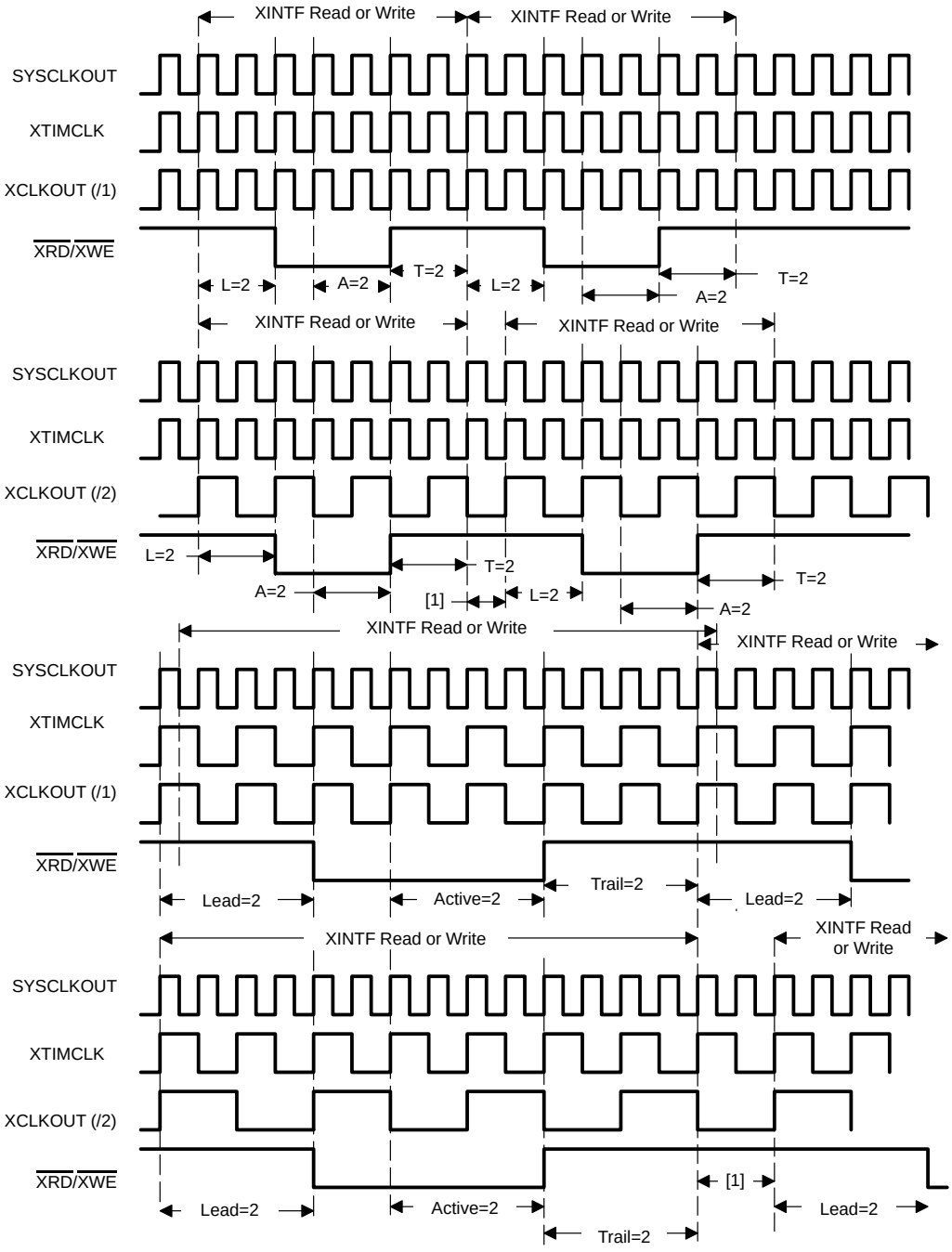
6 Waveforms

Figure 7 shows example timing waveforms for various XTIMCLK and XCLKOUT modes assuming X2TIMING = 0 and Lead = 2, Active = 2 and Trail = 2.

Note:

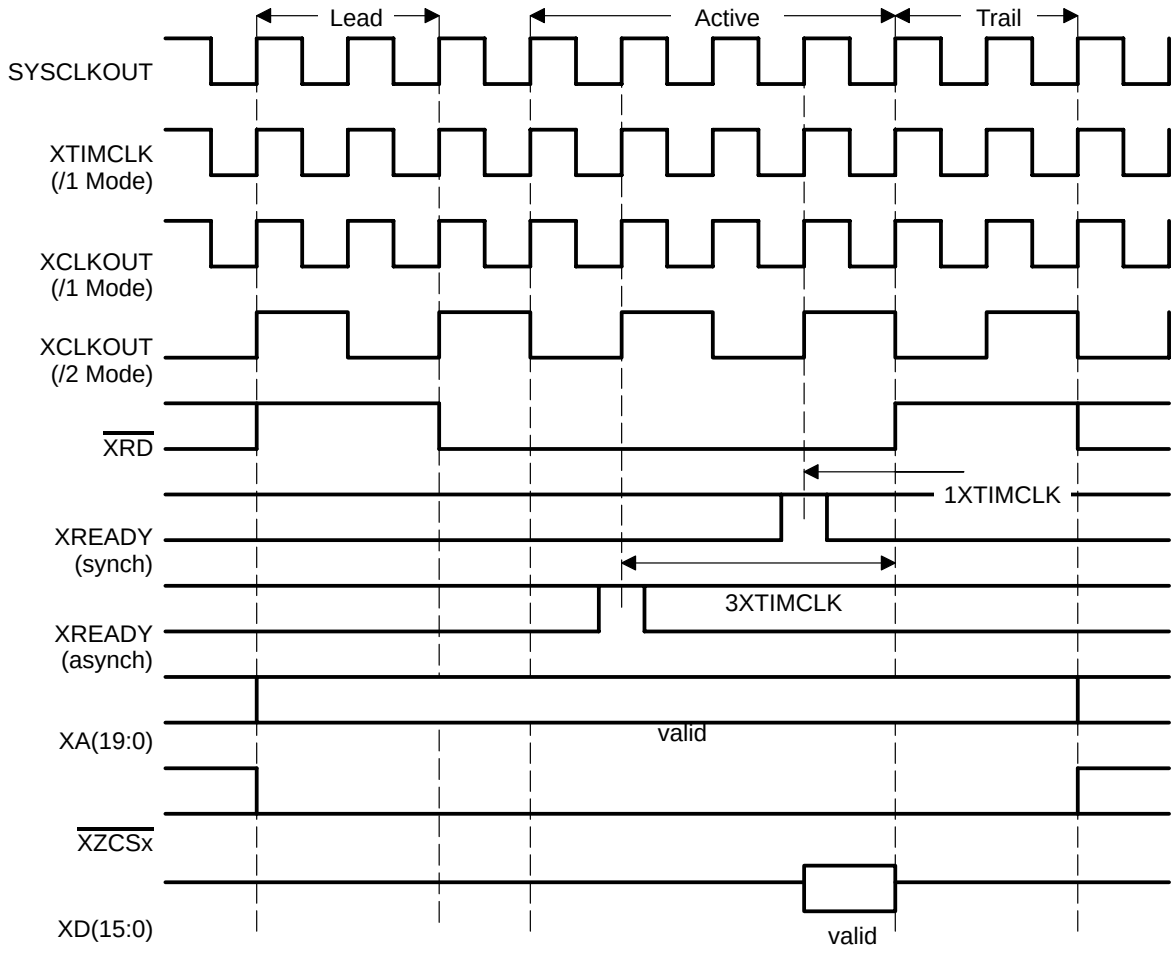
The diagrams included in this document are conceptual, cycle-by-cycle representations of the XINTF behavior. They do not take into account any buffer delays and additional setup times that will be found on a physical device. For more exact device-specific timing information for the XINTF, see the data sheet electrical timing specifications for that device.

Figure 7. XTIMCLK and XCLKOUT Mode Waveforms With X2TIMING = 0, Lead = 2, Active = 2, and Trail = 2



Note: Alignment cycle. Necessary to make sure all bus cycles start on rising edge of XCLKOUT.

Figure 8. Generic Read Cycle (XTIMCLK = SYSCLKOUT mode)



The XREADY signal can be sampled synchronously or asynchronously or ignored by each zone. If it is sampled synchronously, then the XREADY signal MUST meet set-up and hold timing relative to one XTIMCLK edge before the end of the active period. If it is sampled asynchronously, then the XREADY signal MUST meet set-up and hold timing relative to three XTIMCLK edges before the end of the active period. If XREADY is low at the sampling interval, an extra XTIMCLK period is added to the active phase and the XREADY input is sampled again on the next rising edge of XTIMCLK. XCLKOUT has no effect on the sampling interval. Once a valid XREADY high signal has been detected, the input is ignored until the next valid bus cycle.

Figure 9. Generic Read Cycle (XTIMCLK = 1/2 SYSCLKOUT mode)

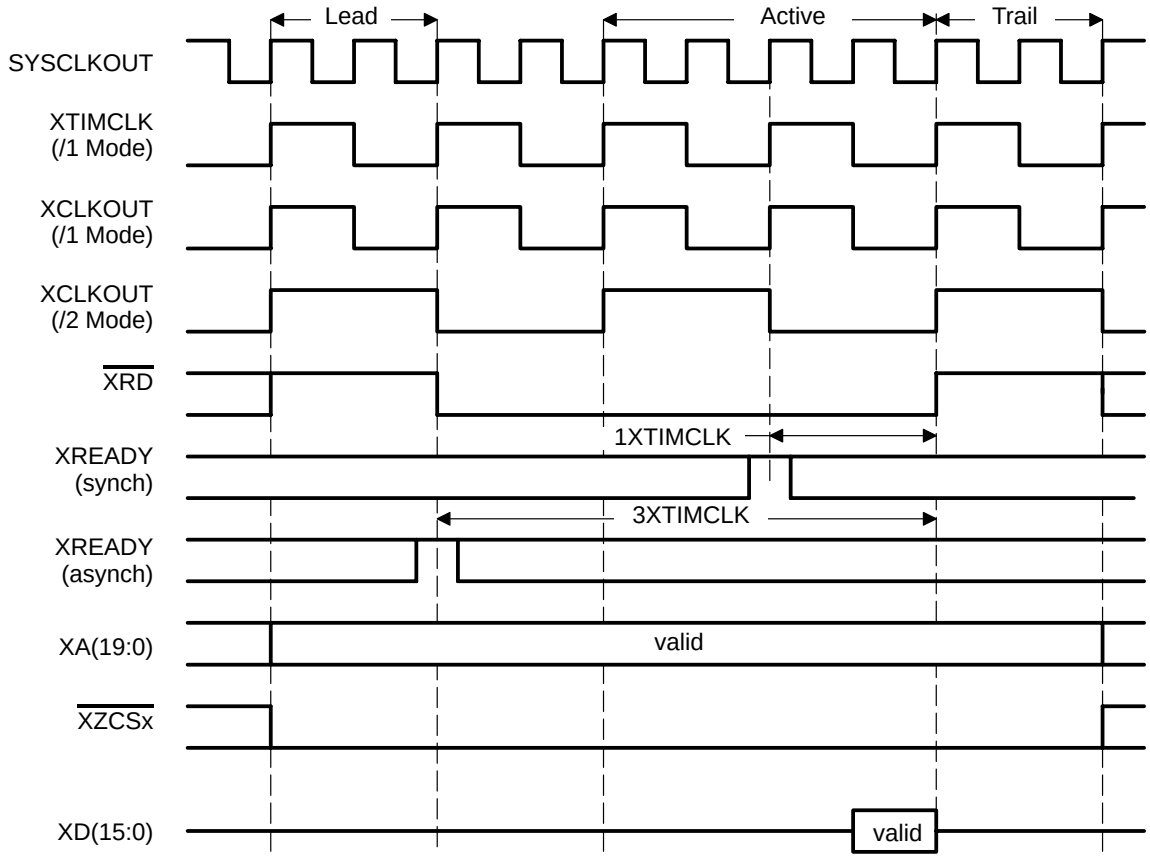
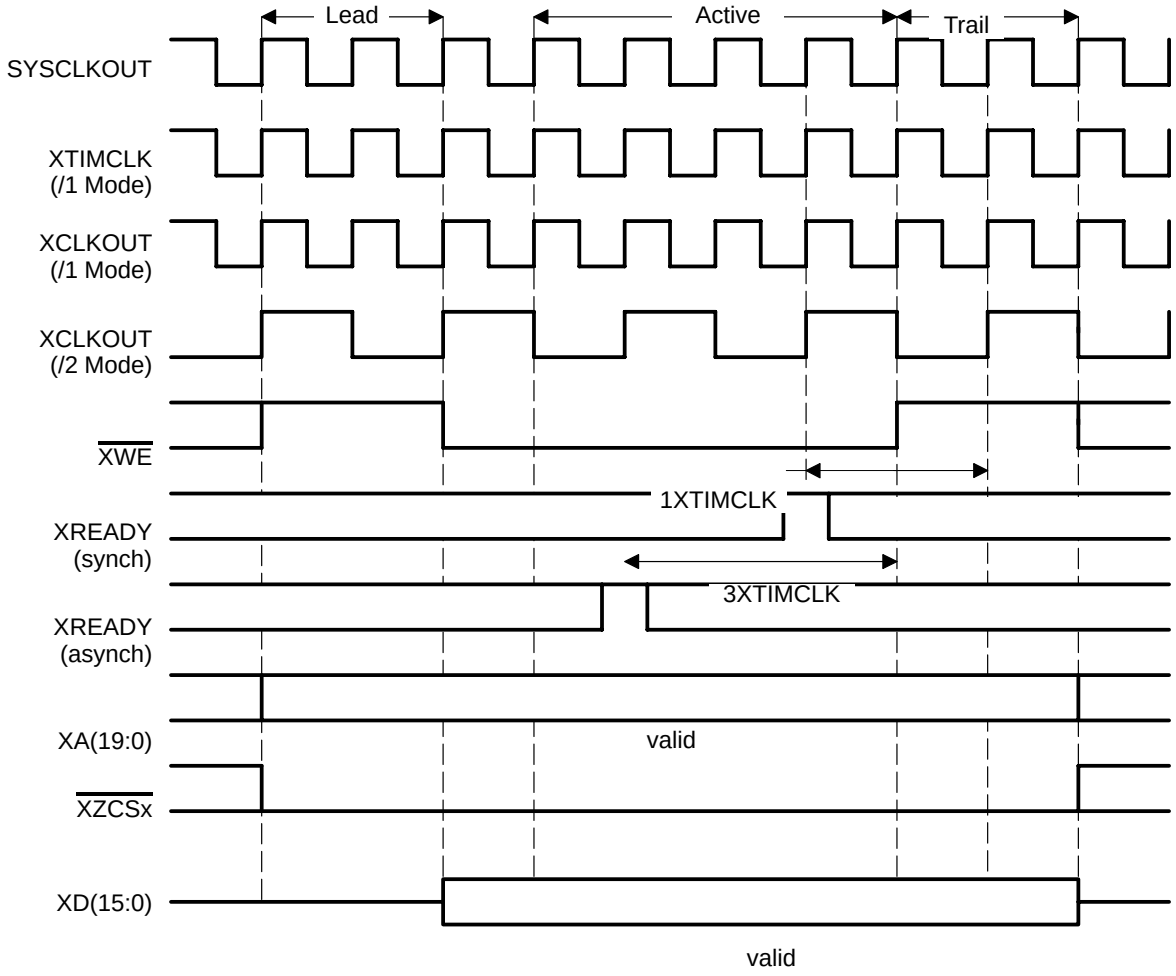


Figure 10. Generic Write Cycle (XTIMCLK = SYSCLKOUT mode)



Note: If the lead and active timing parameters are set low enough, it may not be possible to generate a valid XREADY signal. No hardware is added to detect this.

7 External DMA Support (XHOLD, XHOLDA)

The XINTF supports direct memory access (DMA) to its local (off-chip) program and data spaces. This is accomplished with the XHOLD signal input and XHOLDA output. When XHOLD is asserted (low active) a request to the external interface is generated to hold all outputs from the external interface a high-impedance state. Upon completion of all outstanding accesses to the external interface, XHOLDA is asserted (low active). XHOLDA signals external devices that the external interface has its outputs in high-impedance state and that another device can control access to external memory or peripherals.

The HOLD Mode bit in XINTCNF2 register enables the automatic generation of a XHOLDA signal and granting access of the external bus, when a valid XHOLD signal is detected. While in HOLD mode, the CPU can continue to execute code from on-chip memory attached to the memory bus. If an attempt is made to access the external interface while XHOLDA is low, a not ready condition is generated, halting the processor. Status bits in the XINTCNF2 register will indicate the state of the XHOLD and XHOLDA signals.

If XHOLD is active, and the CPU attempts a write to the XINTF, the write is not buffered and the CPU will stall. The write buffer is disabled.

The HOLD mode bit in XINTCNF2 register bit will take precedence over the XHOLD input signal. Thus enabling customer code to determine when or not a XHOLD request is to be honored.

The XHOLD input signal is synchronized at the input to the XINTF before any actions are taken. Synchronization is with respect to XTIMCLK.

The HOLDS bit in XINTCNF2 register reflects the current synchronized state of the XHOLD input.

On reset, the HOLD mode bit is enabled, allowing for bootload of external memory using an XHOLD request. If XHOLD signal is active low during reset, the XHOLDA signal is driven low as per normal operation.

During power up, any undefined values in the XHOLD synchronizing latches are ignored and would eventually be flushed out when the clock stabilizes. Hence, synchronizing latches do not need to be reset.

If an XHOLD active low signal is detected, the XHOLDA signal is only driven low after all pending XINTF cycles are completed. Any pending CPU cycles are blocked and the CPU is held in a not-ready state if they are targeted for the XINTF.

Definitions:

Pending XINTF Cycle – Any cycle that is currently in the XINTF FIFO queue.

Pending CPU Cycle – Any cycle that is not in the FIFO queue but is active on the core memory bus.

The XHOLD signal should not be removed until the XHOLDA signal becomes active. Unpredictable results will occur if this rule should be violated.

The state of the XINTF external signals is as follows in HOLD mode:

Signal	HOLD Granted Mode
XA(31:0), XD(15:0)	High-impedance
XRD, XWE, XR/W	High-impedance
XZCS	High-impedance
XZCS0	High-impedance
XZCS1	High-impedance
XZCS2	High-impedance
XZCS6	High-impedance
XZCS7	High-impedance

All other signals remain in their normal operating states.

Appendix A

Revision History

This document was revised to SPRU067B from SPRU067A, which was released in June 2003. The scope of the revisions was limited to technical changes as described in A.1. This appendix lists only revisions made in the most recent version.

A.1 Changes Made in This Revision

The following changes were made in this revision:

Page	Additions/Modifications/Deletions
	Figure 3, Note 1 was corrected (reference to Section 2 changed to 3)
	Figure 3, bit description for bits 13–12 corrected (X2TIMING Invalid changed to don't care)
	Figure 3, bit description for bits 11–9 corrected (Invalid changed to 0)
	Figure 3, bit description for bits 8–7 (Invalid changed to 0)
	Figure 3, bit description for bits4–2 (Invalid changed to 0)

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