WHITE PAPER

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# Bringing Efficient Communications to Real-Time Motor Control and Power Conversion Applications with TI's Viterbi Complex Math Unit (VCU)

## Introduction

To take advantage of the growing opportunities in Smart Metering and other energy-control applications, developers need to be able to add communication links to existing systems in a cost-effective manner. TI's innovative Viterbi Complex Math Unit (VCU), introduced to the real-time control TMS320C2000™ microcontroller (MCU) platform, provides an enhanced math engine that accelerates complex communications algorithm processing by a factor of up to 7×. This white paper provides an overview of how the VCU adds system efficiency and performance that complements the TMS320C28x™ DSP core, including key operation examples, benchmarks and architecture benefits.

Initiatives like the Smart Grid and Renewable Energy offer tremendous market opportunities to manufacturers. By introducing intelligent management and communications technology to real-time motor control and power-conversion applications, interactions between systems can be coordinated to improve operating efficiency.

For metering applications and systems where energy efficiency is crucial, power line communication (PLC) is becoming a key enabling technology for implementing intelligent management. By communicating data over the actual power lines, systems can be connected without having to install new wires or require cellular service from a third party. Applications include transmitting data from house meters to the utility companies, controlling street lighting, coordinating movement between solar panel arrays, and enabling remote management of charging for electric vehicles, to name a few.

Modern power line communications standards, including PRIME and G3, rely upon orthogonal frequency division multiplexing (OFDM), a modulation technique similar to what is used by ADSL modems. These standards, however, are computationally intensive, and microcontrollers (MCUs) already pressed to their limits maintaining reliable motor control or power conversion do not have the capacity to also support power line communications.

To meet this need, TI has developed the innovative Viterbi Complex Math Unit (VCU). Integrated into its F28x series of controllers built upon TI's industry-leading C28x™ core, the VCU accelerates the performance of communications-based algorithms by a factor of up to 7×. In addition to eliminating the need for a second processor to manage the communications link, the performance gain of the VCU provides headroom for future system growth and higher bit rates or, conversely, enables devices to operate at a lower MHz to reduce system cost and power consumption.

## Convergence of control and communications

Intelligent power management is essential to achieving higher operating efficiency, and the need for a reliable link between devices is quickly leading to a convergence of control and communications technology:

- **Monitoring:** One way utility companies are reducing peak load requirements on the power grid is to provide economic incentives for consumers and businesses to shift their power usage based on time of day. For example, consumers will pay less to run their dryer during the evening than during the day. To enable time-of-day rates, the utility companies need a communications channel to monitor device usage.
- **Remote Management:** As the distribution of power becomes more complex, control systems are increasingly being required to intelligently control power usage. For example, consider that the majority of drivers will plug in their electric cars right after they finish work, potentially causing the power grid challenges. With intelligent power control, cars can be charged in turn based on the available capacity of the grid.
- **Automation:** For applications such as solar panels and windmill generators, an intelligent controller is required to maximize conversion rates by dynamically adjusting panels and generators to optimally face the sun and wind direction.

With many communications interfaces, receiving signals is typically more compute-intensive than transmitting. This is due, in part, to noise across the physical medium which must be removed using complex filters in order to recover the data. In addition, error detection and corrections mechanisms are used to determine if data has been corrupted during transmission (i.e., CRC) and to potentially correct multiple errors across packets (i.e., Reed Solomon decoding).

Figure 1 shows a generic power line communication block diagram with some of the many components that comprise it. Managing a power line communications link consumes a great deal of CPU capacity, and developers need a processor that is designed not only to support real-time motor control and power conversion but has also been optimized for reliable communications.

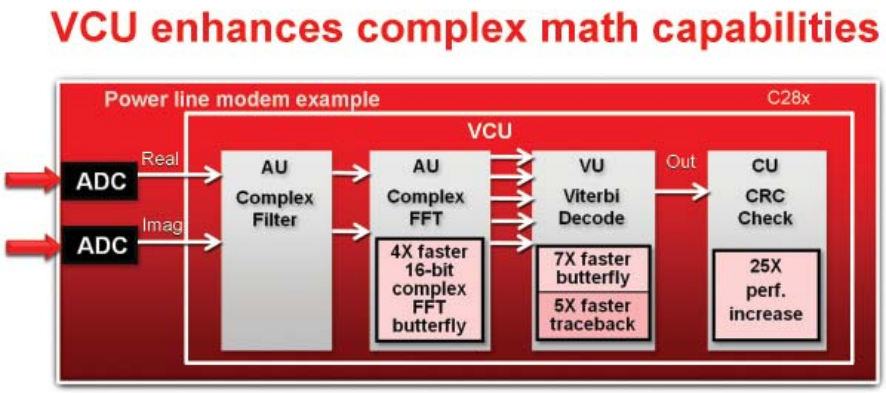



*Figure 1. Communication technologies like power line communications (PLC) require complex algorithms that consume a great deal of CPU capacity. To implement them, developers need a processor that is designed not only to support real-time motor control and power conversion but has also been optimized for reliable communications.*

The ability to offload complex algorithmic processing from the main CPU is crucial to improving performance and efficiency while keeping system cost down, especially as data rates increase. Implementing a real-time communications link completely in software can significantly burden the CPU in a way that can negatively impact the reliability of real-time motor control and power-conversion functions by increasing system latency and reducing real-time responsiveness. TI's F28x MCUs, built on the C28x™ architecture and enhanced with the VCU, were designed for both efficient control and reliable communication.

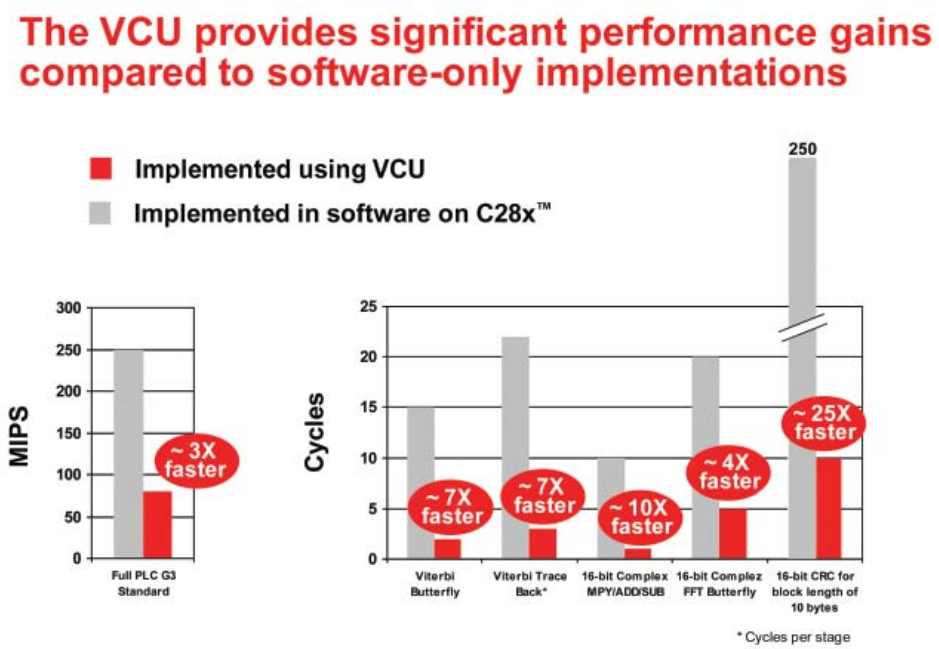
## Accelerating communications with the VCU

When designing the architecture for the VCU, TI evaluated different communications technologies and identified the four key operations which account for approximately 80 percent of the MIPS required to manage a communications link: Viterbi decoding, FFT, complex filters, and CRC calculations. For example, OFDM modulation for PLC uses all of these operations extensively.

Applications utilizing the hardware- and parallel processing-based capabilities of the VCU will see significant performance gains (see Graph 1 below). Several examples of VCU program code detailing its efficiency and programming simplicity are given at the end of this white paper.

## VCU capabilities and key operations

- **Viterbi Decoding:** Viterbi decoding is commonly used in baseband communications applications. Without a VCU, it takes 15 cycles for the C28x DSP core to perform two Viterbi butterfly calculations. F28x MCUs with the VCU option can perform two simultaneous butterflies in just two cycles. Similarly, a Viterbi trace back implemented in software takes 22 cycles per stage compared to just 3 cycles per stage using the VCU.




*Graph 1. The VCU provides significant performance gains compared to software-only implementations.*

- **FFT:** The Fast Fourier Transform is used in spread spectrum communications, as well as in many signal-processing algorithms. A 16-bit complex FFT implemented in software on the C28x™ core requires ~20 cycles; with the VCU, only 5 cycles per stage are required. The VCU can also perform automatic saturation plus rounding and scaling to maximize accuracy of computations.
- **Complex Filters:** Complex filters improve data reliability, transmission distance, and power efficiency. The VCU can perform a complex I and Q multiple with coefficients (four multiplies) in a single cycle. This calculation normally requires ~10 cycles to complete. In addition, the VCU can read/write the real and imaginary parts of 16-bit complex data to memory in a single cycle.
- **CRC:** Cyclical Redundancy Check (CRC) algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The VCU can perform 8-, 16-, and 32-bit CRCs in the background to completely offload CRC processing from the main CPU. For example, the VCU can compute the CRC for a block length of 10 Bytes in 10 cycles compared to approximately 250 cycles without the VCU. Register VCRC contains the current CRC which is updated whenever a CRC instruction is executed, thus simplifying CRC calculations and access to the final CRC value.

As an example of the impact the VCU can have on system performance, consider an implementation of PLC using the G3 standard. Without the VCU, implementing G3 requires ~250 MIPS. Using the VCU, CPU utilization drops significantly to less than 80 MIPS. A reduced CPU load for the communications link allows developers to clock the CPU at a lower frequency to conserve power or frees up the CPU for other operations such as supporting a higher data rate, running a more robust algorithm, or implementing better filtering.

## *Advanced architecture*

The VCU was specifically designed to accelerate the performance of communications. The F28x architecture is already optimized for math processing and real-time control. With the introduction of the VCU option, the F28x is now also optimized for communications. In this way, a single chip can provide reliable, real-time control for one or more motors as well as manage communications with other devices.

To make the VCU as simple to use as possible, TI has implemented it in a similar fashion to an integrated floating-point unit (FPU). An application issues instructions to the VCU in the same way that an application issues an instruction to the FPU using dedicated registers with pointers to data and result buffers. This allows applications to utilize VCU-accelerated calculations at any time.

The VCU implements very optimized, efficient instructions (see Figure 2 on the following page) to complement the high-performance C28x™ core and increase the computational bandwidth of the device. No changes were made to the CPU pipeline, memory bus architecture, emulation features, or existing instruction set. VCU instructions are an extension to the current C28x instruction set and use the same format as C28x and FPU operands. Existing C28x code is 100 percent source code and object code compatible with MCUs enhanced with a VCU. In this way, communications puts much less of a load on the CPU.

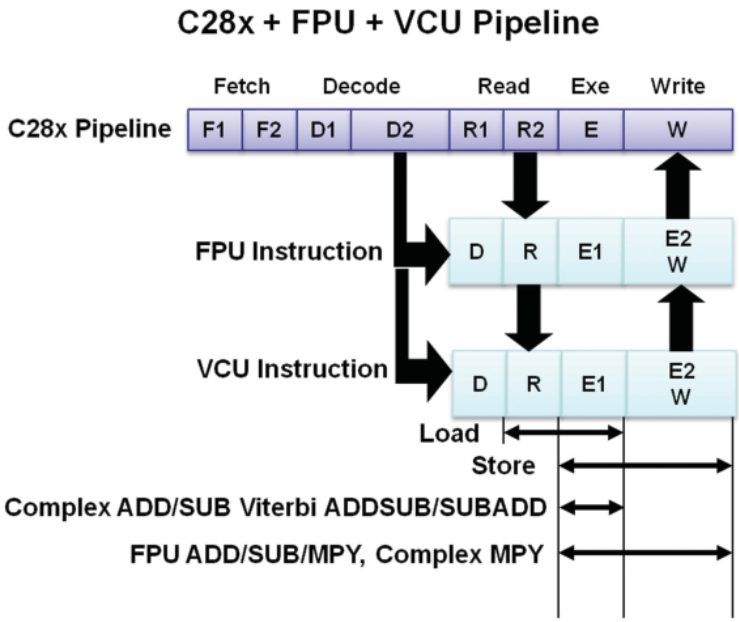



*Figure 2: The VCU implements very optimized, efficient instructions to complement the high-performance C28x core and increase the computational bandwidth of the device.*

Some of the specialized Viterbi decoding instructions that the VCU supports include branch metrics calculations, ADD-Compare-Select operations and trace back. Other enhanced instructions include a variety of complex math operations that support real and imaginary ($a + bj$) numbers as required for filter and FFT calculations. The VCU also adds 12 independent registers to facilitate simplified passing of pointers, reduce memory accesses, and enable the development tools to optimize code for throughput and code size efficiency (see Figure 3 on page 8).

Just as it is with an FPU, a few of the VCU operations require more than a single cycle to execute. In the case of a complex multiply/MAC, there is a two-cycle latency so the result cannot be used by the next instruction. However, as a new instruction can be started each cycle, a non-conflicting instruction (i.e., one that does not use the same source or destination register) can be executed immediately after a two-cycle instruction to improve performance. This instruction can be any C28x, FPU, or VCU operation. As a consequence, multiple instances of the same VCU operation can be issued in sequence. This enables the VCU to provide two complete Viterbi butterfly calculations every cycle. Note that all other VCU instructions execute in a single cycle.

The increased efficiency the VCU brings to the F28x MCU provides many benefits for developers:

- **Better Performance:** The combined effect of the F28x MCU's overall architecture – including VCU, FPU, and Control Law Accelerator (CLA) – provides superior performance, accuracy and efficiency across a wide range of applications.

- **Higher Power Efficiency:** With greater processing efficiency, the F28x can accomplish more work faster, allowing the MCU to be operated at a lower frequency and therefore consume less power. Higher efficiency also gives developers the option of implementing a higher bit rate communications link to reduce overall transmission time.
- **Greater Flexibility:** Because the VCU accelerates complex communications algorithm processing in software, developers can optimize the various characteristics of a communications link to the particular application and its operating environment.
- **Lower System Cost:** The VCU makes it possible to implement a communications link on the same device controlling the system motor or power convertor. This reduces overall system cost by eliminating the need for a second MCU just to manage the PLC communications link.
- **Ease of Design:** Being able to integrate all system functions on a single chip greatly simplifies design compared to having to implement system communications and intelligence across multiple MCUs. In addition, developers are able to design the entire system from a single development environment.

While designed specifically to accelerate communications processing, the VCU is also useful for many signal-processing applications not managing a communications link. Just as an FPU provides advanced mathematical capabilities, the VCU is extremely efficient at performing FFT, filter, and CRC calculations. For example, many motor control applications can improve efficiency by measuring and compensating for vibration using FFT-based algorithms and complex filters. Similarly, memory integrity checks can be accelerated using the VCU's CRC-32 capabilities. By utilizing the VCU for these operations, the architecture significantly reduces the MIPS loading on the C28x core to achieve greater throughput and power efficiency.

### *Flexible efficiency*

Programming the VCU is a straightforward process. TI provides a complete library of functions that can be called from C programs that execute core operations such as an FFT or Viterbi butterfly across an entire data set. These functions utilize the VCU instructions in an efficient manner that simplifies the implementation of complex communications functions while minimizing overhead. Functions with source code are supplied for Viterbi decoding, CRC functions, FFTs, and complex filters.

TI is also supplying higher-level functions to support various communications algorithms, including implementations of the PRIME and G3 standards for PLC. These functions provide the easiest programming route to implementing PLC and include production-ready code. Developers can customize any of these functions for a particular application through flexible parameterization to fine-tune performance.

The ability to customize functions is one of the key advantages of implementing a communications standard like PLC using the VCU. The programmability benefit of the VCU is especially important for PLC because the standards continue to evolve so developers require the flexibility to update firmware and algorithms. Because of their compute-intensive nature, communication algorithms have traditionally been implemented

in hardware; for example, a hardware-based Viterbi function is relatively fixed in its implementation. Characteristics such as filter size are inflexible and therefore hardware-based functions are limited in how well they can be tuned to a particular application and its operating environment.

Because of the efficiency of the VCU and the inherent flexibility of its instruction set, the F28x is able to provide the efficiency and performance of hardware-accelerated computation with the inherent flexibility of software. In this way developers can, for example, create an optimized Viterbi decoder by building upon the library functions provided to implement a lower bit rate for a low-cost member of a product line.

To accelerate evaluation and implementation of the F28x and VCU, TI offers the F2806x controlSTICK and Experimenter's kits. Support for the VCU is integrated into Code Composer Studio™ v4.2 integrated development environment, with full instruction disassembly and register viewing capabilities, making programming and debugging the VCU similar to using the FPU. To further simplify design, the C28x™ Codegen Tools v6.0 support VCU instructions, as well as provide the ability to generate a CRC of an output section and automatically embed it into the .out file. TI also offers plcSUITE, a powerful platform providing specialized software and analysis tools which enables developers to quickly implement a robust PLC link.

### *Evolving with the F28x*

One of the key advantages of the F28x architecture is the ease with which new instructions can be added. The flexibility of the C28x core to add new instructions is important because it gives TI the ability to provide innovative capabilities such as the VCU within a single processor generation. Multi-vendor MCU architectures, for example, have a much longer design chain. To introduce a new instruction to the core, the instruction has to first be added to one of its families. One of the partner vendors then has to manufacturer the new architecture in a system on chip (SoC).

By being in control of its own roadmap, TI is able to work with its customers to determine what they need and more quickly introduce features and capabilities that address these needs. For example, work is already underway to enhance the VCU and increase performance in future generations such as eliminating multi-cycle operation latencies and introducing new operation to accelerate security processing. This will further reduce the number of CPU MIPS required for communications functions as well as increase the maximum data rate that can be supported. Designs built upon the F28x with VCU will be able to transparently benefit from these improvements as they are released.

The drive for renewable energy and more intelligent control systems promises to bring higher levels of efficiency and new market opportunities. Offering a full complement of hardware kits, software libraries, and development tools, TI simplifies the development of intelligent energy systems. However, with the introduction of the VCU, TI has taken a major step ahead of the competition. Not only does the F28x provide superior motor control and power conversion capabilities, developers are able to easily introduce communications such as power line communications to new or existing designs using a single MCU. C2000™ real-time control MCUs

are already being used in a great many motor control and power conversion applications, and TI is well-positioned to assist the industry in taking full advantage of the convergence of control and communications.

## Accelerating communications calculations with the VCU

The following examples illustrate in detail many of the VCU's capabilities for accelerating communications processing:

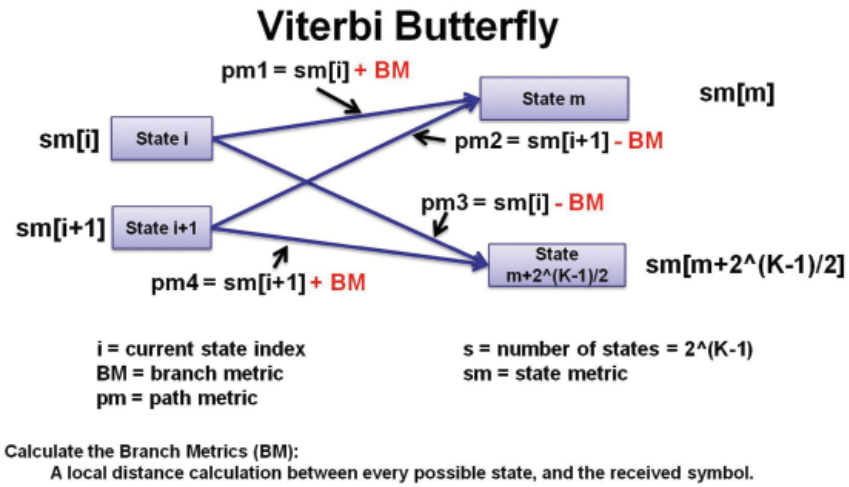



*Figure 3. A butterfly operation as calculated during Viterbi decoding.*

Figure 3 shows a Viterbi Butterfly operation. Four path metrics (pm1, pm2, pm3, pm4) need to be calculated by adding or subtracting the branch metric from the current state metrics (sm[i] and sm[i+1]). When the Code Rate (CR) is 1/2 – one input yields two outputs – there are two branch metric values. Which branch metric will be used depends upon the butterfly being evaluated. New state metrics need to be calculated, as well as transitions bits.

The following code shows how this calculation is achieved using the VCU. Note that the path metrics are calculated in a single cycle, as are both new state metrics. Altogether, the entire operation requires only two cycles to execute. If implemented in software on the F28x without using the VCU, this operation would require 15 cycles.

```
Instruction Example:                    Instruction Operations:
VITDLADDSUB VR4, VR3, VR2, VR0          ; pm1 = VR3L = sm[i]   + BM0 = VR2L + VR0L
                                        ; pm2 = VR3H = sm[i+1] - BM0 = VR2H - VR0L
                                        ; pm3 = VR4L = sm[i]   - BM0 = VR2L - VR0L
                                        ; pm4 = VR4H = sm[i+1] + BM0 = VR2H + VR0L

VITLSEL VR6, VR5, VR4, VR3              ; VT0 = VT0 << 1       VT1 = VT1 << 1
                                        ;
                                        ; Check if pm1 > pm2
                                        ;   if (VR3L > VR3H)
                                        ;         VR5H = VR3L (pm1)   and VT0[0] = 0
                                        ;   else VR5H = VR3H (pm2)   and VT0[0] = 1
                                        ;
                                        ; Check if pm3 > pm4
                                        ;   if (VR4L > VR4H)
                                        ;         VR6H =  VR4L (pm3)  and  VT1[0] = 0
                                        ;   else VR6H =  VR4H (pm4)  and  VT1[0] = 1
```

The following shows code for a complete Viterbi Butterfly. The symbol || indicates an instruction executed in parallel with the previous instruction; both of these instructions are executed together in one cycle.

```
_loop:
; Loop once for each decoder input pair
   VMOV32 VR0, *XAR5++            ; Load VR0L, VR0H with input
   VITBM2 VR0                     ; VR0L = BM0    VR0H = BM1
|| VMOV32 VR2, *XAR1++            ; Load previous state metrics
; 2-cycle Viterbi butterfly
   VITDLADDSUB VR4,VR3,VR2,VR0    ; Perform add/sub
   VITLSEL VR6,VR5,VR4,VR3        ; Perform compare/select
|| VMOV32  VR2, *XAR1++           ; Previous state metrics
; 2-cycle Viterbi butterfly - Next butterfly uses CM1 in R0H
   VITDHADDSUB VR4,VR3,VR2,VR0
   VITHSEL VR6,VR5,VR4,VR3
|| VMOV32 VR2, *XAR1++
   VITDLADDSUB VR4,VR3,VR2,VR0    ; Store new state metrics
|| VMOV32 *XAR2++, VR5
   VITLSEL …… etc                 ; Continue for each state (64 for K=7)

[verify code][complete the loop here]
```

## Complex FFT example

A complex FFT requires simultaneous calculations of both the real and imaginary parts of numbers. Using the complex math capabilities of the VCU, each stage of the butterfly takes only five cycles.

```
Generic Complex FFT Butterfly Equation:
Rx' = Rx  + (Ry*Cos(n) + Iy*Sin(n))
Ix' = Ix  + (Iy*Cos(n) - Ry*Sin(n))
Ry' = Rx  - (Ry*Cos(n) + Iy*Sin(n))
Iy' = Ix  - (Iy*Cos(n) - Ry*Sin(n))
```

```
RPTB  _BUTTERFLY_LOOP,  #count
   VCMPY      VR3, VR2, VR1, VR0  ; Complex Mult w/ parallel store
|| VMOV32     *XAR3++, VR5              ; Ia':Ra'(0) = VR5
   VMOV32     *+XAR3[AR1], VR6          ; Ib':Rb'(0) = VR6
   VCDSUB16   VR6, VR4, VR3, VR2  ; Complex Sub w/ parallel load
|| VMOV32     VR0, *XAR6++              ; VR0 = COSn:SINn(1)
   VCDADD16   VR5, VR4, VR3, VR2  ; Complex Add w/ parallel load
|| VMOV32     VR4, *XAR2++              ; VR4 = Ia:Ra(2)
   VMOV32     VR1, *+XAR2[AR1]          ; VR1 = Ib:Rb(2)
_BUTTERFLY_LOOP
```

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