TMS320F2810, TMS320F2812 Digital Signal Processors

Data Manual

Literature Number: SPRS174I
April 2001 – Revised July 2003

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REVISION HISTORY

REVISION	DATE	PRODUCT STATUS	HIGHLIGHTS

I	July 2003	Advance Information	Device is now at the "TMP" stage of development (final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification)
			
			Added the following:
			– Section 3.8.1, Loss of Input Clock (p.38)
			– Section 7.12, Device Clock Table (p.80)
			– Section 7.13, Clock Requirements and Characteristics (p.81)
			  – Section titled "Input Clock Requirements" now becomes Section 7.13.1 (p.81)
			  – Section titled "Output Clock Characteristics" now becomes Section 7.13.2 (p.82)
			– Section 7.15, Event Manager Interface (p.87)
			– Section 7.16, General-Purpose Input/Output (GPIO) – Output Timings (p.91)
			– Table 7–17, General-Purpose Input Timing Requirements (p.92)
			– Figure 7–18, General-Purpose Input Timing (p.92)
			– Figure 7–25, ADC Analog Input Impedance Model (p.109)
			– Section 7.23, Flash Timings (p.117)
			
			Section 1, Features (p.1):
			– Temperature Options feature: added GHH package to –40°C to 125°C range
			
			Table 2–1, Hardware Features (p.3):
			– added Temperature Options
			– added footnotes
			
			Updated descriptions of the following signals in Table 2–2, Signal Descriptions (p.7):
			– X1/XCLKIN
			– ADCINA[7:0]
			– ADCINB[7:0]
			– GPIOF14
			
			Table 3–1, Addresses of Flash Sectors in F2812 (p.19):
			– added address ranges "0x3F 7F80" and "0x3F 7FF5"
			
			Table 3–2, Addresses of Flash Sectors in F2810 (p.19):
			– added address ranges "0x3F 7F80" and "0x3F 7FF5"
			
			Table 3–3, Wait States (p.21):
			– updated WAIT-STATES column for OTP
			– updated COMMENTS column for Flash
			
			Section 3.2.6, Flash (p.23):
			– updated CAUTION note
			
			(Continued on next page)

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REVISION	DATE	PRODUCT STATUS	HIGHLIGHTS
I (Continued)	July 2003	Advance Information	Section 3.2.10, Security (p.24): – updated first paragraph Table 3–7, Device Emulation Registers (p.29): – updated description of DEVICEID Figure 3–7, Multiplexing of Interrupts Using the PIE Block (p.33): – added PIEACKx Table 3–12, PLL, Clocking, Watchdog, and Low-Power Mode Registers (p.36): – updated footnote about PLLCR Section 3.8, OSC and PLL Block (p.37): – changed “The logic-high level in this case should not exceed 1.8 V.” to “The logic-high level in this case should not exceed V_{DD}.” Figure 3–10b, Recommended Crystal / Clock Connection (p.38): – changed “Toggling 0–1.8 V” to “Toggling 0–V_{DD}” Figure 3–11, Watchdog Module (p.39): – changed “Pull-up” to “Internal Pullup” Table 3–15, F2810 and F2812 Low-Power Modes (p.40): – added “Debugger[§]” to the EXIT column of the IDLE mode Section 3.12, Low-Power Modes Block (p.40): – IDLE Mode: changed “LPMCR(LPM) bits” to “LPMCR0(LPM) bits” Section 4.2.7, Capture Unit (p.48): – added feature about capture pins Section 4.2.8, Quadrature-Encoder Pulse (QEP) Circuit (p.49): – revised “With EXTCON register bits, ...” paragraph Section 4.4, Enhanced Controller Area Network (eCAN) Module (p.53): – added note about smallest bit rate possible Section 4.8, GPIO Mux (p.67): – replaced NOTE about input function of the GPIO pin with a CAUTION note Figure 4–11, Modes of Operation (p.69): – updated drawing – updated footnote about GPxDAT Section 5, Development Support (p.70): – updated Hardware Development Tools list Updated Figure 5–1, TMS320x28x Device Nomenclature (p.71) (Continued on next page)

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REVISION	DATE	PRODUCT STATUS	HIGHLIGHTS
I (Continued)	July 2003	Advance Information	Section 7.1, Absolute Maximum Ratings (p.73): – added V_{DDAIO} to “Supply voltage range, V_{DDIO}, V_{DDA1}, V_{DDA2}, and $AV_{DDREFBG}$” – added V_{DD1} to “Supply voltage range, V_{DD}” – added GHH package to S version of “Operating case temperature ranges, T_C” – added footnote reference to “Operating case temperature ranges, T_C” Section 7.2, Recommended Operating Conditions (p.73): – added V_{DD1} to “Device supply voltage, CPU” – added V_{DDAIO} to “ADC supply voltage” – split V_{IH} into two rows: “All inputs except XCLKIN” and “XCLKIN (@ 50 µA max)” – split V_{IL} into two rows: “All inputs except XCLKIN” and “XCLKIN (@ 50 µA max)” – moved N_f and N_{OTP} to Section 7.23.1, Recommended Operating Conditions – added V_{DDAIO} to footnote about power sequencing Section 7.4, Current Consumption by Power-Supply Pins Over Recommended Operating Conditions During Low-Power Modes at 150-MHz SYSCLKOUT (p.74): – updated table – added CAUTION note about HALT and STANDBY modes Section 7.5, Power Sequencing Requirements (p.75): – Option 2: added V_{DDAIO} to “(V_{DDIO}, V_{DD3VFL}, V_{DDA1}/V_{DDA2}/$AV_{DDREFBG}$)” Figure 7–1, F2812/F2810 Typical Power-Up and Power-Down Sequence – Option 2 (p.76): – updated footnote D – added footnote E Figure 7–2, F2812/F2810 Typical Current Consumption (With Peripheral Clocks Enabled) (p.77): – updated graph – added footnotes Updated Table 7–2, Typical Current Consumption by Various Peripherals (at 150 MHz) (p.77) Section 7.8, Signal Transition Levels (p.78): – first paragraph: replaced “to a maximum logic-low level of 0.8 V” with “to a maximum logic-low level of 0.4 V” – added NOTE about referencing individual timing diagrams Figure 7–5, 3.3-V Test Load Circuit (p.79): – replaced diagram Table 7–3, TMS320F2812 Clock Table and Nomenclature (p.80): – changed MAX $t_{c(LCO)}$ from 150 MHz to 75 MHz (Continued on next page)

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I (Continued)	July 2003	Advance Information	Updated Table 7–5, XCLKIN Timing Requirements – PLL Bypassed or Enabled (p.81) Updated Table 7–6, XCLKIN Timing Requirements – PLL Disabled (p.81) Table 7–8, XCLKOUT Switching Characteristics (PLL Bypassed or Enabled) (p.82): – deleted footnote about $t_{c(CI)}$ approaching ∞ – added "H = 0.5$t_{c(XCO)}$" footnote Updated Table 7–9, Reset ($\overline{XRS}$) Timing Requirements (p.83) Figure 7–7, Power-on Reset in Microcomputer Mode (XMP/$\overline{MC}$ = 0) (p.84): – updated figure – added footnote explaining why XCLKOUT = XCLKIN/8 – added footnote about the state of the GPIO pins Figure 7–8, Power-on Reset in Microprocessor Mode (XMP/$\overline{MC}$ = 1) (p.85): – updated figure – added footnote explaining why XCLKOUT = XCLKIN/8 – added footnote about the state of the GPIO pins Figure 7–9, Warm Reset in Microcomputer Mode (p.86): – added $t_{su(XPLLDIS)}$ parameter Figure 7–17, GPIO Input Qualifier – Example Diagram for QUALPRD = 1 (p.92): – updated footnote B Table 7–18, SPI Master Mode External Timings (Clock Phase = 0) (p.93): – added NOTE about internal clock prescalars Table 7–19, SPI Master Mode External Timings (Clock Phase = 1) (p.95): – added NOTE about internal clock prescalars Table 7–23, External Memory Interface Read Switching Characteristics for XCLKOUT = XTIMCLK (p.103): – updated table – revised footnote about timings for XCLKOUT = 1/2 XTIMCLK (Continued on next page)

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I (Continued)	July 2003	Advance Information	Table 7–24, External Memory Interface Read Timing Requirements (p.103): – deleted “TBD” from MIN $t_{a(A)}$ – deleted footnote about design simulation models – revised footnote with table reference Updated Figure 7–23, Example Read Access (p.104) Table 7–25, External Memory Interface Write Switching Characteristics for XCLKOUT = XTIMCLK (p.105): – updated table – revised footnote about timings for XCLKOUT = 1/2 XTIMCLK – revised footnote with table reference Updated Figure 7–24, Example Write Access (p.106) Table 7–26, DC Specifications (p.108): – updated table – added footnote about 12.5-MHz ADCCLK – added footnote about the SYSCLKOUT value and the ADC clock value Table 7–27 (p.109): – changed title from “AC Specifications” to “AC Specifications (PRELIMINARY DATA)” – revised footnote Section 7.21.3 (p.109): – changed title from “Current Consumption for Different ADC Configurations” to “Current Consumption for Different ADC Configurations (at 25-MHz ADCCLK)” – updated table Figure 7–27, Sequential Sampling Mode (Single-Channel) Timings (p.111): – corrected ADC Event Trigger waveform Table 7–31, McBSP Timing Requirements (p.114): – updated table – revised footnotes Table 7–32, McBSP Switching Characteristics (p.115): – updated table – revised “P = 1/CLKG in ns” footnote Removed information is available in Reference Guides

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H	March 2003	Advance Information	Section 1, Features
			– added package information to the Temperature Options feature
			
			Updated the descriptions of the following signals in Table 2–2, Signal Descriptions:
			– X1/XCLKIN, XCLKOUT, TESTSEL, $\overline{XRS}$, TEST1, TEST2, ADCREFM, ADCBGREFIN, V_{DD}, GPIOF14
			
			Table 2–2, Signal Descriptions
			– updated footnote about typical drive strength
			
			Updated the following sections:
			– Section 3.2.19, 32-Bit CPU-Timers (0, 1, 2)
			– Section 3.9, PLL-Based Clock Module:
			  – replaced “4096 XCLKIN cycles” with “131 072 XCLKIN cycles”
			– Section 3.12, Low-Power Modes Block
			  – added note about state of output pins
			– Section 4.2, Event Manager Modules (EVA, EVB)
			– Section 4.2.3, Programmable Deadband Generator
			– Section 4.3, Enhanced Analog-to-Digital Converter (ADC) Module
			  – in paragraph starting with “To obtain the specified accuracy of the ADC, proper ...”, changed “the ADC module power pins (such as V_{CCA}, V_{REFHI}, and V_{SSA})” to “the ADC module power pins (V_{DDA1}/V_{DDA2}, $AV_{DDREFBG}$)”
			– Section 4.8, GPIO Mux
			  – added note below Figure 4–11, Modes of Operation
			– Section 5, Development Support
			– Section 6, Documentation Support
			– Section 7.1, Absolute Maximum Ratings
			  – added $AV_{DDREFBG}$ to “Supply voltage range”
			  – changed “Operating free-air temperature ranges, T_A” to “Operating case temperature ranges, T_C”
			  – added package information to “Operating case temperature ranges, T_C”
			  – added footnote about long-term high-temperature storage and/or extended use at maximum recommended operating conditions
			– Section 7.2, Recommended Operating Conditions
			  – removed 0 V from the MIN and MAX columns of V_{SS}
			  – added $AV_{DDREFBG}$ to “ADC supply voltage”
			  – changed “T_A, Free-air temperature” to “T_C, Case temperature”
			  – revised † and ‡ footnotes
			– Section 7.3, Electrical Characteristics Over Recommended Operating Conditions
			– Section 7.4, Current Consumption by Power-Supply Pins Over Recommended Operating Conditions During Low-Power Modes at 150-MHz SYSCLKOUT
			  – revised footnote
			
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H (Continued)	March 2003	Advance Information	Updated the following sections:
			– Section 7.5, Power Sequencing Requirements:
			  – Option 1: changed V_{DDA1}/V_{DDA2} to $V_{DDA1}/V_{DDA2}/AV_{DDREFBG}$
			  – Option 2: changed V_{DDA1}/V_{DDA} to $V_{DDA1}/V_{DDA2}/AV_{DDREFBGBG}$
			  – Power-Down Sequencing: changed “(8 µs, typical)” to “(8 µs, minimum)”
			– Section 7.18.1, Absolute Maximum Ratings
			  – added $AV_{DDREFBG}$ to supply voltage range
			  – added footnote about diode clamp protection
			– Section 7.18.3, Current Consumption for Different ADC Configurations
			  – added footnote defining I_{DDA}
			– Section 7.18.5.1, Reference Voltage
			  – replaced “VREFP” with “ADCVREFP”
			  – replaced “VREFM” with “ADCVREFM”
			
			Updated the following figures:
			– Figure 3–2, F2812 Memory Map
			  – changed “0x00 1000” to “0x00 0E00”
			– Figure 3–3, F2810 Memory Map
			  – changed “0x00 1000” to “0x00 0E00”
			– Figure 3–13, Watchdog Module
			  – added $\overline{WDRST}$ and removed note about silicon revision implementation
			  – revised footnote about $\overline{WDRST}$ signal
			– Figure 4–2, CPU-Timer Interrupts Signals and Output Signal:
			  – updated CPU-Timer 1 block
			– Figure 4–11, Modes of Operation
			  – deleted the Pre-Scale block
			  – revised footnote about qualification of selected input signals
			– Figure 7–7, Power-on Reset in Microcomputer Mode (XMP/$\overline{MC}$ = 0)
			  – added footnote defining V_{DDAn}
			– Figure 7–10, Effect of Writing Into PLLCR Register
			  – replaced “4096 XCLKIN Cycles” with “131 072 XCLKIN Cycles”
			  – revised footnote
			
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H
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	March 2003	Advance Information	Updated the following tables:
			– Table 3–7, Device Emulation Registers
			– Table 3–9, DEVICEID Register Bit Definitions
			– Table 3–16, Interrupt Vector Table Mapping
			– Table 7–7, XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)
			  – changed MAX t_p from 4096$t_{c(CI)}$ ns to 131 072$t_{c(CI)}$ ns
			  – revised footnote about future silicon revisions
			– Table 7–17, DC Specifications:
			  – deleted TEST CONDITIONS column
			  – changed “Accuracy, V_{REFP}” to “Accuracy, $ADCV_{REFP}$”
			  – changed “Accuracy, V_{REFM}” to “Accuracy, $ADCV_{REFM}$”
			  – added MIN and MAX values for “Input voltage difference, ADCREFP – ADCREFM”
			  – added footnote about internal band gap reference
			– Table 7–19, ADC Power-Up Delays:
			  – changed MIN and TYP values of both parameters
			
			Added the following:
			– Section 7.18.4, ADC Power-Up Control Bit Timing
			– Figure 7–1, F2812/F2810 Typical Power-Up and Power-Down Sequence – Option 2
			– Table 8–1, Thermal Resistance Characteristics for 179-GHH
			– Table 8–2, Thermal Resistance Characteristics for 176-PGF
			– Table 8–3, Thermal Resistance Characteristics for 128-PBK
			
			Removed the following section (section number is that in Revision G):
			– Section 3.11.1, Emulation Considerations
			
			Removed the following tables (table numbers are those in Revision G):
			– Table 3–35, WDCNTR Register Bit Definitions
			– Table 3–36, WDKEY Register Bit Definitions
			– Table 3–37, WDCR Register Bit Definitions
			– Table 4–11, EXTCONA Register Bit Definitions

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REVISION	DATE	PRODUCT STATUS	HIGHLIGHTS
G	January 2003	Advance Information	Converted Data Sheet to Data Manual format. Added electrical characteristic data. Document product status is now Advance Information. Updated descriptions of the following signals in Table 2–2, Signal Descriptions: – X1/XCLKIN, XCLKOUT, ADCREFP, ADCREFM, V_{DDAIO}, V_{SSAIO}, V_{DD3VFL}, GPIOF14 Updated footnote about drive strength in Table 2–2, Signal Descriptions. Updated Figure 3–1, Functional Block Diagram. Updated Figure 3–2, F2812 Memory Map. Updated Figure 3–3, F2810 Memory Map. Updated Table 3–3, Wait States. Updated the following sections: – Section 1, Features: – ADC – Section 2.4, Signal Descriptions – Section 3.2.6, Flash – Section 3.2.10, Security – Section 3.5.1, Timing Registers – Section 3.6.2, PIE Vector Map – Section 3.8, OSC and PLL Block – Section 3.9, PLL-Based Clock Module – Section 3.10, External Reference Oscillator Clock Option – Section 4.3, Enhanced Analog-to-Digital Converter (ADC) Module – Section 4.5, Multichannel Buffered Serial Port (McBSP) Module – Section 4.6, Serial Communications Interface (SCI) Module – Section 4.7, Serial Peripheral Interface (SPI) Module – Section 4.8, GPIO Mux – Section 5, Development Support – Section 7.1, Absolute Maximum Ratings – Section 7.2, Recommended Operating Conditions – Section 7.3, Electrical Characteristics Over Recommended Operating Free-Air Temperature Ranges – Section 7.5, Power Sequencing Requirements (Continued on next page)

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G (Continued)	January 2003	Advance Information	Removed the following sections: – Section 3.5.2, XINTCNF2 Register – Section 3.5.3, XBANK Register Updated description of REVID in Table 3–9, DEVICEID Register Bit Definitions. Updated Table 3–18, PIE Vector Table. Updated type and description of the PIEACK bit in Table 3–21, PIEACK Register Bit Definitions. Updated description of the LSPCLK bit in Table 3–32, LOSPCP Register Bit Definitions. Updated Figure 3–11, OSC and PLL Block. Updated Figure 3–12, Recommended Crystal / Clock Connection. Updated Table 3–28, PLL, Clocking, Watchdog, and Low-Power Mode Registers. Updated description of the WDOVERRIDE bit in Table 3–30, SCSR Register Bit Definitions. Updated description of the HSPCLK bit in Table 3–31, HISPCP Register Bit Definitions. Added Table 3–34, Possible PLL Configuration Modes. Updated Figure 3–13, Watchdog Module. Updated Table 3–37, WDCR Register Bit Definitions. Updated Figure 4–5, ADC Pin Connections (Preliminary). Added Table 4–13, 3.3-V eCAN Transceivers for the TMS320F28x DSPs. Updated Table 4–12, ADC Registers. Updated Figure 4–7, eCAN Memory Map. Updated Table 4–18, SPI Registers. Updated Table 4–22, GPAQUAL Register Bit Definitions. Updated Table 4–29, GPFMUX, GPFDIR Register Bit Defintions.

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1 Features

- High-Performance Static CMOS Technology
  - 150 MHz (6.67-ns Cycle Time)
  - Low-Power (1.8-V Core, 3.3-V I/O) Design
  - 3.3-V Flash Programming Voltage
- JTAG Boundary Scan Support†
- High-Performance 32-Bit CPU (TMS320C28x)
  - 16 x 16 and 32 x 32 MAC Operations
  - 16 x 16 Dual MAC
  - Harvard Bus Architecture
  - Atomic Operations
  - Fast Interrupt Response and Processing
  - Unified Memory Programming Model
  - 4M Linear Program Address Reach
  - 4M Linear Data Address Reach
  - Code-Efficient (in C/C++ and Assembly)
  - TMS320F24x/LF240x Processor Source Code Compatible
- On-Chip Memory
  - Up to 128K x 16 Flash (Four 8K x 16 and Six 16K x 16 Sectors)
  - 1K x 16 OTP ROM
  - L0 and L1: 2 Blocks of 4K x 16 Each Single-Access RAM (SARAM)
  - H0: 1 Block of 8K x 16 SARAM
  - M0 and M1: 2 Blocks of 1K x 16 Each SARAM
- Boot ROM (4K x 16)
  - With Software Boot Modes
  - Standard Math Tables
- External Interface (F2812)
  - Up to 1M Total Memory
  - Programmable Wait States
  - Programmable Read/Write Strobe Timing
  - Three Individual Chip Selects
- Clock and System Control
  - Dynamic PLL Ratio Changes Supported
  - On-Chip Oscillator
  - Watchdog Timer Module
- Three External Interrupts
- Peripheral Interrupt Expansion (PIE) Block That Supports 45 Peripheral Interrupts
- 128-Bit Security Key/Lock
  - Protects Flash/OTP and L0/L1 SARAM
  - Prevents Firmware Reverse Engineering
- Three 32-Bit CPU-Timers
- Motor Control Peripherals
  - Two Event Managers (EVA, EVB)
  - Compatible to 240xA Devices
- Serial Port Peripherals
  - Serial Peripheral Interface (SPI)
  - Two Serial Communications Interfaces (SCIs), Standard UART
  - Enhanced Controller Area Network (eCAN)
  - Multichannel Buffered Serial Port (McBSP) With SPI Mode
- 12-Bit ADC, 16 Channels
  - 2 x 8 Channel Input Multiplexer
  - Two Sample-and-Hold
  - Single/Simultaneous Conversions
  - Fast Conversion Rate: 80 ns/12.5 MSPS
- Up to 56 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins
- Advanced Emulation Features
  - Analysis and Breakpoint Functions
  - Real-Time Debug via Hardware
- Development Tools Include
  - ANSI C/C++ Compiler/Assembler/Linker
  - Supports TMS320C24x™/240x Instructions
  - Code Composer Studio™ IDE
  - DSP/BIOS™
  - JTAG Scan Controllers† [Texas Instruments (TI) or Third-Party]
  - Evaluation Modules
  - Broad Third-Party Digital Motor Control Support
- Low-Power Modes and Power Savings
  - IDLE, STANDBY, HALT Modes Supported
  - Disable Individual Peripheral Clocks
- Package Options
  - 179-Ball MicroStar BGA™ With External Memory Interface (GHH) (F2812)
  - 176-Pin Low-Profile Quad Flatpack (LQFP) With External Memory Interface (PGF) (F2812)
  - 128-Pin LQFP Without External Memory Interface (PBK) (F2810)
- Temperature Options:
  - A: –40°C to 85°C (GHH, PGF, PBK)
  - S: –40°C to 125°C (GHH, PGF, PBK)

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† IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port

2 Introduction

This section provides a summary of each device's features, lists the pin assignments, and describes the function of each pin. This document also provides detailed descriptions of peripherals, electrical specifications, parameter measurement information, and mechanical data about the available packaging.

2.1 Description

The TMS320F2810 and TMS320F2812 devices, members of the TMS320C28x™ DSP generation, are highly integrated, high-performance solutions for demanding control applications. The functional blocks and the memory maps are described in Section 3, Functional Overview.

Throughout this document, TMS320F2810 and TMS320F2812 are abbreviated as F2810 and F2812, respectively.

ADVANCE INFORMATION

2.2 Device Summary

Table 2–1 provides a summary of each device's features.

Table 2–1. Hardware Features†

FEATURE		F2810	F2812
Instruction Cycle (at 150 MHz)		6.67 ns	6.67 ns
Single-Access RAM (SARAM) (16-bit word)		18K	18K
3.3-V On-Chip Flash (16-bit word)		64K	128K
Code Security for On-Chip Flash/SARAM		Yes	Yes
Boot ROM		Yes	Yes
OTP ROM		Yes	Yes
External Memory Interface		—	Yes
Event Managers A and B (EVA and EVB)		EVA, EVB	EVA, EVB
• General-Purpose (GP) Timers		4	4
• Compare (CMP)/PWM		16	16
• Capture (CAP)/QEP Channels		6/2	6/2
Watchdog Timer		Yes	Yes
12-Bit ADC		Yes	Yes
• Channels		16	16
32-Bit CPU Timers		3	3
SPI		Yes	Yes
SCIA, SCIB		SCIA, SCIB	SCIA, SCIB
CAN		Yes	Yes
McBSP		Yes	Yes
Digital I/O Pins (Shared)		56	56
External Interrupts		3	3
Supply Voltage		1.8-V Core, 3.3-V I/O	1.8-V Core, 3.3-V I/O
Packaging		128-pin PBK	179-ball GHH 176-pin PGF
Temperature Options‡	A: –40°C to 85°C	PBK	PGF and GHH
	S: –40°C to 125°C	Available at TMS only	Available at TMS only
Product Status:§ Product Preview (PP) Advance Information (AI) Production Data (PD)		AI (TMP¶)	AI (TMP¶)

† The errata for this silicon, *TMS320F2810 and TMS320F2812 Digital Signal Processors Silicon Errata* (literature number SPRZ193), has been posted on the Texas Instruments (TI) website. It will be updated as needed.
‡ "S" temperature option (–40°C to 125°C) characterization data will be available at TMS.
§ PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.
ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.
¶ TMP: Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

ADVANCE INFORMATION

2.3 Pin Assignments

Figure 2–1 illustrates the ball locations for the 179-ball GHH ball grid array (BGA) package. Figure 2–2 shows the pin assignments for the 176-pin PGF low-profile quad flatpack (LQFP) and Figure 2–3 shows the pin assignments for the 128-pin PBK LQFP. Table 2–2 describes the function(s) of each pin.

2.3.1 Terminal Assignments for the GHH Package

See Table 2–2 for a description of each terminal's function(s).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	$\overline{XZCS0AND1}$	PWM8	PWM10	V_{SS}	V_{DD}	CAP6_QEPI2	XD[8]	V_{SS}	V_{DD}	$\overline{T3CTRIP}$_$\overline{PDPINTB}$	$\overline{T4CTRIP}$/EVBSOC	V_{DD}	$\overline{XZCS2}$	SCITXDB
N	SPISOMIA	PWM7	PWM9	XR/$\overline{W}$	T4PWM_T4CMP	$\overline{C4TRIP}$	TEST2	V_{DD3VFL}	XD[11]	XA[2]	$\overline{XWE}$	CANTXA	CANRXA	V_{DDIO}
M	SPISIMOA	XA[1]	$\overline{XRD}$	PWM12	CAP4_QEP3	CAP5_QEP4	TEST1	XD[9]	X2	V_{SS}	XA[3]	PWM1	SCIRXDB	PWM2
L	V_{DD}	V_{SS}	XD[6]	PWM11	XD[7]	$\overline{C5TRIP}$	V_{DDIO}	TDIRB	XD[10]	V_{DDIO}	V_{SS}	PWM3	PWM4	XD[12]
K	V_{SS}	SPICLKA	XD[4]	SPISTEA	T3PWM_T3CMP	V_{SS}	$\overline{C6TRIP}$	TCLKINB	X1/XCLKIN	$\overline{XHOLDA}$	PWM5	V_{DD}	V_{SS}	PWM6
J	MCLKXA	MFSRA	XD[3]	V_{DDIO}	XD[5]					XD[13]	T1PWM_T1CMP	XA[4]	T2PWM_T2CMP	V_{SS}
H	V_{DD}	MCLKRA	XD[1]	MFSXA	XD[2]					CAP1_QEP1	CAP2_QEP2	CAP3_QEPI1	XA[5]	$\overline{T1CTRIP}$_$\overline{PDPINTA}$
G	MDXA	MDRA	XD[0]	V_{SS}	XA[0]					$\overline{T2CTRIP}$/EVASOC	V_{DDIO}	V_{DD}	V_{SS}	XA[6]
F	XMP/$\overline{MC}$	ADC-RESEXT	V_{SSA1}	V_{DDA1}	ADCINB7					$\overline{C3TRIP}$	XCLKOUT	XA[7]	TCLKINA	TDIRA
E	AVDD-REFBG	ADCREFP	AVSS-REFBG	ADCREFM	ADCINA5	ADC-BGREFIN	$\overline{XHOLD}$	XNMI_XINT13	V_{DDIO}	XA[13]	$\overline{C2TRIP}$	XA[8]	$\overline{C1TRIP}$	V_{SS}
D	ADCINB6	ADCINB5	ADCINB4	ADCINA1	ADCINA6	$\overline{XRS}$	XA[18]	XINT2_ADCSOC	XINT1_$\overline{XBIO}$	V_{SS}	EMU0	TDO	TMS	XA[9]
C	ADCINB3	ADCINB0	ADCINB1	ADCINA2	V_{SSA2}	V_{SS1}	SCITXDA	V_{DD}	EMU1	V_{SS}	XA[12]	XA[10]	TDI	V_{DD}
B	ADCINB2	V_{DDAIO}	ADCLO	ADCINA3	ADCINA7	XREADY	XA[17]	V_{SS}	XA[15]	V_{DD}	XD[14]	$\overline{TRST}$	$\overline{XZCS6AND7}$	V_{SS}
A		V_{SSAIO}	ADCINA0	ADCINA4	V_{DDA2}	V_{DD1}	SCIRXDA	XA[16]	XD[15]	XA[14]	XF_$\overline{XPLLDIS}$	TCK	TESTSEL	XA[11]

Figure 2–1. TMS320F2812 179-Ball GHH MicroStar BGA™ (Bottom View)

2.3.2 Pin Assignments for the PGF Package

The TMS320F2812 176-pin PGF low-profile quad flatpack (LQFP) pin assignments are shown in Figure 2–2. See Table 2–2 for a description of each pin's function(s).

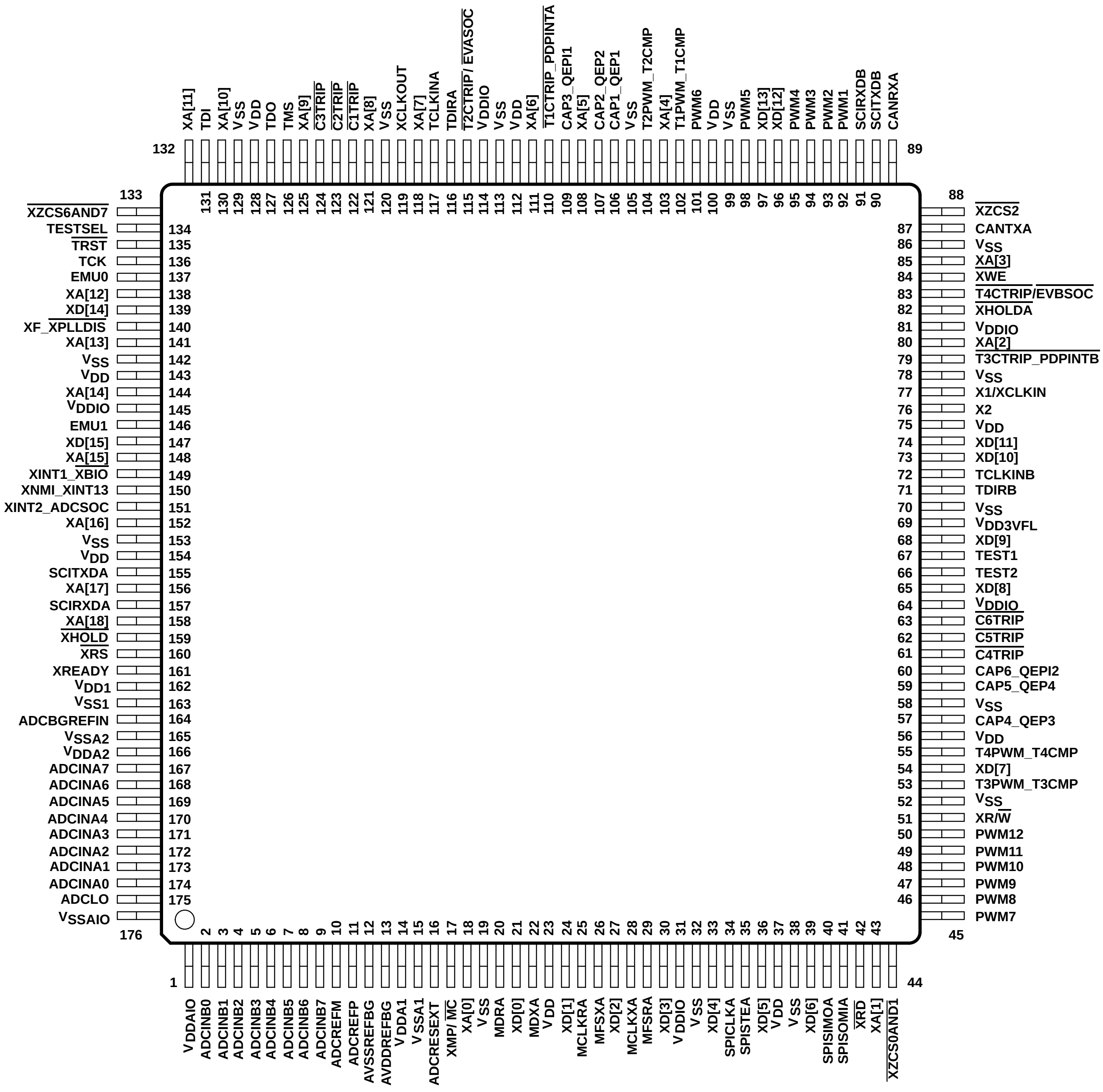

Figure 2–2. TMS320F2812 176-Pin PGF LQFP (Top View)

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2.3.3 Pin Assignments for the PBK Package

The TMS320F2810 128-pin PBK low-profile quad flatpack (LQFP) pin assignments are shown in Figure 2–3. See Table 2–2 for a description of each pin's function(s).

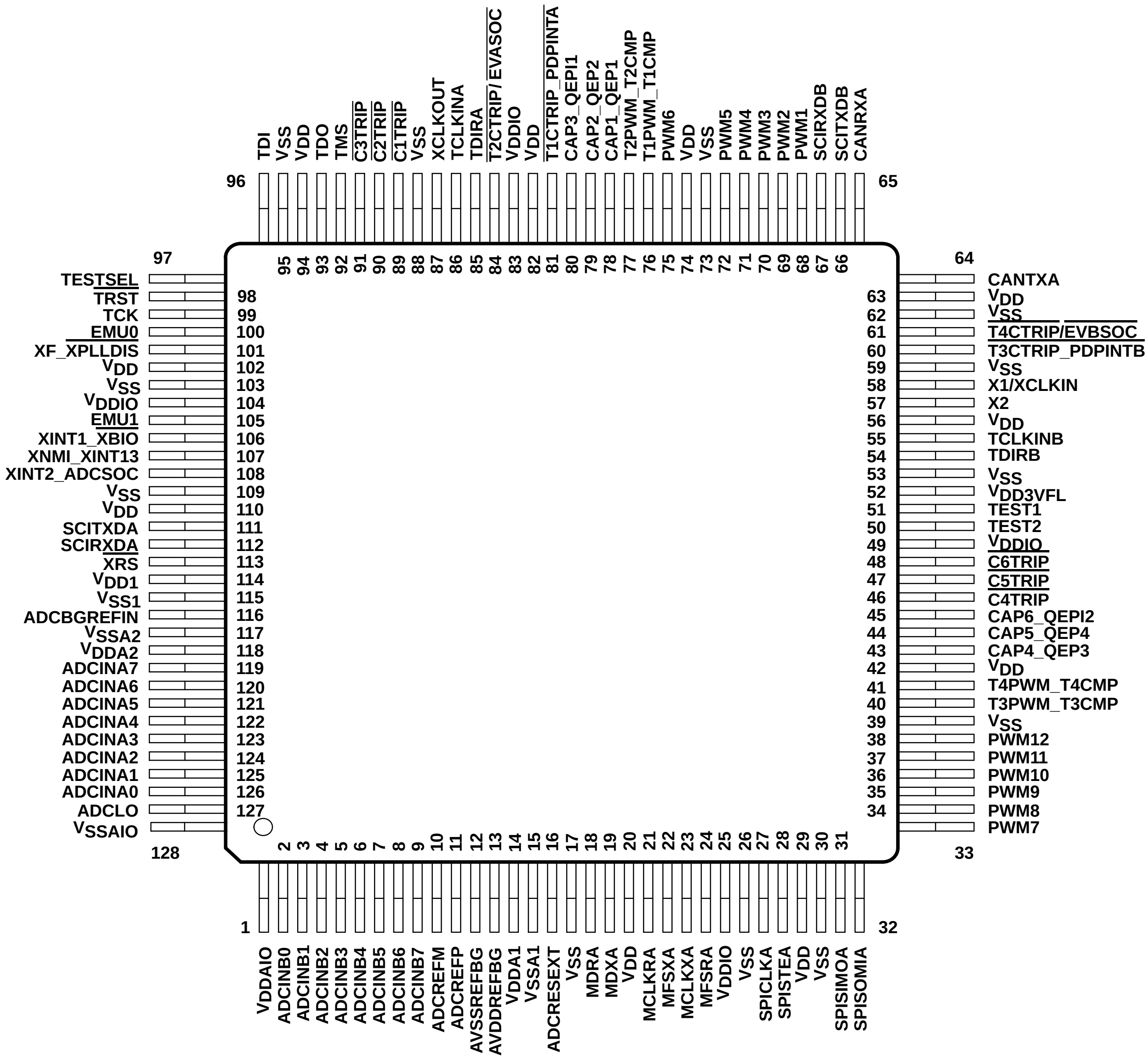

Figure 2–3. TMS320F2810 128-Pin PBK LQFP (Top View)

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2.4 Signal Descriptions

Table 2–2 specifies the signals on the F2810 and F2812 devices. All digital inputs are TTL-compatible. All outputs are 3.3 V with CMOS levels. Inputs are not 5-V tolerant. A 100-µA (or 20-µA) pullup/pulldown is used.

Table 2–2. Signal Descriptions†

NAME	PIN NO.			I/O/Z‡	PU/PD§	DESCRIPTION
	179-PIN GHH	176-PIN PGF	128-PIN PBK			
XINTF SIGNALS (F2812 ONLY)						
XA[18]	D7	158	–	O/Z	–	19-bit XINTF Address Bus
XA[17]	B7	156	–	O/Z	–	
XA[16]	A8	152	–	O/Z	–	
XA[15]	B9	148	–	O/Z	–	
XA[14]	A10	144	–	O/Z	–	
XA[13]	E10	141	–	O/Z	–	
XA[12]	C11	138	–	O/Z	–	
XA[11]	A14	132	–	O/Z		
XA[10]	C12	130	–	O/Z	–	
XA[9]	D14	125	–	O/Z	–	
XA[8]	E12	121	–	O/Z	–	
XA[7]	F12	118	–	O/Z	–	
XA[6]	G14	111	–	O/Z	–	
XA[5]	H13	108	–	O/Z	–	
XA[4]	J12	103	–	O/Z	–	
XA[3]	M11	85	–	O/Z	–	
XA[2]	N10	80	–	O/Z	–	
XA[1]	M2	43	–	O/Z	–	
XA[0]	G5	18	–	O/Z		
XD[15]	A9	147	–	I/O/Z	PU	16-bit XINTF Data Bus
XD[14]	B11	139	–	I/O/Z	PU	
XD[13]	J10	97	–	I/O/Z	PU	
XD[12]	L14	96	–	I/O/Z	PU	
XD[11]	N9	74	–	I/O/Z	PU	
XD[10]	L9	73	–	I/O/Z	PU	
XD[9]	M8	68	–	I/O/Z	PU	
XD[8]	P7	65	–	I/O/Z	PU	
XD[7]	L5	54	–	I/O/Z	PU	
XD[6]	L3	39	–	I/O/Z	PU	
XD[5]	J5	36	–	I/O/Z	PU	
XD[4]	K3	33	–	I/O/Z	PU	
XD[3]	J3	30	–	I/O/Z	PU	
XD[2]	H5	27	–	I/O/Z	PU	
XD[1]	H3	24	–	I/O/Z	PU	
XD[0]	G3	21	–	I/O/Z	PU	

† Typical drive strength of the output buffer for all pins [except TDO, XCLKOUT, XF, XINTF, EMU0, and EMU1 pins] is 4 mA typical.
‡ I = Input, O = Output, Z = High impedance
§ PU = pin has internal pullup; PD = pin has internal pulldown

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Table 2–2. Signal Descriptions† (Continued)

NAME	PIN NO.			I/O/Z‡	PU/PD§	DESCRIPTION
	179-PIN GHH	176-PIN PGF	128-PIN PBK			
XINTF SIGNALS (F2812 ONLY) (CONTINUED)						
XMP/$\overline{MC}$	F1	17	–	I	PD	Microprocessor/Microcomputer Mode Select. Switches between microprocessor and microcomputer mode. When high, Zone 7 is enabled on the external interface. When low, Zone 7 is disabled from the external interface, and on-chip boot ROM may be accessed instead. This signal is latched into the XINTCNF2 register on a reset and the user can modify this bit in software. The state of the XMP/$\overline{MC}$ pin is ignored after reset.
$\overline{XHOLD}$	E7	159	–	I	PU	External DMA Hold Request. $\overline{XHOLD}$, when active (low), requests the XINTF to release the external bus and place all buses and strobes into a high-impedance state. The XINTF will release the bus when any current access is complete and there are no pending accesses on the XINTF. This signal is an asynchronous input and is synchronized by XTIMCLK.
$\overline{XHOLDA}$	K10	82	–	O/Z	–	External DMA Hold Acknowledge. $\overline{XHOLDA}$ is driven active (low) when the XINTF has granted a $\overline{XHOLD}$ request. All XINTF buses and strobe signals will be in a high-impedance state. $\overline{XHOLDA}$ is released when the $\overline{XHOLD}$ signal is released. External devices should only drive the external bus when $\overline{XHOLDA}$ is active (low).
$\overline{XZCS0AND1}$	P1	44	–	O/Z	–	XINTF Zone 0 and Zone 1 Chip Select. $\overline{XZCS0AND1}$ is active (low) when an access to the XINTF Zone 0 or Zone 1 is performed.
$\overline{XZCS2}$	P13	88	–	O/Z	–	XINTF Zone 2 Chip Select. $\overline{XZCS2}$ is active (low) when an access to the XINTF Zone 2 is performed.
$\overline{XZCS6AND7}$	B13	133	–	O/Z	–	XINTF Zone 6 and Zone 7 Chip Select. $\overline{XZCS6AND7}$ is active (low) when an access to the XINTF Zone 6 or Zone 7 is performed.
$\overline{XWE}$	N11	84	–	O/Z	–	Write Enable. Active-low write strobe. The write strobe waveform is specified, per zone basis, by the Lead, Active, and Trail periods in the XTIMINGx registers.
$\overline{XRD}$	M3	42	–	O/Z	–	Read Enable. Active-low read strobe. The read strobe waveform is specified, per zone basis, by the Lead, Active, and Trail periods in the XTIMINGx registers. NOTE: The $\overline{XRD}$ and $\overline{XWE}$ signals are mutually exclusive.
XR/$\overline{W}$	N4	51	–	O/Z	–	Read Not Write Strobe. Normally held high. When low, XR/$\overline{W}$ indicates write cycle is active; when high, XR/$\overline{W}$ indicates read cycle is active.

† Typical drive strength of the output buffer for all pins [except TDO, XCLKOUT, XF, XINTF, EMU0, and EMU1 pins] is 4 mA typical.
‡ I = Input, O = Output, Z = High impedance
§ PU = pin has internal pullup; PD = pin has internal pulldown

Table 2–2. Signal Descriptions† (Continued)

NAME	PIN NO. 179-PIN GHH	PIN NO. 176-PIN PGF	PIN NO. 128-PIN PBK	I/O/Z‡	PU/PD§	DESCRIPTION
XINTF SIGNALS (F2812 ONLY) (CONTINUED)						
XREADY	B6	161	–	I	PU	Input Ready Signal. Indicates peripheral is ready to complete the access when asserted to 1. XREADY can be configured to be a synchronous or an asynchronous input. In synchronous mode, the XINTF interface block will require XREADY to be valid one XTIMCLK clock cycle before the end of the active period. In asynchronous mode, the XINTF interface block will sample XREADY three XTIMCLK clock cycles before the end of the active period. XREADY is sampled at the XTIMCLK rate independent of the XCLKOUT mode.
JTAG AND MISCELLANEOUS SIGNALS						
X1/XCLKIN	K9	77	58	I		Oscillator Input – input of the internal oscillator. This pin is also used to feed an external clock. The 28x can be operated with an external clock source, provided that the proper voltage levels be driven on the X1/XCLKIN pin. It should be noted that the X1/XCLKIN pin is referenced to the 1.8-V core digital power supply (V_{DD}), rather than the 3.3-V I/O supply (V_{DDIO}). A clamping diode may be used to clamp a buffered clock signal to ensure that the logic-high level does not exceed V_{DD} (1.8 V or 1.9 V) or a 1.8-V oscillator may be used.
X2	M9	76	57	I		Oscillator Output
XCLKOUT	F11	119	87	O	–	Single output clock derived from SYSCLKOUT to be used for on-chip and off-chip wait-state generation and as a general-purpose clock source. XCLKOUT is either the same frequency, 1/2 the frequency, or 1/4 the frequency of SYSCLKOUT. At reset, XCLKOUT = SYSCLKOUT/4.
TESTSEL	A13	134	97	I	PD	Test Pin. Reserved for TI. Must be connected to ground.
$\overline{\text{XRS}}$	D6	160	113	I/O	PU	Device Reset (in) and Watchdog Reset (out). Device reset. $\overline{\text{XRS}}$ causes the device to terminate execution. The PC will point to the address contained at the location 0x3FFFC0. When $\overline{\text{XRS}}$ is brought to a high level, execution begins at the location pointed to by the PC. This pin is driven low by the DSP when a watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin will be driven low for the watchdog reset duration of 512 XCLKIN cycles. The output buffer of this pin is an open-drain with an internal pullup (100 µA, typical). It is recommended that this pin be driven by an open-drain device.
TEST1	M7	67	51	I/O	–	Test Pin. Reserved for TI. Must be left unconnected.
TEST2	N7	66	50	I/O	–	Test Pin. Reserved for TI. Must be left unconnected.

† Typical drive strength of the output buffer for all pins [except TDO, XCLKOUT, XF, XINTF, EMU0, and EMU1 pins] is 4 mA typical.
‡ I = Input, O = Output, Z = High impedance
§ PU = pin has internal pullup; PD = pin has internal pulldown

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Table 2–2. Signal Descriptions[†] (Continued)

NAME	PIN NO.			I/O/Z[‡]	PU/PD[§]	DESCRIPTION
	179-PIN GHH	176-PIN PGF	128-PIN PBK			
JTAG						
$\overline{\text{TRST}}$	B12	135	98	I	PD	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: Do not use pullup resistors on $\overline{\text{TRST}}$; it has an internal pulldown device. In a low-noise environment, $\overline{\text{TRST}}$ can be left floating. In a high-noise environment, an additional pulldown resistor may be needed. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Since this is application-specific, it is recommended that each target board is validated for proper operation of the debugger and the application.
TCK	A12	136	99	I	PU	JTAG test clock with internal pullup
TMS	D13	126	92	I	PU	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
TDI	C13	131	96	I	PU	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	D12	127	93	O/Z	–	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK.
EMU0	D11	137	100	I/O/Z	PU	Emulator I/O #0 with internal pullup. When $\overline{\text{TRST}}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan.
EMU1	C9	146	105	I/O/Z	PU	Emulator pin 1. Emulator pin 1 disables all outputs. When $\overline{\text{TRST}}$ is driven high, EMU1 is used as an interrupt to or from the emulator system and is defined as an input/output through the JTAG scan.
ADC ANALOG INPUT SIGNALS						
ADCINA7	B5	167	119	I		8-Channel Analog Inputs for Sample-and-Hold A. The ADC pins should not be driven before the device has been fully powered up.
ADCINA6	D5	168	120	I		
ADCINA5	E5	169	121	I		
ADCINA4	A4	170	122	I		
ADCINA3	B4	171	123	I		
ADCINA2	C4	172	124	I		
ADCINA1	D4	173	125	I		
ADCINA0	A3	174	126	I		

† Typical drive strength of the output buffer for all pins [except TDO, XCLKOUT, XF, XINTF, EMU0, and EMU1 pins] is 4 mA typical.
‡ I = Input, O = Output, Z = High impedance
§ PU = pin has internal pullup; PD = pin has internal pulldown

Table 2–2. Signal Descriptions† (Continued)

NAME	PIN NO. 179-PIN GHH	PIN NO. 176-PIN PGF	PIN NO. 128-PIN PBK	I/O/Z‡	PU/PD§	DESCRIPTION
ADC ANALOG INPUT SIGNALS (CONTINUED)						
ADCINB7	F5	9	9	I		8-Channel Analog Inputs for Sample-and-Hold B. The ADC pins should not be driven before the device has been fully powered up.
ADCINB6	D1	8	8	I		
ADCINB5	D2	7	7	I		
ADCINB4	D3	6	6	I		
ADCINB3	C1	5	5	I		
ADCINB2	B1	4	4	I		
ADCINB1	C3	3	3	I		
ADCINB0	C2	2	2	I		
ADCREFP	E2	11	11	O		ADC Voltage Reference Output (2 V). Requries a low ESR (50 mΩ – 1.5 Ω) ceramic bypass capacitor of 10 µF to analog ground.
ADCREFM	E4	10	10	O		ADC Voltage Reference Output (1 V). Requries a low ESR (50 mΩ – 1.5 Ω) ceramic bypass capacitor of 10 µF to analog ground.
ADCRESEXT	F2	16	16	O		ADC External Current Bias Resistor (24.9 kΩ)
ADCBGREFIN	E6	164	116	I		Test Pin. Reserved for TI. Must be left unconnected.
AVSSREFBG	E3	12	12	I		ADC Analog GND
AVDDREFBG	E1	13	13	I		ADC Analog Power (3.3-V)
ADCLO	B3	175	127	I		Common Low Side Analog Input
V_{SSA1}	F3	15	15	I		ADC Analog GND
V_{SSA2}	C5	165	117	I		ADC Analog GND
V_{DDA1}	F4	14	14	I		ADC Analog 3.3-V Supply
V_{DDA2}	A5	166	118	I		ADC Analog 3.3-V Supply
V_{SS1}	C6	163	115	I		ADC Digital GND
V_{DD1}	A6	162	114	I		ADC Digital 1.8-V Supply
V_{DDAIO}	B2	1	1			3.3-V Analog I/O Power Pin
V_{SSAIO}	A2	176	128			Analog I/O Ground Pin

† Typical drive strength of the output buffer for all pins [except TDO, XCLKOUT, XF, XINTF, EMU0, and EMU1 pins] is 4 mA typical.
‡ I = Input, O = Output, Z = High impedance
§ PU = pin has internal pullup; PD = pin has internal pulldown

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Table 2–2. Signal Descriptions† (Continued)

NAME	PIN NO. 179-PIN GHH	PIN NO. 176-PIN PGF	PIN NO. 128-PIN PBK	I/O/Z‡	PU/PD§	DESCRIPTION
POWER SIGNALS						
V_{DD}	H1	23	20			1.8-V or 1.9-V Core Digital Power Pins. See Section 7.2, Recommended Operating Conditions, for voltage requirements.
V_{DD}	L1	37	29			
V_{DD}	P5	56	42			
V_{DD}	P9	75	56			
V_{DD}	P12	–	63			
V_{DD}	K12	100	74			
V_{DD}	G12	112	82			
V_{DD}	C14	128	94			
V_{DD}	B10	143	102			
V_{DD}	C8	154	110			
V_{SS}	G4	19	17			Core and Digital I/O Ground Pins
V_{SS}	K1	32	26			
V_{SS}	L2	38	30			
V_{SS}	P4	52	39			
V_{SS}	K6	58	–			
V_{SS}	P8	70	53			
V_{SS}	M10	78	59			
V_{SS}	L11	86	62			
V_{SS}	K13	99	73			
V_{SS}	J14	105	–			
V_{SS}	G13	113	–			
V_{SS}	E14	120	88			
V_{SS}	B14	129	95			
V_{SS}	D10	142	–			
V_{SS}	C10	–	103			
V_{SS}	B8	153	109			
V_{DDIO}	J4	31	25			3.3-V I/O Digital Power Pins
V_{DDIO}	L7	64	49			
V_{DDIO}	L10	81	–			
V_{DDIO}	N14	–	–			
V_{DDIO}	G11	114	83			
V_{DDIO}	E9	145	104			
V_{DD3VFL}	N8	69	52			3.3-V Flash core Power Pin. This pin should be connected to 3.3 V at all times after power-up sequence requirements have been met.

† Typical drive strength of the output buffer for all pins [except TDO, XCLKOUT, XF, XINTF, EMU0, and EMU1 pins] is 4 mA typical.
‡ I = Input, O = Output, Z = High impedance
§ PU = pin has internal pullup; PD = pin has internal pulldown

Table 2–2. Signal Descriptions† (Continued)

GPIO	PERIPHERAL SIGNAL	PIN NO.			I/O/Z‡	PU/PD§	DESCRIPTION
		179-PIN GHH	176-PIN PGF	128-PIN PBK			
GPIO OR PERIPHERAL SIGNALS							
GPIOA OR EVA SIGNALS							
GPIOA0	PWM1 (O)	M12	92	68	I/O/Z	PU	GPIO or PWM Output Pin #1
GPIOA1	PWM2 (O)	M14	93	69	I/O/Z	PU	GPIO or PWM Output Pin #2
GPIOA2	PWM3 (O)	L12	94	70	I/O/Z	PU	GPIO or PWM Output Pin #3
GPIOA3	PWM4 (O)	L13	95	71	I/O/Z	PU	GPIO or PWM Output Pin #4
GPIOA4	PWM5 (O)	K11	98	72	I/O/Z	PU	GPIO or PWM Output Pin #5
GPIOA5	PWM6 (O)	K14	101	75	I/O/Z	PU	GPIO or PWM Output Pin #6
GPIOA6	T1PWM_T1CMP (I)	J11	102	76	I/O/Z	PU	GPIO or Timer 1 Output
GPIOA7	T2PWM_T2CMP (I)	J13	104	77	I/O/Z	PU	GPIO or Timer 2 Output
GPIOA8	CAP1_QEP1 (I)	H10	106	78	I/O/Z	PU	GPIO or Capture Input #1
GPIOA9	CAP2_QEP2 (I)	H11	107	79	I/O/Z	PU	GPIO or Capture Input #2
GPIOA10	CAP3_QEPI1 (I)	H12	109	80	I/O/Z	PU	GPIO or Capture Input #3
GPIOA11	TDIRA (I)	F14	116	85	I/O/Z	PU	GPIO or Timer Direction
GPIOA12	TCLKINA (I)	F13	117	86	I/O/Z	PU	GPIO or Timer Clock Input
GPIOA13	$\overline{\text{C1TRIP}}$ (I)	E13	122	89	I/O/Z	PU	GPIO or Compare 1 Output Trip
GPIOA14	$\overline{\text{C2TRIP}}$ (I)	E11	123	90	I/O/Z	PU	GPIO or Compare 2 Output Trip
GPIOA15	$\overline{\text{C3TRIP}}$ (I)	F10	124	91	I/O/Z	PU	GPIO or Compare 3 Output Trip
GPIOB OR EVB SIGNALS							
GPIOB0	PWM7 (O)	N2	45	33	I/O/Z	PU	GPIO or PWM Output Pin #7
GPIOB1	PWM8 (O)	P2	46	34	I/O/Z	PU	GPIO or PWM Output Pin #8
GPIOB2	PWM9 (O)	N3	47	35	I/O/Z	PU	GPIO or PWM Output Pin #9
GPIOB3	PWM10 (O)	P3	48	36	I/O/Z	PU	GPIO or PWM Output Pin #10
GPIOB4	PWM11 (O)	L4	49	37	I/O/Z	PU	GPIO or PWM Output Pin #11
GPIOB5	PWM12 (O)	M4	50	38	I/O/Z	PU	GPIO or PWM Output Pin #12
GPIOB6	T3PWM_T3CMP (I)	K5	53	40	I/O/Z	PU	GPIO or Timer 3 Output
GPIOB7	T4PWM_T4CMP (I)	N5	55	41	I/O/Z	PU	GPIO or Timer 4 Output
GPIOB8	CAP4_QEP3 (I)	M5	57	43	I/O/Z	PU	GPIO or Capture Input #4
GPIOB9	CAP5_QEP4 (I)	M6	59	44	I/O/Z	PU	GPIO or Capture Input #5
GPIOB10	CAP6_QEPI2 (I)	P6	60	45	I/O/Z	PU	GPIO or Capture Input #6
GPIOB11	TDIRB (I)	L8	71	54	I/O/Z	PU	GPIO or Timer Direction
GPIOB12	TCLKINB (I)	K8	72	55	I/O/Z	PU	GPIO or Timer Clock Input
GPIOB13	$\overline{\text{C4TRIP}}$ (I)	N6	61	46	I/O/Z	PU	GPIO or Compare 4 Output Trip
GPIOB14	$\overline{\text{C5TRIP}}$ (I)	L6	62	47	I/O/Z	PU	GPIO or Compare 5 Output Trip
GPIOB15	$\overline{\text{C6TRIP}}$ (I)	K7	63	48	I/O/Z	PU	GPIO or Compare 6 Output Trip

† Typical drive strength of the output buffer for all pins [except TDO, XCLKOUT, XF, XINTF, EMU0, and EMU1 pins] is 4 mA typical.
‡ I = Input, O = Output, Z = High impedance
§ PU = pin has internal pullup; PD = pin has internal pulldown

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Table 2–2. Signal Descriptions† (Continued)

GPIO	PERIPHERAL SIGNAL	PIN NO. 179-PIN GHH	PIN NO. 176-PIN PGF	PIN NO. 128-PIN PBK	I/O/Z‡	PU/PD§	DESCRIPTION
GPIOD OR EVA SIGNALS							
GPIOD0	$\overline{\text{T1CTRIP\_PDPINTA}}$ (I)	H14	110	81	I/O/Z	PU	Timer 1 Compare Output Trip
GPIOD1	$\overline{\text{T2CTRIP}}$/$\overline{\text{EVASOC}}$ (I)	G10	115	84	I/O/Z	PU	Timer 2 Compare Output Trip or External ADC Start-of-Conversion EV-A
GPIOD OR EVB SIGNALS							
GPIOD5	$\overline{\text{T3CTRIP\_PDPINTB}}$ (I)	P10	79	60	I/O/Z	PU	Timer 3 Compare Output Trip
GPIOD6	$\overline{\text{T4CTRIP}}$/$\overline{\text{EVBSOC}}$ (I)	P11	83	61	I/O/Z	PU	Timer 4 Compare Output Trip or External ADC Start-of-Conversion EV-B
GPIOE OR INTERRUPT SIGNALS							
GPIOE0	XINT1_$\overline{\text{XBIO}}$ (I)	D9	149	106	I/O/Z	–	GPIO or XINT1 or $\overline{\text{XBIO}}$ input
GPIOE1	XINT2_ADCSOC (I)	D8	151	108	I/O/Z	–	GPIO or XINT2 or ADC start of conversion
GPIOE2	XNMI_XINT13 (I)	E8	150	107	I/O/Z	PU	GPIO or XNMI or XINT13
GPIOF OR SPI SIGNALS							
GPIOF0	SPISIMOA (O)	M1	40	31	I/O/Z	–	GPIO or SPI slave in, master out
GPIOF1	SPISOMIA (I)	N1	41	32	I/O/Z	–	GPIO or SPI slave out, master in
GPIOF2	SPICLKA (I/O)	K2	34	27	I/O/Z	–	GPIO or SPI clock
GPIOF3	SPISTEA (I/O)	K4	35	28	I/O/Z	–	GPIO or SPI slave transmit enable
GPIOF OR SCI-A SIGNALS							
GPIOF4	SCITXDA (O)	C7	155	111	I/O/Z	PU	GPIO or SCI asynchronous serial port TX data
GPIOF5	SCIRXDA (I)	A7	157	112	I/O/Z	PU	GPIO or SCI asynchronous serial port RX data
GPIOF OR CAN SIGNALS							
GPIOF6	CANTXA (O)	N12	87	64	I/O/Z	PU	GPIO or eCAN transmit data
GPIOF7	CANRXA (I)	N13	89	65	I/O/Z	PU	GPIO or eCAN receive data
GPIOF OR MCBSP SIGNALS							
GPIOF8	MCLKXA (I/O)	J1	28	23	I/O/Z	PU	GPIO or transmit clock
GPIOF9	MCLKRA (I/O)	H2	25	21	I/O/Z	PU	GPIO or receive clock
GPIOF10	MFSXA (I/O)	H4	26	22	I/O/Z	PU	GPIO or transmit frame synch
GPIOF11	MFSRA (I/O)	J2	29	24	I/O/Z	PU	GPIO or receive frame synch
GPIOF12	MDXA (O)	G1	22	19	I/O/Z	–	GPIO or transmitted serial data
GPIOF13	MDRA (I)	G2	20	18	I/O/Z	PU	GPIO or received serial data

† Typical drive strength of the output buffer for all pins [except TDO, XCLKOUT, XF, XINTF, EMU0, and EMU1 pins] is 4 mA typical.
‡ I = Input, O = Output, Z = High impedance
§ PU = pin has internal pullup; PD = pin has internal pulldown

Table 2–2. Signal Descriptions† (Continued)

GPIO	PERIPHERAL SIGNAL	PIN NO.			I/O/Z‡	PU/PD§	DESCRIPTION
		179-PIN GHH	176-PIN PGF	128-PIN PBK			
GPIOF OR XF CPU OUTPUT SIGNAL							
GPIOF14	XF_$\overline{\text{XPLLDIS}}$ (O)	A11	140	101	I/O/Z	PU	This pin has three functions: 1. XF – General-purpose output pin. 2. XPLLDIS – This pin will be sampled during reset to check if the PLL needs to be disabled. The PLL will be disabled if this pin is sensed low. HALT and STANDBY modes cannot be used when the PLL is disabled. 3. GPIO – GPIO function
GPIOG OR SCI-B SIGNALS							
GPIOG4	SCITXDB (O)	P14	90	66	I/O/Z	–	GPIO or SCI asynchronous serial port transmit data
GPIOG5	SCIRXDB (I)	M13	91	67	I/O/Z	–	GPIO or SCI asynchronous serial port receive data

† Typical drive strength of the output buffer for all pins [except TDO, XCLKOUT, XF, XINTF, EMU0, and EMU1 pins] is 4 mA typical.
‡ I = Input, O = Output, Z = High impedance
§ PU = pin has internal pullup; PD = pin has internal pulldown

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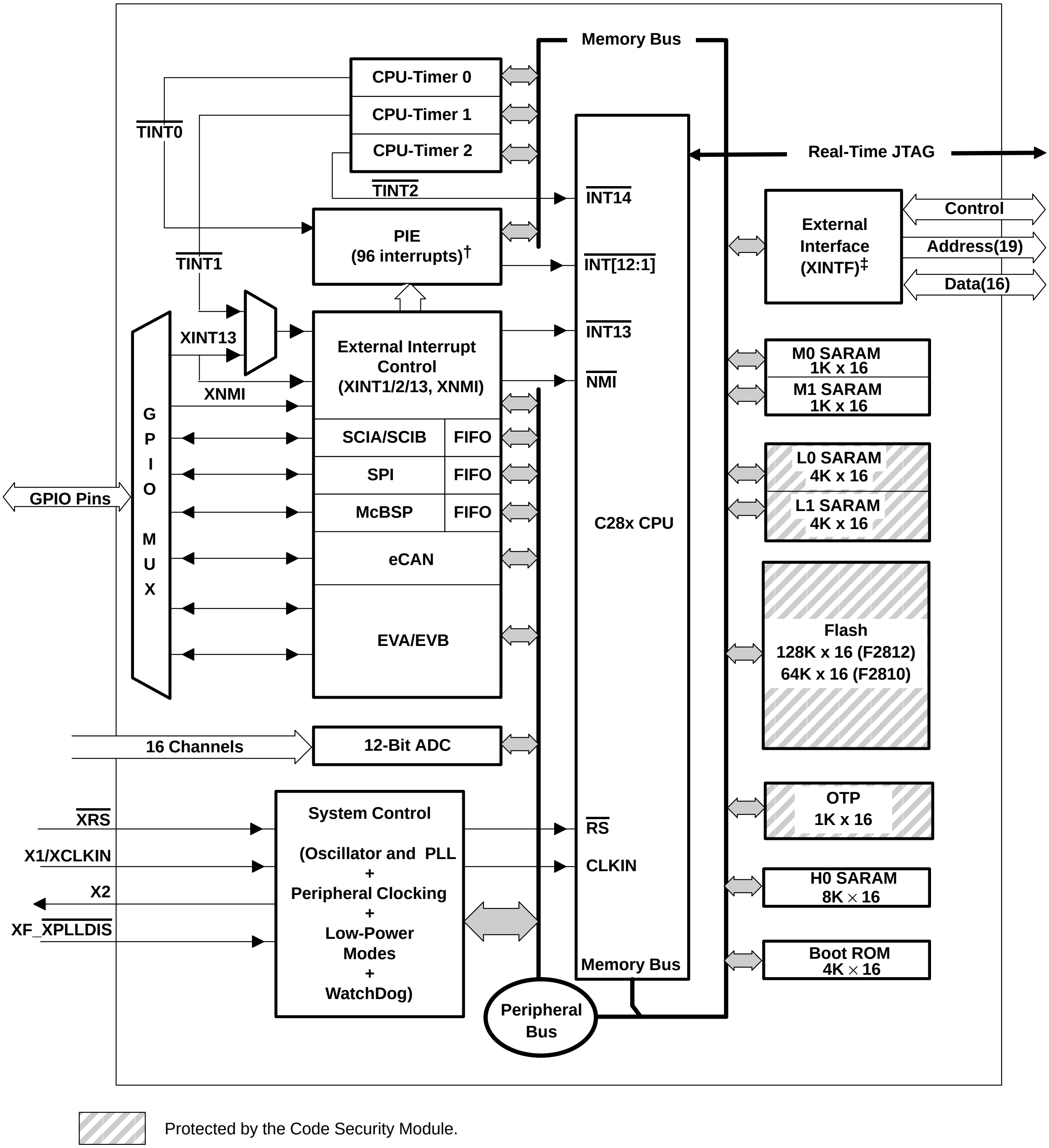
3 Functional Overview



Protected by the Code Security Module.

† 45 of the possible 96 interrupts are used on the devices.
‡ XINTF is not available on the F2810.

Figure 3–1. Functional Block Diagram

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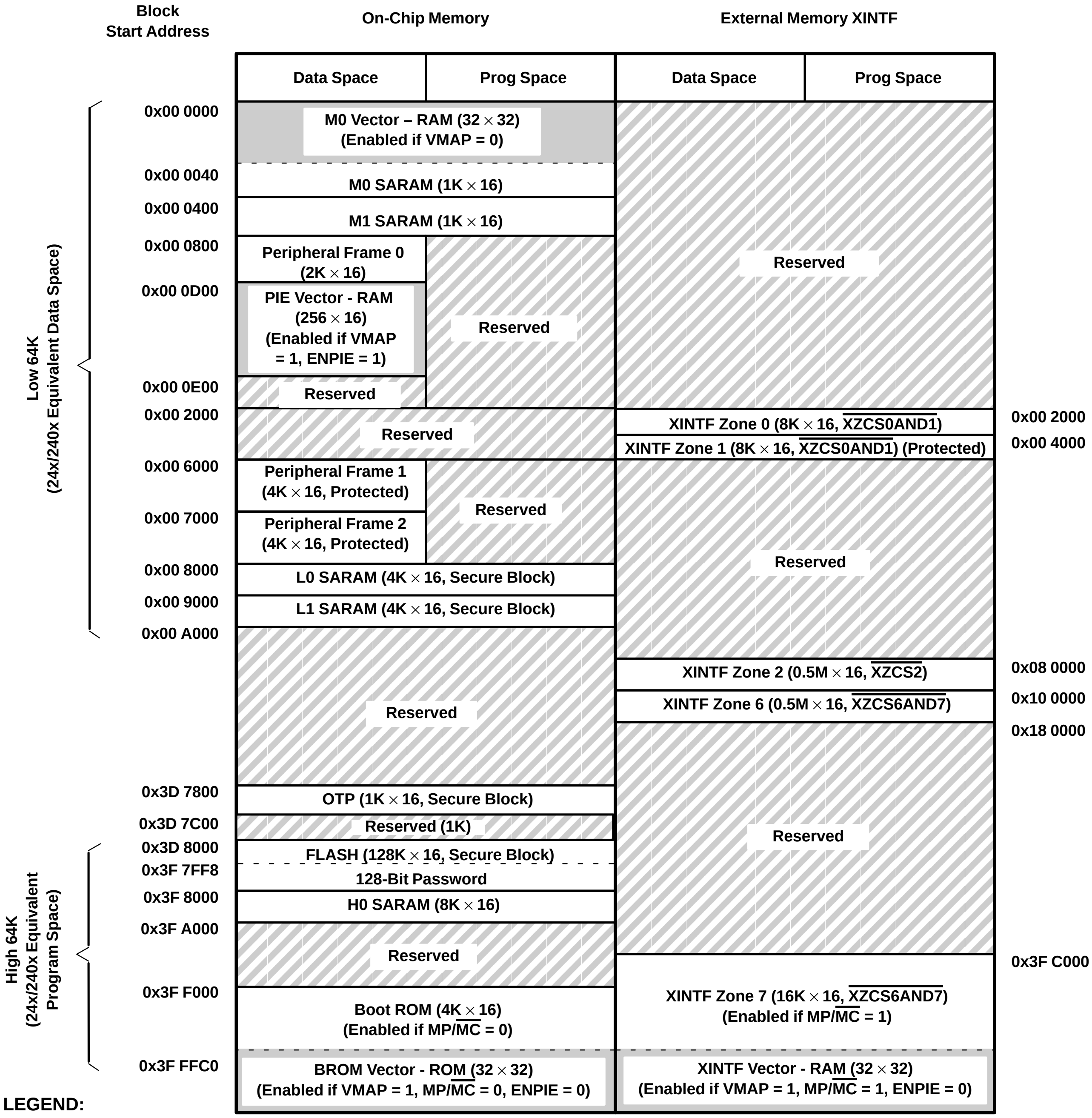
3.1 Memory Map

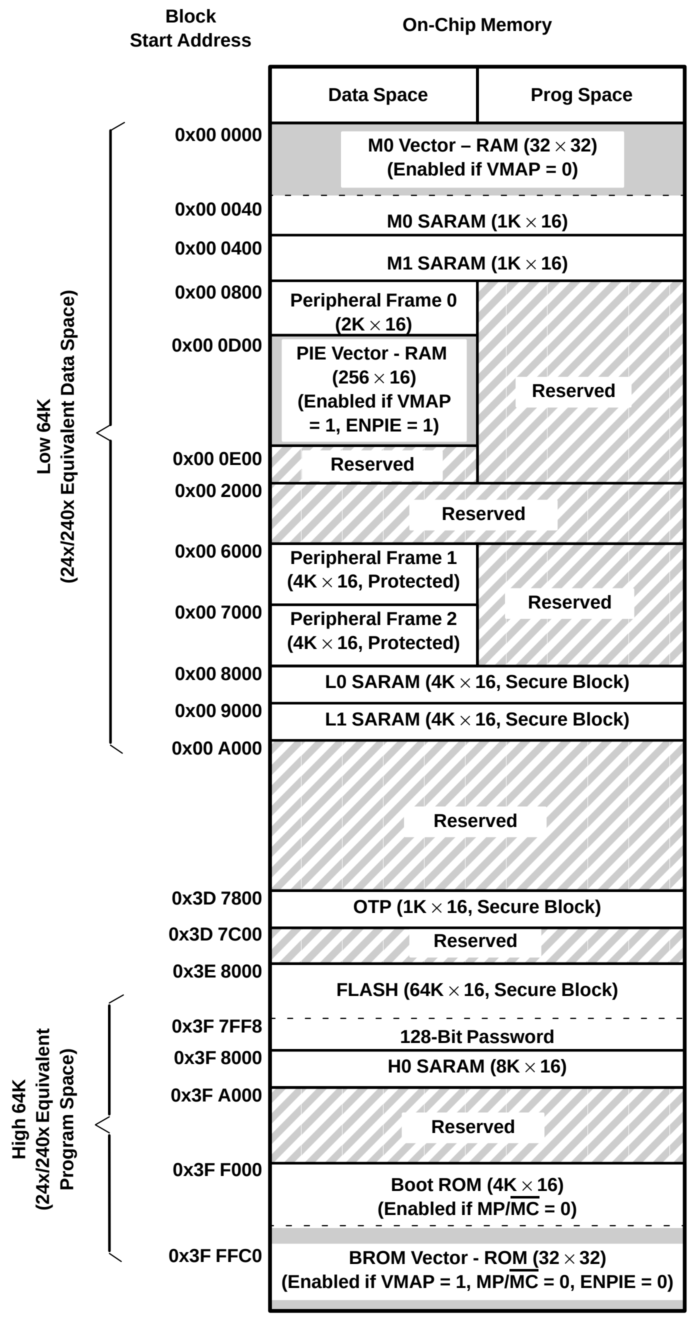


LEGEND:

Only one of these vector maps—M0 vector, PIE vector, BROM vector, XINTF vector—should be enabled at a time.

NOTES:
A. Memory blocks are not to scale.
B. Reserved locations are reserved for future expansion. Application should not access these areas.
C. Boot ROM and Zone 7 memory maps are active either in on-chip or XINTF zone depending on MP/MC, not in both.
D. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.
E. “Protected” means the order of Write followed by Read operations is preserved rather than the pipeline order.
F. Certain memory ranges are EALLOW protected for spurious writes after configuration.
G. Zones 0 and 1 and Zones 6 and 7 share the same chip select; hence, these memory blocks have mirrored locations.

Figure 3–2. F2812 Memory Map



LEGEND:

Only one of these vector maps—M0 vector, PIE vector, BROM vector—should be enabled at a time.

NOTES: A. Memory blocks are not to scale.
B. Reserved locations are reserved for future expansion. Application should not access these areas.
C. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.
D. "Protected" means the order of Write followed by Read operations is preserved rather than the pipeline order.
E. Certain memory ranges are EALLOW protected for spurious writes after configuration.

Figure 3–3. F2810 Memory Map

Table 3–1. Addresses of Flash Sectors in F2812

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3D 8000 0x3D 9FFF	Sector J, 8K x 16
0x3D A000 0x3D BFFF	Sector I, 8K x 16
0x3D C000 0x3D FFFF	Sector H, 16K x 16
0x3E 0000 0x3E 3FFF	Sector G, 16K x 16
0x3E 4000 0x3E 7FFF	Sector F, 16K x 16
0x3E 8000 0x3E BFFF	Sector E, 16K x 16
0x3E C000 0x3E FFFF	Sector D, 16K x 16
0x3F 0000 0x3F 3FFF	Sector C, 16K x 16
0x3F 4000 0x3F 5FFF	Sector B, 8K x 16
0x3F 6000	Sector A, 8K x 16
0x3F 7F80 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 0x3F 7FFF	Security Password (128-Bit)

Table 3–2. Addresses of Flash Sectors in F2810

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3E 8000 0x3E BFFF	Sector E, 16K x 16
0x3E C000 0x3E FFFF	Sector D, 16K x 16
0x3F 0000 0x3F 3FFF	Sector C, 16K x 16
0x3F 4000 0x3F 5FFF	Sector B, 8K x 16
0x3F 6000	Sector A, 8K x 16
0x3F 7F80 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 0x3F 7FFF	Security Password (128-Bit)

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The “Low 64K” of the memory address range maps into the data space of the 240x. The “High 64K” of the memory address range maps into the program space of the 24x/240x. 24x/240x-compatible code will only execute from the “High 64K” memory area. Hence, the top 32K of Flash and H0 SARAM block can be used to run 24x/240x-compatible code (if MP/$\overline{\text{MC}}$ mode is low) or, on the F2812, code can be executed from XINTF Zone 7 (if MP/$\overline{\text{MC}}$ mode is high).

The XINTF consists of five independent zones. One zone has its own chip select and the remaining four zones share two chip selects. Each zone can be programmed with its own timing (wait states) and to either sample or ignore external ready signal. This makes interfacing to external peripherals easy and glueless.

Note: The chip selects of XINTF Zone 0 and Zone 1 are merged together into a single chip select ($\overline{\text{XZCS0AND1}}$); and the chip selects of XINTF Zone 6 and Zone 7 are merged together into a single chip select ($\overline{\text{XZCS6AND7}}$). Refer to Section 3.5, “External Interface, XINTF (F2812 only)”, for details.

Peripheral Frame 1, Peripheral Frame 2, and XINTF Zone 1 are grouped together so as to enable these blocks to be “write/read peripheral block protected”. The “protected” mode ensures that all accesses to these blocks happen as written. Because of the C28x pipeline, a write immediately followed by a read, to different memory locations, will appear in reverse order on the memory bus of the CPU. This can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The C28x CPU supports a block protection mode where a region of memory can be protected so as to make sure that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable and by default, it will protect the selected zones.

On the F2812, at reset, XINTF Zone 7 is accessed if the XMP/$\overline{\text{MC}}$ pin is pulled high. This signal selects microprocessor or microcomputer mode of operation. In microprocessor mode, Zone 7 is mapped to high memory such that the vector table is fetched externally. The Boot ROM is disabled in this mode. In microcomputer mode, Zone 7 is disabled such that the vectors are fetched from Boot ROM. This allows the user to either boot from on-chip memory or from off-chip memory. The state of the XMP/$\overline{\text{MC}}$ signal on reset is stored in an MP/$\overline{\text{MC}}$ mode bit in the XINTCNF2 register. The user can change this mode in software and hence control the mapping of Boot ROM and XINTF Zone 7. No other memory blocks are affected by XMP/$\overline{\text{MC}}$.

I/O space is not supported on the F2812 XINTF.

The wait states for the various spaces in the memory map area are listed in Table 3–3.

Table 3–3. Wait States

AREA	WAIT-STATES	COMMENTS
M0 and M1 SARAMs	0-wait	
Peripheral Frame 0	0-wait	Includes the Flash registers
Peripheral Frame 1	0-wait (writes) 2-wait (reads)	Cycles can be extended by peripheral generated ready.
Peripheral Frame 2	0-wait (writes) 2-wait (reads)	Fixed. Cycles cannot be extended by the peripheral.
L0 & L1 SARAMs	0-wait	
OTP	Programmable, 1-wait minimum	Programmed via the Flash registers. 0-wait-state operation is possible at a reduced CPU frequency. (Frequency limits will be available after device characterization.) Refer to Section 3.2.6, Flash, for more information.
Flash	Programmable, 0-wait minimum	Programmed via the Flash registers. 0-wait-state operation is possible at reduced CPU frequency. (Frequency limits will be available after device characterization.) The CSM password locations are hardwired for 16 wait-states. Refer to Section 3.2.6, Flash, for more information.
H0 SARAM	0-wait	
Boot-ROM	1-wait	
XINTF	Programmable, 1-wait minimum	Programmed via the XINTF registers. Cycles can be extended by external memory or peripheral. 0-wait operation is not possible.

3.2 Brief Descriptions

3.2.1 C28x CPU

The C28x™ DSP generation is the newest member of the TMS320C2000™ DSP platform. The C28x is source code compatible to the 24x/240x DSP devices, hence existing 240x users can leverage their significant software investment. Additionally, the C28x is a very efficient C/C++ engine, hence enabling users to develop not only their system control software in a high-level language, but also enables math algorithms to be developed using C/C++. The C28x is as efficient in DSP math tasks as it is in system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC capabilities of the C28x and its 64-bit processing capabilities, enable the C28x to efficiently handle higher numerical resolution problems that would otherwise demand a more expensive floating-point processor solution. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The C28x has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables the C28x to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

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3.2.2 Memory Bus (Harvard Bus Architecture)

As with many DSP type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The C28x memory bus architecture contains a program read bus, data read bus and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed “Harvard Bus”, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus will prioritize memory accesses. Generally, the priority of Memory Bus accesses can be summarized as follows:

Highest:	Data Writes†
	Program Writes†
	Data Reads
	Program Reads‡
Lowest:	Fetches‡

3.2.3 Peripheral Bus

To enable migration of peripherals between various Texas Instruments (TI) DSP family of devices, the F2810 and F2812 adopt a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various busses that make up the processor “Memory Bus” into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Two versions of the peripheral bus are supported on the F2810 and F2812. One version only supports 16-bit accesses (called peripheral frame 2) and this retains compatibility with C240x-compatible peripherals. The other version supports both 16- and 32-bit accesses (called peripheral frame 1).

3.2.4 Real-Time JTAG and Analysis

The C28x implements the standard IEEE 1149.1 JTAG interface. Additionally, the C28x supports real-time mode of operation whereby the contents of memory, peripheral and register locations can be modified while the processor is running and executing code and servicing interrupts. The user can also single step through non-time critical code while enabling time-critical interrupts to be serviced without interference. The C28x implements the real-time mode in hardware within the CPU. This is a unique feature to the C28x, no software monitor is required. Additionally, special analysis hardware is provided which allows the user to set hardware breakpoint or data/address watch-points and generate various user selectable break events when a match occurs.

3.2.5 External Interface (XINTF) (F2812 Only)

This asynchronous interface consists of 19 address lines, 16 data lines, and three chip-select lines. The chip-select lines are mapped to five external zones, Zones 0, 1, 2, 6, and 7. Zones 0 and 1 share a single chip-select; Zones 6 and 7 also share a single chip-select. Each of the five zones can be programmed with different number of wait states, strobe signal setup and hold timing and each zone can be programmed for extending wait states externally or not. The programmable wait-state, chip-select and programmable strobe timing enables glueless interface to external memories and peripherals.

† Simultaneous Data and Program writes cannot occur on the Memory Bus.
‡ Simultaneous Program Reads and Fetches cannot occur on the Memory Bus.

3.2.6 Flash

The F2812 contains 128K x 16 of embedded Flash memory and 1K x 16 of OTP memory. The Flash memory is segregated into four 8K x 16 sized sectors, and six 16K x 16 sized sectors. The user can individually erase, program and validate a sector while leaving other sectors untouched. However, it is not possible to use one sector of the Flash (or the OTP) to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the Flash module to achieve higher performance. The Flash/OTP is mapped to both program and data space hence can be used to execute code or store data information.

The F2810 has 64K x 16 of embedded Flash and 1K x 16 of OTP memory. The address range of OTP is 0x3D 7800 – 0x3D 7BFF in both the F2812 and F2810 devices.

CAUTION:

The F2810/F2812 Flash and OTP wait states can be configured by the application. This allows applications running at slower frequencies to configure the flash to use fewer wait states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent. The pipeline mode is not available for the OTP block.

For more information on the Flash options, Flash wait-state, and OTP wait-state registers, refer to the *TMS320F28x System Control and Interrupts Peripheral Reference Guide* (literature number SPRU078).

3.2.7 M0, M1 SARAMs

All C28x devices contain these two blocks of single access memory, each 1K x 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 block overlaps the 240x device B0, B1, B2 RAM blocks and hence the mapping of data variables on the 240x devices can remain at the same physical address on C28x devices. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer. This makes for easier programming in high-level languages.

3.2.8 L0, L1, H0 SARAMs

The F2810 and the F2812 contain an additional 16K x 16 of single-access RAM, divided into 3 blocks (4K + 4K + 8K). Each block can be independently accessed hence minimizing pipeline stalls. Each block is mapped to both program and data space.

3.2.9 Boot ROM

The Boot ROM is factory programmed with boot loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash. The Boot ROM will also contain standard tables, such as SIN/COS waveforms, for use in math related algorithms.

3.2.10 Security

The F2810 and F2812 support high levels of security to protect the user firmware from being reversed engineered. The security features a 128-bit password (hardcoded for 16 wait states), which the user programs into the Flash. One code security module (CSM) is used to protect the Flash/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents via the JTAG port, executing code from external memory or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit ”KEY” value, which matches the value stored in the password locations within the Flash.

CAUTION:

For code security operation, all addresses between 0x3F7F80 and 0x3F7FF5 cannot be used as program code or data, but must be programmed to 0x0000 when the Code Security Passwords are programmed. If security is not a concern, then these addresses may be used for code or data.

Code Security Module Disclaimer

The Code Security Module (“CSM”) included on this device was designed to password protect the data stored in the associated memory (either ROM or Flash) and is warranted by Texas Instruments (TI), in accordance with its standard terms and conditions, to conform to TI’s published specifications for the warranty period applicable for this device.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

3.2.11 Peripheral Interrupt Expansion (PIE) Block

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the F2810 and F2812, 45 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines ($\overline{\text{INT1}}$ to $\overline{\text{INT12}}$). Each of the 96 interrupts is, supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is, automatically fetched by the CPU on servicing the interrupt. It takes 9 CPU clock cycles to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

3.2.12 External Interrupts (XINT1, 2, 13, XNMI)

The F2810 and F2812 support three masked external interrupts (XINT1, 2, 13). XINT13 is combined with one non-masked external interrupt (XNMI). The combined signal name is XNMI_XINT13. Each of the interrupts can be selected for negative or positive edge triggering and can also be enabled/disabled (including the XNMI). The masked interrupts also contain a 16-bit free running up counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time stamp the interrupt.

3.2.13 Oscillator and PLL

The F2810 and F2812 can be clocked by an external oscillator or by a crystal attached to the on-chip oscillator circuit. A PLL is provided supporting up to 10-input clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. The PLL block can be set in bypass mode.

3.2.14 Watchdog

The F2810 and F2812 support a watchdog timer. The user software must regularly reset the watchdog counter within a certain time frame; otherwise, the watchdog will generate a reset to the processor. The watchdog can be disabled if necessary.

3.2.15 Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled so as to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except eCAN) and the event managers, CAP and QEP blocks can be scaled relative to the CPU clock. This enables the timing of peripherals to be decoupled from increasing CPU clock speeds.

3.2.16 Low-Power Modes

The F2810 and F2812 devices are full static CMOS devices. Three low-power modes are provided:

IDLE: Place CPU into low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that need to function during IDLE are left operating. An enabled interrupt from an active peripheral will wake the processor from IDLE mode.

STANDBY: Turn off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event.

HALT: Turn off oscillator. This mode basically shuts down the device and places it in the lowest possible power consumption mode. Only a reset or XNMI will wake the device from this mode.

3.2.17 Peripheral Frames 0, 1, 2 (PFn)

The F2810 and F2812 segregate peripherals into three sections. The mapping of peripherals is as follows:

PF0:	XINTF:	External Interface Configuration Registers (F2812 only)
	PIE:	PIE Interrupt Enable and Control Registers Plus PIE Vector Table
	Flash:	Flash Control, Programming, Erase, Verify Registers
	Timers:	CPU-Timers 0, 1, 2 Registers
	CSM:	Code Security Module KEY Registers
PF1:	eCAN:	eCAN Mailbox and Control Registers
PF2:	SYS:	System Control Registers
	GPIO:	GPIO Mux Configuration and Control Registers
	EV:	Event Manager (EVA/EVB) Control Registers
	McBSP:	McBSP Control and TX/RX Registers
	SCI:	Serial Communications Interface (SCI) Control and RX/TX Registers
	SPI:	Serial Peripheral Interface (SPI) Control and RX/TX Registers
	ADC:	12-Bit ADC Registers

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3.2.18 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose I/O (GPIO) signals. This enables the user to use a pin as GPIO if the peripheral signal or function is not used. On reset, all GPIO pins are configured as inputs. The user can then individually program each pin for GPIO mode or Peripheral Signal mode. For specific inputs, the user can also select the number of input qualification cycles. This is to filter unwanted noise glitches.

3.2.19 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value. CPU-Timer 2 is reserved for Real-Time OS (RTOS)/BIOS applications. CPU-Timer 1 is also reserved for TI system functions. CPU-Timer 2 is connected to INT14 of the CPU. CPU-Timer 1 can be connected to INT13 of the CPU. CPU-Timer 0 is for general use and is connected to the PIE block.

3.2.20 Motor Control Peripherals

The F2810 and F2812 support the following peripherals which are used for embedded control and communication:

EV: The event manager module includes general-purpose timers, full-compare/PWM units, capture inputs (CAP) and quadrature-encoder pulse (QEP) circuits. Two such event managers are provided which enable two three-phase motors to be driven or four two-phase motors. The event managers on the F2810 and F2812 are compatible to the event managers on the 240x devices (with some minor enhancements).

ADC: The ADC block is a 12-bit converter, single ended, 16-channels. It contains two sample-and-hold units for simultaneous sampling.

3.2.21 Serial Port Peripherals

The F2810 and F2812 support the following serial communication peripherals:

eCAN: This is the enhanced version of the CAN peripheral. It supports 32 mailboxes, time stamping of messages, and is CAN 2.0B-compliant.

McBSP: This is the multichannel buffered serial port that is used to connect to E1/T1 lines, phone-quality codecs for modem applications or high-quality stereo-quality Audio DAC devices. The McBSP receive and transmit registers are supported by a 16-level FIFO. This significantly reduces the overhead for servicing this peripheral.

SPI: The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. On the F2810 and the F2812, the port supports a 16-level, receive and transmit FIFO for reducing servicing overhead.

SCI: The serial communications interface is a two-wire asynchronous serial port, commonly known as UART. On the F2810 and the F2812, the port supports a 16-level, receive and transmit FIFO for reducing servicing overhead.

3.3 Register Map

The F2810 device contains three peripheral register spaces. The spaces are categorized as follows:

- Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See Table 3–4.
- Peripheral Frame 1: These are peripherals that are mapped to the 32-bit peripheral bus. See Table 3–5.
- Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 3–6.

Table 3–4. Peripheral Frame 0 Registers†

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE‡
Device Emulation Registers	0x00 0880 0x00 09FF	384	EALLOW protected
reserved	0x00 0A00 0x00 0A7F	128	
FLASH Registers§	0x00 0A80 0x00 0ADF	96	EALLOW protected CSM Protected
Code Security Module Registers	0x00 0AE0 0x00 0AEF	16	EALLOW protected
reserved	0x00 0AF0 0x00 0B1F	48	
XINTF Registers	0x00 0B20 0x00 0B3F	32	Not EALLOW protected
reserved	0x00 0B40 0x00 0BFF	192	
CPU-TIMER0/1/2 Registers	0x00 0C00 0x00 0C3F	64	Not EALLOW protected
reserved	0x00 0C40 0x00 0CDF	160	
PIE Registers	0x00 0CE0 0x00 0CFF	32	Not EALLOW protected
PIE Vector Table	0x00 0D00 0x00 0DFF	256	EALLOW protected
Reserved	0x00 0E00 0x00 0FFF	512	

† Registers in Frame 0 support 16-bit and 32-bit accesses.
‡ If registers are EALLOW protected, then writes cannot be performed until the user executes the EALLOW instruction. The EDIS instruction disables writes. This prevents stray code or pointers from corrupting register contents.
§ The Flash Registers are also protected by the Code Security Module (CSM).

Table 3–5. Peripheral Frame 1 Registers¶

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE
eCAN Registers	0x00 6000 0x00 60FF	256 (128 x 32)	Some eCAN control registers (and selected bits in other eCAN control registers) are EALLOW-protected.
eCAN Mailbox RAM	0x00 6100 0x00 61FF	256 (128 x 32)	Not EALLOW-protected
reserved	0x00 6200 0x00 6FFF	3584	

¶ The eCAN control registers only support 32-bit read/write operations. All 32-bit accesses are aligned to even address boundaries.

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Table 3–6. Peripheral Frame 2 Registers†

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE
reserved	0x00 7000 0x00 700F	16	
System Control Registers	0x00 7010 0x00 702F	32	EALLOW Protected
reserved	0x00 7030 0x00 703F	16	
SPI-A Registers	0x00 7040 0x00 704F	16	Not EALLOW Protected
SCI-A Registers	0x00 7050 0x00 705F	16	Not EALLOW Protected
reserved	0x00 7060 0x00 706F	16	
External Interrupt Registers	0x00 7070 0x00 707F	16	Not EALLOW Protected
reserved	0x00 7080 0x00 70BF	64	
GPIO Mux Registers	0x00 70C0 0x00 70DF	32	EALLOW Protected
GPIO Data Registers	0x00 70E0 0x00 70FF	32	Not EALLOW Protected
ADC Registers	0x00 7100 0x00 711F	32	Not EALLOW Protected
reserved	0x00 7120 0x00 73FF	736	
EV-A Registers	0x00 7400 0x00 743F	64	Not EALLOW Protected
reserved	0x00 7440 0x00 74FF	192	
EV-B Registers	0x00 7500 0x00 753F	64	Not EALLOW Protected
reserved	0x00 7540 0x00 774F	528	
SCI-B Registers	0x00 7750 0x00 775F	16	Not EALLOW Protected
reserved	0x00 7760 0x00 77FF	160	
McBSP Registers	0x00 7800 0x00 783F	64	Not EALLOW Protected
reserved	0x00 7840 0x00 7FFF	1984	

† Peripheral Frame 2 only allows 16-bit accesses. All 32-bit accesses are ignored (invalid data may be returned or written).

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3.4 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 3–7.

Table 3–7. Device Emulation Registers

NAME	ADDRESS RANGE	SIZE (x16)	DESCRIPTION
DEVICECNF	0x00 0880 0x00 0881	2	Device Configuration Register
reserved	0x00 0882	1	Not supported on Revision C and later silicon
DEVICEID	0x00 0883	1	Device ID Register (0x0003 – TMP silicon – Rev. C)
PROTSTART	0x00 0884	1	Block Protection Start Address Register
PROTRANGE	0x00 0885	1	Block Protection Range Address Register
reserved	0x00 0886 0x00 09FF	378	

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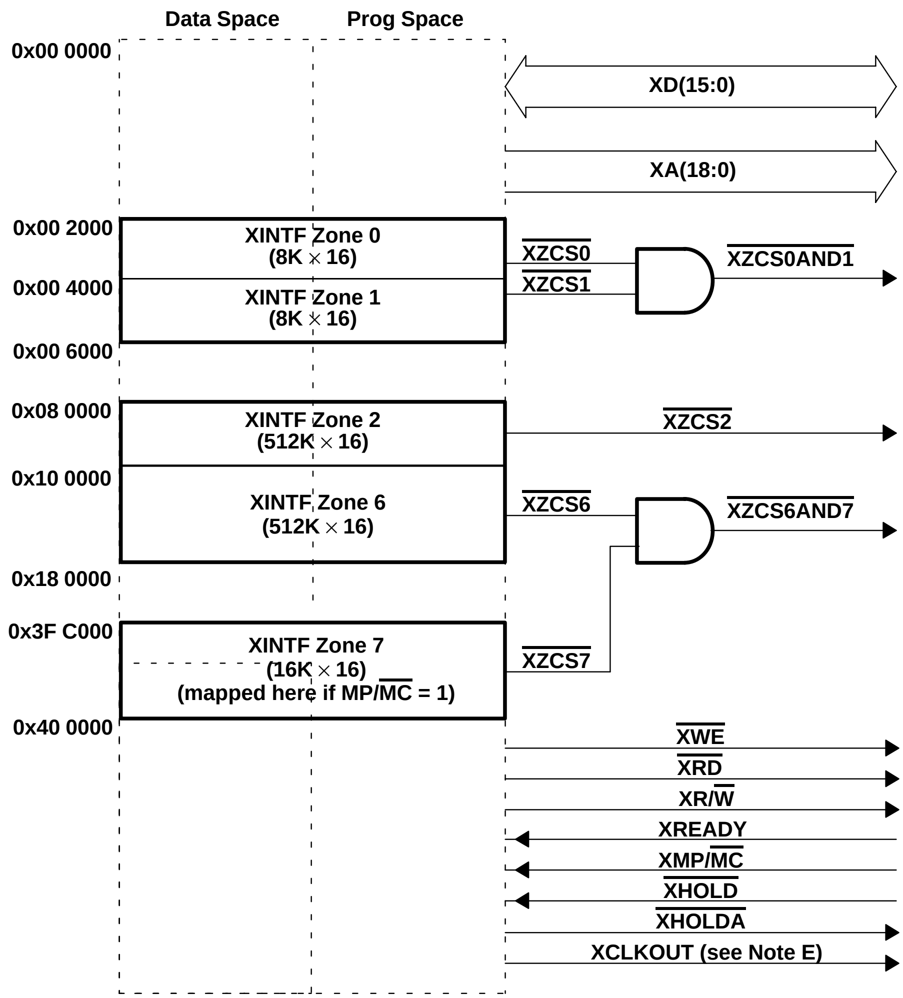
3.5 External Interface, XINTF (F2812 Only)

This section gives a top-level view of the external interface (XINTF) that is implemented on the F2812 device.

The external interface is a non-multiplexed asynchronous bus, similar to the C240x external interface. The external interface on the F2812 is mapped into five fixed zones shown in Figure 3–4.

Figure 3–4 shows the F2812 XINTF signals.



NOTES:
- A. The mapping of XINTF Zone 7 is dependent on the XMP/MC device input signal and the MP/MC mode bit (bit 8 of XINTCNF2 register). Zones 0, 1, 2, and 6 are always enabled.
- B. Each zone can be programmed with different wait states, setup and hold timings, and is supported by zone chip selects (XZCS0AND1, XZCS2, XZCS6AND7), which toggle when an access to a particular zone is performed. These features enable glueless connection to many external memories and peripherals.
- C. The chip selects for Zone 0 and 1 are ANDed internally together to form one chip select (XZCS0AND1). Any external memory that is connected to XZCS0AND1 is dually mapped to both Zones 0 and Zone 1.
- D. The chip selects for Zone 6 and 7 are ANDed internally together to form one chip select (XZCS6AND7). Any external memory that is connected to XZCS6AND7 is dually mapped to both Zones 6 and Zone 7. This means that if Zone 7 is disabled (via the MP/MC mode) then any external memory is still accessible via Zone 6 address space.
- E. XCLKOUT is also pinned out on the F2810.

Figure 3–4. External Interface Block Diagram

The operation and timing of the external interface, can be controlled by the registers listed in Table 3–8.

Table 3–8. XINTF Configuration and Control Register Mappings

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XTIMING0	0x00 0B20	2	XINTF Timing Register, Zone 0 can access as two 16-bit registers or one 32-bit register
XTIMING1	0x00 0B22	2	XINTF Timing Register, Zone 1 can access as two 16-bit registers or one 32-bit register
XTIMING2	0x00 0B24	2	XINTF Timing Register, Zone 2 can access as two 16-bit registers or one 32-bit register
XTIMING6	0x00 0B2C	2	XINTF Timing Register, Zone 6 can access as two 16-bit registers or one 32-bit register
XTIMING7	0x00 0B2E	2	XINTF Timing Register, Zone 7 can access as two 16-bit registers or one 32-bit register
XINTCNF2	0x00 0B34	2	XINTF Configuration Register can access as two 16-bit registers or one 32-bit register
XBANK	0x00 0B38	1	XINTF Bank Control Register
XREVISION	0x00 0B3A	1	XINTF Revision Register

3.5.1 Timing Registers

XINTF signal timing can be tuned to match specific external device requirements such as setup and hold times to strobe signals for contention avoidance and maximizing bus efficiency. The timing parameters can be configured individually for each zone. This allows the programmer to maximize the efficiency of the bus, based on the type of memory or peripheral that the user needs to access. All XINTF timing values are with respect to XTIMCLK, which is equal to or one-half of the SYSCLKOUT rate, as shown in Figure 3–5.

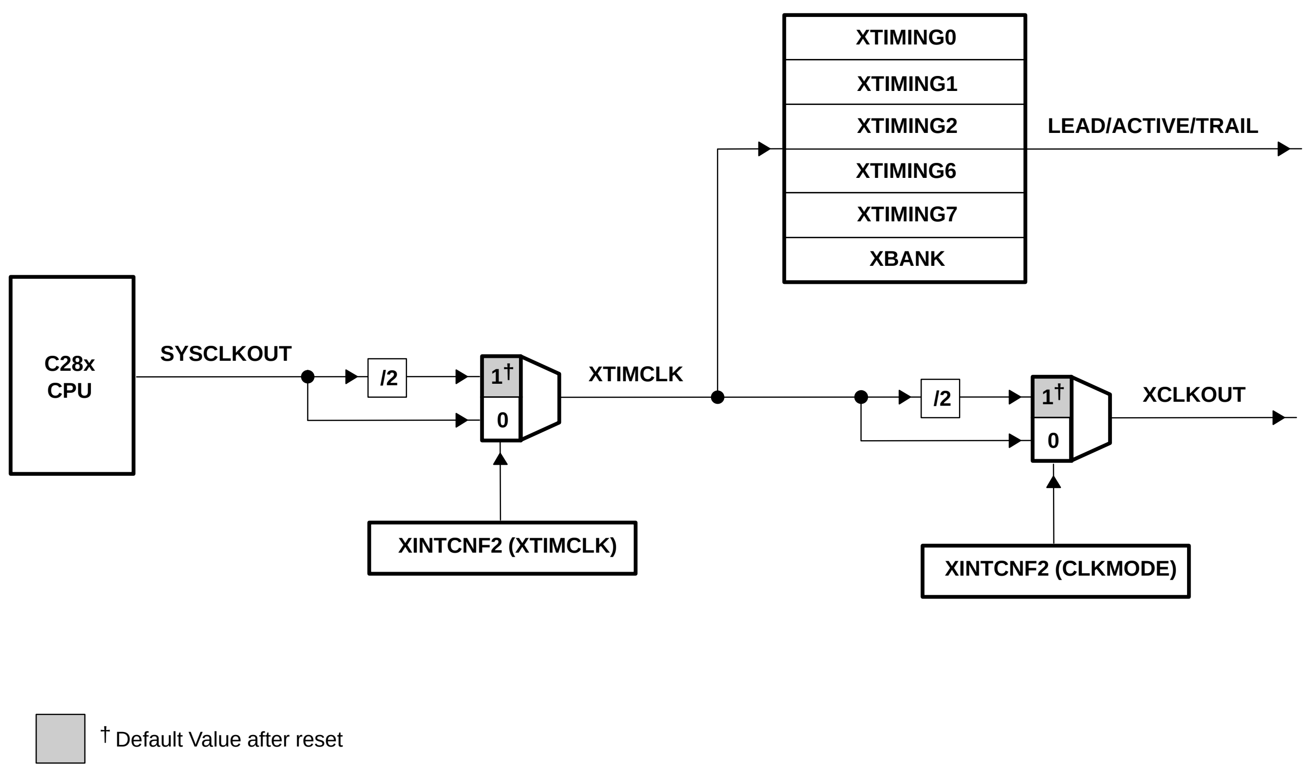


Figure 3–5. Relationship Between XTIMCLK and SYSCLKOUT

For detailed information on the XINTF timing and configuration register bit fields, refer to the *TMS320F28x DSP External Interface (XINTF) Reference Guide* (literature number SPRU067).

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3.5.2 XREVISION Register

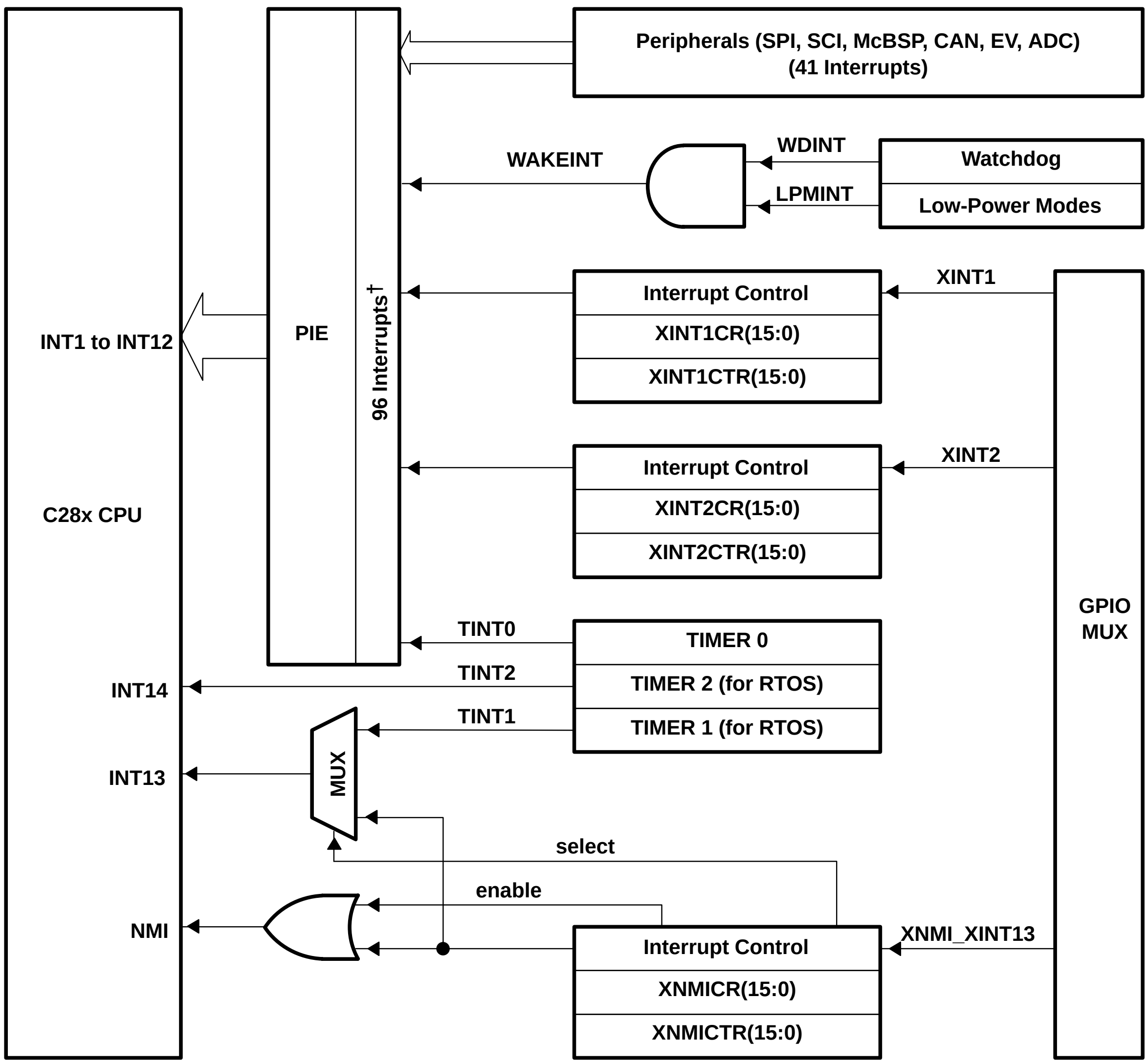
The XREVISION register contains a unique number to identify the particular version of XINTF used in the product. For the F2812, this register will be configured as described in Table 3–9.

Table 3–9. XREVISION Register Bit Defintions

BIT(S)	NAME	TYPE	RESET	DESCRIPTION
15–0	REVISION	R	0x0004	Current XINTF Revision. For internal use/reference. Test purposes only. Subject to change.

3.6 Interrupts

Figure 3–6 shows how the various interrupt sources are multiplexed within the F2810 and F2812 devices.



† Out of a possible 96 interrupts, 45 are currently used by peripherals.

Figure 3–6. Interrupt Sources

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Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. On the F2810/F2812, 45 of these are used by peripherals as shown in Table 3–10.

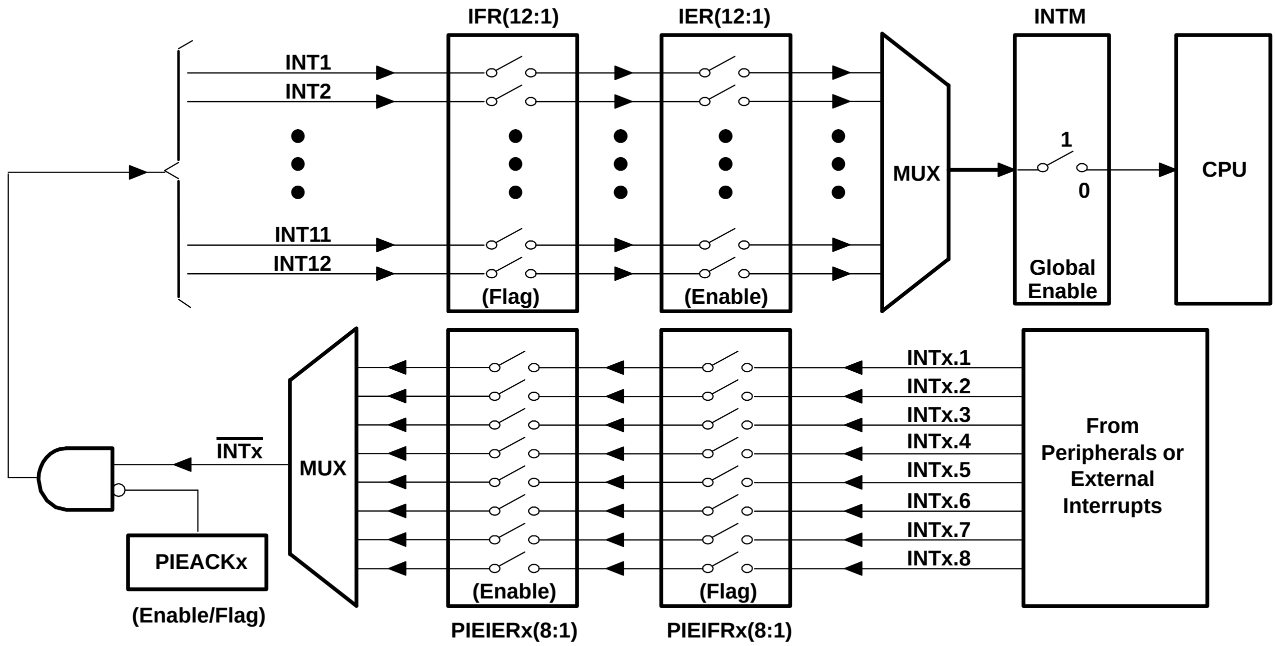

Figure 3–7. Multiplexing of Interrupts Using the PIE Block

Table 3–10. PIE Peripheral Interrupts†

CPU INTERRUPTS	PIE INTERRUPTS							
	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1	$\overline{\text{WAKEINT}}$ (LPM/WD)	TINT0 (TIMER 0)	ADCINT (ADC)	XINT2	XINT1	reserved	PDPINTB (EV-B)	PDPINTA (EV-A)
INT2	reserved	T1OFINT (EV-A)	T1UFINT (EV-A)	T1CINT (EV-A)	T1PINT (EV-A)	CMP3INT (EV-A)	CMP2INT (EV-A)	CMP1INT (EV-A)
INT3	reserved	CAPINT3 (EV-A)	CAPINT2 (EV-A)	CAPINT1 (EV-A)	T2OFINT (EV-A)	T2UFINT (EV-A)	T2CINT (EV-A)	T2PINT (EV-A)
INT4	reserved	T3OFINT (EV-B)	T3UFINT (EV-B)	T3CINT (EV-B)	T3PINT (EV-B)	CMP6INT (EV-B)	CMP5INT (EV-B)	CMP4INT (EV-B)
INT5	reserved	CAPINT6 (EV-B)	CAPINT5 (EV-B)	CAPINT4 (EV-B)	T4OFINT (EV-B)	T4UFINT (EV-B)	T4CINT (EV-B)	T4PINT (EV-B)
INT6	reserved	reserved	MXINT (McBSP)	MRINT (McBSP)	reserved	reserved	SPITXINTA (SPI)	SPIRXINTA (SPI)
INT7	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
INT8	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
INT9	reserved	reserved	ECAN1INT (CAN)	ECAN0INT (CAN)	SCITXINTB (SCI-B)	SCIRXINTB (SCI-B)	SCITXINTA (SCI-A)	SCIRXINTA (SCI-A)
INT10	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
INT11	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
INT12	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

† Out of the 96 possible interrupts, 45 interrupts are currently used. the remaining interrupts are reserved for future devices. However, these interrupts can be used as software interrupts if they are enabled at the PIEIFRx level.

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3.6.1 External Interrupts

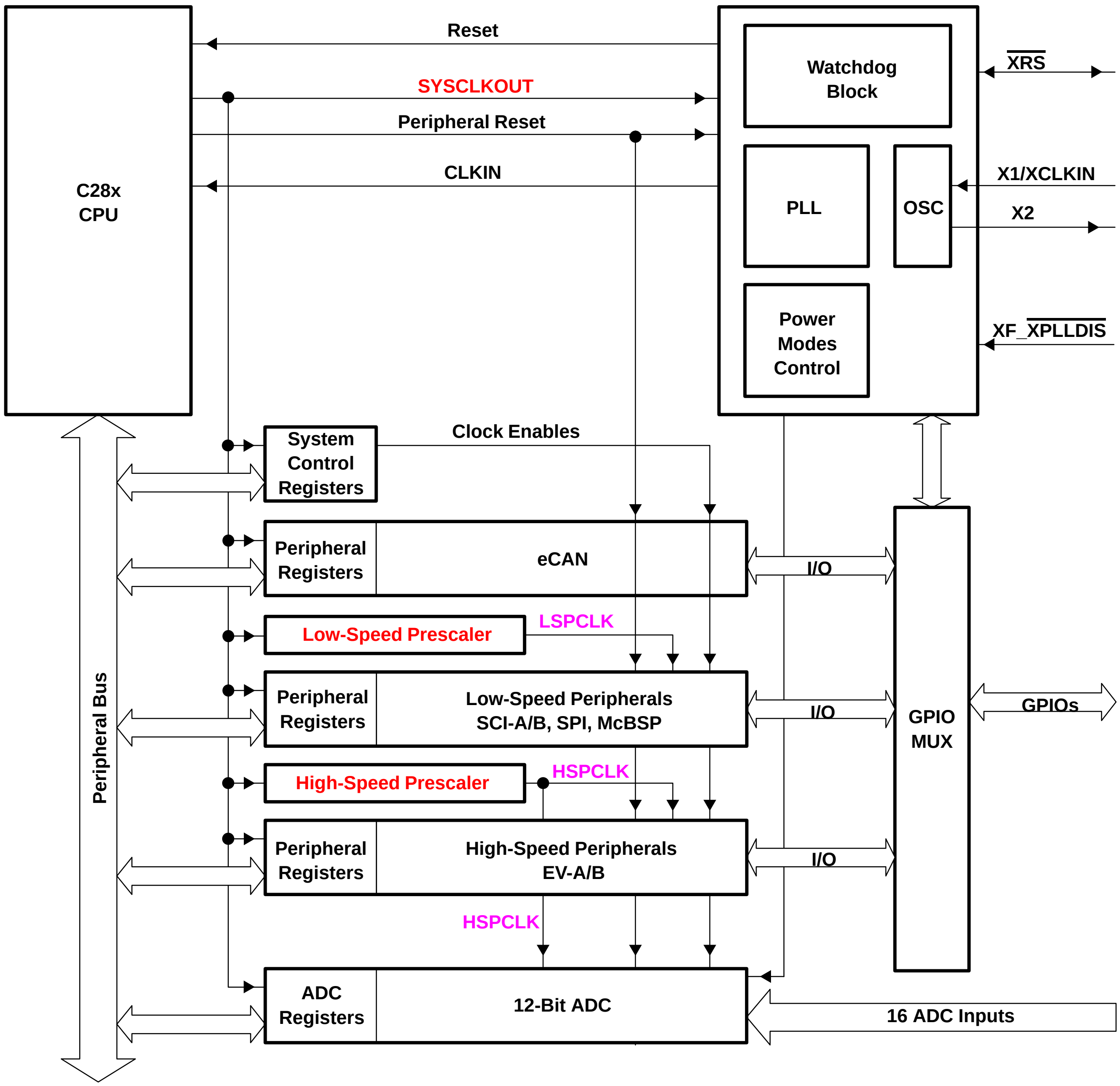
Table 3–11. External Interrupts Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XINT1CR	0x00 7070	1	XINT1 control register
XINT2CR	0x00 7071	1	XINT2 control register
reserved	0x00 7072 0x00 7076	5	
XNMICR	0x00 7077	1	XNMI control register
XINT1CTR	0x00 7078	1	XINT1 counter register
XINT2CTR	0x00 7079	1	XINT2 counter register
reserved	0x00 707A 0x00 707E	5	
XNMICTR	0x00 707F	1	XNMI counter register

Each external interrupt can be enabled/disabled or qualified using positive or negative going edge. For more information, see the *TMS320F28x System Control and Interrupts Peripheral Reference Guide* (literature number SPRU078).

3.7 System Control

This section describes the F2810 and F2812 oscillator, PLL and clocking mechanisms, the watchdog function and the low power modes. Figure 3–8 shows the various clock and reset domains in the F2810 and F2812 devices that will be discussed.



NOTE A: CLKIN is the clock input to the CPU. SYSCLKOUT is the output clock of the CPU. They are of the same frequency.

Figure 3–8. Clock and Reset Domains

The PLL, clocking, watchdog and low-power modes, are controlled by the registers listed in Table 3–12.

Table 3–12. PLL, Clocking, Watchdog, and Low-Power Mode Registers†

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
reserved	0x00 7010 0x00 7017	8	
reserved	0x00 7018	1	
reserved	0x00 7019	1	
HISPCP	0x00 701A	1	High-Speed Peripheral Clock Prescaler Register for HSPCLK clock
LOSPCP	0x00 701B	1	Low-Speed Peripheral Clock Prescaler Register for LSPCLK clock
PCLKCR	0x00 701C	1	Peripheral Clock Control Register
reserved	0x00 701D	1	
LPMCR0	0x00 701E	1	Low Power Mode Control Register 0
LPMCR1	0x00 701F	1	Low Power Mode Control Register 1
reserved	0x00 7020	1	
PLLCR	0x00 7021	1	PLL Control Register‡
SCSR	0x00 7022	1	System Control & Status Register
WDCNTR	0x00 7023	1	Watchdog Counter Register
reserved	0x00 7024	1	
WDKEY	0x00 7025	1	Watchdog Reset Key Register
reserved	0x00 7026 0x00 7028	3	
WDCR	0x00 7029	1	Watchdog Control Register
reserved	0x00 702A 0x00 702F	6	

† All of the above registers can only be accessed, by executing the EALLOW instruction.
‡ The PLL control register (PLLCR) is reset to a known state by the $\overline{XRS}$ signal only. Emulation reset (through Code Composer Studio) will not reset PLLCR.

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3.8 OSC and PLL Block

Figure 3–9 shows the OSC and PLL block on the F2810 and F2812.

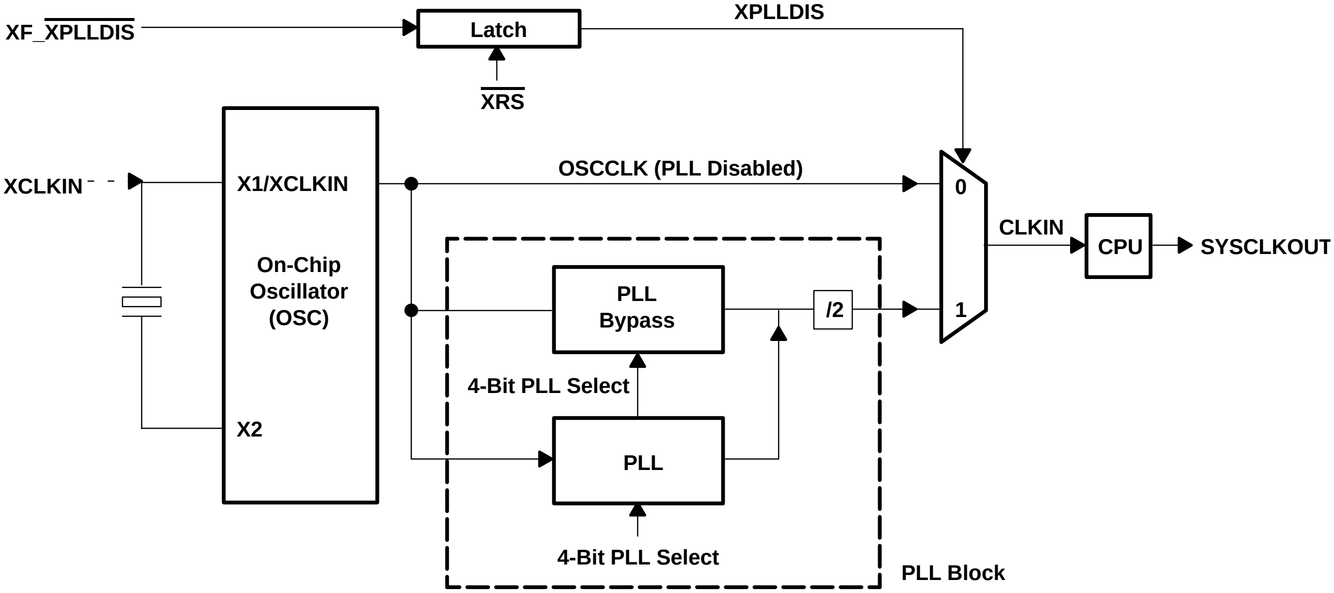

Figure 3–9. OSC and PLL Block

The on-chip oscillator circuit enables a crystal to be attached to the F2810 and F2812 devices using the X1/XCLKIN and X2 pins. If a crystal is not used, then an external oscillator can be directly connected to the X1/XCLKIN pin and the X2 pin is left unconnected. The logic-high level in this case should not exceed V_{DD}. The oscillator input range is 20 MHz to 35 MHz. The PLLCR bits [3:0] set the clocking ratio.

Table 3–13. PLLCR Register Bit Definitions

BIT(S)	NAME	TYPE	$\overline{XRS}$ RESET†	DESCRIPTION
15:4	reserved	R = 0	0:0	
3:0	DIV	R/W	0,0,0,0	SYSCLKOUT = (XCLKIN * n)/2, where n is the PLL multiplication factor. **Bit Value** / **n** / **SYSCLKOUT** 0000 / PLL Bypassed / XCLKIN/2 0001 / 1 / XCLKIN/2 0010 / 2 / XCLKIN 0011 / 3 / XCLKIN * 1.5 0100 / 4 / XCLKIN * 2 0101 / 5 / XCLKIN * 2.5 0110 / 6 / XCLKIN * 3 0111 / 7 / XCLKIN * 3.5 1000 / 8 / XCLKIN * 4 1001 / 9 / XCLKIN * 4.5 1010 / 10 / XCLKIN * 5 1011 / 11 / Reserved 1100 / 12 / Reserved 1101 / 13 / Reserved 1110 / 14 / Reserved 1111 / 15 / Reserved

† The PLLCR register is reset to a known state by the $\overline{XRS}$ reset line. **If a reset is issued by the debugger, the PLL clocking ratio is not changed.**

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3.8.1 Loss of Input Clock

In PLL enabled mode, if the input clock XCLKIN or the oscillator clock is removed or absent, the PLL will still issue a “limp-mode” clock. The limp-mode clock will continue to clock the CPU and peripherals at a typical frequency of 1–4 MHz. The PLLCR register should have been written to with a non-zero value for this feature to work.

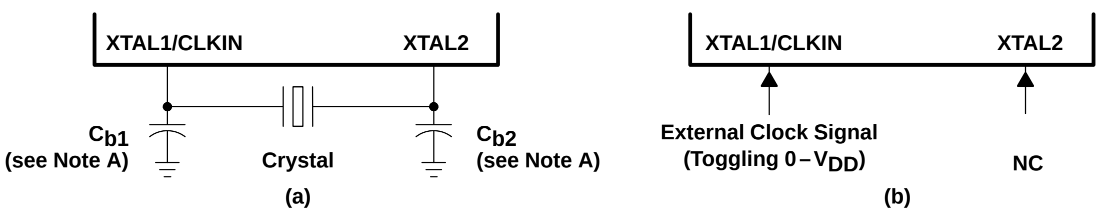
Normally, when the input clocks are present, the watchdog counter will decrement to initiate a watchdog reset or WDINT interrupt. However, when the external input clock fails, the watchdog counter will stop decrementing (i.e., the watchdog counter does not change with the limp-mode clock). This condition could be used by the application firmware to detect the input clock failure and initiate necessary shut-down procedure for the system. The MIN, TYP, and MAX frequencies for the limp-mode clock will be published in the TMS data sheet.

3.9 PLL-Based Clock Module

The F2810 and F2812 have an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 4-bit ratio control to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. It can be re-enabled (if need be) after the PLL module has stabilized, which takes 131 072 XCLKIN cycles.

The PLL-based clock module provides two modes of operation:

- Crystal-operation
  This mode allows the use of an external crystal/resonator to provide the time base to the device.
- External clock source operation
  This mode allows the internal oscillator to be bypassed. The device clocks are generated from an external clock source input on the X1/XCLKIN pin.



NOTE A: TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the DSP chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will ensure start-up and stability over the entire operating range.

Figure 3–10. Recommended Crystal / Clock Connection

Table 3–14. Possible PLL Configuration Modes

PLL MODE	REMARKS	SYSCLKOUT
PLL Disabled	Invoked by tying $\overline{\text{XPLLDIS}}$ pin low upon reset. PLL block is completely disabled. Clock input to the CPU (CLKIN) is directly derived from the clock signal present at the X1/XCLKIN pin.	XCLKIN
PLL Bypassed	Default PLL configuration upon power-up, if PLL is not disabled. The PLL itself is bypassed. However, the /2 module in the PLL block divides the clock input at the X1/XCLKIN pin by two before feeding it to the CPU.	XCLKIN/2
PLL Enabled	Achieved by writing a non-zero value “n” into PLLCR register. The /2 module in the PLL block now divides the output of the PLL by two before feeding it to the CPU.	(XCLKIN * n) / 2

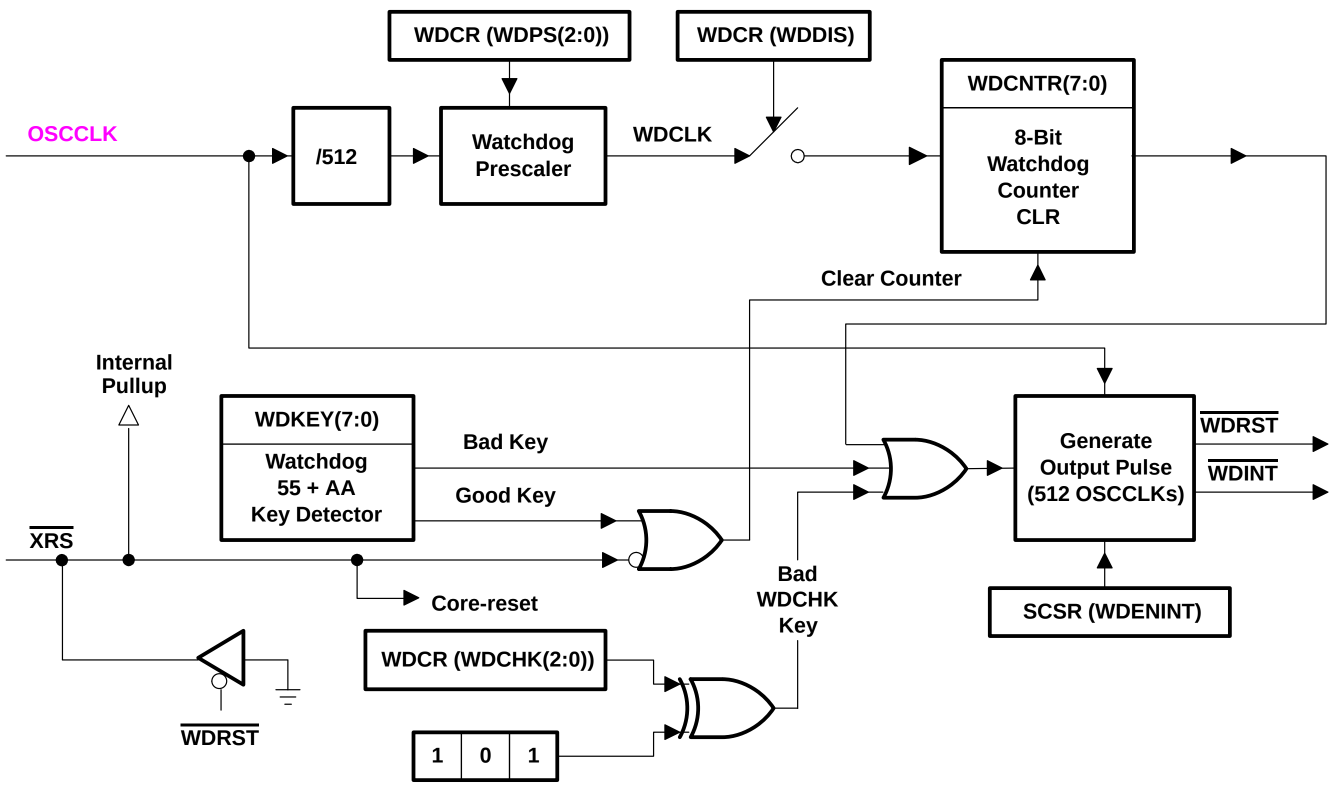
3.10 External Reference Oscillator Clock Option

The typical specifications for the external quartz crystal for a frequency of 30 MHz are listed below:

- Fundamental mode, parallel resonant
- C_L (load capacitance) = 12 pF
- $C_{L1} = C_{L2}$ = 24 pF
- C_{shunt} = 6 pF
- ESR range = 25 to 40 Ω

3.11 Watchdog Block

The watchdog block on the F2810 and F2812 is identical to the one used on the 240x devices. The watchdog module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this, the user disables the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register which will reset the watchdog counter. Figure 3–11 shows the various functional blocks within the watchdog module.



NOTE A: The $\overline{\text{WDRST}}$ signal is driven low for 512 OSCCLK cycles.

Figure 3–11. Watchdog Module

The $\overline{\text{WDINT}}$ signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode timer.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the watchdog. The WATCHDOG module will run off the PLL clock or the oscillator clock. The $\overline{\text{WDINT}}$ signal is fed to the LPM block so that it can wake the device from STANDBY (if enabled). Refer to Section 3.12, Low-Power Modes Block, for more details.

In IDLE mode, the $\overline{\text{WDINT}}$ signal can generate an interrupt to the CPU, via the PIE, to take the CPU out of IDLE mode.

In HALT mode, this feature cannot be used because the oscillator (and PLL) are turned off and hence so is the WATCHDOG.

3.12 Low-Power Modes Block

The low-power modes on the F2810 and F2812 are similar to the 240x devices. Table 3–15 summarizes the various modes.

Table 3–15. F2810 and F2812 Low-Power Modes

MODE	IDLES	LPM(1:0)	OSCCLK	CLKIN	SYSCLKOUT	EXIT†
Normal	low	X,X	on	on	on	–
IDLE	high	0,0	on	on	on‡	$\overline{\text{XRS}}$, $\overline{\text{WDINT}}$, Any Enabled Interrupt, XNMI Debugger§
STANDBY	high	0,1	on (watchdog still running)	off	off	$\overline{\text{XRS}}$, $\overline{\text{WDINT}}$, XINT1, XNMI, $\overline{\text{T1/2/3/4CTRIP}}$, $\overline{\text{C1/2/3/4/5/6TRIP}}$, SCIRXDA, SCIRXDB, CANRX, Debugger§
HALT	high	1,X	off (oscillator and PLL turned off, watchdog not functional)	off	off	$\overline{\text{XRS}}$, XNMI, Debugger§

† The Exit column lists which signals or under what conditions the low power mode will be exited. A low signal, on any of the signals, will exit the low power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise the IDLE mode will not be exited and the device will go back into the indicated low power mode.
‡ The IDLE mode on the C28x behaves differently than on the 24x/240x. On the C28x, the clock output from the core (SYSCLKOUT) is still functional while on the 24x/240x the clock is turned off.
§ On the C28x, the JTAG port can still function even if the core clock (CLKIN) is turned off.

The various low-power modes operate as follows:

IDLE Mode: This mode is, exited by any enabled interrupt or an NMI that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.

STANDBY Mode: All other signals (including XNMI) will wake the device from STANDBY mode if selected by the LPMCR1 register. The user will need to select which signal(s) will wake the device. The selected signal(s) are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.

HALT Mode: Only the $\overline{\text{XRS}}$ and XNMI external signals can wake the device from HALT mode. The XNMI input to the core has an enable/disable bit. Hence, it is safe to use the XNMI signal for this function.

NOTE: The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed.

4 Peripherals

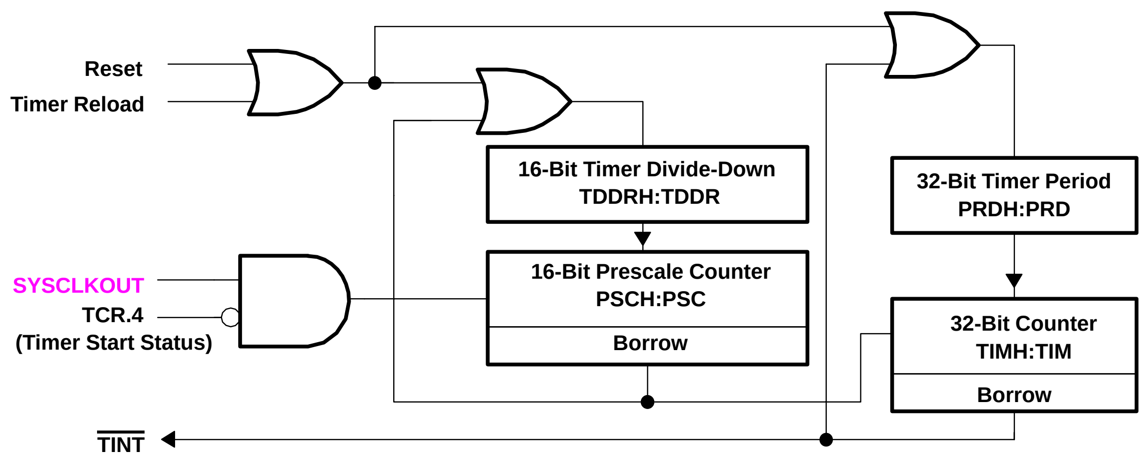
The integrated peripherals of the F2810 and F2812 are described in the following subsections:

- Three 32-bit CPU-Timers
- Two event-manager modules (EVA, EVB)
- Enhanced analog-to-digital converter (ADC) module
- Enhanced controller area network (eCAN) module
- Multichannel buffered serial port (McBSP) module
- Serial communications interface modules (SCI-A, SCI-B)
- Serial peripheral interface (SPI) module
- Digital I/O and shared pin functions

4.1 32-Bit CPU-Timers 0/1/2

There are three 32-bit CPU-timers on the F2810 and F2812 devices (CPU-TIMER0/1/2).

CPU-Timers 1 and 2 are reserved for the Real-Time OS (such as DSP-BIOS).† CPU-Timer 0 can be used in user applications. These timers are different from the general-purpose (GP) timers that are present in the Event Manager modules (EVA, EVB).



NOTE A: The CPU-Timers are different from the general-purpose (GP) timers that are present in the Event Manager modules (EVA, EVB).

Figure 4–1. CPU-Timers

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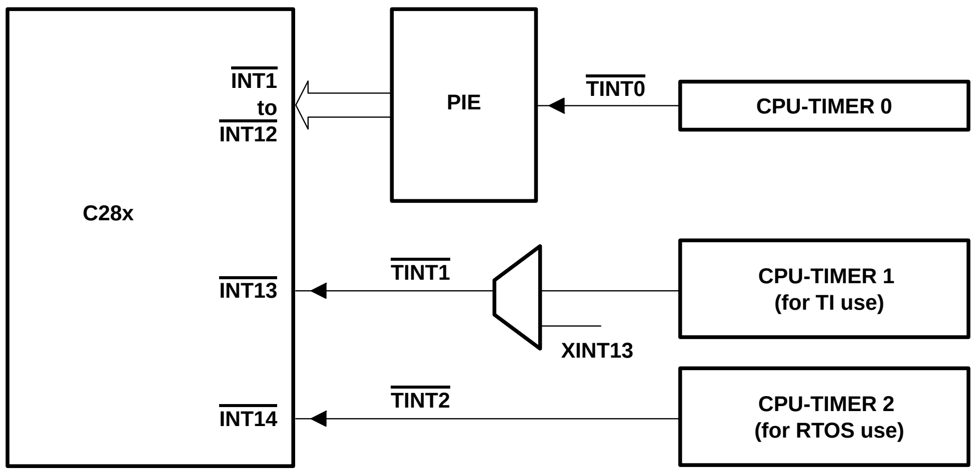
† If the application is not using BIOS, then CPU-Timers 1 and 2 can be used in the application.

In the F2810 and F2812 devices, the timer interrupt signals ($\overline{\text{TINT0}}$, $\overline{\text{TINT1}}$, $\overline{\text{TINT2}}$) are connected as shown in Figure 4–2.



NOTES: A. The timer registers are connected to the Memory Bus of the C28x processor.
B. The timing of the timers is synchronized to SYSCLKOUT of the processor clock.

Figure 4–2. CPU-Timer Interrupts Signals and Output Signal

The general operation of the timer is as follows: The 32-bit counter register “TIMH:TIM” is loaded with the value in the period register “PRDH:PRD”. The counter register, decrements at the SYSCLKOUT rate of the C28x. When the counter reaches 0, a timer interrupt output signal generates an interrupt pulse. The registers listed in Table 4–1 are used to configure the timers. For more information, see the *TMS320F28x System Control and Interrupts Peripheral Reference Guide* (literature number SPRU078).

Table 4–1. CPU-Timers 0, 1, 2 Configuration and Control Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
TIMER0TIM	0x00 0C00	1	CPU-Timer 0, Counter Register
TIMER0TIMH	0x00 0C01	1	CPU-Timer 0, Counter Register High
TIMER0PRD	0x00 0C02	1	CPU-Timer 0, Period Register
TIMER0PRDH	0x00 0C03	1	CPU-Timer 0, Period Register High
TIMER0TCR	0x00 0C04	1	CPU-Timer 0, Control Register
reserved	0x00 0C05	1	
TIMER0TPR	0x00 0C06	1	CPU-Timer 0, Prescale Register
TIMER0TPRH	0x00 0C07	1	CPU-Timer 0, Prescale Register High
TIMER1TIM	0x00 0C08	1	CPU-Timer 1, Counter Register
TIMER1TIMH	0x00 0C09	1	CPU-Timer 1, Counter Register High
TIMER1PRD	0x00 0C0A	1	CPU-Timer 1, Period Register
TIMER1PRDH	0x00 0C0B	1	CPU-Timer 1, Period Register High
TIMER1TCR	0x00 0C0C	1	CPU-Timer 1, Control Register
reserved	0x00 0C0D	1	
TIMER1TPR	0x00 0C0E	1	CPU-Timer 1, Prescale Register
TIMER1TPRH	0x00 0C0F	1	CPU-Timer 1, Prescale Register High
TIMER2TIM	0x00 0C10	1	CPU-Timer 2, Counter Register
TIMER2TIMH	0x00 0C11	1	CPU-Timer 2, Counter Register High
TIMER2PRD	0x00 0C12	1	CPU-Timer 2, Period Register
TIMER2PRDH	0x00 0C13	1	CPU-Timer 2, Period Register High
TIMER2TCR	0x00 0C14	1	CPU-Timer 2, Control Register
reserved	0x00 0C15	1	
TIMER2TPR	0x00 0C16	1	CPU-Timer 2, Prescale Register
TIMER2TPRH	0x00 0C17	1	CPU-Timer 2, Prescale Register High
reserved	0x00 0C18 0x00 0C3F	40	

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4.2 Event Manager Modules (EVA, EVB)

The event-manager modules include general-purpose (GP) timers, full-compare/PWM units, capture units, and quadrature-encoder pulse (QEP) circuits. EVA's and EVB's timers, compare units, and capture units function identically. However, timer/unit names differ for EVA and EVB. Table 4–2 shows the module and signal names used. Table 4–2 shows the features and functionality available for the event-manager modules and highlights EVA nomenclature.

Event managers A and B have identical peripheral register sets with EVA starting at 7400h and EVB starting at 7500h. The paragraphs in this section describe the function of GP timers, compare units, capture units, and QEPs using EVA nomenclature. These paragraphs are applicable to EVB with regard to function—however, module/signal names would differ. Table 4–3 lists the EVA registers. For more information, see the *TMS320F28x DSP Event Manager (EV) Reference Guide* (literature number SPRU065).

Table 4–2. Module and Signal Names for EVA and EVB

EVENT MANAGER MODULES	EVA		EVB	
	MODULE	SIGNAL	MODULE	SIGNAL
GP Timers	GP Timer 1 GP Timer 2	T1PWM/T1CMP T2PWM/T2CMP	GP Timer 3 GP Timer 4	T3PWM/T3CMP T4PWM/T4CMP
Compare Units	Compare 1 Compare 2 Compare 3	PWM1/2 PWM3/4 PWM5/6	Compare 4 Compare 5 Compare 6	PWM7/8 PWM9/10 PWM11/12
Capture Units	Capture 1 Capture 2 Capture 3	CAP1 CAP2 CAP3	Capture 4 Capture 5 Capture 6	CAP4 CAP5 CAP6
QEP Channels	QEP1 QEP2 QEPI1	QEP1 QEP2	QEP3 QEP4 QEPI2	QEP3 QEP4
External Clock Inputs	Direction External Clock	TDIRA TCLKINA	Direction External Clock	TDIRB TCLKINB
External Compare Inputs	Compare	$\overline{\text{C1TRIP}}$ $\overline{\text{C2TRIP}}$ $\overline{\text{C3TRIP}}$		$\overline{\text{C4TRIP}}$ $\overline{\text{C5TRIP}}$ $\overline{\text{C6TRIP}}$
External Trip Inputs		$\overline{\text{T1CTRIP\_PDPINTA}}$ † $\overline{\text{T2CTRIP}}$/EVASOC		$\overline{\text{T3CTRIP\_PDPINTB}}$ † $\overline{\text{T4CTRIP}}$/EVBSOC

† In the 24x/240x-compatible mode, the $\overline{\text{T1CTRIP\_PDPINTA}}$ pin functions as $\overline{\text{PDPINTA}}$ and the $\overline{\text{T3CTRIP\_PDPINTB}}$ pin functions as $\overline{\text{PDPINTB}}$.

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Table 4–3. EVA Registers†

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPTCONA	0x00 7400	1	GP Timer Control Register A
T1CNT	0x00 7401	1	GP Timer 1 Counter Register
T1CMPR	0x00 7402	1	GP Timer 1 Compare Register
T1PR	0x00 7403	1	GP Timer 1 Period Register
T1CON	0x00 7404	1	GP Timer 1 Control Register
T2CNT	0x00 7405	1	GP Timer 2 Counter Register
T2CMPR	0x00 7406	1	GP Timer 2 Compare Register
T2PR	0x00 7407	1	GP Timer 2 Period Register
T2CON	0x00 7408	1	GP Timer 2 Control Register
EXTCONA‡	0x00 7409	1	GP Extension Control Register A
COMCONA	0x00 7411	1	Compare Control Register A
ACTRA	0x00 7413	1	Compare Action Control Register A
DBTCONA	0x00 7415	1	Dead-Band Timer Control Register A
CMPR1	0x00 7417	1	Compare Register 1
CMPR2	0x00 7418	1	Compare Register 2
CMPR3	0x00 7419	1	Compare Register 3
CAPCONA	0x00 7420	1	Capture Control Register A
CAPFIFOA	0x00 7422	1	Capture FIFO Status Register A
CAP1FIFO	0x00 7423	1	Two-Level Deep Capture FIFO Stack 1
CAP2FIFO	0x00 7424	1	Two-Level Deep Capture FIFO Stack 2
CAP3FIFO	0x00 7425	1	Two-Level Deep Capture FIFO Stack 3
CAP1FBOT	0x00 7427	1	Bottom Register Of Capture FIFO Stack 1
CAP2FBOT	0x00 7428	1	Bottom Register Of Capture FIFO Stack 2
CAP3FBOT	0x00 7429	1	Bottom Register Of Capture FIFO Stack 3
EVAIMRA	0x00 742C	1	Interrupt Mask Register A
EVAIMRB	0x00 742D	1	Interrupt Mask Register B
EVAIMRC	0x00 742E	1	Interrupt Mask Register C
EVAIFRA	0x00 742F	1	Interrupt Flag Register A
EVAIFRB	0x00 7430	1	Interrupt Flag Register B
EVAIFRC	0x00 7431	1	Interrupt Flag Register C

† The EV-B register set is identical except the address range is from 0x00–7500 to 0x00–753F. The above registers are mapped to Zone 2. This space allows only 16-bit accesses. 32-bit accesses produce undefined results.
‡ New register compared to 24x/240x

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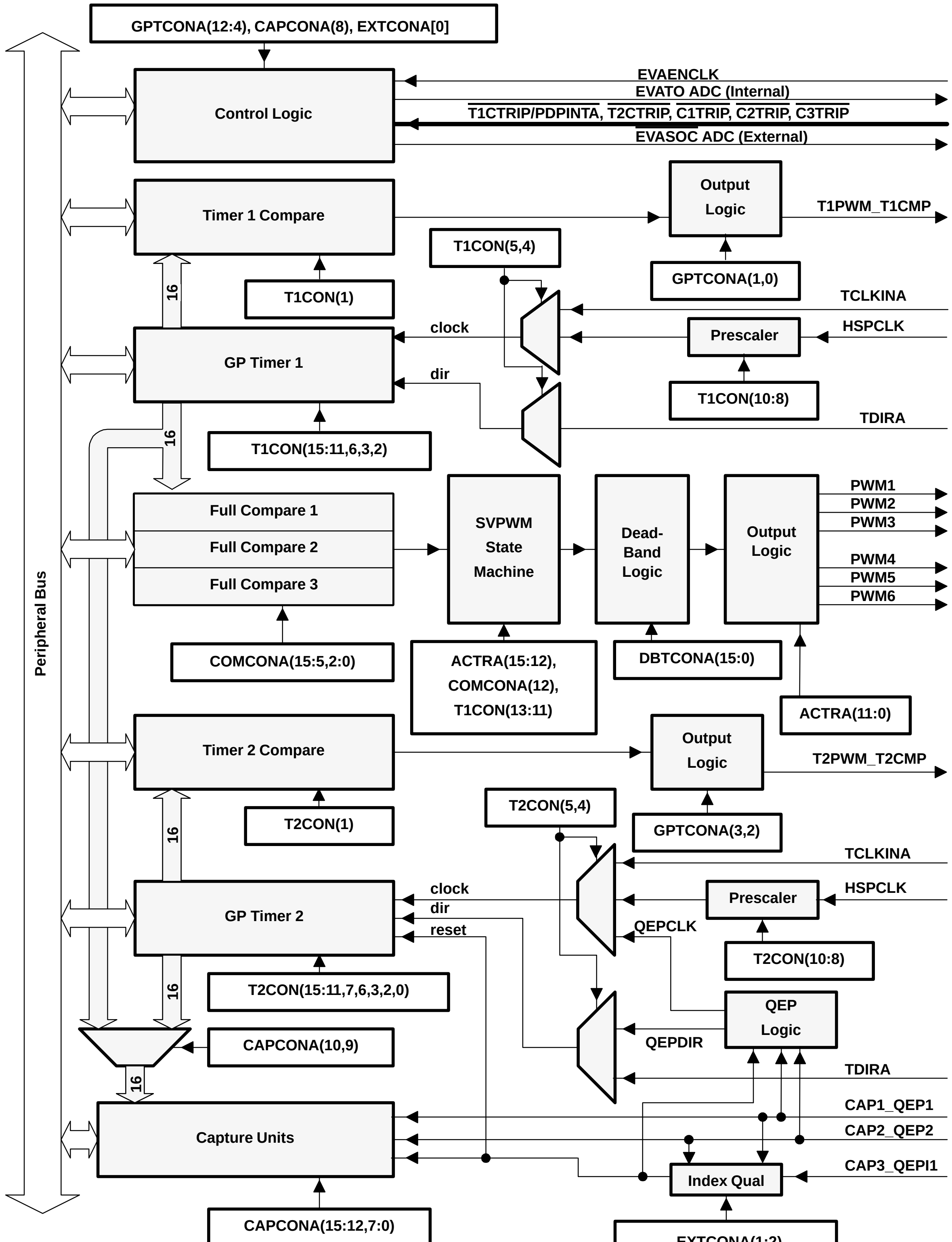

NOTE A: The EVB module is similar to the EVA module.

Figure 4–3. Event Manager A Functional Block Diagram

4.2.1 General-Purpose (GP) Timers

There are two GP timers. The GP timer x (x = 1 or 2 for EVA; x = 3 or 4 for EVB) includes:

- A 16-bit timer, up-/down-counter, TxCNT, for reads or writes
- A 16-bit timer-compare register, TxCMPR (double-buffered with shadow register), for reads or writes
- A 16-bit timer-period register, TxPR (double-buffered with shadow register), for reads or writes
- A 16-bit timer-control register,TxCON, for reads or writes
- Selectable internal or external input clocks
- A programmable prescaler for internal or external clock inputs
- Control and interrupt logic, for four maskable interrupts: *underflow*, *overflow*, *timer compare*, and *period interrupts*
- A selectable direction input pin (TDIRx) (to count up or down when directional up-/down-count mode is selected)

The GP timers can be operated independently or synchronized with each other. The compare register associated with each GP timer can be used for compare function and PWM-waveform generation. There are three continuous modes of operations for each GP timer in up- or up/down-counting operations. Internal or external input clocks with programmable prescaler are used for each GP timer. GP timers also provide the time base for the other event-manager submodules: GP timer 1 for all the compares and PWM circuits, GP timer 2/1 for the capture units and the quadrature-pulse counting operations. Double-buffering of the period and compare registers allows programmable change of the timer (PWM) period and the compare/PWM pulse width as needed.

4.2.2 Full-Compare Units

There are three full-compare units on each event manager. These compare units use GP timer1 as the time base and generate six outputs for compare and PWM-waveform generation using programmable deadband circuit. The state of each of the six outputs is configured independently. The compare registers of the compare units are double-buffered, allowing programmable change of the compare/PWM pulse widths as needed.

4.2.3 Programmable Deadband Generator

Deadband generation can be enabled/disabled for each compare unit output individually. The deadband-generator circuit produces two outputs (with or without deadband zone) for each compare unit output signal. The output states of the deadband generator are configurable and changeable as needed by way of the double-buffered ACTRx register.

4.2.4 PWM Waveform Generation

Up to eight PWM waveforms (outputs) can be generated simultaneously by each event manager: three independent pairs (six outputs) by the three full-compare units with *programmable deadbands*, and two independent PWMs by the GP-timer compares.

4.2.5 Double Update PWM Mode

The F2810/F2812 Event Manager supports “Double Update PWM Mode.” This mode refers to a PWM operation mode in which the position of the leading edge and the position of the trailing edge of a PWM pulse are independently modifiable in each PWM period. To support this mode, the compare register that determines the position of the edges of a PWM pulse must allow (buffered) compare value update once at the beginning of a PWM period and another time in the middle of a PWM period. The compare registers in F2810/F2812 Event Managers are all buffered and support three compare value reload/update (value in buffer becoming active) modes. These modes have earlier been documented as compare value reload conditions. The reload condition that supports double update PWM mode is reloaded on Underflow (beginning of PWM period) OR Period (middle of PWM period). Double update PWM mode can be achieved by using this condition for compare value reload.

4.2.6 PWM Characteristics

Characteristics of the PWMs are as follows:

- 16-bit registers
- Wide range of programmable deadband for the PWM output pairs
- Change of the PWM carrier frequency for PWM frequency wobbling as needed
- Change of the PWM pulse widths within and after each PWM period as needed
- External-maskable power and drive-protection interrupts
- Pulse-pattern-generator circuit, for programmable generation of asymmetric, symmetric, and four-space vector PWM waveforms
- Minimized CPU overhead using auto-reload of the compare and period registers
- The PWM pins are driven to a high-impedance state when the $\overline{\text{PDPINTx}}$ pin is driven low and **after** $\overline{\text{PDPINTx}}$ signal qualification. The $\overline{\text{PDPINTx}}$ pin (after qualification) is reflected in bit 8 of the COMCONx register.
  - $\overline{\text{PDPINTA}}$ pin status is reflected in bit 8 of COMCONA register.
  - $\overline{\text{PDPINTB}}$ pin status is reflected in bit 8 of COMCONB register.
- EXTCON register bits provide options to individually trip control for each PWM pair of signals

4.2.7 Capture Unit

The capture unit provides a logging function for different events or transitions. The values of the selected GP timer counter is captured and stored in the two-level-deep FIFO stacks when selected transitions are detected on capture input pins, CAPx (x = 1, 2, or 3 for EVA; and x = 4, 5, or 6 for EVB). The capture unit consists of three capture circuits.

- Capture units include the following features:
  - One 16-bit capture control register, CAPCONx (R/W)
  - One 16-bit capture FIFO status register, CAPFIFOx
  - Selection of GP timer 1/2 (for EVA) or 3/4 (for EVB) as the time base
  - Three 16-bit 2-level-deep FIFO stacks, one for each capture unit
  - Three capture input pins (CAP1/2/3 for EVA, CAP4/5/6 for EVB)—one input pin per capture unit. [All inputs are synchronized with the device (CPU) clock. In order for a transition to be captured, the input must hold at its current level to meet the input qualification circuitry requirements. The input pins CAP1/2 and CAP4/5 can also be used as QEP inputs to the QEP circuit.]
  - User-specified transition (rising edge, falling edge, or both edges) detection
  - Three maskable interrupt flags, one for each capture unit
  - The capture pins can also be used as general-purpose interrupt pins, if they are not used for the capture function.

4.2.8 Quadrature-Encoder Pulse (QEP) Circuit

Two capture inputs (CAP1 and CAP2 for EVA; CAP4 and CAP5 for EVB) can be used to interface the on-chip QEP circuit with a quadrature encoder pulse. Full synchronization of these inputs is performed on-chip. Direction or leading-quadrature pulse sequence is detected, and GP timer 2/4 is incremented or decremented by the rising and falling edges of the two input signals (four times the frequency of either input pulse).

With EXTCONA register bits, the EVA QEP circuit can use CAP3 as a capture index pin as well. Similarly, with EXTCONB register bits, the EVB QEP circuit can use CAP6 as a capture index pin.

4.2.9 External ADC Start-of-Conversion

EVA/EVB start-of-conversion (SOC) can be sent to an external pin ($\overline{\text{EVASOC}}$/$\overline{\text{EVBSOC}}$) for external ADC interface. $\overline{\text{EVASOC}}$ and $\overline{\text{EVBSOC}}$ are muxed with $\overline{\text{T2CTRIP}}$ and $\overline{\text{T4CTRIP}}$, respectively.

4.3 Enhanced Analog-to-Digital Converter (ADC) Module

A simplified functional block diagram of the ADC module is shown in Figure 4–4. The ADC module consists of a 12-bit ADC with a built-in sample-and-hold (S/H) circuit. Functions of the ADC module include:

- 12-bit ADC core with built-in S/H
- Analog input: 0.0 V to 3.0 V (Voltages above 3.0 V produce full-scale conversion results.)
- Fast conversion rate: 80 ns at 25-MHz ADC clock, 12.5 MSPS
- 16-channel, muxed inputs
- Autosequencing capability provides up to 16 “autoconversions” in a single session. Each conversion can be programmed to select any 1 of 16 input channels
- Sequencer can be operated as two independent 8-state sequencers or as one large 16-state sequencer (i.e., two cascaded 8-state sequencers)
- Sixteen result registers (individually addressable) to store conversion values
  – The digital value of the input analog voltage is derived by:

$$\text{Digital Value} = 4095 \times \frac{\text{Input Analog Voltage} - \text{ADCLO}}{3}$$

- Multiple triggers as sources for the start-of-conversion (SOC) sequence
  – S/W – software immediate start
  – EVA – Event manager A (multiple event sources within EVA)
  – EVB – Event manager B (multiple event sources within EVB)
- Flexible interrupt control allows interrupt request on every end-of-sequence (EOS) or every other EOS
- Sequencer can operate in “start/stop” mode, allowing multiple “time-sequenced triggers” to synchronize conversions
- EVA and EVB triggers can operate independently in dual-sequencer mode
- Sample-and-hold (S/H) acquisition time window has separate prescale control

The ADC module in the F2810 and F2812 has been enhanced to provide flexible interface to event managers A and B. The ADC interface is built around a fast, 12-bit ADC module with a fast conversion rate of 80 ns at 25-MHz ADC clock. The ADC module has 16 channels, configurable as two independent 8-channel modules to service event managers A and B. The two independent 8-channel modules can be cascaded to form a 16-channel module. Although there are multiple input channels and two sequencers, there is only one converter in the ADC module. Figure 4–4 shows the block diagram of the F2810 and F2812 ADC module.

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The two 8-channel modules have the capability to autosequence a series of conversions, each module has the choice of selecting any one of the respective eight channels available through an analog mux. In the cascaded mode, the autosequencer functions as a single 16-channel sequencer. On each sequencer, once the conversion is complete, the selected channel value is stored in its respective RESULT register. Autosequencing allows the system to convert the same channel multiple times, allowing the user to perform oversampling algorithms. This gives increased resolution over traditional single-sampled conversion results.

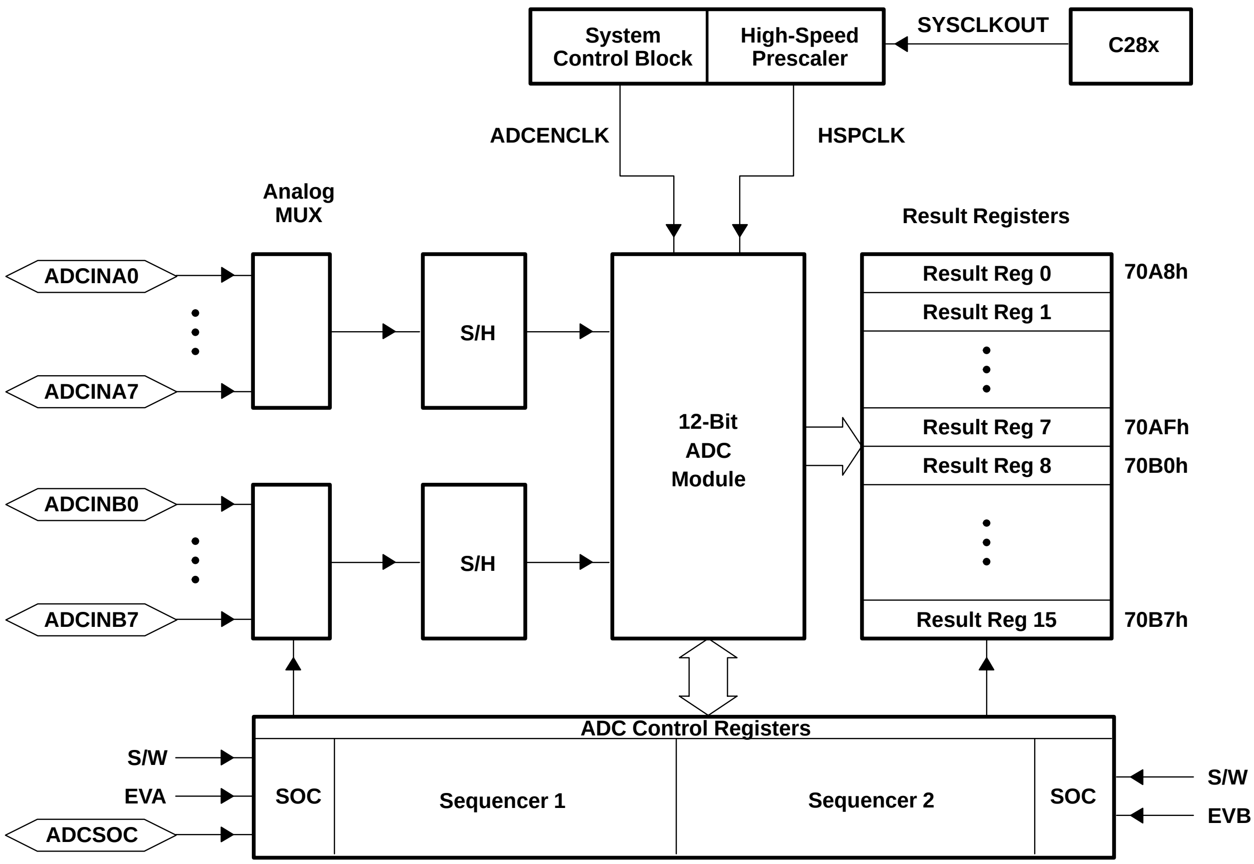


Figure 4–4. Block Diagram of the F2810 and F2812 ADC Module

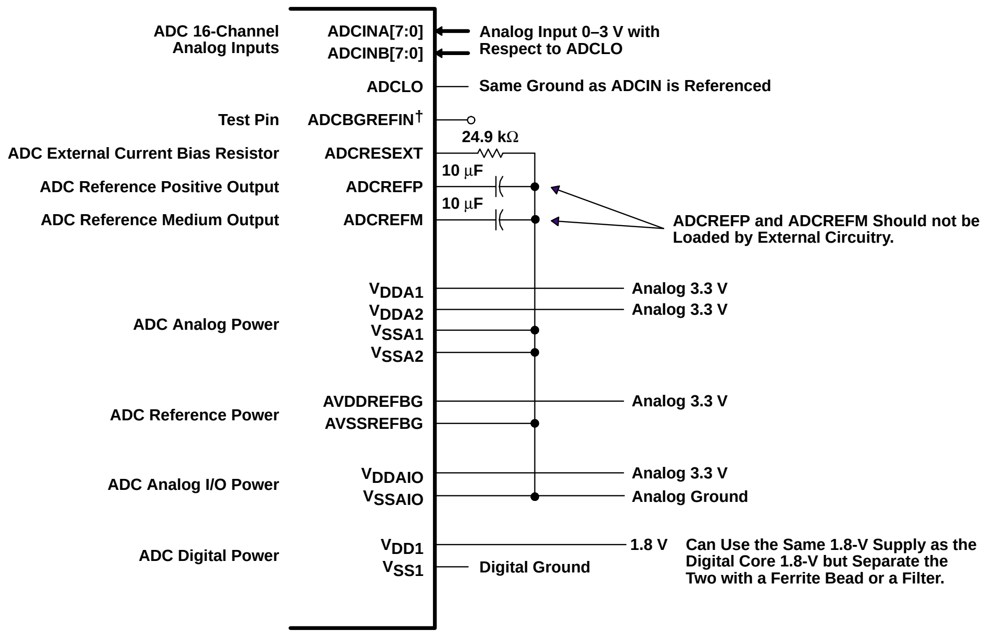
To obtain the specified accuracy of the ADC, proper board layout is very critical. To the best extent possible, traces leading to the ADCIN pins should not run in close proximity to the digital signal paths. This is to minimize switching noise on the digital lines from getting coupled to the ADC inputs. Furthermore, proper isolation techniques must be used to isolate the ADC module power pins (V_{DDA1}/V_{DDA2}, $AV_{DDREFBG}$) from the digital supply. Figure 4–5 shows the ADC pin connections for the F2810 and F2812 devices.

Notes:

1. The ADC registers are accessed at the SYSCLKOUT rate. The internal timing of the ADC module is controlled by the high-speed peripheral clock (HSPCLK).
2. The behavior of the ADC module based on the state of the ADCENCLK and HALT signals is as follows:

   ADCENCLK: On reset, this signal will be low. While reset is active-low ($\overline{\text{XRS}}$) the clock to the register will still function. This is necessary to make sure all registers and modes go into their default reset state. The analog module will however be in a low-power inactive state. As soon as reset goes high, then the clock to the registers will be disabled. When the user sets the ADCENCLK signal high, then the clocks to the registers will be enabled and the analog module will be enabled. There will be a certain time delay (ms range) before the ADC is stable and can be used.

HALT: This signal only affects the analog module. It does not affect the registers. If low, the ADC module is powered. If high, the ADC module goes into low-power mode. The HALT mode will stop the clock to the CPU, which will stop the HSPCLK. Therefore the ADC register logic will be turned off indirectly.



† Provide access to this pin in PCB layouts using TMX samples. Intended for test purposes only.

NOTES: A. External decoupling capacitors are recommended on all power pins.

B. Analog inputs must be driven from an operational amplifier that does not degrade the ADC performance.

Figure 4–5. ADC Pin Connections

ADVANCE INFORMATION

The ADC operation is configured, controlled, and monitored by the registers listed in Table 4–4.

Table 4–4. ADC Registers†

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
ADCTRL1	0x00 7100	1	ADC Control Register 1
ADCTRL2	0x00 7101	1	ADC Control Register 2
ADCMAXCONV	0x00 7102	1	ADC Maximum Conversion Channels Register
ADCCHSELSEQ1	0x00 7103	1	ADC Channel Select Sequencing Control Register 1
ADCCHSELSEQ2	0x00 7104	1	ADC Channel Select Sequencing Control Register 2
ADCCHSELSEQ3	0x00 7105	1	ADC Channel Select Sequencing Control Register 3
ADCCHSELSEQ4	0x00 7106	1	ADC Channel Select Sequencing Control Register 4
ADCASEQSR	0x00 7107	1	ADC Auto-Sequence Status Register
ADCRESULT0	0x00 7108	1	ADC Conversion Result Buffer Register 0
ADCRESULT1	0x00 7109	1	ADC Conversion Result Buffer Register 1
ADCRESULT2	0x00 710A	1	ADC Conversion Result Buffer Register 2
ADCRESULT3	0x00 710B	1	ADC Conversion Result Buffer Register 3
ADCRESULT4	0x00 710C	1	ADC Conversion Result Buffer Register 4
ADCRESULT5	0x00 710D	1	ADC Conversion Result Buffer Register 5
ADCRESULT6	0x00 710E	1	ADC Conversion Result Buffer Register 6
ADCRESULT7	0x00 710F	1	ADC Conversion Result Buffer Register 7
ADCRESULT8	0x00 7110	1	ADC Conversion Result Buffer Register 8
ADCRESULT9	0x00 7111	1	ADC Conversion Result Buffer Register 9
ADCRESULT10	0x00 7112	1	ADC Conversion Result Buffer Register 10
ADCRESULT11	0x00 7113	1	ADC Conversion Result Buffer Register 11
ADCRESULT12	0x00 7114	1	ADC Conversion Result Buffer Register 12
ADCRESULT13	0x00 7115	1	ADC Conversion Result Buffer Register 13
ADCRESULT14	0x00 7116	1	ADC Conversion Result Buffer Register 14
ADCRESULT15	0x00 7117	1	ADC Conversion Result Buffer Register 15
ADCTRL3	0x00 7118	1	ADC Control Register 3
ADCST	0x00 7119	1	ADC Status Register
reserved	0x00 711C 0x00 711F	4	

† The above registers are mapped to peripheral bus 16 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

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4.4 Enhanced Controller Area Network (eCAN) Module

The CAN module has the following features:

- Fully compliant with CAN protocol, version 2.0B
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Has a programmable receive mask
  - Supports data and remote frame
  - Composed of 0 to 8 bytes of data
  - Uses a 32-bit time stamp on receive and transmit message
  - Protects against reception of new message
  - Holds the dynamically programmable priority of transmit message
  - Employs a programmable interrupt scheme with two interrupt levels
  - Employs a programmable alarm on transmission or reception time-out
- Low-power mode
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Self-test mode
  - Operates in a loopback mode receiving its own message. A “dummy” acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

NOTE: For a SYSCLKOUT of 150 MHz, the smallest bit rate possible is 23.4 kbps.

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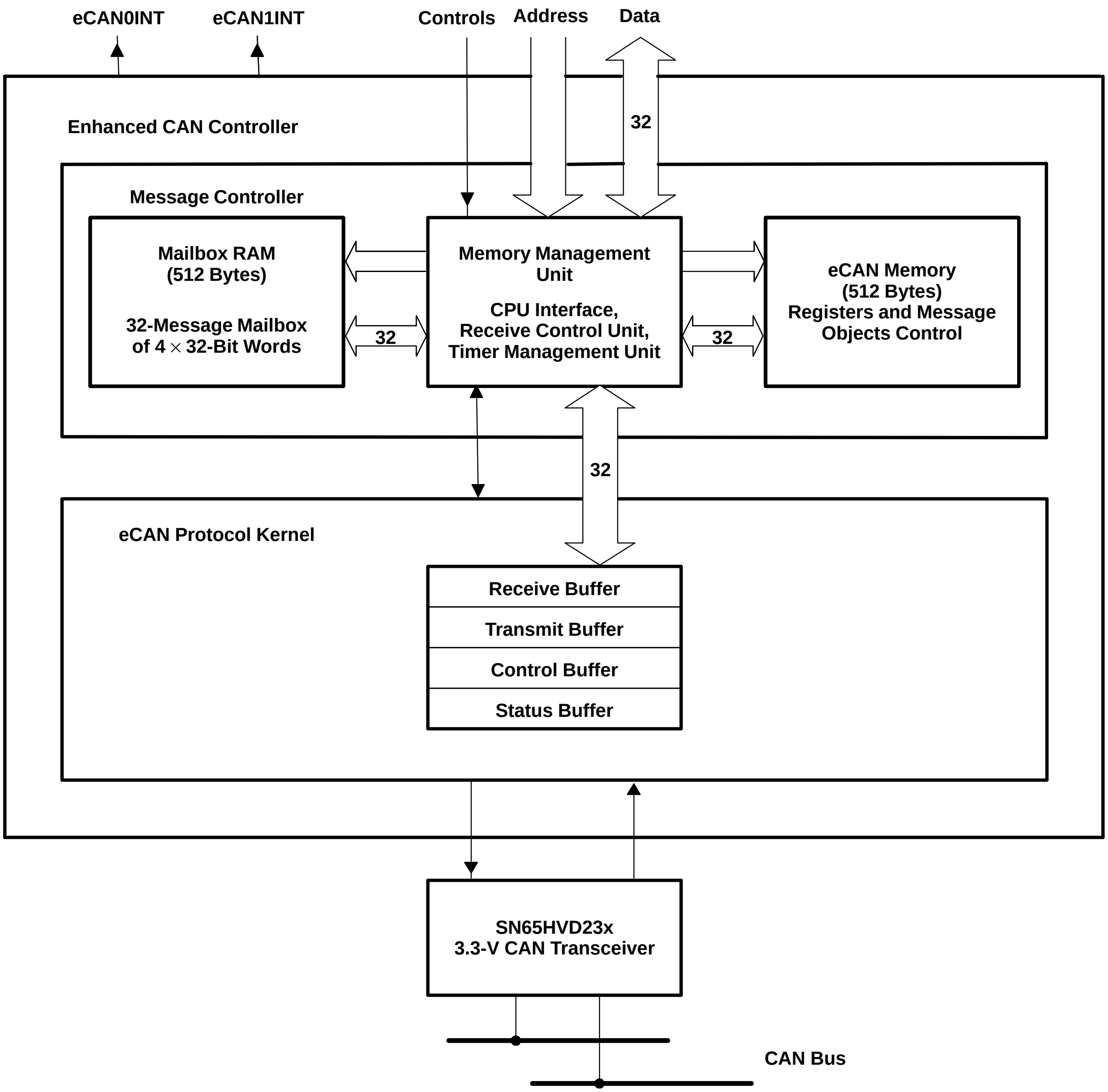

Figure 4–6. eCAN Block Diagram and Interface Circuit

Table 4–5. 3.3-V eCAN Transceivers for the TMS320F28x DSPs

PART NUMBER	LOW-POWER MODE	INTEGRATED SLOPE CONTROL	V_{ref} PIN	T_A	MARKED AS†
SN65HVD230	370 µA standby mode	Yes	Yes	–40°C to 85°C	VP230
SN65HVD231	40 nA sleep mode	Yes	Yes		VP231
SN65HVD232	No standby or sleep mode	No	No		VP232

† This is the nomenclature printed on the device, since the footprint is too small to accommodate the entire part number.

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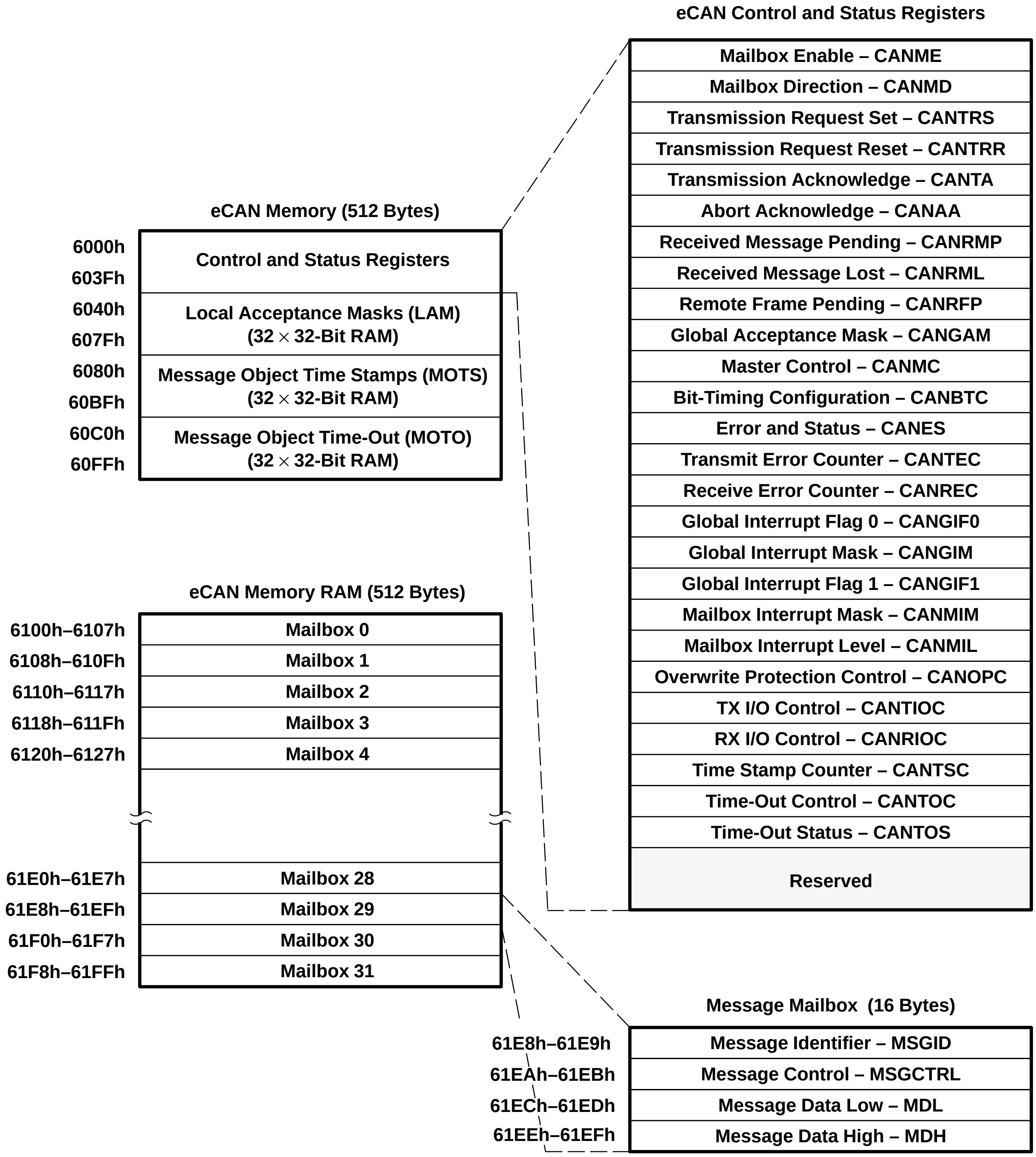

Figure 4–7. eCAN Memory Map

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The CAN registers listed in Table 4–6 are used by the CPU to configure and control the CAN controller and the message objects. eCAN control registers only support 32-bit read/write operations. Mailbox RAM can be accessed as 16 bits or 32 bits. 32-bit accesses are aligned to an even boundary.

Table 4–6. CAN Registers Map†

REGISTER NAME	ADDRESS	SIZE (x32)	DESCRIPTION
CANME	0x00 6000	1	Mailbox enable
CANMD	0x00 6002	1	Mailbox direction
CANTRS	0x00 6004	1	Transmit request set
CANTRR	0x00 6006	1	Transmit request reset
CANTA	0x00 6008	1	Transmission acknowledge
CANAA	0x00 600A	1	Abort acknowledge
CANRMP	0x00 600C	1	Receive message pending
CANRML	0x00 600E	1	Receive message lost
CANRFP	0x00 6010	1	Remote frame pending
CANGAM	0x00 6012	1	Global acceptance mask
CANMC	0x00 6014	1	Master control
CANBTC	0x00 6016	1	Bit-timing configuration
CANES	0x00 6018	1	Error and status
CANTEC	0x00 601A	1	Transmit error counter
CANREC	0x00 601C	1	Receive error counter
CANGIF0	0x00 601E	1	Global interrupt flag 0
CANGIM	0x00 6020	1	Global interrupt mask
CANGIF1	0x00 6022	1	Global interrupt flag 1
CANMIM	0x00 6024	1	Mailbox interrupt mask
CANMIL	0x00 6026	1	Mailbox interrupt level
CANOPC	0x00 6028	1	Overwrite protection control
CANTIOC	0x00 602A	1	TX I/O control
CANRIOC	0x00 602C	1	RX I/O control
CANTSC	0x00 602E	1	Time stamp counter (Reserved in SCC mode)
CANTOC	0x00 6030	1	Time-out control (Reserved in SCC mode)
CANTOS	0x00 6032	1	Time-out status (Reserved in SCC mode)

† These registers are mapped to Peripheral Frame 1.

ADVANCE INFORMATION

4.5 Multichannel Buffered Serial Port (McBSP) Module

The McBSP module has the following features:

- Compatible to McBSP in TMS320C54x™ /TMS320C55x™ DSP devices, except the DMA features
- Full-duplex communication
- Double-buffered data registers which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- A wide selection of data sizes including 8-, 12-, 16-, 20-, 24-, or 32-bits
- 8-bit data transfers with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- HIghly programmable internal clock and frame generation
- Support A-bis mode
- Direct interface to industry-standard CODECs, Analog Interface Chips (AICs), and other serially connected A/D and D/A devices
- Works with SPI-compatible devices
- Two 16 x 16-level FIFO for Transmit channel
- Two 16 x 16-level FIFO for Receive channel

The following application interfaces can be supported on the McBSP:

- T1/E1 framers
- MVIP switching-compatible and ST-BUS-compliant devices including:
  - MVIP framers
  - H.100 framers
  - SCSA framers
  - IOM-2 compliant devices
  - AC97-compliant devices (the necessary multiphase frame synchronization capability is provided.)
  - IIS-compliant devices
- McBSP clock rate = $\text{CLKG} = \frac{\text{CLKSRG}}{(1 + \text{CLKGDIV})}$, where CLKSRG source could be LSPCLK, CLKX, or CLKR.†

TMS320C54x and TMS320C55x are trademarks of Texas Instruments.

† Serial port performance is limited by I/O buffer switching speed. Internal prescalars have to be adjusted such that the peripheral speed is less than the I/O buffer speed limit—20 MHz maximum.

Figure 4–8 shows the block diagram of the McBSP module with FIFO, interfaced to the F2810 and F2812 version of Peripheral Frame 2.

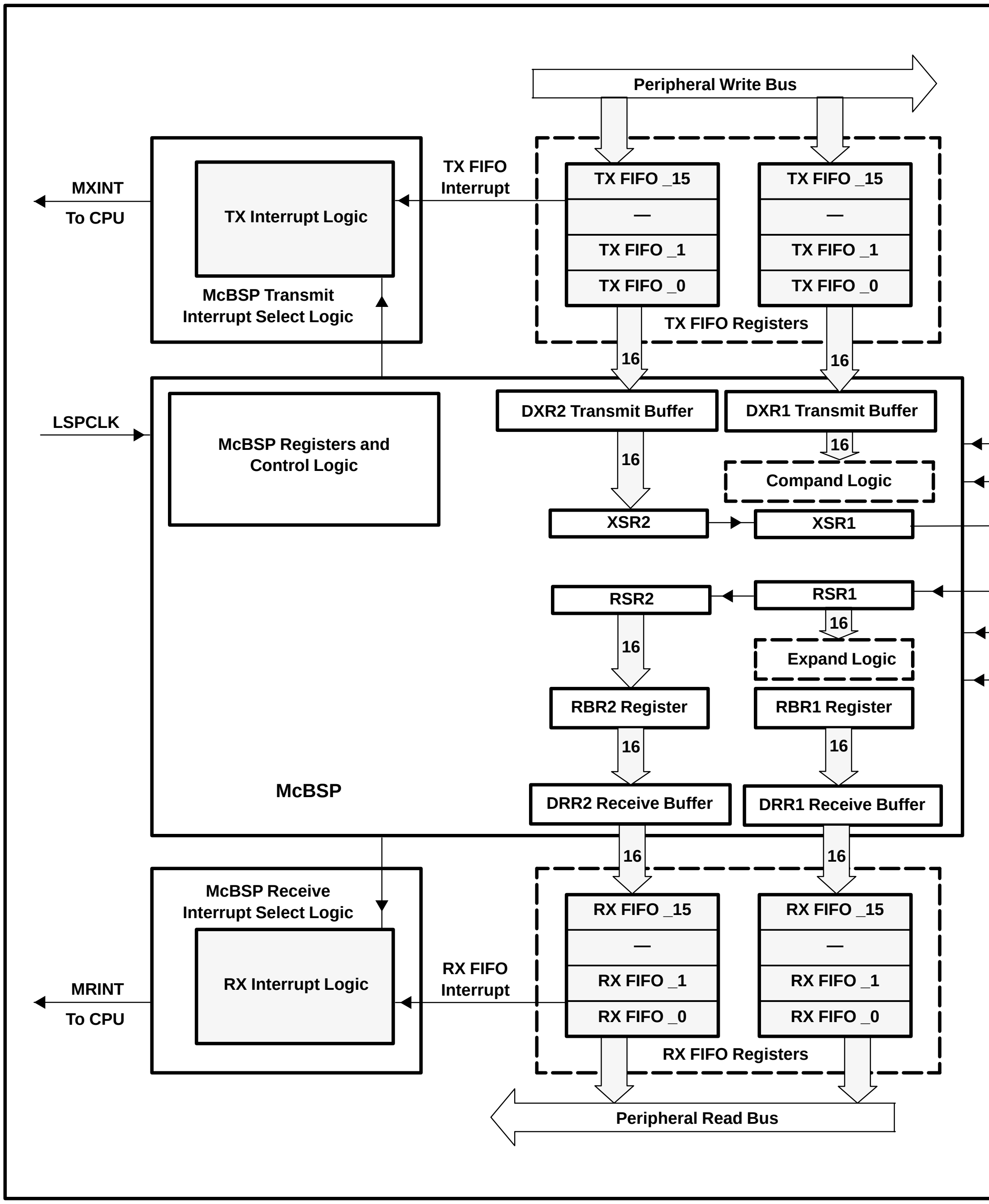

Figure 4–8. McBSP Module With FIFO

Table 4–7 provides a summary of the McBSP registers.

Table 4–7. McBSP Register Summary

NAME	ADDRESS 0x00 78xxh	TYPE (R/W)	RESET VALUE (HEX)	DESCRIPTION
DATA REGISTERS, RECEIVE, TRANSMIT†				
–	–	–	0x0000	McBSP Receive Buffer Register
–	–	–	0x0000	McBSP Receive Shift Register
–	–	–	0x0000	McBSP Transmit Shift Register
DRR2	00	R	0x0000	McBSP Data Receive Register 2 – Read First if the word size is greater than 16 bits, else ignore DRR2
DRR1	01	R	0x0000	McBSP Data Receive Register 1 – Read Second if the word size is greater than 16 bits, else read DRR1 only
DXR2	02	W	0x0000	McBSP Data Transmit Register 2 – Write First if the word size is greater than 16 bits, else ignore DXR2
DXR1	03	W	0x0000	McBSP Data Transmit Register 1 – Write Second if the word size is greater than 16 bits, else write to DXR1 only
McBSP CONTROL REGISTERS				
SPCR2	04	R/W	0x0000	McBSP Serial Port Control Register 2
SPCR1	05	R/W	0x0000	McBSP Serial Port Control Register 1
RCR2	06	R/W	0x0000	McBSP Receive Control Register 2
RCR1	07	R/W	0x0000	McBSP Receive Control Register 1
XCR2	08	R/W	0x0000	McBSP Transmit Control Register 2
XCR1	09	R/W	0x0000	McBSP Transmit Control Register 1
SRGR2	0A	R/W	0x0000	McBSP Sample Rate Generator Register 2
SRGR1	0B	R/W	0x0000	McBSP Sample Rate Generator Register 1
MULTICHANNEL CONTROL REGISTERS				
MCR2	0C	R/W	0x0000	McBSP Multichannel Register 2
MCR1	0D	R/W	0x0000	McBSP Multichannel Register 1
RCERA	0E	R/W	0x0000	McBSP Receive Channel Enable Register Partition A
RCERB	0F	R/W	0x0000	McBSP Receive Channel Enable Register Partition B
XCERA	10	R/W	0x0000	McBSP Transmit Channel Enable Register Partition A
XCERB	11	R/W	0x0000	McBSP Transmit Channel Enable Register Partition B
PCR1	12	R/W	0x0000	McBSP Pin Control Register
RCERC	13	R/W	0x0000	McBSP Receive Channel Enable Register Partition C
RCERD	14	R/W	0x0000	McBSP Receive Channel Enable Register Partition D
XCERC	15	R/W	0x0000	McBSP Transmit Channel Enable Register Partition C
XCERD	16	R/W	0x0000	McBSP Transmit Channel Enable Register Partition D

† DRR2/DRR1 and DXR2/DXR1 share the same addresses of receive and transmit FIFO registers in FIFO mode.
‡ FIFO pointers advancing is based on order of access to DRR2/DRR1 and DXR2/DXR1 registers.

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Table 4–7. McBSP Register Summary (Continued)

NAME	ADDRESS 0x00 78xxh	TYPE (R/W)	RESET VALUE (HEX)	DESCRIPTION
MULTICHANNEL CONTROL REGISTERS (CONTINUED)				
RCERE	17	R/W	0x0000	McBSP Receive Channel Enable Register Partition E
RCERF	18	R/W	0x0000	McBSP Receive Channel Enable Register Partition F
XCERE	19	R/W	0x0000	McBSP Transmit Channel Enable Register Partition E
XCERF	1A	R/W	0x0000	McBSP Transmit Channel Enable Register Partition F
RCERG	1B	R/W	0x0000	McBSP Receive Channel Enable Register Partition G
RCERH	1C	R/W	0x0000	McBSP Receive Channel Enable Register Partition H
XCERG	1D	R/W	0x0000	McBSP Transmit Channel Enable Register Partition G
XCERH	1E	R/W	0x0000	McBSP Transmit Channel Enable Register Partition H
FIFO MODE REGISTERS (applicable only in FIFO mode)				
FIFO Data Registers‡				
DRR2	00	R	0x0000	McBSP Data Receive Register 2 – Top of receive FIFO – Read First FIFO pointers will not advance
DRR1	01	R	0x0000	McBSP Data Receive Register 1 – Top of receive FIFO – Read Second for FIFO pointers to advance
DXR2	02	W	0x0000	McBSP Data Transmit Register 2 – Top of transmit FIFO – Write First FIFO pointers will not advance
DXR1	03	W	0x0000	McBSP Data Transmit Register 1 – Top of transmit FIFO – Write Second for FIFO pointers to advance
FIFO Control Registers				
MFFTX	20	R/W	0xA000	McBSP Transmit FIFO Register
MFFRX	21	R/W	0x201F	McBSP Receive FIFO Register
MFFCT	22	R/W	0x0000	McBSP FIFO Control Register
MFFINT	23	R/W	0x0000	McBSP FIFO Interrupt Register
MFFST	24	R/W	0x0000	McBSP FIFO Status Register

† DRR2/DRR1 and DXR2/DXR1 share the same addresses of receive and transmit FIFO registers in FIFO mode.
‡ FIFO pointers advancing is based on order of access to DRR2/DRR1 and DXR2/DXR1 registers.

4.6 Serial Communications Interface (SCI) Module

The F2810 and F2812 devices include two serial communications interface (SCI) modules. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

  NOTE: Both pins can be used as GPIO if not used for SCI.
- Baud rate programmable to 64K different rates†
  - Baud rate $= \dfrac{\text{LSPCLK}}{(\text{BRR} + 1) * 8}$, when BRR $\neq 0$

    $= \dfrac{\text{LSPCLK}}{16}$, when BRR = 0
- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)

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† Serial port performance is limited by I/O buffer switching speed. Internal prescalars have to be adjusted such that the peripheral speed is less than the I/O buffer speed limit—20 MHz maximum.

- NRZ (non-return-to-zero) format
- Ten SCI module control registers located in the control register frame beginning at address 7050h

  NOTE: All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- Auto baud-detect hardware logic
- 16-level transmit/receive FIFO

The SCI port operation is configured and controlled by the registers listed in Table 4–8 and Table 4–9.

Table 4–8. SCI-A Registers†

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRA	0x00 7050	1	SCI-A Communications Control Register
SCICTL1A	0x00 7051	1	SCI-A Control Register 1
SCIHBAUDA	0x00 7052	1	SCI-A Baud Register, High Bits
SCILBAUDA	0x00 7053	1	SCI-A Baud Register, Low Bits
SCICTL2A	0x00 7054	1	SCI-A Control Register 2
SCIRXSTA	0x00 7055	1	SCI-A Receive Status Register
SCIRXEMUA	0x00 7056	1	SCI-A Receive Emulation Data Buffer Register
SCIRXBUFA	0x00 7057	1	SCI-A Receive Data Buffer Register
SCITXBUFA	0x00 7059	1	SCI-A Transmit Data Buffer Register
SCIFFTXA	0x00 705A	1	SCI-A FIFO Transmit Register
SCIFFRXA	0x00 705B	1	SCI-A FIFO Receive Register
SCIFFCTA	0x00 705C	1	SCI-A FIFO Control Register
SCIPRIA	0x00 705F	1	SCI-A Priority Control Register

† Shaded registers are new registers for the FIFO mode.

Table 4–9. SCI-B Registers†

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRB	0x00 7750	1	SCI-B Communications Control Register
SCICTL1B	0x00 7751	1	SCI-B Control Register 1
SCIHBAUDB	0x00 7752	1	SCI-B Baud Register, High Bits
SCILBAUDB	0x00 7753	1	SCI-B Baud Register, Low Bits
SCICTL2B	0x00 7754	1	SCI-B Control Register 2
SCIRXSTB	0x00 7755	1	SCI-B Receive Status Register
SCIRXEMUB	0x00 7756	1	SCI-B Receive Emulation Data Buffer Register
SCIRXBUFB	0x00 7757	1	SCI-B Receive Data Buffer Register
SCITXBUFB	0x00 7759	1	SCI-B Transmit Data Buffer Register
SCIFFTXB	0x00 775A	1	SCI-B FIFO Transmit Register
SCIFFRXB	0x00 775B	1	SCI-B FIFO Receive Register
SCIFFCTB	0x00 775C	1	SCI-B FIFO Control Register
SCIPRIB	0x00 775F	1	SCI-B Priority Control Register

† Shaded registers are new registers for the FIFO mode.

NOTE: The above registers are mapped to peripheral bus 16 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Figure 4–9 shows the SCI module block diagram.

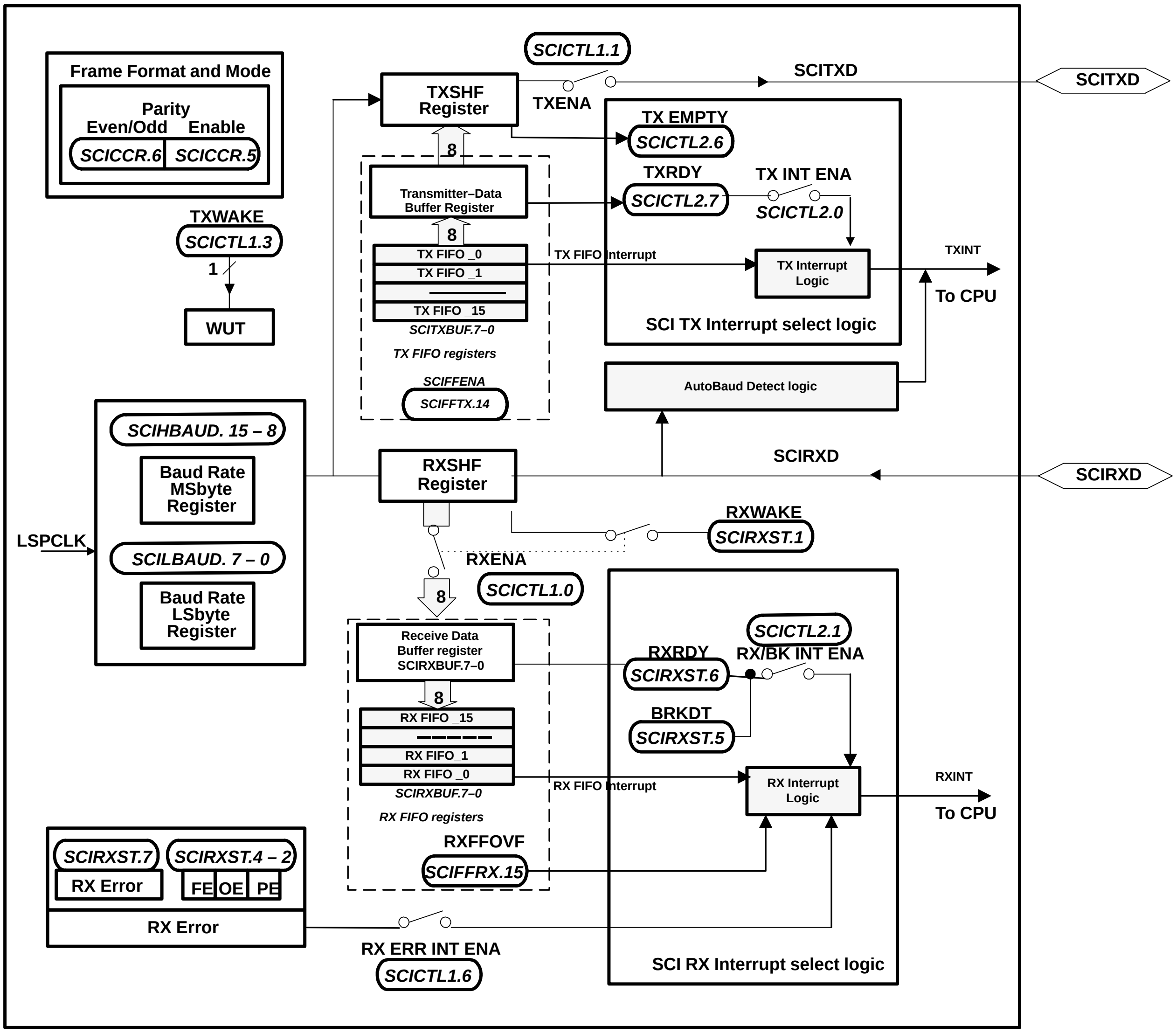

Figure 4–9. Serial Communications Interface (SCI) Module Block Diagram

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4.7 Serial Peripheral Interface (SPI) Module

The F2810 and F2812 devices include the four-pin serial peripheral interface (SPI) module. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

  NOTE: All four pins can be used as GPIO, if the SPI module is not used.
- Two operational modes: master and slave
- Baud rate: 125 different programmable rates†
  - $$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)}, \quad \text{when BRR} \neq 0$$
    $$= \frac{\text{LSPCLK}}{4}, \quad \text{when BRR} = 0, 1, 2, 3$$
- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: Located in control register frame beginning at address 7040h.

  NOTE: All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced feature:

- 16-level transmit/receive FIFO
- Delayed transmit control

† Serial port performance is limited by I/O buffer switching speed. Internal prescalars have to be adjusted such that the peripheral speed is less than the I/O buffer speed limit—20 MHz maximum.

The SPI port operation is configured and controlled by the registers listed in Table 4–10.

Table 4–10. SPI Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SPICCR	0x00 7040	1	SPI Configuration Control Register
SPICTL	0x00 7041	1	SPI Operation Control Register
SPISTS	0x00 7042	1	SPI Status Register
SPIBRR	0x00 7044	1	SPI Baud Rate Register
SPIRXEMU	0x00 7046	1	SPI Receive Emulation Buffer Register
SPIRXBUF	0x00 7047	1	SPI Serial Input Buffer Register
SPITXBUF	0x00 7048	1	SPI Serial Output Buffer Register
SPIDAT	0x00 7049	1	SPI Serial Data Register
SPIFFTX	0x00 704A	1	SPI FIFO Transmit Register
SPIFFRX	0x00 704B	1	SPI FIFO Receive Register
SPIFFCT	0x00 704C	1	SPI FIFO Control Register
SPIPRI	0x00 704F	1	SPI Priority Control Register

NOTE: The above registers are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

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Figure 4–10 is a block diagram of the SPI in slave mode.

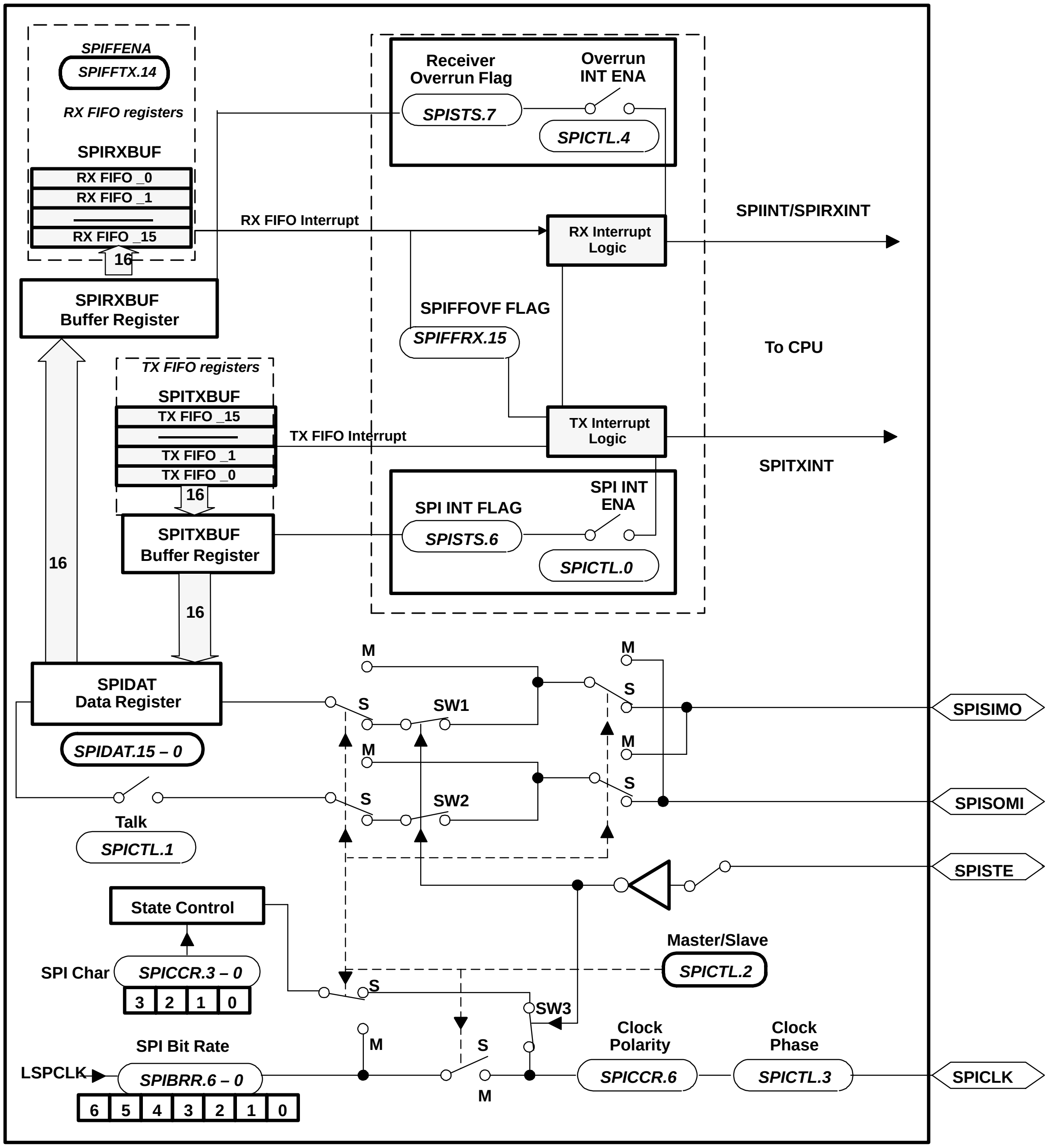

Figure 4–10. Serial Peripheral Interface Module Block Diagram

4.8 GPIO Mux

The GPIO Mux registers, are used to select the operation of shared pins on the F2810 and F2812 devices. The pins can be individually selected to operate as “Digital I/O” or connected to “Peripheral I/O” signals (via the GPxMUX registers). If selected for “Digital I/O” mode, registers are provided to configure the pin direction (via the GPxDIR registers) and to qualify the input signal to remove unwanted noise (via the GPxQUAL) registers). Table 4–11 lists the GPIO Mux Registers.

Table 4–11. GPIO Mux Registers†‡§

NAME	ADDRESS	SIZE (x16)	REGISTER DESCRIPTION
GPAMUX	0x00 70C0	1	GPIO A Mux Control Register
GPADIR	0x00 70C1	1	GPIO A Direction Control Register
GPAQUAL	0x00 70C2	1	GPIO A Input Qualification Control Register
reserved	0x00 70C3	1	
GPBMUX	0x00 70C4	1	GPIO B Mux Control Register
GPBDIR	0x00 70C5	1	GPIO B Direction Control Register
GPBQUAL	0x00 70C6	1	GPIO B Input Qualification Control Register
reserved	0x00 70C7	1	
reserved	0x00 70C8	1	
reserved	0x00 70C9	1	
reserved	0x00 70CA	1	
reserved	0x00 70CB	1	
GPDMUX	0x00 70CC	1	GPIO D Mux Control Register
GPDDIR	0x00 70CD	1	GPIO D Direction Control Register
GPDQUAL	0x00 70CE	1	GPIO D Input Qualification Control Register
reserved	0x00 70CF	1	
GPEMUX	0x00 70D0	1	GPIO E Mux Control Register
GPEDIR	0x00 70D1	1	GPIO E Direction Control Register
GPEQUAL	0x00 70D2	1	GPIO E Input Qualification Control Register
reserved	0x00 70D3	1	
GPFMUX	0x00 70D4	1	GPIO F Mux Control Register
GPFDIR	0x00 70D5	1	GPIO F Direction Control Register
reserved	0x00 70D6	1	
reserved	0x00 70D7	1	
GPGMUX	0x00 70D8	1	GPIO G Mux Control Register
GPGDIR	0x00 70D9	1	GPIO G Direction Control Register
reserved	0x00 70DA	1	
reserved	0x00 70DB	1	
reserved	0x00 70DC 0x00 70DF	4	

† Reserved locations will return undefined values and writes will be ignored.
‡ Not all inputs will support input signal qualification.
§ These registers are EALLOW protected. This prevents spurious writes from overwriting the contents and corrupting the system.

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If configured for ”Digital I/O” mode, additional registers are provided for setting individual I/O signals (via the GPxSET registers), for clearing individual I/O signals (via the GPxCLEAR registers), for toggling individual I/O signals (via the GPxTOGGLE registers), or for reading/writing to the individual I/O signals (via the GPxDAT registers). Table 4–12 lists the GPIO Data Registers. For more information, see the *TMS320F28x System Control and Interrupts Peripheral Reference Guide* (literature number SPRU078).

Table 4–12. GPIO Data Registers†‡

NAME	ADDRESS	SIZE (x16)	REGISTER DESCRIPTION
GPADAT	0x00 70E0	1	GPIO A Data Register
GPASET	0x00 70E1	1	GPIO A Set Register
GPACLEAR	0x00 70E2	1	GPIO A Clear Register
GPATOGGLE	0x00 70E3	1	GPIO A Toggle Register
GPBDAT	0x00 70E4	1	GPIO B Data Register
GPBSET	0x00 70E5	1	GPIO B Set Register
GPBCLEAR	0x00 70E6	1	GPIO B Clear Register
GPBTOGGLE	0x00 70E7	1	GPIO B Toggle Register
reserved	0x00 70E8	1	
reserved	0x00 70E9	1	
reserved	0x00 70EA	1	
reserved	0x00 70EB	1	
GPDDAT	0x00 70EC	1	GPIO D Data Register
GPDSET	0x00 70ED	1	GPIO D Set Register
GPDCLEAR	0x00 70EE	1	GPIO D Clear Register
GPDTOGGLE	0x00 70EF	1	GPIO D Toggle Register
GPEDAT	0x00 70F0	1	GPIO E Data Register
GPESET	0x00 70F1	1	GPIO E Set Register
GPECLEAR	0x00 70F2	1	GPIO E Clear Register
GPETOGGLE	0x00 70F3	1	GPIO E Toggle Register
GPFDAT	0x00 70F4	1	GPIO F Data Register
GPFSET	0x00 70F5	1	GPIO F Set Register
GPFCLEAR	0x00 70F6	1	GPIO F Clear Register
GPFTOGGLE	0x00 70F7	1	GPIO F Toggle Register
GPGDAT	0x00 70F8	1	GPIO G Data Register
GPGSET	0x00 70F9	1	GPIO G Set Register
GPGCLEAR	0x00 70FA	1	GPIO G Clear Register
GPGTOGGLE	0x00 70FB	1	GPIO G Toggle Register
reserved	0x00 70FC 0x00 70FF	4	

† Reserved locations will return undefined values and writes will be ignored.
‡ These registers are NOT EALLOW protected. The above registers will typically be accessed regularly by the user.

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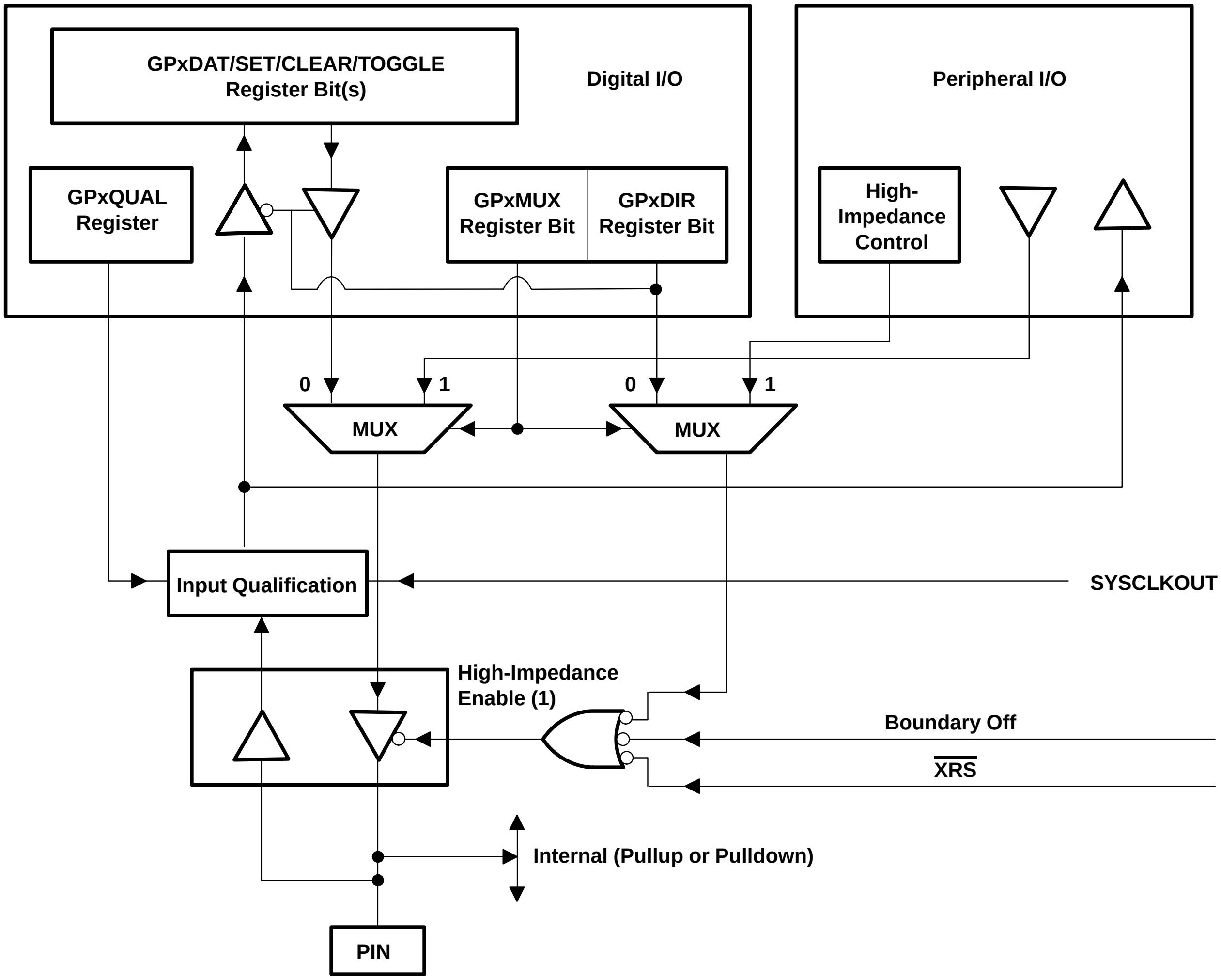
Figure 4–11 shows how the various register bits select the various modes of operation.



NOTES: A. In the GPIO mode, when the GPIO pin is configured for output operation, reading the GPxDAT data register only gives the value written, not the value at the pin. In the peripheral mode, the state of the pin can be read through the GPxDAT register, provided the corresponding direction bit is zero (input mode).

B. Some selected input signals are qualified by the SYSCLKOUT. The GPxQUAL register specifies the qualification sampling period. The sampling window is 6 samples wide and the output is only changed when all samples are the same (all 0's or all 1's). This feature removes unwanted spikes from the input signal.

Figure 4–11. Modes of Operation

CAUTION:

The input function of the GPIO pin and the input path to the peripheral are always enabled. It is the output function of the GPIO pin that is multiplexed with the output path of the primary (peripheral) function. Since the output buffer of a pin connects back to the input buffer, any GPIO signal present at the pin will be propagated to the peripheral module as well. Therefore, when a pin is configured for GPIO operation, the corresponding peripheral functionality (and interrupt-generating capability) must be disabled. Otherwise, interrupts may be inadvertently triggered. This is especially critical when the $\overline{\text{PDPINTA}}$ and $\overline{\text{PDPINTB}}$ pins are used as GPIO pins, since a value of zero for GPDDAT.0 or GPDDAT.5 ($\overline{\text{PDPINTx}}$) will put PWM pins in a high-impedance state. The $\overline{\text{CxTRIP}}$ and $\overline{\text{TxCTRIP}}$ pins will also put the corresponding PWM pins in high impedance, if they are driven low (as GPIO pins) *and* bit EXTCONx.0 = 1.

5 Development Support

Texas Instruments (TI) offers an extensive line of development tools for the C28x™ generation of DSPs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of F2810- and F2812-based applications:

Software Development Tools:
Assembler/linker
Simulator
Optimizing ANSI C compiler
Application algorithms
C/C++/Assembly debugger and code profiler

Hardware Development Tools:
SPI515
XDS510PP, XDS510PP Plus, XDS510 USB

Development tools for the 28x are as follows:

- Code Composer Studio™ Integrated Development Environment (IDE) Version 2.x
  - Code Composer Studio Version 2.0 Debugger
  - Code Generation Tools
  - Assembler/Linker
  - C/C++ Compiler
  - Cycle Accurate Simulator
- JTAG-Based Emulator
- Sample Applications Code
- Universal 5-V DC Power Supply
- Documentation and Cables

5.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

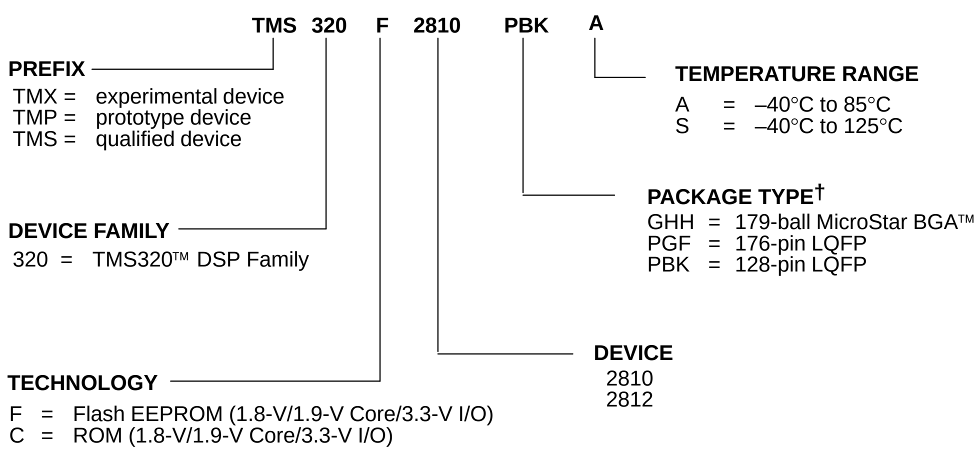
TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped with appropriate disclaimers describing their limitations and intended uses. Experimental devices (TMX) may not be representative of a final product and Texas Instruments reserves the right to change or discontinue these products without notice.

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PBK) and temperature range (for example, A). Figure 5–1 provides a legend for reading the complete device name for any TMS320x28x family member.



† BGA = Ball Grid Array
LQFP = Low-Profile Quad Flatpack

Figure 5–1. TMS320x28x Device Nomenclature

TMS320 is a trademark of Texas Instruments.

6 Documentation Support

Extensive documentation supports all of the TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets and data manuals, with design specifications; and hardware and software applications. Useful reference documentation includes:

- *3.3V DSP for Digital Motor Control* application report (literature number SPRA550)
- *TMS320F28x DSP Serial Communication Interface (SCI) Reference Guide* (literature number SPRU051)
- *TMS320F28x DSP Serial Peripheral Interface (SPI) Reference Guide* (literature number SPRU059)
- *TMS320F28x Analog-to-Digital Converter (ADC) Peripheral Reference Guide* (literature number SPRU060)
- *TMS320F28x DSP Multichannel Buffered Serial Port (McBSP) Reference Guide* (literature number SPRU061)
- *TMS320F28x DSP Event Manager (EV) Reference Guide* (literature number SPRU065)
- *TMS320F28x DSP External Interface (XINTF) Reference Guide* (literature number SPRU067)
- *TMS320F28x DSP Enhanced Controller Area Network (eCAN) Reference Guide* (literature number SPRU074)
- *TMS320F28x System Control and Interrupts Peripheral Reference Guide* (literature number SPRU078)
- *TMS320F28x DSP Boot ROM Reference Guide* (literature number SPRU095)
- *TMS320C28x DSP CPU and Instruction Set Reference Guide* (literature number SPRU430)
- *TMS320F28x DSP Peripherals Reference Guide* (literature number SPRU566)

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320™ DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320™ DSP customers on product information.

Updated information on the TMS320™ DSP controllers can be found on the worldwide web at: **http://www.ti.com**.

To send comments regarding this TMS320F2810/TMS320F2812 data manual (literature number SPRS174), use the *comments@books.sc.ti.com* email address, which is a repository for feedback. For questions and support, contact the Product Information Center listed at the **http://www.ti.com/sc/docs/pic/home.htm** site.

7 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320F2810 and TMS320F2812 DSPs.

7.1 Absolute Maximum Ratings

Unless otherwise noted, the list of absolute maximum ratings are specified over operating temperature ranges. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 7.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to V_{SS}.

Supply voltage range, V_{DDIO}, V_{DDA1}, V_{DDA2}, V_{DDAIO}, and $AV_{DDREFBG}$ . . . . – 0.3 V to 4.6 V
Supply voltage range, V_{DD}, V_{DD1} . . . . – 0.5 V to 2.5 V
V_{DD3VFL} range . . . . – 0.3 V to 4.6 V
Input voltage range, V_{IN} . . . . – 0.3 V to 4.6 V
Output voltage range, V_O . . . . – 0.3 V to 4.6 V
Output voltage range,V_O . . . . – 0.3 V to 4.6 V
Input clamp current, I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO}) . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDIO}) . . . . ± 20 mA
Operating case temperature ranges, T_C: A version (GHH, PGF, PBK)† . . . . – 40°C to 85°C
S version (GHH, PGF, PBK)† . . . . – 40°C to 125°C
Storage temperature range, T_{stg}† . . . . – 65°C to 150°C

† Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. For additional information, please contact TI.

7.2 Recommended Operating Conditions‡

				MIN	NOM	MAX	UNIT
V_{DDIO}	Device supply voltage, I/O			3.14	3.3	3.47	V
V_{DD}, V_{DD1}	Device supply voltage, CPU		1.8 V (135 MHz)	1.71	1.8	1.89	V
			1.9 V (150 MHz)	1.81	1.9	2	
V_{SS}	Supply ground				0		V
V_{DDA1}, V_{DDA2}, $AV_{DDREFBG}$, V_{DDAIO}	ADC supply voltage			3.14	3.3	3.47	V
V_{DD3VFL}	Flash programming supply voltage			3.14	3.3	3.47	V
$f_{SYSCLKOUT}$	Device clock frequency (system clock)		V_{DD} = 1.9 V ± 5%	2		150	MHz
			V_{DD} = 1.8 V ± 5%	2		135	
V_{IH}	High-level input voltage		All inputs except XCLKIN	2			V
			XCLKIN (@ 50 µA max)	0.7V_{DD}			
V_{IL}	Low-level input voltage		All inputs except XCLKIN			0.8	V
			XCLKIN (@ 50 µA max)			0.3V_{DD}	
I_{OH}	High-level output source current, V_{OH} = 2.4 V		All I/Os except Group 2			– 4	mA
			Group 2§			– 8	
I_{OL}	Low-level output sink current, V_{OL} = V_{OL} MAX		All I/Os except Group 2			4	mA
			Group 2§			8	
T_C	Case temperature	A version	TMP	– 40		85	°C
		S version	Available at TMS only	– 40		125	

‡ Refer to Section 7.5 for power sequencing of V_{DDIO}, V_{DDAIO}, V_{DD}, V_{DDA1}/V_{DDA2}/$AV_{DDREFBG}$, and V_{DD3VFL}.
§ Group 2 pins are as follows: XINTF pins, $\overline{\text{PDPINTA}}$, TDO, XCLKOUT, XF, EMU0, and EMU1.
In Revision C, EVA (GPIOA0–GPIOA15) and GPIOD0 are 4 mA drive.

7.3 Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = I_{OH}MAX$		2.4			V
V_{OL}	Low-level output voltage		$I_{OL} = I_{OL}MAX$				0.4	V
I_{IL}	Input current (low level)	With pullup	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All I/Os† except EVB		–100		μA
				GPIOB/EVB		–20		
		With pulldown	V_{DDIO} = 3.3 V, V_{IN} = 0 V				±2	
I_{IH}	Input current (high level)	With pullup	V_{DDIO} = 3.3 V, $V_{IN} = V_{DD}$				±2	μA
		With pulldown	V_{DDIO} = 3.3 V, $V_{IN} = V_{DD}$	All I/Os† except EVB		100		
				GPIOB/EVB		20		
I_{OZ}	Output current, high-impedance state (off-state)		$V_O = V_{DDIO}$ or 0 V				±2	μA
C_i	Input capacitance					2		pF
C_o	Output capacitance					3		pF

† The following pins have no internal PU/PD: GPIOE0, GPIOE1, GPIOF0, GPIOF1, GPIOF2, GPIOF3, GPIOF12, GPIOG4, and GPIOG5.

7.4 Current Consumption by Power-Supply Pins Over Recommended Operating Conditions During Low-Power Modes at 150-MHz SYSCLKOUT

MODE	TEST CONDITIONS	TYP I_{DD}	TYP I_{DDIO}	TYP I_{DD3VFL}	TYP I_{DDA}‡
Operational	All peripheral clocks are enabled. All PWM pins are toggled at 100 kHz. Data is continuously transmitted out of the SCIA, SCIB, and CAN ports. The hardware multiplier is exercised.	195 mA	20 mA	50 mA	40 mA
IDLE	– Flash is powered down – XCLKOUT is turned off – All peripheral clocks are on, except ADC	125 mA	5 mA	4 μA	1 μA
STANDBY	– Flash is powered down – Peripheral clocks are turned off – Pins without an internal PU/PD are tied high/low	5 mA	5 μA	4 μA	1 μA
HALT	– Flash is powered down – Peripheral clocks are turned off – Pins without an internal PU/PD are tied high/low – Input clock is disabled	12 μA	5 μA	4 μA	1 μA

‡ I_{DDA} includes current into V_{DDA1}, V_{DDA2}, $AV_{DDREFBG}$, and V_{DDAIO} pins.

CAUTION:
HALT and STANDBY modes cannot be used when the PLL is disabled.

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7.5 Power Sequencing Requirements

TMS320F2812/F2810 silicon requires dual voltages (1.8 V and 3.3 V) to power up the CPU, Flash, ADC, and the I/Os. To ensure the correct reset state for all modules during power up, there are some requirements to be met while powering up/powering down the device. The current F2812 silicon reference schematics (Spectrum Digital Incorporated eZdsp™ board) suggests two options for the power sequencing circuit.

- Option 1:

  In this approach, an external power sequencing circuit enables V_{DDIO} first, then V_{DD} and V_{DD1} (1.8 V). After 1.8 V ramps, the 3.3 V for Flash (V_{DD3VFL}) and ADC (V_{DDA1}/V_{DDA2}/$AV_{DDREFBG}$) modules are ramped up. While option 1 is still valid, TI has simplified the requirement. Option 2 covers the recommended simplified approach.

- Option 2:

  Enable power to all 3.3-V supply pins (V_{DDIO}, V_{DD3VFL}, V_{DDA1}/V_{DDA2}/V_{DDAIO}/$AV_{DDREFBG}$) and then ramp 1.8 V (V_{DD}/V_{DD1}) supply pins.

  1.8 V (V_{DD}/V_{DD1}) should not reach 0.3 V until V_{DDIO} has reached 2.5 V. This ensures the reset signal from the I/O pin has propagated through the I/O buffer to provide power-on reset to all the modules inside the device. See Figure 7–7 for power-on reset timings.

- Power-Down Sequencing:

  During power-down, the device reset should be asserted low (8 μs, minimum) before the V_{DD} supply reaches 1.5 V. This will help to keep on-chip flash logic in reset prior to the V_{DDIO}/V_{DD} power supplies ramping down. It is recommended that the device reset control from “Low-Dropout (LDO)” regulators or voltage supervisors be used to meet this constraint. LDO regulators that facilitate power-sequencing (with the aid of additional external components) may be used to meet the power sequencing requirement. Refer to www.spectrumdigital.com for F2812 eZdsp™ schematics and updates.

Table 7–1. Recommended “Low-Dropout Regulators”

SUPPLIER	PART NUMBER
Texas Instruments	TPS767D301

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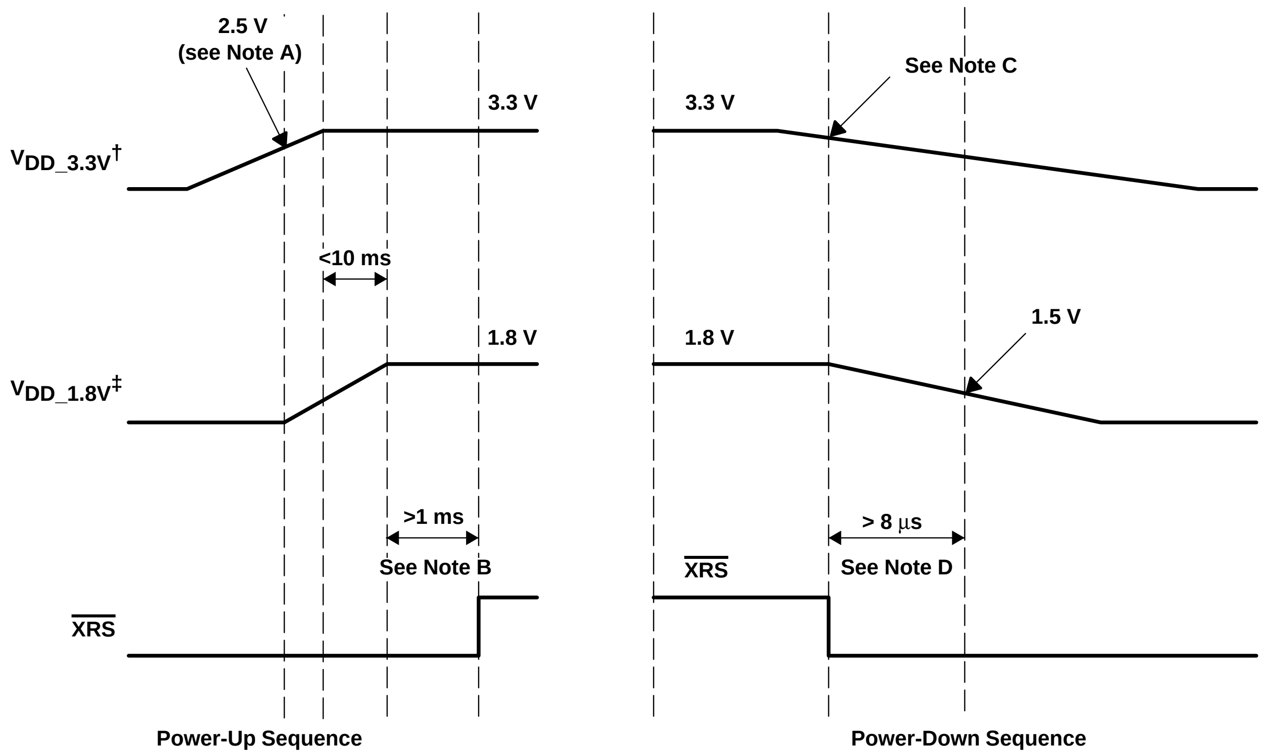
eZdsp is a trademark of Spectrum Digital Incorporated.

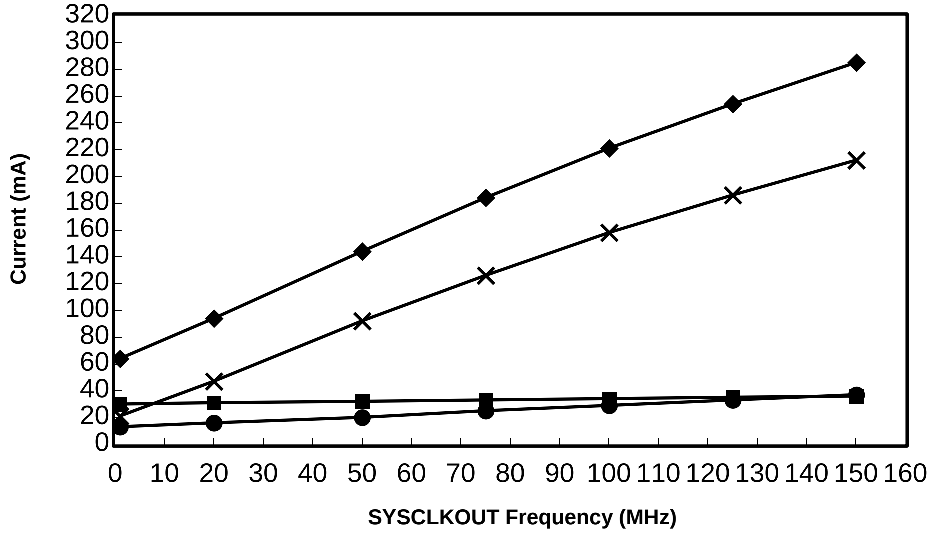


† $V_{DD\_3.3V}$ – V_{DDIO}, V_{DD3VFL}, V_{DDAIO}, V_{DDA1}, V_{DDA2}, $AV_{DDREFBG}$
‡ $V_{DD\_1.8V}$ – V_{DD}, V_{DD1}

NOTES:
- A. 1.8-V supply should ramp after the 3.3-V supply reaches at least 2.5 V.
- B. Reset ($\overline{XRS}$) should remain low until supplies and clocks are stable. Refer to Figure 7–7, Power-on Reset in Microcomputer Mode (XMP/$\overline{MC}$ = 0), for minimum requirements.
- C. Voltage supervisor or LDO reset control will trip reset ($\overline{XRS}$) first when the 3.3-V supply is off regulation. Typically, this occurs a few milliseconds before the 1.8-V supply reaches 1.5 V.
- D. Keeping reset low ($\overline{XRS}$) at least 8 µs prior to the 1.8-V supply reaching 1.5 V will keep the flash module in complete reset before the supplies ramp down.
- E. Since the state of GPIO pins is undefined until the 1.8-V supply reaches at least 1 V, this supply should be ramped as quickly as possible (after the 3.3-V supply reaches at least 2.5 V).

Figure 7–1. F2812/F2810 Typical Power-Up and Power-Down Sequence – Option 2

7.6 Current Consumption Graphs



LEGEND:
◆ – **Total**
x – **I_{DD} + I_{DDIO}**
■ – **I_{DDA1}**
● – **I_{DD3VFL}**

NOTES: A. Flash uses five wait-states for paged and random access for frequencies above 5 MHz. For frequencies of 1 to 5 MHz, it was made to operate at zero wait-states.
B. ADC operates at SYSCLKOUT/6 for frequencies above 5 MHz. For frequencies of 1 to 5 MHz, it was made to operate at SYSCLKOUT. This explains a small discontinuity of data between 5 and 10 MHz.

Figure 7–2. F2812/F2810 Typical Current Consumption (With Peripheral Clocks Enabled)

7.7 Reducing Current Consumption

28x DSPs incorporate a unique method to reduce the device current consumption. A reduction in current consumption can be achieved by turning off the clock to any peripheral module which is not used in a given application. Table 7–2 indicates the typical reduction in current consumption achieved by turning off the clocks to various peripherals.

Table 7–2. Typical Current Consumption by Various Peripherals (at 150 MHz)†

PERIPHERAL MODULE	I_{DD} CURRENT REDUCTION (mA)
eCAN	12
EVA	6
EVB	6
ADC	8‡
SCI	4
SPI	5
McBSP	13

† ***All peripheral clocks are disabled upon reset. Writing to/reading from peripheral registers is possible only after the peripheral clocks are turned on.***
‡ This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I_{CCA}) as well.

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7.8 Signal Transition Levels

The data in this section is shown for the 3.3-V version. Note that some of the signals use different reference voltages, see the recommended operating conditions table. Output levels are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.4 V.

Figure 7–3 shows output levels.

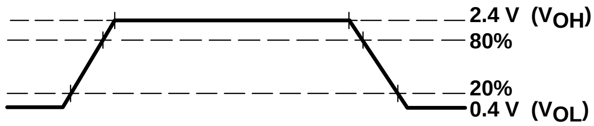


Figure 7–3. Output Levels

Output transition times are specified as follows:

- For a *high-to-low transition*, the level at which the output is said to be no longer high is below 80% of the total voltage range and lower and the level at which the output is said to be low is 20% of the total voltage range and lower.
- For a *low-to-high transition*, the level at which the output is said to be no longer low is 20% of the total voltage range and higher and the level at which the output is said to be high is 80% of the total voltage range and higher.

Figure 7–4 shows the input levels.

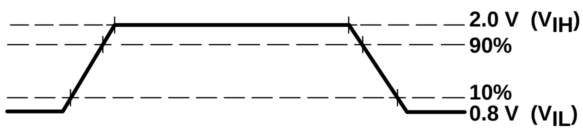


Figure 7–4. Input Levels

Input transition times are specified as follows:

- For a *high-to-low transition* on an input signal, the level at which the input is said to be no longer high is 90% of the total voltage range and lower and the level at which the input is said to be low is 10% of the total voltage range and lower.
- For a *low-to-high transition* on an input signal, the level at which the input is said to be no longer low is 10% of the total voltage range and higher and the level at which the input is said to be high is 90% of the total voltage range and higher.

  NOTE: Refer to the individual timing diagrams for levels used for testing timing parameters.

7.9 Timing Parameter Symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:		Letters and symbols and their meanings:	
a	access time	H	High
c	cycle time (period)	L	Low
d	delay time	V	Valid
f	fall time	X	Unknown, changing, or don't care level
h	hold time	Z	High impedance
r	rise time		
su	setup time		
t	transition time		
v	valid time		
w	pulse duration (width)		

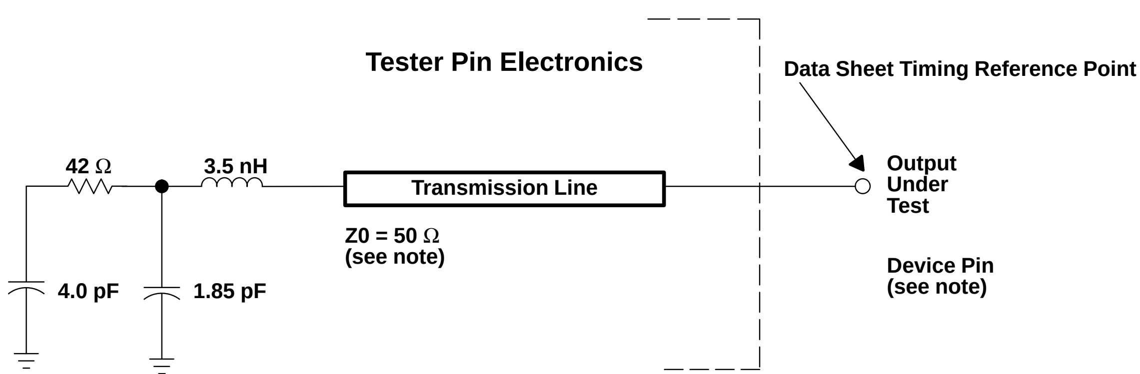
7.10 General Notes on Timing Parameters

All output signals from the 28x devices (including XCLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, refer to the appropriate cycle description section of this document.

7.11 Test Load Circuit

This test load circuit is used to measure all switching characteristics provided in this document.



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 7–5. 3.3-V Test Load Circuit

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7.12 Device Clock Table

This section provides the timing requirements and switching characteristics for the various clock options available on the F2810 and F2812 DSPs. Table 7–3 lists the cycle times of various clocks.

Table 7–3. TMS320F2812 Clock Table and Nomenclature

		MIN	NOM	MAX	UNIT
On-chip oscillator clock	$t_{c(OSC)}$, Cycle time	28.6	33.3	50	ns
	Frequency	20	30	35	MHz
XCLKIN	$t_{c(CI)}$, Cycle time	6.67	33.3	250	ns
	Frequency	4	30	150	MHz
SYSCLKOUT	$t_{c(SCO)}$, Cycle time	6.67		500	ns
	Frequency	2		150	MHz
XCLKOUT	$t_{c(XCO)}$, Cycle time	6.67		2000	ns
	Frequency	0.5		150	MHz
HSPCLK	$t_{c(HCO)}$, Cycle time	6.67	13.3		ns
	Frequency		75	150	MHz
LSPCLK	$t_{c(LCO)}$, Cycle time	13.3	26.6		ns
	Frequency		37.5	75	MHz
ADC clock	$t_{c(ADCCLK)}$, Cycle time†	40			ns
	Frequency			25	MHz
SPI clock	$t_{c(SPC)}$, Cycle time	50			ns
	Frequency			20	MHz
McBSP	$t_{c(CKG)}$, Cycle time	50			ns
	Frequency			20	MHz
XTIMCLK	$t_{c(XTIM)}$, Cycle time	6.67			ns
	Frequency			150	MHz

† The maximum value for ADCCLK frequency is 25 MHz. For SYSCLKOUT values of 25 MHz or lower, ADCCLK has to be SYSCLKOUT/2 or lower. ADCCLK = SYSCLKOUT is not a valid mode for any value of SYSCLKOUT.

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7.13 Clock Requirements and Characteristics

7.13.1 Input Clock Requirements

The clock provided at the XCLKIN pin generates the internal CPU clock cycle.

Table 7–4. Input Clock Frequency

PARAMETER			MIN	MAX	UNIT
f_x	Input clock frequency	Resonator	20	35	MHz
		Crystal	20	35	
		XCLKIN	4	150	

Table 7–5. XCLKIN Timing Requirements – PLL Bypassed or Enabled

NO.				MIN	NOM	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN		6.67		250	ns
C9	$t_{f(CI)}$	Fall time, XCLKIN	Up to 30 MHz			6	ns
			Up to 150 MHz			2	
C10	$t_{r(CI)}$	Rise time, XCLKIN	Up to 30 MHz			6	ns
			Up to 150 MHz			2	
C11	$t_{w(CIL)}$	Pulse duration, X1/XCLKIN low as a percentage of $t_{c(CI)}$		40		60	%
C12	$t_{w(CIH)}$	Pulse duration, X1/XCLKIN high as a percentage of $t_{c(CI)}$		40		60	%

Table 7–6. XCLKIN Timing Requirements – PLL Disabled

NO.				MIN	NOM	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN		6.67		250	ns
C9	$t_{f(CI)}$	Fall time, XCLKIN	Up to 30 MHz			6	ns
			Up to 150 MHz			2	
C10	$t_{r(CI)}$	Rise time, XCLKIN	Up to 30 MHz			6	ns
			Up to 150 MHz			2	
C11	$t_{w(CIL)}$	Pulse duration, X1/XCLKIN low as a percentage of $t_{c(CI)}$		50		50	%
C12	$t_{w(CIH)}$	Pulse duration, X1/XCLKIN high as a percentage of $t_{c(CI)}$		50		50	%

Table 7–7. Possible PLL Configuration Modes

PLL MODE	REMARKS	SYSCLKOUT
PLL Disabled	Invoked by tying $\overline{\text{XPLLDIS}}$ pin low upon reset. PLL block is completely disabled. Clock input to the CPU (CLKIN) is directly derived from the clock signal present at the X1/XCLKIN pin.	XCLKIN
PLL Bypassed	Default PLL configuration upon power-up, if PLL is not disabled. The PLL itself is bypassed. However, the /2 module in the PLL block divides the clock input at the X1/XCLKIN pin by two before feeding it to the CPU.	XCLKIN/2
PLL Enabled	Achieved by writing a non-zero value “n” into PLLCR register. The /2 module in the PLL block now divides the output of the PLL by two before feeding it to the CPU.	(XCLKIN * n) / 2

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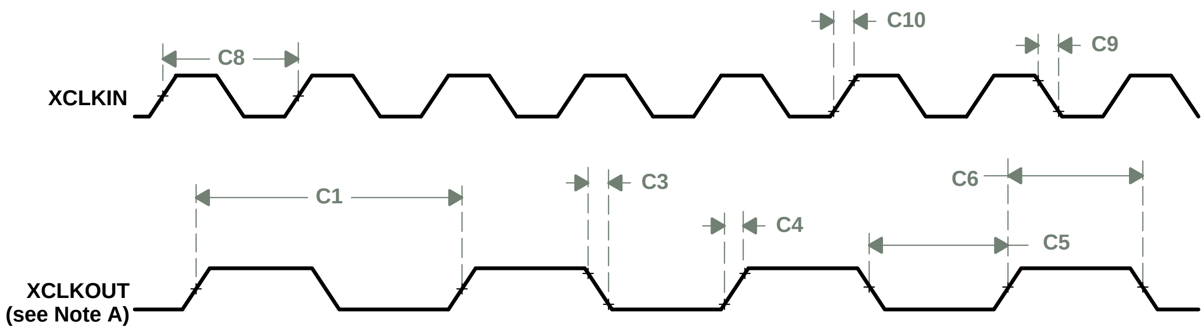
7.13.2 Output Clock Characteristics

Table 7–8. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)†‡

NO.	PARAMETER		MIN	TYP	MAX	UNIT
C1	$t_{c(XCO)}$	Cycle time, XCLKOUT	6.67§			ns
C3	$t_{f(XCO)}$	Fall time, XCLKOUT		2		ns
C4	$t_{r(XCO)}$	Rise time, XCLKOUT		2		ns
C5	$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H–2		H+2	ns
C6	$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H–2		H+2	ns
C7	t_p	PLL lock time¶			$131\,072t_{c(CI)}$	ns

† A load of 40 pF is assumed for these parameters.
‡ H = $0.5t_{c(XCO)}$
§ The PLL must be used for maximum frequency operation.
¶ This parameter has changed from 4096 XCLKIN cycles in the earlier revisions of the silicon.



NOTES: A. XCLKOUT configured to reflect SYSCLKOUT.
B. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship shown in Figure 7–6 is intended to illustrate the timing parameters only and may differ based on configuration.

Figure 7–6. Clock Timing

7.14 Reset Timings

Table 7–9. Reset ($\overline{XRS}$) Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, stable XCLKIN to $\overline{XRS}$ high		$8t_{c(CI)}$			cycles
$t_{w(RSL2)}$	Pulse duration, $\overline{XRS}$ low	Warm reset	$8t_{c(CI)}$			cycles
		WD-initiated reset		$512t_{c(CI)}$		
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog			$512t_{c(CI)}$		cycles
$t_{d(EX)}$	Delay time, address/data valid after $\overline{XRS}$ high			$32t_{c(CI)}$		cycles
t_{OSCST}†	Oscillator start-up time		1	10		ms
$t_{su(XPLLDIS)}$	Setup time for $\overline{XPLLDIS}$ pin		$16t_{c(CI)}$			cycles
$t_{h(XPLLDIS)}$	Hold time for $\overline{XPLLDIS}$ pin		$16t_{c(CI)}$			cycles
$t_{h(XMP/MC)}$	Hold time for XMP/$\overline{MC}$ pin		$16t_{c(CI)}$			cycles
$t_{h(boot\text{-}mode)}$	Hold time for boot-mode pins		$2520t_{c(CI)}$			cycles

† Dependent on crystal/resonator and board design.

NOTE: If external oscillator/clock source are used, reset time has to be low at least for 1 ms after V_{DD} reaches 1.5 V.

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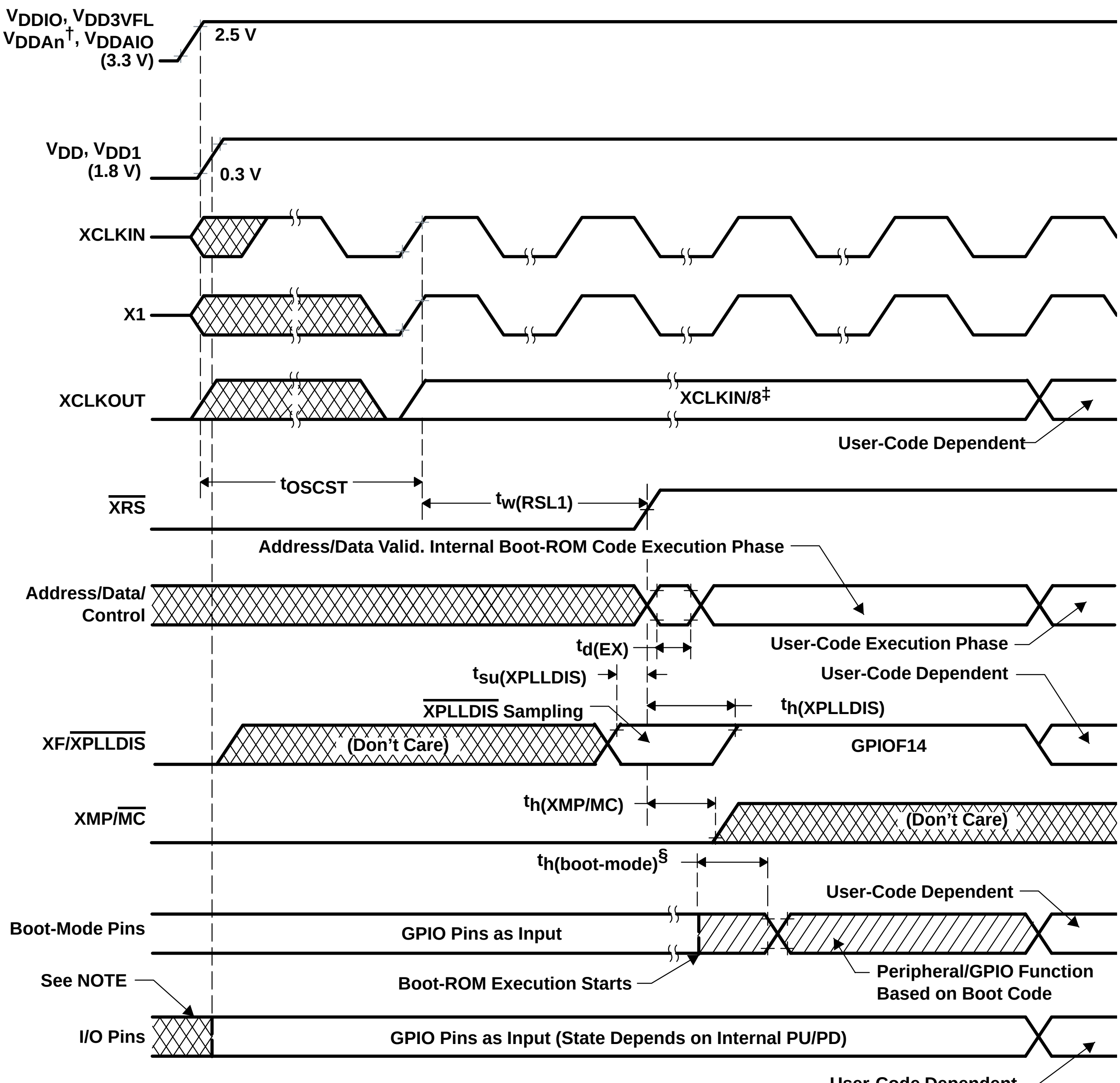


† V_{DDAn} – V_{DDA1}/V_{DDA2} and $AV_{DDREFBG}$

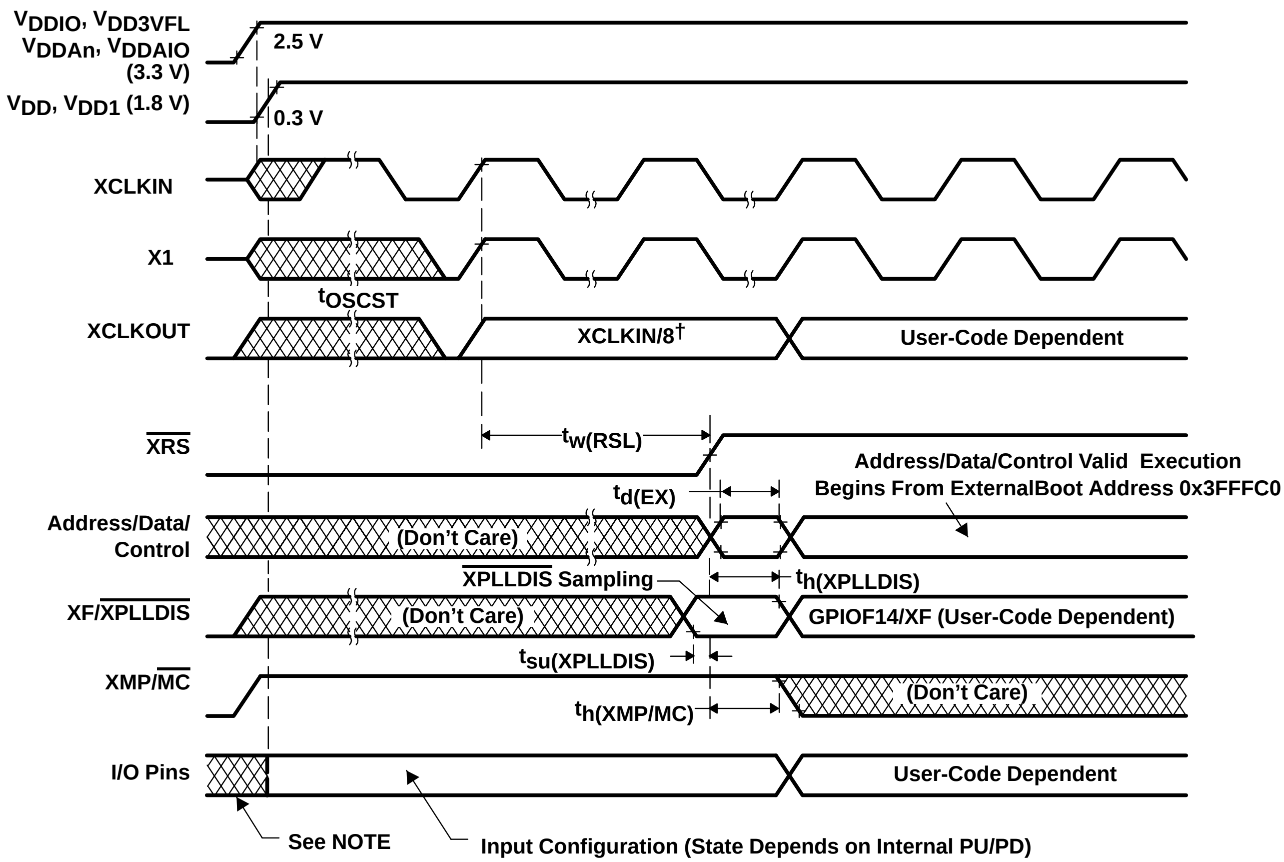
‡ Upon power up, SYSCLKOUT is XCLKIN/2 if the PLL is enabled. Since both the XTIMCLK and CLKMODE bits in the XINTCNF2 register come up with a reset state of 1, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. This explains why XCLKOUT = XCLKIN/8 during this phase.

§ After reset, the Boot ROM code executes instructions for 1260 SYSCLKOUT cycles (SYSCLKOUT = XCLKIN/2) and then samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function in ROM. The BOOT Mode pins should be held high/low for at least 2520 XCLKIN cycles from boot ROM execution time for proper selection of Boot modes.

If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

NOTE: The state of the GPIO pins are undefined (i.e., they could be input or output) until the 1.8-V supply reaches at least 1 V.

Figure 7–7. Power-on Reset in Microcomputer Mode (XMP/$\overline{\text{MC}}$ = 0)



† Upon power up, SYSCLKOUT is XCLKIN/2 if the PLL is enabled. Since both the XTIMCLK and CLKMODE bits in the XINTCNF2 register come up with a reset state of 1, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. This explains why XCLKOUT = XCLKIN/8 during this phase.

NOTE: The state of the GPIO pins are undefined (i.e., they could be input or output) until the 1.8-V supply reaches at least 1 V.

Figure 7–8. Power-on Reset in Microprocessor Mode (XMP/MC = 1)

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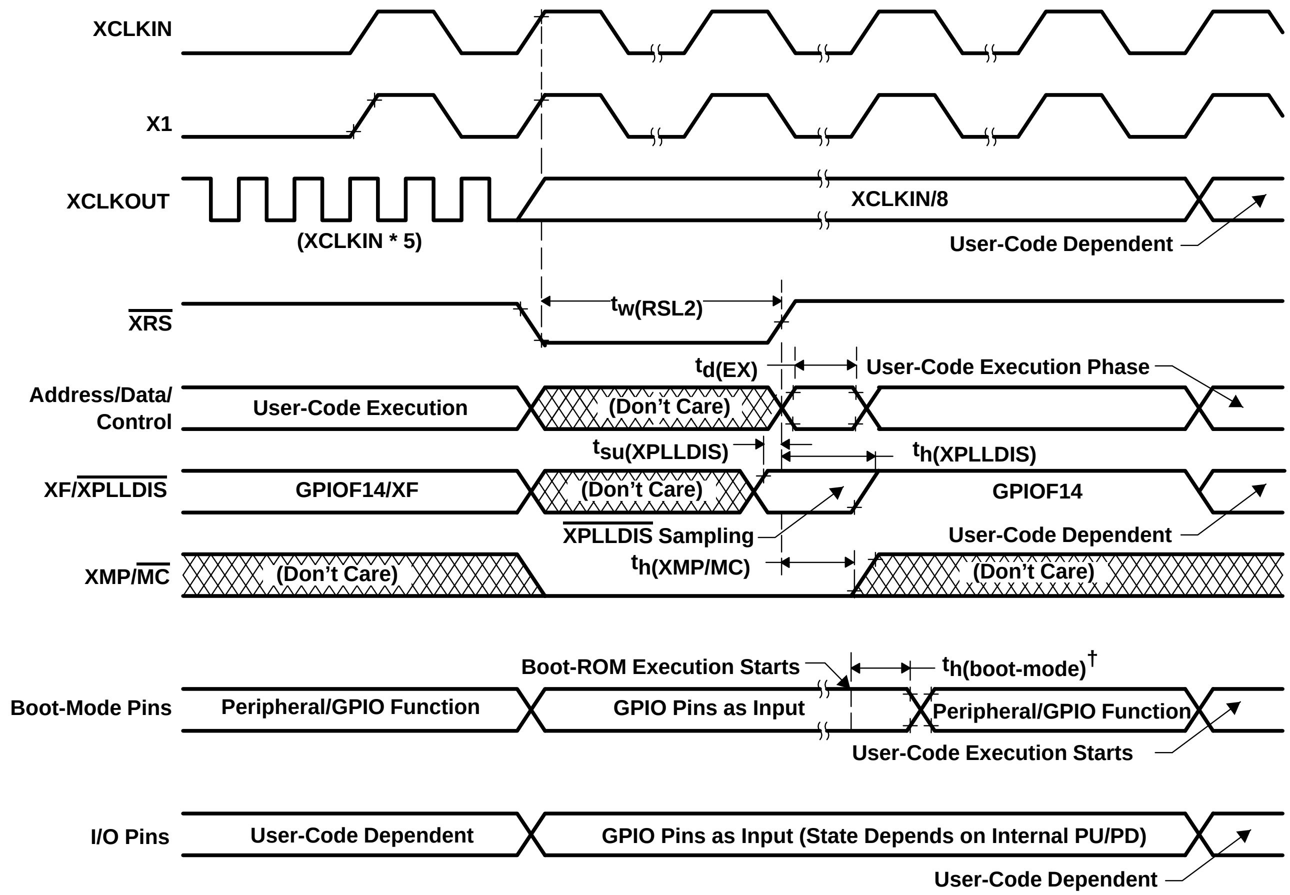
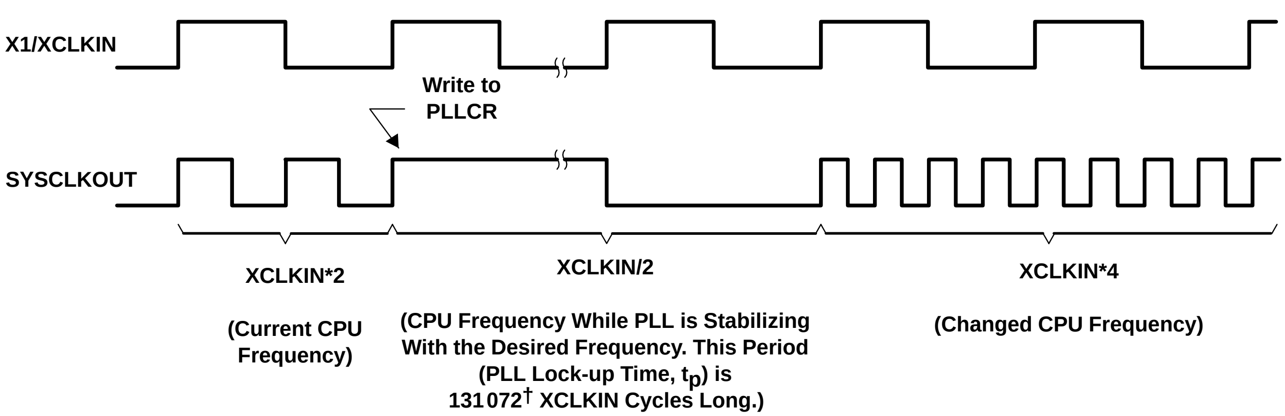


† After reset, the Boot ROM code executes instructions for 1260 SYSCLKOUT cycles (SYSCLKOUT = XCLKIN/2) and then samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function in ROM. The BOOT Mode pins should be held high/low for at least 2520 XCLKIN cycles from boot ROM execution time for proper selection of Boot modes.
If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

Figure 7–9. Warm Reset in Microcomputer Mode



† This parameter has been changed from 4096 to 131 072 XCLKIN cycles.

Figure 7–10. Effect of Writing Into PLLCR Register

7.15 Event Manager Interface

7.15.1 PWM Timings

PWM refers to all PWM outputs on EVA and EVB.

Table 7–10. PWM Switching Characteristics†‡

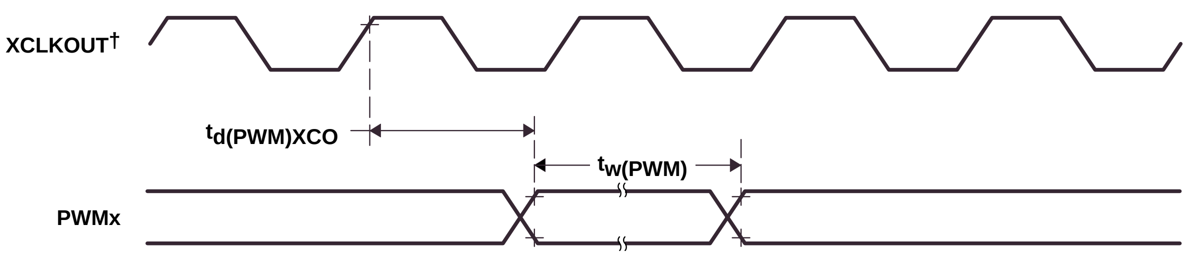
PARAMETER		MIN	MAX	UNIT
$t_{w(PWM)}$§	Pulse duration, PWMx output high/low	25		ns
$t_{d(PWM)XCO}$	Delay time, XCLKOUT high to PWMx output switching		10	ns

† Refer to the GPIO output timing for fall/rise times for PWM pins.
‡ PWM pin toggling frequency is limited by the GPIO output buffer switching frequency (20 MHz).
§ PWM outputs may be 100%, 0%, or increments of $t_{c(HCO)}$ with respect to the PWM period.

Table 7–11. PWM Timing Requirements¶

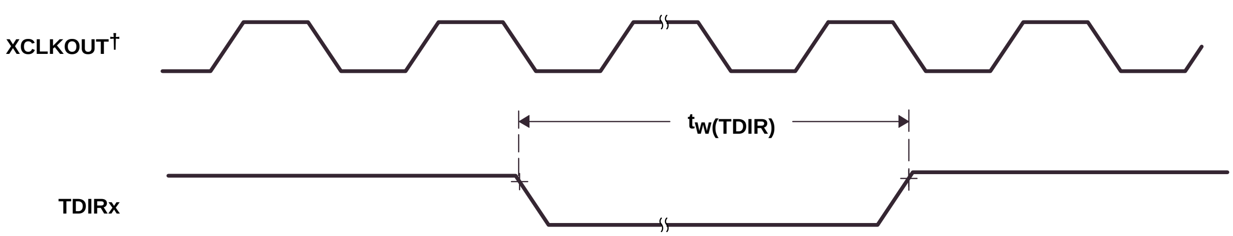
			MIN	MAX	UNIT
$t_{w(TDIR)}$	Pulse duration, TDIRx low/high	Without input qualifier	$2 * t_{c(SCO)}$		cycles
		With input qualifier	$1 * t_{c(SCO)}$ + IQT#		cycles
$t_{w(TCLKINL)}$	Pulse duration, TCLKINx low as a percentage of TCLKINx cycle time		40	60	%
$t_{w(TCLKINH)}$	Pulse duration, TCLKINx high as a percentage of TCLKINx cycle time		40	60	%
$t_{c(TCLKIN)}$	Cycle time, TCLKINx		$4 \times t_{c(HCO)}$		ns

¶ The QUALPRD bit field value can range from 0 (no qualification) through 0xFF (510 SYSCLKOUT cycles). The qualification sampling period is 2n SYSCLKOUT cycles, where “n” is the value stored in the QUALPRD bit field. As an example, when QUALPRD = 1, the qualification sampling period is 1 x 2 = 2 SYSCLKOUT cycles (i.e., the input is sampled every 2 SYSCLKOUT cycles). Six such samples will be taken over five sampling windows, each window being 2n SYSCLKOUT cycles. For QUALPRD = 1, the minimum width that is needed is 5 x 2 = 10 SYSCLKOUT cycles. However, since the external signal is driven asynchronously, a 11-SYSCLKOUT-wide pulse ensures reliable recognition.
# Input Qualification Time (IQT) = [5 x QUALPRD x 2] * $t_{c(SCO)}$



† XCLKOUT = SYSCLKOUT

Figure 7–11. PWM Output Timing



† XCLKOUT = SYSCLKOUT

Figure 7–12. TDIRx Timing

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Table 7–12. External ADC Start-of-Conversion – EVA – Switching Characteristics†

PARAMETER		MIN	MAX	UNIT
$t_{d(XCOH\text{-}EVASOCL)}$	Delay time, XCLKOUT high to $\overline{\text{EVASOC}}$ low		1 * $t_{c(SCO)}$	cycle
$t_{w(EVASOCL)}$	Pulse duration, $\overline{\text{EVASOC}}$ low	32 * $t_{c(HCO)}$		ns

† XCLKOUT = SYSCLKOUT

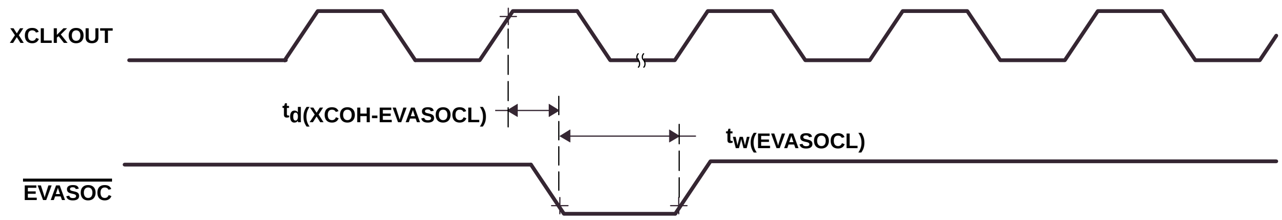

Figure 7–13. $\overline{\text{EVASOC}}$ Timing

Table 7–13. External ADC Start-of-Conversion – EVB – Switching Characteristics†

PARAMETER		MIN	MAX	UNIT
$t_{d(XCOH\text{-}EVBSOCL)}$	Delay time, XCLKOUT high to $\overline{\text{EVBSOC}}$ low		1 * $t_{c(SCO)}$	cycle
$t_{w(EVBSOCL)}$	Pulse duration, $\overline{\text{EVBSOC}}$ low	32 * $t_{c(HCO)}$		ns

† XCLKOUT = SYSCLKOUT

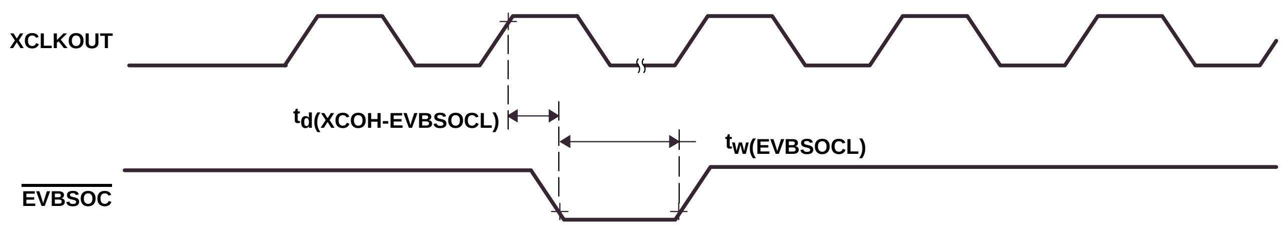

Figure 7–14. $\overline{\text{EVBSOC}}$ Timing

7.15.2 Interrupt Timings

Table 7–14. Interrupts Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(PDP\text{-}PWM)HZ}$	Delay time, $\overline{\text{PDPINTx}}$ low to PWM high-impedance state	Without input qualifier		12	ns
		With input qualifier		$1 * t_{c(SCO)}$ + IQT + 12†	
$t_{d(TRIP\text{-}PWM)HZ}$	Delay time, $\overline{\text{CxTRIP}}$/$\overline{\text{TxCTRIP}}$ signals low to PWM high-impedance state	Without input qualifier		$3 * t_{c(SCO)}$	ns
		With input qualifier		$[2 * t_{c(SCO)}]$ + IQT†	
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch		$t_{qual} + 12t_{c(XCO)}$		ns

† Input Qualification Time (IQT) = [5 x QUALPRD x 2] * $t_{c(SCO)}$

Table 7–15. Interrupts Timing Requirements

			MIN	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	with no qualifier	$2 * t_{c(SCO)}$		cycles
		with qualifier	$1 * t_{c(SCO)}$ + IQT†		
$t_{w(PDP)}$	Pulse duration, $\overline{\text{PDPINTx}}$ input low	with no qualifier	$2 * t_{c(SCO)}$		cycles
		with qualifier	$1 * t_{c(SCO)}$ + IQT†		
$t_{w(CxTRIP)}$	Pulse duration, $\overline{\text{CxTRIP}}$ input low	with no qualifier	$2 * t_{c(SCO)}$		cycles
		with qualifier	$1 * t_{c(SCO)}$ + IQT†		
$t_{w(TxCTRIP)}$	Pulse duration, $\overline{\text{TxCTRIP}}$ input low	with no qualifier	$2 * t_{c(SCO)}$		cycles
		with qualifier	$1 * t_{c(SCO)}$ + IQT†		

† Input Qualification Time (IQT) = [5 x QUALPRD x 2] * $t_{c(SCO)}$

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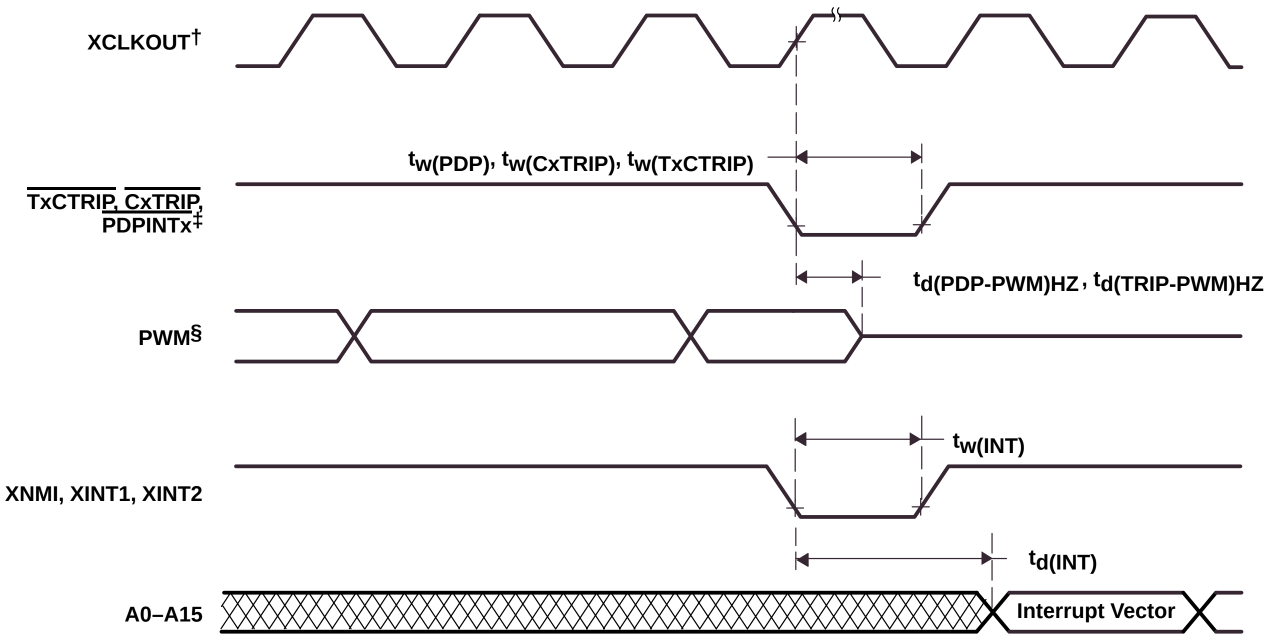

† XCLKOUT = SYSCLKOUT
‡ TxCTRIP – T1CTRIP, T2CTRIP, T3CTRIP, T4CTRIP
CxTRIP – C1TRIP, C2TRIP, C3TRIP, C4TRIP, C5TRIP, or C6TRIP
PDPINTx – PDPINTA or PDPINTB
§ PWM refers to **all** the PWM pins in the device (i.e., PWMn and TnPWM pins or PWM pin pair relevant to each CxTRIP pin). The state of the PWM pins after PDPINTx is taken high depends on the state of the FCOMPOE bit.

Figure 7–15. External Interrupts Timing

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7.16 General-Purpose Input/Output (GPIO) – Output Timings

Table 7–16. General-Purpose Output Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(XCOH-GPO)}$	Delay time, XCLKOUT high to GPIO low/high	All GPIOs		1 * $t_{c(SCO)}$	cycle
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		10	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		10	ns
f_{GPO}	Toggling frequency, GPO pins			20	MHz

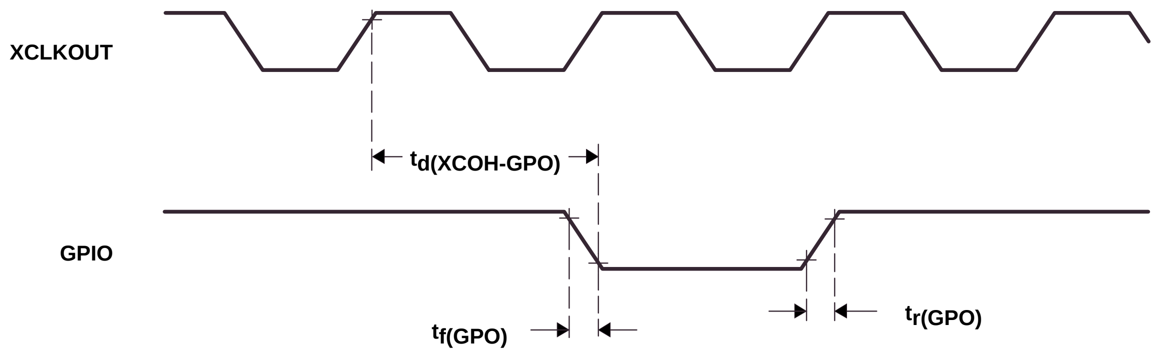

Figure 7–16. General-Purpose Output Timing

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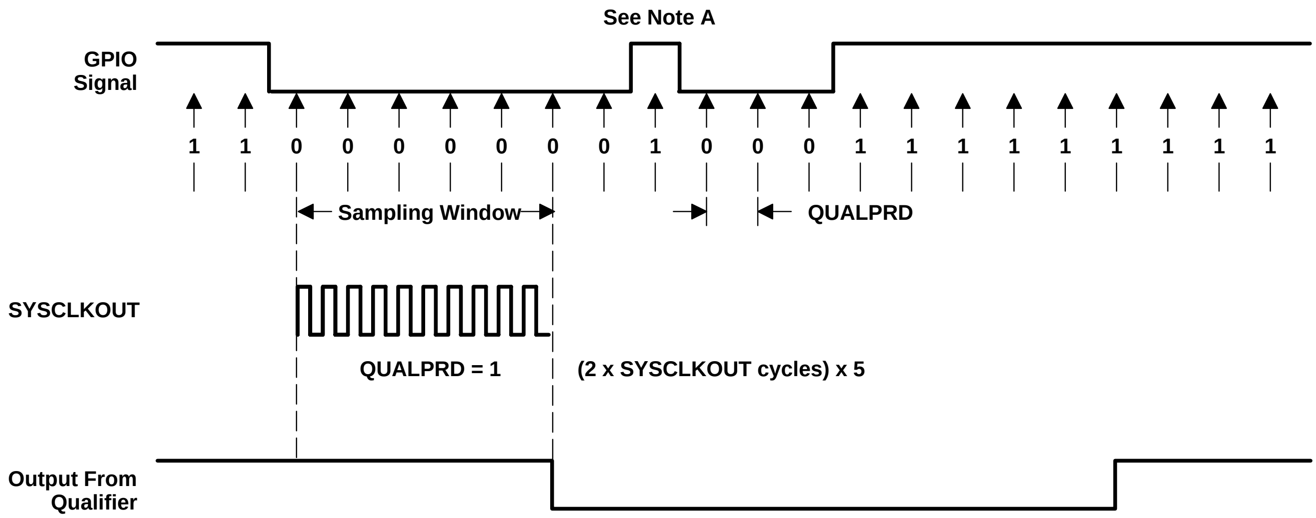
7.17 General-Purpose Input/Output (GPIO) – Input Timings



NOTES: A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. Input qualification is not applicable when QUALPRD = 00. For any other value “n”, the qualification sampling period in 2n SYSCLKOUT cycles (i.e., at every 2n SYSCLKOUT cycle, the GPIO pin will be sampled). Six consecutive samples must be of the same value for a given input to be recognized.

B. For the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles are greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLKOUT cycles. This would ensure six sampling windows for detection to occur. Since external signals are driven asynchronously, a 11-SYSCLKOUT-wide pulse ensures reliable recognition.

Figure 7–17. GPIO Input Qualifier – Example Diagram for QUALPRD = 1

Table 7–17. General-Purpose Input Timing Requirements

				MIN	MAX	UNIT
$t_{w(GPI)}$	Pulse duration, GPIO low/high	All GPIOs	With no qualifier	$2 * t_{c(SCO)}$		cycles
			With qualifier	$1 * t_{c(SCO)}$ + IQT†		

† Input Qualification Time (IQT) = [5 x QUALPRD x 2] * $t_{c(SCO)}$

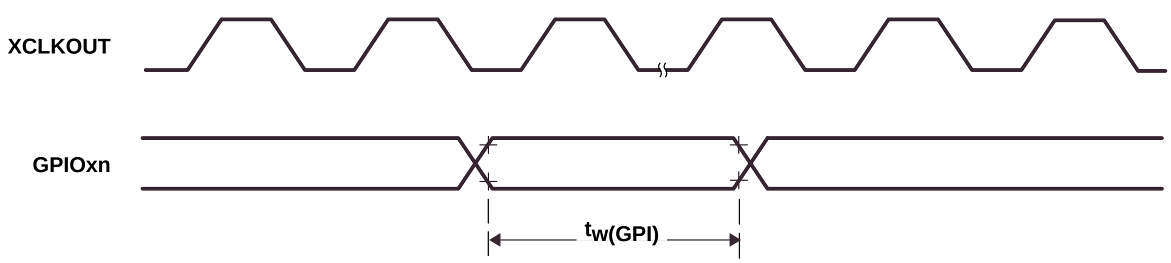


Figure 7–18. General-Purpose Input Timing

NOTE: The pulse width requirement for general-purpose input is applicable for the $\overline{\text{XBIO}}$ and ADCSOC pins as well.

7.18 SPI Master Mode Timings

Table 7–18. SPI Master Mode External Timings (Clock Phase = 0)†‡

NO.			SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2		SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2§	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}-10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}-0.5t_{c(LCO)}-10$	$0.5t_{c(SPC)M}-0.5t_{c(LCO)}$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}-10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}-0.5t_{c(LCO)}-10$	$0.5t_{c(SPC)M}-0.5t_{c(LCO)}$	
3§	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M}-10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}+0.5t_{c(LCO)}-10$	$0.5t_{c(SPC)M}+0.5t_{c(LCO)}$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M}-10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}+0.5t_{c(LCO)}-10$	$0.5t_{c(SPC)M}+0.5t_{c(LCO)}$	
4§	$t_{d(SPCH-SIMO)M}$	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)	– 10	10	– 10	10	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)	– 10	10	– 10	10	
5§	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M}-10$		$0.5t_{c(SPC)M}+0.5t_{c(LCO)}-10$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M}-10$		$0.5t_{c(SPC)M}+0.5t_{c(LCO)}-10$		
8§	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	0		0		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	0		0		
9§	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.25t_{c(SPC)M}-10$		$0.5t_{c(SPC)M}-0.5t_{c(LCO)}-10$		ns
	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.25t_{c(SPC)M}-10$		$0.5t_{c(SPC)M}-0.5t_{c(LCO)}-10$		

† The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.

‡ $t_{c(SPC)}$ = SPI clock cycle time = $\frac{LSPCLK}{4}$ or $\frac{LSPCLK}{(SPIBRR + 1)}$

$t_{c(LCO)}$ = LSPCLK cycle time

§ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

NOTE: Internal clock prescalars have to be adjusted such that the SPI clock speed is not greater than the I/O buffer speed limit (20 MHz).

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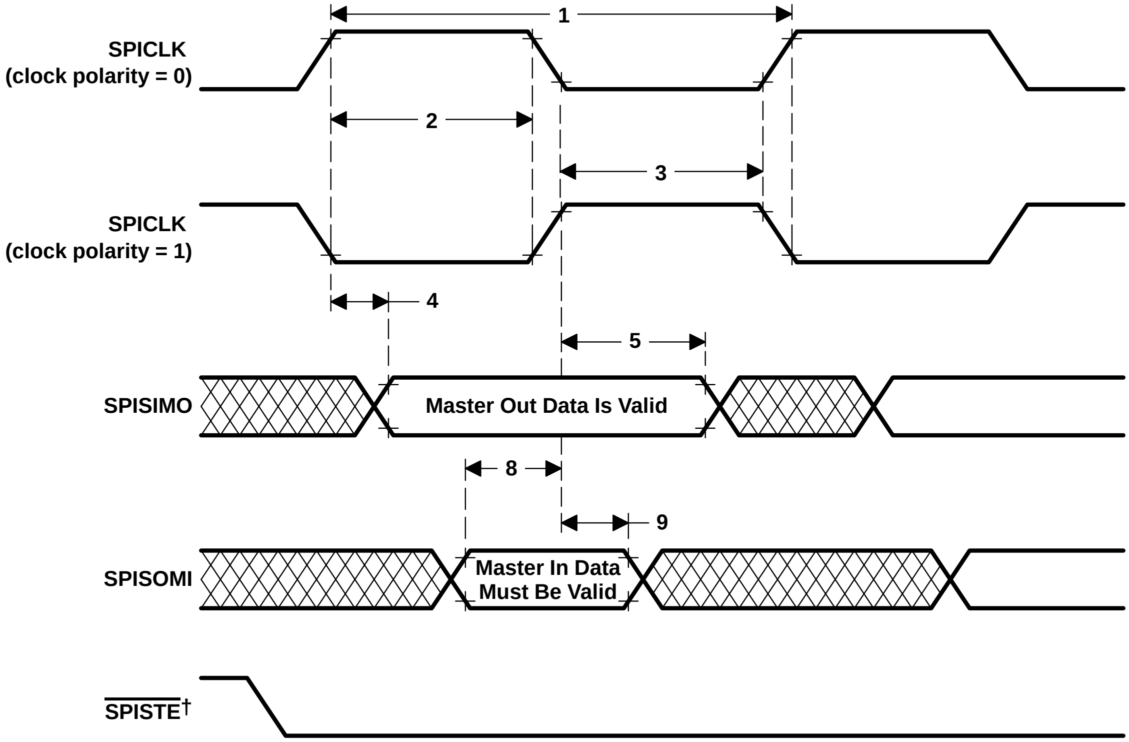

† The $\overline{\text{SPISTE}}$ signal must be active before the SPI communication stream starts; the $\overline{\text{SPISTE}}$ signal must remain active until the SPI communication stream is complete.

Figure 7–19. SPI Master Mode External Timing (Clock Phase = 0)

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Table 7–19. SPI Master Mode External Timings (Clock Phase = 1)†‡

NO.			SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2		SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2§	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}-10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}-0.5t_{c(LCO)}-10$	$0.5t_{c(SPC)M}-0.5t_{c(LCO)}$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}-10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}-0.5t_{c(LCO)}-10$	$0.5t_{c(SPC)M}-0.5t_{c(LCO)}$	
3§	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M}-10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}+0.5t_{c(LCO)}-10$	$0.5t_{c(SPC)M}+0.5t_{c(LCO)}$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M}-10$	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}+0.5t_{c(LCO)}-10$	$0.5t_{c(SPC)M}+0.5t_{c(LCO)}$	
6§	$t_{su(SIMO-SPCH)M}$	Setup time, SPISIMO data valid before SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}-10$		$0.5t_{c(SPC)M}-10$		ns
	$t_{su(SIMO-SPCL)M}$	Setup time, SPISIMO data valid before SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}-10$		$0.5t_{c(SPC)M}-10$		
7§	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}-10$		$0.5t_{c(SPC)M}-10$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}-10$		$0.5t_{c(SPC)M}-10$		
10§	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	0		0		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	0		0		
11§	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$0.25t_{c(SPC)M}-10$		$0.5t_{c(SPC)M}-10$		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$0.25t_{c(SPC)M}-10$		$0.5t_{c(SPC)M}-10$		

† The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.

‡ $t_{c(SPC)}$ = SPI clock cycle time = $\frac{LSPCLK}{4}$ or $\frac{LSPCLK}{(SPIBRR + 1)}$

$t_{c(LCO)}$ = LSPCLK cycle time

§ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

NOTE: Internal clock prescalars have to be adjusted such that the SPI clock speed is not greater than the I/O buffer speed limit (20 MHz).

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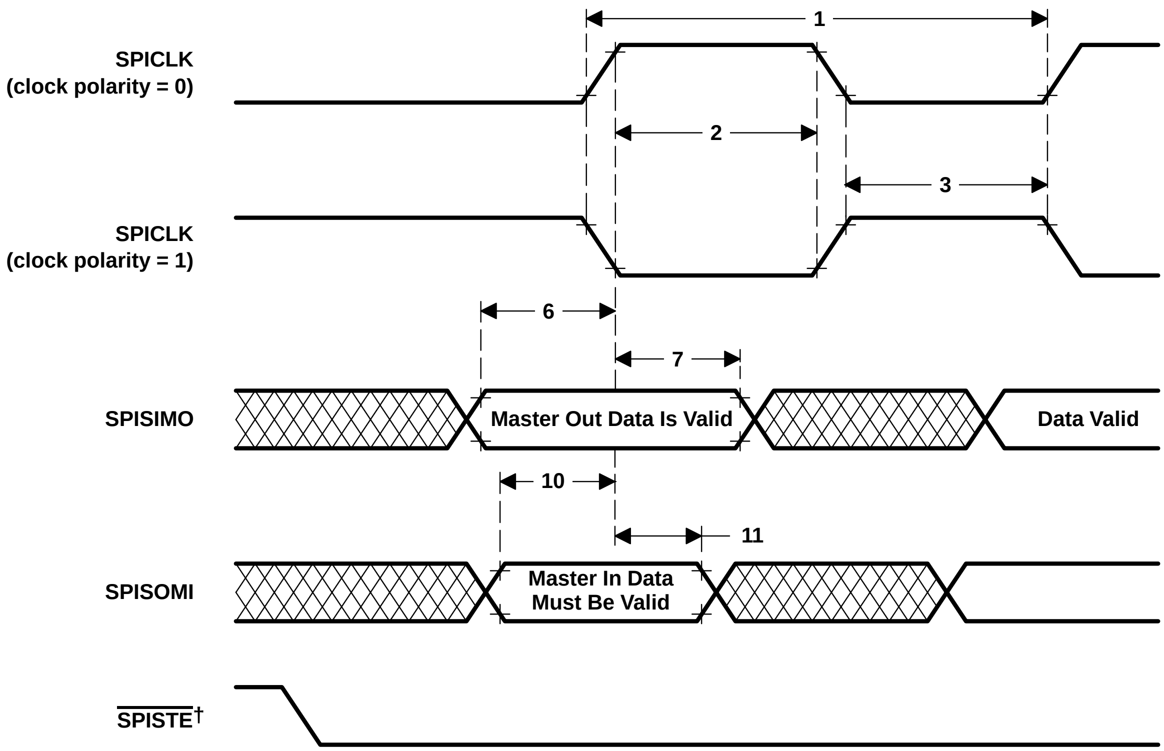

† The SPISTE signal must be active before the SPI communication stream starts; the SPISTE signal must remain active until the SPI communication stream is complete.

Figure 7–20. SPI Master External Timing (Clock Phase = 1)

7.19 SPI Slave Mode Timings

Table 7–20. SPI Slave Mode External Timings (Clock Phase = 0)†‡

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(LCO)}$‡		ns
13§	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S}-10$	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S}-10$	$0.5t_{c(SPC)S}$	
14§	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S}-10$	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S}-10$	$0.5t_{c(SPC)S}$	
15§	$t_{d(SPCH\text{-}SOMI)S}$	Delay time, SPICLK high to SPISOMI valid (clock polarity = 0)	$0.375t_{c(SPC)S}-10$		ns
	$t_{d(SPCL\text{-}SOMI)S}$	Delay time, SPICLK low to SPISOMI valid (clock polarity = 1)	$0.375t_{c(SPC)S}-10$		
16§	$t_{v(SPCL\text{-}SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity =0)	$0.75t_{c(SPC)S}$		ns
	$t_{v(SPCH\text{-}SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity =1)	$0.75t_{c(SPC)S}$		
19§	$t_{su(SIMO\text{-}SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	0		ns
	$t_{su(SIMO\text{-}SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	0		
20§	$t_{v(SPCL\text{-}SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S}$		ns
	$t_{v(SPCH\text{-}SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S}$		

† The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.

‡ $t_{c(SPC)}$ = SPI clock cycle time = $\frac{LSPCLK}{4}$ or $\frac{LSPCLK}{(SPIBRR + 1)}$

$t_{c(LCO)}$ = LSPCLK cycle time

§ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

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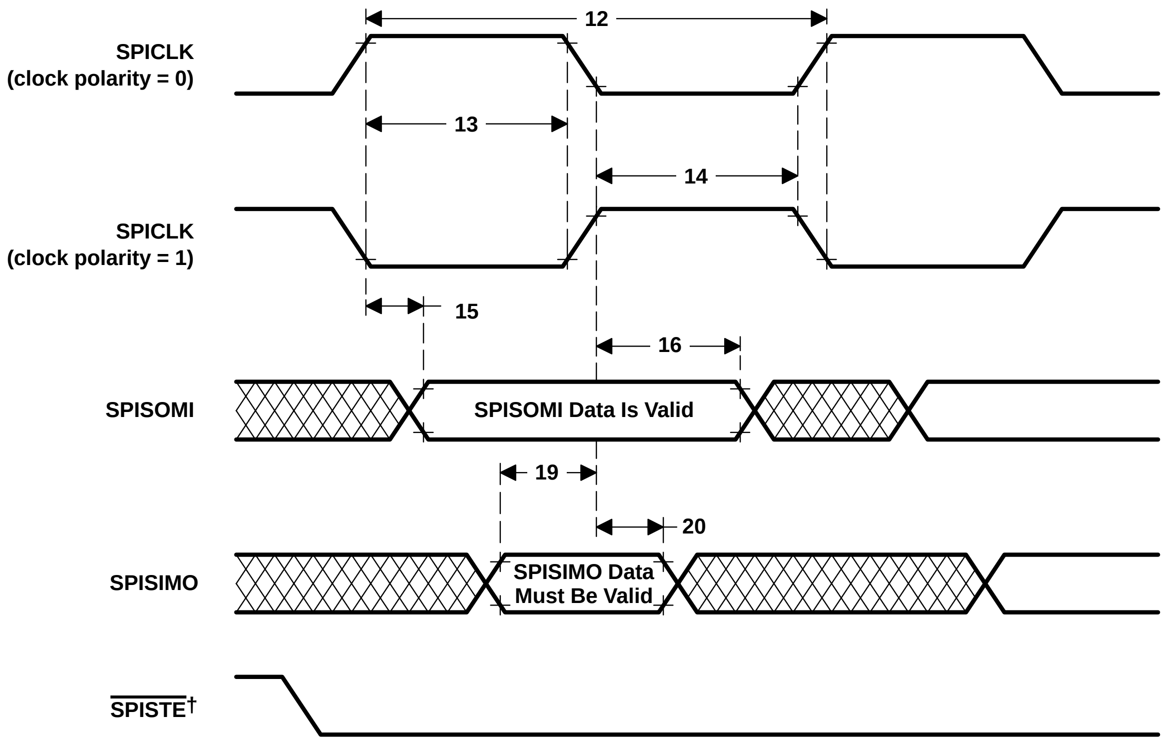

† The SPISTE signal must be active before the SPI communication stream starts; the SPISTE signal must remain active until the SPI communication stream is complete.

Figure 7–21. SPI Slave Mode External Timing (Clock Phase = 0)

Table 7–21. SPI Slave Mode External Timings (Clock Phase = 1)†‡

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$8t_{c(LCO)}$		ns
13§	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S}-10$	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S}-10$	$0.5t_{c(SPC)S}$	
14§	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S}-10$	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S}-10$	$0.5t_{c(SPC)S}$	
17§	$t_{su(SOMI\text{-}SPCH)S}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$0.125t_{c(SPC)S}$		ns
	$t_{su(SOMI\text{-}SPCL)S}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	$0.125t_{c(SPC)S}$		
18§	$t_{v(SPCH\text{-}SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity =0)	$0.75t_{c(SPC)S}$		ns
	$t_{v(SPCL\text{-}SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity =1)	$0.75t_{c(SPC)S}$		
21§	$t_{su(SIMO\text{-}SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	0		ns
	$t_{su(SIMO\text{-}SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	0		
22§	$t_{v(SPCH\text{-}SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S}$		ns
	$t_{v(SPCL\text{-}SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S}$		

† The MASTER/SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is set.

‡ $t_{c(SPC)}$ = SPI clock cycle time = $\frac{LSPCLK}{4}$ or $\frac{LSPCLK}{(SPIBRR + 1)}$

$t_{c(LCO)}$ = LSPCLK cycle time

§ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

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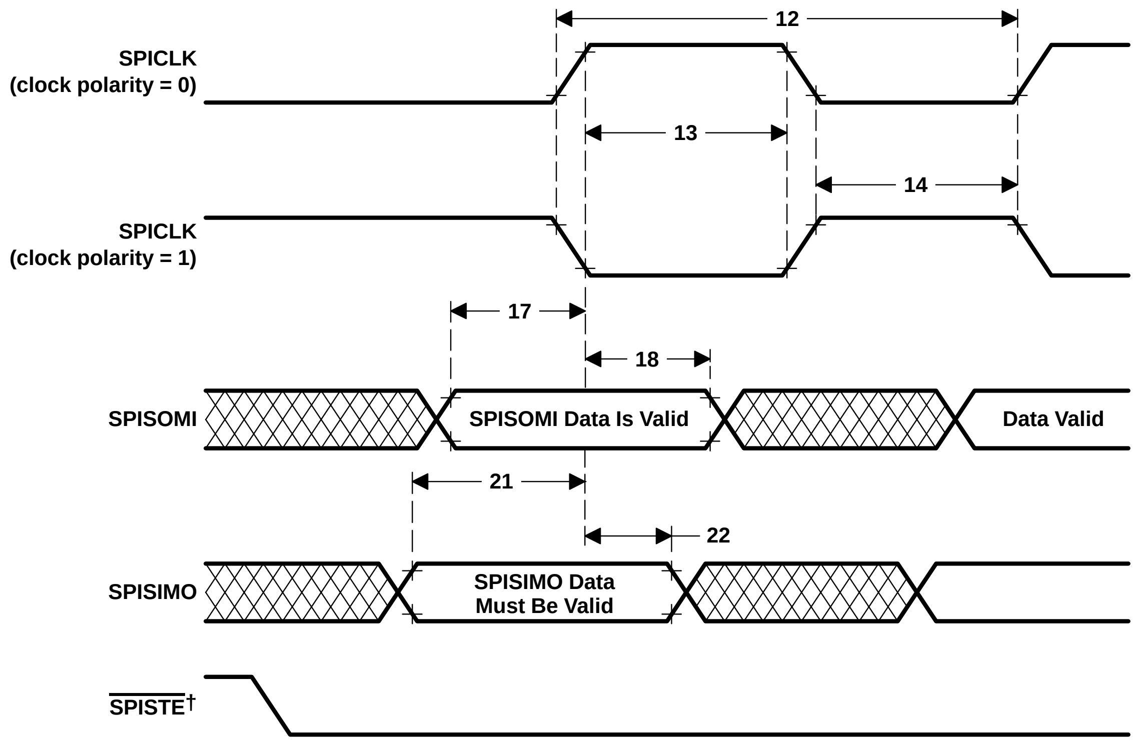

† The SPISTE signal must be active before the SPI communication stream starts; the SPISTE signal must remain active until the SPI communication stream is complete.

Figure 7–22. SPI Slave Mode External Timing (Clock Phase = 1)

7.20 External Interface (XINTF) Timings

Each XINTF access consists of three parts: Lead, Active, and Trail. The user configures the Lead/Active/Trail wait states in the XTIMING registers. There is one XTIMING register for each XINTF zone. Table 7–22 shows the relationship between the parameters configured in the XTIMING register and the duration of the pulse in terms of XTIMCLK cycles.

Table 7–22. Relationship Between Parameters Configured in XTIMING and Duration of Pulse†‡

DESCRIPTION		DURATION (ns)	
		X2TIMING = 0	X2TIMING = 1
LR	Lead period, read access	XRDLEAD x $t_{c(XTIM)}$	(XRDLEAD x 2) x $t_{c(XTIM)}$
AR	Active period, read access	(XRDACTIVE + WS + 1) x $t_{c(XTIM)}$	(XRDACTIVE x 2 + WS + 1) x $t_{c(XTIM)}$
TR	Trail period, read access	XRDTRAIL x $t_{c(XTIM)}$	(XRDTRAIL x 2) x $t_{c(XTIM)}$
LW	Lead period, write access	XWRLEAD x $t_{c(XTIM)}$	(XWRLEAD x 2) x $t_{c(XTIM)}$
AW	Active period, write access	(XWRACTIVE + WS + 1) x $t_{c(XTIM)}$	(XWRACTIVE x 2 + WS + 1) x $t_{c(XTIM)}$
TW	Trail period, write access	XWRTRAIL x $t_{c(XTIM)}$	(XWRTRAIL x 2) x $t_{c(XTIM)}$

† $t_{c(XTIM)}$ – Cycle time, XTIMCLK
‡ WS refers to the number of wait states inserted by hardware when using XREADY. If the zone is configured to ignore XREADY (USEREADY = 0), then WS = 0.

Minimum wait state requirements must be met when configuring each zone's XTIMING register. These requirements are in addition to any timing requirements as specified by that device's data sheet. No internal device hardware is included to detect illegal settings.

- If the XREADY signal is ignored (USEREADY = 0), then:
  1. Lead: $LR \geq t_{c(XTIM)}$
     $LW \geq t_{c(XTIM)}$

  These requirements result in the following XTIMING register configuration restrictions§:

XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
≥ 1	≥ 0	≥ 0	≥ 1	≥ 0	≥ 0	0, 1

§ No hardware to detect illegal XTIMING configurations

Examples of valid and invalid timings when not sampling XREADY§:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid	0	0	0	0	0	0	0, 1
Valid	1	0	0	1	0	0	0, 1

§ No hardware to detect illegal XTIMING configurations

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- If the XREADY signal is sampled in the Synchronous mode (USEREADY = 1, READYMODE = 0), then:
  1. Lead: $LR \geq t_{c(XTIM)}$
     $LW \geq t_{c(XTIM)}$
  2. Active: $AR \geq 2 \times t_{c(XTIM)}$
     $AW \geq 2 \times t_{c(XTIM)}$
     NOTE: Restriction does not include external hardware wait states

  These requirements result in the following XTIMING register configuration restrictions†:

XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
≥ 1	≥ 1	≥ 0	≥ 1	≥ 1	≥ 0	0, 1

† No hardware to detect illegal XTIMING configurations

Examples of valid and invalid timings when using Synchronous XREADY†:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid	0	0	0	0	0	0	0, 1
Invalid	1	0	0	1	0	0	0, 1
Valid	1	1	0	1	1	0	0, 1

† No hardware to detect illegal XTIMING configurations

- If the XREADY signal is sampled in the Asynchronous mode (USEREADY = 1, READYMODE = 1), then:
  1. Lead: $LR \geq t_{c(XTIM)}$
     $LW \geq t_{c(XTIM)}$
  2. Active: $AR \geq 2 \times t_{c(XTIM)}$
     $AW \geq 2 \times t_{c(XTIM)}$
     NOTE: Restriction does not include external hardware wait states
  3. Lead + Active: $LR + AR \geq 4 \times t_{c(XTIM)}$
     $LW + AW \geq 4 \times t_{c(XTIM)}$
     NOTE: Restriction does not include external hardware wait states

  These requirements result in the following XTIMING register configuration restrictions†:

XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
≥ 1	≥ 2	0	≥ 1	≥ 2	0	0, 1

† No hardware to detect illegal XTIMING configurations

or†

XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
≥ 2	≥ 1	0	≥ 2	≥ 1	0	0, 1

† No hardware to detect illegal XTIMING configurations

Examples of valid and invalid timings when using Asynchronous XREADY†:

	XRDLEAD	XRDACTIVE	XRDTRAIL	XWRLEAD	XWRACTIVE	XWRTRAIL	X2TIMING
Invalid	0	0	0	0	0	0	0, 1
Invalid	1	0	0	1	0	0	0, 1
Invalid	1	1	0	1	1	0	0
Valid	1	1	0	1	1	0	1
Valid	1	2	0	1	2	0	0, 1
Valid	2	1	0	2	1	0	0, 1

† No hardware to detect illegal XTIMING configurations

7.20.1 External Interface Read Timings

Table 7–23. External Memory Interface Read Switching Characteristics for XCLKOUT = XTIMCLK†

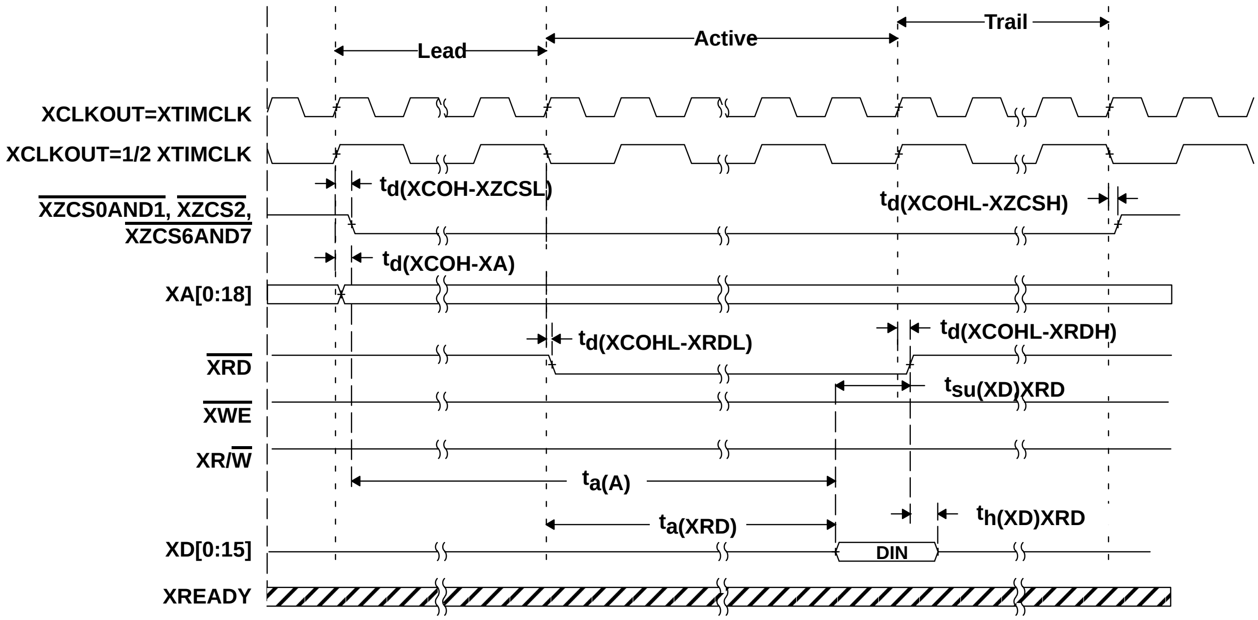
PARAMETER		MIN	MAX	UNIT
$t_{d(XCOH\text{-}XZCSL)}$	Delay time, XCLKOUT high to zone chip-select active low		1	ns
$t_{d(XCOHL\text{-}XZCSH)}$‡	Delay time, XCLKOUT high/low to zone chip-select inactive high	–3	1	ns
$t_{d(XCOH\text{-}XA)}$	Delay time, XCLKOUT high to address valid		2	ns
$t_{d(XCOHL\text{-}XRDL)}$‡	Delay time, XCLKOUT high/low to $\overline{XRD}$ active low		1	ns
$t_{d(XCOHL\text{-}XRDH)}$‡	Delay time, XCLKOUT high/low to $\overline{XRD}$ inactive high	–1	1	ns
$t_{h(XA)XZCSH}$	Hold time, address valid after zone chip-select inactive high	§		ns
$t_{h(XA)XRD}$	Hold time, address valid after $\overline{XRD}$ inactive high	§		ns

† Timings for XCLKOUT = 1/2 XTIMCLK will be included in a future release of the data sheet.
‡ For XCLKOUT = XTIMCLK, strobes will align with the rising edge of XCLKOUT.
§ The XINTF address bus will always hold the last address put out on the bus during inactive cycles. This includes alignment cycles.

Table 7–24. External Memory Interface Read Timing Requirements

		MIN	MAX	UNIT
$t_{a(A)}$	Access time, read data from address valid		(LR + AR) – 14¶	ns
$t_{a(XRD)}$	Access time, read data valid from $\overline{XRD}$ active low		AR – 12¶	ns
$t_{su(XD)XRD}$	Setup time, read data valid before $\overline{XRD}$ strobe inactive high	12		ns
$t_{h(XD)XRD}$	Hold time, read data valid after $\overline{XRD}$ inactive high	0		ns

¶ LR = Lead period, read access. AR = Active period, read access. See Table 7–22.



NOTES: A. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.

B. During alignment cycles, all signals will transition to their inactive state.

C. For USEREADY = 0, the external XREADY input signal is ignored.

D. XAD[0:18] will hold the last address put on the bus during inactive cycles, including alignment cycles.

Figure 7–23. Example Read Access

XTIMING register parameters used for this example:

XRDLEAD	XRDACTIVE	XRDTRAIL	USEREADY	X2TIMING	XWRLEAD	XWRACTIVE	XWRTRAIL	READYMODE
≥1	≥0	≥0	0	0	N/A†	N/A†	N/A†	N/A†

† N/A = “Don’t care” for this example

7.20.2 External Interface Write Timings

Table 7–25. External Memory Interface Write Switching Characteristics for XCLKOUT = XTIMCLK†

PARAMETER		MIN	MAX	UNIT
$t_{d(XCOH-XZCSL)}$	Delay time, XCLKOUT high to zone chip-select active low		1	ns
$t_{d(XCOHL-XZCSH)}$‡	Delay time, XCLKOUT high or low to zone chip-select inactive high	–3	1	ns
$t_{d(XCOH-XA)}$	Delay time, XCLKOUT high to address valid		2	ns
$t_{d(XCOHL-XWEL)}$‡	Delay time, XCLKOUT high/low to $\overline{XWE}$ low		1	ns
$t_{d(XCOHL-XWEH)}$‡	Delay time, XCLKOUT high/low to $\overline{XWE}$ high		1	ns
$t_{d(XCOH-XRNWL)}$	Delay time, XCLKOUT high to XR/$\overline{W}$ low		1	ns
$t_{d(XCOHL-XRNWH)}$‡	Delay time, XCLKOUT high/low to XR/$\overline{W}$ high	–1	1	ns
$t_{en(XD)XWEL}$	Enable time, data bus driven from $\overline{XWE}$ low	0		ns
$t_{d(XWEL-XD)}$	Delay time, data valid after $\overline{XWE}$ active low		4	ns
$t_{h(XA)XZCSH}$	Hold time, address valid after zone chip-select inactive high	§		ns
$t_{h(XD)XWE}$	Hold time, write data valid after $\overline{XWE}$ inactive high	TW¶		ns
$t_{dis(XD)XRNW}$	Data bus disabled after XR/$\overline{W}$ inactive high	4		ns

† Timings for XCLKOUT = 1/2 XTIMCLK will be included in a future release of the data sheet.
‡ For XCLKOUT = XTIMCLK, strobes will align with the rising edge of XCLKOUT.
§ The XINTF address bus will always hold the last address put out on the bus during inactive cycles. This includes alignment cycles.
¶ TW = Trail period, write access. See Table 7–22.

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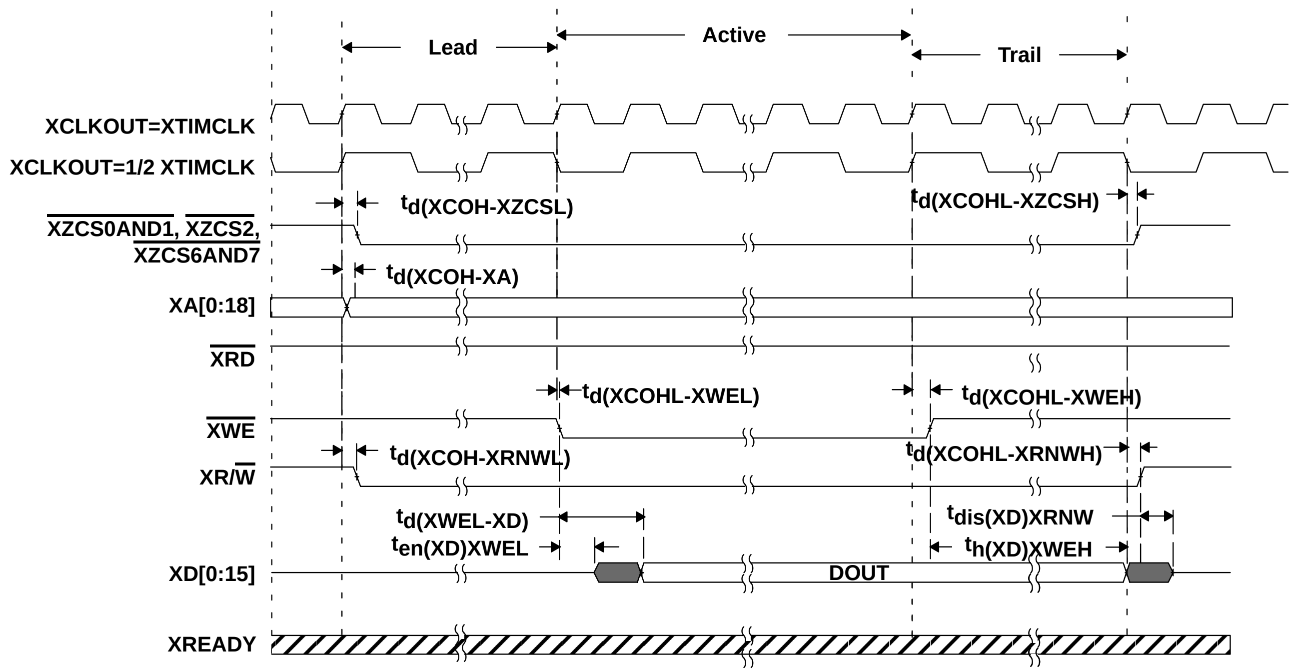

NOTES: A. All XINTF accesses (lead period) begin on the rising edge of XCLKOUT. When necessary, the device will insert an alignment cycle before an access to meet this requirement.
B. During alignment cycles, all signals will transition to their inactive state.
C. For USEREADY = 0, the external XREADY input signal is ignored.
D. XAD[0:18] will hold the last address put on the bus during inactive cycles, including alignment cycles.

Figure 7–24. Example Write Access

XTIMING register parameters used for this example:

XRDLEAD	XRDACTIVE	XRDTRAIL	USEREADY	X2TIMING	XWRLEAD	XWRACTIVE	XWRTRAIL	READYMODE
N/A†	N/A†	N/A†	0	0	≥1	≥0	≥0	N/A†

† N/A = “Don’t care” for this example

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7.20.3 $\overline{\text{XHOLD}}$ and $\overline{\text{XHOLDA}}$

If the HOLD mode bit is set while $\overline{\text{XHOLD}}$ and $\overline{\text{XHOLDA}}$ are both low (external bus accesses granted), the $\overline{\text{XHOLDA}}$ signal is forced high (at the end of the current cycle) and the external interface is taken out of high-impedance mode.

On a reset ($\overline{\text{XRS}}$), the HOLD mode bit is set to 0. If the $\overline{\text{XHOLD}}$ signal is active low on a system reset, the bus and all signal strobes must be in high-impedance mode, and the $\overline{\text{XHOLDA}}$ signal is also driven active low.

When HOLD mode is enabled and $\overline{\text{XHOLDA}}$ is active low (external bus grant active), the CPU can still execute code from internal memory. If an access is made to the external interface, the CPU is stalled until the $\overline{\text{XHOLD}}$ signal is removed.

An external DMA request, when granted, places the following signals in a high-impedance mode:

XA[18:0]	$\overline{\text{XZCS0AND1}}$
XD[15:0]	$\overline{\text{XZCS2}}$
$\overline{\text{XWE}}$, $\overline{\text{XRD}}$	$\overline{\text{XZCS6AND7}}$
XR/$\overline{\text{W}}$	

All other signals not listed in this group remain in their default or functional operational modes during these signal events. Detailed timing diagram will be released in a future revision of this data sheet.

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7.21 On-Chip Analog-to-Digital Converter

This section describes the on-chip analog-to-digital converter (ADC) and provides the absolute maximum ratings and the recommended operating conditions.

7.21.1 Absolute Maximum Ratings

Unless otherwise noted, the list of absolute maximum ratings are specified over operating conditions. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Supply voltage range, V_{SSA1}/V_{SSA2} to $V_{DDA1}/V_{DDA2}/AV_{DDREFBG}$ . . . . –0.3 V to 4.6 V
V_{SS1} to V_{DD1} . . . . –0.3 V to 2.5 V
Analog input voltage range (ADCINx to ADCLO) . . . . AGND – 0.3 V to 3.3 V†

† All analog inputs do not have diode clamp protection.

7.21.2 Electrical Characteristics Over Recommended Operating Conditions

Table 7–26. DC Specifications‡

PARAMETER	MIN	TYP	MAX	UNIT
Resolution	12			Bits
ADC clock	1			kHz
			25§	MHz
Accuracy				
INL (Integral nonlinearity)			±1.5	LSB
DNL (Differential nonlinearity)			±1	LSB
Offset error		±40	±80	LSB¶
Overall gain error with internal reference#		120	200	LSB
Analog input				
Analog input voltage (ADCINx to ADCLO)	0		3	V
ADCLO	–5	0	5	mV
Input capacitance		10		pF
Input leakage current		3	±5	µA
Internal voltage reference#				
Accuracy, $ADCV_{REFP}$	1.9	2	2.10	V
Accuracy, $ADCV_{REFM}$	0.95	1	1.05	V
Input voltage difference, ADCREFP – ADCREFM	0.95	1	1.05	V
Temperature coefficient		50		PPM/°C
Reference noise		100		µV

‡ Tested at 12.5-MHz ADCCLK
§ If SYSCLKOUT ≤ 25 MHz, ADC clock ≤ SYSCLKOUT/2
¶ 1 LSB has the weighted value of 3.0/4096 = 0.732 mV.
# A single internal band gap reference (±5% accuracy) sources both ADCREFP and ADCREFM signals, and hence, these voltages track together. The ADC converter uses the difference between these two as its reference.
The total gain error will be the combination of the gain error shown here and the voltage reference accuracy (ADCREFP – ADCREFM). A software-based calibration procedure is recommended for better accuracy.

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Table 7–27. AC Specifications† (PRELIMINARY DATA)

PARAMETER		MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise ratio + distortion		64		dB
SNR	Signal-to-noise ratio		68		dB
THD	Total harmonic distortion		–68		dB
ENOB (SNR)	Effective number of bits		10.4		Bits
SFDR	Spurious free dynamic range		69		dB

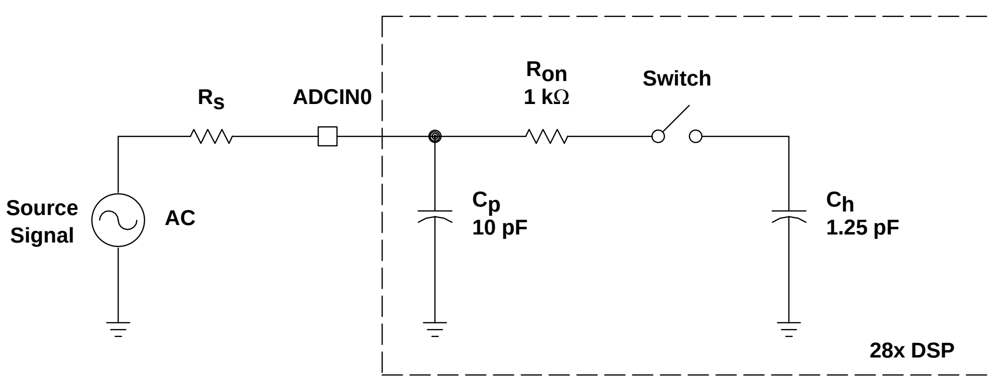
† These numbers are design estimates. Final numbers will be available after device attains “TMS” status.

7.21.3 Current Consumption for Different ADC Configurations (at 25-MHz ADCCLK)‡

I_{DDA} (TYP)§	I_{DDAIO} (TYP)	I_{DD1} (TYP)	ADC OPERATING MODE/CONDITIONS
40 mA	1 µA	0.5 mA	Mode A (Operational Mode): – BG and REF enabled – PWD disabled
7 mA	0	5 µA	Mode B: – ADC clock enabled – BG and REF enabled – PWD enabled
1 µA	0	5 µA	Mode C: – ADC clock enabled – BG and REF disabled – PWD enabled
1 µA	0	0	Mode D: – ADC clock disabled – BG and REF disabled – PWD enabled

‡ Test Conditions: SYSCLKOUT = 150 MHz
ADC module clock = 25 MHz
ADC performing a continuous conversion of all 16 channels in Mode A

§ I_{DDA} – includes current into V_{DDA1} / V_{DDA2} and $AV_{DDREFBG}$



Typical Values of the Input Circuit Components:

Switch Resistance (R_{on}): 1 kΩ
Sampling Capacitor (C_h): 1.25 pF
Parasitic Capacitance (C_p): 10 pF
Source Resistance (R_s): 50 Ω

Figure 7–25. ADC Analog Input Impedance Model

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7.21.4 ADC Power-Up Control Bit Timing

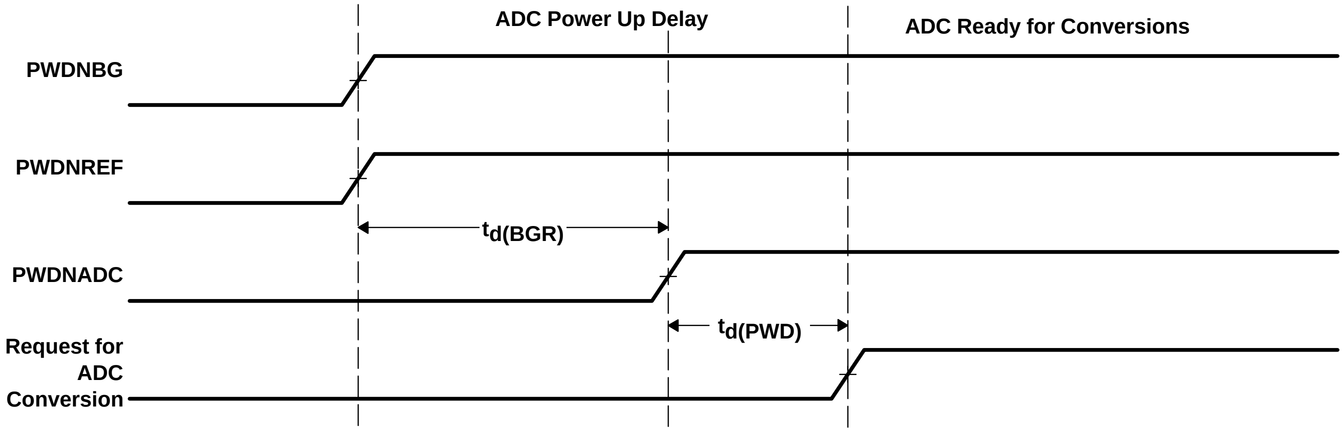

Figure 7–26. ADC Power-Up Control Bit Timing

Table 7–28. ADC Power-Up Delays†

		MIN	TYP	MAX	UNIT
$t_{d(BGR)}$	Delay time for band gap reference to be stable. Bits 6 and 5 of the ADCTRL3 register (PWDNBG and PWDNREF) are to be set to 1 before the PWDNADC bit is enabled.	7	8	10	ms
$t_{d(PWD)}$	Delay time for power-down control to be stable. Bit 7 of the ADCTRL3 register (PWDNADC) is to be set to 1 before any ADC conversions are initiated.	20	50		µs
				1	ms

† These delays are necessary and recommended to make the ADC analog reference circuit stable before conversions are initiated. If conversions are started without these delays, the ADC results will show a higher gain. For power down, all three bits can be cleared at the same time.

7.21.5 Detailed Description

7.21.5.1 Reference Voltage

The on-chip ADC has a built-in reference, which provides the reference voltages for the ADC. ADCVREFP is set to 2.0 V and ADCVREFM is set to 1.0 V.

7.21.5.2 Analog Inputs

The on-chip ADC consists of 16 analog inputs, which are sampled either one at a time or two channels at a time. These inputs are software-selectable.

7.21.5.3 Converter

The on-chip ADC uses a 12-bit four-stage pipeline architecture, which achieves a high sample rate with low power consumption.

7.21.5.4 Conversion Modes

The conversion can be performed in two different conversion modes:

- Sequential sampling mode (SMODE = 0)
- Simultaneous sampling mode (SMODE = 1)

7.21.6 Sequential Sampling Mode (Single-Channel) (SMODE = 0)

In sequential sampling mode, the ADC can continuously convert input signals on any of the channels (Ax to Bx). The ADC can start conversions on event triggers from the Event Managers (EVA/EVB), software trigger, or from an external ADCSOC signal. If the SMODE bit is 0, the ADC will do conversions on the selected channel on every Sample/Hold pulse. The conversion time and latency of the Result register update are explained below. The ADC interrupt flags are set a few SYSCLKOUT cycles after the Result register update. The selected channels will be sampled at every falling edge of the Sample/Hold pulse. The Sample/Hold pulse width can be programmed to be 1 ADC clock wide (minimum) or 16 ADC clocks wide (maximum).

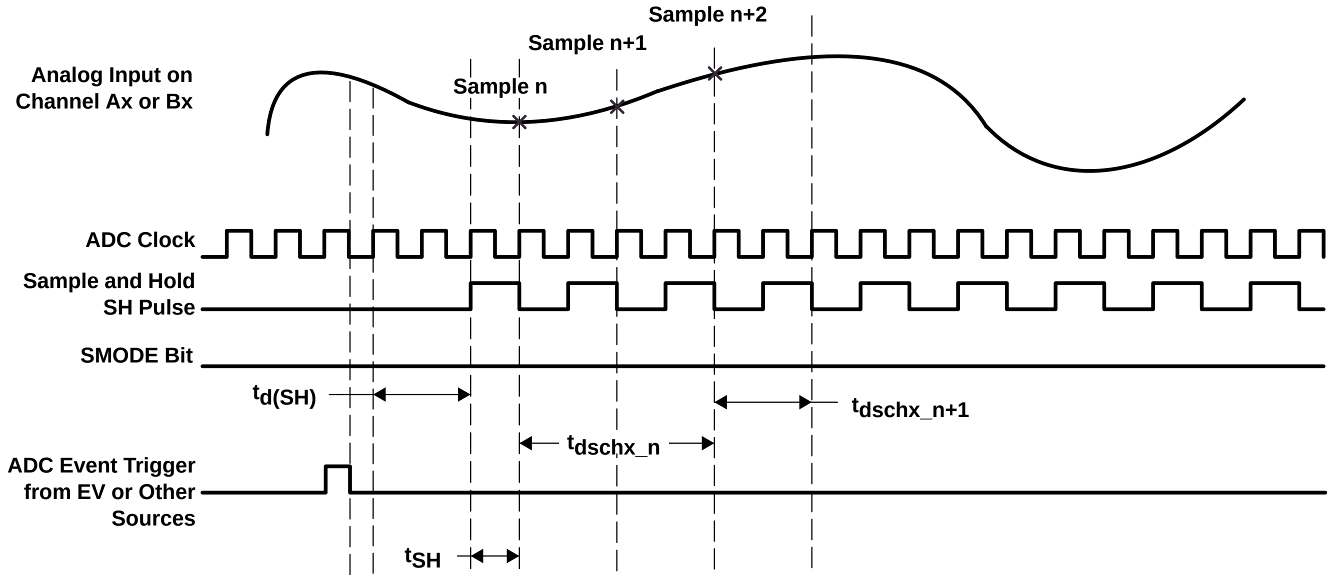

Figure 7–27. Sequential Sampling Mode (Single-Channel) Timings

Table 7–29. Sequential Sampling Mode Timings

		SAMPLE n	SAMPLE n + 1	AT 25-MHz ADC CLOCK, $t_{c(ADCCLK)}$ = 40 ns	REMARKS
$t_{d(SH)}$	Delay time from event trigger to sampling	$2.5t_{c(ADCCLK)}$			
t_{SH}	Sample/Hold width/ Acquisition width	(1 + Acqps) * $t_{c(ADCCLK)}$		40 ns with Acqps = 0	Acqps value = 0–15 ADCCTRL1[8:11]
$t_{d(schx\_n)}$	Delay time for first result to appear in the Result register	$4t_{c(ADCCLK)}$		160 ns	
$t_{d(schx\_n+1)}$	Delay time for successive results to appear in the Result register		(2 + Acqps) * $t_{c(ADCCLK)}$	80 ns	

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7.21.7 Simultaneous Sampling Mode (Dual-Channel) (SMODE = 1)

In simultaneous mode, the ADC can continuously convert input signals on any one pair of channels (A0/B0 to A7/B7). The ADC can start conversions on event triggers from the Event Managers (EVA/EVB), software trigger, or from an external ADCSOC signal. If the SMODE bit is 1, the ADC will do conversions on two selected channels on every Sample/Hold pulse. The conversion time and latency of the Result register update are explained below. The ADC interrupt flags are set a few SYSCLKOUT cycles after the Result register update.The selected channels will be sampled simultaneously at the falling edge of the Sample/Hold pulse. The Sample/Hold pulse width can be programmed to be 1 ADC clock wide (minimum) or 16 ADC clocks wide (maximum).

NOTE: In Simultaneous mode, the ADCIN channel pair select has to be A0/B0, A1/B1, ..., A7/B7, and *not* in other combinations (such as A1/B3, etc.).

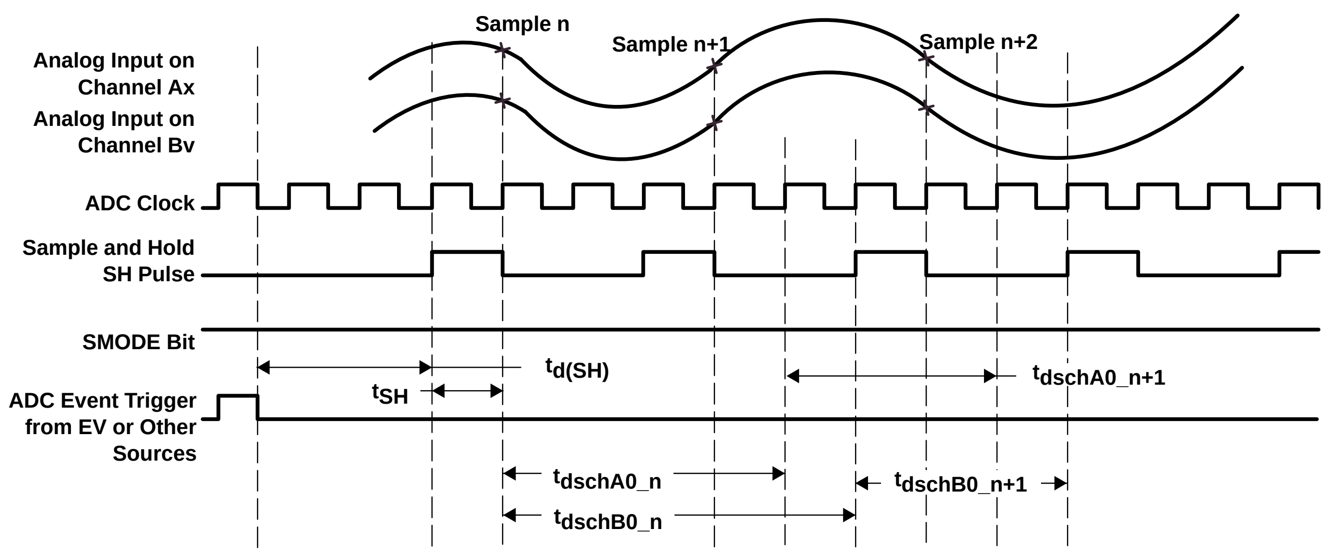

Figure 7–28. Simultaneous Sampling Mode Timings

Table 7–30. Simultaneous Sampling Mode Timings

		SAMPLE n	SAMPLE n + 1	AT 25-MHz ADC CLOCK, $t_{c(ADCCLK)}$ = 40 ns	REMARKS
$t_{d(SH)}$	Delay time from event trigger to sampling	$2.5t_{c(ADCCLK)}$			
t_{SH}	Sample/Hold width/ Acquisition Width	(1 + Acqps) * $t_{c(ADCCLK)}$		40 ns with Acqps = 0	Acqps value = 0–15 ADCCTRL1[8:11]
$t_{d(schA0\_n)}$	Delay time for first result to appear in Result register	$4t_{c(ADCCLK)}$		160 ns	
$t_{d(schB0\_n)}$	Delay time for first result to appear in Result register	$5t_{c(ADCCLK)}$		200 ns	
$t_{d(schA0\_n+1)}$	Delay time for successive results to appear in Result register		(3 + Acqps) * $t_{c(ADCCLK)}$	120 ns	
$t_{d(schB0\_n+1)}$	Delay time for successive results to appear in Result register		(3 + Acqps) * $t_{c(ADCCLK)}$	120 ns	

7.21.8 Definitions of Specifications and Terminology

Integral Nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

Differential Nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

Zero Offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-Noise Ratio + Distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = \frac{(\text{SINAD} - 1.76)}{6.02}$$

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Spurious Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

7.22 Multichannel Buffered Serial Port (McBSP) Timings

7.22.1 McBSP Transmit and Receive Timings

Table 7–31. McBSP Timing Requirements†‡

NO.				MIN	MAX	UNIT
		McBSP module clock (CLKG, CLKX, CLKR) range		1		kHz
					20§	MHz
		McBSP module cycle time (CLKG, CLKX, CLKR) range		50		ns
					1	ms
M11	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P		ns
M12	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P–7		ns
M13	$t_{r(CKRX)}$	Rise time, CLKR/X	CLKR/X ext		7	ns
M14	$t_{f(CKRX)}$	Fall time, CLKR/X	CLKR/X ext		7	ns
M15	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	18		ns
			CLKR ext	2		
M16	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	0		ns
			CLKR ext	6		
M17	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	18		ns
			CLKR ext	2		
M18	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	0		ns
			CLKR ext	6		
M19	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	18		ns
			CLKX ext	2		
M20	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	0		ns
			CLKX ext	6		

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ 2P = 1/CLKG in ns. CLKG is the output of sample rate generator mux. $\text{CLKG} = \frac{\text{CLKSRG}}{(1 + \text{CLKGDV})}$. CLKSRG can be LSPCLK, CLKX, CLKR as source CLKSRG ≤ (SYSCLKOUT/2). McBSP performance is limited by I/O buffer switching speed.

§ Internal clock prescalars have to be adjusted such that the McBSP clock (CLKG, CLKX, CLKR) speeds are not greater than the I/O buffer speed limit (20 MHz).

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Table 7–32. McBSP Switching Characteristics[†‡]

NO.	PARAMETER				MIN	MAX	UNIT
M1	$t_{c(CKRX)}$	Cycle time, CLKR/X		CLKR/X int	2P		ns
M2	$t_{w(CKRXH)}$	Pulse duration, CLKR/X high		CLKR/X int	D–5[§]	D+5[§]	ns
M3	$t_{w(CKRXL)}$	Pulse duration, CLKR/X low		CLKR/X int	C–5[§]	C+5[§]	ns
M4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid		CLKR int	0	4	ns
				CLKR ext	3	27	ns
M5	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid		CLKX int	0	4	ns
				CLKX ext	3	27	
M6	$t_{dis(CKXH-DXHZ)}$	Disable time, CLKX high to DX high impedance following last data bit		CLKX int		8	ns
				CLKX ext		14	
M7	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted.		CLKX int		9	ns
				CLKX ext		28	
		Delay time, CLKX high to DX valid	DXENA = 0	CLKX int		8	
				CLKX ext		14	
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int		P + 8	
				CLKX ext		P + 14	
M8	$t_{en(CKXH-DX)}$	Enable time, CLKX high to DX driven	DXENA = 0	CLKX int	0		ns
				CLKX ext	6		
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int	P		
				CLKX ext	P + 6		
M9	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid	DXENA = 0	FSX int		8	ns
				FSX ext		14	
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode.	DXENA = 1	FSX int		P + 8	
				FSX ext		P + 14	
M10	$t_{en(FXH-DX)}$	Enable time, FSX high to DX driven	DXENA = 0	FSX int	0		ns
				FSX ext	6		
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode	DXENA = 1	FSX int	P		
				FSX ext	P + 6		

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
‡ 2P = 1/CLKG in ns.
§ T=CLKRX period = (1 + CLKGDV) * P
C=CLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D=CLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even

ADVANCE INFORMATION

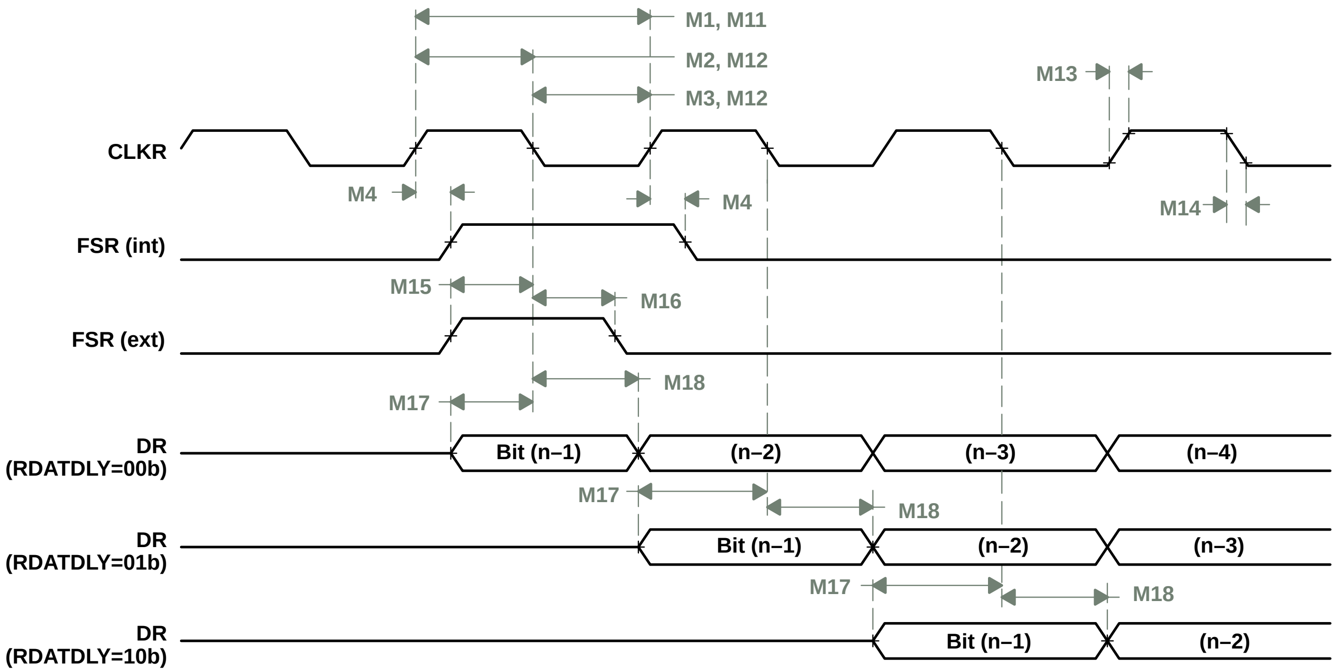


Figure 7–29. McBSP Receive Timings

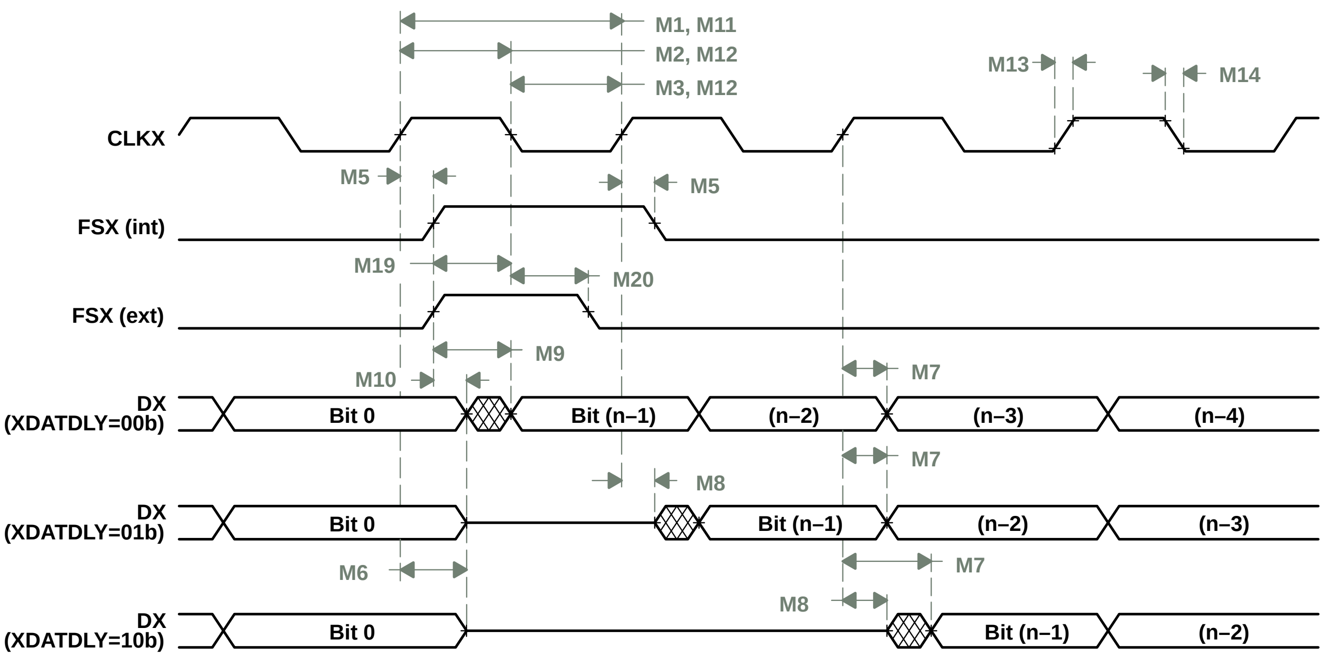


Figure 7–30. McBSP Transmit Timings

7.23 Flash Timings

7.23.1 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
N_f	Flash endurance for the array (Write/erase cycles)	0°C to 85°C	100	1000		cycles
N_{OTP}	OTP endurance for the array (Write cycles)	0°C to 85°C			1	write

Table 7–33. Flash/OTP Access Timings

PARAMETER		MIN	TYP	MAX	UNIT
$t_{a(fp)}$	Paged Flash access time	36			ns
$t_{a(fr)}$	Random Flash access time	36			ns

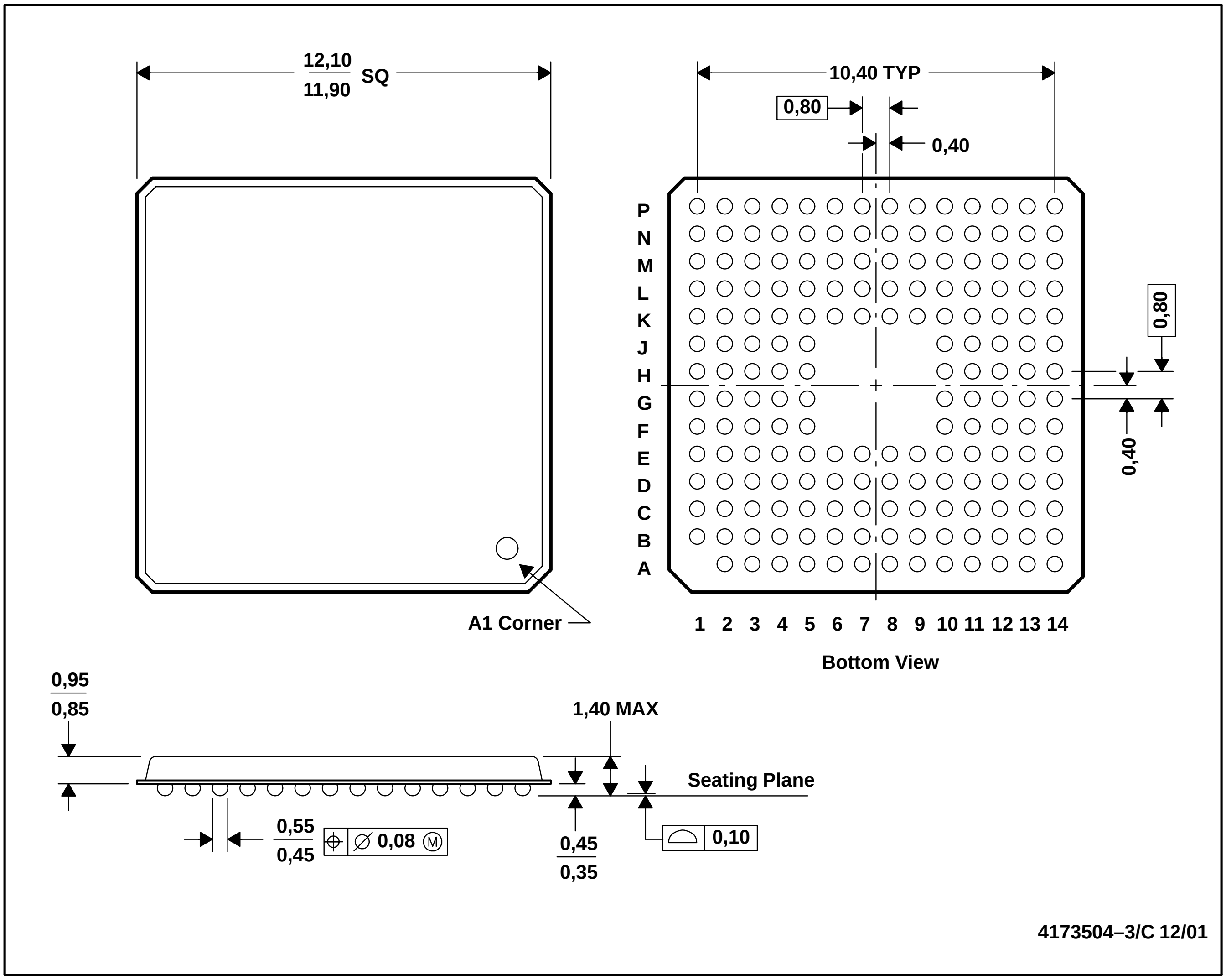
NOTE: For 150 MHz, PAGE WS = 5 and RANDOM WS = 5
For 135 MHz, PAGE WS = 4 and RANDOM WS = 4

ADVANCE INFORMATION

8 Mechanical Data

8.1 Ball Grid Array (BGA)

GHH (S-PBGA-N179) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice
C. MicroStar BGA configuration.

Figure 8–1. TMS320F2812 179-Ball GHH MicroStar BGA™

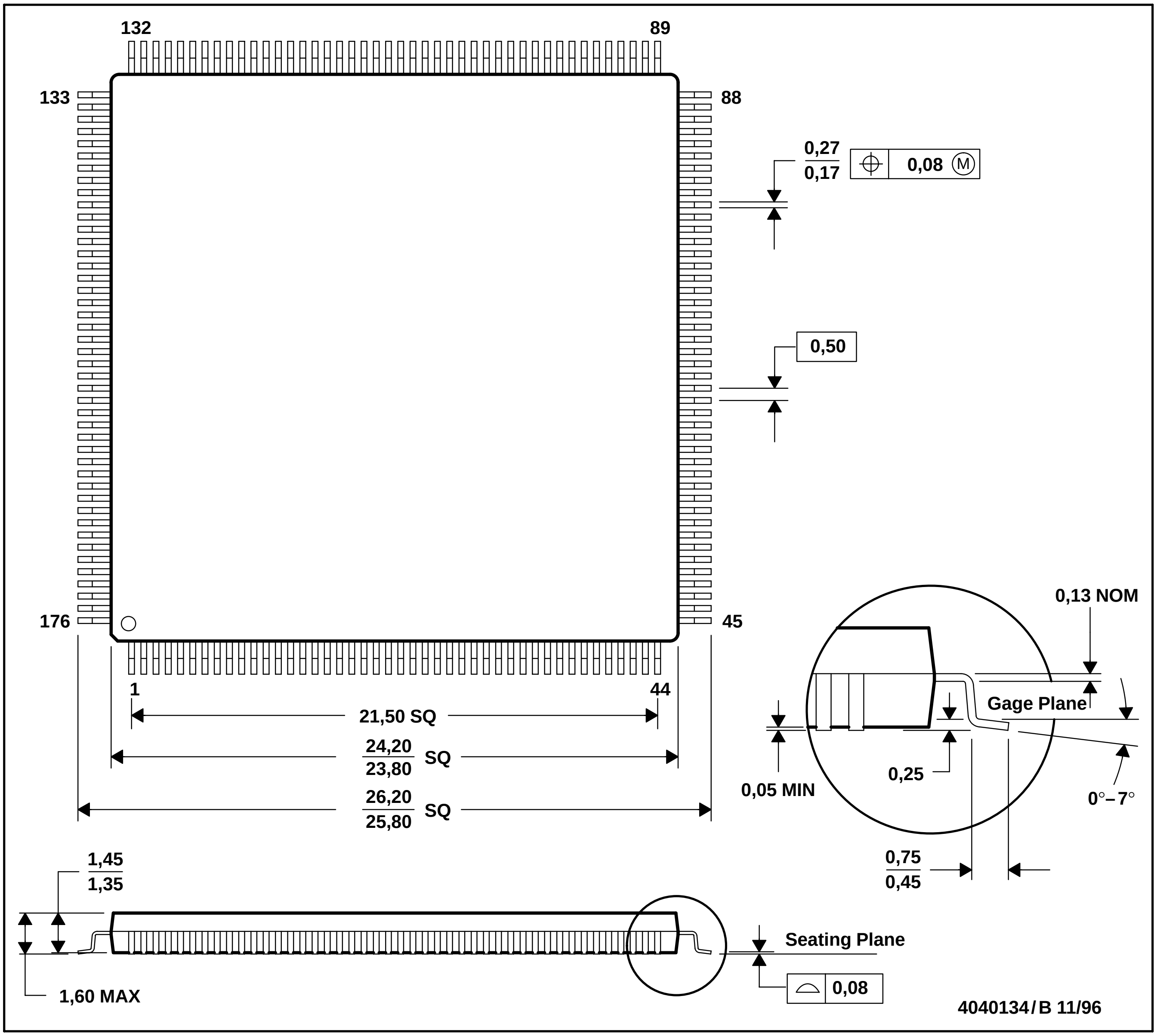
Table 8–1. Thermal Resistance Characteristics for 179-GHH

PARAMETER	179-GHH PACKAGE	UNIT
Psi_{JT}	0.658	°C/W
Θ_{JA}	42.57	°C/W
Θ_{JC}	16.08	°C/W

MicroStar BGA is a trademark of Texas Instruments.

8.2 Low-Profile Quad Flatpacks (LQFPs)

PGF (S-PQFP-G176) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

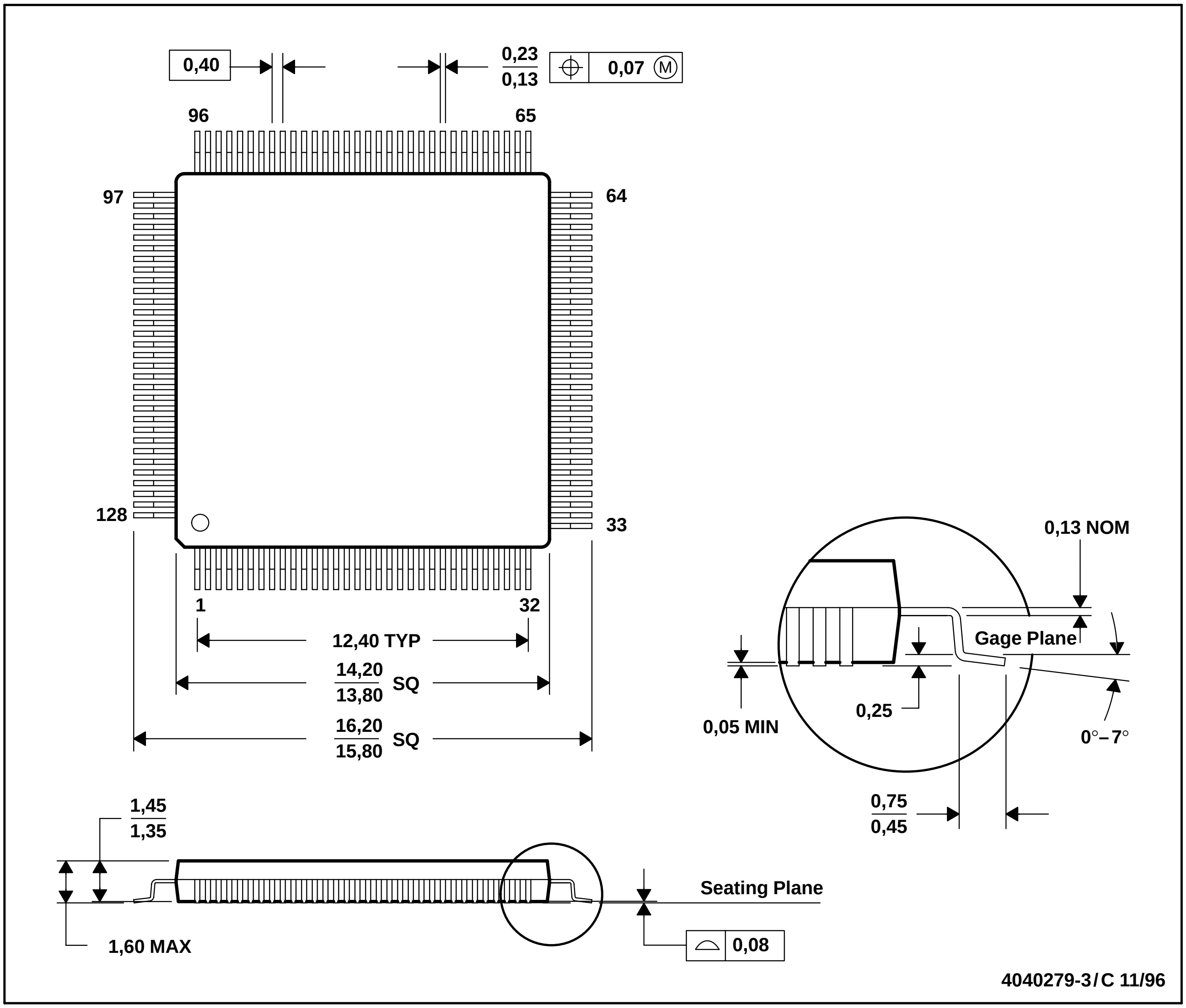
Figure 8–2. TMS320F2812 176-Pin PGF LQFP

Table 8–2. Thermal Resistance Characteristics for 176-PGF

PARAMETER	176-PGF PACKAGE	UNIT
Psi_{JT}	0.247	°C/W
Θ_{JA}	41.88	°C/W
Θ_{JC}	9.73	°C/W

ADVANCE INFORMATION

PBK (S-PQFP-G128) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Figure 8–3. TMS320F2810 128-Pin PBK LQFP

Table 8–3. Thermal Resistance Characteristics for 128-PBK

PARAMETER	128-PBK PACKAGE	UNIT
Psi_{JT}	0.271	°C/W
Θ_{JA}	41.65	°C/W
Θ_{JC}	10.76	°C/W

ADVANCE INFORMATION