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# CDMS Analog Feedback FPGA/CPLD Register Map (Rev. C.1)

### **0x00: Present Phonon pointer value upper bits**

If SDRam writes are enabled, this register contains the upper six bits of the phonon pointer captured at the time of the read at this address. If SDRam writes are disabled the pointer is held at 0

### **0x01: Present Phonon pointer value lower bits**

If SDRam writes are enabled, this register contains the lower 16 bits of the phonon pointer captured at the time of the read at address 0. If SDRam writes are disabled the pointer is held at 0

### **0x02: SDRam Read address upper bits**

A write to this address defines bits the upper 9 bits of the SDRam read address

### **0x03: SDRam Read address lower bits**

A write to this address defines bits the lower 16 bits of the SDRam read address. At the end of this write cycle, the FIFO attached to the SDRAM read data is reset, the specified address is applied to the SDRam and a burst read into the spooling FIFO is started.

### **0x04: Phonon A read address upper bits**

A write to this address defines bits the upper six bits of the SDRam read address within the Phonon A sector. The idea is that the address value stored in the trigger fifo can be written into the following six sets of addresses without the need to account for the sector offsets corresponding to the six ADC data streams.

### **0x05: Phonon A read address lower bits**

A write to this address defines bits the lower 16 bits of the SDRam read address within the Phonon A sector.

### **0x06: Phonon B read address upper bits**

### **0x07: Phonon B read address lower bits**

### **0x08: Phonon C read address upper bits**

### **0x09: Phonon C read address lower bits**

### **0x0A: Phonon D read address upper bits**

### **0x0B: Phonon D read address lower bits**

### **0x0C: Charge inner read address upper bits**

A write to this address defines bits the upper seven bits of the SDRam read address within the Charge Inner sector. The offset value is shifted left one place before being applied to the SDRam to account for the factor of two higher data rate for the charge ADCs

### **0x0D: Charge inner read address lower bits**

A write to this address defines bits the lower 16 bits of the SDRam read address within the Charge Inner sector.

### **0x0E: Charge outer read address upper bits**

### **0x0F: Charge outer read address lower bits**

### **0x10: Trigger FIFO upper bits**

A read from this address returns the trigger status bits and the upper bits of the value of phonon write pointer at the time the trigger requirements were satisfied. The bits are defined as follows:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 15:14 | 13..12 | 11..8 | 6..7 | 5:0 |
| 0 | Charge Trigger bits | Phonon Trigger bits | 0 | Phonon Pointer upper bits |

### **0x11: Trigger FIFO lower bits**

A read from this address returns lower 16 bits of the value of phonon write pointer at the time the trigger requirements were satisfied. In response to this read, a read request is issued to the trigger FIFO making the next trigger word available for reading.

### **0x12: Test Counter upper bits – NOW LEMO MESSAGE.**

~~A 32 bit diagnostic counter is provided as an aid for checking Ethernet transactions.~~

~~This is a 16 bit read/write register. Writing to this address sets the upper 16 bits of a 32 bit counter. Reads return the present value of the counter upper bits.~~

### **0x13: Test Counter lower bits – TEST COUNTER MOVED TO 5E,5F**

~~This is a 16 bit read/write register. Writing to this address set the lower 16 bits of a 32 bit counter. Reads return the value of the counter lower bits, then increment the count.~~

### **0x14: SDRam data port**

This provides SDRam data to the microcontroller from the output of the spooling FIFO. The significance of the data depends on the read address.

### **0x15: Control and status register**

Bits 0: Set the data direction (transmit or receive) of the 4 channel LVDS bus. A “0” sets the direction to receive, a “1” to transmit. Setting this to “1” makes the card a bus master,

a “0” makes the card a slave, if the PLL reference is set to LVDS.

Bit 1: Not yet assigned.

Bit 2: Swaps the upper and lower bytes of SDRAM data if set to “1”.

Bits 4:3 determine which reference is used to lock the VXO frequency. 00: no external reference, the VXO tuning voltage is set to the middle of its range. 01: the reference in the external frequency LEMO connector. 10: the reference is bit 0 of the LVDS bus. 11: not defined. If the 50 MHz crystal is enabled, then the reference is set to the Setup Return line from the CPLD which is 12.5MHz. This synchronizes the 40MHz VXO at the FPGA to the 50MHz oscillator used as the clock source for the DDS synthesizer.

Bit 5: This bit enables SDRam writes of ADC data.

Bit 6 Enable averaging of ADC data

Bit 7 : Trigger FIFO empty flag

Bit 8: Trigger FIFO full flag

Bit 9: CPLD serial command buffer empty

Bit 10: CPLD serial command buffer full

Bit 11: Enable writing of DDS phase data

Bit 12: Trigger Source 0: Threshold logic. 1: Inflection of the test signal

Bit 13: Set Charge ADC reset 1: Reset On, 0: Reset Off

Bit 14: Global clear of all the buffers and flags associated with the LVDS bus

Bit 15: Clear trigger scalers

Setting location 0x15 to 0x20 should put it in a mode to transmit the console output to the LEMO. Gets reset each start of run which is mildly inconvenient.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4:3 | 2 | 1 | 0 |
| Clear Trigger Scalers | Link  Buffer  Reset | Charge ADC Reset | Enable Test Signal Trigger | Enable Phase data writes | CPLD Link Buffer full | CPLD Link Buffer empty | Trig FIFO full | Trig FIFO empty | Enable  Average by 64 | Memory write enable | PLL Reference Source | Byte Swap Enable | Not Used | LVDS bus direction control |

### **0x16: not yet defined** (reserved for programmable averaging interval)

### **0x17:** Trigger Parameter register

This register defines which channels contribute to a trigger

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 15:7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Not Used | LEMO Trig Enable | Charge Outer  Trigger Enable | Charge Inner  Trigger Enable | Phonon D  Trigger Enable | Phonon C  Trigger Enable | Phonon B  Trigger Enable | Phonon A  Trigger Enable |

### **0x18: Trigger Baseline length register**

This register sets the length of the baseline sample interval defined in terms of ADC samples.

|  |  |  |  |
| --- | --- | --- | --- |
| 15 | 14:8 | 7 | 6:0 |
| Not Used | Charge trigger baseline length | Not Used | Phonon trigger baseline length |

### **0x19: Trigger sample length register**

This register sets the length of the baseline sample interval defined in terms of ADC samples.

|  |  |  |  |
| --- | --- | --- | --- |
| 15:13 | 12:8 | 7:5 | 4:0 |
| Not Used | Charge trigger sample length | Not Used | Phonon trigger sample length |

### **0x1A: Phonon A trigger threshold**

This register defines the trigger threshold for Phonon A in terms of ADC counts. The register is a 14 bit signed number, signed extended to 16 bits, since the polarity of the phonon signal is reversible.

### **0x1B: Phonon B trigger threshold**

### **0x1C: Phonon C trigger threshold**

### **0x1D: Phonon D trigger threshold**

### **0x1E: Charge Inner trigger threshold**

This register defines the trigger threshold for Charge Inner in terms of ADC counts. The register is a 15 bit unsigned number, since the polarity of the charge signal is (while biased appropriately) fixed.

### **0x1F: Charge Outer trigger threshold**

Each of the following 16 bit counters are attached to the appropriate trigger threshold comparator.

### **0x20: Phonon A trigger counter**

### **0x21: Phonon B trigger counter**

### **0x22: Phonon B trigger counter**

### **0x23: Phonon D trigger counter**

### **0x24: Charge Inner trigger counter**

### **0x25: Charge Outer trigger counter**

### **0x26: LED Pulser ADC data**

A write to this address sends commands to the LED pulser voltage ADC. A read from this address presents the most recently converted data. There is a one command latency. There will be no readable data until after the second command has been sent. For command details, see the AD7922 ADC data sheet.

### **0x27: LED Pulser width**

This is a 10 bit wide register that defines LED flasher pulse width a least count of 10us.

### **0x28: LED Pulser repetition rate**

This 16 bit register sets the repetition rate of the LED flasher in units of 20us

### **0x29: Trigger FIFO used words/Link Daisy Chain Transmit 0**

Read: This 8 bit register contains the number of triggers stored at the time of the read. It has a span of 0 to 0x80, where 0x80 indicates FIFO full.

### **0x2A: Link Daisy Chain Port 0**

This is an 8 bit port used to send and receive ascii data

### **0x2B: Link Daisy Chain Port 1**

This is an 16 bit port used to send and receive binary data

### **0x2C: Link Bus Port 0**

This is an 8 bit port used to receive ascii data. Synchronous control messages are sent on Bus Port 1 and go directly to FPGA logic and not to a receive FIFO.

### **0x2D: Link Interrupt Register**

|  |  |  |  |
| --- | --- | --- | --- |
| 15:3 | 2 | 1 | 0 |
| Not Used | Init Received Bus 1 | “CR” Received on Bus 0 | Null Char Received on  Daisy Chain 0 |

### **0x2E: Link Status Register**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 7:8 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Daisy Chain Tx 1  Empty | Daisy Chain Tx 0  Empty | Daisy Chain Rx 1  Full | Daisy Chain Rx 0  Full | Daisy Chain Rx 1  Empty | Daisy Chain Rx 0  Empty | Bus Rx 0  Empty | Not Used | Link Transmit Enable | Far Link Port Activity | Link Bus Terminator Enabled | Daisy Chain 1  Parity Error | Daisy Chain 0  Parity Error | Bus Rx 1  Parity Error | Bus Rx 0  Parity Error |

### **0x30: LED Pulser control bits**

This defines the operating mode of the LED flasher. The FET heat enable is tacked on to this register.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15:12 | 11 | 10 | 9 | 8 | 7:5 | 4 | 3 | 2 | 1 | 0 |
| Not Used | Enable 15V  power | Not Used | Enable  Zap Charging | FET heat enable | Not Used | Single step / free run | Not Used | Connect LED Voltages to Phonon ADCs | Enable LED 2 | Enable LED 1 |

### **0x33: DAC control bits for LED pulser, QAmp Offset, VGA DAC**

This defines the operating mode of this octal 12 bit DAC. See the AD5328 data sheet

### **0x34: LED1 pulser current.**

The current is scaled from -10mA at a setting of 0 to +10mA at a setting of 0xFFF

### **0x35: LED2 pulser current.**

### **0x36: Charge Amp Inner Offset**

The charge offset voltage is scaled from -2V at a setting of 0x000 to +2V at a setting of 0xFFF.

### **0x37: Charge Amp Outer Offset**

The charge offset voltage is scaled from -2V at a setting of 0x000 to +2V at a setting of 0xFFF.

### **0x38: VGA gain for Phonon A**

Gain voltage is scaled from -0.7V (gain of .884) at a setting of 0x000 to +0.7V (gain of 113) at a setting of 0xFFF. Refer to the AD600 data sheet for details.

### **0x39: VGA gain for Phonon B**

### **0x3A: VGA gain for Phonon C**

### **0x3B: VGA gain for Phonon D**

### **0x3C: Test signal generator control bits**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 14 | 13 | 12 | 11:9 | 8 | 7:5 | 4 | 3:1 | 0 |
| QET bias range select | Not  Used | DDS chip Ctrl Pin | Connect QET D to test signal | Not USed | Connect QET C to test signal | Not USed | Connect QET B to test signal | Not Used | Connect QET A to test signal |

### **0x3D: DDS control register**

### For the bit significances of these registers, refer to the AD5932 data sheet

### **0x3E: DDS no. of increments register**

### **0x3F: DDS Frequency increment value lower bits**

### **0x40: DDS Frequency increment value upper bits**

### **0x41: DDS Increment interval**

### **0x42: DDS Start frequency lower bits**

### **0x43: DDS Start frequency upper bits**

### **0x44: Test Signal Scaling DAC**

A 10 bit DAC value of 0x000 to 0xFFF scales the DDS output from 6mV to approximately 6Vpp. Internally, the DAC ignores the two lower order bits in the data field. This voltage is divided by 5 when connected to the phonon feedback amplifiers. It is routed through 10K ohm resistors when connected to the QET bias.

### **0x45:** Configuration bits for Phonon A and Phonon B

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 13:12 | 11 | 10 | 9:8 | 7 | 5:4 | 3 | 2 | 1:0 |
| Zap enable Ph B | Ph B PGA gain select | Ph B FB test signal connect | Ph B ADC signal source select | Polarity select Phonon B | Zap enable Ph A | Ph A PGA gain select | Ph A FB test signal connect | Ph A ADC signal source select | Polarity select Phonon A |

Chan A Bits:

Bits 1:0 00: Feedback disabled

01: Non\_Inverting

10: Inverting

11: Feedback disabled

Bit 2 0 : ADC connected to feedback amp output

1 : ADC connected to preamp output

Bit 3 0 : Test Signal disconnected

1 : Test Signal connected

Bits 5:4: 00:11 – PGA Gain settings of 1,2,4 and 8

Bit 7 0 : Squid connected to preamp input

1 : Squid connected to VZap

Chan B Bits:

Bits 9:8 00: Feedback disabled

01: Non\_Inverting

10: Inverting

11: Feedback disabled

Bit 10 0 : ADC connected to feedback amp output

1 : ADC connected to preamp output

Bit 11 0 : Test Signal disconnected

1 : Test Signal connected

Bits 13:12: 00:11 – PGA Gain settings of 1,2,4 and 8

Bit 15 0 : Squid connected to preamp input

1 : Squid connected to VZap

### **0x46: DAC control bits for settings on Phonon A and B**

This defines the operating mode of this octal 16 bit DAC. See the AD5668 data sheet

### **0x47:** ADC offset for Phonon A

A DAC range of 0x0000 to 0xFFFF is scaled to an offset range at the PGA input of -4 to 4 volts. Between this offset is and the phonon ADC is the PGA and a fixed gain of two.

### **0x48:** Lockpoint adjustment for Phonon A

A DAC range of 0x0000 to 0xFFFF is scaled to an offset range at the preamp input of -27mV to +27mV

### **0x49:** Squid Bias for Phonon A

A DAC range of 0x0000 to 0xFFFF is scaled to a bias current range of -200uA to 200uA

### **0x4A:** QET bias for Phonon A

A DAC range of 0x000) to 0xFFFF is scaled to a bias current range of -1.6mA to 1.6mA in the low range and -4mA to 4mA in high range

### **0x4B:** ADC offset for Phonon B

### **0x4C:** Lockpoint adjustment for Phonon B

### **0x4D:** Squid Bias for Phonon B

### **0x4E:** QET bias for Phonon B

### **0x4F:** Configuration bits for Phonon D and Phonon C

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15 | 13:12 | 11 | 10 | 9:8 | 7 | 5:4 | 3 | 2 | 1:0 |
| Zap enable Ph D | Ph D PGA gain select | Ph D FB test signal connect | Ph D ADC signal source select | Polarity select Phonon D | Zap enable Ph C | Ph C PGA gain select | Ph C FB test signal connect | Ph C ADC signal source select | Polarity select Phonon C |

Chan C Bits:

Bits 1:0 00: Feedback disabled

01: Non\_Inverting

10: Inverting

11: Feedback disabled

Bit 2 0 : ADC connected to feedback amp output

1 : ADC connected to preamp output

Bit 3 0 : Test Signal disconnected

1 : Test Signal connected

Bits 5:4 00:11 – PGA Gain settings of 1,2,4 and 8

Bit 7 0 : Squid connected to preamp input

1 : Squid connected to VZap

Chan D Bits:

Bits 9:8 00: Feedback disabled

01: Non\_Inverting

10: Inverting

11: Feedback disabled

Bit 10 0 : ADC connected to feedback amp output

1 : ADC connected to preamp output

Bit 11 0 : Test Signal disconnected

1 : Test Signal connected

Bits 14:12 000: PGA disabled

001:111 – PGA Gain settings from 1:7

Bit 15 0 : Squid connected to preamp input

1 : Squid connected to VZap

### **0x50: DAC control bits for settings on Phonon C and D**

This defines the operating mode of this octal 16 bit DAC. See the AD5668 data sheet

### **0x51:** ADC offset for Phonon C

### **0x52:** Lockpoint adjustment for Phonon C

### **0x53:** Squid Bias for Phonon C

### **0x54:** QET bias for Phonon C

### **0x55:** ADC offset for Phonon D

### **0x56:** Lockpoint adjustment for Phonon D

### **0x57:** Squid Bias for Phonon D

### **0x58:** QET bias for Phonon D

### **0x59:** Charge Inner Bias DAC

A 16 bit DAC range of 0x0000 to 0xFFFF is scaled to a bias voltage of -14V to +14V

### **0x5A:** Charge Outer Bias DAC

### **0x5B:** Read of un-buffered QI data

### **0x5C:** Read of un-buffered QO data

### **0x5D:** Write to charge ADC command registers