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In addition, see the Virtex-6 FPGA Memory Interface Solutions User Guide [Ref 6] and the Virtex-6 FPGA Memory Resources User Guide [Ref ML605 Hardware User Guide www.xilinx.com UG534 (v1.2.1) January 21, 2010... Page 20: Mb Platform Flash Xl FPGA design recommendations. 4.

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82. www.xilinx.com. ML605 Hardware User Guide. UG534 (v1.8) October 2, 2012. Appendix C: VITA 57.1 FMC LPC (J63) and HPC (J64) Connector Pinout Figure C-35. shows the pinout of the FMC HPC connector.. For more information, refer to the VITA 57.1 FMC HPC Connections table (. X-Ref Target - Figure C-35

Figure c-35: fmc hpc connector pinout | Xilinx ML605 User ...

ML605 Evaluation Kit Getting Started Guide www.xilinx.com 5 UG533 (v1.5) October 20, 2011 Preface About This Guide This user guide introduces the Virtex®-6 FPGA ML605 board features, provides instructions for setting up the hardware, and includes step-by-step procedures for verifying the ML605 board functionality. Additional Documentation

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1. UG534, ML605 Hardware User Guide 2. UG535, ML605 Reference Design User Guide 3. DS150, Virtex-6 Family Overview 4. DS152, Virtex-6 FPGA Data Sheet: DC and Switching Characteristics 5. UG360, Virtex-6 FPGA Configuration User Guide 6. UG361, Virtex-6 FPGA SelectIO Resources User Guide 7. UG362, Virtex-6 FPGA User Guide: Clocking Resources 8.

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ML605 Hardware User Guide. UG534 (v1.2.1) January 21, 2010. Detailed Description. Table 1-8 shows the PCIe connector (P1) that provides up to 8-lane access through the GTX transceivers to the Virtex-6 FPGA integrated Endpoint block for PCIe designs. Table 1-8: PCIe Edge Connector Connections. U1 FPGA.

Xilinx ML605. 5. System ACE CF and CompactFlash Connector ...

Xilinx Virtex-6 Mig User Guide A board to discuss topics on MIG GUI,DDR2,DDR3,DDRII, RLDRAM,QDR,QDRII,LPDDR,MCB,etc. MIG-core for DDR3 in Virtex-7 hangs after every ot4. The Virtex-6 DDR2/DDR3 MIG design has two clock inputs, the reference clock section of theVirtex-6 FPGA Memory Interface Solutions User Guide(UG406):.

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