Verificando arquivos...
Código-fonte do programa: Quicksort_malloc.c
Arquivo de configuração de CPU: MyO3CPU.py --> MyO3CPU.py
Arquivo de configuração de caches e memória: MyCaches.py --> MyCaches.py
Arquivo de configuração de sistema: MySystem.py --> MySystem.py

****
* Compilando o programa ...
* g++ -static Quicksort_malloc.c -o Quicksort_malloc
****

****
* Executando o gem5...
* gem5 --outdir=m5out MySimulation.py -c Quicksort_malloc
****

gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 compiled Feb 16 2016 16:35:34
gem5 started Dec 14 2017 15:02:00
gem5 executing on simulacaolse3
command line: gem5 --outdir=m5out MySimulation.py -c Quicksort_malloc

Programa a ser executado: Quicksort_malloc
Global frequency set at 1000000000000 ticks per second
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb.listener: listening for remote gdb on port 7002

---------- Begin Simulation ----------
info: Entering event queue @ 0. Starting simulation...

Vetor
info: Increasing stack size by one page.
23, 9, 16, 29, 23, 1, 22, 13, 33, 5, 6, 40, 0, 46, 2, 2, 3, 48, 45, 8, 8, 34, 0, 13, 24, 18, 18, 17, 39, 27, 28, 13, 38, 44, 44, 13, 47, 18, 26, 32, 23, 32, 22, 24, 31, 27, 28, 36, 25, 24, 45, 33, 10, 45, 49, 34, 16, 17, 2, 7, 46, 32, 22, 34, 28, 16, 49, 25, 34, 26, 7, 10, 8, 32, 34, 41, 9, 12, 28, 36, 38, 23, 19, 49, 20, 18, 33, 36, 37, 37, 46, 35, 19, 18, 21, 47, 35, 21, 24, 21, 47, 32, 31, 7, 16, 17, 49, 27, 30, 27, 13, 20, 2, 34, 19, 22, 3, 5, 11, 42, 42, 7, 28, 12, 25, 1, 11, 12, 22, 38, 34, 19, 22, 17, 29, 38, 35, 28, 15, 17, 7, 30, 37, 9, 14, 7, 31, 17, 12, 44, 12, 6, 1, 42, 18, 29, 43, 32, 43, 16, 20, 29, 37, 44, 47, 16, 32, 34, 46, 49, 1, 3, 29, 38, 12, 43, 47, 46, 13, 11, 42, 27, 18, 46, 21, 38, 27, 14, 22, 20, 32, 44, 2, 22, 38, 1, 38, 22, 35, 37, 21, 36, 40, 2, 26, 5, 48, 24, 3, 11, 37, 45, 40, 5, 43, 11, 44, 20, 25, 18, 43, 10, 13, 45, 32, 1, 46, 22, 24, 31, 9, 47, 19, 2, 0, 45, 9, 48, 21, 12, 11, 11, 9, 1, 16, 5, 12, 12, 25, 39, 31, 18, 49, 44, 15, 33, 47, 13, 6, 21, 46, 17, 19, 15, 21, 21, 13, 30, 19, 36, 44, 30, 47, 6, 31, 14, 11, 45, 28, 38, 34, 11, 9, 34, 7, 24, 17, 5, 38, 25, 26, 34, 45, 47, 2, 16, 18, 15, 47, 39, 1, 43, 21, 49, 49, 4, 15, 10, 49, 45, 1, 34, 7, 10, 20, 14, 34, 39, 19, 24, 15, 48, 11, 12, 47, 13, 28, 18, 30, 25, 7, 33, 21, 31, 34, 20, 35, 49, 33, 37, 47, 34, 21, 4, 44, 43, 18, 30, 32, 40, 5, 49, 40, 16, 11, 37, 31, 42, 7, 11, 19, 17, 44, 40,

48, 29, 11, 33, 30, 44, 20, 27, 30, 43, 33, 24, 36, 4, 4, 21, 44, 11, 22, 36, 29, 36, 25, 10, 28, 33, 23, 47, 0, 20, 38, 0, 1, 1, 33, 33, 47, 6, 11, 27, 1, 44, 1, 40, 0, 7, 13, 46, 19, 35, 32, 48, 21, 8, 11, 1, 43, 36, 49, 43, 6, 39, 45, 7, 40, 28, 41, 39, 36, 4, 16, 40, 0, 19, 30, 1, 26, 43, 47, 45, 28, 32, 46, 2, 40, 9, 3, 35, 45, 4, 30, 4, 43, 25, 11, 35, 5, 4, 24, 42, 10, 42, 32, 13, 11, 14, 14, 38, 7, 13, 35, 37, 45, 33, 39, 37, 42, 45, 24, 40, 49, 4, 44, 45, 29, 7, 30, 35, 14, 7, 29, 24, 49, 13, 37, 11, 27, 3, 1, 36, 19, 36, 23, 16, 22, 13, 6, 14, 8, 30, 6, 9, 37, 0, 4, 18, 8, 37, 3, 22, 44, 34, 48, 45, 49, 38, 8, 26, 43, 9, 12, 12, 48, 36, 31, 20, 1, 39, 36, 11, 21, 43, 20, 8, 43, 27, 27, 3, 14, 32, 25, 10, 19, 24, 5, 18, 14, 14, 47, 7, 25, 9, 22, 25, 47, 5, 47, 0, 44, 34, 13, 15, 29, 36, 26, 24, 13, 5, 28, 29, 39, 5, 39, 8, 31, 44, 29, 45, 10, 26, 5, 36, 37, 27, 11, 35, 32, 11, 37, 28, 45, 1, 43, 26, 39, 21, 2, 2, 26, 30, 31, 16, 38, 20, 26, 21, 16, 5, 19, 27, 31, 24, 15, 19, 1, 28, 6, 35, 39, 45, 13, 36, 48, 8, 14, 37, 30, 17, 41, 8, 47, 24, 26, 37, 44, 5, 9, 13, 10, 28, 42, 44, 4, 9, 13, 7, 37, 21, 42, 29, 16, 7, 15, 15, 15, 30, 4, 47, 49, 46, 8, 48, 20, 36, 36, 17, 41, 47, 30, 2, 27, 24, 46, 31, 33, 11, 38, 20, 34, 32, 1, 2, 39, 19, 19, 6, 1, 24, 6, 0, 20, 14, 48, 40, 0, 34, 9, 42, 33, 39, 46, 10, 15, 44, 41, 48, 5, 31, 19, 41, 13, 22, 43, 4, 41, 13, 11, 42, 37, 17, 42, 9, 33, 41, 1, 35, 27, 11, 29, 11, 2, 25, 21, 18, 19, 15, 16, 26, 48, 37, 17, 12, 10, 13, 18, 1, 26, 31, 44, 15, 0, 38, 26, 33, 29, 27, 21, 9, 40, 0, 20, 45, 26, 43, 13, 47, 10, 31, 24, 9, 21, 43, 23, 31, 6, 41, 34, 34, 23, 30, 1, 23, 19, 27, 9, 0, 7, 30, 9, 49, 30, 31, 44, 8, 25, 9, 6, 35, 41, 32, 44, 12, 25, 17, 45, 34, 11, 29, 18, 34, 12, 22, 9, 31, 49, 18, 33, 8, 0, 45, 8, 33, 26, 2, 41, 3, 14, 49, 39, 5, 33, 35, 19, 11, 5, 16, 45, 16, 45, 15, 2, 9, 37, 13, 42, 39, 34, 26, 47, 34, 21, 7, 17, 49, 12, 11, 3, 26, 12, 42, 33, 46, 29, 2, 7, 34, 18, 4, 2, 15, 19, 4, 25, 9, 18, 19, 48, 2, 45, 47, 38, 18, 7, 8, 18, 19, 19, 21, 47, 31, 15, 30, 29, 44, 34, 36, 31, 4, 40, 33, 21, 12, 40, 48, 21, 8, 18, 21, 12, 13, 20, 2, 34, 27, 10, 2, 48, 31, 25, 45, 13, 40, 25, 42, 34, 9, 31, 17, 15, 23, 1, 37, 35, 41, 35, 6, 1, 3, 29, 15, 19, 0, 17, 3, 29, 28, 7, 28, 9, 32, 23, 24, 22, 1, 19, 8, 12, 2, 26, 28, 25, 27, 15, 11, 20, 2, 19, 21, 8, 49, 36, 27, 1, 3, 32, 30, 33, 39, 10, 45, 21, 34, 19, 45, 35, 40,

Vetor

0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 23, 23, 23, 23, 23, 23, 23, 23, 23, 23, 23, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 34, 34, 34, 34, 34,

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48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 49, 49, 49, 49, 49, 49, 49, 49, 49,
49, 49, 49, 49, 49, 49, 49, 49, 49, 49, 49, 49,
Finishing simulation. Current tick: 1042033500. Reason: target called exit()
---------------- End Simulation ----------------
****
* Resultados da simulação
****

sim_seconds 0.001042 # Number of seconds simulated
sim_ticks 1042033500 # Number of ticks simulated
final_tick 1042033500 # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
sim_freq 1000000000000 # Frequency of simulated ticks
host_inst_rate 106812 # Simulator instruction rate (inst/s)
host_op_rate 198033 # Simulator op (including micro ops) rate (op/s)
host_tick_rate 71316274 # Simulator tick rate (ticks/s)
host_mem_usage 654372 # Number of bytes of host memory used
host_seconds 14.61 # Real time elapsed on the host
sim_insts 1560675 # Number of instructions simulated
sim_ops 2893543 # Number of ops (including micro ops) simulated
system.clk_domain.voltage_domain.voltage 1 # Voltage in Volts
system.clk_domain.clock 500 # Clock period in ticks
system.mem_ctrl.bytes_read::cpu.inst 26304 # Number of bytes read from this memory
system.mem_ctrl.bytes_read::cpu.data 19200 # Number of bytes read from this memory
system.mem_ctrl.bytes_read::total 45504 # Number of bytes read from this memory
system.mem_ctrl.bytes_inst_read::cpu.inst 26304 # Number of instructions bytes read from this memory
system.mem_ctrl.bytes_inst_read::total 26304 # Number of instructions bytes read from this memory
system.mem_ctrl.num_reads::cpu.inst 411 # Number of read requests responded to by this memory
system.mem_ctrl.num_reads::cpu.data 300 # Number of read requests responded to by this memory
system.mem_ctrl.num_reads::total 711 # Number of read requests responded to by this memory
system.mem_ctrl.bw_read::cpu.inst 25242950 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_read::cpu.data 18425511 # Total read bandwidth from this memory (bytes/s)

system.mem_ctrl.bw_read::total 43668462 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_inst_read::cpu.inst 25242950 # Instruction read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_inst_read::total 25242950 # Instruction read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_total::cpu.inst 25242950 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.bw_total::cpu.data 18425511 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.bw_total::total 43668462 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.readReqs 711 # Number of read requests accepted
system.mem_ctrl.writeReqs 0 # Number of write requests accepted
system.mem_ctrl.readBursts 711 # Number of DRAM read bursts, including those serviced by the write queue
system.mem_ctrl.writeBursts 0 # Number of DRAM write bursts, including those merged in the write queue
system.mem_ctrl.bytesReadDRAM 45504 # Total number of bytes read from DRAM
system.mem_ctrl.bytesReadWrQ 0 # Total number of bytes read from write queue
system.mem_ctrl.bytesWritten 0 # Total number of bytes written to DRAM
system.mem_ctrl.bytesReadSys 45504 # Total read bytes from the system interface side
system.mem_ctrl.bytesWrittenSys 0 # Total written bytes from the system interface side
system.mem_ctrl.servicedByWrQ 0 # Number of DRAM read bursts serviced by the write queue
system.mem_ctrl.mergedWrBursts 0 # Number of DRAM write bursts merged with an existing one
system.mem_ctrl.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write
system.mem_ctrl.perBankRdBursts::0 71 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::1 121 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::2 73 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::3 59 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::4 73 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::5 24 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::6 136 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::7 9 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::8 12 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::9 36 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::10 19 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::11 14 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::12 25 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::13 32 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::14 5 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::15 2 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::0 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::1 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::2 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::3 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::4 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::5 0 # Per bank write bursts

system.mem_ctrl.perBankWrBursts::6 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::7 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::8 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::9 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::10 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::11 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::12 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::13 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::14 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::15 0 # Per bank write bursts
system.mem_ctrl.numRdRetry 0 # Number of times read queue was full causing retry
system.mem_ctrl.numWrRetry 0 # Number of times write queue was full causing retry
system.mem_ctrl.totGap 1041958500 # Total gap between requests
system.mem_ctrl.readPktSize::0 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::1 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::2 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::3 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::4 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::5 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::6 711 # Read request sizes (log2)
system.mem_ctrl.writePktSize::0 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::1 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::2 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::3 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::4 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::5 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::6 0 # Write request sizes (log2)
system.mem_ctrl.rdQLenPdf::0 513 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::1 155 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::2 37 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::3 6 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::4 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::5 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::6 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::7 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::8 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::9 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::10 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::11 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::12 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::13 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::14 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::15 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::16 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::17 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::18 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::19 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::20 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::21 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::22 0 # What read queue length does an incoming req see

system.mem_ctrl.rdQLenPdf::23 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::24 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::25 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::26 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::27 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::28 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::29 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::30 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::31 0 # What read queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::0 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::1 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::2 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::3 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::4 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::5 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::6 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::7 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::8 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::9 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::10 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::11 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::12 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::13 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::14 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::15 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::16 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::17 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::18 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::19 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::20 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::21 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::22 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::23 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::24 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::25 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::26 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::27 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::28 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::29 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::30 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::31 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::32 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::33 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::34 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::35 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::36 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::37 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::38 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::39 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::40 0 # What write queue length does an incoming req see

system.mem_ctrl.wrQLenPdf::41 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::42 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::43 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::44 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::45 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::46 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::47 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::48 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::49 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::50 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::51 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::52 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::53 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::54 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::55 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::56 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::57 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::58 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::59 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::60 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::61 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::62 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::63 0 # What write queue length does an incoming req see
system.mem_ctrl.bytesPerActivate::samples 181 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::mean 241.149171 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::gmean 148.511764 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::stdev 273.626682 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::0-127 78 43.09% 43.09% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::128-255 48 26.52% 69.61% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::256-383 18 9.94% 79.56% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::384-511 9 4.97% 84.53% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::512-639 6 3.31% 87.85% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::640-767 2 1.10% 88.95% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::768-895 8 4.42% 93.37% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::896-1023 4 2.21% 95.58% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::1024-1151 8 4.42% 100.00% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::total 181 # Bytes accessed per row activation
system.mem_ctrl.totQLat 6080750 # Total ticks spent queuing
system.mem_ctrl.totMemAccLat 19412000 # Total ticks spent from burst creation until serviced by the DRAM
system.mem_ctrl.totBusLat 3555000 # Total ticks spent in databus transfers

system.mem_ctrl.avgQLat 8552.39 # Average queueing delay per DRAM burst
system.mem_ctrl.avgBusLat 5000.00 # Average bus latency per DRAM burst
system.mem_ctrl.avgMemAccLat 27302.39 # Average memory access latency per DRAM burst
system.mem_ctrl.avgRdBW 43.67 # Average DRAM read bandwidth in MiByte/s
system.mem_ctrl.avgWrBW 0.00 # Average achieved write bandwidth in MiByte/s
system.mem_ctrl.avgRdBWSys 43.67 # Average system read bandwidth in MiByte/s
system.mem_ctrl.avgWrBWSys 0.00 # Average system write bandwidth in MiByte/s
system.mem_ctrl.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s
system.mem_ctrl.busUtil 0.34 # Data bus utilization in percentage
system.mem_ctrl.busUtilRead 0.34 # Data bus utilization in percentage for reads
system.mem_ctrl.busUtilWrite 0.00 # Data bus utilization in percentage for writes
system.mem_ctrl.avgRdQLen 1.09 # Average read queue length when enqueuing
system.mem_ctrl.avgWrQLen 0.00 # Average write queue length when enqueuing
system.mem_ctrl.readRowHits 523 # Number of row buffer hits during reads
system.mem_ctrl.writeRowHits 0 # Number of row buffer hits during writes
system.mem_ctrl.readRowHitRate 73.56 # Row buffer hit rate for reads
system.mem_ctrl.writeRowHitRate nan # Row buffer hit rate for writes
system.mem_ctrl.avgGap 1465483.12 # Average gap between requests
system.mem_ctrl.pageHitRate 73.56 # Row buffer hit rate, read and write combined
system.mem_ctrl_0.actEnergy 1005480 # Energy for activate commands per rank (pJ)
system.mem_ctrl_0.preEnergy 548625 # Energy for precharge commands per rank (pJ)
system.mem_ctrl_0.readEnergy 3939000 # Energy for read commands per rank (pJ)
system.mem_ctrl_0.writeEnergy 0 # Energy for write commands per rank (pJ)
system.mem_ctrl_0.refreshEnergy 67638480 # Energy for refresh commands per rank (pJ)
system.mem_ctrl_0.actBackEnergy 229216095 # Energy for active background per rank (pJ)
system.mem_ctrl_0.preBackEnergy 420423750 # Energy for precharge background per rank (pJ)
system.mem_ctrl_0.totalEnergy 722771430 # Total energy per rank (pJ)
system.mem_ctrl_0.averagePower 697.778740 # Core power per rank (mW)
system.mem_ctrl_0.memoryStateTime::IDLE 699844000 # Time in different power states
system.mem_ctrl_0.memoryStateTime::REF 34580000 # Time in different power states
system.mem_ctrl_0.memoryStateTime::PRE_PDN 0 # Time in different power states
system.mem_ctrl_0.memoryStateTime::ACT 303910500 # Time in different power states
system.mem_ctrl_0.memoryStateTime::ACT_PDN 0 # Time in different power states
system.mem_ctrl_1.actEnergy 287280 # Energy for activate commands per rank (pJ)
system.mem_ctrl_1.preEnergy 156750 # Energy for precharge commands per rank (pJ)
system.mem_ctrl_1.readEnergy 1021800 # Energy for read commands per rank (pJ)
system.mem_ctrl_1.writeEnergy 0 # Energy for write commands per rank (pJ)
system.mem_ctrl_1.refreshEnergy 67638480 # Energy for refresh commands per rank (pJ)
system.mem_ctrl_1.actBackEnergy 39246210 # Energy for active background per rank (pJ)
system.mem_ctrl_1.preBackEnergy 587064000 # Energy for precharge background per rank (pJ)
system.mem_ctrl_1.totalEnergy 695414520 # Total energy per rank (pJ)
system.mem_ctrl_1.averagePower 671.367804 # Core power per rank (mW)
system.mem_ctrl_1.memoryStateTime::IDLE 980004750 # Time in different power states
system.mem_ctrl_1.memoryStateTime::REF 34580000 # Time in different power states
system.mem_ctrl_1.memoryStateTime::PRE_PDN 0 # Time in different power states
system.mem_ctrl_1.memoryStateTime::ACT 24682250 # Time in different power states
system.mem_ctrl_1.memoryStateTime::ACT_PDN 0 # Time in different power states

system.cpu.branchPred.lookups 341138 # Number of BP lookups
system.cpu.branchPred.condPredicted 341138 # Number of conditional branches predicted
system.cpu.branchPred.condIncorrect 8793 # Number of conditional branches incorrect
system.cpu.branchPred.BTBLookups 231197 # Number of BTB lookups
system.cpu.branchPred.BTBHits 185997 # Number of BTB hits
system.cpu.branchPred.BTBCorrect 0 # Number of correct BTB predictions (this stat may not work properly.
system.cpu.branchPred.BTBHitPct 80.449573 # BTB Hit Percentage
system.cpu.branchPred.usedRAS 24749 # Number of times the RAS was used to get a target.
system.cpu.branchPred.RASInCorrect 115 # Number of incorrect RAS predictions.
system.cpu.apic_clk_domain.clock 8000 # Clock period in ticks
system.cpu.workload.num_syscalls 14 # Number of system calls
system.cpu.numCycles 2084068 # number of cpu cycles simulated
system.cpu.numWorkItemsStarted 0 # number of work items this cpu started
system.cpu.numWorkItemsCompleted 0 # number of work items this cpu completed
system.cpu.fetch.icacheStallCycles 619363 # Number of cycles fetch is stalled on an Icache miss
system.cpu.fetch.Insts 1760002 # Number of instructions fetch has processed
system.cpu.fetch.Branches 341138 # Number of branches that fetch encountered
system.cpu.fetch.predictedBranches 210746 # Number of branches that fetch has predicted taken
system.cpu.fetch.Cycles 1429614 # Number of cycles fetch has run and was not squashing or blocked
system.cpu.fetch.SquashCycles 17765 # Number of cycles fetch has spent squashing
system.cpu.fetch.MiscStallCycles 36 # Number of cycles fetch has spent waiting on interrupts, or bad addresses, or out of MSHRs
system.cpu.fetch.PendingTrapStallCycles 567 # Number of stall cycles due to pending traps
system.cpu.fetch.PendingQuiesceStallCycles 13 # Number of stall cycles due to pending quiesce instructions
system.cpu.fetch.CacheLines 598471 # Number of cache lines fetched
system.cpu.fetch.IcacheSquashes 2401 # Number of outstanding Icache misses that were squashed
system.cpu.fetch.rateDist::samples 2058475 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::mean 1.567555 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::stdev 1.373388 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::underflows 0 0.00% 0.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::0 792169 38.48% 38.48% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::1 202400 9.83% 48.32% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::2 167345 8.13% 56.45% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::3 896561 43.55% 100.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::overflows 0 0.00% 100.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::min_value 0 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::max_value 3 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::total 2058475 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.branchRate 0.163689 # Number of branch fetches per cycle
system.cpu.fetch.rate 0.844503 # Number of inst fetches per cycle
system.cpu.decode.IdleCycles 647644 # Number of cycles decode is idle
system.cpu.decode.BlockedCycles 209889 # Number of cycles decode is blocked
system.cpu.decode.RunCycles 1136765 # Number of cycles decode is running
system.cpu.decode.UnblockCycles 55295 # Number of cycles decode is unblocking
system.cpu.decode.SquashCycles 8882 # Number of cycles decode is squashing
system.cpu.decode.DecodedInsts 3095241 # Number of instructions handled by decode
system.cpu.decode.SquashedInsts 23065 # Number of squashed instructions handled by decode
system.cpu.rename.SquashCycles 8882 # Number of cycles rename is squashing
system.cpu.rename.IdleCycles 690416 # Number of cycles rename is idle
system.cpu.rename.BlockCycles 126924 # Number of cycles rename is blocking
system.cpu.rename.serializeStallCycles 494 # count of cycles rename stalled for serializing inst
system.cpu.rename.RunCycles 1140553 # Number of cycles rename is running
system.cpu.rename.UnblockCycles 91206 # Number of cycles rename is unblocking
system.cpu.rename.RenamedInsts 3065667 # Number of instructions processed by rename
system.cpu.rename.SquashedInsts 16379 # Number of squashed instructions processed by rename
system.cpu.rename.ROBFullEvents 64358 # Number of times rename has blocked due to ROB full
system.cpu.rename.IQFullEvents 5064 # Number of times rename has blocked due to IQ full
system.cpu.rename.SQFullEvents 8919 # Number of times rename has blocked due to SQ full
system.cpu.rename.RenamedOperands 3613252 # Number of destination operands rename has renamed
system.cpu.rename.RenameLookups 7948908 # Number of register rename lookups that rename has made
system.cpu.rename.int_rename_lookups 4547242 # Number of integer rename lookups
system.cpu.rename.fp_rename_lookups 156482 # Number of floating rename lookups
system.cpu.rename.CommittedMaps 3397021 # Number of HB maps that are committed
system.cpu.rename.UndoneMaps 216231 # Number of HB maps that are undone due to squashing
system.cpu.rename.serializingInsts 23 # count of serializing insts renamed
system.cpu.rename.tempSerializingInsts 23 # count of temporary serializing insts renamed
system.cpu.rename.skidInsts 127390 # count of insts added to the skid buffer
system.cpu.memDep0.insertedLoads 467880 # Number of loads inserted to the mem dependence unit.
system.cpu.memDep0.insertedStores 241389 # Number of stores inserted to the mem dependence unit.
system.cpu.memDep0.conflictingLoads 79964 # Number of conflicting loads.
system.cpu.memDep0.conflictingStores 17849 # Number of conflicting stores.
system.cpu.iq.iqInstsAdded 3052467 # Number of instructions added to the IQ (excludes non-spec)
system.cpu.iq.iqNonSpecInstsAdded 62 # Number of non-speculative instructions added to the IQ

system.cpu.iq.iqInstsIssued 3003321 # Number of instructions issued
system.cpu.iq.iqSquashedInstsIssued 2618 # Number of squashed instructions issued
system.cpu.iq.iqSquashedInstsExamined 158986 # Number of squashed instructions iterated over during squash; mainly for profiling
system.cpu.iq.iqSquashedOperandsExamined 196365 # Number of squashed operands that are examined and possibly removed from graph
system.cpu.iq.iqSquashedNonSpecRemoved 47 # Number of squashed non-spec instructions that were removed
system.cpu.iq.issued_per_cycle::samples 2058475 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::mean 1.459003 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::stdev 0.977663 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::underflows 0 0.00% 0.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::0 433306 21.05% 21.05% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::1 526428 25.57% 46.62% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::2 834803 40.55% 87.18% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::3 248465 12.07% 99.25% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::4 15473 0.75% 100.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::overflows 0 0.00% 100.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::min_value 0 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::max_value 4 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::total 2058475 # Number of insts issued each cycle
system.cpu.iq.fu_full::No_OpClass 0 0.00% 0.00% # attempts to use FU when none available
system.cpu.iq.fu_full::IntAlu 426131 73.38% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::IntMult 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::IntDiv 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatAdd 16 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatCmp 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatCvt 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatMult 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatDiv 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatSqrt 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAdd 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAddAcc 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAlu 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdCmp 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdCvt 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMisc 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMult 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMultAcc 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdShift 0 0.00% 73.38% # attempts to use FU when none available

system.cpu.iq.fu_full::SimdShiftAcc 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdSqrt 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatAdd 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatAlu 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatCmp 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatCvt 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatDiv 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMisc 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMult 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMultAcc 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatSqrt 0 0.00% 73.38% # attempts to use FU when none available
system.cpu.iq.fu_full::MemRead 110535 19.03% 92.41% # attempts to use FU when none available
system.cpu.iq.fu_full::MemWrite 44068 7.59% 100.00% # attempts to use FU when none available
system.cpu.iq.fu_full::IprAccess 0 0.00% 100.00% # attempts to use FU when none available
system.cpu.iq.fu_full::InstPrefetch 0 0.00% 100.00% # attempts to use FU when none available
system.cpu.iq.FU_type_0::No_OpClass 14207 0.47% 0.47% # Type of FU issued
system.cpu.iq.FU_type_0::IntAlu 2216224 73.79% 74.27% # Type of FU issued
system.cpu.iq.FU_type_0::IntMult 5739 0.19% 74.46% # Type of FU issued
system.cpu.iq.FU_type_0::IntDiv 28 0.00% 74.46% # Type of FU issued
system.cpu.iq.FU_type_0::FloatAdd 72198 2.40% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::FloatCmp 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::FloatCvt 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::FloatMult 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::FloatDiv 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::FloatSqrt 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAdd 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAddAcc 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAlu 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdCmp 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdCvt 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMisc 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMult 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMultAcc 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdShift 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdShiftAcc 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdSqrt 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatAdd 0 0.00% 76.86% # Type of FU issued

system.cpu.iq.FU_type_0::SimdFloatAlu 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatCmp 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatCvt 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatDiv 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMisc 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMult 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMultAcc 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatSqrt 0 0.00% 76.86% # Type of FU issued
system.cpu.iq.FU_type_0::MemRead 457843 15.24% 92.11% # Type of FU issued
system.cpu.iq.FU_type_0::MemWrite 237082 7.89% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::IprAccess 0 0.00% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::InstPrefetch 0 0.00% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::total 3003321 # Type of FU issued
system.cpu.iq.rate 1.441086 # Inst issue rate
system.cpu.iq.fu_busy_cnt 580750 # FU busy when requested
system.cpu.iq.fu_busy_rate 0.193369 # FU busy rate (busy events/executed inst)
system.cpu.iq.int_inst_queue_reads 8459890 # Number of integer instruction queue reads
system.cpu.iq.int_inst_queue_writes 3119163 # Number of integer instruction queue writes
system.cpu.iq.int_inst_queue_wakeup_accesses 2891279 # Number of integer instruction queue wakeup accesses
system.cpu.iq.fp_inst_queue_reads 188595 # Number of floating instruction queue reads
system.cpu.iq.fp_inst_queue_writes 92413 # Number of floating instruction queue writes
system.cpu.iq.fp_inst_queue_wakeup_accesses 92255 # Number of floating instruction queue wakeup accesses
system.cpu.iq.int_alu_accesses 3473546 # Number of integer alu accesses
system.cpu.iq.fp_alu_accesses 96318 # Number of floating point alu accesses
system.cpu.iew.lsq.thread0.forwLoads 53331 # Number of loads that had data forwarded from stores
system.cpu.iew.lsq.thread0.invAddrLoads 0 # Number of loads ignored due to an invalid address
system.cpu.iew.lsq.thread0.squashedLoads 39188 # Number of loads squashed
system.cpu.iew.lsq.thread0.ignoredResponses 34 # Number of memory responses ignored because the instruction is squashed
system.cpu.iew.lsq.thread0.memOrderViolation 61 # Number of memory ordering violations
system.cpu.iew.lsq.thread0.squashedStores 6473 # Number of stores squashed
system.cpu.iew.lsq.thread0.invAddrSwpfs 0 # Number of software prefetches ignored due to an invalid address
system.cpu.iew.lsq.thread0.blockedLoads 0 # Number of blocked loads due to partial load-store forwarding
system.cpu.iew.lsq.thread0.rescheduledLoads 34 # Number of loads that were rescheduled
system.cpu.iew.lsq.thread0.cacheBlocked 9 # Number of times an access to memory failed due to the cache being blocked
system.cpu.iew.iewIdleCycles 0 # Number of cycles IEW is idle
system.cpu.iew.iewSquashCycles 8882 # Number of cycles IEW is squashing
system.cpu.iew.iewBlockCycles 38734 # Number of cycles IEW is blocking
system.cpu.iew.iewUnblockCycles 23 # Number of cycles IEW is unblocking
system.cpu.iew.iewDispatchedInsts 3052529 # Number of instructions dispatched to IQ
system.cpu.iew.iewDispSquashedInsts 0 # Number of squashed instructions skipped by dispatch
system.cpu.iew.iewDispLoadInsts 467880 # Number of dispatched load instructions

system.cpu.iew.iewDispStoreInsts 241389 # Number of dispatched store instructions
system.cpu.iew.iewDispNonSpecInsts 24 # Number of dispatched non-speculative instructions
system.cpu.iew.iewIQFullEvents 5 # Number of times the IQ has become full, causing a stall
system.cpu.iew.iewLSQFullEvents 9 # Number of times the LSQ has become full, causing a stall
system.cpu.iew.memOrderViolationEvents 61 # Number of memory order violations
system.cpu.iew.predictedTakenIncorrect 5723 # Number of branches that were predicted taken incorrectly
system.cpu.iew.predictedNotTakenIncorrect 3359 # Number of branches that were predicted not taken incorrectly
system.cpu.iew.branchMispredicts 9082 # Number of branch mispredicts detected at execute
system.cpu.iew.iewExecutedInsts 2991610 # Number of executed instructions
system.cpu.iew.iewExecLoadInsts 453255 # Number of load instructions executed
system.cpu.iew.iewExecSquashedInsts 11711 # Number of squashed instructions skipped in execute
system.cpu.iew.exec_swp 0 # number of swp insts executed
system.cpu.iew.exec_nop 0 # number of nop insts executed
system.cpu.iew.exec_refs 689404 # number of memory reference insts executed
system.cpu.iew.exec_branches 318594 # Number of branches executed
system.cpu.iew.exec_stores 236149 # Number of stores executed
system.cpu.iew.exec_rate 1.435467 # Inst execution rate
system.cpu.iew.wb_sent 2985797 # cumulative count of insts sent to commit
system.cpu.iew.wb_count 2983534 # cumulative count of insts written-back
system.cpu.iew.wb_producers 2073333 # num instructions producing a value
system.cpu.iew.wb_consumers 3243260 # num instructions consuming a value
system.cpu.iew.wb_penalized 0 # number of instrctions required to write to 'other' IQ
system.cpu.iew.wb_rate 1.431591 # insts written-back per cycle
system.cpu.iew.wb_fanout 0.639274 # average fanout of values written-back
system.cpu.iew.wb_penalized_rate 0 # fraction of instructions written-back that wrote to 'other' IQ
system.cpu.commit.commitSquashedInsts 145268 # The number of squashed insts skipped by commit
system.cpu.commit.commitNonSpecStalls 15 # The number of times commit has been forced to stall to communicate backwards
system.cpu.commit.branchMispredicts 8827 # The number of times a branch was mispredicted
system.cpu.commit.committed_per_cycle::samples 2016464 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::mean 1.434959 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::stdev 1.479554 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::underflows 0 0.00% 0.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::0 772769 38.32% 38.32% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::1 440594 21.85% 60.17% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::2 296145 14.69% 74.86% # Number of insts

commited each cycle
system.cpu.commit.committed_per_cycle::3 167165 8.29% 83.15% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::4 339791 16.85% 100.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::overflows 0 0.00% 100.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::min_value 0 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::max_value 4 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::total 2016464 # Number of insts commited each cycle
system.cpu.commit.committedInsts 1560675 # Number of instructions committed
system.cpu.commit.committedOps 2893543 # Number of ops (including micro ops) committed
system.cpu.commit.swp_count 0 # Number of s/w prefetches committed
system.cpu.commit.refs 663608 # Number of memory references committed
system.cpu.commit.loads 428692 # Number of loads committed
system.cpu.commit.membars 0 # Number of memory barriers committed
system.cpu.commit.branches 307998 # Number of branches committed
system.cpu.commit.fp_insts 92175 # Number of committed floating point instructions.
system.cpu.commit.int_insts 2807982 # Number of committed integer instructions.
system.cpu.commit.function_calls 23882 # Number of function calls committed.
system.cpu.commit.op_class_0::No_OpClass 14060 0.49% 0.49% # Class of committed instruction
system.cpu.commit.op_class_0::IntAlu 2137978 73.89% 74.37% # Class of committed instruction
system.cpu.commit.op_class_0::IntMult 5735 0.20% 74.57% # Class of committed instruction
system.cpu.commit.op_class_0::IntDiv 28 0.00% 74.57% # Class of committed instruction
system.cpu.commit.op_class_0::FloatAdd 72134 2.49% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::FloatCmp 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::FloatCvt 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::FloatMult 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::FloatDiv 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::FloatSqrt 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAdd 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAddAcc 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAlu 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdCmp 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdCvt 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMisc 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMult 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMultAcc 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdShift 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdShiftAcc 0 0.00% 77.07% # Class of committed

instruction
system.cpu.commit.op_class_0::SimdSqrt 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatAdd 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatAlu 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatCmp 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatCvt 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatDiv 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMisc 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMult 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMultAcc 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatSqrt 0 0.00% 77.07% # Class of committed instruction
system.cpu.commit.op_class_0::MemRead 428692 14.82% 91.88% # Class of committed instruction
system.cpu.commit.op_class_0::MemWrite 234916 8.12% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::IprAccess 0 0.00% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::InstPrefetch 0 0.00% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::total 2893543 # Class of committed instruction
system.cpu.commit.bw_lim_events 339791 # number cycles where commit BW limit reached
system.cpu.rob.rob_reads 4715484 # The number of ROB reads
system.cpu.rob.rob_writes 6119676 # The number of ROB writes
system.cpu.timesIdled 287 # Number of times that the entire CPU went into an idle state and unscheduled itself
system.cpu.idleCycles 25593 # Total number of cycles that the CPU has spent unscheduled due to idling
system.cpu.committedInsts 1560675 # Number of Instructions Simulated
system.cpu.committedOps 2893543 # Number of Ops (including micro ops) Simulated
system.cpu.cpi 1.335363 # CPI: Cycles Per Instruction
system.cpu.cpi_total 1.335363 # CPI: Total CPI of All Threads
system.cpu.ipc 0.748860 # IPC: Instructions Per Cycle
system.cpu.ipc_total 0.748860 # IPC: Total IPC of All Threads
system.cpu.int_regfile_reads 4413338 # number of integer regfile reads
system.cpu.int_regfile_writes 2342475 # number of integer regfile writes
system.cpu.fp_regfile_reads 156415 # number of floating regfile reads
system.cpu.fp_regfile_writes 76201 # number of floating regfile writes
system.cpu.cc_regfile_reads 1844152 # number of cc regfile reads
system.cpu.cc_regfile_writes 1084057 # number of cc regfile writes
system.cpu.misc_regfile_reads 1319074 # number of misc regfile reads
system.cpu.misc_regfile_writes 1 # number of misc regfile writes

system.cpu.dcache.tags.replacements 10 # number of replacements
system.cpu.dcache.tags.tagsinuse 261.179468 # Cycle average of tags in use
system.cpu.dcache.tags.total_refs 634397 # Total number of references to valid blocks.
system.cpu.dcache.tags.sampled_refs 302 # Sample count of references to valid blocks.
system.cpu.dcache.tags.avg_refs 2100.652318 # Average number of references to valid blocks.
system.cpu.dcache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.dcache.tags.occ_blocks::cpu.data 261.179468 # Average occupied blocks per requestor
system.cpu.dcache.tags.occ_percent::cpu.data 0.510116 # Average percentage of cache occupancy
system.cpu.dcache.tags.occ_percent::total 0.510116 # Average percentage of cache occupancy
system.cpu.dcache.tags.occ_task_id_blocks::1024 292 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::0 10 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::2 123 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::3 159 # Occupied blocks per task id
system.cpu.dcache.tags.occ_task_id_percent::1024 0.570312 # Percentage of cache occupancy per task id
system.cpu.dcache.tags.tag_accesses 2539350 # Number of tag accesses
system.cpu.dcache.tags.data_accesses 2539350 # Number of data accesses
system.cpu.dcache.ReadReq_hits::cpu.data 399693 # number of ReadReq hits
system.cpu.dcache.ReadReq_hits::total 399693 # number of ReadReq hits
system.cpu.dcache.WriteReq_hits::cpu.data 234704 # number of WriteReq hits
system.cpu.dcache.WriteReq_hits::total 234704 # number of WriteReq hits
system.cpu.dcache.demand_hits::cpu.data 634397 # number of demand (read+write) hits
system.cpu.dcache.demand_hits::total 634397 # number of demand (read+write) hits
system.cpu.dcache.overall_hits::cpu.data 634397 # number of overall hits
system.cpu.dcache.overall_hits::total 634397 # number of overall hits
system.cpu.dcache.ReadReq_misses::cpu.data 153 # number of ReadReq misses
system.cpu.dcache.ReadReq_misses::total 153 # number of ReadReq misses
system.cpu.dcache.WriteReq_misses::cpu.data 212 # number of WriteReq misses
system.cpu.dcache.WriteReq_misses::total 212 # number of WriteReq misses
system.cpu.dcache.demand_misses::cpu.data 365 # number of demand (read+write) misses
system.cpu.dcache.demand_misses::total 365 # number of demand (read+write) misses
system.cpu.dcache.overall_misses::cpu.data 365 # number of overall misses
system.cpu.dcache.overall_misses::total 365 # number of overall misses
system.cpu.dcache.ReadReq_miss_latency::cpu.data 11028500 # number of ReadReq miss cycles
system.cpu.dcache.ReadReq_miss_latency::total 11028500 # number of ReadReq miss cycles
system.cpu.dcache.WriteReq_miss_latency::cpu.data 15284750 # number of WriteReq miss cycles
system.cpu.dcache.WriteReq_miss_latency::total 15284750 # number of WriteReq miss cycles
system.cpu.dcache.demand_miss_latency::cpu.data 26313250 # number of demand (read+write) miss cycles
system.cpu.dcache.demand_miss_latency::total 26313250 # number of demand (read+write) miss cycles
system.cpu.dcache.overall_miss_latency::cpu.data 26313250 # number of overall miss cycles

system.cpu.dcache.overall_miss_latency::total 26313250 # number of overall miss cycles
system.cpu.dcache.ReadReq_accesses::cpu.data 399846 # number of ReadReq accesses(hits+misses)
system.cpu.dcache.ReadReq_accesses::total 399846 # number of ReadReq accesses(hits+misses)
system.cpu.dcache.WriteReq_accesses::cpu.data 234916 # number of WriteReq accesses(hits+misses)
system.cpu.dcache.WriteReq_accesses::total 234916 # number of WriteReq accesses(hits+misses)
system.cpu.dcache.demand_accesses::cpu.data 634762 # number of demand (read+write) accesses
system.cpu.dcache.demand_accesses::total 634762 # number of demand (read+write) accesses
system.cpu.dcache.overall_accesses::cpu.data 634762 # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total 634762 # number of overall (read+write) accesses
system.cpu.dcache.ReadReq_miss_rate::cpu.data 0.000383 # miss rate for ReadReq accesses
system.cpu.dcache.ReadReq_miss_rate::total 0.000383 # miss rate for ReadReq accesses
system.cpu.dcache.WriteReq_miss_rate::cpu.data 0.000902 # miss rate for WriteReq accesses
system.cpu.dcache.WriteReq_miss_rate::total 0.000902 # miss rate for WriteReq accesses
system.cpu.dcache.demand_miss_rate::cpu.data 0.000575 # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total 0.000575 # miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data 0.000575 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.000575 # miss rate for overall accesses
system.cpu.dcache.ReadReq_avg_miss_latency::cpu.data 72081.699346 # average ReadReq miss latency
system.cpu.dcache.ReadReq_avg_miss_latency::total 72081.699346 # average ReadReq miss latency
system.cpu.dcache.WriteReq_avg_miss_latency::cpu.data 72097.877358 # average WriteReq miss latency
system.cpu.dcache.WriteReq_avg_miss_latency::total 72097.877358 # average WriteReq miss latency
system.cpu.dcache.demand_avg_miss_latency::cpu.data 72091.095890 # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total 72091.095890 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data 72091.095890 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total 72091.095890 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 229 # number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs 6 # number of cycles access was blocked
system.cpu.dcache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs 38.166667 # average number of cycles each access was blocked
system.cpu.dcache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.dcache.fast_writes 0 # number of fast writes performed

system.cpu.dcache.cache_copies 0 # number of cache copies performed
system.cpu.dcache.writebacks::writebacks 9 # number of writebacks
system.cpu.dcache.writebacks::total 9 # number of writebacks
system.cpu.dcache.ReadReq_mshr_hits::cpu.data 63 # number of ReadReq MSHR hits
system.cpu.dcache.ReadReq_mshr_hits::total 63 # number of ReadReq MSHR hits
system.cpu.dcache.demand_mshr_hits::cpu.data 63 # number of demand (read+write) MSHR hits
system.cpu.dcache.demand_mshr_hits::total 63 # number of demand (read+write) MSHR hits
system.cpu.dcache.overall_mshr_hits::cpu.data 63 # number of overall MSHR hits
system.cpu.dcache.overall_mshr_hits::total 63 # number of overall MSHR hits
system.cpu.dcache.ReadReq_mshr_misses::cpu.data 90 # number of ReadReq MSHR misses
system.cpu.dcache.ReadReq_mshr_misses::total 90 # number of ReadReq MSHR misses
system.cpu.dcache.WriteReq_mshr_misses::cpu.data 212 # number of WriteReq MSHR misses
system.cpu.dcache.WriteReq_mshr_misses::total 212 # number of WriteReq MSHR misses
system.cpu.dcache.demand_mshr_misses::cpu.data 302 # number of demand (read+write) MSHR misses
system.cpu.dcache.demand_mshr_misses::total 302 # number of demand (read+write) MSHR misses
system.cpu.dcache.overall_mshr_misses::cpu.data 302 # number of overall MSHR misses
system.cpu.dcache.overall_mshr_misses::total 302 # number of overall MSHR misses
system.cpu.dcache.ReadReq_mshr_miss_latency::cpu.data 6782000 # number of ReadReq MSHR miss cycles
system.cpu.dcache.ReadReq_mshr_miss_latency::total 6782000 # number of ReadReq MSHR miss cycles
system.cpu.dcache.WriteReq_mshr_miss_latency::cpu.data 14892250 # number of WriteReq MSHR miss cycles
system.cpu.dcache.WriteReq_mshr_miss_latency::total 14892250 # number of WriteReq MSHR miss cycles
system.cpu.dcache.demand_mshr_miss_latency::cpu.data 21674250 # number of demand (read+write) MSHR miss cycles
system.cpu.dcache.demand_mshr_miss_latency::total 21674250 # number of demand (read+write) MSHR miss cycles
system.cpu.dcache.overall_mshr_miss_latency::cpu.data 21674250 # number of overall MSHR miss cycles
system.cpu.dcache.overall_mshr_miss_latency::total 21674250 # number of overall MSHR miss cycles
system.cpu.dcache.ReadReq_mshr_miss_rate::cpu.data 0.000225 # mshr miss rate for ReadReq accesses
system.cpu.dcache.ReadReq_mshr_miss_rate::total 0.000225 # mshr miss rate for ReadReq accesses
system.cpu.dcache.WriteReq_mshr_miss_rate::cpu.data 0.000902 # mshr miss rate for WriteReq accesses
system.cpu.dcache.WriteReq_mshr_miss_rate::total 0.000902 # mshr miss rate for WriteReq accesses
system.cpu.dcache.demand_mshr_miss_rate::cpu.data 0.000476 # mshr miss rate for demand accesses
system.cpu.dcache.demand_mshr_miss_rate::total 0.000476 # mshr miss rate for demand accesses
system.cpu.dcache.overall_mshr_miss_rate::cpu.data 0.000476 # mshr miss rate for overall

accesses
system.cpu.dcache.overall_mshr_miss_rate::total 0.000476 # mshr miss rate for overall accesses
system.cpu.dcache.ReadReq_avg_mshr_miss_latency::cpu.data 75355.555556 # average ReadReq mshr miss latency
system.cpu.dcache.ReadReq_avg_mshr_miss_latency::total 75355.555556 # average ReadReq mshr miss latency
system.cpu.dcache.WriteReq_avg_mshr_miss_latency::cpu.data 70246.462264 # average WriteReq mshr miss latency
system.cpu.dcache.WriteReq_avg_mshr_miss_latency::total 70246.462264 # average WriteReq mshr miss latency
system.cpu.dcache.demand_avg_mshr_miss_latency::cpu.data 71769.039735 # average overall mshr miss latency
system.cpu.dcache.demand_avg_mshr_miss_latency::total 71769.039735 # average overall mshr miss latency
system.cpu.dcache.overall_avg_mshr_miss_latency::cpu.data 71769.039735 # average overall mshr miss latency
system.cpu.dcache.overall_avg_mshr_miss_latency::total 71769.039735 # average overall mshr miss latency
system.cpu.dcache.no_allocate_misses 0 # Number of misses that were no-allocate
system.cpu.icache.tags.replacements 24 # number of replacements
system.cpu.icache.tags.tagsinuse 326.393601 # Cycle average of tags in use
system.cpu.icache.tags.total_refs 597985 # Total number of references to valid blocks.
system.cpu.icache.tags.sampled_refs 414 # Sample count of references to valid blocks.
system.cpu.icache.tags.avg_refs 1444.408213 # Average number of references to valid blocks.
system.cpu.icache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.icache.tags.occ_blocks::cpu.inst 326.393601 # Average occupied blocks per requestor
system.cpu.icache.tags.occ_percent::cpu.inst 0.637488 # Average percentage of cache occupancy
system.cpu.icache.tags.occ_percent::total 0.637488 # Average percentage of cache occupancy
system.cpu.icache.tags.occ_task_id_blocks::1024 390 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::0 65 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::2 130 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::3 195 # Occupied blocks per task id
system.cpu.icache.tags.occ_task_id_percent::1024 0.761719 # Percentage of cache occupancy per task id
system.cpu.icache.tags.tag_accesses 2394298 # Number of tag accesses
system.cpu.icache.tags.data_accesses 2394298 # Number of data accesses
system.cpu.icache.ReadReq_hits::cpu.inst 597985 # number of ReadReq hits
system.cpu.icache.ReadReq_hits::total 597985 # number of ReadReq hits
system.cpu.icache.demand_hits::cpu.inst 597985 # number of demand (read+write) hits
system.cpu.icache.demand_hits::total 597985 # number of demand (read+write) hits
system.cpu.icache.overall_hits::cpu.inst 597985 # number of overall hits
system.cpu.icache.overall_hits::total 597985 # number of overall hits
system.cpu.icache.ReadReq_misses::cpu.inst 486 # number of ReadReq misses
system.cpu.icache.ReadReq_misses::total 486 # number of ReadReq misses
system.cpu.icache.demand_misses::cpu.inst 486 # number of demand (read+write) misses

system.cpu.icache.demand_misses::total 486 # number of demand (read+write) misses
system.cpu.icache.overall_misses::cpu.inst 486 # number of overall misses
system.cpu.icache.overall_misses::total 486 # number of overall misses
system.cpu.icache.ReadReq_miss_latency::cpu.inst 32332750 # number of ReadReq miss cycles
system.cpu.icache.ReadReq_miss_latency::total 32332750 # number of ReadReq miss cycles
system.cpu.icache.demand_miss_latency::cpu.inst 32332750 # number of demand (read+write) miss cycles
system.cpu.icache.demand_miss_latency::total 32332750 # number of demand (read+write) miss cycles
system.cpu.icache.overall_miss_latency::cpu.inst 32332750 # number of overall miss cycles
system.cpu.icache.overall_miss_latency::total 32332750 # number of overall miss cycles
system.cpu.icache.ReadReq_accesses::cpu.inst 598471 # number of ReadReq accesses(hits+misses)
system.cpu.icache.ReadReq_accesses::total 598471 # number of ReadReq accesses(hits+misses)
system.cpu.icache.demand_accesses::cpu.inst 598471 # number of demand (read+write) accesses
system.cpu.icache.demand_accesses::total 598471 # number of demand (read+write) accesses
system.cpu.icache.overall_accesses::cpu.inst 598471 # number of overall (read+write) accesses
system.cpu.icache.overall_accesses::total 598471 # number of overall (read+write) accesses
system.cpu.icache.ReadReq_miss_rate::cpu.inst 0.000812 # miss rate for ReadReq accesses
system.cpu.icache.ReadReq_miss_rate::total 0.000812 # miss rate for ReadReq accesses
system.cpu.icache.demand_miss_rate::cpu.inst 0.000812 # miss rate for demand accesses
system.cpu.icache.demand_miss_rate::total 0.000812 # miss rate for demand accesses
system.cpu.icache.overall_miss_rate::cpu.inst 0.000812 # miss rate for overall accesses
system.cpu.icache.overall_miss_rate::total 0.000812 # miss rate for overall accesses
system.cpu.icache.ReadReq_avg_miss_latency::cpu.inst 66528.292181 # average ReadReq miss latency
system.cpu.icache.ReadReq_avg_miss_latency::total 66528.292181 # average ReadReq miss latency
system.cpu.icache.demand_avg_miss_latency::cpu.inst 66528.292181 # average overall miss latency
system.cpu.icache.demand_avg_miss_latency::total 66528.292181 # average overall miss latency
system.cpu.icache.overall_avg_miss_latency::cpu.inst 66528.292181 # average overall miss latency
system.cpu.icache.overall_avg_miss_latency::total 66528.292181 # average overall miss latency
system.cpu.icache.blocked_cycles::no_mshrs 32 # number of cycles access was blocked
system.cpu.icache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.icache.blocked::no_mshrs 1 # number of cycles access was blocked
system.cpu.icache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.icache.avg_blocked_cycles::no_mshrs 32 # average number of cycles each access was blocked
system.cpu.icache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.icache.fast_writes 0 # number of fast writes performed

system.cpu.icache.cache_copies 0 # number of cache copies performed
system.cpu.icache.ReadReq_mshr_hits::cpu.inst 71 # number of ReadReq MSHR hits
system.cpu.icache.ReadReq_mshr_hits::total 71 # number of ReadReq MSHR hits
system.cpu.icache.demand_mshr_hits::cpu.inst 71 # number of demand (read+write) MSHR hits
system.cpu.icache.demand_mshr_hits::total 71 # number of demand (read+write) MSHR hits
system.cpu.icache.overall_mshr_hits::cpu.inst 71 # number of overall MSHR hits
system.cpu.icache.overall_mshr_hits::total 71 # number of overall MSHR hits
system.cpu.icache.ReadReq_mshr_misses::cpu.inst 415 # number of ReadReq MSHR misses
system.cpu.icache.ReadReq_mshr_misses::total 415 # number of ReadReq MSHR misses
system.cpu.icache.demand_mshr_misses::cpu.inst 415 # number of demand (read+write) MSHR misses
system.cpu.icache.demand_mshr_misses::total 415 # number of demand (read+write) MSHR misses
system.cpu.icache.overall_mshr_misses::cpu.inst 415 # number of overall MSHR misses
system.cpu.icache.overall_mshr_misses::total 415 # number of overall MSHR misses
system.cpu.icache.ReadReq_mshr_miss_latency::cpu.inst 27543750 # number of ReadReq MSHR miss cycles
system.cpu.icache.ReadReq_mshr_miss_latency::total 27543750 # number of ReadReq MSHR miss cycles
system.cpu.icache.demand_mshr_miss_latency::cpu.inst 27543750 # number of demand (read+write) MSHR miss cycles
system.cpu.icache.demand_mshr_miss_latency::total 27543750 # number of demand (read+write) MSHR miss cycles
system.cpu.icache.overall_mshr_miss_latency::cpu.inst 27543750 # number of overall MSHR miss cycles
system.cpu.icache.overall_mshr_miss_latency::total 27543750 # number of overall MSHR miss cycles
system.cpu.icache.ReadReq_mshr_miss_rate::cpu.inst 0.000693 # mshr miss rate for ReadReq accesses
system.cpu.icache.ReadReq_mshr_miss_rate::total 0.000693 # mshr miss rate for ReadReq accesses
system.cpu.icache.demand_mshr_miss_rate::cpu.inst 0.000693 # mshr miss rate for demand accesses
system.cpu.icache.demand_mshr_miss_rate::total 0.000693 # mshr miss rate for demand accesses
system.cpu.icache.overall_mshr_miss_rate::cpu.inst 0.000693 # mshr miss rate for overall accesses
system.cpu.icache.overall_mshr_miss_rate::total 0.000693 # mshr miss rate for overall accesses
system.cpu.icache.ReadReq_avg_mshr_miss_latency::cpu.inst 66370.481928 # average ReadReq mshr miss latency
system.cpu.icache.ReadReq_avg_mshr_miss_latency::total 66370.481928 # average ReadReq mshr miss latency
system.cpu.icache.demand_avg_mshr_miss_latency::cpu.inst 66370.481928 # average overall mshr miss latency
system.cpu.icache.demand_avg_mshr_miss_latency::total 66370.481928 # average overall mshr miss latency
system.cpu.icache.overall_avg_mshr_miss_latency::cpu.inst 66370.481928 # average overall mshr miss latency

system.cpu.icache.overall_avg_mshr_miss_latency::total 66370.481928 # average overall mshr miss latency
system.cpu.icache.no_allocate_misses 0 # Number of misses that were no-allocate
system.cpu.l2cache.tags.replacements 0 # number of replacements
system.cpu.l2cache.tags.tagsinuse 414.871890 # Cycle average of tags in use
system.cpu.l2cache.tags.total_refs 7 # Total number of references to valid blocks.
system.cpu.l2cache.tags.sampled_refs 506 # Sample count of references to valid blocks.
system.cpu.l2cache.tags.avg_refs 0.013834 # Average number of references to valid blocks.
system.cpu.l2cache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.l2cache.tags.occ_blocks::writebacks 5.316497 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_blocks::cpu.inst 333.939660 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_blocks::cpu.data 75.615734 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_percent::writebacks 0.000081 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::cpu.inst 0.005096 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::cpu.data 0.001154 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::total 0.006330 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_task_id_blocks::1024 506 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::0 76 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::2 153 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::3 277 # Occupied blocks per task id
system.cpu.l2cache.tags.occ_task_id_percent::1024 0.007721 # Percentage of cache occupancy per task id
system.cpu.l2cache.tags.tag_accesses 6526 # Number of tag accesses
system.cpu.l2cache.tags.data_accesses 6526 # Number of data accesses
system.cpu.l2cache.ReadReq_hits::cpu.inst 3 # number of ReadReq hits
system.cpu.l2cache.ReadReq_hits::cpu.data 2 # number of ReadReq hits
system.cpu.l2cache.ReadReq_hits::total 5 # number of ReadReq hits
system.cpu.l2cache.Writeback_hits::writebacks 9 # number of Writeback hits
system.cpu.l2cache.Writeback_hits::total 9 # number of Writeback hits
system.cpu.l2cache.demand_hits::cpu.inst 3 # number of demand (read+write) hits
system.cpu.l2cache.demand_hits::cpu.data 2 # number of demand (read+write) hits
system.cpu.l2cache.demand_hits::total 5 # number of demand (read+write) hits
system.cpu.l2cache.overall_hits::cpu.inst 3 # number of overall hits
system.cpu.l2cache.overall_hits::cpu.data 2 # number of overall hits
system.cpu.l2cache.overall_hits::total 5 # number of overall hits
system.cpu.l2cache.ReadReq_misses::cpu.inst 412 # number of ReadReq misses
system.cpu.l2cache.ReadReq_misses::cpu.data 88 # number of ReadReq misses
system.cpu.l2cache.ReadReq_misses::total 500 # number of ReadReq misses
system.cpu.l2cache.ReadExReq_misses::cpu.data 212 # number of ReadExReq misses
system.cpu.l2cache.ReadExReq_misses::total 212 # number of ReadExReq misses
system.cpu.l2cache.demand_misses::cpu.inst 412 # number of demand (read+write) misses
system.cpu.l2cache.demand_misses::cpu.data 300 # number of demand (read+write) misses
system.cpu.l2cache.demand_misses::total 712 # number of demand (read+write) misses

system.cpu.l2cache.overall_misses::cpu.inst 412 # number of overall misses
system.cpu.l2cache.overall_misses::cpu.data 300 # number of overall misses
system.cpu.l2cache.overall_misses::total 712 # number of overall misses
system.cpu.l2cache.ReadReq_miss_latency::cpu.inst 27095250 # number of ReadReq miss cycles
system.cpu.l2cache.ReadReq_miss_latency::cpu.data 6578500 # number of ReadReq miss cycles
system.cpu.l2cache.ReadReq_miss_latency::total 33673750 # number of ReadReq miss cycles
system.cpu.l2cache.ReadExReq_miss_latency::cpu.data 14468250 # number of ReadExReq miss cycles
system.cpu.l2cache.ReadExReq_miss_latency::total 14468250 # number of ReadExReq miss cycles
system.cpu.l2cache.demand_miss_latency::cpu.inst 27095250 # number of demand (read+write) miss cycles
system.cpu.l2cache.demand_miss_latency::cpu.data 21046750 # number of demand (read+write) miss cycles
system.cpu.l2cache.demand_miss_latency::total 48142000 # number of demand (read+write) miss cycles
system.cpu.l2cache.overall_miss_latency::cpu.inst 27095250 # number of overall miss cycles
system.cpu.l2cache.overall_miss_latency::cpu.data 21046750 # number of overall miss cycles
system.cpu.l2cache.overall_miss_latency::total 48142000 # number of overall miss cycles
system.cpu.l2cache.ReadReq_accesses::cpu.inst 415 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.ReadReq_accesses::cpu.data 90 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.ReadReq_accesses::total 505 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.Writeback_accesses::writebacks 9 # number of Writeback accesses(hits+misses)
system.cpu.l2cache.Writeback_accesses::total 9 # number of Writeback accesses(hits+misses)
system.cpu.l2cache.ReadExReq_accesses::cpu.data 212 # number of ReadExReq accesses(hits+misses)
system.cpu.l2cache.ReadExReq_accesses::total 212 # number of ReadExReq accesses(hits+misses)
system.cpu.l2cache.demand_accesses::cpu.inst 415 # number of demand (read+write) accesses
system.cpu.l2cache.demand_accesses::cpu.data 302 # number of demand (read+write) accesses
system.cpu.l2cache.demand_accesses::total 717 # number of demand (read+write) accesses
system.cpu.l2cache.overall_accesses::cpu.inst 415 # number of overall (read+write) accesses
system.cpu.l2cache.overall_accesses::cpu.data 302 # number of overall (read+write) accesses
system.cpu.l2cache.overall_accesses::total 717 # number of overall (read+write) accesses
system.cpu.l2cache.ReadReq_miss_rate::cpu.inst 0.992771 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_miss_rate::cpu.data 0.977778 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_miss_rate::total 0.990099 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadExReq_miss_rate::cpu.data 1 # miss rate for ReadExReq accesses
system.cpu.l2cache.ReadExReq_miss_rate::total 1 # miss rate for ReadExReq accesses

system.cpu.l2cache.demand_miss_rate::cpu.inst 0.992771 # miss rate for demand accesses
system.cpu.l2cache.demand_miss_rate::cpu.data 0.993377 # miss rate for demand accesses
system.cpu.l2cache.demand_miss_rate::total 0.993026 # miss rate for demand accesses
system.cpu.l2cache.overall_miss_rate::cpu.inst 0.992771 # miss rate for overall accesses
system.cpu.l2cache.overall_miss_rate::cpu.data 0.993377 # miss rate for overall accesses
system.cpu.l2cache.overall_miss_rate::total 0.993026 # miss rate for overall accesses
system.cpu.l2cache.ReadReq_avg_miss_latency::cpu.inst 65765.169903 # average ReadReq miss latency
system.cpu.l2cache.ReadReq_avg_miss_latency::cpu.data 74755.681818 # average ReadReq miss latency
system.cpu.l2cache.ReadReq_avg_miss_latency::total 67347.500000 # average ReadReq miss latency
system.cpu.l2cache.ReadExReq_avg_miss_latency::cpu.data 68246.462264 # average ReadExReq miss latency
system.cpu.l2cache.ReadExReq_avg_miss_latency::total 68246.462264 # average ReadExReq miss latency
system.cpu.l2cache.demand_avg_miss_latency::cpu.inst 65765.169903 # average overall miss latency
system.cpu.l2cache.demand_avg_miss_latency::cpu.data 70155.833333 # average overall miss latency
system.cpu.l2cache.demand_avg_miss_latency::total 67615.168539 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::cpu.inst 65765.169903 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::cpu.data 70155.833333 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::total 67615.168539 # average overall miss latency
system.cpu.l2cache.blocked_cycles::no_mshrs 0 # number of cycles access was blocked
system.cpu.l2cache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.l2cache.blocked::no_mshrs 0 # number of cycles access was blocked
system.cpu.l2cache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.l2cache.avg_blocked_cycles::no_mshrs nan # average number of cycles each access was blocked
system.cpu.l2cache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.l2cache.fast_writes 0 # number of fast writes performed
system.cpu.l2cache.cache_copies 0 # number of cache copies performed
system.cpu.l2cache.ReadReq_mshr_misses::cpu.inst 412 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadReq_mshr_misses::cpu.data 88 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadReq_mshr_misses::total 500 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadExReq_mshr_misses::cpu.data 212 # number of ReadExReq MSHR misses
system.cpu.l2cache.ReadExReq_mshr_misses::total 212 # number of ReadExReq MSHR misses
system.cpu.l2cache.demand_mshr_misses::cpu.inst 412 # number of demand (read+write) MSHR misses
system.cpu.l2cache.demand_mshr_misses::cpu.data 300 # number of demand (read+write) MSHR misses

system.cpu.l2cache.demand_mshr_misses::total 712 # number of demand (read+write) MSHR misses
system.cpu.l2cache.overall_mshr_misses::cpu.inst 412 # number of overall MSHR misses
system.cpu.l2cache.overall_mshr_misses::cpu.data 300 # number of overall MSHR misses
system.cpu.l2cache.overall_mshr_misses::total 712 # number of overall MSHR misses
system.cpu.l2cache.ReadReq_mshr_miss_latency::cpu.inst 24857750 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_latency::cpu.data 6105500 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_latency::total 30963250 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadExReq_mshr_miss_latency::cpu.data 13333750 # number of ReadExReq MSHR miss cycles
system.cpu.l2cache.ReadExReq_mshr_miss_latency::total 13333750 # number of ReadExReq MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::cpu.inst 24857750 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::cpu.data 19439250 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::total 44297000 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::cpu.inst 24857750 # number of overall MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::cpu.data 19439250 # number of overall MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::total 44297000 # number of overall MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_rate::cpu.inst 0.992771 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_mshr_miss_rate::cpu.data 0.977778 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_mshr_miss_rate::total 0.990099 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadExReq_mshr_miss_rate::cpu.data 1 # mshr miss rate for ReadExReq accesses
system.cpu.l2cache.ReadExReq_mshr_miss_rate::total 1 # mshr miss rate for ReadExReq accesses
system.cpu.l2cache.demand_mshr_miss_rate::cpu.inst 0.992771 # mshr miss rate for demand accesses
system.cpu.l2cache.demand_mshr_miss_rate::cpu.data 0.993377 # mshr miss rate for demand accesses
system.cpu.l2cache.demand_mshr_miss_rate::total 0.993026 # mshr miss rate for demand accesses
system.cpu.l2cache.overall_mshr_miss_rate::cpu.inst 0.992771 # mshr miss rate for overall accesses
system.cpu.l2cache.overall_mshr_miss_rate::cpu.data 0.993377 # mshr miss rate for overall accesses
system.cpu.l2cache.overall_mshr_miss_rate::total 0.993026 # mshr miss rate for overall accesses
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::cpu.inst 60334.344660 # average

ReadReq mshr miss latency
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::cpu.data 69380.681818 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::total 61926.500000 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadExReq_avg_mshr_miss_latency::cpu.data 62895.047170 # average ReadExReq mshr miss latency
system.cpu.l2cache.ReadExReq_avg_mshr_miss_latency::total 62895.047170 # average ReadExReq mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::cpu.inst 60334.344660 # average overall mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::cpu.data 64797.500000 # average overall mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::total 62214.887640 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::cpu.inst 60334.344660 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::cpu.data 64797.500000 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::total 62214.887640 # average overall mshr miss latency
system.cpu.l2cache.no_allocate_misses 0 # Number of misses that were no-allocate
system.l2bus.trans_dist::ReadReq 505 # Transaction distribution
system.l2bus.trans_dist::ReadResp 504 # Transaction distribution
system.l2bus.trans_dist::Writeback 9 # Transaction distribution
system.l2bus.trans_dist::ReadExReq 212 # Transaction distribution
system.l2bus.trans_dist::ReadExResp 212 # Transaction distribution
system.l2bus.pkt_count_system.cpu.icache.mem_side::system.cpu.l2cache.cpu_side 829 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_count_system.cpu.dcache.mem_side::system.cpu.l2cache.cpu_side 613 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_count::total 1442 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_size_system.cpu.icache.mem_side::system.cpu.l2cache.cpu_side 26496 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.pkt_size_system.cpu.dcache.mem_side::system.cpu.l2cache.cpu_side 19904 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.pkt_size::total 46400 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.snoops 0 # Total snoops (count)
system.l2bus.snoop_fanout::samples 726 # Request fanout histogram
system.l2bus.snoop_fanout::mean 1 # Request fanout histogram
system.l2bus.snoop_fanout::stdev 0 # Request fanout histogram
system.l2bus.snoop_fanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.l2bus.snoop_fanout::0 0 0.00% 0.00% # Request fanout histogram
system.l2bus.snoop_fanout::1 726 100.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::2 0 0.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::min_value 1 # Request fanout histogram
system.l2bus.snoop_fanout::max_value 1 # Request fanout histogram
system.l2bus.snoop_fanout::total 726 # Request fanout histogram

system.l2bus.reqLayer0.occupancy 381000 # Layer occupancy (ticks)
system.l2bus.reqLayer0.utilization 0.0 # Layer utilization (%)
system.l2bus.respLayer0.occupancy 1126250 # Layer occupancy (ticks)
system.l2bus.respLayer0.utilization 0.1 # Layer utilization (%)
system.l2bus.respLayer1.occupancy 808750 # Layer occupancy (ticks)
system.l2bus.respLayer1.utilization 0.1 # Layer utilization (%)
system.membus.trans_dist::ReadReq 499 # Transaction distribution
system.membus.trans_dist::ReadResp 499 # Transaction distribution
system.membus.trans_dist::ReadExReq 212 # Transaction distribution
system.membus.trans_dist::ReadExResp 212 # Transaction distribution
system.membus.pkt_count_system.cpu.l2cache.mem_side::system.mem_ctrl.port 1422 # Packet count per connected master and slave (bytes)
system.membus.pkt_count_system.cpu.l2cache.mem_side::total 1422 # Packet count per connected master and slave (bytes)
system.membus.pkt_count::total 1422 # Packet count per connected master and slave (bytes)
system.membus.pkt_size_system.cpu.l2cache.mem_side::system.mem_ctrl.port 45504 # Cumulative packet size per connected master and slave (bytes)
system.membus.pkt_size_system.cpu.l2cache.mem_side::total 45504 # Cumulative packet size per connected master and slave (bytes)
system.membus.pkt_size::total 45504 # Cumulative packet size per connected master and slave (bytes)
system.membus.snoops 0 # Total snoops (count)
system.membus.snoop_fanout::samples 711 # Request fanout histogram
system.membus.snoop_fanout::mean 0 # Request fanout histogram
system.membus.snoop_fanout::stdev 0 # Request fanout histogram
system.membus.snoop_fanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.membus.snoop_fanout::0 711 100.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::1 0 0.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::min_value 0 # Request fanout histogram
system.membus.snoop_fanout::max_value 0 # Request fanout histogram
system.membus.snoop_fanout::total 711 # Request fanout histogram
system.membus.reqLayer2.occupancy 355500 # Layer occupancy (ticks)
system.membus.reqLayer2.utilization 0.0 # Layer utilization (%)
system.membus.respLayer0.occupancy 1922500 # Layer occupancy (ticks)
system.membus.respLayer0.utilization 0.2 # Layer utilization (%)