Verificando arquivos...
Código-fonte do programa: Quicksort_calloc.c
Arquivo de configuração de CPU: MyO3CPU.py --> MyO3CPU.py
Arquivo de configuração de caches e memória: 16.py --> MyCaches.py
Arquivo de configuração de sistema: MySystem.py --> MySystem.py

****
* Compilando o programa ...
* g++ -static Quicksort_calloc.c -o Quicksort_calloc
****

****
* Executando o gem5...
* gem5 --outdir=m5out MySimulation.py -c Quicksort_calloc
****

gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 compiled Feb 16 2016 16:35:34
gem5 started Dec 14 2017 19:01:20
gem5 executing on simulacaolse3
command line: gem5 --outdir=m5out MySimulation.py -c Quicksort_calloc

Programa a ser executado: Quicksort_calloc
Global frequency set at 1000000000000 ticks per second
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb.listener: listening for remote gdb on port 7000

---------- Begin Simulation ----------
info: Entering event queue @ 0. Starting simulation...

Vetor
info: Increasing stack size by one page.
9873, 3259, 9416, 10029, 10573, 2801, 12422, 3263, 2783, 9305, 6056, 4640, 10400, 6196, 12352, 13502, 7253, 6798, 5595, 8658, 7208, 11284, 3650, 4763, 10724, 8768, 9318, 13417, 7239, 6427, 5628, 2113, 1038, 44, 3494, 2963, 9197, 7268, 6226, 3332, 1573, 12282, 7972, 11974, 9831, 11677, 1828, 8436, 3475, 7424, 2095, 10683, 10060, 5745, 6799, 5784, 5866, 1117, 4202, 4457, 13896, 1182, 12922, 14934, 7578, 1416, 9249, 1775, 8684, 476, 5107, 1610, 12758, 4432, 13584, 13941, 1109, 412, 7378, 10936, 14188, 9473, 6619, 9249, 6570, 13418, 33, 12436, 5887, 10587, 8246, 11135, 11769, 6168, 2421, 4347, 7585, 11671, 12474, 7621, 12147, 2582, 9231, 1257, 13366, 14167, 199, 5827, 14580, 7577, 1763, 5120, 8402, 14734, 14369, 14972, 13153, 5755, 3761, 10392, 1342, 12007, 6528, 13112, 3175, 301, 8811, 2112, 11972, 12638, 9734, 9119, 6572, 10317, 1729, 4938, 9485, 1928, 10765, 417, 857, 3880, 5537, 9259, 3614, 4907, 9231, 1767, 10662, 4344, 3512, 3356, 1351, 1392, 1468, 10879, 1693, 1632, 4343, 13666, 14270, 5429, 14137, 12194, 747, 866, 2132, 1584, 9146, 4249, 2001, 10003, 8129, 7538, 4262, 11743, 3797, 4846, 4863, 5811, 542, 14727, 9168,

8246, 7471, 1988, 10477, 9164, 9972, 14820, 14182, 594, 11602, 4672, 12788, 3701, 5538, 6272, 5285, 6037, 10521, 7286, 1040, 10002, 6176, 11655, 13098, 9974, 7853, 2961, 7137, 8395, 9040, 1305, 7993, 1511, 3294, 3470, 10675, 4618, 9643, 1210, 5213, 6245, 5882, 3001, 9946, 2772, 9274, 231, 8809, 11147, 13869, 1202, 6150, 5045, 4209, 4248, 6371, 12062, 13561, 4861, 11809, 7601, 6166, 11155, 9112, 812, 14625, 11139, 5431, 9268, 12349, 10644, 6865, 9583, 4997, 8163, 12356, 14271, 14746, 12517, 10419, 13615, 5071, 7921, 10013, 9280, 12169, 7736, 12694, 10730, 12597, 856, 3331, 3764, 12011, 3795, 10928, 2988, 14934, 7711, 3609, 12284, 9707, 10474, 6867, 14705, 3638, 10575, 13976, 3384, 14445, 747, 8352, 4516, 8668, 3365, 13797, 12189, 11101, 2843, 14271, 8699, 3699, 8954, 3815, 710, 12749, 6095, 10051, 12684, 13807, 13660, 1320, 8514, 9134, 14539, 8219, 4124, 10115, 13548, 13861, 912, 5647, 7213, 5428, 5668, 1930, 4225, 2857, 4383, 13421, 8481, 4434, 2120, 2435, 8249, 9183, 6537, 5697, 4234, 4221, 4504, 2894, 11893, 13018, 3380, 11432, 12590, 7505, 12899, 2490, 6366, 13811, 8137, 4931, 10592, 5157, 6861, 6169, 14367, 11244, 4590, 7848, 679, 6711, 10283, 280, 894, 1820, 5977, 11480, 12393, 1833, 14374, 9286, 6204, 2754, 12071, 3794, 1611, 1322, 12636, 14329, 6486, 12125, 4260, 2078, 2283, 2473, 8247, 1650, 5070, 12838, 850, 12101, 10901, 11133, 3733, 3147, 4306, 9711, 14627, 8051, 11544, 14001, 8690, 9100, 8107, 12113, 4246, 9719, 13435, 1882, 9048, 4921, 14008, 4661, 13351, 7643, 13486, 6599, 9293, 3556, 10789, 1495, 657, 6690, 12628, 4391, 1189, 8286, 5454, 816, 7690, 8350, 6169, 1380, 2451, 14276, 13493, 6697, 8995, 11928, 14932, 9396, 8202, 13940, 5409, 6553, 12935, 3895, 4504, 13580, 13804, 293, 75, 14461, 13335, 4055, 10204, 14524, 12342, 7010, 6692, 5032, 6713, 12861, 12764, 9164, 12138, 11257, 7213, 12485, 14537, 7145, 13233, 7739, 12437, 3642, 5645, 1724, 13890, 10149, 304, 12694, 1795, 379, 3507, 130, 4435, 5064, 6007, 8129, 12074, 12699, 4513, 3787, 10561, 2277, 4303, 14051, 4886, 2869, 11536, 4423, 1366, 1122, 12163, 5156, 4764, 2808, 6880, 10006, 4309, 13537, 7700, 6104, 5268, 11208, 12587, 9703, 1272, 3594, 9184, 4698, 7645, 5049, 14838, 9558, 7326, 10493, 8609, 12212, 13362, 11498, 1636, 6081, 12620, 5151, 2589, 8736, 14311, 821, 3743, 3620, 14358, 11443, 1077, 4627, 14003, 13664, 5682, 275, 8610, 6219, 4974, 1255, 11268, 11164, 10814, 9947, 6657, 10775, 7159, 11372, 13625, 147, 8805, 2597, 11650, 11394, 11334, 2313, 12215, 6429, 12286, 2926, 9224, 13363, 13905, 8228, 3379, 10939, 14855, 11989, 2158, 11181, 13244, 4779, 7345, 410, 14726, 5355, 11186, 13237, 1727, 9811, 13385, 10532, 3761, 1387, 13278, 95, 3701, 10493, 12876, 7339, 4771, 13452, 5702, 3676, 6680, 9081, 14616, 12888, 6070, 8126, 421, 10666, 12905, 14119, 11077, 12631, 4474, 13615, 10869, 6201, 14778, 606, 8085, 3539, 8345, 6363, 9986, 3398, 8208, 14214, 10737, 12980, 12667, 7791, 8008, 4347, 8224, 13976, 8587, 14294, 13455, 9009, 1313, 11360, 8128, 3742, 344, 3954, 8709, 11213, 1507, 8487, 3171, 9592, 3379, 11516, 7307, 13365, 14915, 515, 12580, 2004, 4847, 1599, 9796, 4208, 12298, 3020, 9536, 5886, 8667, 7991, 6247, 9980, 4352, 5727, 5074, 4696, 9681, 13783, 7261, 11188, 7270, 1784, 12132, 2001, 4652, 4439, 6719, 10919, 11306, 10651, 12924, 7506, 12250, 7720, 11714, 9548, 10740, 6250, 434, 10759, 14242, 13033, 5739, 9946, 3760, 2165, 5994, 13441, 948, 13255, 981, 8219, 6391, 13113, 1572, 11043, 8904, 8291, 6963, 5211, 3942, 4887, 12717, 1192, 3959, 783, 10741, 6051, 13385, 2527, 1811, 3979, 561, 13902, 13925, 4321, 1068, 4919, 9115, 2016, 9526, 1448, 1587, 917, 14562, 3160, 3313, 14818, 11451, 10276, 11381, 394, 6515, 450, 7938, 1826, 1233, 3679, 7877, 5971, 12559, 1040, 9950, 13120, 6295, 8876, 8793, 7363, 5147, 9260, 731, 14674, 10709, 8671, 6943, 1623, 11831, 10256, 1441, 14634, 11884, 12823, 6380, 9751, 13273, 14319, 11577, 5859, 9350, 10807, 11830, 6909, 3199, 6780, 11381, 9494, 7008, 5175, 8209, 12156, 14435, 8941, 3182, 10144, 2612, 10125, 11767, 5795, 11734, 4561, 5429, 8618, 2384, 3162, 9722, 7009, 2481, 6299, 12868, 3183, 8458, 1050, 1445, 11658, 14183, 12826, 6152, 6191, 9353, 5714, 9699, 8789, 14655, 4233, 10285, 8619, 5711, 13405, 5766, 2445, 2966, 11195, 2415, 11702, 5709, 12137, 10063, 14542, 9789, 14284, 2726, 3247, 334, 4171, 6257, 14517, 8349, 3762, 12061, 2703, 9476, 13112, 11492, 483, 2346, 13129, 9102, 8057, 11534, 14868, 1854, 5852, 2415, 4269, 2554, 8125, 7759, 12618, 14019, 2548, 11902, 1745, 12147, 3588, 12268, 9757, 9458, 5618, 13519, 6519, 8321, 14347, 4631, 11165, 14830,

13329, 9294, 284, 6386, 12181, 6504, 8240, 3033, 271, 3862, 11940, 14748, 11621, 9558, 13768, 5521, 12812, 513, 9020, 7752, 4134, 3777, 2210, 9752, 8648, 81, 9425, 7995, 4713, 5590, 7825, 3042, 14884, 8109, 781, 3417, 5965, 373, 6451, 6237, 4235, 3391, 5985, 856, 4301, 4753, 12729, 8465, 11619, 6750, 1217, 753, 1879, 3428, 1857, 10528, 3509, 11282, 3523, 14574, 1872, 2701, 8969, 8108, 2162, 1102, 11526, 8128, 1475, 2977, 14365, 5711, 12720, 11702, 12919, 2021, 7808, 10649, 10486, 4427, 8751, 11703, 11532, 10630, 6483, 13389, 12510, 1345, 9671, 1034, 919, 2895, 3735, 1240,

Vetor

33, 44, 75, 81, 95, 130, 147, 199, 231, 271, 275, 280, 284, 293, 301, 304, 334, 344, 373, 379, 394, 410, 412, 417, 421, 434, 450, 476, 483, 513, 515, 542, 561, 594, 606, 657, 679, 710, 731, 747, 747, 753, 781, 783, 812, 816, 821, 850, 856, 856, 857, 866, 894, 912, 917, 919, 948, 981, 1034, 1038, 1040, 1040, 1050, 1068, 1077, 1102, 1109, 1117, 1122, 1182, 1189, 1192, 1202, 1210, 1217, 1233, 1240, 1255, 1257, 1272, 1305, 1313, 1320, 1322, 1342, 1345, 1351, 1366, 1380, 1387, 1392, 1416, 1441, 1445, 1448, 1468, 1475, 1495, 1507, 1511, 1572, 1573, 1584, 1587, 1599, 1610, 1611, 1623, 1632, 1636, 1650, 1693, 1724, 1727, 1729, 1745, 1763, 1767, 1775, 1784, 1795, 1811, 1820, 1826, 1828, 1833, 1854, 1857, 1872, 1879, 1882, 1928, 1930, 1988, 2001, 2001, 2004, 2016, 2021, 2078, 2095, 2112, 2113, 2120, 2132, 2158, 2162, 2165, 2210, 2277, 2283, 2313, 2346, 2384, 2415, 2415, 2421, 2435, 2445, 2451, 2473, 2481, 2490, 2527, 2548, 2554, 2582, 2589, 2597, 2612, 2701, 2703, 2726, 2754, 2772, 2783, 2801, 2808, 2843, 2857, 2869, 2894, 2895, 2926, 2961, 2963, 2966, 2977, 2988, 3001, 3020, 3033, 3042, 3147, 3160, 3162, 3171, 3175, 3182, 3183, 3199, 3247, 3259, 3263, 3294, 3313, 3331, 3332, 3356, 3365, 3379, 3379, 3380, 3384, 3391, 3398, 3417, 3428, 3470, 3475, 3494, 3507, 3509, 3512, 3523, 3539, 3556, 3588, 3594, 3609, 3614, 3620, 3638, 3642, 3650, 3676, 3679, 3699, 3701, 3701, 3733, 3735, 3742, 3743, 3760, 3761, 3761, 3762, 3764, 3777, 3787, 3794, 3795, 3797, 3815, 3862, 3880, 3895, 3942, 3954, 3959, 3979, 4055, 4124, 4134, 4171, 4202, 4208, 4209, 4221, 4225, 4233, 4234, 4235, 4246, 4248, 4249, 4260, 4262, 4269, 4301, 4303, 4306, 4309, 4321, 4343, 4344, 4347, 4347, 4352, 4383, 4391, 4423, 4427, 4432, 4434, 4435, 4439, 4457, 4474, 4504, 4504, 4513, 4516, 4561, 4590, 4618, 4627, 4631, 4640, 4652, 4661, 4672, 4696, 4698, 4713, 4753, 4763, 4764, 4771, 4779, 4846, 4847, 4861, 4863, 4886, 4887, 4907, 4919, 4921, 4931, 4938, 4974, 4997, 5032, 5045, 5049, 5064, 5070, 5071, 5074, 5107, 5120, 5147, 5151, 5156, 5157, 5175, 5211, 5213, 5268, 5285, 5355, 5409, 5428, 5429, 5429, 5431, 5454, 5521, 5537, 5538, 5590, 5595, 5618, 5628, 5645, 5647, 5668, 5682, 5697, 5702, 5709, 5711, 5711, 5714, 5727, 5739, 5745, 5755, 5766, 5784, 5795, 5811, 5827, 5852, 5859, 5866, 5882, 5886, 5887, 5965, 5971, 5977, 5985, 5994, 6007, 6037, 6051, 6056, 6070, 6081, 6095, 6104, 6150, 6152, 6166, 6168, 6169, 6169, 6176, 6191, 6196, 6201, 6204, 6219, 6226, 6237, 6245, 6247, 6250, 6257, 6272, 6295, 6299, 6363, 6366, 6371, 6380, 6386, 6391, 6427, 6429, 6451, 6483, 6486, 6504, 6515, 6519, 6528, 6537, 6553, 6570, 6572, 6599, 6619, 6657, 6680, 6690, 6692, 6697, 6711, 6713, 6719, 6750, 6780, 6798, 6799, 6861, 6865, 6867, 6880, 6909, 6943, 6963, 7008, 7009, 7010, 7137, 7145, 7159, 7208, 7213, 7213, 7239, 7253, 7261, 7268, 7270, 7286, 7307, 7326, 7339, 7345, 7363, 7378, 7424, 7471, 7505, 7506, 7538, 7577, 7578, 7585, 7601, 7621, 7643, 7645, 7690, 7700, 7711, 7720, 7736, 7739, 7752, 7759, 7791, 7808, 7825, 7848, 7853, 7877, 7921, 7938, 7972, 7991, 7993, 7995, 8008, 8051, 8057, 8085, 8107, 8108, 8109, 8125, 8126, 8128, 8128, 8129, 8129, 8137, 8163, 8202, 8208, 8209, 8219, 8219, 8224, 8228, 8240, 8246, 8246, 8247, 8249, 8286, 8291, 8321, 8345, 8349, 8350, 8352, 8395, 8402, 8436, 8458, 8465, 8481, 8487, 8514, 8587, 8609, 8610, 8618, 8619, 8648, 8658, 8667, 8668, 8671, 8684, 8690, 8699, 8709, 8736, 8751, 8768, 8789, 8793, 8805, 8809, 8811, 8876, 8904, 8941, 8954, 8969, 8995, 9009, 9020, 9040, 9048, 9081, 9100, 9102, 9112, 9115, 9119, 9134, 9146, 9164, 9164, 9168, 9183, 9184, 9197, 9224, 9231, 9231, 9249, 9249, 9259, 9260, 9268, 9274, 9280, 9286, 9293, 9294, 9305, 9318, 9350, 9353, 9396, 9416, 9425, 9458, 9473, 9476, 9485, 9494, 9526, 9536, 9548, 9558, 9558, 9583, 9592, 9643, 9671, 9681, 9699, 9703, 9707, 9711, 9719, 9722, 9734, 9751, 9752, 9757, 9789,

9796, 9811, 9831, 9873, 9946, 9946, 9947, 9950, 9972, 9974, 9980, 9986, 10002, 10003, 10006, 10013, 10029, 10051, 10060, 10063, 10115, 10125, 10144, 10149, 10204, 10256, 10276, 10283, 10285, 10317, 10392, 10400, 10419, 10474, 10477, 10486, 10493, 10493, 10521, 10528, 10532, 10561, 10573, 10575, 10587, 10592, 10630, 10644, 10649, 10651, 10662, 10666, 10675, 10683, 10709, 10724, 10730, 10737, 10740, 10741, 10759, 10765, 10775, 10789, 10807, 10814, 10869, 10879, 10901, 10919, 10928, 10936, 10939, 11043, 11077, 11101, 11133, 11135, 11139, 11147, 11155, 11164, 11165, 11181, 11186, 11188, 11195, 11208, 11213, 11244, 11257, 11268, 11282, 11284, 11306, 11334, 11360, 11372, 11381, 11381, 11394, 11432, 11443, 11451, 11480, 11492, 11498, 11516, 11526, 11532, 11534, 11536, 11544, 11577, 11602, 11619, 11621, 11650, 11655, 11658, 11671, 11677, 11702, 11702, 11703, 11714, 11734, 11743, 11767, 11769, 11809, 11830, 11831, 11884, 11893, 11902, 11928, 11940, 11972, 11974, 11989, 12007, 12011, 12061, 12062, 12071, 12074, 12101, 12113, 12125, 12132, 12137, 12138, 12147, 12147, 12156, 12163, 12169, 12181, 12189, 12194, 12212, 12215, 12250, 12268, 12282, 12284, 12286, 12298, 12342, 12349, 12352, 12356, 12393, 12422, 12436, 12437, 12474, 12485, 12510, 12517, 12559, 12580, 12587, 12590, 12597, 12618, 12620, 12628, 12631, 12636, 12638, 12667, 12684, 12694, 12694, 12699, 12717, 12720, 12729, 12749, 12758, 12764, 12788, 12812, 12823, 12826, 12838, 12861, 12868, 12876, 12888, 12899, 12905, 12919, 12922, 12924, 12935, 12980, 13018, 13033, 13098, 13112, 13112, 13113, 13120, 13129, 13153, 13233, 13237, 13244, 13255, 13273, 13278, 13329, 13335, 13351, 13362, 13363, 13365, 13366, 13385, 13385, 13389, 13405, 13417, 13418, 13421, 13435, 13441, 13452, 13455, 13486, 13493, 13502, 13519, 13537, 13548, 13561, 13580, 13584, 13615, 13615, 13625, 13660, 13664, 13666, 13768, 13783, 13797, 13804, 13807, 13811, 13861, 13869, 13890, 13896, 13902, 13905, 13925, 13940, 13941, 13976, 13976, 14001, 14003, 14008, 14019, 14051, 14119, 14137, 14167, 14182, 14183, 14188, 14214, 14242, 14270, 14271, 14271, 14276, 14284, 14294, 14311, 14319, 14329, 14347, 14358, 14365, 14367, 14369, 14374, 14435, 14445, 14461, 14517, 14524, 14537, 14539, 14542, 14562, 14574, 14580, 14616, 14625, 14627, 14634, 14655, 14674, 14705, 14726, 14727, 14734, 14746, 14748, 14778, 14818, 14820, 14830, 14838, 14855, 14868, 14884, 14915, 14932, 14934, 14934, 14972,
Finishing simulation. Current tick: 2038648500. Reason: target called exit()
---------- End Simulation ----------
****
* Resultados da simulação
****

sim_seconds 0.002039 # Number of seconds simulated
sim_ticks 2038648500 # Number of ticks simulated
final_tick 2038648500 # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
sim_freq 1000000000000 # Frequency of simulated ticks
host_inst_rate 93187 # Simulator instruction rate (inst/s)
host_op_rate 172989 # Simulator op (including micro ops) rate (op/s)
host_tick_rate 113042237 # Simulator tick rate (ticks/s)
host_mem_usage 645148 # Number of bytes of host memory used
host_seconds 18.03 # Real time elapsed on the host
sim_insts 1680562 # Number of instructions simulated
sim_ops 3119746 # Number of ops (including micro ops) simulated
system.clk_domain.voltage_domain.voltage 1 # Voltage in Volts
system.clk_domain.clock 500 # Clock period in ticks
system.mem_ctrl.bytes_read::cpu.inst 27904 # Number of bytes read from this memory

system.mem_ctrl.bytes_read::cpu.data 21888 # Number of bytes read from this memory
system.mem_ctrl.bytes_read::total 49792 # Number of bytes read from this memory
system.mem_ctrl.bytes_inst_read::cpu.inst 27904 # Number of instructions bytes read from this memory
system.mem_ctrl.bytes_inst_read::total 27904 # Number of instructions bytes read from this memory
system.mem_ctrl.num_reads::cpu.inst 436 # Number of read requests responded to by this memory
system.mem_ctrl.num_reads::cpu.data 342 # Number of read requests responded to by this memory
system.mem_ctrl.num_reads::total 778 # Number of read requests responded to by this memory
system.mem_ctrl.bw_read::cpu.inst 13687499 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_read::cpu.data 10736525 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_read::total 24424024 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_inst_read::cpu.inst 13687499 # Instruction read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_inst_read::total 13687499 # Instruction read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_total::cpu.inst 13687499 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.bw_total::cpu.data 10736525 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.bw_total::total 24424024 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.readReqs 778 # Number of read requests accepted
system.mem_ctrl.writeReqs 0 # Number of write requests accepted
system.mem_ctrl.readBursts 778 # Number of DRAM read bursts, including those serviced by the write queue
system.mem_ctrl.writeBursts 0 # Number of DRAM write bursts, including those merged in the write queue
system.mem_ctrl.bytesReadDRAM 49792 # Total number of bytes read from DRAM
system.mem_ctrl.bytesReadWrQ 0 # Total number of bytes read from write queue
system.mem_ctrl.bytesWritten 0 # Total number of bytes written to DRAM
system.mem_ctrl.bytesReadSys 49792 # Total read bytes from the system interface side
system.mem_ctrl.bytesWrittenSys 0 # Total written bytes from the system interface side
system.mem_ctrl.servicedByWrQ 0 # Number of DRAM read bursts serviced by the write queue
system.mem_ctrl.mergedWrBursts 0 # Number of DRAM write bursts merged with an existing one
system.mem_ctrl.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write
system.mem_ctrl.perBankRdBursts::0 74 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::1 123 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::2 74 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::3 60 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::4 72 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::5 35 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::6 140 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::7 44 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::8 12 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::9 36 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::10 28 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::11 14 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::12 27 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::13 32 # Per bank write bursts

system.mem_ctrl.perBankRdBursts::14 5 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::15 2 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::0 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::1 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::2 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::3 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::4 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::5 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::6 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::7 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::8 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::9 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::10 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::11 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::12 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::13 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::14 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::15 0 # Per bank write bursts
system.mem_ctrl.numRdRetry 0 # Number of times read queue was full causing retry
system.mem_ctrl.numWrRetry 0 # Number of times write queue was full causing retry
system.mem_ctrl.totGap 2038573500 # Total gap between requests
system.mem_ctrl.readPktSize::0 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::1 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::2 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::3 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::4 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::5 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::6 778 # Read request sizes (log2)
system.mem_ctrl.writePktSize::0 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::1 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::2 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::3 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::4 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::5 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::6 0 # Write request sizes (log2)
system.mem_ctrl.rdQLenPdf::0 581 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::1 152 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::2 39 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::3 6 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::4 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::5 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::6 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::7 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::8 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::9 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::10 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::11 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::12 0 # What read queue length does an incoming req see

system.mem_ctrl.rdQLenPdf::13 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::14 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::15 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::16 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::17 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::18 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::19 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::20 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::21 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::22 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::23 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::24 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::25 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::26 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::27 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::28 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::29 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::30 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::31 0 # What read queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::0 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::1 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::2 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::3 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::4 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::5 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::6 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::7 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::8 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::9 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::10 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::11 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::12 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::13 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::14 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::15 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::16 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::17 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::18 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::19 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::20 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::21 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::22 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::23 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::24 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::25 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::26 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::27 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::28 0 # What write queue length does an incoming req see

system.mem_ctrl.wrQLenPdf::29 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::30 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::31 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::32 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::33 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::34 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::35 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::36 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::37 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::38 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::39 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::40 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::41 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::42 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::43 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::44 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::45 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::46 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::47 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::48 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::49 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::50 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::51 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::52 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::53 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::54 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::55 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::56 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::57 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::58 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::59 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::60 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::61 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::62 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::63 0 # What write queue length does an incoming req see
system.mem_ctrl.bytesPerActivate::samples 244 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::mean 196.459016 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::gmean 117.776192 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::stdev 252.946916 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::0-127 151 61.89% 61.89% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::128-255 34 13.93% 75.82% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::256-383 21 8.61% 84.43% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::384-511 10 4.10% 88.52% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::512-639 8 3.28% 91.80% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::640-767 3 1.23% 93.03% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::768-895 1 0.41% 93.44% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::896-1023 6 2.46% 95.90% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::1024-1151 10 4.10% 100.00% # Bytes accessed per row

activation
system.mem_ctrl.bytesPerActivate::total 244 # Bytes accessed per row activation
system.mem_ctrl.totQLat 7457750 # Total ticks spent queuing
system.mem_ctrl.totMemAccLat 22045250 # Total ticks spent from burst creation until serviced by the DRAM
system.mem_ctrl.totBusLat 3890000 # Total ticks spent in databus transfers
system.mem_ctrl.avgQLat 9585.80 # Average queueing delay per DRAM burst
system.mem_ctrl.avgBusLat 5000.00 # Average bus latency per DRAM burst
system.mem_ctrl.avgMemAccLat 28335.80 # Average memory access latency per DRAM burst
system.mem_ctrl.avgRdBW 24.42 # Average DRAM read bandwidth in MiByte/s
system.mem_ctrl.avgWrBW 0.00 # Average achieved write bandwidth in MiByte/s
system.mem_ctrl.avgRdBWSys 24.42 # Average system read bandwidth in MiByte/s
system.mem_ctrl.avgWrBWSys 0.00 # Average system write bandwidth in MiByte/s
system.mem_ctrl.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s
system.mem_ctrl.busUtil 0.19 # Data bus utilization in percentage
system.mem_ctrl.busUtilRead 0.19 # Data bus utilization in percentage for reads
system.mem_ctrl.busUtilWrite 0.00 # Data bus utilization in percentage for writes
system.mem_ctrl.avgRdQLen 1.01 # Average read queue length when enqueuing
system.mem_ctrl.avgWrQLen 0.00 # Average write queue length when enqueuing
system.mem_ctrl.readRowHits 527 # Number of row buffer hits during reads
system.mem_ctrl.writeRowHits 0 # Number of row buffer hits during writes
system.mem_ctrl.readRowHitRate 67.74 # Row buffer hit rate for reads
system.mem_ctrl.writeRowHitRate nan # Row buffer hit rate for writes
system.mem_ctrl.avgGap 2620274.42 # Average gap between requests
system.mem_ctrl.pageHitRate 67.74 # Row buffer hit rate, read and write combined
system.mem_ctrl_0.actEnergy 1436400 # Energy for activate commands per rank (pJ)
system.mem_ctrl_0.preEnergy 783750 # Energy for precharge commands per rank (pJ)
system.mem_ctrl_0.readEnergy 4383600 # Energy for read commands per rank (pJ)
system.mem_ctrl_0.writeEnergy 0 # Energy for write commands per rank (pJ)
system.mem_ctrl_0.refreshEnergy 132734160 # Energy for refresh commands per rank (pJ)
system.mem_ctrl_0.actBackEnergy 355631265 # Energy for active background per rank (pJ)
system.mem_ctrl_0.preBackEnergy 907517250 # Energy for precharge background per rank (pJ)
system.mem_ctrl_0.totalEnergy 1402486425 # Total energy per rank (pJ)
system.mem_ctrl_0.averagePower 690.044650 # Core power per rank (mW)
system.mem_ctrl_0.memoryStateTime::IDLE 1509114000 # Time in different power states
system.mem_ctrl_0.memoryStateTime::REF 67860000 # Time in different power states
system.mem_ctrl_0.memoryStateTime::PRE_PDN 0 # Time in different power states
system.mem_ctrl_0.memoryStateTime::ACT 457934500 # Time in different power states
system.mem_ctrl_0.memoryStateTime::ACT_PDN 0 # Time in different power states
system.mem_ctrl_1.actEnergy 325080 # Energy for activate commands per rank (pJ)
system.mem_ctrl_1.preEnergy 177375 # Energy for precharge commands per rank (pJ)
system.mem_ctrl_1.readEnergy 1107600 # Energy for read commands per rank (pJ)
system.mem_ctrl_1.writeEnergy 0 # Energy for write commands per rank (pJ)
system.mem_ctrl_1.refreshEnergy 132734160 # Energy for refresh commands per rank (pJ)
system.mem_ctrl_1.actBackEnergy 70522965 # Energy for active background per rank (pJ)
system.mem_ctrl_1.preBackEnergy 1157612250 # Energy for precharge background per rank (pJ)
system.mem_ctrl_1.totalEnergy 1362479430 # Total energy per rank (pJ)
system.mem_ctrl_1.averagePower 670.360600 # Core power per rank (mW)

system.mem_ctrl_1.memoryStateTime::IDLE 1928898000 # Time in different power states
system.mem_ctrl_1.memoryStateTime::REF 67860000 # Time in different power states
system.mem_ctrl_1.memoryStateTime::PRE_PDN 0 # Time in different power states
system.mem_ctrl_1.memoryStateTime::ACT 38917000 # Time in different power states
system.mem_ctrl_1.memoryStateTime::ACT_PDN 0 # Time in different power states
system.cpu.branchPred.lookups 384817 # Number of BP lookups
system.cpu.branchPred.condPredicted 384817 # Number of conditional branches predicted
system.cpu.branchPred.condIncorrect 13834 # Number of conditional branches incorrect
system.cpu.branchPred.BTBLookups 259199 # Number of BTB lookups
system.cpu.branchPred.BTBHits 211774 # Number of BTB hits
system.cpu.branchPred.BTBCorrect 0 # Number of correct BTB predictions (this stat may not work properly.
system.cpu.branchPred.BTBHitPct 81.703247 # BTB Hit Percentage
system.cpu.branchPred.usedRAS 25636 # Number of times the RAS was used to get a target.
system.cpu.branchPred.RASInCorrect 120 # Number of incorrect RAS predictions.
system.cpu.apic_clk_domain.clock 8000 # Clock period in ticks
system.cpu.workload.num_syscalls 14 # Number of system calls
system.cpu.numCycles 4077298 # number of cpu cycles simulated
system.cpu.numWorkItemsStarted 0 # number of work items this cpu started
system.cpu.numWorkItemsCompleted 0 # number of work items this cpu completed
system.cpu.fetch.icacheStallCycles 2478357 # Number of cycles fetch is stalled on an Icache miss
system.cpu.fetch.Insts 1952689 # Number of instructions fetch has processed
system.cpu.fetch.Branches 384817 # Number of branches that fetch encountered
system.cpu.fetch.predictedBranches 237410 # Number of branches that fetch has predicted taken
system.cpu.fetch.Cycles 1557328 # Number of cycles fetch has run and was not squashing or blocked
system.cpu.fetch.SquashCycles 27875 # Number of cycles fetch has spent squashing
system.cpu.fetch.MiscStallCycles 39 # Number of cycles fetch has spent waiting on interrupts, or bad addresses, or out of MSHRs
system.cpu.fetch.PendingTrapStallCycles 602 # Number of stall cycles due to pending traps
system.cpu.fetch.PendingQuiesceStallCycles 13 # Number of stall cycles due to pending quiesce instructions
system.cpu.fetch.CacheLines 639002 # Number of cache lines fetched
system.cpu.fetch.IcacheSquashes 4786 # Number of outstanding Icache misses that were squashed
system.cpu.fetch.rateDist::samples 4050276 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::mean 0.883948 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::stdev 1.295076 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::underflows 0 0.00% 0.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::0 2654066 65.53% 65.53% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::1 217019 5.36% 70.89% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::2 174357 4.30% 75.19% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::3 1004834 24.81% 100.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::overflows 0 0.00% 100.00% # Number of instructions fetched each cycle

(Total)
system.cpu.fetch.rateDist::min_value 0 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::max_value 3 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::total 4050276 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.branchRate 0.094380 # Number of branch fetches per cycle
system.cpu.fetch.rate 0.478917 # Number of inst fetches per cycle
system.cpu.decode.IdleCycles 2501635 # Number of cycles decode is idle
system.cpu.decode.BlockedCycles 212376 # Number of cycles decode is blocked
system.cpu.decode.RunCycles 1279816 # Number of cycles decode is running
system.cpu.decode.UnblockCycles 42512 # Number of cycles decode is unblocking
system.cpu.decode.SquashCycles 13937 # Number of cycles decode is squashing
system.cpu.decode.DecodedInsts 3418136 # Number of instructions handled by decode
system.cpu.decode.SquashedInsts 34216 # Number of squashed instructions handled by decode
system.cpu.rename.SquashCycles 13937 # Number of cycles rename is squashing
system.cpu.rename.IdleCycles 2546948 # Number of cycles rename is idle
system.cpu.rename.BlockCycles 139758 # Number of cycles rename is blocking
system.cpu.rename.serializeStallCycles 492 # count of cycles rename stalled for serializing inst
system.cpu.rename.RunCycles 1268643 # Number of cycles rename is running
system.cpu.rename.UnblockCycles 80498 # Number of cycles rename is unblocking
system.cpu.rename.RenamedInsts 3373614 # Number of instructions processed by rename
system.cpu.rename.SquashedInsts 24518 # Number of squashed instructions processed by rename
system.cpu.rename.ROBFullEvents 55127 # Number of times rename has blocked due to ROB full
system.cpu.rename.IQFullEvents 4426 # Number of times rename has blocked due to IQ full
system.cpu.rename.SQFullEvents 9988 # Number of times rename has blocked due to SQ full
system.cpu.rename.RenamedOperands 4022107 # Number of destination operands rename has renamed
system.cpu.rename.RenameLookups 8688702 # Number of register rename lookups that rename has made
system.cpu.rename.int_rename_lookups 5000252 # Number of integer rename lookups
system.cpu.rename.fp_rename_lookups 156430 # Number of floating rename lookups
system.cpu.rename.CommittedMaps 3700162 # Number of HB maps that are committed
system.cpu.rename.UndoneMaps 321945 # Number of HB maps that are undone due to squashing
system.cpu.rename.serializingInsts 22 # count of serializing insts renamed
system.cpu.rename.tempSerializingInsts 22 # count of temporary serializing insts renamed
system.cpu.rename.skidInsts 109587 # count of insts added to the skid buffer
system.cpu.memDep0.insertedLoads 504168 # Number of loads inserted to the mem dependence unit.
system.cpu.memDep0.insertedStores 255194 # Number of stores inserted to the mem dependence unit.
system.cpu.memDep0.conflictingLoads 77508 # Number of conflicting loads.
system.cpu.memDep0.conflictingStores 14823 # Number of conflicting stores.
system.cpu.iq.iqInstsAdded 3354626 # Number of instructions added to the IQ (excludes non-spec)
system.cpu.iq.iqNonSpecInstsAdded 65 # Number of non-speculative instructions added to the IQ
system.cpu.iq.iqInstsIssued 3280126 # Number of instructions issued
system.cpu.iq.iqSquashedInstsIssued 4285 # Number of squashed instructions issued
system.cpu.iq.iqSquashedInstsExamined 234945 # Number of squashed instructions iterated over during squash; mainly for profiling
system.cpu.iq.iqSquashedOperandsExamined 284201 # Number of squashed operands that are

examined and possibly removed from graph
system.cpu.iq.iqSquashedNonSpecRemoved 50 # Number of squashed non-spec instructions that were removed
system.cpu.iq.issued_per_cycle::samples 4050276 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::mean 0.809852 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::stdev 0.998047 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::underflows 0 0.00% 0.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::0 2198431 54.28% 54.28% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::1 695121 17.16% 71.44% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::2 890711 21.99% 93.43% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::3 260469 6.43% 99.86% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::4 5544 0.14% 100.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::overflows 0 0.00% 100.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::min_value 0 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::max_value 4 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::total 4050276 # Number of insts issued each cycle
system.cpu.iq.fu_full::No_OpClass 0 0.00% 0.00% # attempts to use FU when none available
system.cpu.iq.fu_full::IntAlu 388323 71.46% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::IntMult 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::IntDiv 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatAdd 17 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatCmp 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatCvt 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatMult 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatDiv 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatSqrt 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAdd 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAddAcc 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAlu 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdCmp 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdCvt 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMisc 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMult 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMultAcc 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdShift 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdShiftAcc 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdSqrt 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatAdd 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatAlu 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatCmp 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatCvt 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatDiv 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMisc 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMult 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMultAcc 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatSqrt 0 0.00% 71.46% # attempts to use FU when none available
system.cpu.iq.fu_full::MemRead 114823 21.13% 92.59% # attempts to use FU when none available
system.cpu.iq.fu_full::MemWrite 40243 7.41% 100.00% # attempts to use FU when none available

system.cpu.iq.fu_full::IprAccess 0 0.00% 100.00% # attempts to use FU when none available
system.cpu.iq.fu_full::InstPrefetch 0 0.00% 100.00% # attempts to use FU when none available
system.cpu.iq.FU_type_0::No_OpClass 14203 0.43% 0.43% # Type of FU issued
system.cpu.iq.FU_type_0::IntAlu 2446485 74.59% 75.02% # Type of FU issued
system.cpu.iq.FU_type_0::IntMult 10674 0.33% 75.34% # Type of FU issued
system.cpu.iq.FU_type_0::IntDiv 28 0.00% 75.34% # Type of FU issued
system.cpu.iq.FU_type_0::FloatAdd 72186 2.20% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::FloatCmp 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::FloatCvt 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::FloatMult 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::FloatDiv 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::FloatSqrt 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAdd 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAddAcc 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAlu 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdCmp 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdCvt 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMisc 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMult 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMultAcc 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdShift 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdShiftAcc 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdSqrt 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatAdd 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatAlu 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatCmp 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatCvt 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatDiv 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMisc 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMult 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMultAcc 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatSqrt 0 0.00% 77.55% # Type of FU issued
system.cpu.iq.FU_type_0::MemRead 488736 14.90% 92.44% # Type of FU issued
system.cpu.iq.FU_type_0::MemWrite 247814 7.56% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::IprAccess 0 0.00% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::InstPrefetch 0 0.00% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::total 3280126 # Type of FU issued
system.cpu.iq.rate 0.804485 # Inst issue rate
system.cpu.iq.fu_busy_cnt 543406 # FU busy when requested
system.cpu.iq.fu_busy_rate 0.165666 # FU busy rate (busy events/executed inst)
system.cpu.iq.int_inst_queue_reads 10969662 # Number of integer instruction queue reads
system.cpu.iq.int_inst_queue_writes 3497347 # Number of integer instruction queue writes
system.cpu.iq.int_inst_queue_wakeup_accesses 3159697 # Number of integer instruction queue wakeup accesses
system.cpu.iq.fp_inst_queue_reads 188557 # Number of floating instruction queue reads
system.cpu.iq.fp_inst_queue_writes 92357 # Number of floating instruction queue writes
system.cpu.iq.fp_inst_queue_wakeup_accesses 92241 # Number of floating instruction queue wakeup accesses

system.cpu.iq.int_alu_accesses 3713029 # Number of integer alu accesses
system.cpu.iq.fp_alu_accesses 96300 # Number of floating point alu accesses
system.cpu.iew.lsq.thread0.forwLoads 36048 # Number of loads that had data forwarded from stores
system.cpu.iew.lsq.thread0.invAddrLoads 0 # Number of loads ignored due to an invalid address
system.cpu.iew.lsq.thread0.squashedLoads 57040 # Number of loads squashed
system.cpu.iew.lsq.thread0.ignoredResponses 59 # Number of memory responses ignored because the instruction is squashed
system.cpu.iew.lsq.thread0.memOrderViolation 68 # Number of memory ordering violations
system.cpu.iew.lsq.thread0.squashedStores 10067 # Number of stores squashed
system.cpu.iew.lsq.thread0.invAddrSwpfs 0 # Number of software prefetches ignored due to an invalid address
system.cpu.iew.lsq.thread0.blockedLoads 0 # Number of blocked loads due to partial load-store forwarding
system.cpu.iew.lsq.thread0.rescheduledLoads 1 # Number of loads that were rescheduled
system.cpu.iew.lsq.thread0.cacheBlocked 9 # Number of times an access to memory failed due to the cache being blocked
system.cpu.iew.iewIdleCycles 0 # Number of cycles IEW is idle
system.cpu.iew.iewSquashCycles 13937 # Number of cycles IEW is squashing
system.cpu.iew.iewBlockCycles 55065 # Number of cycles IEW is blocking
system.cpu.iew.iewUnblockCycles 4127 # Number of cycles IEW is unblocking
system.cpu.iew.iewDispatchedInsts 3354691 # Number of instructions dispatched to IQ
system.cpu.iew.iewDispSquashedInsts 0 # Number of squashed instructions skipped by dispatch
system.cpu.iew.iewDispLoadInsts 504168 # Number of dispatched load instructions
system.cpu.iew.iewDispStoreInsts 255194 # Number of dispatched store instructions
system.cpu.iew.iewDispNonSpecInsts 23 # Number of dispatched non-speculative instructions
system.cpu.iew.iewIQFullEvents 14 # Number of times the IQ has become full, causing a stall
system.cpu.iew.iewLSQFullEvents 4098 # Number of times the LSQ has become full, causing a stall
system.cpu.iew.memOrderViolationEvents 68 # Number of memory order violations
system.cpu.iew.predictedTakenIncorrect 8717 # Number of branches that were predicted taken incorrectly
system.cpu.iew.predictedNotTakenIncorrect 5510 # Number of branches that were predicted not taken incorrectly
system.cpu.iew.branchMispredicts 14227 # Number of branch mispredicts detected at execute
system.cpu.iew.iewExecutedInsts 3263180 # Number of executed instructions
system.cpu.iew.iewExecLoadInsts 481721 # Number of load instructions executed
system.cpu.iew.iewExecSquashedInsts 16946 # Number of squashed instructions skipped in execute
system.cpu.iew.exec_swp 0 # number of swp insts executed
system.cpu.iew.exec_nop 0 # number of nop insts executed
system.cpu.iew.exec_refs 728401 # number of memory reference insts executed
system.cpu.iew.exec_branches 352678 # Number of branches executed
system.cpu.iew.exec_stores 246680 # Number of stores executed
system.cpu.iew.exec_rate 0.800329 # Inst execution rate
system.cpu.iew.wb_sent 3254593 # cumulative count of insts sent to commit
system.cpu.iew.wb_count 3251938 # cumulative count of insts written-back
system.cpu.iew.wb_producers 2247993 # num instructions producing a value
system.cpu.iew.wb_consumers 3450837 # num instructions consuming a value
system.cpu.iew.wb_penalized 0 # number of instrctions required to write to 'other' IQ

system.cpu.iew.wb_rate 0.797572 # insts written-back per cycle
system.cpu.iew.wb_fanout 0.651434 # average fanout of values written-back
system.cpu.iew.wb_penalized_rate 0 # fraction of instructions written-back that wrote to 'other' IQ
system.cpu.commit.commitSquashedInsts 214330 # The number of squashed insts skipped by commit
system.cpu.commit.commitNonSpecStalls 15 # The number of times commit has been forced to stall to communicate backwards
system.cpu.commit.branchMispredicts 13872 # The number of times a branch was mispredicted
system.cpu.commit.committed_per_cycle::samples 3987916 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::mean 0.782300 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::stdev 1.250460 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::underflows 0 0.00% 0.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::0 2516927 63.11% 63.11% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::1 637695 15.99% 79.10% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::2 331878 8.32% 87.43% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::3 187369 4.70% 92.13% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::4 314047 7.87% 100.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::overflows 0 0.00% 100.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::min_value 0 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::max_value 4 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::total 3987916 # Number of insts commited each cycle
system.cpu.commit.committedInsts 1680562 # Number of instructions committed
system.cpu.commit.committedOps 3119746 # Number of ops (including micro ops) committed
system.cpu.commit.swp_count 0 # Number of s/w prefetches committed
system.cpu.commit.refs 692255 # Number of memory references committed
system.cpu.commit.loads 447128 # Number of loads committed
system.cpu.commit.membars 0 # Number of memory barriers committed
system.cpu.commit.branches 336284 # Number of branches committed
system.cpu.commit.fp_insts 92175 # Number of committed floating point instructions.
system.cpu.commit.int_insts 3034698 # Number of committed integer instructions.
system.cpu.commit.function_calls 24008 # Number of function calls committed.
system.cpu.commit.op_class_0::No_OpClass 14063 0.45% 0.45% # Class of committed instruction
system.cpu.commit.op_class_0::IntAlu 2330593 74.70% 75.16% # Class of committed instruction
system.cpu.commit.op_class_0::IntMult 10673 0.34% 75.50% # Class of committed instruction
system.cpu.commit.op_class_0::IntDiv 28 0.00% 75.50% # Class of committed instruction
system.cpu.commit.op_class_0::FloatAdd 72134 2.31% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::FloatCmp 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::FloatCvt 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::FloatMult 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::FloatDiv 0 0.00% 77.81% # Class of committed instruction

system.cpu.commit.op_class_0::FloatSqrt 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAdd 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAddAcc 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAlu 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdCmp 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdCvt 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMisc 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMult 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMultAcc 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdShift 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdShiftAcc 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdSqrt 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatAdd 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatAlu 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatCmp 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatCvt 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatDiv 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMisc 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMult 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMultAcc 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatSqrt 0 0.00% 77.81% # Class of committed instruction
system.cpu.commit.op_class_0::MemRead 447128 14.33% 92.14% # Class of committed instruction
system.cpu.commit.op_class_0::MemWrite 245127 7.86% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::IprAccess 0 0.00% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::InstPrefetch 0 0.00% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::total 3119746 # Class of committed instruction
system.cpu.commit.bw_lim_events 314047 # number cycles where commit BW limit reached
system.cpu.rob.rob_reads 7007945 # The number of ROB reads
system.cpu.rob.rob_writes 6730621 # The number of ROB writes
system.cpu.timesIdled 352 # Number of times that the entire CPU went into an idle state and unscheduled itself
system.cpu.idleCycles 27022 # Total number of cycles that the CPU has spent unscheduled due to idling
system.cpu.committedInsts 1680562 # Number of Instructions Simulated
system.cpu.committedOps 3119746 # Number of Ops (including micro ops) Simulated
system.cpu.cpi 2.426151 # CPI: Cycles Per Instruction
system.cpu.cpi_total 2.426151 # CPI: Total CPI of All Threads
system.cpu.ipc 0.412175 # IPC: Instructions Per Cycle
system.cpu.ipc_total 0.412175 # IPC: Total IPC of All Threads
system.cpu.int_regfile_reads 4798684 # number of integer regfile reads
system.cpu.int_regfile_writes 2572254 # number of integer regfile writes
system.cpu.fp_regfile_reads 156385 # number of floating regfile reads
system.cpu.fp_regfile_writes 76193 # number of floating regfile writes
system.cpu.cc_regfile_reads 1992762 # number of cc regfile reads
system.cpu.cc_regfile_writes 1208301 # number of cc regfile writes
system.cpu.misc_regfile_reads 1428155 # number of misc regfile reads
system.cpu.misc_regfile_writes 1 # number of misc regfile writes
system.cpu.dcache.tags.replacements 758 # number of replacements

system.cpu.dcache.tags.tagsinuse 63.880949 # Cycle average of tags in use
system.cpu.dcache.tags.total_refs 689790 # Total number of references to valid blocks.
system.cpu.dcache.tags.sampled_refs 822 # Sample count of references to valid blocks.
system.cpu.dcache.tags.avg_refs 839.160584 # Average number of references to valid blocks.
system.cpu.dcache.tags.warmup_cycle 9414250 # Cycle when the warmup percentage was hit.
system.cpu.dcache.tags.occ_blocks::cpu.data 63.880949 # Average occupied blocks per requestor
system.cpu.dcache.tags.occ_percent::cpu.data 0.998140 # Average percentage of cache occupancy
system.cpu.dcache.tags.occ_percent::total 0.998140 # Average percentage of cache occupancy
system.cpu.dcache.tags.occ_task_id_blocks::1024 64 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::0 32 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::1 4 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::2 21 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::3 7 # Occupied blocks per task id
system.cpu.dcache.tags.occ_task_id_percent::1024 1 # Percentage of cache occupancy per task id
system.cpu.dcache.tags.tag_accesses 11052966 # Number of tag accesses
system.cpu.dcache.tags.data_accesses 11052966 # Number of data accesses
system.cpu.dcache.ReadReq_hits::cpu.data 445106 # number of ReadReq hits
system.cpu.dcache.ReadReq_hits::total 445106 # number of ReadReq hits
system.cpu.dcache.WriteReq_hits::cpu.data 244684 # number of WriteReq hits
system.cpu.dcache.WriteReq_hits::total 244684 # number of WriteReq hits
system.cpu.dcache.demand_hits::cpu.data 689790 # number of demand (read+write) hits
system.cpu.dcache.demand_hits::total 689790 # number of demand (read+write) hits
system.cpu.dcache.overall_hits::cpu.data 689790 # number of overall hits
system.cpu.dcache.overall_hits::total 689790 # number of overall hits
system.cpu.dcache.ReadReq_misses::cpu.data 526 # number of ReadReq misses
system.cpu.dcache.ReadReq_misses::total 526 # number of ReadReq misses
system.cpu.dcache.WriteReq_misses::cpu.data 443 # number of WriteReq misses
system.cpu.dcache.WriteReq_misses::total 443 # number of WriteReq misses
system.cpu.dcache.demand_misses::cpu.data 969 # number of demand (read+write) misses
system.cpu.dcache.demand_misses::total 969 # number of demand (read+write) misses
system.cpu.dcache.overall_misses::cpu.data 969 # number of overall misses
system.cpu.dcache.overall_misses::total 969 # number of overall misses
system.cpu.dcache.ReadReq_miss_latency::cpu.data 15943750 # number of ReadReq miss cycles
system.cpu.dcache.ReadReq_miss_latency::total 15943750 # number of ReadReq miss cycles
system.cpu.dcache.WriteReq_miss_latency::cpu.data 21727500 # number of WriteReq miss cycles
system.cpu.dcache.WriteReq_miss_latency::total 21727500 # number of WriteReq miss cycles
system.cpu.dcache.demand_miss_latency::cpu.data 37671250 # number of demand (read+write) miss cycles
system.cpu.dcache.demand_miss_latency::total 37671250 # number of demand (read+write) miss cycles
system.cpu.dcache.overall_miss_latency::cpu.data 37671250 # number of overall miss cycles
system.cpu.dcache.overall_miss_latency::total 37671250 # number of overall miss cycles
system.cpu.dcache.ReadReq_accesses::cpu.data 445632 # number of ReadReq accesses(hits+misses)
system.cpu.dcache.ReadReq_accesses::total 445632 # number of ReadReq accesses(hits+misses)
system.cpu.dcache.WriteReq_accesses::cpu.data 245127 # number of WriteReq accesses(hits+misses)
system.cpu.dcache.WriteReq_accesses::total 245127 # number of WriteReq accesses(hits+misses)

system.cpu.dcache.demand_accesses::cpu.data 690759 # number of demand (read+write) accesses
system.cpu.dcache.demand_accesses::total 690759 # number of demand (read+write) accesses
system.cpu.dcache.overall_accesses::cpu.data 690759 # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total 690759 # number of overall (read+write) accesses
system.cpu.dcache.ReadReq_miss_rate::cpu.data 0.001180 # miss rate for ReadReq accesses
system.cpu.dcache.ReadReq_miss_rate::total 0.001180 # miss rate for ReadReq accesses
system.cpu.dcache.WriteReq_miss_rate::cpu.data 0.001807 # miss rate for WriteReq accesses
system.cpu.dcache.WriteReq_miss_rate::total 0.001807 # miss rate for WriteReq accesses
system.cpu.dcache.demand_miss_rate::cpu.data 0.001403 # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total 0.001403 # miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data 0.001403 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.001403 # miss rate for overall accesses
system.cpu.dcache.ReadReq_avg_miss_latency::cpu.data 30311.311787 # average ReadReq miss latency
system.cpu.dcache.ReadReq_avg_miss_latency::total 30311.311787 # average ReadReq miss latency
system.cpu.dcache.WriteReq_avg_miss_latency::cpu.data 49046.275395 # average WriteReq miss latency
system.cpu.dcache.WriteReq_avg_miss_latency::total 49046.275395 # average WriteReq miss latency
system.cpu.dcache.demand_avg_miss_latency::cpu.data 38876.418989 # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total 38876.418989 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data 38876.418989 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total 38876.418989 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 229 # number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs 6 # number of cycles access was blocked
system.cpu.dcache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs 38.166667 # average number of cycles each access was blocked
system.cpu.dcache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.dcache.fast_writes 0 # number of fast writes performed
system.cpu.dcache.cache_copies 0 # number of cache copies performed
system.cpu.dcache.writebacks::writebacks 685 # number of writebacks
system.cpu.dcache.writebacks::total 685 # number of writebacks
system.cpu.dcache.ReadReq_mshr_hits::cpu.data 145 # number of ReadReq MSHR hits
system.cpu.dcache.ReadReq_mshr_hits::total 145 # number of ReadReq MSHR hits
system.cpu.dcache.WriteReq_mshr_hits::cpu.data 2 # number of WriteReq MSHR hits
system.cpu.dcache.WriteReq_mshr_hits::total 2 # number of WriteReq MSHR hits
system.cpu.dcache.demand_mshr_hits::cpu.data 147 # number of demand (read+write) MSHR hits
system.cpu.dcache.demand_mshr_hits::total 147 # number of demand (read+write) MSHR hits
system.cpu.dcache.overall_mshr_hits::cpu.data 147 # number of overall MSHR hits
system.cpu.dcache.overall_mshr_hits::total 147 # number of overall MSHR hits
system.cpu.dcache.ReadReq_mshr_misses::cpu.data 381 # number of ReadReq MSHR misses
system.cpu.dcache.ReadReq_mshr_misses::total 381 # number of ReadReq MSHR misses

system.cpu.dcache.WriteReq_mshr_misses::cpu.data 441 # number of WriteReq MSHR misses
system.cpu.dcache.WriteReq_mshr_misses::total 441 # number of WriteReq MSHR misses
system.cpu.dcache.demand_mshr_misses::cpu.data 822 # number of demand (read+write) MSHR misses
system.cpu.dcache.demand_mshr_misses::total 822 # number of demand (read+write) MSHR misses
system.cpu.dcache.overall_mshr_misses::cpu.data 822 # number of overall MSHR misses
system.cpu.dcache.overall_mshr_misses::total 822 # number of overall MSHR misses
system.cpu.dcache.ReadReq_mshr_miss_latency::cpu.data 10817000 # number of ReadReq MSHR miss cycles
system.cpu.dcache.ReadReq_mshr_miss_latency::total 10817000 # number of ReadReq MSHR miss cycles
system.cpu.dcache.WriteReq_mshr_miss_latency::cpu.data 20972500 # number of WriteReq MSHR miss cycles
system.cpu.dcache.WriteReq_mshr_miss_latency::total 20972500 # number of WriteReq MSHR miss cycles
system.cpu.dcache.demand_mshr_miss_latency::cpu.data 31789500 # number of demand (read+write) MSHR miss cycles
system.cpu.dcache.demand_mshr_miss_latency::total 31789500 # number of demand (read+write) MSHR miss cycles
system.cpu.dcache.overall_mshr_miss_latency::cpu.data 31789500 # number of overall MSHR miss cycles
system.cpu.dcache.overall_mshr_miss_latency::total 31789500 # number of overall MSHR miss cycles
system.cpu.dcache.ReadReq_mshr_miss_rate::cpu.data 0.000855 # mshr miss rate for ReadReq accesses
system.cpu.dcache.ReadReq_mshr_miss_rate::total 0.000855 # mshr miss rate for ReadReq accesses
system.cpu.dcache.WriteReq_mshr_miss_rate::cpu.data 0.001799 # mshr miss rate for WriteReq accesses
system.cpu.dcache.WriteReq_mshr_miss_rate::total 0.001799 # mshr miss rate for WriteReq accesses
system.cpu.dcache.demand_mshr_miss_rate::cpu.data 0.001190 # mshr miss rate for demand accesses
system.cpu.dcache.demand_mshr_miss_rate::total 0.001190 # mshr miss rate for demand accesses
system.cpu.dcache.overall_mshr_miss_rate::cpu.data 0.001190 # mshr miss rate for overall accesses
system.cpu.dcache.overall_mshr_miss_rate::total 0.001190 # mshr miss rate for overall accesses
system.cpu.dcache.ReadReq_avg_mshr_miss_latency::cpu.data 28391.076115 # average ReadReq mshr miss latency
system.cpu.dcache.ReadReq_avg_mshr_miss_latency::total 28391.076115 # average ReadReq mshr miss latency
system.cpu.dcache.WriteReq_avg_mshr_miss_latency::cpu.data 47556.689342 # average WriteReq mshr miss latency
system.cpu.dcache.WriteReq_avg_mshr_miss_latency::total 47556.689342 # average WriteReq mshr miss latency
system.cpu.dcache.demand_avg_mshr_miss_latency::cpu.data 38673.357664 # average overall mshr miss latency

system.cpu.dcache.demand_avg_mshr_miss_latency::total 38673.357664 # average overall mshr miss latency
system.cpu.dcache.overall_avg_mshr_miss_latency::cpu.data 38673.357664 # average overall mshr miss latency
system.cpu.dcache.overall_avg_mshr_miss_latency::total 38673.357664 # average overall mshr miss latency
system.cpu.dcache.no_allocate_misses 0 # Number of misses that were no-allocate
system.cpu.icache.tags.replacements 70628 # number of replacements
system.cpu.icache.tags.tagsinuse 63.884764 # Cycle average of tags in use
system.cpu.icache.tags.total_refs 567121 # Total number of references to valid blocks.
system.cpu.icache.tags.sampled_refs 70692 # Sample count of references to valid blocks.
system.cpu.icache.tags.avg_refs 8.022421 # Average number of references to valid blocks.
system.cpu.icache.tags.warmup_cycle 12833250 # Cycle when the warmup percentage was hit.
system.cpu.icache.tags.occ_blocks::cpu.inst 63.884764 # Average occupied blocks per requestor
system.cpu.icache.tags.occ_percent::cpu.inst 0.998199 # Average percentage of cache occupancy
system.cpu.icache.tags.occ_percent::total 0.998199 # Average percentage of cache occupancy
system.cpu.icache.tags.occ_task_id_blocks::1024 64 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::0 58 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::2 3 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::3 3 # Occupied blocks per task id
system.cpu.icache.tags.occ_task_id_percent::1024 1 # Percentage of cache occupancy per task id
system.cpu.icache.tags.tag_accesses 1348696 # Number of tag accesses
system.cpu.icache.tags.data_accesses 1348696 # Number of data accesses
system.cpu.icache.ReadReq_hits::cpu.inst 567121 # number of ReadReq hits
system.cpu.icache.ReadReq_hits::total 567121 # number of ReadReq hits
system.cpu.icache.demand_hits::cpu.inst 567121 # number of demand (read+write) hits
system.cpu.icache.demand_hits::total 567121 # number of demand (read+write) hits
system.cpu.icache.overall_hits::cpu.inst 567121 # number of overall hits
system.cpu.icache.overall_hits::total 567121 # number of overall hits
system.cpu.icache.ReadReq_misses::cpu.inst 71881 # number of ReadReq misses
system.cpu.icache.ReadReq_misses::total 71881 # number of ReadReq misses
system.cpu.icache.demand_misses::cpu.inst 71881 # number of demand (read+write) misses
system.cpu.icache.demand_misses::total 71881 # number of demand (read+write) misses
system.cpu.icache.overall_misses::cpu.inst 71881 # number of overall misses
system.cpu.icache.overall_misses::total 71881 # number of overall misses
system.cpu.icache.ReadReq_miss_latency::cpu.inst 1023909498 # number of ReadReq miss cycles
system.cpu.icache.ReadReq_miss_latency::total 1023909498 # number of ReadReq miss cycles
system.cpu.icache.demand_miss_latency::cpu.inst 1023909498 # number of demand (read+write) miss cycles
system.cpu.icache.demand_miss_latency::total 1023909498 # number of demand (read+write) miss cycles
system.cpu.icache.overall_miss_latency::cpu.inst 1023909498 # number of overall miss cycles
system.cpu.icache.overall_miss_latency::total 1023909498 # number of overall miss cycles
system.cpu.icache.ReadReq_accesses::cpu.inst 639002 # number of ReadReq accesses(hits+misses)
system.cpu.icache.ReadReq_accesses::total 639002 # number of ReadReq accesses(hits+misses)
system.cpu.icache.demand_accesses::cpu.inst 639002 # number of demand (read+write) accesses
system.cpu.icache.demand_accesses::total 639002 # number of demand (read+write) accesses
system.cpu.icache.overall_accesses::cpu.inst 639002 # number of overall (read+write) accesses

system.cpu.icache.overall_accesses::total 639002 # number of overall (read+write) accesses
system.cpu.icache.ReadReq_miss_rate::cpu.inst 0.112489 # miss rate for ReadReq accesses
system.cpu.icache.ReadReq_miss_rate::total 0.112489 # miss rate for ReadReq accesses
system.cpu.icache.demand_miss_rate::cpu.inst 0.112489 # miss rate for demand accesses
system.cpu.icache.demand_miss_rate::total 0.112489 # miss rate for demand accesses
system.cpu.icache.overall_miss_rate::cpu.inst 0.112489 # miss rate for overall accesses
system.cpu.icache.overall_miss_rate::total 0.112489 # miss rate for overall accesses
system.cpu.icache.ReadReq_avg_miss_latency::cpu.inst 14244.508257 # average ReadReq miss latency
system.cpu.icache.ReadReq_avg_miss_latency::total 14244.508257 # average ReadReq miss latency
system.cpu.icache.demand_avg_miss_latency::cpu.inst 14244.508257 # average overall miss latency
system.cpu.icache.demand_avg_miss_latency::total 14244.508257 # average overall miss latency
system.cpu.icache.overall_avg_miss_latency::cpu.inst 14244.508257 # average overall miss latency
system.cpu.icache.overall_avg_miss_latency::total 14244.508257 # average overall miss latency
system.cpu.icache.blocked_cycles::no_mshrs 32 # number of cycles access was blocked
system.cpu.icache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.icache.blocked::no_mshrs 1 # number of cycles access was blocked
system.cpu.icache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.icache.avg_blocked_cycles::no_mshrs 32 # average number of cycles each access was blocked
system.cpu.icache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.icache.fast_writes 0 # number of fast writes performed
system.cpu.icache.cache_copies 0 # number of cache copies performed
system.cpu.icache.ReadReq_mshr_hits::cpu.inst 1188 # number of ReadReq MSHR hits
system.cpu.icache.ReadReq_mshr_hits::total 1188 # number of ReadReq MSHR hits
system.cpu.icache.demand_mshr_hits::cpu.inst 1188 # number of demand (read+write) MSHR hits
system.cpu.icache.demand_mshr_hits::total 1188 # number of demand (read+write) MSHR hits
system.cpu.icache.overall_mshr_hits::cpu.inst 1188 # number of overall MSHR hits
system.cpu.icache.overall_mshr_hits::total 1188 # number of overall MSHR hits
system.cpu.icache.ReadReq_mshr_misses::cpu.inst 70693 # number of ReadReq MSHR misses
system.cpu.icache.ReadReq_mshr_misses::total 70693 # number of ReadReq MSHR misses
system.cpu.icache.demand_mshr_misses::cpu.inst 70693 # number of demand (read+write) MSHR misses
system.cpu.icache.demand_mshr_misses::total 70693 # number of demand (read+write) MSHR misses
system.cpu.icache.overall_mshr_misses::cpu.inst 70693 # number of overall MSHR misses
system.cpu.icache.overall_mshr_misses::total 70693 # number of overall MSHR misses
system.cpu.icache.ReadReq_mshr_miss_latency::cpu.inst 907514752 # number of ReadReq MSHR miss cycles
system.cpu.icache.ReadReq_mshr_miss_latency::total 907514752 # number of ReadReq MSHR miss cycles
system.cpu.icache.demand_mshr_miss_latency::cpu.inst 907514752 # number of demand (read+write) MSHR miss cycles
system.cpu.icache.demand_mshr_miss_latency::total 907514752 # number of demand (read+write) MSHR miss cycles
system.cpu.icache.overall_mshr_miss_latency::cpu.inst 907514752 # number of overall MSHR miss

cycles
system.cpu.icache.overall_mshr_miss_latency::total 907514752 # number of overall MSHR miss cycles
system.cpu.icache.ReadReq_mshr_miss_rate::cpu.inst 0.110630 # mshr miss rate for ReadReq accesses
system.cpu.icache.ReadReq_mshr_miss_rate::total 0.110630 # mshr miss rate for ReadReq accesses
system.cpu.icache.demand_mshr_miss_rate::cpu.inst 0.110630 # mshr miss rate for demand accesses
system.cpu.icache.demand_mshr_miss_rate::total 0.110630 # mshr miss rate for demand accesses
system.cpu.icache.overall_mshr_miss_rate::cpu.inst 0.110630 # mshr miss rate for overall accesses
system.cpu.icache.overall_mshr_miss_rate::total 0.110630 # mshr miss rate for overall accesses
system.cpu.icache.ReadReq_avg_mshr_miss_latency::cpu.inst 12837.406136 # average ReadReq mshr miss latency
system.cpu.icache.ReadReq_avg_mshr_miss_latency::total 12837.406136 # average ReadReq mshr miss latency
system.cpu.icache.demand_avg_mshr_miss_latency::cpu.inst 12837.406136 # average overall mshr miss latency
system.cpu.icache.demand_avg_mshr_miss_latency::total 12837.406136 # average overall mshr miss latency
system.cpu.icache.overall_avg_mshr_miss_latency::cpu.inst 12837.406136 # average overall mshr miss latency
system.cpu.icache.overall_avg_mshr_miss_latency::total 12837.406136 # average overall mshr miss latency
system.cpu.icache.no_allocate_misses 0 # Number of misses that were no-allocate
system.cpu.l2cache.tags.replacements 0 # number of replacements
system.cpu.l2cache.tags.tagsinuse 639.461143 # Cycle average of tags in use
system.cpu.l2cache.tags.total_refs 70966 # Total number of references to valid blocks.
system.cpu.l2cache.tags.sampled_refs 762 # Sample count of references to valid blocks.
system.cpu.l2cache.tags.avg_refs 93.131234 # Average number of references to valid blocks.
system.cpu.l2cache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.l2cache.tags.occ_blocks::writebacks 200.200481 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_blocks::cpu.inst 363.036109 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_blocks::cpu.data 76.224553 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_percent::writebacks 0.048877 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::cpu.inst 0.088632 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::cpu.data 0.018610 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::total 0.156118 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_task_id_blocks::1024 762 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::0 93 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::1 11 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::2 73 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::3 585 # Occupied blocks per task id
system.cpu.l2cache.tags.occ_task_id_percent::1024 0.186035 # Percentage of cache occupancy per task id
system.cpu.l2cache.tags.tag_accesses 290003 # Number of tag accesses
system.cpu.l2cache.tags.data_accesses 290003 # Number of data accesses

system.cpu.l2cache.ReadReq_hits::cpu.inst 70256 # number of ReadReq hits
system.cpu.l2cache.ReadReq_hits::cpu.data 291 # number of ReadReq hits
system.cpu.l2cache.ReadReq_hits::total 70547 # number of ReadReq hits
system.cpu.l2cache.Writeback_hits::writebacks 685 # number of Writeback hits
system.cpu.l2cache.Writeback_hits::total 685 # number of Writeback hits
system.cpu.l2cache.ReadExReq_hits::cpu.data 189 # number of ReadExReq hits
system.cpu.l2cache.ReadExReq_hits::total 189 # number of ReadExReq hits
system.cpu.l2cache.demand_hits::cpu.inst 70256 # number of demand (read+write) hits
system.cpu.l2cache.demand_hits::cpu.data 480 # number of demand (read+write) hits
system.cpu.l2cache.demand_hits::total 70736 # number of demand (read+write) hits
system.cpu.l2cache.overall_hits::cpu.inst 70256 # number of overall hits
system.cpu.l2cache.overall_hits::cpu.data 480 # number of overall hits
system.cpu.l2cache.overall_hits::total 70736 # number of overall hits
system.cpu.l2cache.ReadReq_misses::cpu.inst 437 # number of ReadReq misses
system.cpu.l2cache.ReadReq_misses::cpu.data 90 # number of ReadReq misses
system.cpu.l2cache.ReadReq_misses::total 527 # number of ReadReq misses
system.cpu.l2cache.ReadExReq_misses::cpu.data 252 # number of ReadExReq misses
system.cpu.l2cache.ReadExReq_misses::total 252 # number of ReadExReq misses
system.cpu.l2cache.demand_misses::cpu.inst 437 # number of demand (read+write) misses
system.cpu.l2cache.demand_misses::cpu.data 342 # number of demand (read+write) misses
system.cpu.l2cache.demand_misses::total 779 # number of demand (read+write) misses
system.cpu.l2cache.overall_misses::cpu.inst 437 # number of overall misses
system.cpu.l2cache.overall_misses::cpu.data 342 # number of overall misses
system.cpu.l2cache.overall_misses::total 779 # number of overall misses
system.cpu.l2cache.ReadReq_miss_latency::cpu.inst 28855250 # number of ReadReq miss cycles
system.cpu.l2cache.ReadReq_miss_latency::cpu.data 6692500 # number of ReadReq miss cycles
system.cpu.l2cache.ReadReq_miss_latency::total 35547750 # number of ReadReq miss cycles
system.cpu.l2cache.ReadExReq_miss_latency::cpu.data 17910000 # number of ReadExReq miss cycles
system.cpu.l2cache.ReadExReq_miss_latency::total 17910000 # number of ReadExReq miss cycles
system.cpu.l2cache.demand_miss_latency::cpu.inst 28855250 # number of demand (read+write) miss cycles
system.cpu.l2cache.demand_miss_latency::cpu.data 24602500 # number of demand (read+write) miss cycles
system.cpu.l2cache.demand_miss_latency::total 53457750 # number of demand (read+write) miss cycles
system.cpu.l2cache.overall_miss_latency::cpu.inst 28855250 # number of overall miss cycles
system.cpu.l2cache.overall_miss_latency::cpu.data 24602500 # number of overall miss cycles
system.cpu.l2cache.overall_miss_latency::total 53457750 # number of overall miss cycles
system.cpu.l2cache.ReadReq_accesses::cpu.inst 70693 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.ReadReq_accesses::cpu.data 381 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.ReadReq_accesses::total 71074 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.Writeback_accesses::writebacks 685 # number of Writeback accesses(hits+misses)
system.cpu.l2cache.Writeback_accesses::total 685 # number of Writeback accesses(hits+misses)
system.cpu.l2cache.ReadExReq_accesses::cpu.data 441 # number of ReadExReq accesses(hits+misses)
system.cpu.l2cache.ReadExReq_accesses::total 441 # number of ReadExReq accesses(hits+misses)

system.cpu.l2cache.demand_accesses::cpu.inst 70693 # number of demand (read+write) accesses
system.cpu.l2cache.demand_accesses::cpu.data 822 # number of demand (read+write) accesses
system.cpu.l2cache.demand_accesses::total 71515 # number of demand (read+write) accesses
system.cpu.l2cache.overall_accesses::cpu.inst 70693 # number of overall (read+write) accesses
system.cpu.l2cache.overall_accesses::cpu.data 822 # number of overall (read+write) accesses
system.cpu.l2cache.overall_accesses::total 71515 # number of overall (read+write) accesses
system.cpu.l2cache.ReadReq_miss_rate::cpu.inst 0.006182 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_miss_rate::cpu.data 0.236220 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_miss_rate::total 0.007415 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadExReq_miss_rate::cpu.data 0.571429 # miss rate for ReadExReq accesses
system.cpu.l2cache.ReadExReq_miss_rate::total 0.571429 # miss rate for ReadExReq accesses
system.cpu.l2cache.demand_miss_rate::cpu.inst 0.006182 # miss rate for demand accesses
system.cpu.l2cache.demand_miss_rate::cpu.data 0.416058 # miss rate for demand accesses
system.cpu.l2cache.demand_miss_rate::total 0.010893 # miss rate for demand accesses
system.cpu.l2cache.overall_miss_rate::cpu.inst 0.006182 # miss rate for overall accesses
system.cpu.l2cache.overall_miss_rate::cpu.data 0.416058 # miss rate for overall accesses
system.cpu.l2cache.overall_miss_rate::total 0.010893 # miss rate for overall accesses
system.cpu.l2cache.ReadReq_avg_miss_latency::cpu.inst 66030.320366 # average ReadReq miss latency
system.cpu.l2cache.ReadReq_avg_miss_latency::cpu.data 74361.111111 # average ReadReq miss latency
system.cpu.l2cache.ReadReq_avg_miss_latency::total 67453.036053 # average ReadReq miss latency
system.cpu.l2cache.ReadExReq_avg_miss_latency::cpu.data 71071.428571 # average ReadExReq miss latency
system.cpu.l2cache.ReadExReq_avg_miss_latency::total 71071.428571 # average ReadExReq miss latency
system.cpu.l2cache.demand_avg_miss_latency::cpu.inst 66030.320366 # average overall miss latency
system.cpu.l2cache.demand_avg_miss_latency::cpu.data 71937.134503 # average overall miss latency
system.cpu.l2cache.demand_avg_miss_latency::total 68623.555841 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::cpu.inst 66030.320366 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::cpu.data 71937.134503 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::total 68623.555841 # average overall miss latency
system.cpu.l2cache.blocked_cycles::no_mshrs 0 # number of cycles access was blocked
system.cpu.l2cache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.l2cache.blocked::no_mshrs 0 # number of cycles access was blocked
system.cpu.l2cache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.l2cache.avg_blocked_cycles::no_mshrs nan # average number of cycles each access was blocked
system.cpu.l2cache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.l2cache.fast_writes 0 # number of fast writes performed
system.cpu.l2cache.cache_copies 0 # number of cache copies performed
system.cpu.l2cache.ReadReq_mshr_misses::cpu.inst 437 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadReq_mshr_misses::cpu.data 90 # number of ReadReq MSHR misses

system.cpu.l2cache.ReadReq_mshr_misses::total 527 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadExReq_mshr_misses::cpu.data 252 # number of ReadExReq MSHR misses
system.cpu.l2cache.ReadExReq_mshr_misses::total 252 # number of ReadExReq MSHR misses
system.cpu.l2cache.demand_mshr_misses::cpu.inst 437 # number of demand (read+write) MSHR misses
system.cpu.l2cache.demand_mshr_misses::cpu.data 342 # number of demand (read+write) MSHR misses
system.cpu.l2cache.demand_mshr_misses::total 779 # number of demand (read+write) MSHR misses
system.cpu.l2cache.overall_mshr_misses::cpu.inst 437 # number of overall MSHR misses
system.cpu.l2cache.overall_mshr_misses::cpu.data 342 # number of overall MSHR misses
system.cpu.l2cache.overall_mshr_misses::total 779 # number of overall MSHR misses
system.cpu.l2cache.ReadReq_mshr_miss_latency::cpu.inst 26484750 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_latency::cpu.data 6209500 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_latency::total 32694250 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadExReq_mshr_miss_latency::cpu.data 16581000 # number of ReadExReq MSHR miss cycles
system.cpu.l2cache.ReadExReq_mshr_miss_latency::total 16581000 # number of ReadExReq MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::cpu.inst 26484750 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::cpu.data 22790500 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::total 49275250 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::cpu.inst 26484750 # number of overall MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::cpu.data 22790500 # number of overall MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::total 49275250 # number of overall MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_rate::cpu.inst 0.006182 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_mshr_miss_rate::cpu.data 0.236220 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_mshr_miss_rate::total 0.007415 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadExReq_mshr_miss_rate::cpu.data 0.571429 # mshr miss rate for ReadExReq accesses
system.cpu.l2cache.ReadExReq_mshr_miss_rate::total 0.571429 # mshr miss rate for ReadExReq accesses
system.cpu.l2cache.demand_mshr_miss_rate::cpu.inst 0.006182 # mshr miss rate for demand accesses
system.cpu.l2cache.demand_mshr_miss_rate::cpu.data 0.416058 # mshr miss rate for demand accesses

system.cpu.l2cache.demand_mshr_miss_rate::total 0.010893 # mshr miss rate for demand accesses
system.cpu.l2cache.overall_mshr_miss_rate::cpu.inst 0.006182 # mshr miss rate for overall accesses
system.cpu.l2cache.overall_mshr_miss_rate::cpu.data 0.416058 # mshr miss rate for overall accesses
system.cpu.l2cache.overall_mshr_miss_rate::total 0.010893 # mshr miss rate for overall accesses
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::cpu.inst 60605.835240 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::cpu.data 68994.444444 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::total 62038.425047 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadExReq_avg_mshr_miss_latency::cpu.data 65797.619048 # average ReadExReq mshr miss latency
system.cpu.l2cache.ReadExReq_avg_mshr_miss_latency::total 65797.619048 # average ReadExReq mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::cpu.inst 60605.835240 # average overall mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::cpu.data 66638.888889 # average overall mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::total 63254.492940 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::cpu.inst 60605.835240 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::cpu.data 66638.888889 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::total 63254.492940 # average overall mshr miss latency
system.cpu.l2cache.no_allocate_misses 0 # Number of misses that were no-allocate
system.l2bus.trans_dist::ReadReq 71074 # Transaction distribution
system.l2bus.trans_dist::ReadResp 71073 # Transaction distribution
system.l2bus.trans_dist::Writeback 685 # Transaction distribution
system.l2bus.trans_dist::ReadExReq 441 # Transaction distribution
system.l2bus.trans_dist::ReadExResp 441 # Transaction distribution
system.l2bus.pkt_count_system.cpu.icache.mem_side::system.cpu.l2cache.cpu_side 141385 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_count_system.cpu.dcache.mem_side::system.cpu.l2cache.cpu_side 2329 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_count::total 143714 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_size_system.cpu.icache.mem_side::system.cpu.l2cache.cpu_side 4524288 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.pkt_size_system.cpu.dcache.mem_side::system.cpu.l2cache.cpu_side 96448 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.pkt_size::total 4620736 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.snoops 0 # Total snoops (count)
system.l2bus.snoop_fanout::samples 72200 # Request fanout histogram
system.l2bus.snoop_fanout::mean 1 # Request fanout histogram
system.l2bus.snoop_fanout::stdev 0 # Request fanout histogram

system.l2bus.snoop_fanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.l2bus.snoop_fanout::0 0 0.00% 0.00% # Request fanout histogram
system.l2bus.snoop_fanout::1 72200 100.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::2 0 0.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::min_value 1 # Request fanout histogram
system.l2bus.snoop_fanout::max_value 1 # Request fanout histogram
system.l2bus.snoop_fanout::total 72200 # Request fanout histogram
system.l2bus.reqLayer0.occupancy 37470000 # Layer occupancy (ticks)
system.l2bus.reqLayer0.utilization 1.8 # Layer utilization (%)
system.l2bus.respLayer0.occupancy 176825748 # Layer occupancy (ticks)
system.l2bus.respLayer0.utilization 8.7 # Layer utilization (%)
system.l2bus.respLayer1.occupancy 2106000 # Layer occupancy (ticks)
system.l2bus.respLayer1.utilization 0.1 # Layer utilization (%)
system.membus.trans_dist::ReadReq 526 # Transaction distribution
system.membus.trans_dist::ReadResp 526 # Transaction distribution
system.membus.trans_dist::ReadExReq 252 # Transaction distribution
system.membus.trans_dist::ReadExResp 252 # Transaction distribution
system.membus.pkt_count_system.cpu.l2cache.mem_side::system.mem_ctrl.port 1556 # Packet count per connected master and slave (bytes)
system.membus.pkt_count_system.cpu.l2cache.mem_side::total 1556 # Packet count per connected master and slave (bytes)
system.membus.pkt_count::total 1556 # Packet count per connected master and slave (bytes)
system.membus.pkt_size_system.cpu.l2cache.mem_side::system.mem_ctrl.port 49792 # Cumulative packet size per connected master and slave (bytes)
system.membus.pkt_size_system.cpu.l2cache.mem_side::total 49792 # Cumulative packet size per connected master and slave (bytes)
system.membus.pkt_size::total 49792 # Cumulative packet size per connected master and slave (bytes)
system.membus.snoops 0 # Total snoops (count)
system.membus.snoop_fanout::samples 778 # Request fanout histogram
system.membus.snoop_fanout::mean 0 # Request fanout histogram
system.membus.snoop_fanout::stdev 0 # Request fanout histogram
system.membus.snoop_fanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.membus.snoop_fanout::0 778 100.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::1 0 0.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::min_value 0 # Request fanout histogram
system.membus.snoop_fanout::max_value 0 # Request fanout histogram
system.membus.snoop_fanout::total 778 # Request fanout histogram
system.membus.reqLayer2.occupancy 389000 # Layer occupancy (ticks)
system.membus.reqLayer2.utilization 0.0 # Layer utilization (%)
system.membus.respLayer0.occupancy 2091250 # Layer occupancy (ticks)
system.membus.respLayer0.utilization 0.1 # Layer utilization (%)