Verificando arquivos...
Código-fonte do programa: Quicksort_calloc.c
Arquivo de configuração de CPU: MyO3CPU.py --> MyO3CPU.py
Arquivo de configuração de caches e memória: MyCaches.py --> MyCaches.py
Arquivo de configuração de sistema: MySystem.py --> MySystem.py

****
* Compilando o programa ...
* g++ -static Quicksort_calloc.c -o Quicksort_calloc
****

****
* Executando o gem5...
* gem5 --outdir=m5out MySimulation.py -c Quicksort_calloc
****

gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 compiled Feb 16 2016 16:35:34
gem5 started Dec 14 2017 15:10:20
gem5 executing on simulacaolse3
command line: gem5 --outdir=m5out MySimulation.py -c Quicksort_calloc

Programa a ser executado: Quicksort_calloc
Global frequency set at 1000000000000 ticks per second
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb.listener: listening for remote gdb on port 7002

---------- Begin Simulation ----------
info: Entering event queue @ 0. Starting simulation...

Vetor
info: Increasing stack size by one page.
23, 9, 16, 29, 23, 1, 22, 13, 33, 5, 6, 40, 0, 46, 2, 2, 3, 48, 45, 8, 8, 34, 0, 13, 24, 18, 18, 17, 39, 27, 28, 13, 38, 44, 44, 13, 47, 18, 26, 32, 23, 32, 22, 24, 31, 27, 28, 36, 25, 24, 45, 33, 10, 45, 49, 34, 16, 17, 2, 7, 46, 32, 22, 34, 28, 16, 49, 25, 34, 26, 7, 10, 8, 32, 34, 41, 9, 12, 28, 36, 38, 23, 19, 49, 20, 18, 33, 36, 37, 37, 46, 35, 19, 18, 21, 47, 35, 21, 24, 21, 47, 32, 31, 7, 16, 17, 49, 27, 30, 27, 13, 20, 2, 34, 19, 22, 3, 5, 11, 42, 42, 7, 28, 12, 25, 1, 11, 12, 22, 38, 34, 19, 22, 17, 29, 38, 35, 28, 15, 17, 7, 30, 37, 9, 14, 7, 31, 17, 12, 44, 12, 6, 1, 42, 18, 29, 43, 32, 43, 16, 20, 29, 37, 44, 47, 16, 32, 34, 46, 49, 1, 3, 29, 38, 12, 43, 47, 46, 13, 11, 42, 27, 18, 46, 21, 38, 27, 14, 22, 20, 32, 44, 2, 22, 38, 1, 38, 22, 35, 37, 21, 36, 40, 2, 26, 5, 48, 24, 3, 11, 37, 45, 40, 5, 43, 11, 44, 20, 25, 18, 43, 10, 13, 45, 32, 1, 46, 22, 24, 31, 9, 47, 19, 2, 0, 45, 9, 48, 21, 12, 11, 11, 9, 1, 16, 5, 12, 12, 25, 39, 31, 18, 49, 44, 15, 33, 47, 13, 6, 21, 46, 17, 19, 15, 21, 21, 13, 30, 19, 36, 44, 30, 47, 6, 31, 14, 11, 45, 28, 38, 34, 11, 9, 34, 7, 24, 17, 5, 38, 25, 26, 34, 45, 47, 2, 16, 18, 15, 47, 39, 1, 43, 21, 49, 49, 4, 15, 10, 49, 45, 1, 34, 7, 10, 20, 14, 34, 39, 19, 24, 15, 48, 11, 12, 47, 13, 28, 18, 30, 25, 7, 33, 21, 31, 34, 20, 35, 49, 33, 37, 47, 34, 21, 4, 44, 43, 18, 30, 32, 40, 5, 49, 40, 16, 11, 37, 31, 42, 7, 11, 19, 17, 44, 40,

48, 29, 11, 33, 30, 44, 20, 27, 30, 43, 33, 24, 36, 4, 4, 21, 44, 11, 22, 36, 29, 36, 25, 10, 28, 33, 23, 47, 0, 20, 38, 0, 1, 1, 33, 33, 47, 6, 11, 27, 1, 44, 1, 40, 0, 7, 13, 46, 19, 35, 32, 48, 21, 8, 11, 1, 43, 36, 49, 43, 6, 39, 45, 7, 40, 28, 41, 39, 36, 4, 16, 40, 0, 19, 30, 1, 26, 43, 47, 45, 28, 32, 46, 2, 40, 9, 3, 35, 45, 4, 30, 4, 43, 25, 11, 35, 5, 4, 24, 42, 10, 42, 32, 13, 11, 14, 14, 38, 7, 13, 35, 37, 45, 33, 39, 37, 42, 45, 24, 40, 49, 4, 44, 45, 29, 7, 30, 35, 14, 7, 29, 24, 49, 13, 37, 11, 27, 3, 1, 36, 19, 36, 23, 16, 22, 13, 6, 14, 8, 30, 6, 9, 37, 0, 4, 18, 8, 37, 3, 22, 44, 34, 48, 45, 49, 38, 8, 26, 43, 9, 12, 12, 48, 36, 31, 20, 1, 39, 36, 11, 21, 43, 20, 8, 43, 27, 27, 3, 14, 32, 25, 10, 19, 24, 5, 18, 14, 14, 47, 7, 25, 9, 22, 25, 47, 5, 47, 0, 44, 34, 13, 15, 29, 36, 26, 24, 13, 5, 28, 29, 39, 5, 39, 8, 31, 44, 29, 45, 10, 26, 5, 36, 37, 27, 11, 35, 32, 11, 37, 28, 45, 1, 43, 26, 39, 21, 2, 2, 26, 30, 31, 16, 38, 20, 26, 21, 16, 5, 19, 27, 31, 24, 15, 19, 1, 28, 6, 35, 39, 45, 13, 36, 48, 8, 14, 37, 30, 17, 41, 8, 47, 24, 26, 37, 44, 5, 9, 13, 10, 28, 42, 44, 4, 9, 13, 7, 37, 21, 42, 29, 16, 7, 15, 15, 15, 30, 4, 47, 49, 46, 8, 48, 20, 36, 36, 17, 41, 47, 30, 2, 27, 24, 46, 31, 33, 11, 38, 20, 34, 32, 1, 2, 39, 19, 19, 6, 1, 24, 6, 0, 20, 14, 48, 40, 0, 34, 9, 42, 33, 39, 46, 10, 15, 44, 41, 48, 5, 31, 19, 41, 13, 22, 43, 4, 41, 13, 11, 42, 37, 17, 42, 9, 33, 41, 1, 35, 27, 11, 29, 11, 2, 25, 21, 18, 19, 15, 16, 26, 48, 37, 17, 12, 10, 13, 18, 1, 26, 31, 44, 15, 0, 38, 26, 33, 29, 27, 21, 9, 40, 0, 20, 45, 26, 43, 13, 47, 10, 31, 24, 9, 21, 43, 23, 31, 6, 41, 34, 34, 23, 30, 1, 23, 19, 27, 9, 0, 7, 30, 9, 49, 30, 31, 44, 8, 25, 9, 6, 35, 41, 32, 44, 12, 25, 17, 45, 34, 11, 29, 18, 34, 12, 22, 9, 31, 49, 18, 33, 8, 0, 45, 8, 33, 26, 2, 41, 3, 14, 49, 39, 5, 33, 35, 19, 11, 5, 16, 45, 16, 45, 15, 2, 9, 37, 13, 42, 39, 34, 26, 47, 34, 21, 7, 17, 49, 12, 11, 3, 26, 12, 42, 33, 46, 29, 2, 7, 34, 18, 4, 2, 15, 19, 4, 25, 9, 18, 19, 48, 2, 45, 47, 38, 18, 7, 8, 18, 19, 19, 21, 47, 31, 15, 30, 29, 44, 34, 36, 31, 4, 40, 33, 21, 12, 40, 48, 21, 8, 18, 21, 12, 13, 20, 2, 34, 27, 10, 2, 48, 31, 25, 45, 13, 40, 25, 42, 34, 9, 31, 17, 15, 23, 1, 37, 35, 41, 35, 6, 1, 3, 29, 15, 19, 0, 17, 3, 29, 28, 7, 28, 9, 32, 23, 24, 22, 1, 19, 8, 12, 2, 26, 28, 25, 27, 15, 11, 20, 2, 19, 21, 8, 49, 36, 27, 1, 3, 32, 30, 33, 39, 10, 45, 21, 34, 19, 45, 35, 40,

Vetor

0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 23, 23, 23, 23, 23, 23, 23, 23, 23, 23, 23, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 34, 34, 34, 34, 34,

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42, 42, 42, 42, 42, 42, 42, 42, 42, 42, 42, 42, 42, 42, 42, 43, 43, 43, 43, 43, 43, 43, 43, 43, 43,
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48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 49, 49, 49, 49, 49, 49, 49, 49, 49,
49, 49, 49, 49, 49, 49, 49, 49, 49, 49, 49, 49,
Finishing simulation. Current tick: 1047459500. Reason: target called exit()
---------------- End Simulation ----------------
****
* Resultados da simulação
****

sim_seconds 0.001047 # Number of seconds simulated
sim_ticks 1047459500 # Number of ticks simulated
final_tick 1047459500 # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
sim_freq 1000000000000 # Frequency of simulated ticks
host_inst_rate 106844 # Simulator instruction rate (inst/s)
host_op_rate 198062 # Simulator op (including micro ops) rate (op/s)
host_tick_rate 71678669 # Simulator tick rate (ticks/s)
host_mem_usage 654368 # Number of bytes of host memory used
host_seconds 14.61 # Real time elapsed on the host
sim_insts 1561340 # Number of instructions simulated
sim_ops 2894328 # Number of ops (including micro ops) simulated
system.clk_domain.voltage_domain.voltage 1 # Voltage in Volts
system.clk_domain.clock 500 # Clock period in ticks
system.mem_ctrl.bytes_read::cpu.inst 27840 # Number of bytes read from this memory
system.mem_ctrl.bytes_read::cpu.data 19264 # Number of bytes read from this memory
system.mem_ctrl.bytes_read::total 47104 # Number of bytes read from this memory
system.mem_ctrl.bytes_inst_read::cpu.inst 27840 # Number of instructions bytes read from this memory
system.mem_ctrl.bytes_inst_read::total 27840 # Number of instructions bytes read from this memory
system.mem_ctrl.num_reads::cpu.inst 435 # Number of read requests responded to by this memory
system.mem_ctrl.num_reads::cpu.data 301 # Number of read requests responded to by this memory
system.mem_ctrl.num_reads::total 736 # Number of read requests responded to by this memory
system.mem_ctrl.bw_read::cpu.inst 26578593 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_read::cpu.data 18391165 # Total read bandwidth from this memory (bytes/s)

system.mem_ctrl.bw_read::total 44969758 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_inst_read::cpu.inst 26578593 # Instruction read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_inst_read::total 26578593 # Instruction read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_total::cpu.inst 26578593 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.bw_total::cpu.data 18391165 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.bw_total::total 44969758 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.readReqs 736 # Number of read requests accepted
system.mem_ctrl.writeReqs 0 # Number of write requests accepted
system.mem_ctrl.readBursts 736 # Number of DRAM read bursts, including those serviced by the write queue
system.mem_ctrl.writeBursts 0 # Number of DRAM write bursts, including those merged in the write queue
system.mem_ctrl.bytesReadDRAM 47104 # Total number of bytes read from DRAM
system.mem_ctrl.bytesReadWrQ 0 # Total number of bytes read from write queue
system.mem_ctrl.bytesWritten 0 # Total number of bytes written to DRAM
system.mem_ctrl.bytesReadSys 47104 # Total read bytes from the system interface side
system.mem_ctrl.bytesWrittenSys 0 # Total written bytes from the system interface side
system.mem_ctrl.servicedByWrQ 0 # Number of DRAM read bursts serviced by the write queue
system.mem_ctrl.mergedWrBursts 0 # Number of DRAM write bursts merged with an existing one
system.mem_ctrl.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write
system.mem_ctrl.perBankRdBursts::0 73 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::1 122 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::2 74 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::3 59 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::4 71 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::5 35 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::6 136 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::7 9 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::8 12 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::9 36 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::10 29 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::11 14 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::12 27 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::13 32 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::14 5 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::15 2 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::0 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::1 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::2 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::3 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::4 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::5 0 # Per bank write bursts

system.mem_ctrl.perBankWrBursts::6 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::7 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::8 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::9 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::10 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::11 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::12 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::13 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::14 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::15 0 # Per bank write bursts
system.mem_ctrl.numRdRetry 0 # Number of times read queue was full causing retry
system.mem_ctrl.numWrRetry 0 # Number of times write queue was full causing retry
system.mem_ctrl.totGap 1047384500 # Total gap between requests
system.mem_ctrl.readPktSize::0 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::1 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::2 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::3 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::4 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::5 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::6 736 # Read request sizes (log2)
system.mem_ctrl.writePktSize::0 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::1 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::2 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::3 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::4 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::5 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::6 0 # Write request sizes (log2)
system.mem_ctrl.rdQLenPdf::0 528 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::1 162 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::2 39 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::3 7 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::4 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::5 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::6 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::7 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::8 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::9 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::10 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::11 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::12 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::13 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::14 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::15 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::16 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::17 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::18 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::19 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::20 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::21 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::22 0 # What read queue length does an incoming req see

system.mem_ctrl.rdQLenPdf::23 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::24 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::25 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::26 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::27 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::28 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::29 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::30 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::31 0 # What read queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::0 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::1 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::2 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::3 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::4 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::5 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::6 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::7 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::8 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::9 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::10 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::11 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::12 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::13 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::14 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::15 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::16 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::17 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::18 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::19 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::20 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::21 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::22 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::23 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::24 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::25 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::26 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::27 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::28 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::29 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::30 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::31 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::32 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::33 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::34 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::35 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::36 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::37 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::38 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::39 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::40 0 # What write queue length does an incoming req see

system.mem_ctrl.wrQLenPdf::41 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::42 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::43 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::44 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::45 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::46 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::47 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::48 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::49 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::50 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::51 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::52 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::53 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::54 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::55 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::56 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::57 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::58 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::59 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::60 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::61 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::62 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::63 0 # What write queue length does an incoming req see
system.mem_ctrl.bytesPerActivate::samples 189 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::mean 239.407407 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::gmean 149.185381 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::stdev 270.978660 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::0-127 79 41.80% 41.80% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::128-255 51 26.98% 68.78% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::256-383 22 11.64% 80.42% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::384-511 9 4.76% 85.19% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::512-639 6 3.17% 88.36% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::640-767 6 3.17% 91.53% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::768-895 2 1.06% 92.59% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::896-1023 4 2.12% 94.71% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::1024-1151 10 5.29% 100.00% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::total 189 # Bytes accessed per row activation
system.mem_ctrl.totQLat 6962500 # Total ticks spent queuing
system.mem_ctrl.totMemAccLat 20762500 # Total ticks spent from burst creation until serviced by the DRAM
system.mem_ctrl.totBusLat 3680000 # Total ticks spent in databus transfers

system.mem_ctrl.avgQLat 9459.92 # Average queueing delay per DRAM burst
system.mem_ctrl.avgBusLat 5000.00 # Average bus latency per DRAM burst
system.mem_ctrl.avgMemAccLat 28209.92 # Average memory access latency per DRAM burst
system.mem_ctrl.avgRdBW 44.97 # Average DRAM read bandwidth in MiByte/s
system.mem_ctrl.avgWrBW 0.00 # Average achieved write bandwidth in MiByte/s
system.mem_ctrl.avgRdBWSys 44.97 # Average system read bandwidth in MiByte/s
system.mem_ctrl.avgWrBWSys 0.00 # Average system write bandwidth in MiByte/s
system.mem_ctrl.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s
system.mem_ctrl.busUtil 0.35 # Data bus utilization in percentage
system.mem_ctrl.busUtilRead 0.35 # Data bus utilization in percentage for reads
system.mem_ctrl.busUtilWrite 0.00 # Data bus utilization in percentage for writes
system.mem_ctrl.avgRdQLen 1.02 # Average read queue length when enqueuing
system.mem_ctrl.avgWrQLen 0.00 # Average write queue length when enqueuing
system.mem_ctrl.readRowHits 540 # Number of row buffer hits during reads
system.mem_ctrl.writeRowHits 0 # Number of row buffer hits during writes
system.mem_ctrl.readRowHitRate 73.37 # Row buffer hit rate for reads
system.mem_ctrl.writeRowHitRate nan # Row buffer hit rate for writes
system.mem_ctrl.avgGap 1423076.77 # Average gap between requests
system.mem_ctrl.pageHitRate 73.37 # Row buffer hit rate, read and write combined
system.mem_ctrl_0.actEnergy 1020600 # Energy for activate commands per rank (pJ)
system.mem_ctrl_0.preEnergy 556875 # Energy for precharge commands per rank (pJ)
system.mem_ctrl_0.readEnergy 4149600 # Energy for read commands per rank (pJ)
system.mem_ctrl_0.writeEnergy 0 # Energy for write commands per rank (pJ)
system.mem_ctrl_0.refreshEnergy 68147040 # Energy for refresh commands per rank (pJ)
system.mem_ctrl_0.actBackEnergy 209884545 # Energy for active background per rank (pJ)
system.mem_ctrl_0.preBackEnergy 442061250 # Energy for precharge background per rank (pJ)
system.mem_ctrl_0.totalEnergy 725819910 # Total energy per rank (pJ)
system.mem_ctrl_0.averagePower 695.484610 # Core power per rank (mW)
system.mem_ctrl_0.memoryStateTime::IDLE 734048000 # Time in different power states
system.mem_ctrl_0.memoryStateTime::REF 34840000 # Time in different power states
system.mem_ctrl_0.memoryStateTime::PRE_PDN 0 # Time in different power states
system.mem_ctrl_0.memoryStateTime::ACT 274743250 # Time in different power states
system.mem_ctrl_0.memoryStateTime::ACT_PDN 0 # Time in different power states
system.mem_ctrl_1.actEnergy 340200 # Energy for activate commands per rank (pJ)
system.mem_ctrl_1.preEnergy 185625 # Energy for precharge commands per rank (pJ)
system.mem_ctrl_1.readEnergy 1115400 # Energy for read commands per rank (pJ)
system.mem_ctrl_1.writeEnergy 0 # Energy for write commands per rank (pJ)
system.mem_ctrl_1.refreshEnergy 68147040 # Energy for refresh commands per rank (pJ)
system.mem_ctrl_1.actBackEnergy 45930600 # Energy for active background per rank (pJ)
system.mem_ctrl_1.preBackEnergy 585872250 # Energy for precharge background per rank (pJ)
system.mem_ctrl_1.totalEnergy 701591115 # Total energy per rank (pJ)
system.mem_ctrl_1.averagePower 672.277304 # Core power per rank (mW)
system.mem_ctrl_1.memoryStateTime::IDLE 975561250 # Time in different power states
system.mem_ctrl_1.memoryStateTime::REF 34840000 # Time in different power states
system.mem_ctrl_1.memoryStateTime::PRE_PDN 0 # Time in different power states
system.mem_ctrl_1.memoryStateTime::ACT 34236750 # Time in different power states
system.mem_ctrl_1.memoryStateTime::ACT_PDN 0 # Time in different power states

system.cpu.branchPred.lookups 341045 # Number of BP lookups
system.cpu.branchPred.condPredicted 341045 # Number of conditional branches predicted
system.cpu.branchPred.condIncorrect 8734 # Number of conditional branches incorrect
system.cpu.branchPred.BTBLookups 231364 # Number of BTB lookups
system.cpu.branchPred.BTBHits 185944 # Number of BTB hits
system.cpu.branchPred.BTBCorrect 0 # Number of correct BTB predictions (this stat may not work properly.
system.cpu.branchPred.BTBHitPct 80.368597 # BTB Hit Percentage
system.cpu.branchPred.usedRAS 24687 # Number of times the RAS was used to get a target.
system.cpu.branchPred.RASInCorrect 111 # Number of incorrect RAS predictions.
system.cpu.apic_clk_domain.clock 8000 # Clock period in ticks
system.cpu.workload.num_syscalls 14 # Number of system calls
system.cpu.numCycles 2094920 # number of cpu cycles simulated
system.cpu.numWorkItemsStarted 0 # number of work items this cpu started
system.cpu.numWorkItemsCompleted 0 # number of work items this cpu completed
system.cpu.fetch.icacheStallCycles 620073 # Number of cycles fetch is stalled on an Icache miss
system.cpu.fetch.Insts 1760603 # Number of instructions fetch has processed
system.cpu.fetch.Branches 341045 # Number of branches that fetch encountered
system.cpu.fetch.predictedBranches 210631 # Number of branches that fetch has predicted taken
system.cpu.fetch.Cycles 1437224 # Number of cycles fetch has run and was not squashing or blocked
system.cpu.fetch.SquashCycles 17647 # Number of cycles fetch has spent squashing
system.cpu.fetch.MiscStallCycles 36 # Number of cycles fetch has spent waiting on interrupts, or bad addresses, or out of MSHRs
system.cpu.fetch.PendingTrapStallCycles 567 # Number of stall cycles due to pending traps
system.cpu.fetch.PendingQuiesceStallCycles 13 # Number of stall cycles due to pending quiesce instructions
system.cpu.fetch.CacheLines 598464 # Number of cache lines fetched
system.cpu.fetch.IcacheSquashes 2422 # Number of outstanding Icache misses that were squashed
system.cpu.fetch.rateDist::samples 2066736 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::mean 1.561232 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::stdev 1.374162 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::underflows 0 0.00% 0.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::0 800312 38.72% 38.72% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::1 202745 9.81% 48.53% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::2 167128 8.09% 56.62% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::3 896551 43.38% 100.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::overflows 0 0.00% 100.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::min_value 0 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::max_value 3 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::total 2066736 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.branchRate 0.162796 # Number of branch fetches per cycle
system.cpu.fetch.rate 0.840415 # Number of inst fetches per cycle
system.cpu.decode.IdleCycles 648974 # Number of cycles decode is idle
system.cpu.decode.BlockedCycles 216236 # Number of cycles decode is blocked
system.cpu.decode.RunCycles 1137550 # Number of cycles decode is running
system.cpu.decode.UnblockCycles 55153 # Number of cycles decode is unblocking
system.cpu.decode.SquashCycles 8823 # Number of cycles decode is squashing
system.cpu.decode.DecodedInsts 3096112 # Number of instructions handled by decode
system.cpu.decode.SquashedInsts 23044 # Number of squashed instructions handled by decode
system.cpu.rename.SquashCycles 8823 # Number of cycles rename is squashing
system.cpu.rename.IdleCycles 691562 # Number of cycles rename is idle
system.cpu.rename.BlockCycles 131256 # Number of cycles rename is blocking
system.cpu.rename.serializeStallCycles 496 # count of cycles rename stalled for serializing inst
system.cpu.rename.RunCycles 1141476 # Number of cycles rename is running
system.cpu.rename.UnblockCycles 93123 # Number of cycles rename is unblocking
system.cpu.rename.RenamedInsts 3066659 # Number of instructions processed by rename
system.cpu.rename.SquashedInsts 16271 # Number of squashed instructions processed by rename
system.cpu.rename.ROBFullEvents 64375 # Number of times rename has blocked due to ROB full
system.cpu.rename.IQFullEvents 5035 # Number of times rename has blocked due to IQ full
system.cpu.rename.SQFullEvents 11075 # Number of times rename has blocked due to SQ full
system.cpu.rename.RenamedOperands 3614204 # Number of destination operands rename has renamed
system.cpu.rename.RenameLookups 7952396 # Number of register rename lookups that rename has made
system.cpu.rename.int_rename_lookups 4549480 # Number of integer rename lookups
system.cpu.rename.fp_rename_lookups 156476 # Number of floating rename lookups
system.cpu.rename.CommittedMaps 3397362 # Number of HB maps that are committed
system.cpu.rename.UndoneMaps 216842 # Number of HB maps that are undone due to squashing
system.cpu.rename.serializingInsts 24 # count of serializing insts renamed
system.cpu.rename.tempSerializingInsts 24 # count of temporary serializing insts renamed
system.cpu.rename.skidInsts 126964 # count of insts added to the skid buffer
system.cpu.memDep0.insertedLoads 467921 # Number of loads inserted to the mem dependence unit.
system.cpu.memDep0.insertedStores 242024 # Number of stores inserted to the mem dependence unit.
system.cpu.memDep0.conflictingLoads 80303 # Number of conflicting loads.
system.cpu.memDep0.conflictingStores 17900 # Number of conflicting stores.
system.cpu.iq.iqInstsAdded 3053456 # Number of instructions added to the IQ (excludes non-spec)
system.cpu.iq.iqNonSpecInstsAdded 65 # Number of non-speculative instructions added to the IQ

system.cpu.iq.iqInstsIssued 3003969 # Number of instructions issued
system.cpu.iq.iqSquashedInstsIssued 2614 # Number of squashed instructions issued
system.cpu.iq.iqSquashedInstsExamined 159193 # Number of squashed instructions iterated over during squash; mainly for profiling
system.cpu.iq.iqSquashedOperandsExamined 197239 # Number of squashed operands that are examined and possibly removed from graph
system.cpu.iq.iqSquashedNonSpecRemoved 50 # Number of squashed non-spec instructions that were removed
system.cpu.iq.issued_per_cycle::samples 2066736 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::mean 1.453485 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::stdev 0.979634 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::underflows 0 0.00% 0.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::0 440702 21.32% 21.32% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::1 527569 25.53% 46.85% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::2 834422 40.37% 87.22% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::3 248616 12.03% 99.25% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::4 15427 0.75% 100.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::overflows 0 0.00% 100.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::min_value 0 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::max_value 4 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::total 2066736 # Number of insts issued each cycle
system.cpu.iq.fu_full::No_OpClass 0 0.00% 0.00% # attempts to use FU when none available
system.cpu.iq.fu_full::IntAlu 425627 73.35% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::IntMult 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::IntDiv 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatAdd 16 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatCmp 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatCvt 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatMult 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatDiv 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatSqrt 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAdd 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAddAcc 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAlu 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdCmp 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdCvt 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMisc 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMult 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMultAcc 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdShift 0 0.00% 73.35% # attempts to use FU when none available

system.cpu.iq.fu_full::SimdShiftAcc 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdSqrt 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatAdd 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatAlu 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatCmp 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatCvt 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatDiv 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMisc 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMult 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMultAcc 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatSqrt 0 0.00% 73.35% # attempts to use FU when none available
system.cpu.iq.fu_full::MemRead 110452 19.04% 92.39% # attempts to use FU when none available
system.cpu.iq.fu_full::MemWrite 44158 7.61% 100.00% # attempts to use FU when none available
system.cpu.iq.fu_full::IprAccess 0 0.00% 100.00% # attempts to use FU when none available
system.cpu.iq.fu_full::InstPrefetch 0 0.00% 100.00% # attempts to use FU when none available
system.cpu.iq.FU_type_0::No_OpClass 14217 0.47% 0.47% # Type of FU issued
system.cpu.iq.FU_type_0::IntAlu 2216389 73.78% 74.26% # Type of FU issued
system.cpu.iq.FU_type_0::IntMult 5739 0.19% 74.45% # Type of FU issued
system.cpu.iq.FU_type_0::IntDiv 28 0.00% 74.45% # Type of FU issued
system.cpu.iq.FU_type_0::FloatAdd 72198 2.40% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::FloatCmp 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::FloatCvt 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::FloatMult 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::FloatDiv 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::FloatSqrt 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAdd 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAddAcc 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAlu 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdCmp 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdCvt 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMisc 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMult 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMultAcc 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdShift 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdShiftAcc 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdSqrt 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatAdd 0 0.00% 76.85% # Type of FU issued

system.cpu.iq.FU_type_0::SimdFloatAlu 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatCmp 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatCvt 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatDiv 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMisc 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMult 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMultAcc 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatSqrt 0 0.00% 76.85% # Type of FU issued
system.cpu.iq.FU_type_0::MemRead 457736 15.24% 92.09% # Type of FU issued
system.cpu.iq.FU_type_0::MemWrite 237662 7.91% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::IprAccess 0 0.00% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::InstPrefetch 0 0.00% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::total 3003969 # Type of FU issued
system.cpu.iq.rate 1.433930 # Inst issue rate
system.cpu.iq.fu_busy_cnt 580253 # FU busy when requested
system.cpu.iq.fu_busy_rate 0.193162 # FU busy rate (busy events/executed inst)
system.cpu.iq.int_inst_queue_reads 8468946 # Number of integer instruction queue reads
system.cpu.iq.int_inst_queue_writes 3120362 # Number of integer instruction queue writes
system.cpu.iq.int_inst_queue_wakeup_accesses 2891991 # Number of integer instruction queue wakeup accesses
system.cpu.iq.fp_inst_queue_reads 188595 # Number of floating instruction queue reads
system.cpu.iq.fp_inst_queue_writes 92413 # Number of floating instruction queue writes
system.cpu.iq.fp_inst_queue_wakeup_accesses 92257 # Number of floating instruction queue wakeup accesses
system.cpu.iq.int_alu_accesses 3473687 # Number of integer alu accesses
system.cpu.iq.fp_alu_accesses 96318 # Number of floating point alu accesses
system.cpu.iew.lsq.thread0.forwLoads 52077 # Number of loads that had data forwarded from stores
system.cpu.iew.lsq.thread0.invAddrLoads 0 # Number of loads ignored due to an invalid address
system.cpu.iew.lsq.thread0.squashedLoads 39219 # Number of loads squashed
system.cpu.iew.lsq.thread0.ignoredResponses 49 # Number of memory responses ignored because the instruction is squashed
system.cpu.iew.lsq.thread0.memOrderViolation 61 # Number of memory ordering violations
system.cpu.iew.lsq.thread0.squashedStores 6604 # Number of stores squashed
system.cpu.iew.lsq.thread0.invAddrSwpfs 0 # Number of software prefetches ignored due to an invalid address
system.cpu.iew.lsq.thread0.blockedLoads 0 # Number of blocked loads due to partial load-store forwarding
system.cpu.iew.lsq.thread0.rescheduledLoads 33 # Number of loads that were rescheduled
system.cpu.iew.lsq.thread0.cacheBlocked 9 # Number of times an access to memory failed due to the cache being blocked
system.cpu.iew.iewIdleCycles 0 # Number of cycles IEW is idle
system.cpu.iew.iewSquashCycles 8823 # Number of cycles IEW is squashing
system.cpu.iew.iewBlockCycles 38745 # Number of cycles IEW is blocking
system.cpu.iew.iewUnblockCycles 4114 # Number of cycles IEW is unblocking
system.cpu.iew.iewDispatchedInsts 3053521 # Number of instructions dispatched to IQ
system.cpu.iew.iewDispSquashedInsts 0 # Number of squashed instructions skipped by dispatch
system.cpu.iew.iewDispLoadInsts 467921 # Number of dispatched load instructions

system.cpu.iew.iewDispStoreInsts 242024 # Number of dispatched store instructions
system.cpu.iew.iewDispNonSpecInsts 25 # Number of dispatched non-speculative instructions
system.cpu.iew.iewIQFullEvents 3 # Number of times the IQ has become full, causing a stall
system.cpu.iew.iewLSQFullEvents 4096 # Number of times the LSQ has become full, causing a stall
system.cpu.iew.memOrderViolationEvents 61 # Number of memory order violations
system.cpu.iew.predictedTakenIncorrect 5675 # Number of branches that were predicted taken incorrectly
system.cpu.iew.predictedNotTakenIncorrect 3338 # Number of branches that were predicted not taken incorrectly
system.cpu.iew.branchMispredicts 9013 # Number of branch mispredicts detected at execute
system.cpu.iew.iewExecutedInsts 2992286 # Number of executed instructions
system.cpu.iew.iewExecLoadInsts 453151 # Number of load instructions executed
system.cpu.iew.iewExecSquashedInsts 11683 # Number of squashed instructions skipped in execute
system.cpu.iew.exec_swp 0 # number of swp insts executed
system.cpu.iew.exec_nop 0 # number of nop insts executed
system.cpu.iew.exec_refs 689863 # number of memory reference insts executed
system.cpu.iew.exec_branches 318629 # Number of branches executed
system.cpu.iew.exec_stores 236712 # Number of stores executed
system.cpu.iew.exec_rate 1.428353 # Inst execution rate
system.cpu.iew.wb_sent 2986484 # cumulative count of insts sent to commit
system.cpu.iew.wb_count 2984248 # cumulative count of insts written-back
system.cpu.iew.wb_producers 2073214 # num instructions producing a value
system.cpu.iew.wb_consumers 3243471 # num instructions consuming a value
system.cpu.iew.wb_penalized 0 # number of instrctions required to write to 'other' IQ
system.cpu.iew.wb_rate 1.424516 # insts written-back per cycle
system.cpu.iew.wb_fanout 0.639196 # average fanout of values written-back
system.cpu.iew.wb_penalized_rate 0 # fraction of instructions written-back that wrote to 'other' IQ
system.cpu.commit.commitSquashedInsts 145458 # The number of squashed insts skipped by commit
system.cpu.commit.commitNonSpecStalls 15 # The number of times commit has been forced to stall to communicate backwards
system.cpu.commit.branchMispredicts 8768 # The number of times a branch was mispredicted
system.cpu.commit.committed_per_cycle::samples 2024770 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::mean 1.429460 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::stdev 1.478770 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::underflows 0 0.00% 0.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::0 779781 38.51% 38.51% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::1 442033 21.83% 60.34% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::2 296193 14.63% 74.97% # Number of insts

commited each cycle
system.cpu.commit.committed_per_cycle::3 167143 8.25% 83.23% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::4 339620 16.77% 100.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::overflows 0 0.00% 100.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::min_value 0 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::max_value 4 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::total 2024770 # Number of insts commited each cycle
system.cpu.commit.committedInsts 1561340 # Number of instructions committed
system.cpu.commit.committedOps 2894328 # Number of ops (including micro ops) committed
system.cpu.commit.swp_count 0 # Number of s/w prefetches committed
system.cpu.commit.refs 664122 # Number of memory references committed
system.cpu.commit.loads 428702 # Number of loads committed
system.cpu.commit.membars 0 # Number of memory barriers committed
system.cpu.commit.branches 308047 # Number of branches committed
system.cpu.commit.fp_insts 92175 # Number of committed floating point instructions.
system.cpu.commit.int_insts 2808764 # Number of committed integer instructions.
system.cpu.commit.function_calls 23883 # Number of function calls committed.
system.cpu.commit.op_class_0::No_OpClass 14063 0.49% 0.49% # Class of committed instruction
system.cpu.commit.op_class_0::IntAlu 2138244 73.88% 74.36% # Class of committed instruction
system.cpu.commit.op_class_0::IntMult 5737 0.20% 74.56% # Class of committed instruction
system.cpu.commit.op_class_0::IntDiv 28 0.00% 74.56% # Class of committed instruction
system.cpu.commit.op_class_0::FloatAdd 72134 2.49% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::FloatCmp 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::FloatCvt 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::FloatMult 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::FloatDiv 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::FloatSqrt 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAdd 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAddAcc 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAlu 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdCmp 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdCvt 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMisc 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMult 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMultAcc 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdShift 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdShiftAcc 0 0.00% 77.05% # Class of committed

instruction
system.cpu.commit.op_class_0::SimdSqrt 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatAdd 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatAlu 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatCmp 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatCvt 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatDiv 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMisc 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMult 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMultAcc 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatSqrt 0 0.00% 77.05% # Class of committed instruction
system.cpu.commit.op_class_0::MemRead 428702 14.81% 91.87% # Class of committed instruction
system.cpu.commit.op_class_0::MemWrite 235420 8.13% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::IprAccess 0 0.00% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::InstPrefetch 0 0.00% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::total 2894328 # Class of committed instruction
system.cpu.commit.bw_lim_events 339620 # number cycles where commit BW limit reached
system.cpu.rob.rob_reads 4724936 # The number of ROB reads
system.cpu.rob.rob_writes 6121573 # The number of ROB writes
system.cpu.timesIdled 301 # Number of times that the entire CPU went into an idle state and unscheduled itself
system.cpu.idleCycles 28184 # Total number of cycles that the CPU has spent unscheduled due to idling
system.cpu.committedInsts 1561340 # Number of Instructions Simulated
system.cpu.committedOps 2894328 # Number of Ops (including micro ops) Simulated
system.cpu.cpi 1.341745 # CPI: Cycles Per Instruction
system.cpu.cpi_total 1.341745 # CPI: Total CPI of All Threads
system.cpu.ipc 0.745298 # IPC: Instructions Per Cycle
system.cpu.ipc_total 0.745298 # IPC: Total IPC of All Threads
system.cpu.int_regfile_reads 4415068 # number of integer regfile reads
system.cpu.int_regfile_writes 2342559 # number of integer regfile writes
system.cpu.fp_regfile_reads 156419 # number of floating regfile reads
system.cpu.fp_regfile_writes 76203 # number of floating regfile writes
system.cpu.cc_regfile_reads 1844484 # number of cc regfile reads
system.cpu.cc_regfile_writes 1084359 # number of cc regfile writes
system.cpu.misc_regfile_reads 1319607 # number of misc regfile reads
system.cpu.misc_regfile_writes 1 # number of misc regfile writes

system.cpu.dcache.tags.replacements 10 # number of replacements
system.cpu.dcache.tags.tagsinuse 263.000865 # Cycle average of tags in use
system.cpu.dcache.tags.total_refs 636063 # Total number of references to valid blocks.
system.cpu.dcache.tags.sampled_refs 302 # Sample count of references to valid blocks.
system.cpu.dcache.tags.avg_refs 2106.168874 # Average number of references to valid blocks.
system.cpu.dcache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.dcache.tags.occ_blocks::cpu.data 263.000865 # Average occupied blocks per requestor
system.cpu.dcache.tags.occ_percent::cpu.data 0.513674 # Average percentage of cache occupancy
system.cpu.dcache.tags.occ_percent::total 0.513674 # Average percentage of cache occupancy
system.cpu.dcache.tags.occ_task_id_blocks::1024 292 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::0 10 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::2 89 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::3 193 # Occupied blocks per task id
system.cpu.dcache.tags.occ_task_id_percent::1024 0.570312 # Percentage of cache occupancy per task id
system.cpu.dcache.tags.tag_accesses 2546018 # Number of tag accesses
system.cpu.dcache.tags.data_accesses 2546018 # Number of data accesses
system.cpu.dcache.ReadReq_hits::cpu.data 400855 # number of ReadReq hits
system.cpu.dcache.ReadReq_hits::total 400855 # number of ReadReq hits
system.cpu.dcache.WriteReq_hits::cpu.data 235208 # number of WriteReq hits
system.cpu.dcache.WriteReq_hits::total 235208 # number of WriteReq hits
system.cpu.dcache.demand_hits::cpu.data 636063 # number of demand (read+write) hits
system.cpu.dcache.demand_hits::total 636063 # number of demand (read+write) hits
system.cpu.dcache.overall_hits::cpu.data 636063 # number of overall hits
system.cpu.dcache.overall_hits::total 636063 # number of overall hits
system.cpu.dcache.ReadReq_misses::cpu.data 154 # number of ReadReq misses
system.cpu.dcache.ReadReq_misses::total 154 # number of ReadReq misses
system.cpu.dcache.WriteReq_misses::cpu.data 212 # number of WriteReq misses
system.cpu.dcache.WriteReq_misses::total 212 # number of WriteReq misses
system.cpu.dcache.demand_misses::cpu.data 366 # number of demand (read+write) misses
system.cpu.dcache.demand_misses::total 366 # number of demand (read+write) misses
system.cpu.dcache.overall_misses::cpu.data 366 # number of overall misses
system.cpu.dcache.overall_misses::total 366 # number of overall misses
system.cpu.dcache.ReadReq_miss_latency::cpu.data 11156250 # number of ReadReq miss cycles
system.cpu.dcache.ReadReq_miss_latency::total 11156250 # number of ReadReq miss cycles
system.cpu.dcache.WriteReq_miss_latency::cpu.data 15009000 # number of WriteReq miss cycles
system.cpu.dcache.WriteReq_miss_latency::total 15009000 # number of WriteReq miss cycles
system.cpu.dcache.demand_miss_latency::cpu.data 26165250 # number of demand (read+write) miss cycles
system.cpu.dcache.demand_miss_latency::total 26165250 # number of demand (read+write) miss cycles
system.cpu.dcache.overall_miss_latency::cpu.data 26165250 # number of overall miss cycles

system.cpu.dcache.overall_miss_latency::total 26165250 # number of overall miss cycles
system.cpu.dcache.ReadReq_accesses::cpu.data 401009 # number of ReadReq accesses(hits+misses)
system.cpu.dcache.ReadReq_accesses::total 401009 # number of ReadReq accesses(hits+misses)
system.cpu.dcache.WriteReq_accesses::cpu.data 235420 # number of WriteReq accesses(hits+misses)
system.cpu.dcache.WriteReq_accesses::total 235420 # number of WriteReq accesses(hits+misses)
system.cpu.dcache.demand_accesses::cpu.data 636429 # number of demand (read+write) accesses
system.cpu.dcache.demand_accesses::total 636429 # number of demand (read+write) accesses
system.cpu.dcache.overall_accesses::cpu.data 636429 # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total 636429 # number of overall (read+write) accesses
system.cpu.dcache.ReadReq_miss_rate::cpu.data 0.000384 # miss rate for ReadReq accesses
system.cpu.dcache.ReadReq_miss_rate::total 0.000384 # miss rate for ReadReq accesses
system.cpu.dcache.WriteReq_miss_rate::cpu.data 0.000901 # miss rate for WriteReq accesses
system.cpu.dcache.WriteReq_miss_rate::total 0.000901 # miss rate for WriteReq accesses
system.cpu.dcache.demand_miss_rate::cpu.data 0.000575 # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total 0.000575 # miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data 0.000575 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.000575 # miss rate for overall accesses
system.cpu.dcache.ReadReq_avg_miss_latency::cpu.data 72443.181818 # average ReadReq miss latency
system.cpu.dcache.ReadReq_avg_miss_latency::total 72443.181818 # average ReadReq miss latency
system.cpu.dcache.WriteReq_avg_miss_latency::cpu.data 70797.169811 # average WriteReq miss latency
system.cpu.dcache.WriteReq_avg_miss_latency::total 70797.169811 # average WriteReq miss latency
system.cpu.dcache.demand_avg_miss_latency::cpu.data 71489.754098 # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total 71489.754098 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data 71489.754098 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total 71489.754098 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 229 # number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs 6 # number of cycles access was blocked
system.cpu.dcache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs 38.166667 # average number of cycles each access was blocked
system.cpu.dcache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.dcache.fast_writes 0 # number of fast writes performed

system.cpu.dcache.cache_copies 0 # number of cache copies performed
system.cpu.dcache.writebacks::writebacks 9 # number of writebacks
system.cpu.dcache.writebacks::total 9 # number of writebacks
system.cpu.dcache.ReadReq_mshr_hits::cpu.data 64 # number of ReadReq MSHR hits
system.cpu.dcache.ReadReq_mshr_hits::total 64 # number of ReadReq MSHR hits
system.cpu.dcache.demand_mshr_hits::cpu.data 64 # number of demand (read+write) MSHR hits
system.cpu.dcache.demand_mshr_hits::total 64 # number of demand (read+write) MSHR hits
system.cpu.dcache.overall_mshr_hits::cpu.data 64 # number of overall MSHR hits
system.cpu.dcache.overall_mshr_hits::total 64 # number of overall MSHR hits
system.cpu.dcache.ReadReq_mshr_misses::cpu.data 90 # number of ReadReq MSHR misses
system.cpu.dcache.ReadReq_mshr_misses::total 90 # number of ReadReq MSHR misses
system.cpu.dcache.WriteReq_mshr_misses::cpu.data 212 # number of WriteReq MSHR misses
system.cpu.dcache.WriteReq_mshr_misses::total 212 # number of WriteReq MSHR misses
system.cpu.dcache.demand_mshr_misses::cpu.data 302 # number of demand (read+write) MSHR misses
system.cpu.dcache.demand_mshr_misses::total 302 # number of demand (read+write) MSHR misses
system.cpu.dcache.overall_mshr_misses::cpu.data 302 # number of overall MSHR misses
system.cpu.dcache.overall_mshr_misses::total 302 # number of overall MSHR misses
system.cpu.dcache.ReadReq_mshr_miss_latency::cpu.data 6845000 # number of ReadReq MSHR miss cycles
system.cpu.dcache.ReadReq_mshr_miss_latency::total 6845000 # number of ReadReq MSHR miss cycles
system.cpu.dcache.WriteReq_mshr_miss_latency::cpu.data 14617000 # number of WriteReq MSHR miss cycles
system.cpu.dcache.WriteReq_mshr_miss_latency::total 14617000 # number of WriteReq MSHR miss cycles
system.cpu.dcache.demand_mshr_miss_latency::cpu.data 21462000 # number of demand (read+write) MSHR miss cycles
system.cpu.dcache.demand_mshr_miss_latency::total 21462000 # number of demand (read+write) MSHR miss cycles
system.cpu.dcache.overall_mshr_miss_latency::cpu.data 21462000 # number of overall MSHR miss cycles
system.cpu.dcache.overall_mshr_miss_latency::total 21462000 # number of overall MSHR miss cycles
system.cpu.dcache.ReadReq_mshr_miss_rate::cpu.data 0.000224 # mshr miss rate for ReadReq accesses
system.cpu.dcache.ReadReq_mshr_miss_rate::total 0.000224 # mshr miss rate for ReadReq accesses
system.cpu.dcache.WriteReq_mshr_miss_rate::cpu.data 0.000901 # mshr miss rate for WriteReq accesses
system.cpu.dcache.WriteReq_mshr_miss_rate::total 0.000901 # mshr miss rate for WriteReq accesses
system.cpu.dcache.demand_mshr_miss_rate::cpu.data 0.000475 # mshr miss rate for demand accesses
system.cpu.dcache.demand_mshr_miss_rate::total 0.000475 # mshr miss rate for demand accesses
system.cpu.dcache.overall_mshr_miss_rate::cpu.data 0.000475 # mshr miss rate for overall

accesses
system.cpu.dcache.overall_mshr_miss_rate::total 0.000475 # mshr miss rate for overall accesses
system.cpu.dcache.ReadReq_avg_mshr_miss_latency::cpu.data 76055.555556 # average ReadReq mshr miss latency
system.cpu.dcache.ReadReq_avg_mshr_miss_latency::total 76055.555556 # average ReadReq mshr miss latency
system.cpu.dcache.WriteReq_avg_mshr_miss_latency::cpu.data 68948.113208 # average WriteReq mshr miss latency
system.cpu.dcache.WriteReq_avg_mshr_miss_latency::total 68948.113208 # average WriteReq mshr miss latency
system.cpu.dcache.demand_avg_mshr_miss_latency::cpu.data 71066.225166 # average overall mshr miss latency
system.cpu.dcache.demand_avg_mshr_miss_latency::total 71066.225166 # average overall mshr miss latency
system.cpu.dcache.overall_avg_mshr_miss_latency::cpu.data 71066.225166 # average overall mshr miss latency
system.cpu.dcache.overall_avg_mshr_miss_latency::total 71066.225166 # average overall mshr miss latency
system.cpu.dcache.no_allocate_misses 0 # Number of misses that were no-allocate
system.cpu.icache.tags.replacements 32 # number of replacements
system.cpu.icache.tags.tagsinuse 345.941109 # Cycle average of tags in use
system.cpu.icache.tags.total_refs 597949 # Total number of references to valid blocks.
system.cpu.icache.tags.sampled_refs 438 # Sample count of references to valid blocks.
system.cpu.icache.tags.avg_refs 1365.180365 # Average number of references to valid blocks.
system.cpu.icache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.icache.tags.occ_blocks::cpu.inst 345.941109 # Average occupied blocks per requestor
system.cpu.icache.tags.occ_percent::cpu.inst 0.675666 # Average percentage of cache occupancy
system.cpu.icache.tags.occ_percent::total 0.675666 # Average percentage of cache occupancy
system.cpu.icache.tags.occ_task_id_blocks::1024 406 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::0 65 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::2 133 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::3 208 # Occupied blocks per task id
system.cpu.icache.tags.occ_task_id_percent::1024 0.792969 # Percentage of cache occupancy per task id
system.cpu.icache.tags.tag_accesses 2394294 # Number of tag accesses
system.cpu.icache.tags.data_accesses 2394294 # Number of data accesses
system.cpu.icache.ReadReq_hits::cpu.inst 597949 # number of ReadReq hits
system.cpu.icache.ReadReq_hits::total 597949 # number of ReadReq hits
system.cpu.icache.demand_hits::cpu.inst 597949 # number of demand (read+write) hits
system.cpu.icache.demand_hits::total 597949 # number of demand (read+write) hits
system.cpu.icache.overall_hits::cpu.inst 597949 # number of overall hits
system.cpu.icache.overall_hits::total 597949 # number of overall hits
system.cpu.icache.ReadReq_misses::cpu.inst 515 # number of ReadReq misses
system.cpu.icache.ReadReq_misses::total 515 # number of ReadReq misses
system.cpu.icache.demand_misses::cpu.inst 515 # number of demand (read+write) misses

system.cpu.icache.demand_misses::total 515 # number of demand (read+write) misses
system.cpu.icache.overall_misses::cpu.inst 515 # number of overall misses
system.cpu.icache.overall_misses::total 515 # number of overall misses
system.cpu.icache.ReadReq_miss_latency::cpu.inst 35176500 # number of ReadReq miss cycles
system.cpu.icache.ReadReq_miss_latency::total 35176500 # number of ReadReq miss cycles
system.cpu.icache.demand_miss_latency::cpu.inst 35176500 # number of demand (read+write) miss cycles
system.cpu.icache.demand_miss_latency::total 35176500 # number of demand (read+write) miss cycles
system.cpu.icache.overall_miss_latency::cpu.inst 35176500 # number of overall miss cycles
system.cpu.icache.overall_miss_latency::total 35176500 # number of overall miss cycles
system.cpu.icache.ReadReq_accesses::cpu.inst 598464 # number of ReadReq accesses(hits+misses)
system.cpu.icache.ReadReq_accesses::total 598464 # number of ReadReq accesses(hits+misses)
system.cpu.icache.demand_accesses::cpu.inst 598464 # number of demand (read+write) accesses
system.cpu.icache.demand_accesses::total 598464 # number of demand (read+write) accesses
system.cpu.icache.overall_accesses::cpu.inst 598464 # number of overall (read+write) accesses
system.cpu.icache.overall_accesses::total 598464 # number of overall (read+write) accesses
system.cpu.icache.ReadReq_miss_rate::cpu.inst 0.000861 # miss rate for ReadReq accesses
system.cpu.icache.ReadReq_miss_rate::total 0.000861 # miss rate for ReadReq accesses
system.cpu.icache.demand_miss_rate::cpu.inst 0.000861 # miss rate for demand accesses
system.cpu.icache.demand_miss_rate::total 0.000861 # miss rate for demand accesses
system.cpu.icache.overall_miss_rate::cpu.inst 0.000861 # miss rate for overall accesses
system.cpu.icache.overall_miss_rate::total 0.000861 # miss rate for overall accesses
system.cpu.icache.ReadReq_avg_miss_latency::cpu.inst 68303.883495 # average ReadReq miss latency
system.cpu.icache.ReadReq_avg_miss_latency::total 68303.883495 # average ReadReq miss latency
system.cpu.icache.demand_avg_miss_latency::cpu.inst 68303.883495 # average overall miss latency
system.cpu.icache.demand_avg_miss_latency::total 68303.883495 # average overall miss latency
system.cpu.icache.overall_avg_miss_latency::cpu.inst 68303.883495 # average overall miss latency
system.cpu.icache.overall_avg_miss_latency::total 68303.883495 # average overall miss latency
system.cpu.icache.blocked_cycles::no_mshrs 32 # number of cycles access was blocked
system.cpu.icache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.icache.blocked::no_mshrs 1 # number of cycles access was blocked
system.cpu.icache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.icache.avg_blocked_cycles::no_mshrs 32 # average number of cycles each access was blocked
system.cpu.icache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.icache.fast_writes 0 # number of fast writes performed

system.cpu.icache.cache_copies 0 # number of cache copies performed
system.cpu.icache.ReadReq_mshr_hits::cpu.inst 76 # number of ReadReq MSHR hits
system.cpu.icache.ReadReq_mshr_hits::total 76 # number of ReadReq MSHR hits
system.cpu.icache.demand_mshr_hits::cpu.inst 76 # number of demand (read+write) MSHR hits
system.cpu.icache.demand_mshr_hits::total 76 # number of demand (read+write) MSHR hits
system.cpu.icache.overall_mshr_hits::cpu.inst 76 # number of overall MSHR hits
system.cpu.icache.overall_mshr_hits::total 76 # number of overall MSHR hits
system.cpu.icache.ReadReq_mshr_misses::cpu.inst 439 # number of ReadReq MSHR misses
system.cpu.icache.ReadReq_mshr_misses::total 439 # number of ReadReq MSHR misses
system.cpu.icache.demand_mshr_misses::cpu.inst 439 # number of demand (read+write) MSHR misses
system.cpu.icache.demand_mshr_misses::total 439 # number of demand (read+write) MSHR misses
system.cpu.icache.overall_mshr_misses::cpu.inst 439 # number of overall MSHR misses
system.cpu.icache.overall_mshr_misses::total 439 # number of overall MSHR misses
system.cpu.icache.ReadReq_mshr_miss_latency::cpu.inst 30126000 # number of ReadReq MSHR miss cycles
system.cpu.icache.ReadReq_mshr_miss_latency::total 30126000 # number of ReadReq MSHR miss cycles
system.cpu.icache.demand_mshr_miss_latency::cpu.inst 30126000 # number of demand (read+write) MSHR miss cycles
system.cpu.icache.demand_mshr_miss_latency::total 30126000 # number of demand (read+write) MSHR miss cycles
system.cpu.icache.overall_mshr_miss_latency::cpu.inst 30126000 # number of overall MSHR miss cycles
system.cpu.icache.overall_mshr_miss_latency::total 30126000 # number of overall MSHR miss cycles
system.cpu.icache.ReadReq_mshr_miss_rate::cpu.inst 0.000734 # mshr miss rate for ReadReq accesses
system.cpu.icache.ReadReq_mshr_miss_rate::total 0.000734 # mshr miss rate for ReadReq accesses
system.cpu.icache.demand_mshr_miss_rate::cpu.inst 0.000734 # mshr miss rate for demand accesses
system.cpu.icache.demand_mshr_miss_rate::total 0.000734 # mshr miss rate for demand accesses
system.cpu.icache.overall_mshr_miss_rate::cpu.inst 0.000734 # mshr miss rate for overall accesses
system.cpu.icache.overall_mshr_miss_rate::total 0.000734 # mshr miss rate for overall accesses
system.cpu.icache.ReadReq_avg_mshr_miss_latency::cpu.inst 68624.145786 # average ReadReq mshr miss latency
system.cpu.icache.ReadReq_avg_mshr_miss_latency::total 68624.145786 # average ReadReq mshr miss latency
system.cpu.icache.demand_avg_mshr_miss_latency::cpu.inst 68624.145786 # average overall mshr miss latency
system.cpu.icache.demand_avg_mshr_miss_latency::total 68624.145786 # average overall mshr miss latency
system.cpu.icache.overall_avg_mshr_miss_latency::cpu.inst 68624.145786 # average overall mshr miss latency

system.cpu.icache.overall_avg_mshr_miss_latency::total 68624.145786 # average overall mshr miss latency
system.cpu.icache.no_allocate_misses 0 # Number of misses that were no-allocate
system.cpu.l2cache.tags.replacements 0 # number of replacements
system.cpu.l2cache.tags.tagsinuse 438.960073 # Cycle average of tags in use
system.cpu.l2cache.tags.total_refs 6 # Total number of references to valid blocks.
system.cpu.l2cache.tags.sampled_refs 531 # Sample count of references to valid blocks.
system.cpu.l2cache.tags.avg_refs 0.011299 # Average number of references to valid blocks.
system.cpu.l2cache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.l2cache.tags.occ_blocks::writebacks 5.288939 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_blocks::cpu.inst 356.250786 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_blocks::cpu.data 77.420348 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_percent::writebacks 0.000081 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::cpu.inst 0.005436 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::cpu.data 0.001181 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::total 0.006698 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_task_id_blocks::1024 531 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::0 76 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::2 154 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::3 301 # Occupied blocks per task id
system.cpu.l2cache.tags.occ_task_id_percent::1024 0.008102 # Percentage of cache occupancy per task id
system.cpu.l2cache.tags.tag_accesses 6743 # Number of tag accesses
system.cpu.l2cache.tags.data_accesses 6743 # Number of data accesses
system.cpu.l2cache.ReadReq_hits::cpu.inst 3 # number of ReadReq hits
system.cpu.l2cache.ReadReq_hits::cpu.data 1 # number of ReadReq hits
system.cpu.l2cache.ReadReq_hits::total 4 # number of ReadReq hits
system.cpu.l2cache.Writeback_hits::writebacks 9 # number of Writeback hits
system.cpu.l2cache.Writeback_hits::total 9 # number of Writeback hits
system.cpu.l2cache.demand_hits::cpu.inst 3 # number of demand (read+write) hits
system.cpu.l2cache.demand_hits::cpu.data 1 # number of demand (read+write) hits
system.cpu.l2cache.demand_hits::total 4 # number of demand (read+write) hits
system.cpu.l2cache.overall_hits::cpu.inst 3 # number of overall hits
system.cpu.l2cache.overall_hits::cpu.data 1 # number of overall hits
system.cpu.l2cache.overall_hits::total 4 # number of overall hits
system.cpu.l2cache.ReadReq_misses::cpu.inst 436 # number of ReadReq misses
system.cpu.l2cache.ReadReq_misses::cpu.data 89 # number of ReadReq misses
system.cpu.l2cache.ReadReq_misses::total 525 # number of ReadReq misses
system.cpu.l2cache.ReadExReq_misses::cpu.data 212 # number of ReadExReq misses
system.cpu.l2cache.ReadExReq_misses::total 212 # number of ReadExReq misses
system.cpu.l2cache.demand_misses::cpu.inst 436 # number of demand (read+write) misses
system.cpu.l2cache.demand_misses::cpu.data 301 # number of demand (read+write) misses
system.cpu.l2cache.demand_misses::total 737 # number of demand (read+write) misses

system.cpu.l2cache.overall_misses::cpu.inst 436 # number of overall misses
system.cpu.l2cache.overall_misses::cpu.data 301 # number of overall misses
system.cpu.l2cache.overall_misses::total 737 # number of overall misses
system.cpu.l2cache.ReadReq_miss_latency::cpu.inst 29653500 # number of ReadReq miss cycles
system.cpu.l2cache.ReadReq_miss_latency::cpu.data 6653000 # number of ReadReq miss cycles
system.cpu.l2cache.ReadReq_miss_latency::total 36306500 # number of ReadReq miss cycles
system.cpu.l2cache.ReadExReq_miss_latency::cpu.data 14193000 # number of ReadExReq miss cycles
system.cpu.l2cache.ReadExReq_miss_latency::total 14193000 # number of ReadExReq miss cycles
system.cpu.l2cache.demand_miss_latency::cpu.inst 29653500 # number of demand (read+write) miss cycles
system.cpu.l2cache.demand_miss_latency::cpu.data 20846000 # number of demand (read+write) miss cycles
system.cpu.l2cache.demand_miss_latency::total 50499500 # number of demand (read+write) miss cycles
system.cpu.l2cache.overall_miss_latency::cpu.inst 29653500 # number of overall miss cycles
system.cpu.l2cache.overall_miss_latency::cpu.data 20846000 # number of overall miss cycles
system.cpu.l2cache.overall_miss_latency::total 50499500 # number of overall miss cycles
system.cpu.l2cache.ReadReq_accesses::cpu.inst 439 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.ReadReq_accesses::cpu.data 90 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.ReadReq_accesses::total 529 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.Writeback_accesses::writebacks 9 # number of Writeback accesses(hits+misses)
system.cpu.l2cache.Writeback_accesses::total 9 # number of Writeback accesses(hits+misses)
system.cpu.l2cache.ReadExReq_accesses::cpu.data 212 # number of ReadExReq accesses(hits+misses)
system.cpu.l2cache.ReadExReq_accesses::total 212 # number of ReadExReq accesses(hits+misses)
system.cpu.l2cache.demand_accesses::cpu.inst 439 # number of demand (read+write) accesses
system.cpu.l2cache.demand_accesses::cpu.data 302 # number of demand (read+write) accesses
system.cpu.l2cache.demand_accesses::total 741 # number of demand (read+write) accesses
system.cpu.l2cache.overall_accesses::cpu.inst 439 # number of overall (read+write) accesses
system.cpu.l2cache.overall_accesses::cpu.data 302 # number of overall (read+write) accesses
system.cpu.l2cache.overall_accesses::total 741 # number of overall (read+write) accesses
system.cpu.l2cache.ReadReq_miss_rate::cpu.inst 0.993166 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_miss_rate::cpu.data 0.988889 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_miss_rate::total 0.992439 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadExReq_miss_rate::cpu.data 1 # miss rate for ReadExReq accesses
system.cpu.l2cache.ReadExReq_miss_rate::total 1 # miss rate for ReadExReq accesses

system.cpu.l2cache.demand_miss_rate::cpu.inst 0.993166 # miss rate for demand accesses
system.cpu.l2cache.demand_miss_rate::cpu.data 0.996689 # miss rate for demand accesses
system.cpu.l2cache.demand_miss_rate::total 0.994602 # miss rate for demand accesses
system.cpu.l2cache.overall_miss_rate::cpu.inst 0.993166 # miss rate for overall accesses
system.cpu.l2cache.overall_miss_rate::cpu.data 0.996689 # miss rate for overall accesses
system.cpu.l2cache.overall_miss_rate::total 0.994602 # miss rate for overall accesses
system.cpu.l2cache.ReadReq_avg_miss_latency::cpu.inst 68012.614679 # average ReadReq miss latency
system.cpu.l2cache.ReadReq_avg_miss_latency::cpu.data 74752.808989 # average ReadReq miss latency
system.cpu.l2cache.ReadReq_avg_miss_latency::total 69155.238095 # average ReadReq miss latency
system.cpu.l2cache.ReadExReq_avg_miss_latency::cpu.data 66948.113208 # average ReadExReq miss latency
system.cpu.l2cache.ReadExReq_avg_miss_latency::total 66948.113208 # average ReadExReq miss latency
system.cpu.l2cache.demand_avg_miss_latency::cpu.inst 68012.614679 # average overall miss latency
system.cpu.l2cache.demand_avg_miss_latency::cpu.data 69255.813953 # average overall miss latency
system.cpu.l2cache.demand_avg_miss_latency::total 68520.352782 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::cpu.inst 68012.614679 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::cpu.data 69255.813953 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::total 68520.352782 # average overall miss latency
system.cpu.l2cache.blocked_cycles::no_mshrs 0 # number of cycles access was blocked
system.cpu.l2cache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.l2cache.blocked::no_mshrs 0 # number of cycles access was blocked
system.cpu.l2cache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.l2cache.avg_blocked_cycles::no_mshrs nan # average number of cycles each access was blocked
system.cpu.l2cache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.l2cache.fast_writes 0 # number of fast writes performed
system.cpu.l2cache.cache_copies 0 # number of cache copies performed
system.cpu.l2cache.ReadReq_mshr_misses::cpu.inst 436 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadReq_mshr_misses::cpu.data 89 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadReq_mshr_misses::total 525 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadExReq_mshr_misses::cpu.data 212 # number of ReadExReq MSHR misses
system.cpu.l2cache.ReadExReq_mshr_misses::total 212 # number of ReadExReq MSHR misses
system.cpu.l2cache.demand_mshr_misses::cpu.inst 436 # number of demand (read+write) MSHR misses
system.cpu.l2cache.demand_mshr_misses::cpu.data 301 # number of demand (read+write) MSHR misses

system.cpu.l2cache.demand_mshr_misses::total 737 # number of demand (read+write) MSHR misses
system.cpu.l2cache.overall_mshr_misses::cpu.inst 436 # number of overall MSHR misses
system.cpu.l2cache.overall_mshr_misses::cpu.data 301 # number of overall MSHR misses
system.cpu.l2cache.overall_mshr_misses::total 737 # number of overall MSHR misses
system.cpu.l2cache.ReadReq_mshr_miss_latency::cpu.inst 27288500 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_latency::cpu.data 6175000 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_latency::total 33463500 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadExReq_mshr_miss_latency::cpu.data 13059000 # number of ReadExReq MSHR miss cycles
system.cpu.l2cache.ReadExReq_mshr_miss_latency::total 13059000 # number of ReadExReq MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::cpu.inst 27288500 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::cpu.data 19234000 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::total 46522500 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::cpu.inst 27288500 # number of overall MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::cpu.data 19234000 # number of overall MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::total 46522500 # number of overall MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_rate::cpu.inst 0.993166 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_mshr_miss_rate::cpu.data 0.988889 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_mshr_miss_rate::total 0.992439 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadExReq_mshr_miss_rate::cpu.data 1 # mshr miss rate for ReadExReq accesses
system.cpu.l2cache.ReadExReq_mshr_miss_rate::total 1 # mshr miss rate for ReadExReq accesses
system.cpu.l2cache.demand_mshr_miss_rate::cpu.inst 0.993166 # mshr miss rate for demand accesses
system.cpu.l2cache.demand_mshr_miss_rate::cpu.data 0.996689 # mshr miss rate for demand accesses
system.cpu.l2cache.demand_mshr_miss_rate::total 0.994602 # mshr miss rate for demand accesses
system.cpu.l2cache.overall_mshr_miss_rate::cpu.inst 0.993166 # mshr miss rate for overall accesses
system.cpu.l2cache.overall_mshr_miss_rate::cpu.data 0.996689 # mshr miss rate for overall accesses
system.cpu.l2cache.overall_mshr_miss_rate::total 0.994602 # mshr miss rate for overall accesses
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::cpu.inst 62588.302752 # average

ReadReq mshr miss latency
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::cpu.data 69382.022472 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::total 63740 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadExReq_avg_mshr_miss_latency::cpu.data 61599.056604 # average ReadExReq mshr miss latency
system.cpu.l2cache.ReadExReq_avg_mshr_miss_latency::total 61599.056604 # average ReadExReq mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::cpu.inst 62588.302752 # average overall mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::cpu.data 63900.332226 # average overall mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::total 63124.151967 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::cpu.inst 62588.302752 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::cpu.data 63900.332226 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::total 63124.151967 # average overall mshr miss latency
system.cpu.l2cache.no_allocate_misses 0 # Number of misses that were no-allocate
system.l2bus.trans_dist::ReadReq 529 # Transaction distribution
system.l2bus.trans_dist::ReadResp 528 # Transaction distribution
system.l2bus.trans_dist::Writeback 9 # Transaction distribution
system.l2bus.trans_dist::ReadExReq 212 # Transaction distribution
system.l2bus.trans_dist::ReadExResp 212 # Transaction distribution
system.l2bus.pkt_count_system.cpu.icache.mem_side::system.cpu.l2cache.cpu_side 877 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_count_system.cpu.dcache.mem_side::system.cpu.l2cache.cpu_side 613 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_count::total 1490 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_size_system.cpu.icache.mem_side::system.cpu.l2cache.cpu_side 28032 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.pkt_size_system.cpu.dcache.mem_side::system.cpu.l2cache.cpu_side 19904 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.pkt_size::total 47936 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.snoops 0 # Total snoops (count)
system.l2bus.snoop_fanout::samples 750 # Request fanout histogram
system.l2bus.snoop_fanout::mean 1 # Request fanout histogram
system.l2bus.snoop_fanout::stdev 0 # Request fanout histogram
system.l2bus.snoop_fanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.l2bus.snoop_fanout::0 0 0.00% 0.00% # Request fanout histogram
system.l2bus.snoop_fanout::1 750 100.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::2 0 0.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::min_value 1 # Request fanout histogram
system.l2bus.snoop_fanout::max_value 1 # Request fanout histogram
system.l2bus.snoop_fanout::total 750 # Request fanout histogram

system.l2bus.reqLayer0.occupancy 393000 # Layer occupancy (ticks)
system.l2bus.reqLayer0.utilization 0.0 # Layer utilization (%)
system.l2bus.respLayer0.occupancy 1190000 # Layer occupancy (ticks)
system.l2bus.respLayer0.utilization 0.1 # Layer utilization (%)
system.l2bus.respLayer1.occupancy 808500 # Layer occupancy (ticks)
system.l2bus.respLayer1.utilization 0.1 # Layer utilization (%)
system.membus.trans_dist::ReadReq 524 # Transaction distribution
system.membus.trans_dist::ReadResp 524 # Transaction distribution
system.membus.trans_dist::ReadExReq 212 # Transaction distribution
system.membus.trans_dist::ReadExResp 212 # Transaction distribution
system.membus.pkt_count_system.cpu.l2cache.mem_side::system.mem_ctrl.port 1472 # Packet count per connected master and slave (bytes)
system.membus.pkt_count_system.cpu.l2cache.mem_side::total 1472 # Packet count per connected master and slave (bytes)
system.membus.pkt_count::total 1472 # Packet count per connected master and slave (bytes)
system.membus.pkt_size_system.cpu.l2cache.mem_side::system.mem_ctrl.port 47104 # Cumulative packet size per connected master and slave (bytes)
system.membus.pkt_size_system.cpu.l2cache.mem_side::total 47104 # Cumulative packet size per connected master and slave (bytes)
system.membus.pkt_size::total 47104 # Cumulative packet size per connected master and slave (bytes)
system.membus.snoops 0 # Total snoops (count)
system.membus.snoop_fanout::samples 736 # Request fanout histogram
system.membus.snoop_fanout::mean 0 # Request fanout histogram
system.membus.snoop_fanout::stdev 0 # Request fanout histogram
system.membus.snoop_fanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.membus.snoop_fanout::0 736 100.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::1 0 0.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::min_value 0 # Request fanout histogram
system.membus.snoop_fanout::max_value 0 # Request fanout histogram
system.membus.snoop_fanout::total 736 # Request fanout histogram
system.membus.reqLayer2.occupancy 368000 # Layer occupancy (ticks)
system.membus.reqLayer2.utilization 0.0 # Layer utilization (%)
system.membus.respLayer0.occupancy 1988500 # Layer occupancy (ticks)
system.membus.respLayer0.utilization 0.2 # Layer utilization (%)