Verificando arquivos...
Código-fonte do programa: Blocos_outro_vetor.c
Arquivo de configuração de CPU: MyO3CPU.py --> MyO3CPU.py
Arquivo de configuração de caches e memória: MyCaches.py --> MyCaches.py
Arquivo de configuração de sistema: MySystem.py --> MySystem.py

**********
* Compilando o programa ...
* g++ -static Blocos_outro_vetor.c -o Blocos_outro_vetor
**********

**********
* Executando o gem5...
* gem5 --outdir=m5out MySimulation.py -c Blocos_outro_vetor
**********

gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 compiled Feb 16 2016 16:35:34
gem5 started Dec 14 2017 15:09:22
gem5 executing on simulacaolse3
command line: gem5 --outdir=m5out MySimulation.py -c Blocos_outro_vetor

Programa a ser executado: Blocos_outro_vetor
Global frequency set at 1000000000000 ticks per second
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb.listener: listening for remote gdb on port 7003

---------- Begin Simulation ----------
info: Entering event queue @ 0. Starting simulation...

Vetor
info: Increasing stack size by one page.
23, 9, 16, 29, 23, 1, 22, 13, 33, 5, 6, 40, 0, 46, 2, 2, 3, 48, 45, 8, 8, 34, 0, 13, 24, 18, 18, 17, 39, 27, 28, 13, 38, 44, 44, 13, 47, 18, 26, 32, 23, 32, 22, 24, 31, 27, 28, 36, 25, 24, 45, 33, 10, 45, 49, 34, 16, 17, 2, 7, 46, 32, 22, 34, 28, 16, 49, 25, 34, 26, 7, 10, 8, 32, 34, 41, 9, 12, 28, 36, 38, 23, 19, 49, 20, 18, 33, 36, 37, 37, 46, 35, 19, 18, 21, 47, 35, 21, 24, 21, 47, 32, 31, 7, 16, 17, 49, 27, 30, 27, 13, 20, 2, 34, 19, 22, 3, 5, 11, 42, 42, 7, 28, 12, 25, 1, 11, 12, 22, 38, 34, 19, 22, 17, 29, 38, 35, 28, 15, 17, 7, 30, 37, 9, 14, 7, 31, 17, 12, 44, 12, 6, 1, 42, 18, 29, 43, 32, 43, 16, 20, 29, 37, 44, 47, 16, 32, 34, 46, 49, 1, 3, 29, 38, 12, 43, 47, 46, 13, 11, 42, 27, 18, 46, 21, 38, 27, 14, 22, 20, 32, 44, 2, 22, 38, 1, 38, 22, 35, 37, 21, 36, 40, 2, 26, 5, 48, 24, 3, 11, 37, 45, 40, 5, 43, 11, 44, 20, 25, 18, 43, 10, 13, 45, 32, 1, 46, 22, 24, 31, 9, 47, 19, 2, 0, 45, 9, 48, 21, 12, 11, 11, 9, 1, 16, 5, 12, 12, 25, 39, 31, 18, 49, 44, 15, 33, 47, 13, 6, 21, 46, 17, 19, 15, 21, 21, 13, 30, 19, 36, 44, 30, 47, 6, 31, 14, 11, 45, 28, 38, 34, 11, 9, 34, 7, 24, 17, 5, 38, 25, 26, 34, 45, 47, 2, 16, 18, 15, 47, 39, 1, 43, 21, 49, 49, 4, 15, 10, 49, 45, 1, 34, 7, 10, 20, 14, 34, 39, 19, 24, 15, 48, 11, 12, 47, 13, 28, 18, 30, 25, 7, 33, 21, 31, 34, 20, 35, 49, 33, 37, 47, 34, 21, 4, 44, 43, 18, 30, 32, 40, 5, 49, 40, 16, 11, 37, 31, 42, 7, 11, 19, 17, 44, 40,

48, 29, 11, 33, 30, 44, 20, 27, 30, 43, 33, 24, 36, 4, 4, 21, 44, 11, 22, 36, 29, 36, 25, 10, 28,
33, 23, 47, 0, 20, 38, 0, 1, 1, 33, 33, 47, 6, 11, 27, 1, 44, 1, 40, 0, 7, 13, 46, 19, 35, 32, 48, 21,
8, 11, 1, 43, 36, 49, 43, 6, 39, 45, 7, 40, 28, 41, 39, 36, 4, 16, 40, 0, 19, 30, 1, 26, 43, 47, 45,
28, 32, 46, 2, 40, 9, 3, 35, 45, 4, 30, 4, 43, 25, 11, 35, 5, 4, 24, 42, 10, 42, 32, 13, 11, 14, 14,
38, 7, 13, 35, 37, 45, 33, 39, 37, 42, 45, 24, 40, 49, 4, 44, 45, 29, 7, 30, 35, 14, 7, 29, 24, 49,
13, 37, 11, 27, 3, 1, 36, 19, 36, 23, 16, 22, 13, 6, 14, 8, 30, 6, 9, 37, 0, 4, 18, 8, 37, 3, 22, 44,
34, 48, 45, 49, 38, 8, 26, 43, 9, 12, 12, 48, 36, 31, 20, 1, 39, 36, 11, 21, 43, 20, 8, 43, 27, 27,
3, 14, 32, 25, 10, 19, 24, 5, 18, 14, 14, 47, 7, 25, 9, 22, 25, 47, 5, 47, 0, 44, 34, 13, 15, 29, 36,
26, 24, 13, 5, 28, 29, 39, 5, 39, 8, 31, 44, 29, 45, 10, 26, 5, 36, 37, 27, 11, 35, 32, 11, 37, 28,
45, 1, 43, 26, 39, 21, 2, 2, 26, 30, 31, 16, 38, 20, 26, 21, 16, 5, 19, 27, 31, 24, 15, 19, 1, 28, 6,
35, 39, 45, 13, 36, 48, 8, 14, 37, 30, 17, 41, 8, 47, 24, 26, 37, 44, 5, 9, 13, 10, 28, 42, 44, 4, 9,
13, 7, 37, 21, 42, 29, 16, 7, 15, 15, 15, 30, 4, 47, 49, 46, 8, 48, 20, 36, 36, 17, 41, 47, 30, 2,
27, 24, 46, 31, 33, 11, 38, 20, 34, 32, 1, 2, 39, 19, 19, 6, 1, 24, 6, 0, 20, 14, 48, 40, 0, 34, 9,
42, 33, 39, 46, 10, 15, 44, 41, 48, 5, 31, 19, 41, 13, 22, 43, 4, 41, 13, 11, 42, 37, 17, 42, 9, 33,
41, 1, 35, 27, 11, 29, 11, 2, 25, 21, 18, 19, 15, 16, 26, 48, 37, 17, 12, 10, 13, 18, 1, 26, 31, 44,
15, 0, 38, 26, 33, 29, 27, 21, 9, 40, 0, 20, 45, 26, 43, 13, 47, 10, 31, 24, 9, 21, 43, 23, 31, 6,
41, 34, 34, 23, 30, 1, 23, 19, 27, 9, 0, 7, 30, 9, 49, 30, 31, 44, 8, 25, 9, 6, 35, 41, 32, 44, 12,
25, 17, 45, 34, 11, 29, 18, 34, 12, 22, 9, 31, 49, 18, 33, 8, 0, 45, 8, 33, 26, 2, 41, 3, 14, 49, 39,
5, 33, 35, 19, 11, 5, 16, 45, 16, 45, 15, 2, 9, 37, 13, 42, 39, 34, 26, 47, 34, 21, 7, 17, 49, 12,
11, 3, 26, 12, 42, 33, 46, 29, 2, 7, 34, 18, 4, 2, 15, 19, 4, 25, 9, 18, 19, 48, 2, 45, 47, 38, 18, 7,
8, 18, 19, 19, 21, 47, 31, 15, 30, 29, 44, 34, 36, 31, 4, 40, 33, 21, 12, 40, 48, 21, 8, 18, 21, 12,
13, 20, 2, 34, 27, 10, 2, 48, 31, 25, 45, 13, 40, 25, 42, 34, 9, 31, 17, 15, 23, 1, 37, 35, 41, 35,
6, 1, 3, 29, 15, 19, 0, 17, 3, 29, 28, 7, 28, 9, 32, 23, 24, 22, 1, 19, 8, 12, 2, 26, 28, 25, 27, 15,
11, 20, 2, 19, 21, 8, 49, 36, 27, 1, 3, 32, 30, 33, 39, 10, 45, 21, 34, 19, 45, 35, 40,
Vetor ordenado
32, 45, 24, 35, 38, 46, 46, 4, 51, 53, 42, 13, 42, 35, 66, 41, 82, 57, 65, 58, 55, 46, 58, 64, 49,
78, 55, 83, 33, 9, 78, 56, 44, 74, 60, 17, 40, 75, 21, 64, 61, 68, 38, 69, 74, 81, 37, 68, 56, 45,
79, 38, 33, 76, 57, 33, 36, 41, 8, 53, 49, 40, 26, 23, 60, 53, 39, 67, 63, 32, 37, 46, 21, 48, 56,
18, 43, 47, 75, 59, 49, 81, 63, 66, 95, 4, 67, 55, 93, 24, 69, 64, 59, 41, 42, 76, 24, 39, 60, 72,
57, 42, 31, 72, 14, 82, 45, 54, 64, 43, 53, 58, 33, 68, 55, 56, 21, 45, 57, 33, 22, 10, 21, 24, 64,
49, 93, 48, 60, 27, 63, 34, 42, 43, 55, 74, 53, 45, 56, 66, 45, 43, 31, 22, 63, 60, 92, 18, 33, 86,
44, 70, 53, 25, 94, 35, 17, 34, 73, 43, 63, 23, 60, 46, 55, 40, 52, 54, 84, 70, 81, 25, 87, 48, 72,
54, 56, 48, 73, 18, 36, 84, 77, 44, 74, 47, 73, 57, 40, 25, 55, 58, 65, 35, 61, 70, 20, 38, 2, 66,
53, 38, 45, 41, 7, 59, 54, 80, 29, 12, 79, 92, 45, 52, 68, 80, 40, 56, 19, 31, 69, 92, 60, 48, 49,
38, 49, 34, 68, 46, 9, 66, 52, 45, 25, 52, 20, 72, 78, 76, 87, 64, 53, 89, 36, 65, 21, 53, 62, 48,
30, 37, 55, 39, 35, 20, 38, 15, 37, 22, 45, 25, 78, 93, 87, 34, 52, 24, 84, 51, 40, 47, 64, 28, 70,
30, 46, 35, 43, 23, 28, 54, 34, 47, 52, 47, 78, 28, 65, 50, 18, 57, 44, 47, 75, 74, 36, 41, 64, 46,
43, 65, 46, 69, 60, 4, 56, 47, 58, 47, 21, 46, 55, 34, 29, 41, 84, 49, 56, 51, 47, 49, 71, 63, 49,
22, 38, 86, 13, 20, 58, 71, 23, 30, 45, 51, 95, 56, 56, 53, 88, 32, 51, 77, 44, 58, 66, 3, 58, 25,
25, 6, 34, 88, 34, 51, 72, 56, 59, 89, 36, 60, 35, 47, 54, 53, 54, 51, 74, 36, 38, 40, 27, 39, 34,
42, 85, 29, 23, 19, 57, 59, 38, 59, 56, 30, 40, 65, 69, 60, 41, 33, 64, 54, 47, 68, 53, 24, 46, 9,
37, 58, 61, 52, 34, 41, 73, 56, 42, 79, 40, 52, 34, 40, 67, 41, 45, 41, 28, 44, 63, 44, 68, 30, 21,
61, 60, 11, 50, 81, 60, 81, 28, 66, 23, 29, 54, 79, 31, 41, 22, 17, 23, 34, 37, 50, 92, 56, 15, 37,
40, 78, 45, 73, 70, 35, 73, 33, 88, 29, 39, 25, 22, 61, 12, 79, 70, 53, 67, 43, 48, 38, 38, 76, 41,
4, 44, 19, 20, 57, 35, 41, 47, 23, 27, 14, 54, 52, 26, 22, 40, 57, 63, 4, 62, 72, 55, 55, 64, 75,
Finishing simulation. Current tick: 645711000. Reason: target called exit()
---------- End Simulation ----------
**********
* Resultados da simulação
**********

sim_seconds 0.000646 # Number of seconds simulated
sim_ticks 645711000 # Number of ticks simulated
final_tick 645711000 # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
sim_freq 1000000000000 # Frequency of simulated ticks
host_inst_rate 111468 # Simulator instruction rate (inst/s)
host_op_rate 210739 # Simulator op (including micro ops) rate (op/s)
host_tick_rate 71735039 # Simulator tick rate (ticks/s)
host_mem_usage 654404 # Number of bytes of host memory used
host_seconds 9.00 # Real time elapsed on the host
sim_insts 1003354 # Number of instructions simulated
sim_ops 1896931 # Number of ops (including micro ops) simulated
system.clk_domain.voltage_domain.voltage 1 # Voltage in Volts
system.clk_domain.clock 500 # Clock period in ticks
system.mem_ctrl.bytes_read::cpu.inst 27456 # Number of bytes read from this memory
system.mem_ctrl.bytes_read::cpu.data 35392 # Number of bytes read from this memory
system.mem_ctrl.bytes_read::total 62848 # Number of bytes read from this memory
system.mem_ctrl.bytes_inst_read::cpu.inst 27456 # Number of instructions bytes read from this memory
system.mem_ctrl.bytes_inst_read::total 27456 # Number of instructions bytes read from this memory
system.mem_ctrl.num_reads::cpu.inst 429 # Number of read requests responded to by this memory
system.mem_ctrl.num_reads::cpu.data 553 # Number of read requests responded to by this memory
system.mem_ctrl.num_reads::total 982 # Number of read requests responded to by this memory
system.mem_ctrl.bw_read::cpu.inst 42520570 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_read::cpu.data 54810898 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_read::total 97331469 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_inst_read::cpu.inst 42520570 # Instruction read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_inst_read::total 42520570 # Instruction read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_total::cpu.inst 42520570 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.bw_total::cpu.data 54810898 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.bw_total::total 97331469 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.readReqs 982 # Number of read requests accepted
system.mem_ctrl.writeReqs 0 # Number of write requests accepted
system.mem_ctrl.readBursts 982 # Number of DRAM read bursts, including those serviced by the write queue
system.mem_ctrl.writeBursts 0 # Number of DRAM write bursts, including those merged in the write queue
system.mem_ctrl.bytesReadDRAM 62848 # Total number of bytes read from DRAM

system.mem_ctrl.bytesReadWrQ 0 # Total number of bytes read from write queue
system.mem_ctrl.bytesWritten 0 # Total number of bytes written to DRAM
system.mem_ctrl.bytesReadSys 62848 # Total read bytes from the system interface side
system.mem_ctrl.bytesWrittenSys 0 # Total written bytes from the system interface side
system.mem_ctrl.servicedByWrQ 0 # Number of DRAM read bursts serviced by the write queue
system.mem_ctrl.mergedWrBursts 0 # Number of DRAM write bursts merged with an existing one
system.mem_ctrl.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write
system.mem_ctrl.perBankRdBursts::0 72 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::1 122 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::2 74 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::3 60 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::4 68 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::5 36 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::6 175 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::7 137 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::8 95 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::9 32 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::10 30 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::11 17 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::12 30 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::13 27 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::14 5 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::15 2 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::0 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::1 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::2 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::3 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::4 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::5 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::6 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::7 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::8 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::9 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::10 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::11 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::12 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::13 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::14 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::15 0 # Per bank write bursts
system.mem_ctrl.numRdRetry 0 # Number of times read queue was full causing retry
system.mem_ctrl.numWrRetry 0 # Number of times write queue was full causing retry
system.mem_ctrl.totGap 645640000 # Total gap between requests
system.mem_ctrl.readPktSize::0 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::1 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::2 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::3 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::4 0 # Read request sizes (log2)

system.mem_ctrl.readPktSize::5 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::6 982 # Read request sizes (log2)
system.mem_ctrl.writePktSize::0 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::1 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::2 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::3 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::4 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::5 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::6 0 # Write request sizes (log2)
system.mem_ctrl.rdQLenPdf::0 772 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::1 163 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::2 43 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::3 4 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::4 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::5 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::6 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::7 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::8 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::9 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::10 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::11 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::12 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::13 0 # What read queue length does an incoming req see
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system.mem_ctrl.rdQLenPdf::15 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::16 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::17 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::18 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::19 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::20 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::21 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::22 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::23 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::24 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::25 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::26 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::27 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::28 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::29 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::30 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::31 0 # What read queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::0 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::1 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::2 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::3 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::4 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::5 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::6 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::7 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::8 0 # What write queue length does an incoming req see

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system.mem_ctrl.wrQLenPdf::31 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::32 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::33 0 # What write queue length does an incoming req see
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system.mem_ctrl.wrQLenPdf::36 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::37 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::38 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::39 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::40 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::41 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::42 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::43 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::44 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::45 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::46 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::47 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::48 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::49 0 # What write queue length does an incoming req see
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system.mem_ctrl.wrQLenPdf::52 0 # What write queue length does an incoming req see
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system.mem_ctrl.wrQLenPdf::56 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::57 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::58 0 # What write queue length does an incoming req see

system.mem_ctrl.wrQLenPdf::59 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::60 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::61 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::62 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::63 0 # What write queue length does an incoming req see
system.mem_ctrl.bytesPerActivate::samples 218 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::mean 279.192661 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::gmean 161.294794 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::stdev 322.683577 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::0-127 90 41.28% 41.28% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::128-255 60 27.52% 68.81% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::256-383 14 6.42% 75.23% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::384-511 11 5.05% 80.28% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::512-639 8 3.67% 83.94% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::640-767 4 1.83% 85.78% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::768-895 1 0.46% 86.24% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::896-1023 6 2.75% 88.99% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::1024-1151 24 11.01% 100.00% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::total 218 # Bytes accessed per row activation
system.mem_ctrl.totQLat 7822250 # Total ticks spent queuing
system.mem_ctrl.totMemAccLat 26234750 # Total ticks spent from burst creation until serviced by the DRAM
system.mem_ctrl.totBusLat 4910000 # Total ticks spent in databus transfers
system.mem_ctrl.avgQLat 7965.63 # Average queueing delay per DRAM burst
system.mem_ctrl.avgBusLat 5000.00 # Average bus latency per DRAM burst
system.mem_ctrl.avgMemAccLat 26715.63 # Average memory access latency per DRAM burst
system.mem_ctrl.avgRdBW 97.33 # Average DRAM read bandwidth in MiByte/s
system.mem_ctrl.avgWrBW 0.00 # Average achieved write bandwidth in MiByte/s
system.mem_ctrl.avgRdBWSys 97.33 # Average system read bandwidth in MiByte/s
system.mem_ctrl.avgWrBWSys 0.00 # Average system write bandwidth in MiByte/s
system.mem_ctrl.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s
system.mem_ctrl.busUtil 0.76 # Data bus utilization in percentage
system.mem_ctrl.busUtilRead 0.76 # Data bus utilization in percentage for reads
system.mem_ctrl.busUtilWrite 0.00 # Data bus utilization in percentage for writes
system.mem_ctrl.avgRdQLen 1.03 # Average read queue length when enqueuing
system.mem_ctrl.avgWrQLen 0.00 # Average write queue length when enqueuing
system.mem_ctrl.readRowHits 755 # Number of row buffer hits during reads
system.mem_ctrl.writeRowHits 0 # Number of row buffer hits during writes
system.mem_ctrl.readRowHitRate 76.88 # Row buffer hit rate for reads
system.mem_ctrl.writeRowHitRate nan # Row buffer hit rate for writes

system.mem_ctrl.avgGap 657474.54 # Average gap between requests
system.mem_ctrl.pageHitRate 76.88 # Row buffer hit rate, read and write combined
system.mem_ctrl_0.actEnergy 1134000 # Energy for activate commands per rank (pJ)
system.mem_ctrl_0.preEnergy 618750 # Energy for precharge commands per rank (pJ)
system.mem_ctrl_0.readEnergy 5280600 # Energy for read commands per rank (pJ)
system.mem_ctrl_0.writeEnergy 0 # Energy for write commands per rank (pJ)
system.mem_ctrl_0.refreshEnergy 41701920 # Energy for refresh commands per rank (pJ)
system.mem_ctrl_0.actBackEnergy 212298210 # Energy for active background per rank (pJ)
system.mem_ctrl_0.preBackEnergy 197004750 # Energy for precharge background per rank (pJ)
system.mem_ctrl_0.totalEnergy 458038230 # Total energy per rank (pJ)
system.mem_ctrl_0.averagePower 717.120376 # Core power per rank (mW)
system.mem_ctrl_0.memoryStateTime::IDLE 329171500 # Time in different power states
system.mem_ctrl_0.memoryStateTime::REF 21320000 # Time in different power states
system.mem_ctrl_0.memoryStateTime::PRE_PDN 0 # Time in different power states
system.mem_ctrl_0.memoryStateTime::ACT 291064000 # Time in different power states
system.mem_ctrl_0.memoryStateTime::ACT_PDN 0 # Time in different power states
system.mem_ctrl_1.actEnergy 415800 # Energy for activate commands per rank (pJ)
system.mem_ctrl_1.preEnergy 226875 # Energy for precharge commands per rank (pJ)
system.mem_ctrl_1.readEnergy 1762800 # Energy for read commands per rank (pJ)
system.mem_ctrl_1.writeEnergy 0 # Energy for write commands per rank (pJ)
system.mem_ctrl_1.refreshEnergy 41701920 # Energy for refresh commands per rank (pJ)
system.mem_ctrl_1.actBackEnergy 52061805 # Energy for active background per rank (pJ)
system.mem_ctrl_1.preBackEnergy 337563000 # Energy for precharge background per rank (pJ)
system.mem_ctrl_1.totalEnergy 433732200 # Total energy per rank (pJ)
system.mem_ctrl_1.averagePower 679.066021 # Core power per rank (mW)
system.mem_ctrl_1.memoryStateTime::IDLE 565536500 # Time in different power states
system.mem_ctrl_1.memoryStateTime::REF 21320000 # Time in different power states
system.mem_ctrl_1.memoryStateTime::PRE_PDN 0 # Time in different power states
system.mem_ctrl_1.memoryStateTime::ACT 56199000 # Time in different power states
system.mem_ctrl_1.memoryStateTime::ACT_PDN 0 # Time in different power states
system.cpu.branchPred.lookups 204567 # Number of BP lookups
system.cpu.branchPred.condPredicted 204567 # Number of conditional branches predicted
system.cpu.branchPred.condIncorrect 1325 # Number of conditional branches incorrect
system.cpu.branchPred.BTBLookups 170191 # Number of BTB lookups
system.cpu.branchPred.BTBHits 111730 # Number of BTB hits
system.cpu.branchPred.BTBCorrect 0 # Number of correct BTB predictions (this stat may not work properly.
system.cpu.branchPred.BTBHitPct 65.649770 # BTB Hit Percentage
system.cpu.branchPred.usedRAS 18328 # Number of times the RAS was used to get a target.
system.cpu.branchPred.RASInCorrect 104 # Number of incorrect RAS predictions.
system.cpu.apic_clk_domain.clock 8000 # Clock period in ticks
system.cpu.workload.num_syscalls 14 # Number of system calls
system.cpu.numCycles 1291423 # number of cpu cycles simulated
system.cpu.numWorkItemsStarted 0 # number of work items this cpu started
system.cpu.numWorkItemsCompleted 0 # number of work items this cpu completed
system.cpu.fetch.icacheStallCycles 386902 # Number of cycles fetch is stalled on an Icache miss
system.cpu.fetch.Insts 1016446 # Number of instructions fetch has processed

system.cpu.fetch.Branches 204567 # Number of branches that fetch encountered
system.cpu.fetch.predictedBranches 130058 # Number of branches that fetch has predicted taken
system.cpu.fetch.Cycles 872782 # Number of cycles fetch has run and was not squashing or blocked
system.cpu.fetch.SquashCycles 2769 # Number of cycles fetch has spent squashing
system.cpu.fetch.MiscStallCycles 31 # Number of cycles fetch has spent waiting on interrupts, or bad addresses, or out of MSHRs
system.cpu.fetch.PendingTrapStallCycles 509 # Number of stall cycles due to pending traps
system.cpu.fetch.PendingQuiesceStallCycles 8 # Number of stall cycles due to pending quiesce instructions
system.cpu.fetch.CacheLines 370845 # Number of cache lines fetched
system.cpu.fetch.IcacheSquashes 546 # Number of outstanding Icache misses that were squashed
system.cpu.fetch.rateDist::samples 1261616 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::mean 1.522856 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::stdev 1.380710 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::underflows 0 0.00% 0.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::0 509047 40.35% 40.35% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::1 120006 9.51% 49.86% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::2 96436 7.64% 57.50% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::3 536127 42.50% 100.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::overflows 0 0.00% 100.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::min_value 0 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::max_value 3 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::total 1261616 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.branchRate 0.158404 # Number of branch fetches per cycle
system.cpu.fetch.rate 0.787074 # Number of inst fetches per cycle
system.cpu.decode.IdleCycles 427074 # Number of cycles decode is idle
system.cpu.decode.BlockedCycles 90549 # Number of cycles decode is blocked
system.cpu.decode.RunCycles 732584 # Number of cycles decode is running
system.cpu.decode.UnblockCycles 10025 # Number of cycles decode is unblocking
system.cpu.decode.SquashCycles 1384 # Number of cycles decode is squashing
system.cpu.decode.DecodedInsts 1914314 # Number of instructions handled by decode
system.cpu.decode.SquashedInsts 4312 # Number of squashed instructions handled by decode
system.cpu.rename.SquashCycles 1384 # Number of cycles rename is squashing
system.cpu.rename.IdleCycles 437363 # Number of cycles rename is idle
system.cpu.rename.BlockCycles 33713 # Number of cycles rename is blocking
system.cpu.rename.serializeStallCycles 848 # count of cycles rename stalled for serializing inst

system.cpu.rename.RunCycles 729210 # Number of cycles rename is running
system.cpu.rename.UnblockCycles 59098 # Number of cycles rename is unblocking
system.cpu.rename.RenamedInsts 1910685 # Number of instructions processed by rename
system.cpu.rename.SquashedInsts 1628 # Number of squashed instructions processed by rename
system.cpu.rename.ROBFullEvents 11958 # Number of times rename has blocked due to ROB full
system.cpu.rename.IQFullEvents 3232 # Number of times rename has blocked due to IQ full
system.cpu.rename.SQFullEvents 41536 # Number of times rename has blocked due to SQ full
system.cpu.rename.RenamedOperands 2217514 # Number of destination operands rename has renamed
system.cpu.rename.RenameLookups 4960954 # Number of register rename lookups that rename has made
system.cpu.rename.int_rename_lookups 2832871 # Number of integer rename lookups
system.cpu.rename.fp_rename_lookups 117460 # Number of floating rename lookups
system.cpu.rename.CommittedMaps 2200759 # Number of HB maps that are committed
system.cpu.rename.UndoneMaps 16755 # Number of HB maps that are undone due to squashing
system.cpu.rename.serializingInsts 25 # count of serializing insts renamed
system.cpu.rename.tempSerializingInsts 25 # count of temporary serializing insts renamed
system.cpu.rename.skidInsts 34401 # count of insts added to the skid buffer
system.cpu.memDep0.insertedLoads 242038 # Number of loads inserted to the mem dependence unit.
system.cpu.memDep0.insertedStores 162812 # Number of stores inserted to the mem dependence unit.
system.cpu.memDep0.conflictingLoads 12026 # Number of conflicting loads.
system.cpu.memDep0.conflictingStores 6787 # Number of conflicting stores.
system.cpu.iq.iqInstsAdded 1908868 # Number of instructions added to the IQ (excludes non-spec)
system.cpu.iq.iqNonSpecInstsAdded 67 # Number of non-speculative instructions added to the IQ
system.cpu.iq.iqInstsIssued 1903675 # Number of instructions issued
system.cpu.iq.iqSquashedInstsIssued 1186 # Number of squashed instructions issued
system.cpu.iq.iqSquashedInstsExamined 12004 # Number of squashed instructions iterated over during squash; mainly for profiling
system.cpu.iq.iqSquashedOperandsExamined 18046 # Number of squashed operands that are examined and possibly removed from graph
system.cpu.iq.iqSquashedNonSpecRemoved 52 # Number of squashed non-spec instructions that were removed
system.cpu.iq.issued_per_cycle::samples 1261616 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::mean 1.508918 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::stdev 0.983707 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::underflows 0 0.00% 0.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::0 255056 20.22% 20.22% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::1 294886 23.37% 43.59% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::2 538504 42.68% 86.27% # Number of insts issued each

cycle
system.cpu.iq.issued_per_cycle::3 160899 12.75% 99.03% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::4 12271 0.97% 100.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::overflows 0 0.00% 100.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::min_value 0 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::max_value 4 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::total 1261616 # Number of insts issued each cycle
system.cpu.iq.fu_full::No_OpClass 0 0.00% 0.00% # attempts to use FU when none available
system.cpu.iq.fu_full::IntAlu 300227 79.59% 79.59% # attempts to use FU when none available
system.cpu.iq.fu_full::IntMult 0 0.00% 79.59% # attempts to use FU when none available
system.cpu.iq.fu_full::IntDiv 0 0.00% 79.59% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatAdd 32 0.01% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatCmp 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatCvt 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatMult 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatDiv 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatSqrt 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAdd 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAddAcc 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAlu 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdCmp 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdCvt 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMisc 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMult 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMultAcc 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdShift 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdShiftAcc 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdSqrt 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatAdd 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatAlu 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatCmp 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatCvt 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatDiv 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMisc 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMult 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatMultAcc 0 0.00% 79.60% # attempts to use FU when none

available
system.cpu.iq.fu_full::SimdFloatSqrt 0 0.00% 79.60% # attempts to use FU when none available
system.cpu.iq.fu_full::MemRead 43732 11.59% 91.19% # attempts to use FU when none available
system.cpu.iq.fu_full::MemWrite 33231 8.81% 100.00% # attempts to use FU when none available
system.cpu.iq.fu_full::IprAccess 0 0.00% 100.00% # attempts to use FU when none available
system.cpu.iq.fu_full::InstPrefetch 0 0.00% 100.00% # attempts to use FU when none available
system.cpu.iq.FU_type_0::No_OpClass 10707 0.56% 0.56% # Type of FU issued
system.cpu.iq.FU_type_0::IntAlu 1429589 75.10% 75.66% # Type of FU issued
system.cpu.iq.FU_type_0::IntMult 4922 0.26% 75.92% # Type of FU issued
system.cpu.iq.FU_type_0::IntDiv 28 0.00% 75.92% # Type of FU issued
system.cpu.iq.FU_type_0::FloatAdd 54195 2.85% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::FloatCmp 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::FloatCvt 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::FloatMult 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::FloatDiv 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::FloatSqrt 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAdd 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAddAcc 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAlu 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdCmp 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdCvt 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMisc 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMult 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMultAcc 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdShift 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdShiftAcc 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdSqrt 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatAdd 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatAlu 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatCmp 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatCvt 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatDiv 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMisc 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMult 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMultAcc 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatSqrt 0 0.00% 78.77% # Type of FU issued
system.cpu.iq.FU_type_0::MemRead 241669 12.69% 91.46% # Type of FU issued
system.cpu.iq.FU_type_0::MemWrite 162565 8.54% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::IprAccess 0 0.00% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::InstPrefetch 0 0.00% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::total 1903675 # Type of FU issued
system.cpu.iq.rate 1.474091 # Inst issue rate
system.cpu.iq.fu_busy_cnt 377222 # FU busy when requested
system.cpu.iq.fu_busy_rate 0.198155 # FU busy rate (busy events/executed inst)
system.cpu.iq.int_inst_queue_reads 5305796 # Number of integer instruction queue reads
system.cpu.iq.int_inst_queue_writes 1851575 # Number of integer instruction queue writes

system.cpu.iq.int_inst_queue_wakeup_accesses 1832763 # Number of integer instruction queue wakeup accesses
system.cpu.iq.fp_inst_queue_reads 141578 # Number of floating instruction queue reads
system.cpu.iq.fp_inst_queue_writes 69397 # Number of floating instruction queue writes
system.cpu.iq.fp_inst_queue_wakeup_accesses 69249 # Number of floating instruction queue wakeup accesses
system.cpu.iq.int_alu_accesses 2197874 # Number of integer alu accesses
system.cpu.iq.fp_alu_accesses 72316 # Number of floating point alu accesses
system.cpu.iew.lsq.thread0.forwLoads 29659 # Number of loads that had data forwarded from stores
system.cpu.iew.lsq.thread0.invAddrLoads 0 # Number of loads ignored due to an invalid address
system.cpu.iew.lsq.thread0.squashedLoads 1413 # Number of loads squashed
system.cpu.iew.lsq.thread0.ignoredResponses 9 # Number of memory responses ignored because the instruction is squashed
system.cpu.iew.lsq.thread0.memOrderViolation 34 # Number of memory ordering violations
system.cpu.iew.lsq.thread0.squashedStores 630 # Number of stores squashed
system.cpu.iew.lsq.thread0.invAddrSwpfs 0 # Number of software prefetches ignored due to an invalid address
system.cpu.iew.lsq.thread0.blockedLoads 0 # Number of blocked loads due to partial load-store forwarding
system.cpu.iew.lsq.thread0.rescheduledLoads 41 # Number of loads that were rescheduled
system.cpu.iew.lsq.thread0.cacheBlocked 8 # Number of times an access to memory failed due to the cache being blocked
system.cpu.iew.iewIdleCycles 0 # Number of cycles IEW is idle
system.cpu.iew.iewSquashCycles 1384 # Number of cycles IEW is squashing
system.cpu.iew.iewBlockCycles 5095 # Number of cycles IEW is blocking
system.cpu.iew.iewUnblockCycles 3883 # Number of cycles IEW is unblocking
system.cpu.iew.iewDispatchedInsts 1908935 # Number of instructions dispatched to IQ
system.cpu.iew.iewDispSquashedInsts 0 # Number of squashed instructions skipped by dispatch
system.cpu.iew.iewDispLoadInsts 242038 # Number of dispatched load instructions
system.cpu.iew.iewDispStoreInsts 162812 # Number of dispatched store instructions
system.cpu.iew.iewDispNonSpecInsts 24 # Number of dispatched non-speculative instructions
system.cpu.iew.iewIQFullEvents 1 # Number of times the IQ has become full, causing a stall
system.cpu.iew.iewLSQFullEvents 3875 # Number of times the LSQ has become full, causing a stall
system.cpu.iew.memOrderViolationEvents 34 # Number of memory order violations
system.cpu.iew.predictedTakenIncorrect 435 # Number of branches that were predicted taken incorrectly
system.cpu.iew.predictedNotTakenIncorrect 962 # Number of branches that were predicted not taken incorrectly
system.cpu.iew.branchMispredicts 1397 # Number of branch mispredicts detected at execute
system.cpu.iew.iewExecutedInsts 1902517 # Number of executed instructions
system.cpu.iew.iewExecLoadInsts 241308 # Number of load instructions executed
system.cpu.iew.iewExecSquashedInsts 1158 # Number of squashed instructions skipped in execute
system.cpu.iew.exec_swp 0 # number of swp insts executed
system.cpu.iew.exec_nop 0 # number of nop insts executed

system.cpu.iew.exec_refs 403749 # number of memory reference insts executed
system.cpu.iew.exec_branches 202165 # Number of branches executed
system.cpu.iew.exec_stores 162441 # Number of stores executed
system.cpu.iew.exec_rate 1.473194 # Inst execution rate
system.cpu.iew.wb_sent 1902191 # cumulative count of insts sent to commit
system.cpu.iew.wb_count 1902012 # cumulative count of insts written-back
system.cpu.iew.wb_producers 1287042 # num instructions producing a value
system.cpu.iew.wb_consumers 2071281 # num instructions consuming a value
system.cpu.iew.wb_penalized 0 # number of instrctions required to write to 'other' IQ
system.cpu.iew.wb_rate 1.472803 # insts written-back per cycle
system.cpu.iew.wb_fanout 0.621375 # average fanout of values written-back
system.cpu.iew.wb_penalized_rate 0 # fraction of instructions written-back that wrote to 'other' IQ
system.cpu.commit.commitSquashedInsts 10007 # The number of squashed insts skipped by commit
system.cpu.commit.commitNonSpecStalls 15 # The number of times commit has been forced to stall to communicate backwards
system.cpu.commit.branchMispredicts 1355 # The number of times a branch was mispredicted
system.cpu.commit.committed_per_cycle::samples 1258461 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::mean 1.507342 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::stdev 1.480611 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::underflows 0 0.00% 0.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::0 448062 35.60% 35.60% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::1 276985 22.01% 57.61% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::2 201246 15.99% 73.61% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::3 111218 8.84% 82.44% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::4 220950 17.56% 100.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::overflows 0 0.00% 100.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::min_value 0 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::max_value 4 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::total 1258461 # Number of insts commited each cycle
system.cpu.commit.committedInsts 1003354 # Number of instructions committed
system.cpu.commit.committedOps 1896931 # Number of ops (including micro ops) committed
system.cpu.commit.swp_count 0 # Number of s/w prefetches committed
system.cpu.commit.refs 402807 # Number of memory references committed

system.cpu.commit.loads 240625 # Number of loads committed
system.cpu.commit.membars 0 # Number of memory barriers committed
system.cpu.commit.branches 201942 # Number of branches committed
system.cpu.commit.fp_insts 69163 # Number of committed floating point instructions.
system.cpu.commit.int_insts 1835272 # Number of committed integer instructions.
system.cpu.commit.function_calls 18142 # Number of function calls committed.
system.cpu.commit.op_class_0::No_OpClass 10559 0.56% 0.56% # Class of committed instruction
system.cpu.commit.op_class_0::IntAlu 1424492 75.09% 75.65% # Class of committed instruction
system.cpu.commit.op_class_0::IntMult 4919 0.26% 75.91% # Class of committed instruction
system.cpu.commit.op_class_0::IntDiv 28 0.00% 75.91% # Class of committed instruction
system.cpu.commit.op_class_0::FloatAdd 54126 2.85% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::FloatCmp 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::FloatCvt 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::FloatMult 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::FloatDiv 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::FloatSqrt 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAdd 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAddAcc 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAlu 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdCmp 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdCvt 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMisc 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMult 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMultAcc 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdShift 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdShiftAcc 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdSqrt 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatAdd 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatAlu 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatCmp 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatCvt 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatDiv 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMisc 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMult 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMultAcc 0 0.00% 78.77% # Class of committed instruction

system.cpu.commit.op_class_0::SimdFloatSqrt 0 0.00% 78.77% # Class of committed instruction
system.cpu.commit.op_class_0::MemRead 240625 12.68% 91.45% # Class of committed instruction
system.cpu.commit.op_class_0::MemWrite 162182 8.55% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::IprAccess 0 0.00% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::InstPrefetch 0 0.00% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::total 1896931 # Class of committed instruction
system.cpu.commit.bw_lim_events 220950 # number cycles where commit BW limit reached
system.cpu.rob.rob_reads 2944449 # The number of ROB reads
system.cpu.rob.rob_writes 3817045 # The number of ROB writes
system.cpu.timesIdled 305 # Number of times that the entire CPU went into an idle state and unscheduled itself
system.cpu.idleCycles 29807 # Total number of cycles that the CPU has spent unscheduled due to idling
system.cpu.committedInsts 1003354 # Number of Instructions Simulated
system.cpu.committedOps 1896931 # Number of Ops (including micro ops) Simulated
system.cpu.cpi 1.287106 # CPI: Cycles Per Instruction
system.cpu.cpi_total 1.287106 # CPI: Total CPI of All Threads
system.cpu.ipc 0.776937 # IPC: Instructions Per Cycle
system.cpu.ipc_total 0.776937 # IPC: Total IPC of All Threads
system.cpu.int_regfile_reads 2819571 # number of integer regfile reads
system.cpu.int_regfile_writes 1474581 # number of integer regfile writes
system.cpu.fp_regfile_reads 117413 # number of floating regfile reads
system.cpu.fp_regfile_writes 57199 # number of floating regfile writes
system.cpu.cc_regfile_reads 1202117 # number of cc regfile reads
system.cpu.cc_regfile_writes 675428 # number of cc regfile writes
system.cpu.misc_regfile_reads 799197 # number of misc regfile reads
system.cpu.misc_regfile_writes 1 # number of misc regfile writes
system.cpu.dcache.tags.replacements 104 # number of replacements
system.cpu.dcache.tags.tagsinuse 309.753605 # Cycle average of tags in use
system.cpu.dcache.tags.total_refs 373105 # Total number of references to valid blocks.
system.cpu.dcache.tags.sampled_refs 576 # Sample count of references to valid blocks.
system.cpu.dcache.tags.avg_refs 647.751736 # Average number of references to valid blocks.
system.cpu.dcache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.dcache.tags.occ_blocks::cpu.data 309.753605 # Average occupied blocks per requestor
system.cpu.dcache.tags.occ_percent::cpu.data 0.604988 # Average percentage of cache occupancy
system.cpu.dcache.tags.occ_percent::total 0.604988 # Average percentage of cache occupancy
system.cpu.dcache.tags.occ_task_id_blocks::1024 472 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::0 22 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::2 450 # Occupied blocks per task id
system.cpu.dcache.tags.occ_task_id_percent::1024 0.921875 # Percentage of cache occupancy per task id
system.cpu.dcache.tags.tag_accesses 1495544 # Number of tag accesses

system.cpu.dcache.tags.data_accesses 1495544 # Number of data accesses
system.cpu.dcache.ReadReq_hits::cpu.data 211387 # number of ReadReq hits
system.cpu.dcache.ReadReq_hits::total 211387 # number of ReadReq hits
system.cpu.dcache.WriteReq_hits::cpu.data 161718 # number of WriteReq hits
system.cpu.dcache.WriteReq_hits::total 161718 # number of WriteReq hits
system.cpu.dcache.demand_hits::cpu.data 373105 # number of demand (read+write) hits
system.cpu.dcache.demand_hits::total 373105 # number of demand (read+write) hits
system.cpu.dcache.overall_hits::cpu.data 373105 # number of overall hits
system.cpu.dcache.overall_hits::total 373105 # number of overall hits
system.cpu.dcache.ReadReq_misses::cpu.data 173 # number of ReadReq misses
system.cpu.dcache.ReadReq_misses::total 173 # number of ReadReq misses
system.cpu.dcache.WriteReq_misses::cpu.data 464 # number of WriteReq misses
system.cpu.dcache.WriteReq_misses::total 464 # number of WriteReq misses
system.cpu.dcache.demand_misses::cpu.data 637 # number of demand (read+write) misses
system.cpu.dcache.demand_misses::total 637 # number of demand (read+write) misses
system.cpu.dcache.overall_misses::cpu.data 637 # number of overall misses
system.cpu.dcache.overall_misses::total 637 # number of overall misses
system.cpu.dcache.ReadReq_miss_latency::cpu.data 11724250 # number of ReadReq miss cycles
system.cpu.dcache.ReadReq_miss_latency::total 11724250 # number of ReadReq miss cycles
system.cpu.dcache.WriteReq_miss_latency::cpu.data 31855250 # number of WriteReq miss cycles
system.cpu.dcache.WriteReq_miss_latency::total 31855250 # number of WriteReq miss cycles
system.cpu.dcache.demand_miss_latency::cpu.data 43579500 # number of demand (read+write) miss cycles
system.cpu.dcache.demand_miss_latency::total 43579500 # number of demand (read+write) miss cycles
system.cpu.dcache.overall_miss_latency::cpu.data 43579500 # number of overall miss cycles
system.cpu.dcache.overall_miss_latency::total 43579500 # number of overall miss cycles
system.cpu.dcache.ReadReq_accesses::cpu.data 211560 # number of ReadReq accesses(hits+misses)
system.cpu.dcache.ReadReq_accesses::total 211560 # number of ReadReq accesses(hits+misses)
system.cpu.dcache.WriteReq_accesses::cpu.data 162182 # number of WriteReq accesses(hits+misses)
system.cpu.dcache.WriteReq_accesses::total 162182 # number of WriteReq accesses(hits+misses)
system.cpu.dcache.demand_accesses::cpu.data 373742 # number of demand (read+write) accesses
system.cpu.dcache.demand_accesses::total 373742 # number of demand (read+write) accesses
system.cpu.dcache.overall_accesses::cpu.data 373742 # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total 373742 # number of overall (read+write) accesses
system.cpu.dcache.ReadReq_miss_rate::cpu.data 0.000818 # miss rate for ReadReq accesses
system.cpu.dcache.ReadReq_miss_rate::total 0.000818 # miss rate for ReadReq accesses
system.cpu.dcache.WriteReq_miss_rate::cpu.data 0.002861 # miss rate for WriteReq accesses

system.cpu.dcache.WriteReq_miss_rate::total 0.002861 # miss rate for WriteReq accesses
system.cpu.dcache.demand_miss_rate::cpu.data 0.001704 # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total 0.001704 # miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data 0.001704 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.001704 # miss rate for overall accesses
system.cpu.dcache.ReadReq_avg_miss_latency::cpu.data 67770.231214 # average ReadReq miss latency
system.cpu.dcache.ReadReq_avg_miss_latency::total 67770.231214 # average ReadReq miss latency
system.cpu.dcache.WriteReq_avg_miss_latency::cpu.data 68653.556034 # average WriteReq miss latency
system.cpu.dcache.WriteReq_avg_miss_latency::total 68653.556034 # average WriteReq miss latency
system.cpu.dcache.demand_avg_miss_latency::cpu.data 68413.657771 # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total 68413.657771 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data 68413.657771 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total 68413.657771 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 329 # number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs 6 # number of cycles access was blocked
system.cpu.dcache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs 54.833333 # average number of cycles each access was blocked
system.cpu.dcache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.dcache.fast_writes 0 # number of fast writes performed
system.cpu.dcache.cache_copies 0 # number of cache copies performed
system.cpu.dcache.writebacks::writebacks 88 # number of writebacks
system.cpu.dcache.writebacks::total 88 # number of writebacks
system.cpu.dcache.ReadReq_mshr_hits::cpu.data 61 # number of ReadReq MSHR hits
system.cpu.dcache.ReadReq_mshr_hits::total 61 # number of ReadReq MSHR hits
system.cpu.dcache.demand_mshr_hits::cpu.data 61 # number of demand (read+write) MSHR hits
system.cpu.dcache.demand_mshr_hits::total 61 # number of demand (read+write) MSHR hits
system.cpu.dcache.overall_mshr_hits::cpu.data 61 # number of overall MSHR hits
system.cpu.dcache.overall_mshr_hits::total 61 # number of overall MSHR hits
system.cpu.dcache.ReadReq_mshr_misses::cpu.data 112 # number of ReadReq MSHR misses
system.cpu.dcache.ReadReq_mshr_misses::total 112 # number of ReadReq MSHR misses
system.cpu.dcache.WriteReq_mshr_misses::cpu.data 464 # number of WriteReq MSHR misses
system.cpu.dcache.WriteReq_mshr_misses::total 464 # number of WriteReq MSHR misses
system.cpu.dcache.demand_mshr_misses::cpu.data 576 # number of demand (read+write) MSHR misses
system.cpu.dcache.demand_mshr_misses::total 576 # number of demand (read+write) MSHR misses

system.cpu.dcache.overall_mshr_misses::cpu.data 576 # number of overall MSHR misses
system.cpu.dcache.overall_mshr_misses::total 576 # number of overall MSHR misses
system.cpu.dcache.ReadReq_mshr_miss_latency::cpu.data 7498500 # number of ReadReq MSHR miss cycles
system.cpu.dcache.ReadReq_mshr_miss_latency::total 7498500 # number of ReadReq MSHR miss cycles
system.cpu.dcache.WriteReq_mshr_miss_latency::cpu.data 30971750 # number of WriteReq MSHR miss cycles
system.cpu.dcache.WriteReq_mshr_miss_latency::total 30971750 # number of WriteReq MSHR miss cycles
system.cpu.dcache.demand_mshr_miss_latency::cpu.data 38470250 # number of demand (read+write) MSHR miss cycles
system.cpu.dcache.demand_mshr_miss_latency::total 38470250 # number of demand (read+write) MSHR miss cycles
system.cpu.dcache.overall_mshr_miss_latency::cpu.data 38470250 # number of overall MSHR miss cycles
system.cpu.dcache.overall_mshr_miss_latency::total 38470250 # number of overall MSHR miss cycles
system.cpu.dcache.ReadReq_mshr_miss_rate::cpu.data 0.000529 # mshr miss rate for ReadReq accesses
system.cpu.dcache.ReadReq_mshr_miss_rate::total 0.000529 # mshr miss rate for ReadReq accesses
system.cpu.dcache.WriteReq_mshr_miss_rate::cpu.data 0.002861 # mshr miss rate for WriteReq accesses
system.cpu.dcache.WriteReq_mshr_miss_rate::total 0.002861 # mshr miss rate for WriteReq accesses
system.cpu.dcache.demand_mshr_miss_rate::cpu.data 0.001541 # mshr miss rate for demand accesses
system.cpu.dcache.demand_mshr_miss_rate::total 0.001541 # mshr miss rate for demand accesses
system.cpu.dcache.overall_mshr_miss_rate::cpu.data 0.001541 # mshr miss rate for overall accesses
system.cpu.dcache.overall_mshr_miss_rate::total 0.001541 # mshr miss rate for overall accesses
system.cpu.dcache.ReadReq_avg_mshr_miss_latency::cpu.data 66950.892857 # average ReadReq mshr miss latency
system.cpu.dcache.ReadReq_avg_mshr_miss_latency::total 66950.892857 # average ReadReq mshr miss latency
system.cpu.dcache.WriteReq_avg_mshr_miss_latency::cpu.data 66749.461207 # average WriteReq mshr miss latency
system.cpu.dcache.WriteReq_avg_mshr_miss_latency::total 66749.461207 # average WriteReq mshr miss latency
system.cpu.dcache.demand_avg_mshr_miss_latency::cpu.data 66788.628472 # average overall mshr miss latency
system.cpu.dcache.demand_avg_mshr_miss_latency::total 66788.628472 # average overall mshr miss latency
system.cpu.dcache.overall_avg_mshr_miss_latency::cpu.data 66788.628472 # average overall mshr miss latency
system.cpu.dcache.overall_avg_mshr_miss_latency::total 66788.628472 # average overall mshr miss latency

system.cpu.dcache.no_allocate_misses 0 # Number of misses that were no-allocate
system.cpu.icache.tags.replacements 29 # number of replacements
system.cpu.icache.tags.tagsinuse 335.198926 # Cycle average of tags in use
system.cpu.icache.tags.total_refs 370321 # Total number of references to valid blocks.
system.cpu.icache.tags.sampled_refs 433 # Sample count of references to valid blocks.
system.cpu.icache.tags.avg_refs 855.244804 # Average number of references to valid blocks.
system.cpu.icache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.icache.tags.occ_blocks::cpu.inst 335.198926 # Average occupied blocks per requestor
system.cpu.icache.tags.occ_percent::cpu.inst 0.654685 # Average percentage of cache occupancy
system.cpu.icache.tags.occ_percent::total 0.654685 # Average percentage of cache occupancy
system.cpu.icache.tags.occ_task_id_blocks::1024 404 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::0 66 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::2 338 # Occupied blocks per task id
system.cpu.icache.tags.occ_task_id_percent::1024 0.789062 # Percentage of cache occupancy per task id
system.cpu.icache.tags.tag_accesses 1483813 # Number of tag accesses
system.cpu.icache.tags.data_accesses 1483813 # Number of data accesses
system.cpu.icache.ReadReq_hits::cpu.inst 370321 # number of ReadReq hits
system.cpu.icache.ReadReq_hits::total 370321 # number of ReadReq hits
system.cpu.icache.demand_hits::cpu.inst 370321 # number of demand (read+write) hits
system.cpu.icache.demand_hits::total 370321 # number of demand (read+write) hits
system.cpu.icache.overall_hits::cpu.inst 370321 # number of overall hits
system.cpu.icache.overall_hits::total 370321 # number of overall hits
system.cpu.icache.ReadReq_misses::cpu.inst 524 # number of ReadReq misses
system.cpu.icache.ReadReq_misses::total 524 # number of ReadReq misses
system.cpu.icache.demand_misses::cpu.inst 524 # number of demand (read+write) misses
system.cpu.icache.demand_misses::total 524 # number of demand (read+write) misses
system.cpu.icache.overall_misses::cpu.inst 524 # number of overall misses
system.cpu.icache.overall_misses::total 524 # number of overall misses
system.cpu.icache.ReadReq_miss_latency::cpu.inst 35512250 # number of ReadReq miss cycles
system.cpu.icache.ReadReq_miss_latency::total 35512250 # number of ReadReq miss cycles
system.cpu.icache.demand_miss_latency::cpu.inst 35512250 # number of demand (read+write) miss cycles
system.cpu.icache.demand_miss_latency::total 35512250 # number of demand (read+write) miss cycles
system.cpu.icache.overall_miss_latency::cpu.inst 35512250 # number of overall miss cycles
system.cpu.icache.overall_miss_latency::total 35512250 # number of overall miss cycles
system.cpu.icache.ReadReq_accesses::cpu.inst 370845 # number of ReadReq accesses(hits+misses)
system.cpu.icache.ReadReq_accesses::total 370845 # number of ReadReq accesses(hits+misses)
system.cpu.icache.demand_accesses::cpu.inst 370845 # number of demand (read+write) accesses
system.cpu.icache.demand_accesses::total 370845 # number of demand (read+write) accesses
system.cpu.icache.overall_accesses::cpu.inst 370845 # number of overall (read+write)

accesses
system.cpu.icache.overall_accesses::total 370845 # number of overall (read+write) accesses
system.cpu.icache.ReadReq_miss_rate::cpu.inst 0.001413 # miss rate for ReadReq accesses
system.cpu.icache.ReadReq_miss_rate::total 0.001413 # miss rate for ReadReq accesses
system.cpu.icache.demand_miss_rate::cpu.inst 0.001413 # miss rate for demand accesses
system.cpu.icache.demand_miss_rate::total 0.001413 # miss rate for demand accesses
system.cpu.icache.overall_miss_rate::cpu.inst 0.001413 # miss rate for overall accesses
system.cpu.icache.overall_miss_rate::total 0.001413 # miss rate for overall accesses
system.cpu.icache.ReadReq_avg_miss_latency::cpu.inst 67771.469466 # average ReadReq miss latency
system.cpu.icache.ReadReq_avg_miss_latency::total 67771.469466 # average ReadReq miss latency
system.cpu.icache.demand_avg_miss_latency::cpu.inst 67771.469466 # average overall miss latency
system.cpu.icache.demand_avg_miss_latency::total 67771.469466 # average overall miss latency
system.cpu.icache.overall_avg_miss_latency::cpu.inst 67771.469466 # average overall miss latency
system.cpu.icache.overall_avg_miss_latency::total 67771.469466 # average overall miss latency
system.cpu.icache.blocked_cycles::no_mshrs 55 # number of cycles access was blocked
system.cpu.icache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.icache.blocked::no_mshrs 1 # number of cycles access was blocked
system.cpu.icache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.icache.avg_blocked_cycles::no_mshrs 55 # average number of cycles each access was blocked
system.cpu.icache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.icache.fast_writes 0 # number of fast writes performed
system.cpu.icache.cache_copies 0 # number of cache copies performed
system.cpu.icache.ReadReq_mshr_hits::cpu.inst 91 # number of ReadReq MSHR hits
system.cpu.icache.ReadReq_mshr_hits::total 91 # number of ReadReq MSHR hits
system.cpu.icache.demand_mshr_hits::cpu.inst 91 # number of demand (read+write) MSHR hits
system.cpu.icache.demand_mshr_hits::total 91 # number of demand (read+write) MSHR hits
system.cpu.icache.overall_mshr_hits::cpu.inst 91 # number of overall MSHR hits
system.cpu.icache.overall_mshr_hits::total 91 # number of overall MSHR hits
system.cpu.icache.ReadReq_mshr_misses::cpu.inst 433 # number of ReadReq MSHR misses
system.cpu.icache.ReadReq_mshr_misses::total 433 # number of ReadReq MSHR misses
system.cpu.icache.demand_mshr_misses::cpu.inst 433 # number of demand (read+write) MSHR misses
system.cpu.icache.demand_mshr_misses::total 433 # number of demand (read+write) MSHR misses
system.cpu.icache.overall_mshr_misses::cpu.inst 433 # number of overall MSHR misses
system.cpu.icache.overall_mshr_misses::total 433 # number of overall MSHR misses
system.cpu.icache.ReadReq_mshr_miss_latency::cpu.inst 29348500 # number of ReadReq MSHR miss cycles
system.cpu.icache.ReadReq_mshr_miss_latency::total 29348500 # number of ReadReq MSHR miss cycles
system.cpu.icache.demand_mshr_miss_latency::cpu.inst 29348500 # number of demand

(read+write) MSHR miss cycles
system.cpu.icache.demand_mshr_miss_latency::total 29348500 # number of demand (read+write) MSHR miss cycles
system.cpu.icache.overall_mshr_miss_latency::cpu.inst 29348500 # number of overall MSHR miss cycles
system.cpu.icache.overall_mshr_miss_latency::total 29348500 # number of overall MSHR miss cycles
system.cpu.icache.ReadReq_mshr_miss_rate::cpu.inst 0.001168 # mshr miss rate for ReadReq accesses
system.cpu.icache.ReadReq_mshr_miss_rate::total 0.001168 # mshr miss rate for ReadReq accesses
system.cpu.icache.demand_mshr_miss_rate::cpu.inst 0.001168 # mshr miss rate for demand accesses
system.cpu.icache.demand_mshr_miss_rate::total 0.001168 # mshr miss rate for demand accesses
system.cpu.icache.overall_mshr_miss_rate::cpu.inst 0.001168 # mshr miss rate for overall accesses
system.cpu.icache.overall_mshr_miss_rate::total 0.001168 # mshr miss rate for overall accesses
system.cpu.icache.ReadReq_avg_mshr_miss_latency::cpu.inst 67779.445727 # average ReadReq mshr miss latency
system.cpu.icache.ReadReq_avg_mshr_miss_latency::total 67779.445727 # average ReadReq mshr miss latency
system.cpu.icache.demand_avg_mshr_miss_latency::cpu.inst 67779.445727 # average overall mshr miss latency
system.cpu.icache.demand_avg_mshr_miss_latency::total 67779.445727 # average overall mshr miss latency
system.cpu.icache.overall_avg_mshr_miss_latency::cpu.inst 67779.445727 # average overall mshr miss latency
system.cpu.icache.overall_avg_mshr_miss_latency::total 67779.445727 # average overall mshr miss latency
system.cpu.icache.no_allocate_misses 0 # Number of misses that were no-allocate
system.cpu.l2cache.tags.replacements 0 # number of replacements
system.cpu.l2cache.tags.tagsinuse 438.006399 # Cycle average of tags in use
system.cpu.l2cache.tags.total_refs 37 # Total number of references to valid blocks.
system.cpu.l2cache.tags.sampled_refs 592 # Sample count of references to valid blocks.
system.cpu.l2cache.tags.avg_refs 0.062500 # Average number of references to valid blocks.
system.cpu.l2cache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.l2cache.tags.occ_blocks::writebacks 15.493331 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_blocks::cpu.inst 344.129684 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_blocks::cpu.data 78.383383 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_percent::writebacks 0.000236 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::cpu.inst 0.005251 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::cpu.data 0.001196 # Average percentage of cache occupancy

system.cpu.l2cache.tags.occ_percent::total 0.006683 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_task_id_blocks::1024 592 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::0 95 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::2 497 # Occupied blocks per task id
system.cpu.l2cache.tags.occ_task_id_percent::1024 0.009033 # Percentage of cache occupancy per task id
system.cpu.l2cache.tags.tag_accesses 9832 # Number of tag accesses
system.cpu.l2cache.tags.data_accesses 9832 # Number of data accesses
system.cpu.l2cache.ReadReq_hits::cpu.inst 4 # number of ReadReq hits
system.cpu.l2cache.ReadReq_hits::cpu.data 16 # number of ReadReq hits
system.cpu.l2cache.ReadReq_hits::total 20 # number of ReadReq hits
system.cpu.l2cache.Writeback_hits::writebacks 88 # number of Writeback hits
system.cpu.l2cache.Writeback_hits::total 88 # number of Writeback hits
system.cpu.l2cache.ReadExReq_hits::cpu.data 7 # number of ReadExReq hits
system.cpu.l2cache.ReadExReq_hits::total 7 # number of ReadExReq hits
system.cpu.l2cache.demand_hits::cpu.inst 4 # number of demand (read+write) hits
system.cpu.l2cache.demand_hits::cpu.data 23 # number of demand (read+write) hits
system.cpu.l2cache.demand_hits::total 27 # number of demand (read+write) hits
system.cpu.l2cache.overall_hits::cpu.inst 4 # number of overall hits
system.cpu.l2cache.overall_hits::cpu.data 23 # number of overall hits
system.cpu.l2cache.overall_hits::total 27 # number of overall hits
system.cpu.l2cache.ReadReq_misses::cpu.inst 429 # number of ReadReq misses
system.cpu.l2cache.ReadReq_misses::cpu.data 96 # number of ReadReq misses
system.cpu.l2cache.ReadReq_misses::total 525 # number of ReadReq misses
system.cpu.l2cache.ReadExReq_misses::cpu.data 457 # number of ReadExReq misses
system.cpu.l2cache.ReadExReq_misses::total 457 # number of ReadExReq misses
system.cpu.l2cache.demand_misses::cpu.inst 429 # number of demand (read+write) misses
system.cpu.l2cache.demand_misses::cpu.data 553 # number of demand (read+write) misses
system.cpu.l2cache.demand_misses::total 982 # number of demand (read+write) misses
system.cpu.l2cache.overall_misses::cpu.inst 429 # number of overall misses
system.cpu.l2cache.overall_misses::cpu.data 553 # number of overall misses
system.cpu.l2cache.overall_misses::total 982 # number of overall misses
system.cpu.l2cache.ReadReq_miss_latency::cpu.inst 28869500 # number of ReadReq miss cycles
system.cpu.l2cache.ReadReq_miss_latency::cpu.data 7088500 # number of ReadReq miss cycles
system.cpu.l2cache.ReadReq_miss_latency::total 35958000 # number of ReadReq miss cycles
system.cpu.l2cache.ReadExReq_miss_latency::cpu.data 29963250 # number of ReadExReq miss cycles
system.cpu.l2cache.ReadExReq_miss_latency::total 29963250 # number of ReadExReq miss cycles
system.cpu.l2cache.demand_miss_latency::cpu.inst 28869500 # number of demand (read+write) miss cycles
system.cpu.l2cache.demand_miss_latency::cpu.data 37051750 # number of demand (read+write) miss cycles
system.cpu.l2cache.demand_miss_latency::total 65921250 # number of demand (read+write) miss cycles
system.cpu.l2cache.overall_miss_latency::cpu.inst 28869500 # number of overall miss cycles

system.cpu.l2cache.overall_miss_latency::cpu.data 37051750 # number of overall miss cycles
system.cpu.l2cache.overall_miss_latency::total 65921250 # number of overall miss cycles
system.cpu.l2cache.ReadReq_accesses::cpu.inst 433 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.ReadReq_accesses::cpu.data 112 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.ReadReq_accesses::total 545 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.Writeback_accesses::writebacks 88 # number of Writeback accesses(hits+misses)
system.cpu.l2cache.Writeback_accesses::total 88 # number of Writeback accesses(hits+misses)
system.cpu.l2cache.ReadExReq_accesses::cpu.data 464 # number of ReadExReq accesses(hits+misses)
system.cpu.l2cache.ReadExReq_accesses::total 464 # number of ReadExReq accesses(hits+misses)
system.cpu.l2cache.demand_accesses::cpu.inst 433 # number of demand (read+write) accesses
system.cpu.l2cache.demand_accesses::cpu.data 576 # number of demand (read+write) accesses
system.cpu.l2cache.demand_accesses::total 1009 # number of demand (read+write) accesses
system.cpu.l2cache.overall_accesses::cpu.inst 433 # number of overall (read+write) accesses
system.cpu.l2cache.overall_accesses::cpu.data 576 # number of overall (read+write) accesses
system.cpu.l2cache.overall_accesses::total 1009 # number of overall (read+write) accesses
system.cpu.l2cache.ReadReq_miss_rate::cpu.inst 0.990762 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_miss_rate::cpu.data 0.857143 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_miss_rate::total 0.963303 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadExReq_miss_rate::cpu.data 0.984914 # miss rate for ReadExReq accesses
system.cpu.l2cache.ReadExReq_miss_rate::total 0.984914 # miss rate for ReadExReq accesses
system.cpu.l2cache.demand_miss_rate::cpu.inst 0.990762 # miss rate for demand accesses
system.cpu.l2cache.demand_miss_rate::cpu.data 0.960069 # miss rate for demand accesses
system.cpu.l2cache.demand_miss_rate::total 0.973241 # miss rate for demand accesses
system.cpu.l2cache.overall_miss_rate::cpu.inst 0.990762 # miss rate for overall accesses
system.cpu.l2cache.overall_miss_rate::cpu.data 0.960069 # miss rate for overall accesses
system.cpu.l2cache.overall_miss_rate::total 0.973241 # miss rate for overall accesses
system.cpu.l2cache.ReadReq_avg_miss_latency::cpu.inst 67294.871795 # average ReadReq miss latency
system.cpu.l2cache.ReadReq_avg_miss_latency::cpu.data 73838.541667 # average ReadReq miss latency
system.cpu.l2cache.ReadReq_avg_miss_latency::total 68491.428571 # average ReadReq miss latency
system.cpu.l2cache.ReadExReq_avg_miss_latency::cpu.data 65565.098468 # average ReadExReq miss latency
system.cpu.l2cache.ReadExReq_avg_miss_latency::total 65565.098468 # average ReadExReq miss latency
system.cpu.l2cache.demand_avg_miss_latency::cpu.inst 67294.871795 # average overall miss latency

system.cpu.l2cache.demand_avg_miss_latency::cpu.data 67001.356239 # average overall miss latency
system.cpu.l2cache.demand_avg_miss_latency::total 67129.582485 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::cpu.inst 67294.871795 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::cpu.data 67001.356239 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::total 67129.582485 # average overall miss latency
system.cpu.l2cache.blocked_cycles::no_mshrs 0 # number of cycles access was blocked
system.cpu.l2cache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.l2cache.blocked::no_mshrs 0 # number of cycles access was blocked
system.cpu.l2cache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.l2cache.avg_blocked_cycles::no_mshrs nan # average number of cycles each access was blocked
system.cpu.l2cache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.l2cache.fast_writes 0 # number of fast writes performed
system.cpu.l2cache.cache_copies 0 # number of cache copies performed
system.cpu.l2cache.ReadReq_mshr_misses::cpu.inst 429 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadReq_mshr_misses::cpu.data 96 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadReq_mshr_misses::total 525 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadExReq_mshr_misses::cpu.data 457 # number of ReadExReq MSHR misses
system.cpu.l2cache.ReadExReq_mshr_misses::total 457 # number of ReadExReq MSHR misses
system.cpu.l2cache.demand_mshr_misses::cpu.inst 429 # number of demand (read+write) MSHR misses
system.cpu.l2cache.demand_mshr_misses::cpu.data 553 # number of demand (read+write) MSHR misses
system.cpu.l2cache.demand_mshr_misses::total 982 # number of demand (read+write) MSHR misses
system.cpu.l2cache.overall_mshr_misses::cpu.inst 429 # number of overall MSHR misses
system.cpu.l2cache.overall_mshr_misses::cpu.data 553 # number of overall MSHR misses
system.cpu.l2cache.overall_mshr_misses::total 982 # number of overall MSHR misses
system.cpu.l2cache.ReadReq_mshr_miss_latency::cpu.inst 26538500 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_latency::cpu.data 6575500 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_latency::total 33114000 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadExReq_mshr_miss_latency::cpu.data 27490750 # number of ReadExReq MSHR miss cycles
system.cpu.l2cache.ReadExReq_mshr_miss_latency::total 27490750 # number of ReadExReq MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::cpu.inst 26538500 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::cpu.data 34066250 # number of demand

(read+write) MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::total 60604750 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::cpu.inst 26538500 # number of overall MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::cpu.data 34066250 # number of overall MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::total 60604750 # number of overall MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_rate::cpu.inst 0.990762 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_mshr_miss_rate::cpu.data 0.857143 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_mshr_miss_rate::total 0.963303 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadExReq_mshr_miss_rate::cpu.data 0.984914 # mshr miss rate for ReadExReq accesses
system.cpu.l2cache.ReadExReq_mshr_miss_rate::total 0.984914 # mshr miss rate for ReadExReq accesses
system.cpu.l2cache.demand_mshr_miss_rate::cpu.inst 0.990762 # mshr miss rate for demand accesses
system.cpu.l2cache.demand_mshr_miss_rate::cpu.data 0.960069 # mshr miss rate for demand accesses
system.cpu.l2cache.demand_mshr_miss_rate::total 0.973241 # mshr miss rate for demand accesses
system.cpu.l2cache.overall_mshr_miss_rate::cpu.inst 0.990762 # mshr miss rate for overall accesses
system.cpu.l2cache.overall_mshr_miss_rate::cpu.data 0.960069 # mshr miss rate for overall accesses
system.cpu.l2cache.overall_mshr_miss_rate::total 0.973241 # mshr miss rate for overall accesses
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::cpu.inst 61861.305361 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::cpu.data 68494.791667 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::total 63074.285714 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadExReq_avg_mshr_miss_latency::cpu.data 60154.814004 # average ReadExReq mshr miss latency
system.cpu.l2cache.ReadExReq_avg_mshr_miss_latency::total 60154.814004 # average ReadExReq mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::cpu.inst 61861.305361 # average overall mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::cpu.data 61602.622061 # average overall mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::total 61715.631365 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::cpu.inst 61861.305361 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::cpu.data 61602.622061 # average

overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::total 61715.631365 # average overall mshr miss latency
system.cpu.l2cache.no_allocate_misses 0 # Number of misses that were no-allocate
system.l2bus.trans_dist::ReadReq 545 # Transaction distribution
system.l2bus.trans_dist::ReadResp 545 # Transaction distribution
system.l2bus.trans_dist::Writeback 88 # Transaction distribution
system.l2bus.trans_dist::ReadExReq 464 # Transaction distribution
system.l2bus.trans_dist::ReadExResp 464 # Transaction distribution
system.l2bus.pkt_count_system.cpu.icache.mem_side::system.cpu.l2cache.cpu_side 866 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_count_system.cpu.dcache.mem_side::system.cpu.l2cache.cpu_side 1240 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_count::total 2106 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_size_system.cpu.icache.mem_side::system.cpu.l2cache.cpu_side 27712 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.pkt_size_system.cpu.dcache.mem_side::system.cpu.l2cache.cpu_side 42496 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.pkt_size::total 70208 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.snoops 0 # Total snoops (count)
system.l2bus.snoop_fanout::samples 1097 # Request fanout histogram
system.l2bus.snoop_fanout::mean 1 # Request fanout histogram
system.l2bus.snoop_fanout::stdev 0 # Request fanout histogram
system.l2bus.snoop_fanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.l2bus.snoop_fanout::0 0 0.00% 0.00% # Request fanout histogram
system.l2bus.snoop_fanout::1 1097 100.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::2 0 0.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::min_value 1 # Request fanout histogram
system.l2bus.snoop_fanout::max_value 1 # Request fanout histogram
system.l2bus.snoop_fanout::total 1097 # Request fanout histogram
system.l2bus.reqLayer0.occupancy 724500 # Layer occupancy (ticks)
system.l2bus.reqLayer0.utilization 0.1 # Layer utilization (%)
system.l2bus.respLayer0.occupancy 1175500 # Layer occupancy (ticks)
system.l2bus.respLayer0.utilization 0.2 # Layer utilization (%)
system.l2bus.respLayer1.occupancy 1550250 # Layer occupancy (ticks)
system.l2bus.respLayer1.utilization 0.2 # Layer utilization (%)
system.membus.trans_dist::ReadReq 525 # Transaction distribution
system.membus.trans_dist::ReadResp 525 # Transaction distribution
system.membus.trans_dist::ReadExReq 457 # Transaction distribution
system.membus.trans_dist::ReadExResp 457 # Transaction distribution
system.membus.pkt_count_system.cpu.l2cache.mem_side::system.mem_ctrl.port 1964 # Packet count per connected master and slave (bytes)
system.membus.pkt_count_system.cpu.l2cache.mem_side::total 1964 # Packet count per connected master and slave (bytes)
system.membus.pkt_count::total 1964 # Packet count per connected master and slave (bytes)
system.membus.pkt_size_system.cpu.l2cache.mem_side::system.mem_ctrl.port 62848 # Cumulative packet size per connected master and slave (bytes)
system.membus.pkt_size_system.cpu.l2cache.mem_side::total 62848 # Cumulative packet

size per connected master and slave (bytes)
system.membus.pkt_size::total 62848 # Cumulative packet size per connected master and slave (bytes)
system.membus.snoops 0 # Total snoops (count)
system.membus.snoop_fanout::samples 982 # Request fanout histogram
system.membus.snoop_fanout::mean 0 # Request fanout histogram
system.membus.snoop_fanout::stdev 0 # Request fanout histogram
system.membus.snoop_fanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.membus.snoop_fanout::0 982 100.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::1 0 0.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::min_value 0 # Request fanout histogram
system.membus.snoop_fanout::max_value 0 # Request fanout histogram
system.membus.snoop_fanout::total 982 # Request fanout histogram
system.membus.reqLayer2.occupancy 491000 # Layer occupancy (ticks)
system.membus.reqLayer2.utilization 0.1 # Layer utilization (%)
system.membus.respLayer0.occupancy 2658250 # Layer occupancy (ticks)
system.membus.respLayer0.utilization 0.4 # Layer utilization (%)