Verificando arquivos...
Código-fonte do programa: selectionSort.c
Arquivo de configuração de CPU: MyO3CPU.py --> MyO3CPU.py
Arquivo de configuração de caches e memória: MyCaches.py --> MyCaches.py
Arquivo de configuração de sistema: MySystem.py --> MySystem.py

****
* Compilando o programa ...
* g++ -static selectionSort.c -o selectionSort
****

****
* Executando o gem5...
* gem5 --outdir=m5out MySimulation.py -c selectionSort
****

gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 compiled Feb 16 2016 16:35:34
gem5 started Dec 14 2017 15:11:11
gem5 executing on simulacaolse3
command line: gem5 --outdir=m5out MySimulation.py -c selectionSort

Programa a ser executado: selectionSort
Global frequency set at 1000000000000 ticks per second
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb.listener: listening for remote gdb on port 7002

---------- Begin Simulation ----------
info: Entering event queue @ 0. Starting simulation...

Vetor
info: Increasing stack size by one page.
23, 9, 16, 29, 23, 1, 22, 13, 33, 5, 6, 40, 0, 46, 2, 2, 3, 48, 45, 8, 8, 34, 0, 13, 24, 18, 18, 17, 39, 27, 28, 13, 38, 44, 44, 13, 47, 18, 26, 32, 23, 32, 22, 24, 31, 27, 28, 36, 25, 24, 45, 33, 10, 45, 49, 34, 16, 17, 2, 7, 46, 32, 22, 34, 28, 16, 49, 25, 34, 26, 7, 10, 8, 32, 34, 41, 9, 12, 28, 36, 38, 23, 19, 49, 20, 18, 33, 36, 37, 37, 46, 35, 19, 18, 21, 47, 35, 21, 24, 21, 47, 32, 31, 7, 16, 17, 49, 27, 30, 27, 13, 20, 2, 34, 19, 22, 3, 5, 11, 42, 42, 7, 28, 12, 25, 1, 11, 12, 22, 38, 34, 19, 22, 17, 29, 38, 35, 28, 15, 17, 7, 30, 37, 9, 14, 7, 31, 17, 12, 44, 12, 6, 1, 42, 18, 29, 43, 32, 43, 16, 20, 29, 37, 44, 47, 16, 32, 34, 46, 49, 1, 3, 29, 38, 12, 43, 47, 46, 13, 11, 42, 27, 18, 46, 21, 38, 27, 14, 22, 20, 32, 44, 2, 22, 38, 1, 38, 22, 35, 37, 21, 36, 40, 2, 26, 5, 48, 24, 3, 11, 37, 45, 40, 5, 43, 11, 44, 20, 25, 18, 43, 10, 13, 45, 32, 1, 46, 22, 24, 31, 9, 47, 19, 2, 0, 45, 9, 48, 21, 12, 11, 11, 9, 1, 16, 5, 12, 12, 25, 39, 31, 18, 49, 44, 15, 33, 47, 13, 6, 21, 46, 17, 19, 15, 21, 21, 13, 30, 19, 36, 44, 30, 47, 6, 31, 14, 11, 45, 28, 38, 34, 11, 9, 34, 7, 24, 17, 5, 38, 25, 26, 34, 45, 47, 2, 16, 18, 15, 47, 39, 1, 43, 21, 49, 49, 4, 15, 10, 49, 45, 1, 34, 7, 10, 20, 14, 34, 39, 19, 24, 15, 48, 11, 12, 47, 13, 28, 18, 30, 25, 7, 33, 21, 31, 34, 20, 35, 49, 33, 37, 47, 34, 21, 4, 44, 43, 18, 30, 32, 40, 5, 49, 40, 16, 11, 37, 31, 42, 7, 11, 19, 17, 44, 40,

48, 29, 11, 33, 30, 44, 20, 27, 30, 43, 33, 24, 36, 4, 4, 21, 44, 11, 22, 36, 29, 36, 25, 10, 28, 33, 23, 47, 0, 20, 38, 0, 1, 1, 33, 33, 47, 6, 11, 27, 1, 44, 1, 40, 0, 7, 13, 46, 19, 35, 32, 48, 21, 8, 11, 1, 43, 36, 49, 43, 6, 39, 45, 7, 40, 28, 41, 39, 36, 4, 16, 40, 0, 19, 30, 1, 26, 43, 47, 45, 28, 32, 46, 2, 40, 9, 3, 35, 45, 4, 30, 4, 43, 25, 11, 35, 5, 4, 24, 42, 10, 42, 32, 13, 11, 14, 14, 38, 7, 13, 35, 37, 45, 33, 39, 37, 42, 45, 24, 40, 49, 4, 44, 45, 29, 7, 30, 35, 14, 7, 29, 24, 49, 13, 37, 11, 27, 3, 1, 36, 19, 36, 23, 16, 22, 13, 6, 14, 8, 30, 6, 9, 37, 0, 4, 18, 8, 37, 3, 22, 44, 34, 48, 45, 49, 38, 8, 26, 43, 9, 12, 12, 48, 36, 31, 20, 1, 39, 36, 11, 21, 43, 20, 8, 43, 27, 27, 3, 14, 32, 25, 10, 19, 24, 5, 18, 14, 14, 47, 7, 25, 9, 22, 25, 47, 5, 47, 0, 44, 34, 13, 15, 29, 36, 26, 24, 13, 5, 28, 29, 39, 5, 39, 8, 31, 44, 29, 45, 10, 26, 5, 36, 37, 27, 11, 35, 32, 11, 37, 28, 45, 1, 43, 26, 39, 21, 2, 2, 26, 30, 31, 16, 38, 20, 26, 21, 16, 5, 19, 27, 31, 24, 15, 19, 1, 28, 6, 35, 39, 45, 13, 36, 48, 8, 14, 37, 30, 17, 41, 8, 47, 24, 26, 37, 44, 5, 9, 13, 10, 28, 42, 44, 4, 9, 13, 7, 37, 21, 42, 29, 16, 7, 15, 15, 15, 30, 4, 47, 49, 46, 8, 48, 20, 36, 36, 17, 41, 47, 30, 2, 27, 24, 46, 31, 33, 11, 38, 20, 34, 32, 1, 2, 39, 19, 19, 6, 1, 24, 6, 0, 20, 14, 48, 40, 0, 34, 9, 42, 33, 39, 46, 10, 15, 44, 41, 48, 5, 31, 19, 41, 13, 22, 43, 4, 41, 13, 11, 42, 37, 17, 42, 9, 33, 41, 1, 35, 27, 11, 29, 11, 2, 25, 21, 18, 19, 15, 16, 26, 48, 37, 17, 12, 10, 13, 18, 1, 26, 31, 44, 15, 0, 38, 26, 33, 29, 27, 21, 9, 40, 0, 20, 45, 26, 43, 13, 47, 10, 31, 24, 9, 21, 43, 23, 31, 6, 41, 34, 34, 23, 30, 1, 23, 19, 27, 9, 0, 7, 30, 9, 49, 30, 31, 44, 8, 25, 9, 6, 35, 41, 32, 44, 12, 25, 17, 45, 34, 11, 29, 18, 34, 12, 22, 9, 31, 49, 18, 33, 8, 0, 45, 8, 33, 26, 2, 41, 3, 14, 49, 39, 5, 33, 35, 19, 11, 5, 16, 45, 16, 45, 15, 2, 9, 37, 13, 42, 39, 34, 26, 47, 34, 21, 7, 17, 49, 12, 11, 3, 26, 12, 42, 33, 46, 29, 2, 7, 34, 18, 4, 2, 15, 19, 4, 25, 9, 18, 19, 48, 2, 45, 47, 38, 18, 7, 8, 18, 19, 19, 21, 47, 31, 15, 30, 29, 44, 34, 36, 31, 4, 40, 33, 21, 12, 40, 48, 21, 8, 18, 21, 12, 13, 20, 2, 34, 27, 10, 2, 48, 31, 25, 45, 13, 40, 25, 42, 34, 9, 31, 17, 15, 23, 1, 37, 35, 41, 35, 6, 1, 3, 29, 15, 19, 0, 17, 3, 29, 28, 7, 28, 9, 32, 23, 24, 22, 1, 19, 8, 12, 2, 26, 28, 25, 27, 15, 11, 20, 2, 19, 21, 8, 49, 36, 27, 1, 3, 32, 30, 33, 39, 10, 45, 21, 34, 19, 45, 35, 40,

Vetor

0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 5, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 6, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 7, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 9, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 11, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 12, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 13, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 14, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 16, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 17, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 18, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 19, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 20, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 21, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 22, 23, 23, 23, 23, 23, 23, 23, 23, 23, 23, 23, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 24, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 25, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 26, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 27, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 28, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 29, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 30, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 31, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 32, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 33, 34, 34, 34, 34, 34,

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48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 48, 49, 49, 49, 49, 49, 49, 49, 49, 49,
49, 49, 49, 49, 49, 49, 49, 49, 49, 49, 49, 49,
Finishing simulation. Current tick: 5189488000. Reason: target called exit()
---------------- End Simulation ----------------
****
* Resultados da simulação
****

sim_seconds 0.005189 # Number of seconds simulated
sim_ticks 5189488000 # Number of ticks simulated
final_tick 5189488000 # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
sim_freq 1000000000000 # Frequency of simulated ticks
host_inst_rate 123193 # Simulator instruction rate (inst/s)
host_op_rate 202733 # Simulator op (including micro ops) rate (op/s)
host_tick_rate 61909090 # Simulator tick rate (ticks/s)
host_mem_usage 654372 # Number of bytes of host memory used
host_seconds 83.82 # Real time elapsed on the host
sim_insts 10326587 # Number of instructions simulated
sim_ops 16993968 # Number of ops (including micro ops) simulated
system.clk_domain.voltage_domain.voltage 1 # Voltage in Volts
system.clk_domain.clock 500 # Clock period in ticks
system.mem_ctrl.bytes_read::cpu.inst 27648 # Number of bytes read from this memory
system.mem_ctrl.bytes_read::cpu.data 19200 # Number of bytes read from this memory
system.mem_ctrl.bytes_read::total 46848 # Number of bytes read from this memory
system.mem_ctrl.bytes_inst_read::cpu.inst 27648 # Number of instructions bytes read from this memory
system.mem_ctrl.bytes_inst_read::total 27648 # Number of instructions bytes read from this memory
system.mem_ctrl.num_reads::cpu.inst 432 # Number of read requests responded to by this memory
system.mem_ctrl.num_reads::cpu.data 300 # Number of read requests responded to by this memory
system.mem_ctrl.num_reads::total 732 # Number of read requests responded to by this memory
system.mem_ctrl.bw_read::cpu.inst 5327693 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_read::cpu.data 3699787 # Total read bandwidth from this memory (bytes/s)

system.mem_ctrl.bw_read::total 9027480 # Total read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_inst_read::cpu.inst 5327693 # Instruction read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_inst_read::total 5327693 # Instruction read bandwidth from this memory (bytes/s)
system.mem_ctrl.bw_total::cpu.inst 5327693 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.bw_total::cpu.data 3699787 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.bw_total::total 9027480 # Total bandwidth to/from this memory (bytes/s)
system.mem_ctrl.readReqs 732 # Number of read requests accepted
system.mem_ctrl.writeReqs 0 # Number of write requests accepted
system.mem_ctrl.readBursts 732 # Number of DRAM read bursts, including those serviced by the write queue
system.mem_ctrl.writeBursts 0 # Number of DRAM write bursts, including those merged in the write queue
system.mem_ctrl.bytesReadDRAM 46848 # Total number of bytes read from DRAM
system.mem_ctrl.bytesReadWrQ 0 # Total number of bytes read from write queue
system.mem_ctrl.bytesWritten 0 # Total number of bytes written to DRAM
system.mem_ctrl.bytesReadSys 46848 # Total read bytes from the system interface side
system.mem_ctrl.bytesWrittenSys 0 # Total written bytes from the system interface side
system.mem_ctrl.servicedByWrQ 0 # Number of DRAM read bursts serviced by the write queue
system.mem_ctrl.mergedWrBursts 0 # Number of DRAM write bursts merged with an existing one
system.mem_ctrl.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write
system.mem_ctrl.perBankRdBursts::0 72 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::1 120 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::2 73 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::3 60 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::4 66 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::5 35 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::6 136 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::7 8 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::8 14 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::9 33 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::10 34 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::11 16 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::12 31 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::13 27 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::14 5 # Per bank write bursts
system.mem_ctrl.perBankRdBursts::15 2 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::0 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::1 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::2 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::3 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::4 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::5 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::6 0 # Per bank write bursts

system.mem_ctrl.perBankWrBursts::7 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::8 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::9 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::10 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::11 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::12 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::13 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::14 0 # Per bank write bursts
system.mem_ctrl.perBankWrBursts::15 0 # Per bank write bursts
system.mem_ctrl.numRdRetry 0 # Number of times read queue was full causing retry
system.mem_ctrl.numWrRetry 0 # Number of times write queue was full causing retry
system.mem_ctrl.totGap 5189412000 # Total gap between requests
system.mem_ctrl.readPktSize::0 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::1 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::2 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::3 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::4 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::5 0 # Read request sizes (log2)
system.mem_ctrl.readPktSize::6 732 # Read request sizes (log2)
system.mem_ctrl.writePktSize::0 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::1 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::2 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::3 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::4 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::5 0 # Write request sizes (log2)
system.mem_ctrl.writePktSize::6 0 # Write request sizes (log2)
system.mem_ctrl.rdQLenPdf::0 521 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::1 164 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::2 36 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::3 10 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::4 1 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::5 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::6 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::7 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::8 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::9 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::10 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::11 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::12 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::13 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::14 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::15 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::16 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::17 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::18 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::19 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::20 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::21 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::22 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::23 0 # What read queue length does an incoming req see

system.mem_ctrl.rdQLenPdf::24 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::25 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::26 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::27 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::28 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::29 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::30 0 # What read queue length does an incoming req see
system.mem_ctrl.rdQLenPdf::31 0 # What read queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::0 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::1 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::2 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::3 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::4 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::5 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::6 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::7 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::8 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::9 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::10 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::11 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::12 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::13 0 # What write queue length does an incoming req see
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system.mem_ctrl.wrQLenPdf::16 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::17 0 # What write queue length does an incoming req see
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system.mem_ctrl.wrQLenPdf::19 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::20 0 # What write queue length does an incoming req see
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system.mem_ctrl.wrQLenPdf::22 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::23 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::24 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::25 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::26 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::27 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::28 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::29 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::30 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::31 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::32 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::33 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::34 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::35 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::36 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::37 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::38 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::39 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::40 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::41 0 # What write queue length does an incoming req see

system.mem_ctrl.wrQLenPdf::42 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::43 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::44 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::45 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::46 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::47 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::48 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::49 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::50 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::51 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::52 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::53 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::54 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::55 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::56 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::57 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::58 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::59 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::60 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::61 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::62 0 # What write queue length does an incoming req see
system.mem_ctrl.wrQLenPdf::63 0 # What write queue length does an incoming req see
system.mem_ctrl.bytesPerActivate::samples 193 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::mean 232.787565 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::gmean 141.654434 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::stdev 274.055426 # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::0-127 90 46.63% 46.63% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::128-255 48 24.87% 71.50% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::256-383 15 7.77% 79.27% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::384-511 11 5.70% 84.97% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::512-639 7 3.63% 88.60% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::640-767 5 2.59% 91.19% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::768-895 1 0.52% 91.71% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::896-1023 6 3.11% 94.82% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::1024-1151 10 5.18% 100.00% # Bytes accessed per row activation
system.mem_ctrl.bytesPerActivate::total 193 # Bytes accessed per row activation
system.mem_ctrl.totQLat 7611250 # Total ticks spent queuing
system.mem_ctrl.totMemAccLat 21336250 # Total ticks spent from burst creation until serviced by the DRAM
system.mem_ctrl.totBusLat 3660000 # Total ticks spent in databus transfers
system.mem_ctrl.avgQLat 10397.88 # Average queueing delay per DRAM burst

system.mem_ctrl.avgBusLat 5000.00 # Average bus latency per DRAM burst
system.mem_ctrl.avgMemAccLat 29147.88 # Average memory access latency per DRAM burst
system.mem_ctrl.avgRdBW 9.03 # Average DRAM read bandwidth in MiByte/s
system.mem_ctrl.avgWrBW 0.00 # Average achieved write bandwidth in MiByte/s
system.mem_ctrl.avgRdBWSys 9.03 # Average system read bandwidth in MiByte/s
system.mem_ctrl.avgWrBWSys 0.00 # Average system write bandwidth in MiByte/s
system.mem_ctrl.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s
system.mem_ctrl.busUtil 0.07 # Data bus utilization in percentage
system.mem_ctrl.busUtilRead 0.07 # Data bus utilization in percentage for reads
system.mem_ctrl.busUtilWrite 0.00 # Data bus utilization in percentage for writes
system.mem_ctrl.avgRdQLen 1.00 # Average read queue length when enqueuing
system.mem_ctrl.avgWrQLen 0.00 # Average write queue length when enqueuing
system.mem_ctrl.readRowHits 532 # Number of row buffer hits during reads
system.mem_ctrl.writeRowHits 0 # Number of row buffer hits during writes
system.mem_ctrl.readRowHitRate 72.68 # Row buffer hit rate for reads
system.mem_ctrl.writeRowHitRate nan # Row buffer hit rate for writes
system.mem_ctrl.avgGap 7089360.66 # Average gap between requests
system.mem_ctrl.pageHitRate 72.68 # Row buffer hit rate, read and write combined
system.mem_ctrl_0.actEnergy 1028160 # Energy for activate commands per rank (pJ)
system.mem_ctrl_0.preEnergy 561000 # Energy for precharge commands per rank (pJ)
system.mem_ctrl_0.readEnergy 4095000 # Energy for read commands per rank (pJ)
system.mem_ctrl_0.writeEnergy 0 # Energy for write commands per rank (pJ)
system.mem_ctrl_0.refreshEnergy 338700960 # Energy for refresh commands per rank (pJ)
system.mem_ctrl_0.actBackEnergy 307740150 # Energy for active background per rank (pJ)
system.mem_ctrl_0.preBackEnergy 2841594000 # Energy for precharge background per rank (pJ)
system.mem_ctrl_0.totalEnergy 3493719270 # Total energy per rank (pJ)
system.mem_ctrl_0.averagePower 673.695518 # Core power per rank (mW)
system.mem_ctrl_0.memoryStateTime::IDLE 4725970250 # Time in different power states
system.mem_ctrl_0.memoryStateTime::REF 173160000 # Time in different power states
system.mem_ctrl_0.memoryStateTime::PRE_PDN 0 # Time in different power states
system.mem_ctrl_0.memoryStateTime::ACT 286786000 # Time in different power states
system.mem_ctrl_0.memoryStateTime::ACT_PDN 0 # Time in different power states
system.mem_ctrl_1.actEnergy 362880 # Energy for activate commands per rank (pJ)
system.mem_ctrl_1.preEnergy 198000 # Energy for precharge commands per rank (pJ)
system.mem_ctrl_1.readEnergy 1154400 # Energy for read commands per rank (pJ)
system.mem_ctrl_1.writeEnergy 0 # Energy for write commands per rank (pJ)
system.mem_ctrl_1.refreshEnergy 338700960 # Energy for refresh commands per rank (pJ)
system.mem_ctrl_1.actBackEnergy 137382255 # Energy for active background per rank (pJ)
system.mem_ctrl_1.preBackEnergy 2991022500 # Energy for precharge background per rank (pJ)
system.mem_ctrl_1.totalEnergy 3468820995 # Total energy per rank (pJ)
system.mem_ctrl_1.averagePower 668.896145 # Core power per rank (mW)
system.mem_ctrl_1.memoryStateTime::IDLE 4976555000 # Time in different power states
system.mem_ctrl_1.memoryStateTime::REF 173160000 # Time in different power states
system.mem_ctrl_1.memoryStateTime::PRE_PDN 0 # Time in different power states
system.mem_ctrl_1.memoryStateTime::ACT 37029500 # Time in different power states
system.mem_ctrl_1.memoryStateTime::ACT_PDN 0 # Time in different power states
system.cpu.branchPred.lookups 1293422 # Number of BP lookups

system.cpu.branchPred.condPredicted 1293422 # Number of conditional branches predicted
system.cpu.branchPred.condIncorrect 11870 # Number of conditional branches incorrect
system.cpu.branchPred.BTBLookups 1212010 # Number of BTB lookups
system.cpu.branchPred.BTBHits 1162032 # Number of BTB hits
system.cpu.branchPred.BTBCorrect 0 # Number of correct BTB predictions (this stat may not work properly.
system.cpu.branchPred.BTBHitPct 95.876437 # BTB Hit Percentage
system.cpu.branchPred.usedRAS 23339 # Number of times the RAS was used to get a target.
system.cpu.branchPred.RASInCorrect 2113 # Number of incorrect RAS predictions.
system.cpu.apic_clk_domain.clock 8000 # Clock period in ticks
system.cpu.workload.num_syscalls 14 # Number of system calls
system.cpu.numCycles 10378977 # number of cpu cycles simulated
system.cpu.numWorkItemsStarted 0 # number of work items this cpu started
system.cpu.numWorkItemsCompleted 0 # number of work items this cpu completed
system.cpu.fetch.icacheStallCycles 3080325 # Number of cycles fetch is stalled on an Icache miss
system.cpu.fetch.Insts 10539132 # Number of instructions fetch has processed
system.cpu.fetch.Branches 1293422 # Number of branches that fetch encountered
system.cpu.fetch.predictedBranches 1185371 # Number of branches that fetch has predicted taken
system.cpu.fetch.Cycles 7256342 # Number of cycles fetch has run and was not squashing or blocked
system.cpu.fetch.SquashCycles 23971 # Number of cycles fetch has spent squashing
system.cpu.fetch.MiscStallCycles 33 # Number of cycles fetch has spent waiting on interrupts, or bad addresses, or out of MSHRs
system.cpu.fetch.PendingTrapStallCycles 620 # Number of stall cycles due to pending traps
system.cpu.fetch.PendingQuiesceStallCycles 13 # Number of stall cycles due to pending quiesce instructions
system.cpu.fetch.CacheLines 3058327 # Number of cache lines fetched
system.cpu.fetch.IcacheSquashes 4738 # Number of outstanding Icache misses that were squashed
system.cpu.fetch.rateDist::samples 10349318 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::mean 1.677259 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::stdev 1.330249 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::underflows 0 0.00% 0.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::0 3227284 31.18% 31.18% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::1 1684109 16.27% 47.46% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::2 639400 6.18% 53.63% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::3 4798525 46.37% 100.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::overflows 0 0.00% 100.00% # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::min_value 0 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::max_value 3 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.rateDist::total 10349318 # Number of instructions fetched each cycle (Total)
system.cpu.fetch.branchRate 0.124619 # Number of branch fetches per cycle
system.cpu.fetch.rate 1.015431 # Number of inst fetches per cycle
system.cpu.decode.IdleCycles 3049309 # Number of cycles decode is idle
system.cpu.decode.BlockedCycles 250882 # Number of cycles decode is blocked
system.cpu.decode.RunCycles 6943992 # Number of cycles decode is running
system.cpu.decode.UnblockCycles 93150 # Number of cycles decode is unblocking
system.cpu.decode.SquashCycles 11985 # Number of cycles decode is squashing
system.cpu.decode.DecodedInsts 17278344 # Number of instructions handled by decode
system.cpu.decode.SquashedInsts 35949 # Number of squashed instructions handled by decode
system.cpu.rename.SquashCycles 11985 # Number of cycles rename is squashing
system.cpu.rename.IdleCycles 3120293 # Number of cycles rename is idle
system.cpu.rename.BlockCycles 135071 # Number of cycles rename is blocking
system.cpu.rename.serializeStallCycles 833 # count of cycles rename stalled for serializing inst
system.cpu.rename.RunCycles 6958612 # Number of cycles rename is running
system.cpu.rename.UnblockCycles 122524 # Number of cycles rename is unblocking
system.cpu.rename.RenamedInsts 17233838 # Number of instructions processed by rename
system.cpu.rename.SquashedInsts 19961 # Number of squashed instructions processed by rename
system.cpu.rename.ROBFullEvents 81132 # Number of times rename has blocked due to ROB full
system.cpu.rename.IQFullEvents 4003 # Number of times rename has blocked due to IQ full
system.cpu.rename.SQFullEvents 11559 # Number of times rename has blocked due to SQ full
system.cpu.rename.RenamedOperands 24205347 # Number of destination operands rename has renamed
system.cpu.rename.RenameLookups 49674876 # Number of register rename lookups that rename has made
system.cpu.rename.int_rename_lookups 28080818 # Number of integer rename lookups
system.cpu.rename.fp_rename_lookups 156470 # Number of floating rename lookups
system.cpu.rename.CommittedMaps 23879123 # Number of HB maps that are committed
system.cpu.rename.UndoneMaps 326224 # Number of HB maps that are undone due to squashing
system.cpu.rename.serializingInsts 26 # count of serializing insts renamed
system.cpu.rename.tempSerializingInsts 26 # count of temporary serializing insts renamed
system.cpu.rename.skidInsts 204664 # count of insts added to the skid buffer
system.cpu.memDep0.insertedLoads 4885497 # Number of loads inserted to the mem dependence unit.
system.cpu.memDep0.insertedStores 729005 # Number of stores inserted to the mem dependence unit.
system.cpu.memDep0.conflictingLoads 1258349 # Number of conflicting loads.
system.cpu.memDep0.conflictingStores 15658 # Number of conflicting stores.
system.cpu.iq.iqInstsAdded 17218676 # Number of instructions added to the IQ (excludes non-spec)
system.cpu.iq.iqNonSpecInstsAdded 65 # Number of non-speculative instructions added to the IQ

system.cpu.iq.iqInstsIssued 17120529 # Number of instructions issued
system.cpu.iq.iqSquashedInstsIssued 3667 # Number of squashed instructions issued
system.cpu.iq.iqSquashedInstsExamined 224773 # Number of squashed instructions iterated over during squash; mainly for profiling
system.cpu.iq.iqSquashedOperandsExamined 445557 # Number of squashed operands that are examined and possibly removed from graph
system.cpu.iq.iqSquashedNonSpecRemoved 50 # Number of squashed non-spec instructions that were removed
system.cpu.iq.issued_per_cycle::samples 10349318 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::mean 1.654266 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::stdev 0.846531 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::underflows 0 0.00% 0.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::0 651160 6.29% 6.29% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::1 4035707 38.99% 45.29% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::2 4029169 38.93% 84.22% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::3 1506644 14.56% 98.78% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::4 126638 1.22% 100.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::overflows 0 0.00% 100.00% # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::min_value 0 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::max_value 4 # Number of insts issued each cycle
system.cpu.iq.issued_per_cycle::total 10349318 # Number of insts issued each cycle
system.cpu.iq.fu_full::No_OpClass 0 0.00% 0.00% # attempts to use FU when none available
system.cpu.iq.fu_full::IntAlu 1231152 34.50% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::IntMult 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::IntDiv 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatAdd 15 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatCmp 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatCvt 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatMult 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatDiv 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::FloatSqrt 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAdd 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAddAcc 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdAlu 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdCmp 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdCvt 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMisc 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMult 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdMultAcc 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdShift 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdShiftAcc 0 0.00% 34.50% # attempts to use FU when none

available
system.cpu.iq.fu_full::SimdSqrt 0 0.00% 34.50% # attempts to use FU when none available
system.cpu.iq.fu_full::SimdFloatAdd 0 0.00% 34.50% # attempts to use FU when none
available
system.cpu.iq.fu_full::SimdFloatAlu 0 0.00% 34.50% # attempts to use FU when none
available
system.cpu.iq.fu_full::SimdFloatCmp 0 0.00% 34.50% # attempts to use FU when none
available
system.cpu.iq.fu_full::SimdFloatCvt 0 0.00% 34.50% # attempts to use FU when none
available
system.cpu.iq.fu_full::SimdFloatDiv 0 0.00% 34.50% # attempts to use FU when none
available
system.cpu.iq.fu_full::SimdFloatMisc 0 0.00% 34.50% # attempts to use FU when none
available
system.cpu.iq.fu_full::SimdFloatMult 0 0.00% 34.50% # attempts to use FU when none
available
system.cpu.iq.fu_full::SimdFloatMultAcc 0 0.00% 34.50% # attempts to use FU when none
available
system.cpu.iq.fu_full::SimdFloatSqrt 0 0.00% 34.50% # attempts to use FU when none
available
system.cpu.iq.fu_full::MemRead 2288710 64.14% 98.64% # attempts to use FU when none
available
system.cpu.iq.fu_full::MemWrite 48579 1.36% 100.00% # attempts to use FU when none
available
system.cpu.iq.fu_full::IprAccess 0 0.00% 100.00% # attempts to use FU when none available
system.cpu.iq.fu_full::InstPrefetch 0 0.00% 100.00% # attempts to use FU when none
available
system.cpu.iq.FU_type_0::No_OpClass 14206 0.08% 0.08% # Type of FU issued
system.cpu.iq.FU_type_0::IntAlu 11437932 66.81% 66.89% # Type of FU issued
system.cpu.iq.FU_type_0::IntMult 5738 0.03% 66.92% # Type of FU issued
system.cpu.iq.FU_type_0::IntDiv 28 0.00% 66.92% # Type of FU issued
system.cpu.iq.FU_type_0::FloatAdd 72189 0.42% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::FloatCmp 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::FloatCvt 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::FloatMult 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::FloatDiv 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::FloatSqrt 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAdd 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAddAcc 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdAlu 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdCmp 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdCvt 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMisc 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMult 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdMultAcc 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdShift 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdShiftAcc 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdSqrt 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatAdd 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatAlu 0 0.00% 67.35% # Type of FU issued

system.cpu.iq.FU_type_0::SimdFloatCmp 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatCvt 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatDiv 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMisc 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMult 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatMultAcc 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::SimdFloatSqrt 0 0.00% 67.35% # Type of FU issued
system.cpu.iq.FU_type_0::MemRead 4868059 28.43% 95.78% # Type of FU issued
system.cpu.iq.FU_type_0::MemWrite 722377 4.22% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::IprAccess 0 0.00% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::InstPrefetch 0 0.00% 100.00% # Type of FU issued
system.cpu.iq.FU_type_0::total 17120529 # Type of FU issued
system.cpu.iq.rate 1.649539 # Inst issue rate
system.cpu.iq.fu_busy_cnt 3568456 # FU busy when requested
system.cpu.iq.fu_busy_rate 0.208431 # FU busy rate (busy events/executed inst)
system.cpu.iq.int_inst_queue_reads 47973933 # Number of integer instruction queue reads
system.cpu.iq.int_inst_queue_writes 17351191 # Number of integer instruction queue writes
system.cpu.iq.int_inst_queue_wakeup_accesses 16997994 # Number of integer instruction queue wakeup accesses
system.cpu.iq.fp_inst_queue_reads 188566 # Number of floating instruction queue reads
system.cpu.iq.fp_inst_queue_writes 92407 # Number of floating instruction queue writes
system.cpu.iq.fp_inst_queue_wakeup_accesses 92237 # Number of floating instruction queue wakeup accesses
system.cpu.iq.int_alu_accesses 20578475 # Number of integer alu accesses
system.cpu.iq.fp_alu_accesses 96304 # Number of floating point alu accesses
system.cpu.iew.lsq.thread0.forwLoads 1351711 # Number of loads that had data forwarded from stores
system.cpu.iew.lsq.thread0.invAddrLoads 0 # Number of loads ignored due to an invalid address
system.cpu.iew.lsq.thread0.squashedLoads 62951 # Number of loads squashed
system.cpu.iew.lsq.thread0.ignoredResponses 10 # Number of memory responses ignored because the instruction is squashed
system.cpu.iew.lsq.thread0.memOrderViolation 87 # Number of memory ordering violations
system.cpu.iew.lsq.thread0.squashedStores 11457 # Number of stores squashed
system.cpu.iew.lsq.thread0.invAddrSwpfs 0 # Number of software prefetches ignored due to an invalid address
system.cpu.iew.lsq.thread0.blockedLoads 0 # Number of blocked loads due to partial load-store forwarding
system.cpu.iew.lsq.thread0.rescheduledLoads 33 # Number of loads that were rescheduled
system.cpu.iew.lsq.thread0.cacheBlocked 5 # Number of times an access to memory failed due to the cache being blocked
system.cpu.iew.iewIdleCycles 0 # Number of cycles IEW is idle
system.cpu.iew.iewSquashCycles 11985 # Number of cycles IEW is squashing
system.cpu.iew.iewBlockCycles 46982 # Number of cycles IEW is blocking
system.cpu.iew.iewUnblockCycles 3668 # Number of cycles IEW is unblocking
system.cpu.iew.iewDispatchedInsts 17218741 # Number of instructions dispatched to IQ
system.cpu.iew.iewDispSquashedInsts 0 # Number of squashed instructions skipped by dispatch
system.cpu.iew.iewDispLoadInsts 4885497 # Number of dispatched load instructions
system.cpu.iew.iewDispStoreInsts 729005 # Number of dispatched store instructions

system.cpu.iew.iewDispNonSpecInsts 26 # Number of dispatched non-speculative instructions
system.cpu.iew.iewIQFullEvents 1 # Number of times the IQ has become full, causing a stall
system.cpu.iew.iewLSQFullEvents 3660 # Number of times the LSQ has become full, causing a stall
system.cpu.iew.memOrderViolationEvents 87 # Number of memory order violations
system.cpu.iew.predictedTakenIncorrect 6625 # Number of branches that were predicted taken incorrectly
system.cpu.iew.predictedNotTakenIncorrect 7282 # Number of branches that were predicted not taken incorrectly
system.cpu.iew.branchMispredicts 13907 # Number of branch mispredicts detected at execute
system.cpu.iew.iewExecutedInsts 17106419 # Number of executed instructions
system.cpu.iew.iewExecLoadInsts 4861371 # Number of load instructions executed
system.cpu.iew.iewExecSquashedInsts 14110 # Number of squashed instructions skipped in execute
system.cpu.iew.exec_swp 0 # number of swp insts executed
system.cpu.iew.exec_nop 0 # number of nop insts executed
system.cpu.iew.exec_refs 5583112 # number of memory reference insts executed
system.cpu.iew.exec_branches 1267321 # Number of branches executed
system.cpu.iew.exec_stores 721741 # Number of stores executed
system.cpu.iew.exec_rate 1.648180 # Inst execution rate
system.cpu.iew.wb_sent 17095606 # cumulative count of insts sent to commit
system.cpu.iew.wb_count 17090231 # cumulative count of insts written-back
system.cpu.iew.wb_producers 14749050 # num instructions producing a value
system.cpu.iew.wb_consumers 22786770 # num instructions consuming a value
system.cpu.iew.wb_penalized 0 # number of instrctions required to write to 'other' IQ
system.cpu.iew.wb_rate 1.646620 # insts written-back per cycle
system.cpu.iew.wb_fanout 0.647264 # average fanout of values written-back
system.cpu.iew.wb_penalized_rate 0 # fraction of instructions written-back that wrote to 'other' IQ
system.cpu.commit.commitSquashedInsts 200268 # The number of squashed insts skipped by commit
system.cpu.commit.commitNonSpecStalls 15 # The number of times commit has been forced to stall to communicate backwards
system.cpu.commit.branchMispredicts 11903 # The number of times a branch was mispredicted
system.cpu.commit.committed_per_cycle::samples 10294534 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::mean 1.650776 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::stdev 1.532054 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::underflows 0 0.00% 0.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::0 3412856 33.15% 33.15% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::1 2183490 21.21% 54.36% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::2 1368943 13.30% 67.66% # Number of insts

commited each cycle
system.cpu.commit.committed_per_cycle::3 1244388 12.09% 79.75% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::4 2084857 20.25% 100.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::overflows 0 0.00% 100.00% # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::min_value 0 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::max_value 4 # Number of insts commited each cycle
system.cpu.commit.committed_per_cycle::total 10294534 # Number of insts commited each cycle
system.cpu.commit.committedInsts 10326587 # Number of instructions committed
system.cpu.commit.committedOps 16993968 # Number of ops (including micro ops) committed
system.cpu.commit.swp_count 0 # Number of s/w prefetches committed
system.cpu.commit.refs 5540094 # Number of memory references committed
system.cpu.commit.loads 4822546 # Number of loads committed
system.cpu.commit.membars 0 # Number of memory barriers committed
system.cpu.commit.branches 1265077 # Number of branches committed
system.cpu.commit.fp_insts 92163 # Number of committed floating point instructions.
system.cpu.commit.int_insts 16911809 # Number of committed integer instructions.
system.cpu.commit.function_calls 23134 # Number of function calls committed.
system.cpu.commit.op_class_0::No_OpClass 14059 0.08% 0.08% # Class of committed instruction
system.cpu.commit.op_class_0::IntAlu 11361924 66.86% 66.94% # Class of committed instruction
system.cpu.commit.op_class_0::IntMult 5737 0.03% 66.98% # Class of committed instruction
system.cpu.commit.op_class_0::IntDiv 28 0.00% 66.98% # Class of committed instruction
system.cpu.commit.op_class_0::FloatAdd 72126 0.42% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::FloatCmp 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::FloatCvt 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::FloatMult 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::FloatDiv 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::FloatSqrt 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAdd 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAddAcc 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdAlu 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdCmp 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdCvt 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMisc 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMult 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdMultAcc 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdShift 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdShiftAcc 0 0.00% 67.40% # Class of committed

instruction
system.cpu.commit.op_class_0::SimdSqrt 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatAdd 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatAlu 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatCmp 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatCvt 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatDiv 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMisc 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMult 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatMultAcc 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::SimdFloatSqrt 0 0.00% 67.40% # Class of committed instruction
system.cpu.commit.op_class_0::MemRead 4822546 28.38% 95.78% # Class of committed instruction
system.cpu.commit.op_class_0::MemWrite 717548 4.22% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::IprAccess 0 0.00% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::InstPrefetch 0 0.00% 100.00% # Class of committed instruction
system.cpu.commit.op_class_0::total 16993968 # Class of committed instruction
system.cpu.commit.bw_lim_events 2084857 # number cycles where commit BW limit reached
system.cpu.rob.rob_reads 25403913 # The number of ROB reads
system.cpu.rob.rob_writes 34443272 # The number of ROB writes
system.cpu.timesIdled 304 # Number of times that the entire CPU went into an idle state and unscheduled itself
system.cpu.idleCycles 29659 # Total number of cycles that the CPU has spent unscheduled due to idling
system.cpu.committedInsts 10326587 # Number of Instructions Simulated
system.cpu.committedOps 16993968 # Number of Ops (including micro ops) Simulated
system.cpu.cpi 1.005073 # CPI: Cycles Per Instruction
system.cpu.cpi_total 1.005073 # CPI: Total CPI of All Threads
system.cpu.ipc 0.994952 # IPC: Instructions Per Cycle
system.cpu.ipc_total 0.994952 # IPC: Total IPC of All Threads
system.cpu.int_regfile_reads 27844941 # number of integer regfile reads
system.cpu.int_regfile_writes 15021857 # number of integer regfile writes
system.cpu.fp_regfile_reads 156395 # number of floating regfile reads
system.cpu.fp_regfile_writes 76191 # number of floating regfile writes
system.cpu.cc_regfile_reads 13112231 # number of cc regfile reads
system.cpu.cc_regfile_writes 8902391 # number of cc regfile writes
system.cpu.misc_regfile_reads 8118850 # number of misc regfile reads

system.cpu.misc_regfile_writes 1 # number of misc regfile writes
system.cpu.dcache.tags.replacements 9 # number of replacements
system.cpu.dcache.tags.tagsinuse 280.176401 # Cycle average of tags in use
system.cpu.dcache.tags.total_refs 4226766 # Total number of references to valid blocks.
system.cpu.dcache.tags.sampled_refs 302 # Sample count of references to valid blocks.
system.cpu.dcache.tags.avg_refs 13995.913907 # Average number of references to valid blocks.
system.cpu.dcache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.dcache.tags.occ_blocks::cpu.data 280.176401 # Average occupied blocks per requestor
system.cpu.dcache.tags.occ_percent::cpu.data 0.547220 # Average percentage of cache occupancy
system.cpu.dcache.tags.occ_percent::total 0.547220 # Average percentage of cache occupancy
system.cpu.dcache.tags.occ_task_id_blocks::1024 293 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::0 10 # Occupied blocks per task id
system.cpu.dcache.tags.age_task_id_blocks_1024::3 283 # Occupied blocks per task id
system.cpu.dcache.tags.occ_task_id_percent::1024 0.572266 # Percentage of cache occupancy per task id
system.cpu.dcache.tags.tag_accesses 16908806 # Number of tag accesses
system.cpu.dcache.tags.data_accesses 16908806 # Number of data accesses
system.cpu.dcache.ReadReq_hits::cpu.data 3509427 # number of ReadReq hits
system.cpu.dcache.ReadReq_hits::total 3509427 # number of ReadReq hits
system.cpu.dcache.WriteReq_hits::cpu.data 717339 # number of WriteReq hits
system.cpu.dcache.WriteReq_hits::total 717339 # number of WriteReq hits
system.cpu.dcache.demand_hits::cpu.data 4226766 # number of demand (read+write) hits
system.cpu.dcache.demand_hits::total 4226766 # number of demand (read+write) hits
system.cpu.dcache.overall_hits::cpu.data 4226766 # number of overall hits
system.cpu.dcache.overall_hits::total 4226766 # number of overall hits
system.cpu.dcache.ReadReq_misses::cpu.data 151 # number of ReadReq misses
system.cpu.dcache.ReadReq_misses::total 151 # number of ReadReq misses
system.cpu.dcache.WriteReq_misses::cpu.data 209 # number of WriteReq misses
system.cpu.dcache.WriteReq_misses::total 209 # number of WriteReq misses
system.cpu.dcache.demand_misses::cpu.data 360 # number of demand (read+write) misses
system.cpu.dcache.demand_misses::total 360 # number of demand (read+write) misses
system.cpu.dcache.overall_misses::cpu.data 360 # number of overall misses
system.cpu.dcache.overall_misses::total 360 # number of overall misses
system.cpu.dcache.ReadReq_miss_latency::cpu.data 11008750 # number of ReadReq miss cycles
system.cpu.dcache.ReadReq_miss_latency::total 11008750 # number of ReadReq miss cycles
system.cpu.dcache.WriteReq_miss_latency::cpu.data 15026750 # number of WriteReq miss cycles
system.cpu.dcache.WriteReq_miss_latency::total 15026750 # number of WriteReq miss cycles
system.cpu.dcache.demand_miss_latency::cpu.data 26035500 # number of demand (read+write) miss cycles
system.cpu.dcache.demand_miss_latency::total 26035500 # number of demand (read+write) miss cycles
system.cpu.dcache.overall_miss_latency::cpu.data 26035500 # number of overall miss cycles

system.cpu.dcache.overall_miss_latency::total 26035500 # number of overall miss cycles
system.cpu.dcache.ReadReq_accesses::cpu.data 3509578 # number of ReadReq accesses(hits+misses)
system.cpu.dcache.ReadReq_accesses::total 3509578 # number of ReadReq accesses(hits+misses)
system.cpu.dcache.WriteReq_accesses::cpu.data 717548 # number of WriteReq accesses(hits+misses)
system.cpu.dcache.WriteReq_accesses::total 717548 # number of WriteReq accesses(hits+misses)
system.cpu.dcache.demand_accesses::cpu.data 4227126 # number of demand (read+write) accesses
system.cpu.dcache.demand_accesses::total 4227126 # number of demand (read+write) accesses
system.cpu.dcache.overall_accesses::cpu.data 4227126 # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total 4227126 # number of overall (read+write) accesses
system.cpu.dcache.ReadReq_miss_rate::cpu.data 0.000043 # miss rate for ReadReq accesses
system.cpu.dcache.ReadReq_miss_rate::total 0.000043 # miss rate for ReadReq accesses
system.cpu.dcache.WriteReq_miss_rate::cpu.data 0.000291 # miss rate for WriteReq accesses
system.cpu.dcache.WriteReq_miss_rate::total 0.000291 # miss rate for WriteReq accesses
system.cpu.dcache.demand_miss_rate::cpu.data 0.000085 # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total 0.000085 # miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data 0.000085 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.000085 # miss rate for overall accesses
system.cpu.dcache.ReadReq_avg_miss_latency::cpu.data 72905.629139 # average ReadReq miss latency
system.cpu.dcache.ReadReq_avg_miss_latency::total 72905.629139 # average ReadReq miss latency
system.cpu.dcache.WriteReq_avg_miss_latency::cpu.data 71898.325359 # average WriteReq miss latency
system.cpu.dcache.WriteReq_avg_miss_latency::total 71898.325359 # average WriteReq miss latency
system.cpu.dcache.demand_avg_miss_latency::cpu.data 72320.833333 # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total 72320.833333 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data 72320.833333 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total 72320.833333 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 212 # number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs 5 # number of cycles access was blocked
system.cpu.dcache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs 42.400000 # average number of cycles each access was blocked
system.cpu.dcache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.dcache.fast_writes 0 # number of fast writes performed

system.cpu.dcache.cache_copies 0 # number of cache copies performed
system.cpu.dcache.writebacks::writebacks 7 # number of writebacks
system.cpu.dcache.writebacks::total 7 # number of writebacks
system.cpu.dcache.ReadReq_mshr_hits::cpu.data 57 # number of ReadReq MSHR hits
system.cpu.dcache.ReadReq_mshr_hits::total 57 # number of ReadReq MSHR hits
system.cpu.dcache.WriteReq_mshr_hits::cpu.data 1 # number of WriteReq MSHR hits
system.cpu.dcache.WriteReq_mshr_hits::total 1 # number of WriteReq MSHR hits
system.cpu.dcache.demand_mshr_hits::cpu.data 58 # number of demand (read+write) MSHR hits
system.cpu.dcache.demand_mshr_hits::total 58 # number of demand (read+write) MSHR hits
system.cpu.dcache.overall_mshr_hits::cpu.data 58 # number of overall MSHR hits
system.cpu.dcache.overall_mshr_hits::total 58 # number of overall MSHR hits
system.cpu.dcache.ReadReq_mshr_misses::cpu.data 94 # number of ReadReq MSHR misses
system.cpu.dcache.ReadReq_mshr_misses::total 94 # number of ReadReq MSHR misses
system.cpu.dcache.WriteReq_mshr_misses::cpu.data 208 # number of WriteReq MSHR misses
system.cpu.dcache.WriteReq_mshr_misses::total 208 # number of WriteReq MSHR misses
system.cpu.dcache.demand_mshr_misses::cpu.data 302 # number of demand (read+write) MSHR misses
system.cpu.dcache.demand_mshr_misses::total 302 # number of demand (read+write) MSHR misses
system.cpu.dcache.overall_mshr_misses::cpu.data 302 # number of overall MSHR misses
system.cpu.dcache.overall_mshr_misses::total 302 # number of overall MSHR misses
system.cpu.dcache.ReadReq_mshr_miss_latency::cpu.data 7239500 # number of ReadReq MSHR miss cycles
system.cpu.dcache.ReadReq_mshr_miss_latency::total 7239500 # number of ReadReq MSHR miss cycles
system.cpu.dcache.WriteReq_mshr_miss_latency::cpu.data 14608250 # number of WriteReq MSHR miss cycles
system.cpu.dcache.WriteReq_mshr_miss_latency::total 14608250 # number of WriteReq MSHR miss cycles
system.cpu.dcache.demand_mshr_miss_latency::cpu.data 21847750 # number of demand (read+write) MSHR miss cycles
system.cpu.dcache.demand_mshr_miss_latency::total 21847750 # number of demand (read+write) MSHR miss cycles
system.cpu.dcache.overall_mshr_miss_latency::cpu.data 21847750 # number of overall MSHR miss cycles
system.cpu.dcache.overall_mshr_miss_latency::total 21847750 # number of overall MSHR miss cycles
system.cpu.dcache.ReadReq_mshr_miss_rate::cpu.data 0.000027 # mshr miss rate for ReadReq accesses
system.cpu.dcache.ReadReq_mshr_miss_rate::total 0.000027 # mshr miss rate for ReadReq accesses
system.cpu.dcache.WriteReq_mshr_miss_rate::cpu.data 0.000290 # mshr miss rate for WriteReq accesses
system.cpu.dcache.WriteReq_mshr_miss_rate::total 0.000290 # mshr miss rate for WriteReq accesses
system.cpu.dcache.demand_mshr_miss_rate::cpu.data 0.000071 # mshr miss rate for demand accesses
system.cpu.dcache.demand_mshr_miss_rate::total 0.000071 # mshr miss rate for demand

accesses
system.cpu.dcache.overall_mshr_miss_rate::cpu.data 0.000071 # mshr miss rate for overall accesses
system.cpu.dcache.overall_mshr_miss_rate::total 0.000071 # mshr miss rate for overall accesses
system.cpu.dcache.ReadReq_avg_mshr_miss_latency::cpu.data 77015.957447 # average ReadReq mshr miss latency
system.cpu.dcache.ReadReq_avg_mshr_miss_latency::total 77015.957447 # average ReadReq mshr miss latency
system.cpu.dcache.WriteReq_avg_mshr_miss_latency::cpu.data 70231.971154 # average WriteReq mshr miss latency
system.cpu.dcache.WriteReq_avg_mshr_miss_latency::total 70231.971154 # average WriteReq mshr miss latency
system.cpu.dcache.demand_avg_mshr_miss_latency::cpu.data 72343.543046 # average overall mshr miss latency
system.cpu.dcache.demand_avg_mshr_miss_latency::total 72343.543046 # average overall mshr miss latency
system.cpu.dcache.overall_avg_mshr_miss_latency::cpu.data 72343.543046 # average overall mshr miss latency
system.cpu.dcache.overall_avg_mshr_miss_latency::total 72343.543046 # average overall mshr miss latency
system.cpu.dcache.no_allocate_misses 0 # Number of misses that were no-allocate
system.cpu.icache.tags.replacements 29 # number of replacements
system.cpu.icache.tags.tagsinuse 355.685918 # Cycle average of tags in use
system.cpu.icache.tags.total_refs 3057812 # Total number of references to valid blocks.
system.cpu.icache.tags.sampled_refs 438 # Sample count of references to valid blocks.
system.cpu.icache.tags.avg_refs 6981.305936 # Average number of references to valid blocks.
system.cpu.icache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.icache.tags.occ_blocks::cpu.inst 355.685918 # Average occupied blocks per requestor
system.cpu.icache.tags.occ_percent::cpu.inst 0.694699 # Average percentage of cache occupancy
system.cpu.icache.tags.occ_percent::total 0.694699 # Average percentage of cache occupancy
system.cpu.icache.tags.occ_task_id_blocks::1024 409 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::0 64 # Occupied blocks per task id
system.cpu.icache.tags.age_task_id_blocks_1024::3 345 # Occupied blocks per task id
system.cpu.icache.tags.occ_task_id_percent::1024 0.798828 # Percentage of cache occupancy per task id
system.cpu.icache.tags.tag_accesses 12233746 # Number of tag accesses
system.cpu.icache.tags.data_accesses 12233746 # Number of data accesses
system.cpu.icache.ReadReq_hits::cpu.inst 3057812 # number of ReadReq hits
system.cpu.icache.ReadReq_hits::total 3057812 # number of ReadReq hits
system.cpu.icache.demand_hits::cpu.inst 3057812 # number of demand (read+write) hits
system.cpu.icache.demand_hits::total 3057812 # number of demand (read+write) hits
system.cpu.icache.overall_hits::cpu.inst 3057812 # number of overall hits
system.cpu.icache.overall_hits::total 3057812 # number of overall hits
system.cpu.icache.ReadReq_misses::cpu.inst 515 # number of ReadReq misses
system.cpu.icache.ReadReq_misses::total 515 # number of ReadReq misses

system.cpu.icache.demand_misses::cpu.inst 515 # number of demand (read+write) misses
system.cpu.icache.demand_misses::total 515 # number of demand (read+write) misses
system.cpu.icache.overall_misses::cpu.inst 515 # number of overall misses
system.cpu.icache.overall_misses::total 515 # number of overall misses
system.cpu.icache.ReadReq_miss_latency::cpu.inst 35497000 # number of ReadReq miss cycles
system.cpu.icache.ReadReq_miss_latency::total 35497000 # number of ReadReq miss cycles
system.cpu.icache.demand_miss_latency::cpu.inst 35497000 # number of demand (read+write) miss cycles
system.cpu.icache.demand_miss_latency::total 35497000 # number of demand (read+write) miss cycles
system.cpu.icache.overall_miss_latency::cpu.inst 35497000 # number of overall miss cycles
system.cpu.icache.overall_miss_latency::total 35497000 # number of overall miss cycles
system.cpu.icache.ReadReq_accesses::cpu.inst 3058327 # number of ReadReq accesses(hits+misses)
system.cpu.icache.ReadReq_accesses::total 3058327 # number of ReadReq accesses(hits+misses)
system.cpu.icache.demand_accesses::cpu.inst 3058327 # number of demand (read+write) accesses
system.cpu.icache.demand_accesses::total 3058327 # number of demand (read+write) accesses
system.cpu.icache.overall_accesses::cpu.inst 3058327 # number of overall (read+write) accesses
system.cpu.icache.overall_accesses::total 3058327 # number of overall (read+write) accesses
system.cpu.icache.ReadReq_miss_rate::cpu.inst 0.000168 # miss rate for ReadReq accesses
system.cpu.icache.ReadReq_miss_rate::total 0.000168 # miss rate for ReadReq accesses
system.cpu.icache.demand_miss_rate::cpu.inst 0.000168 # miss rate for demand accesses
system.cpu.icache.demand_miss_rate::total 0.000168 # miss rate for demand accesses
system.cpu.icache.overall_miss_rate::cpu.inst 0.000168 # miss rate for overall accesses
system.cpu.icache.overall_miss_rate::total 0.000168 # miss rate for overall accesses
system.cpu.icache.ReadReq_avg_miss_latency::cpu.inst 68926.213592 # average ReadReq miss latency
system.cpu.icache.ReadReq_avg_miss_latency::total 68926.213592 # average ReadReq miss latency
system.cpu.icache.demand_avg_miss_latency::cpu.inst 68926.213592 # average overall miss latency
system.cpu.icache.demand_avg_miss_latency::total 68926.213592 # average overall miss latency
system.cpu.icache.overall_avg_miss_latency::cpu.inst 68926.213592 # average overall miss latency
system.cpu.icache.overall_avg_miss_latency::total 68926.213592 # average overall miss latency
system.cpu.icache.blocked_cycles::no_mshrs 113 # number of cycles access was blocked
system.cpu.icache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.icache.blocked::no_mshrs 1 # number of cycles access was blocked
system.cpu.icache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.icache.avg_blocked_cycles::no_mshrs 113 # average number of cycles each access was blocked
system.cpu.icache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked

system.cpu.icache.fast_writes 0 # number of fast writes performed
system.cpu.icache.cache_copies 0 # number of cache copies performed
system.cpu.icache.ReadReq_mshr_hits::cpu.inst 76 # number of ReadReq MSHR hits
system.cpu.icache.ReadReq_mshr_hits::total 76 # number of ReadReq MSHR hits
system.cpu.icache.demand_mshr_hits::cpu.inst 76 # number of demand (read+write) MSHR hits
system.cpu.icache.demand_mshr_hits::total 76 # number of demand (read+write) MSHR hits
system.cpu.icache.overall_mshr_hits::cpu.inst 76 # number of overall MSHR hits
system.cpu.icache.overall_mshr_hits::total 76 # number of overall MSHR hits
system.cpu.icache.ReadReq_mshr_misses::cpu.inst 439 # number of ReadReq MSHR misses
system.cpu.icache.ReadReq_mshr_misses::total 439 # number of ReadReq MSHR misses
system.cpu.icache.demand_mshr_misses::cpu.inst 439 # number of demand (read+write) MSHR misses
system.cpu.icache.demand_mshr_misses::total 439 # number of demand (read+write) MSHR misses
system.cpu.icache.overall_mshr_misses::cpu.inst 439 # number of overall MSHR misses
system.cpu.icache.overall_mshr_misses::total 439 # number of overall MSHR misses
system.cpu.icache.ReadReq_mshr_miss_latency::cpu.inst 30192000 # number of ReadReq MSHR miss cycles
system.cpu.icache.ReadReq_mshr_miss_latency::total 30192000 # number of ReadReq MSHR miss cycles
system.cpu.icache.demand_mshr_miss_latency::cpu.inst 30192000 # number of demand (read+write) MSHR miss cycles
system.cpu.icache.demand_mshr_miss_latency::total 30192000 # number of demand (read+write) MSHR miss cycles
system.cpu.icache.overall_mshr_miss_latency::cpu.inst 30192000 # number of overall MSHR miss cycles
system.cpu.icache.overall_mshr_miss_latency::total 30192000 # number of overall MSHR miss cycles
system.cpu.icache.ReadReq_mshr_miss_rate::cpu.inst 0.000144 # mshr miss rate for ReadReq accesses
system.cpu.icache.ReadReq_mshr_miss_rate::total 0.000144 # mshr miss rate for ReadReq accesses
system.cpu.icache.demand_mshr_miss_rate::cpu.inst 0.000144 # mshr miss rate for demand accesses
system.cpu.icache.demand_mshr_miss_rate::total 0.000144 # mshr miss rate for demand accesses
system.cpu.icache.overall_mshr_miss_rate::cpu.inst 0.000144 # mshr miss rate for overall accesses
system.cpu.icache.overall_mshr_miss_rate::total 0.000144 # mshr miss rate for overall accesses
system.cpu.icache.ReadReq_avg_mshr_miss_latency::cpu.inst 68774.487472 # average ReadReq mshr miss latency
system.cpu.icache.ReadReq_avg_mshr_miss_latency::total 68774.487472 # average ReadReq mshr miss latency
system.cpu.icache.demand_avg_mshr_miss_latency::cpu.inst 68774.487472 # average overall mshr miss latency
system.cpu.icache.demand_avg_mshr_miss_latency::total 68774.487472 # average overall mshr miss latency
system.cpu.icache.overall_avg_mshr_miss_latency::cpu.inst 68774.487472 # average overall

mshr miss latency
system.cpu.icache.overall_avg_mshr_miss_latency::total 68774.487472 # average overall mshr miss latency
system.cpu.icache.no_allocate_misses 0 # Number of misses that were no-allocate
system.cpu.l2cache.tags.replacements 0 # number of replacements
system.cpu.l2cache.tags.tagsinuse 452.055820 # Cycle average of tags in use
system.cpu.l2cache.tags.total_refs 11 # Total number of references to valid blocks.
system.cpu.l2cache.tags.sampled_refs 528 # Sample count of references to valid blocks.
system.cpu.l2cache.tags.avg_refs 0.020833 # Average number of references to valid blocks.
system.cpu.l2cache.tags.warmup_cycle 0 # Cycle when the warmup percentage was hit.
system.cpu.l2cache.tags.occ_blocks::writebacks 2.894717 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_blocks::cpu.inst 367.534513 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_blocks::cpu.data 81.626591 # Average occupied blocks per requestor
system.cpu.l2cache.tags.occ_percent::writebacks 0.000044 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::cpu.inst 0.005608 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::cpu.data 0.001246 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_percent::total 0.006898 # Average percentage of cache occupancy
system.cpu.l2cache.tags.occ_task_id_blocks::1024 528 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::0 73 # Occupied blocks per task id
system.cpu.l2cache.tags.age_task_id_blocks_1024::3 455 # Occupied blocks per task id
system.cpu.l2cache.tags.occ_task_id_percent::1024 0.008057 # Percentage of cache occupancy per task id
system.cpu.l2cache.tags.tag_accesses 6720 # Number of tag accesses
system.cpu.l2cache.tags.data_accesses 6720 # Number of data accesses
system.cpu.l2cache.ReadReq_hits::cpu.inst 6 # number of ReadReq hits
system.cpu.l2cache.ReadReq_hits::cpu.data 2 # number of ReadReq hits
system.cpu.l2cache.ReadReq_hits::total 8 # number of ReadReq hits
system.cpu.l2cache.Writeback_hits::writebacks 7 # number of Writeback hits
system.cpu.l2cache.Writeback_hits::total 7 # number of Writeback hits
system.cpu.l2cache.demand_hits::cpu.inst 6 # number of demand (read+write) hits
system.cpu.l2cache.demand_hits::cpu.data 2 # number of demand (read+write) hits
system.cpu.l2cache.demand_hits::total 8 # number of demand (read+write) hits
system.cpu.l2cache.overall_hits::cpu.inst 6 # number of overall hits
system.cpu.l2cache.overall_hits::cpu.data 2 # number of overall hits
system.cpu.l2cache.overall_hits::total 8 # number of overall hits
system.cpu.l2cache.ReadReq_misses::cpu.inst 433 # number of ReadReq misses
system.cpu.l2cache.ReadReq_misses::cpu.data 92 # number of ReadReq misses
system.cpu.l2cache.ReadReq_misses::total 525 # number of ReadReq misses
system.cpu.l2cache.ReadExReq_misses::cpu.data 208 # number of ReadExReq misses
system.cpu.l2cache.ReadExReq_misses::total 208 # number of ReadExReq misses
system.cpu.l2cache.demand_misses::cpu.inst 433 # number of demand (read+write) misses
system.cpu.l2cache.demand_misses::cpu.data 300 # number of demand (read+write) misses
system.cpu.l2cache.demand_misses::total 733 # number of demand (read+write) misses

system.cpu.l2cache.overall_misses::cpu.inst 433 # number of overall misses
system.cpu.l2cache.overall_misses::cpu.data 300 # number of overall misses
system.cpu.l2cache.overall_misses::total 733 # number of overall misses
system.cpu.l2cache.ReadReq_miss_latency::cpu.inst 29685000 # number of ReadReq miss cycles
system.cpu.l2cache.ReadReq_miss_latency::cpu.data 7025500 # number of ReadReq miss cycles
system.cpu.l2cache.ReadReq_miss_latency::total 36710500 # number of ReadReq miss cycles
system.cpu.l2cache.ReadExReq_miss_latency::cpu.data 14191250 # number of ReadExReq miss cycles
system.cpu.l2cache.ReadExReq_miss_latency::total 14191250 # number of ReadExReq miss cycles
system.cpu.l2cache.demand_miss_latency::cpu.inst 29685000 # number of demand (read+write) miss cycles
system.cpu.l2cache.demand_miss_latency::cpu.data 21216750 # number of demand (read+write) miss cycles
system.cpu.l2cache.demand_miss_latency::total 50901750 # number of demand (read+write) miss cycles
system.cpu.l2cache.overall_miss_latency::cpu.inst 29685000 # number of overall miss cycles
system.cpu.l2cache.overall_miss_latency::cpu.data 21216750 # number of overall miss cycles
system.cpu.l2cache.overall_miss_latency::total 50901750 # number of overall miss cycles
system.cpu.l2cache.ReadReq_accesses::cpu.inst 439 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.ReadReq_accesses::cpu.data 94 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.ReadReq_accesses::total 533 # number of ReadReq accesses(hits+misses)
system.cpu.l2cache.Writeback_accesses::writebacks 7 # number of Writeback accesses(hits+misses)
system.cpu.l2cache.Writeback_accesses::total 7 # number of Writeback accesses(hits+misses)
system.cpu.l2cache.ReadExReq_accesses::cpu.data 208 # number of ReadExReq accesses(hits+misses)
system.cpu.l2cache.ReadExReq_accesses::total 208 # number of ReadExReq accesses(hits+misses)
system.cpu.l2cache.demand_accesses::cpu.inst 439 # number of demand (read+write) accesses
system.cpu.l2cache.demand_accesses::cpu.data 302 # number of demand (read+write) accesses
system.cpu.l2cache.demand_accesses::total 741 # number of demand (read+write) accesses
system.cpu.l2cache.overall_accesses::cpu.inst 439 # number of overall (read+write) accesses
system.cpu.l2cache.overall_accesses::cpu.data 302 # number of overall (read+write) accesses
system.cpu.l2cache.overall_accesses::total 741 # number of overall (read+write) accesses
system.cpu.l2cache.ReadReq_miss_rate::cpu.inst 0.986333 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_miss_rate::cpu.data 0.978723 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_miss_rate::total 0.984991 # miss rate for ReadReq accesses
system.cpu.l2cache.ReadExReq_miss_rate::cpu.data 1 # miss rate for ReadExReq accesses
system.cpu.l2cache.ReadExReq_miss_rate::total 1 # miss rate for ReadExReq accesses

system.cpu.l2cache.demand_miss_rate::cpu.inst 0.986333 # miss rate for demand accesses
system.cpu.l2cache.demand_miss_rate::cpu.data 0.993377 # miss rate for demand accesses
system.cpu.l2cache.demand_miss_rate::total 0.989204 # miss rate for demand accesses
system.cpu.l2cache.overall_miss_rate::cpu.inst 0.986333 # miss rate for overall accesses
system.cpu.l2cache.overall_miss_rate::cpu.data 0.993377 # miss rate for overall accesses
system.cpu.l2cache.overall_miss_rate::total 0.989204 # miss rate for overall accesses
system.cpu.l2cache.ReadReq_avg_miss_latency::cpu.inst 68556.581986 # average ReadReq miss latency
system.cpu.l2cache.ReadReq_avg_miss_latency::cpu.data 76364.130435 # average ReadReq miss latency
system.cpu.l2cache.ReadReq_avg_miss_latency::total 69924.761905 # average ReadReq miss latency
system.cpu.l2cache.ReadExReq_avg_miss_latency::cpu.data 68227.163462 # average ReadExReq miss latency
system.cpu.l2cache.ReadExReq_avg_miss_latency::total 68227.163462 # average ReadExReq miss latency
system.cpu.l2cache.demand_avg_miss_latency::cpu.inst 68556.581986 # average overall miss latency
system.cpu.l2cache.demand_avg_miss_latency::cpu.data 70722.500000 # average overall miss latency
system.cpu.l2cache.demand_avg_miss_latency::total 69443.042292 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::cpu.inst 68556.581986 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::cpu.data 70722.500000 # average overall miss latency
system.cpu.l2cache.overall_avg_miss_latency::total 69443.042292 # average overall miss latency
system.cpu.l2cache.blocked_cycles::no_mshrs 0 # number of cycles access was blocked
system.cpu.l2cache.blocked_cycles::no_targets 0 # number of cycles access was blocked
system.cpu.l2cache.blocked::no_mshrs 0 # number of cycles access was blocked
system.cpu.l2cache.blocked::no_targets 0 # number of cycles access was blocked
system.cpu.l2cache.avg_blocked_cycles::no_mshrs nan # average number of cycles each access was blocked
system.cpu.l2cache.avg_blocked_cycles::no_targets nan # average number of cycles each access was blocked
system.cpu.l2cache.fast_writes 0 # number of fast writes performed
system.cpu.l2cache.cache_copies 0 # number of cache copies performed
system.cpu.l2cache.ReadReq_mshr_misses::cpu.inst 433 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadReq_mshr_misses::cpu.data 92 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadReq_mshr_misses::total 525 # number of ReadReq MSHR misses
system.cpu.l2cache.ReadExReq_mshr_misses::cpu.data 208 # number of ReadExReq MSHR misses
system.cpu.l2cache.ReadExReq_mshr_misses::total 208 # number of ReadExReq MSHR misses
system.cpu.l2cache.demand_mshr_misses::cpu.inst 433 # number of demand (read+write) MSHR misses
system.cpu.l2cache.demand_mshr_misses::cpu.data 300 # number of demand (read+write) MSHR misses

system.cpu.l2cache.demand_mshr_misses::total 733 # number of demand (read+write) MSHR misses
system.cpu.l2cache.overall_mshr_misses::cpu.inst 433 # number of overall MSHR misses
system.cpu.l2cache.overall_mshr_misses::cpu.data 300 # number of overall MSHR misses
system.cpu.l2cache.overall_mshr_misses::total 733 # number of overall MSHR misses
system.cpu.l2cache.ReadReq_mshr_miss_latency::cpu.inst 27343000 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_latency::cpu.data 6533500 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_latency::total 33876500 # number of ReadReq MSHR miss cycles
system.cpu.l2cache.ReadExReq_mshr_miss_latency::cpu.data 13079750 # number of ReadExReq MSHR miss cycles
system.cpu.l2cache.ReadExReq_mshr_miss_latency::total 13079750 # number of ReadExReq MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::cpu.inst 27343000 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::cpu.data 19613250 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.demand_mshr_miss_latency::total 46956250 # number of demand (read+write) MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::cpu.inst 27343000 # number of overall MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::cpu.data 19613250 # number of overall MSHR miss cycles
system.cpu.l2cache.overall_mshr_miss_latency::total 46956250 # number of overall MSHR miss cycles
system.cpu.l2cache.ReadReq_mshr_miss_rate::cpu.inst 0.986333 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_mshr_miss_rate::cpu.data 0.978723 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadReq_mshr_miss_rate::total 0.984991 # mshr miss rate for ReadReq accesses
system.cpu.l2cache.ReadExReq_mshr_miss_rate::cpu.data 1 # mshr miss rate for ReadExReq accesses
system.cpu.l2cache.ReadExReq_mshr_miss_rate::total 1 # mshr miss rate for ReadExReq accesses
system.cpu.l2cache.demand_mshr_miss_rate::cpu.inst 0.986333 # mshr miss rate for demand accesses
system.cpu.l2cache.demand_mshr_miss_rate::cpu.data 0.993377 # mshr miss rate for demand accesses
system.cpu.l2cache.demand_mshr_miss_rate::total 0.989204 # mshr miss rate for demand accesses
system.cpu.l2cache.overall_mshr_miss_rate::cpu.inst 0.986333 # mshr miss rate for overall accesses
system.cpu.l2cache.overall_mshr_miss_rate::cpu.data 0.993377 # mshr miss rate for overall accesses
system.cpu.l2cache.overall_mshr_miss_rate::total 0.989204 # mshr miss rate for overall accesses
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::cpu.inst 63147.806005 # average

ReadReq mshr miss latency
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::cpu.data 71016.304348 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadReq_avg_mshr_miss_latency::total 64526.666667 # average ReadReq mshr miss latency
system.cpu.l2cache.ReadExReq_avg_mshr_miss_latency::cpu.data 62883.413462 # average ReadExReq mshr miss latency
system.cpu.l2cache.ReadExReq_avg_mshr_miss_latency::total 62883.413462 # average ReadExReq mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::cpu.inst 63147.806005 # average overall mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::cpu.data 65377.500000 # average overall mshr miss latency
system.cpu.l2cache.demand_avg_mshr_miss_latency::total 64060.368349 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::cpu.inst 63147.806005 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::cpu.data 65377.500000 # average overall mshr miss latency
system.cpu.l2cache.overall_avg_mshr_miss_latency::total 64060.368349 # average overall mshr miss latency
system.cpu.l2cache.no_allocate_misses 0 # Number of misses that were no-allocate
system.l2bus.trans_dist::ReadReq 533 # Transaction distribution
system.l2bus.trans_dist::ReadResp 532 # Transaction distribution
system.l2bus.trans_dist::Writeback 7 # Transaction distribution
system.l2bus.trans_dist::ReadExReq 208 # Transaction distribution
system.l2bus.trans_dist::ReadExResp 208 # Transaction distribution
system.l2bus.pkt_count_system.cpu.icache.mem_side::system.cpu.l2cache.cpu_side 877 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_count_system.cpu.dcache.mem_side::system.cpu.l2cache.cpu_side 611 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_count::total 1488 # Packet count per connected master and slave (bytes)
system.l2bus.pkt_size_system.cpu.icache.mem_side::system.cpu.l2cache.cpu_side 28032 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.pkt_size_system.cpu.dcache.mem_side::system.cpu.l2cache.cpu_side 19776 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.pkt_size::total 47808 # Cumulative packet size per connected master and slave (bytes)
system.l2bus.snoops 0 # Total snoops (count)
system.l2bus.snoop_fanout::samples 748 # Request fanout histogram
system.l2bus.snoop_fanout::mean 1 # Request fanout histogram
system.l2bus.snoop_fanout::stdev 0 # Request fanout histogram
system.l2bus.snoop_fanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.l2bus.snoop_fanout::0 0 0.00% 0.00% # Request fanout histogram
system.l2bus.snoop_fanout::1 748 100.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::2 0 0.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.l2bus.snoop_fanout::min_value 1 # Request fanout histogram
system.l2bus.snoop_fanout::max_value 1 # Request fanout histogram
system.l2bus.snoop_fanout::total 748 # Request fanout histogram

system.l2bus.reqLayer0.occupancy 388000 # Layer occupancy (ticks)
system.l2bus.reqLayer0.utilization 0.0 # Layer utilization (%)
system.l2bus.respLayer0.occupancy 1186000 # Layer occupancy (ticks)
system.l2bus.respLayer0.utilization 0.0 # Layer utilization (%)
system.l2bus.respLayer1.occupancy 806750 # Layer occupancy (ticks)
system.l2bus.respLayer1.utilization 0.0 # Layer utilization (%)
system.membus.trans_dist::ReadReq 524 # Transaction distribution
system.membus.trans_dist::ReadResp 524 # Transaction distribution
system.membus.trans_dist::ReadExReq 208 # Transaction distribution
system.membus.trans_dist::ReadExResp 208 # Transaction distribution
system.membus.pkt_count_system.cpu.l2cache.mem_side::system.mem_ctrl.port 1464 # Packet count per connected master and slave (bytes)
system.membus.pkt_count_system.cpu.l2cache.mem_side::total 1464 # Packet count per connected master and slave (bytes)
system.membus.pkt_count::total 1464 # Packet count per connected master and slave (bytes)
system.membus.pkt_size_system.cpu.l2cache.mem_side::system.mem_ctrl.port 46848 # Cumulative packet size per connected master and slave (bytes)
system.membus.pkt_size_system.cpu.l2cache.mem_side::total 46848 # Cumulative packet size per connected master and slave (bytes)
system.membus.pkt_size::total 46848 # Cumulative packet size per connected master and slave (bytes)
system.membus.snoops 0 # Total snoops (count)
system.membus.snoop_fanout::samples 732 # Request fanout histogram
system.membus.snoop_fanout::mean 0 # Request fanout histogram
system.membus.snoop_fanout::stdev 0 # Request fanout histogram
system.membus.snoop_fanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.membus.snoop_fanout::0 732 100.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::1 0 0.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.membus.snoop_fanout::min_value 0 # Request fanout histogram
system.membus.snoop_fanout::max_value 0 # Request fanout histogram
system.membus.snoop_fanout::total 732 # Request fanout histogram
system.membus.reqLayer2.occupancy 366000 # Layer occupancy (ticks)
system.membus.reqLayer2.utilization 0.0 # Layer utilization (%)
system.membus.respLayer0.occupancy 1972750 # Layer occupancy (ticks)
system.membus.respLayer0.utilization 0.0 # Layer utilization (%)