Performance Analysis of CSA using BEC and FZF Logic with Optimized Full Adder Cell

Shivendra Pandey
Department of ECE
LPU, Jalandhar
Punjab, India
nrishivendra@gmail.com

Afshan Khan
Department of ECE
University of Kashmir
Srinagar, India
gtafshan1@gmail.com

Jyotirmoy Pathak
Department of ECE
LPU, Jalandhar
Punjab, India
jyotirmoy4ever@gmail.com

Rajkumar Sarma
Department of ECE
LPU, Jalandhar
Punjab, India
rajkumar.sarma86@gmail.com

***Abstract*— This paper shows the implementation and comparison of Carry Select Adder (CSA) using BEC (Binary Excess one Converter) and First Zero Finding (FZF) logic implementation techniques with optimization of the Full Adder (FA) cell by minimize number of transistors. The results have been analyzed and compared for implementation of both the above logic styles for 28T, 10T and 8T FA cells where as keeping all other basic cells used for implementation of BEC and FZF based CSA same for all three of adder cells. The analysis shows that the CSA using FZF logic is better in terms of power consumption and Power Delay Product (PDP) for all three FA cells however BEC based CSA proves to be better in terms of number of transistors used to implement the overall circuit. All the designs are implemented 1.8Volt power supply and 180nm CMOS process technology in Cadence Virtuoso environment.**

Keywords*— *MUX free CSA; First Zero Finding Logic; BEC; Carry Select Adder; 8T FA; 10T FA.

I. INTRODUCTION

In recent years a large amount of the research effort has been given to improve the system architectures as a whole such as ALU, FIR Filters, FFT implementation etc. However the backbone of a digital system is an adder block. Thus improvement of the adder block will lead to the improvement of the system as a whole without any change in the architecture of the system[1].This work provides a detailed analysis of the MUX free architecture of CSA [1,2] by making use of 28T [3], 10T[4] and 8T[5,6] adder. In the current VLSI industry optimization of both power and area are of prime importance since the demand of the consumers is not only restricted to smaller size of the devices but also higher battery life. In order to achieve such a design specification high speed architectures are to be considered one such architecture is CSA. The CSA is used in many computational systems to alleviate the problem of carry propagation delay by independent generating multiple carries and then select a carry to generate the sum[7]. However, due to the use of an extra Ripple Carry Adder (RCA) as the second stage and ultimately a final stage MUX the area consumed by such a CSA design is very huge, thus not only occupies a large area but also increases the power dissipation of the overall circuit, which can be a point of concern so as to make a device more and more portable. Hence in order to avoid the extra area and power consumption by the CSA an intelligent design scheme was given in[2] which gives the idea of using FZF logic circuit to eliminate the second stage RCA and final stage MUX in a traditional CSA design for front end implementation.

This paper is organized as follows, in section II, we explain the architecture of CSA using BEC logic, in section III architecture of CSA using FZF logic, in section IV Implementation of optimized FA cell, in section V Simulation and result analysis, in section V simulation and result analysis and in section VI give conclusion.

II. ARCHITECTURE OF CSA USING BEC LOGIC

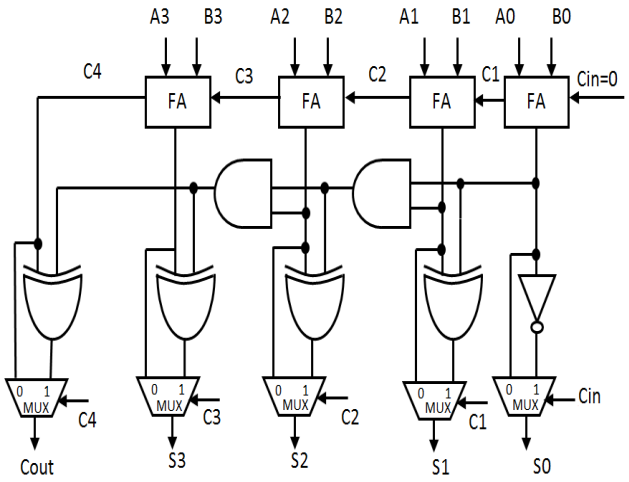


Fig. 1. Architecture of 4-Bit CSA using BEC logic

First, a traditional CSA will consist of the following major blocks that are first stage RCA, second stage RCA and final stage multiplexers for the final selection of the sum bit either for input carry being 0 or 1. In [1,2] a unique design is given that gives implementation of CSA with elimination of the second stage RCA. It uses a BEC logic block to perform the operation provided by the RCA as in Fig 1. When analyzed the second stage of a CSA is nothing but a RCA with input carry as 1, thus any circuit that gives add one operation can be placed in place of the second stage RCA to achieve the desired operation. The operation is achieved by using BEC logic.

A BEC is a combination of XOR gates in conjugation with AND gates such that each and gate acts as an internal carry generator circuit that generates the carry of the two

consecutive sum bits. The first sum bit S0 of the first stage RCA is passed through an inverter and inverted bit is taken as the first sum bit of add one operation. The first sum bit of first stage of RCA is ANDed with the second sum bit of first stage RCA, so as to generate the first internal carry bit. This carry bit generated is summed with third sum bit of the first stage RCA. The same process of generation of the carry from first stage sum bits and summation of consecutive internally generated carry bits with previous sum bits gives the overall add one operation using BEC logic. Thus we obtain the final sum bits for both the possibilities of carry being 0 by first stage RCA and carry being 1 by BEC logic block. These two sequences are sent to a final stage MUX array which selects any of the two sequences based on the previous stage carry being either 0 or 1 as in Fig.1.

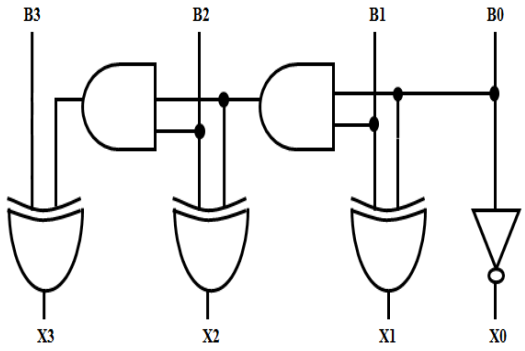


Fig. 2. 4-Bit Binary Excess Converter (BEC) logic

Table I. Function Table of the 4-bit BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
0010	0011
.	.
.	.
.	.
1110	1111
1111	0000

$$X0 = \overline{B0}$$
$$X1 = B0 \oplus B1$$
$$X2 = B2 \oplus (B0 \,\&\, B1)$$
$$X3 = B3 \oplus (B0 \,\&\, B1 \,\&\, B2) \qquad (1)$$

A structure and the function table of a 4-bit BEC are shown in Fig.2 and Table I respectively [6]. The equation (1) shows Boolean expression of 4-bit BEC [1,2,8].

The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. Hence reduces the area and power consumption of the regular CSA to replace the n-bit RCA by an n+1-bit BEC.

One of the reasons of this degradation is the use of 2T MUX at the last stage of the CSA. The use of this MUX adds to the already existing degradation of this CSA. The design of 2T MUX is given in Fig.3. This 2:1 MUX is used to select correct sum and carry output based on carry coming from previous stage [1]. It is implemented in Gate Diffusion Input (GDI) technique, and is bound to give some degradation.

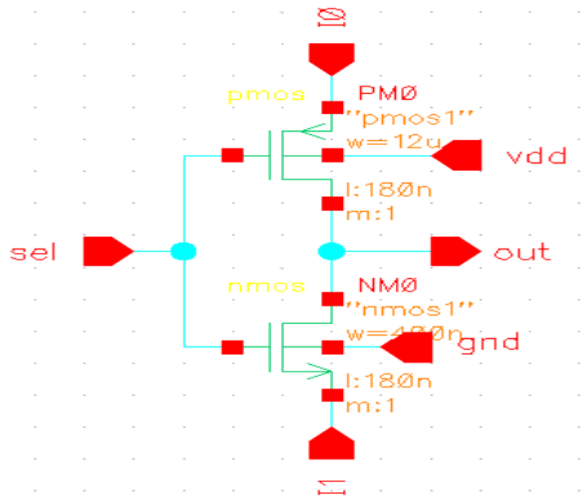


Fig.3 2T MUX cell

III. Architecture Of Mux Free CSA Using FZF Logic

The architecture of a MUX Free CSA uses the advantage of a First Zero Finding (FZF) logic circuit. The operation of the CSA using FZF logic shown in Fig.4 varies on Cin being 1 and 0.Where Cin is the carry of the previous stage. If Cin=0 the logic values of the output of RCA will be passed as such as the final output of CSA. Now if Cin =1 logic circuit will invert all the output bits of RCA from LSB to MSB until it encounters the first zero in the sequence[2,9].

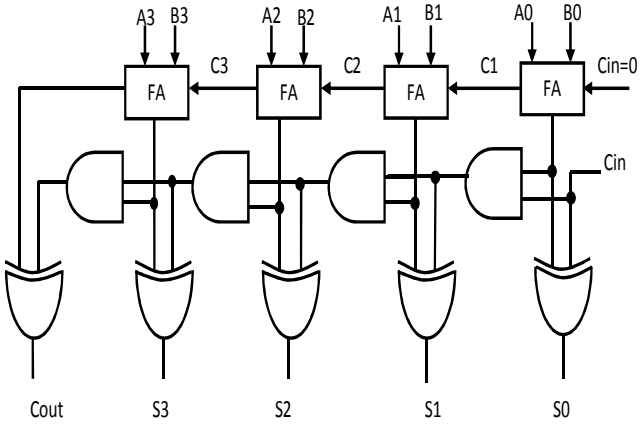


Fig. 4. Architecture of 4-Bit CSA using FZF logic

The use of FZF as the second stage of the CSA shown in Fig. 5 [9] helps eliminate the RCA with Cin=1 and final MUX stage in a traditional CSA architecture. The explanation of FZF logic is given by Example shown in Fig. 6.

The advantages of FZF logic are saving a large amount of power and area as compared to traditional CSA design. However by eliminating the RCA and MUX from final stage the delay of the circuit gets increased to some extent, since the carry has to propagate through large number of AND gates. Thus the critical path of the MUX free CSA is changed and hence results in overall delay slightly greater than the traditional CSA. But compared to the variation in the amount of the delay as compared to the amount of power and area saved is quite appreciable.

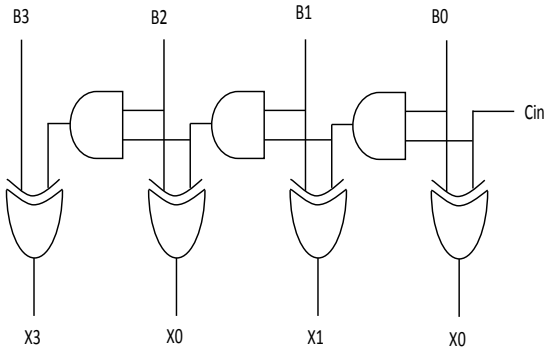
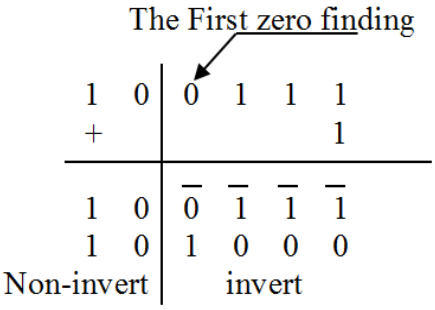
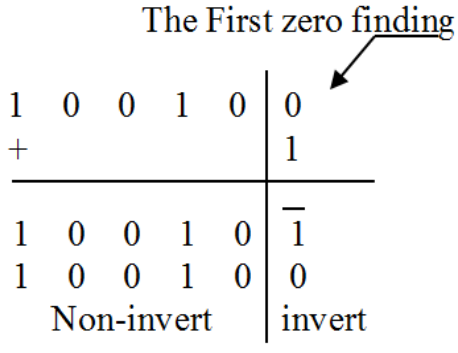


Fig. 5. 4-bit First Zero Finding (FZF) logic



(a)



(b)

Fig. 6. (a) and (b) Example of FZF logic

IV. Implementation of Optimized Full Adder Cell

A. 28T Full Adder cell

The above architecture of CSA using BEC and FZF logic Fig.1 and Fig.4 are implemented by 28T [3] 1-bit FA. The 28T FA cell shown in Fig.7 gives no threshold loss problem that is, gives full swing outputs. It was observed that implementing the above CSA using FZF architecture using 28T adder cell also gives full swing outputs for all input combinations while using BEC logic gives degradation. But has a disadvantage of using large number of transistors for its implementation. In order to save the amount of the area occupied by the large number of transistors in the overall system we shift to smaller adder cells where the number of transistors used to design the adder is lesser than 28T. Since adder being the base cell of a CSA, thus will help to improve the overall area to a great deal.

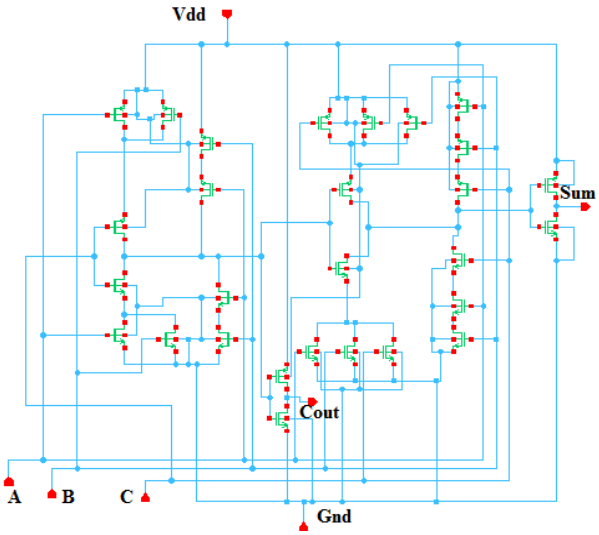


Fig. 7. 28T FA Cell

B. 10T Full Adder Cell

The basic cell used in CSA using BEC and FZF logic is a 10T FA [1,4] shown in Fig.8. Since we are trying to implement the FA using only 10T thus a problem in the output called as threshold loss is expected to be present. Thus may reduce the driving capability of the circuit. However, this full adder proves to be better in terms of the threshold loss problem despite the reduced number of transistors. Moreover after implementing the CSA from both logic shown in Fig.1 and Fig.4 using 10T adder, we are able to reduce power consumption and transistor count to a great deal as compared to CSA implementation using 28T FA.

C. 8T Full Adder Cell

The basic cell used is 8T full adder [5], this cell comprises of three PMOS with a fixed gate negative voltage at volt terminal shown in Fig. 9. The advantage of using negative fixed gate supply is that it keeps PM3 always slightly on so as to improve the output response of the XOR circuit. One of the big advantage of using 8T adder cell as basic cell is that area is reduced to a great deal but has a disadvantage of very much decreased driving capabilities [1].

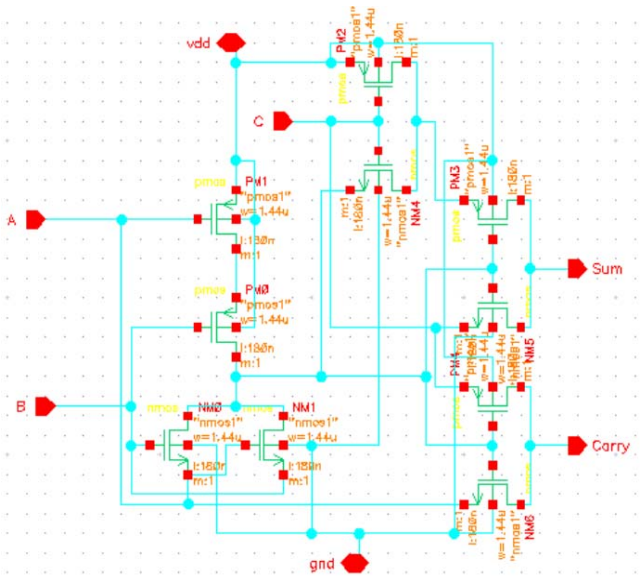


Fig. 8. 10T FA Cell

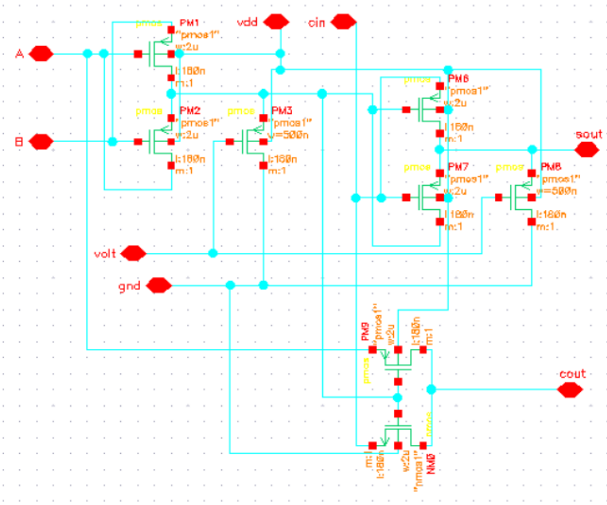


Fig. 9. 8T FA Cell

However when CSA using FZF [2] shown in Fig.4 designed using above 8T adder cell it was observed that the threshold loss problem of the circuit vanishes away and provides almost full swing outputs as the final output of a CSA. The reason for this full swing operation is that the inputs going to the FZF logic circuit act as the gate signals to the transistors present in the FZF logic Circuit but the output of the CSA is driven by the Vdd of the FZF circuit, hence eliminated the threshold loss problem in a 8T based MUX free CSA. However the same FZF incorporates an extra amount of the delay as compared to the traditional CSA. Thus we are able to conclude that it's not only the RCA that can be a reason of delay for a CSA. While in BEC logic gives degraded output.

V. Simulation and Result Analysis

The Simulated waveform of CSA using BEC and FZF logic with optimized FA cell 28T, 10T and 8T are shown in Fig.10, Fig.11, Fig.12, Fig.13, Fig.14 and Fig.15 respectively. Simulated waveform shows that full swing output occurred in case of CSA using FZF logic with 28T, 10T and 8T while degraded output occurred in case of CSA using BEC logic with 28T, 10T and 8T FA. The reason of this degradation is 2T MUX used in last stage.

Table II, Table III, Table IV and Table V shows the comparative analysis of CSA using BEC and FZF logic with 28T, 10T and 8T FA in terms of number of transistors, power, delay and its Power Delay Product (PDP). Graph 1. Shows the graphical representation of CSA using BEC and FZF with optimized FA cells.

TABLE II. Comparison of Number of Transistors used in CSA

Carry Select Adder	28T FA	10T FA	8T FA
Using BEC	184	112	104
Using FZF	196	124	116

TABLE III. Comparison of Power (µw) for CSA

Carry Select Adder	28T FA	10T FA	8T FA
Using BEC	96.6	86.85	363.8
Using FZF	81.4	25.89	274.2

TABLE IV. Comparison of Delay (nS) in CSA

Carry Select Adder	28T FA	10T FA	8T FA
Using BEC	9.23	3.08	22.08
Using FZF	9.16	9.05	10.79

TABLE V. Comparison of PDP (fJ) for CSA

Carry Select Adder	28T FA	10T FA	8T FA
Using BEC	891.61	267.49	2132.98
Using FZF	746.45	234.45	879.27

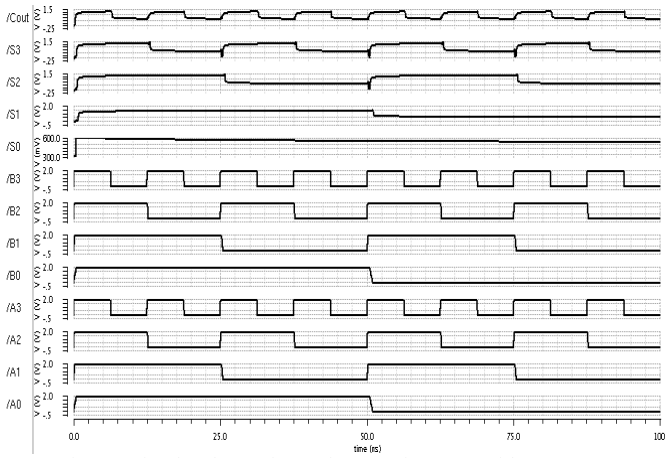


Fig. 10. Simulated waveform of CSA using BEC with 28T FA

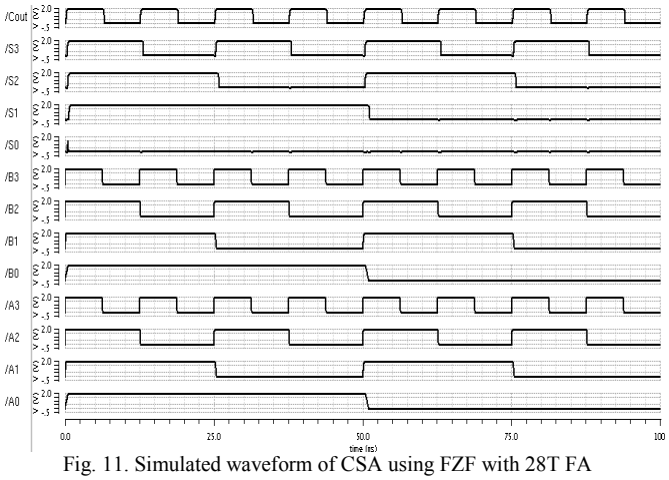


Fig. 11. Simulated waveform of CSA using FZF with 28T FA

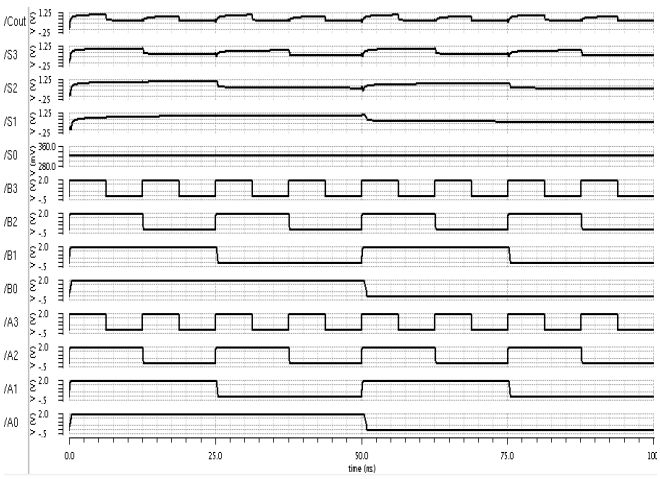


Fig. 12. Simulated waveform of CSA using BEC with 10T FA

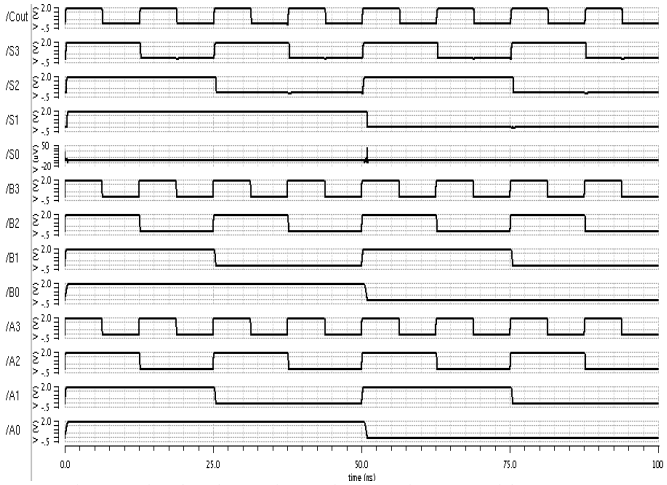


Fig. 13. Simulated waveform of CSA using FZF with 10T FA

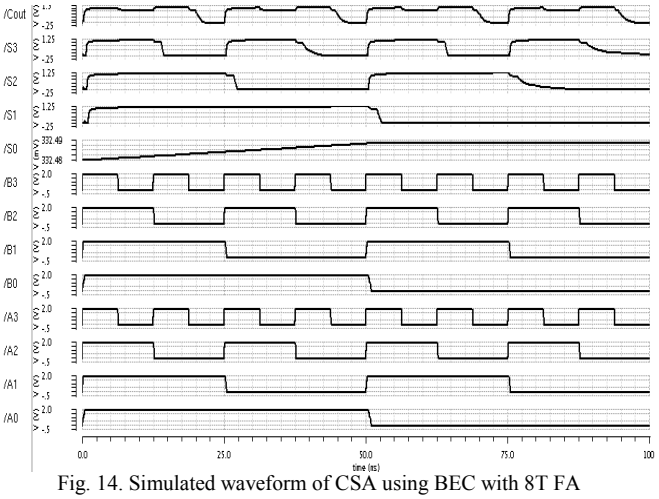


Fig. 14. Simulated waveform of CSA using BEC with 8T FA

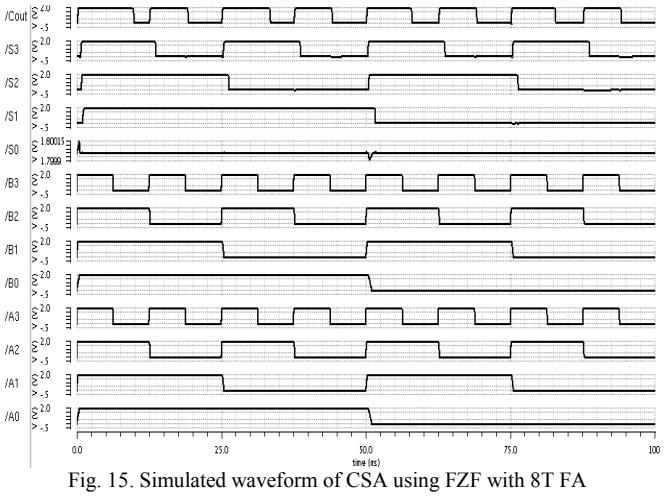
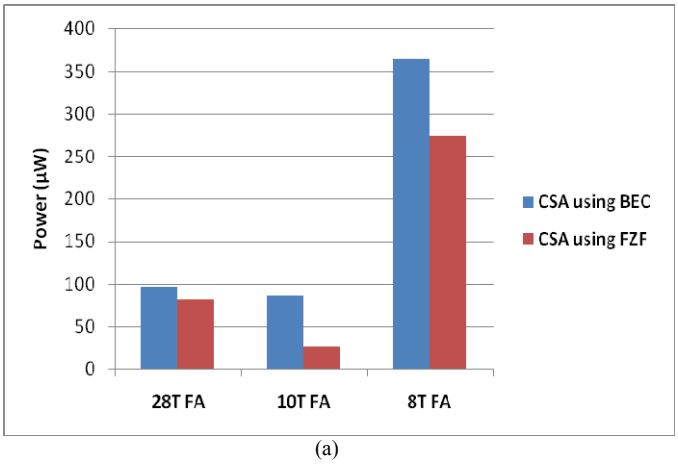
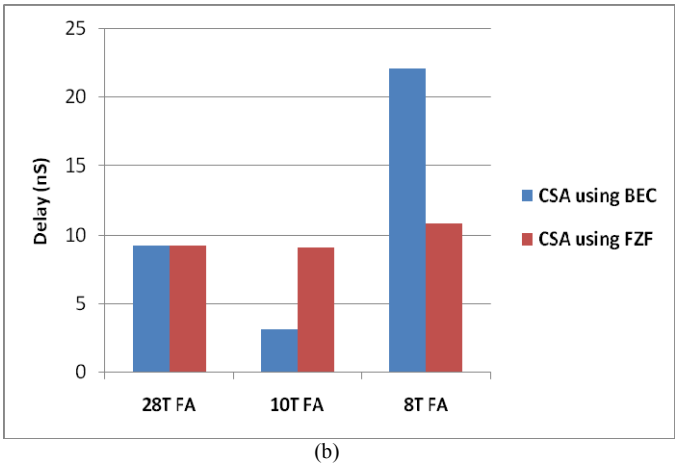


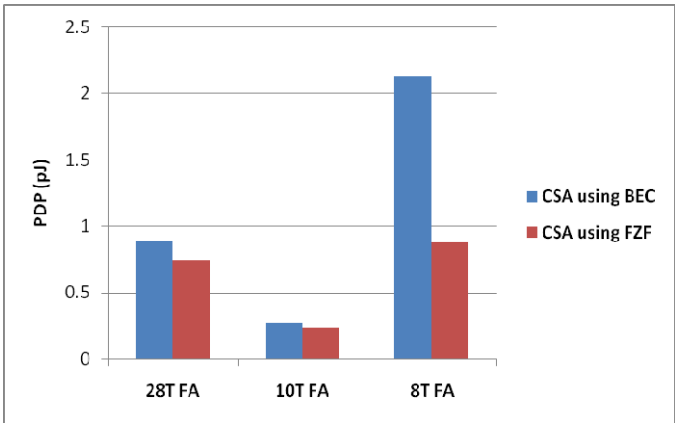
Fig. 15. Simulated waveform of CSA using FZF with 8T FA



(a)



(b)



(c) PDP

Graph 1. Bar graph representation of CSA for (a) Power (b) Delay (c) PDP

VI. Conclusion

In this paper, we have shown the design of CSA using BEC and FZF logic with optimized 28T, 10T and 8T FA cells. It was observed that the power dissipation for CSA using FZF logic is reduced by 15.64%, 70.18% and 24.62% compared to CSA using BEC with 28T, 10T, 8T FA cell respectively. Overall CSA using FZF with 10T FA is better than 28T and 8T. Delay in CSA using FZF is reduced by 0.75% and 65.96% compared to CSA using BEC with 28T and 8T FA respectively. While as for 10T base CSA using FZF logic we observe a delay trade-off of 51.13% compared to BEC logic. However evaluation of PDP shows that PDP of CSA using FZF is reduced by 16.28%, 12.35% and 58.77% compared to CSA using BEC with 28T, 10T and 8T FA cell respectively. Thus we can say the presented design provides significant advantage for applications where battery life is a concern, as the amount of energy used by 10T based CSA using FZF logic is least among all the designs presented above, however the future scope and challenges of the presented design can be taken in the field of using an 8T Full Adder Cell to implement the CSA for higher order bits without any degradation in output.

Acknowledgment

We are very thankful to Department of Electronics and Communication, Lovely Professional University, Jalandhar, India which provided Cadence Virtuoso tool for our analysis. And are also thankful to all the lab staff and security personals involved whose patience and support made us to work with full zeal and zest.

References

[1] Shivendra Pandey,Afshan Amin khan and Rajkumar Sarma," Comparative Analysis of Carry Select Adder using 8T and 10T Full Adder Cells",IEEE International Conference on communication and signal processing,April 2014.

[2] Sajesh Kumar U.,Mohammed Salih K. K. and Sajith K. "Design and Implementation of Carry Select Adder without using Multiplexer," IEEE International Conference on Emerging Technology Trends in Electroncis, Communication and Networking, vol. A247, pp. 529-551,December 2012.

[3] R. Zimmermann and W. Fichtner, "Low-Power logic style : CMOS versus pass-transistor logic," IEEE J.Solid State circuitI,vol.32,p-p 1079-90, July 1997.

[4] Raj Johri, Raghvendra Singh, Satya Prakash, Shyam Akashe, "Comparative analysis of 10T and 14T full adder at 45nm technology", 2nd IEEE International Conference on Parallel, Distributed and Grid Computing, p-p 833-837,Dec 2012.

[5] Afshan Amin, Shivendra Pandey and Jyotirmoy Pathak, "A Review Paper On 3-T XOR cells And 8-T Adder Design in Cadence 180nm," I2CT, Pune, 2014(inpress).

[6] Shiwani Singh, Tripti Sharma, K. G.Sharma,Prof. B. P. Singh, "Array multiplier using PMOS based 3T XOR cell", Innovative Systems Design and Engineering, ISSN 2222-1727, Vol. 3, No 5, 2012.

[7] B. Ramkumar and Harish M Kittur, "Low-Power and area-efficient carry select adder" IEEE transactions on very large scale integration (VLSI) systems. vol. no.-20, p-p 371-375, Feb 2012.

[8] Hemima. R and Chrisjin Gnana Suji.C, "Design of 4 bit low power carry select adder" IEEE International Conference on Signal Processing, Communication, Computing and Networking Technologies (ICSCCN),vol. no.1,p-p 685-688, July 2011.

[9] Shivendra Pandey, Afshan Khan, Jyotirmoy Pathak and Rajkumar Sarma, "Compact Low Power Multiplexer Free Carry Select Adder Using 8T and 10T Full Adder Cell For Emerging VLSI Applications"(Unpublished).