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About



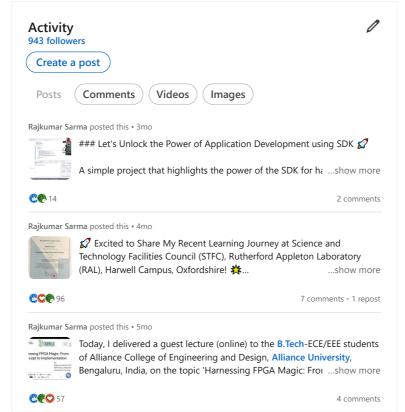
Mith over 12 years of expertise in Digital and Analog circuit design, Low-power VLSI contribute significantly to academia and University of Limerick, I actively Circuits (ADDC) Project, collaborating o. Our collaboration led to first entirely ML-generated Application e of these ML-generated designs has icated using TSMC 65 nm technology, on.

lance Educator at Unacademy, Program-be-University), and Associate Professor my career, I have supervised numerous

M.Tech theses, published extensively in reputable journals, and secured multiple patents, demonstrating my commitment to innovation and research.

Proficient in languages like Verilog HDL, VHDL, and Embedded C, I utilize tools such as Cadence, AMD Xilinx, and KiCad to drive projects forward. My technical competence covers RTL Design, FPGA Prototyping, Analogue/Mixed signal design, Static Timing Analysis (STA), Place-and-route (PnR), and more.

Driven by a passion for technological advancement, I aim to contribute to cuttingedge projects and collaborate with like-minded professionals. Let's connect and explore opportunities to drive innovation and excellence in VLSI design together.



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Experience







Postdoctoral Researcher

University of Limerick \cdot Full-time Sep 2022 - Present \cdot 2 yrs 1 mo Limerick, Ireland

igoplus Report Writing, Verilog HDL and +7 skills



Jain (Deemed-to-be University)

Full-time · 1 yr 5 mos Bengaluru, Karnataka, India

Progam Head (ECE) & Assistant Professor-3

Jul 2022 - Sep 2022 · 3 mos Academic | Administrative | Research

▽ Report Writing, University Teaching and +8 skills

ning and +8 skills

Find more about my profile here: https://unacademy.com/@unacademy-user-x388d26dw8qh

♥ VHDL, Verilog HDL and +7 skills



Lovely Professional University

Full-time · 8 yrs 11 mos

Associate Professor

Oct 2020 - May 2021 · 8 mos Phagwara, Punjab, India

Academic | Research | Administrative

Assistant Professor

Jul 2012 - Sep 2020 · 8 yrs 3 mos Phagwara, Punjab, India

Academic | Research | Administrative

▽ Report Writing, University Teaching and +8 skills



Teaching Assistant

Lovely Professional University · Part-time Jan 2012 - Apr 2012 · 4 mos

Phagwara, Punjab, India

Academic

♥ University Teaching, Interpersonal Communication and +3 skills

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Education







Lovely Professional University

Doctor of Philosophy - PhD, VLSI design

2014 - 2019

Grade: 8.86

♥ Interpersonal Communication, Administrative Processes and +5 skills



Lovely Professional University

 ${\it Master of Technology - MTech, Electrical, Electronics and Communications}$

Engineering 2010 - 2012

Grade: 7.65

♥ Interpersonal Communication, Report Writing and +3 skills

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