QCA Based Sequential And Combinational Circuit Design And Importance Of Parasitic Components

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***Abstract*— As the scaling of transistors has reached its nadir [6], [7], the valid replacement for the CMOS technology to achieve further advancements in the circuits, on the parameters of low power and area occupancy has become an immediate necessity. QCA is one of the greatest potential device technologies ever proposed till date, for the replacement of CMOS Technology. This paper presents the basic theory of Quantum dots with the technology involved in its fabrication, followed by the introduction of QCA including its fundamental concepts i.e. polarization and clocking and, its basic gate(inverter, majority gate) implementations. The working mechanism of complex circuit is given deep glance and, the problems faced during their implementation and working are identified. JK Flip-Flop is used as an example of complex circuitry to understand mechanism and identify problems. At last, the solutions for the identified problems are provided. The output waveforms are provided to demonstrate the behavior of faulty as well as the modified fault free circuits. These designs are captured and simulated using a designing tool called QCA Designer.**

Keywords—QCA, CMOS technology, QCADesigner, Clock, Polarization .

I. INTRODUCTION

The CMOS technology has been ruling the roost for many years and even today it is the best technology available to us, in the electronic field. The Moore's law states that the growth of Integrated Circuits is at the rate of 2X per every 18 months where, X represents number of transistors per unit area [2], [3]. Sadly, since the evinced limitations of this technology viz., leakage current, power dissipation, area overhead, noise margin, speed, error analysis problems (Difficulties in generation of DFTs) and oxide thickness; magnify with the greater circuit complexity as we move to higher level of system integration, the valid replacement for the CMOS technology has become an immediate necessity. Quantum Dot Cellular Automaton proposed(physical implementation) by lent et al. in 1993 [6], [8], is the potential device technology for the replacement of CMOS Technology which provides greater speed, lower power and lesser area overhead [2], [4]. So far, all the practical implementation of the complex circuits in this technology at software level are achievable but, there is still a long way to go, as far as fabrication of the complex circuits is concerned, but it still appears feasible. Also, there are some problems which arise during the designing of complex circuits like power dissipation, signal level, and delay which should be taken care of and, for which it is necessary to have a fundamental knowledge of quantum dots, their polarization and the clocking mechanism of QCA. The identified problems and their solutions are provided in the later sections of this paper.

The rest of this paper is organized as follows. The section II gives a brief description of Quantum Dot. In the section III we have described the QCA Cells, there polarization, there clocking mechanism, the basic gates implementation and, the complex circuit realization using JK Flip-Flop. The section IV identifies the problems which occur in the complex circuits and finally, in the section V some possible solutions for the problems identified are proposed. Finally, the paper is concluded in section VI.

II. QUANTUM DOT

Quantum dots are tiny particles of a semiconducting material with diameters in the ranges of 2-10 nm (size of 10-50 atoms) [13]. They were first discovered in 1980. Quantum dots display unique electronic structural properties, intermediate between those of bulk semiconductors and discrete molecules, because they have unusually high surface-to-volume ratios. In order to implement a logic system that encodes information in the form of electron positioning, it becomes necessary to construct a vessel in which an electron can be trapped and "counted" as if that electron is present in that vessel or not.

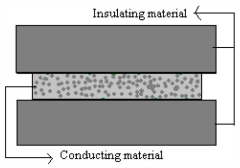

Fig. 1. Fabricated structure of Quantum Dot

A quantum dot does this just by establishing a region of low potential surrounded by a ring of high potential. Such rings are able to trap electrons of sufficiently low energies and are sometimes called potential wells. Quantum dots are made by creating an island of conductive material (such as aluminium) surrounded by insulating material (generally GaAs) as shown in the Fig. 1. An electron that enters a quantum dot will be confined in it because of the deficiency high potential which is required to escape from it. The QCA cell is composed of four and sometimes, five quantum dots.

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III. QCA DESIGN SCHEME

A. QCA Cell

Quantum cell automata consist of four quantum dots which are arranged in square pattern. Each cell is loaded with two extra electrons which tunnel from one low potential region to another through a high potential path (insulator). The electrons will reside diagonally to each other due to mutual repulsive electrostatic force, keeping the farthest distance between them. As mentioned in [10], [11], the QCA Cell is composed of two series connected metal dots separated by tunneling resistance and capacitively coupled to a second identical quantum dot pair. These barriers of the high potential material cause power dissipation during the tunneling of electrons.

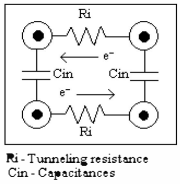


Fig. 2. QCA Cell model

The fig. 2 demonstrates the presence of parasitic elements in a QCA Cell. “Ri” represents the tunneling resistance which is quite high due to insulating material and “Cin” represents the internal capacitance between the two half quantum cells (quantum dot pair).

B. Polarisation

The position of electrons in a QCA Cell determines its polarity and so, the cell polarity in turn determines the logic value of the signal propagating through the circuit [1]. The logic values according to the polarities and the positioning of electrons are represented in Fig. 3 below, where logic 0 represents polarity '-1' and logic 1 represents polarity '+1' repectively.

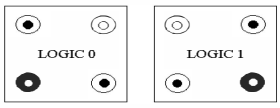


Fig.3. Two polarization states of a basic QCA Cell

The two electrons always acquire diagonal positions due to the presence of electrostatic repulsive forces between them [15]. That’s why, there are only two possible states available in the case of four quantum dot QCA Cell.

C. QCA Clock

In QCA, there are four clocks having phase difference of 90 degrees to one another, which maintain the synchronization in the circuit [10], [12]. Unlike, CMOS technology in which the clock has only two states (low and high).Clock in QCA has four phase namely switch (high to low), hold (low), release (low to high) and relax (high) [9] as shown in Fig. 5(b). In some research papers [1], [6], [11], it is stated that the transition of output transition occurs in low-to-high clock phase but, then there are some journals [9], [17], which show that output transition occur in high-to-low clock phases. Also, we found during our design simulation and analysis that high-to-low clock is the clock phase in which output transition takes place and so, we propose as follows. Out of these four clocks, each clock is fed to the different fragment of the circuit consecutively. Clock 0, Clock 1, Clock 2, Clock 3 are shown in Fig. 5(a) below.

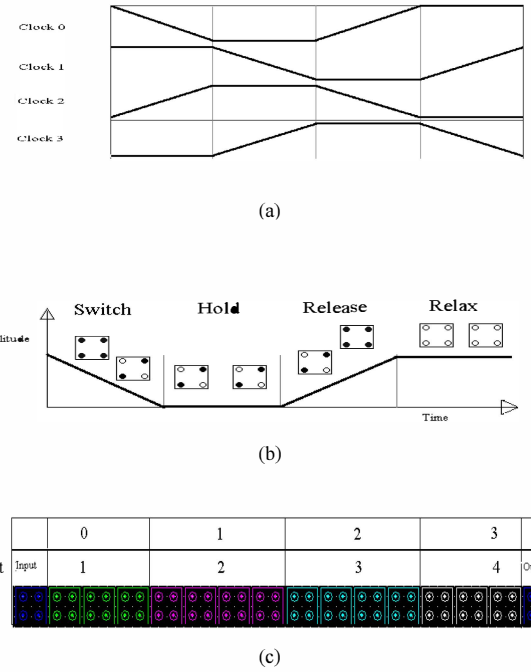


Fig. 5. (a) Four distinctive Clocks in QCA. (b) Effect of a clock on a QCA Cell. (c)QCA Clock dependent QCA wire

A QCA binary wire depicting different clocks forced on the different fragments of the wire is shown in fig. 5(c). The first fragment along with the primary input is fed clock 0, fragment 2 is fed clock 1, fragment 3 is fed clock 2, fragment 4 is fed clock 3 and output is fed clock 0 again, resulting in the total phase shift of 360 degrees and one clock delay at the output. Now, when fragment 1 will be in hold phase, the fragment 2 will be in switch phase. So, the tunneling barrier in fragment 2 starts rising and so, the electron within the cell can be influenced by the columbic charge of neighboring fragment cells. Also, the tunneling barrier of fragment 1 is high and so the states of the cell will not change and so, the polarization states of fragment 1 is propagated to fragment 2. In the second condition , when the fragment 1 is in release phase, the fragment 2 will be in hold state and fragment 3 in switch phase and then the polarization states of fragment 2 are propagated to fragment 3, whereas fragment 1 remains unaffected as the release and relax phase decrease the tunneling barrier making the cells non-influenced by others. Thus, the polarization states of input are propagated to the output with a delay of one clock period.

In this way, the synchronization of the circuit is maintained because the polarization of fragment 1 will not be affected by

the polarization of fragment 2, 3 or, 4 and so the flow of signal will be unidirectional in a single wire. Also, in the sequential circuits in which the output of the present state depends on the previous state output, the clock phases provide one clock period delay.

D. QCA wire

QCA wire consists of chain of cells where the cells are aligned one after another. QCA wire is used to transmit signal from one point to another in a circuit. Logic values are passed from cell to cell due to the Coulomb interactions [14]. There are two types of orientations in a QCA wire viz. Binary wire and Inverter chain [10] as shown in Fig. 4(a) and Fig.4(b) respectively . Binary wire transmits signal with same polarity from one point to another , whereas Inverter chain inverts the polarity of the input cell when odd numbers of cells are used in it.

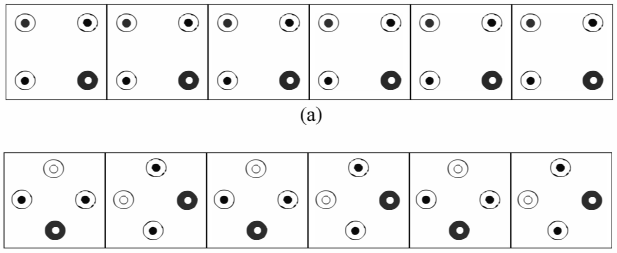


Fig. 4. (a) QCA binary wire. (b) QCA Inverter chain.

E. Basic gate implementation

There are two basic gates in QCA Viz. Inverter and Majority gate [13] as shown in Fig. 6(a, b) .Inverter gate act as NOT gate which gives the inverted logic level of its input at the output. Majority gate is a three input logic gate whose output depends on the majority of the input signals i.e. if two inputs are at logic 1 and one is at logic zero, then output will be the logic 1. The Inverter gate act as a NOT gate whereas the majority gate may act as AND or OR logic gate depending on the fixed polarity applied at its one of the inputs [19].

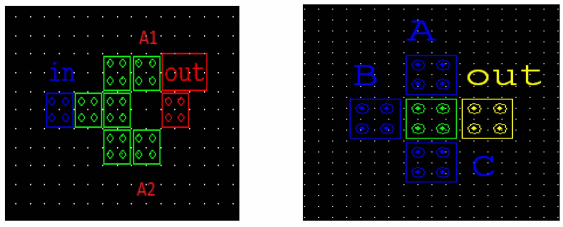


Fig. 6 (a) Basic Inverter gate. (b) Basic Majority gate.

The majority gate can act as AND or OR logic gate depending on the fixed polarity of the third input of the majority gate. If the fixed polarity applied to the third input is +1 then the majority gate will act as an OR logic gate else if the fixed polarity is -1 then majority gate will act as AND logic gate.

The inverter logic gate as shown in Fig. 6(a) above gives the inverted output of the input logic level applied to it. When the input logic 1 is fed to the cell 'in', the input polarization states are propagated to cell A1 and A2 as shown in Fig. 7. Now the polarization state at cell "out" will be dependent on the electrostatic repulsion forces between the electrons present in the top right corner of quantum cell A2 and the bottom left corner of quantum cell A1, which results to logic 0 at output cell.

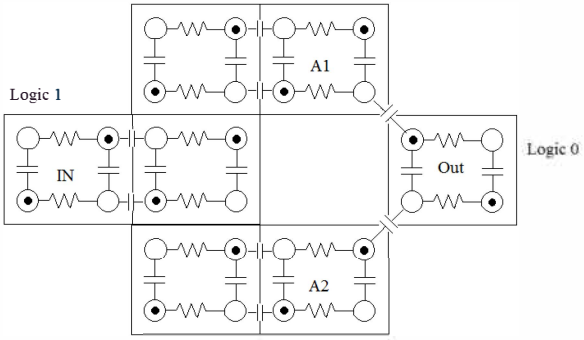


Fig. 7. Involvement of parasitic components in the dissipation and delay caused in an Inverter gate.

Also, in the case of input logic 0 the polarity of output cell will depend on the electrostatic repulsion forces between A1, A2 and 'out' cell, resulting in inverted output 1.In case of majority gate, the basic design is shown in Fig. 8.

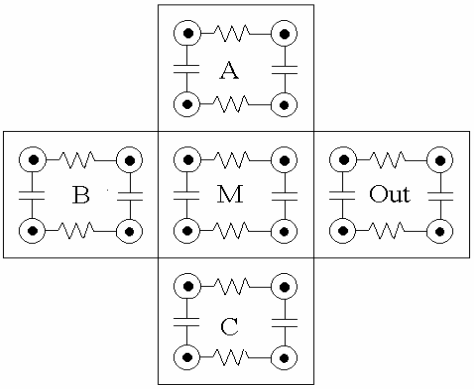


Fig. 8. Involvement of parasitic components in the dissipation and delay caused in an Majority gate.

When the input C is at fixed polarity 1 then the majority gate will act as OR logic AND gate. The waveforms of AND logic gate and OR logic gates implementation using majority gate are shown in Fig. 9 and Fig. 10.

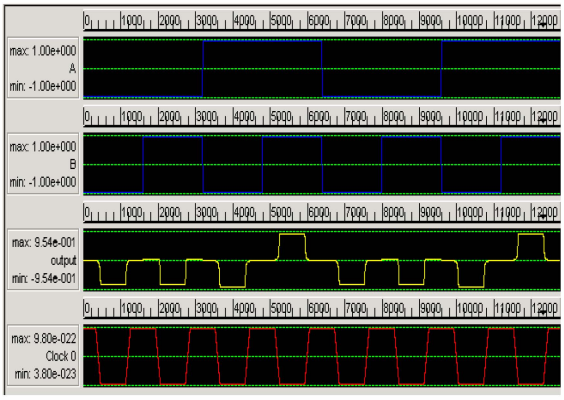


Fig. 9. Simulation output waveform of AND gate.

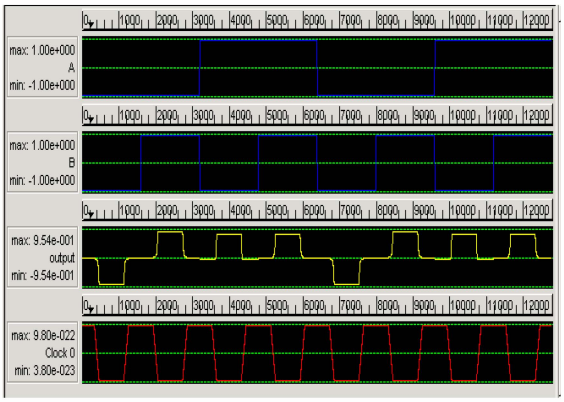


Fig. 10. Simulation output waveform of OR gate.

The Boolean expression of the majority gate is given as:

$$Out = AB+BC+CA \quad (1)$$

so when C=1,

$$Out = AB+B+C$$

i.e.

$$Out = A+B \quad (2)$$

and when C=0,

$$Out = AB \quad (3)$$

F. Complex circuit realization

In the above section, we have studied about the basic gates in QCA. This section explains that how we can construct the complex circuits using basic (inverter and majority) gates. Here, JK flip flop is taken as an example for demonstration of the complex circuit realization. A JK flip flop is a bi-stable multi-vibrator which is used to store one bit of information. When inputs J and K are low, then output is same as that of previous state. If J and K have different values (high and low or low and high) then the output follows J, else if both J and K are high then the output toggles.

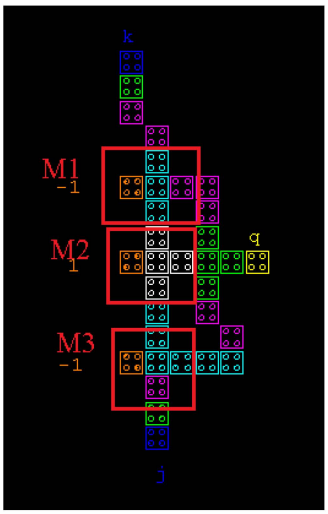


Fig. 11. JK Flip-Flop.

In this circuit, three majority gates and two inverter gates are used. Firstly we have computed the boolean algebra of JK flip flop by Karnaugh Map. The boolean equation of JK flip is evaluated as:

$$Q(t+1)=JQ(t)'+K'Q(t) \quad (4)$$

Then, we have realized this equation using majority gate and inverter gate and designed the circuit as shown on Fig. 11. Also, Fig. 12 shows that how the output waveform of the JK flip flop should be.

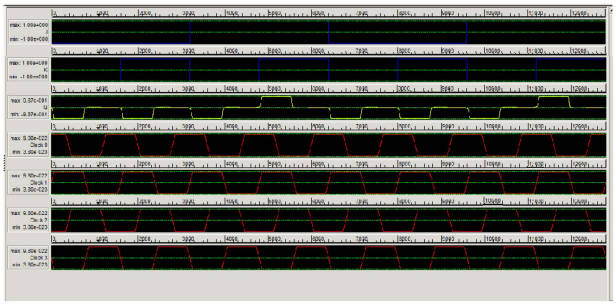


Fig. 12. Simulation output waveform of JK Flip-Flop.

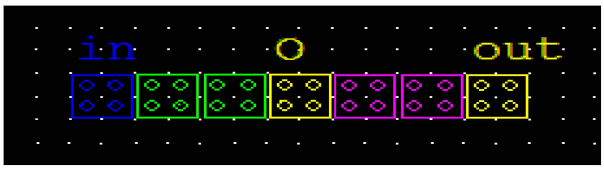
IV. PROBLEMS IN COMPLEX CIRCUITS

During the tunneling of electron from one quantum dot to another in a cell, the power dissipation occurs due to the presence of parasitic effect of the internal tunneling resistance which is present between the two serially connected quantum dots as shown in Fig. 2. Although tangible, this problem is negligible in case of basic gates as shown in Fig. (7) and, Fig. (8). But in case of more complex circuits the problem of power dissipation magnifies which effects the desired output of the circuit. Due to the power dissipation the level of polarization of the cell coming from the input side degrades and thus in a complex circuit during the computation at majority gate the polarization level of fixed polarity cell becomes dominant at

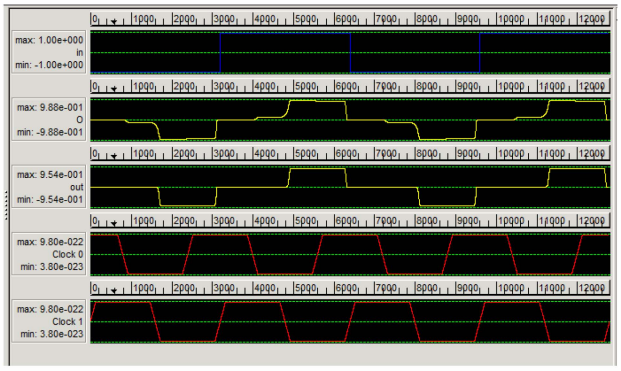
the output of the majority gate and so the output is driven by the fixed polarized cell.

For example, as shown in the Fig. 11, the majority gate of JK flip flop i.e. M1,M2, and M3 drives their respective output in accordance to their fixed polarity cell if the polarization level of their respective fixed polarity cell is at maximum level (P= +1 or P= -1).

Secondly, there is an additional problem which arises due to the transition of the clock phase during the propagation of a signal polarity from cells of one clock region to another in a quantum cell based circuit. As shown in the Fig. 13(a), that when the signal propagates from a cell of one clock region to another than it needs some time to develop polarity in the cells of the second clock region. In the figure it is shown that at cell 'O' which uses clock 1 it takes some amount of time to achieve its polarization, while at the output cell the waveform is proper with some delay because of internal capacitance between the two adjacent cells. The simulated output waveform of fig. 13(a) is shown in Fig. 13(b).



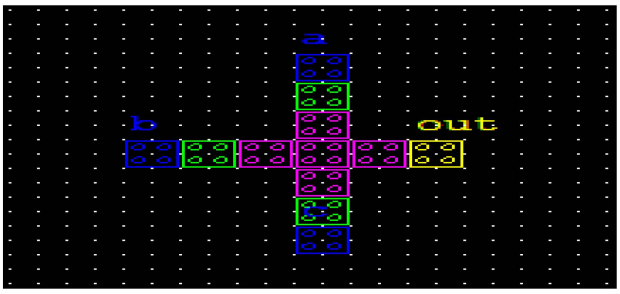
(a)



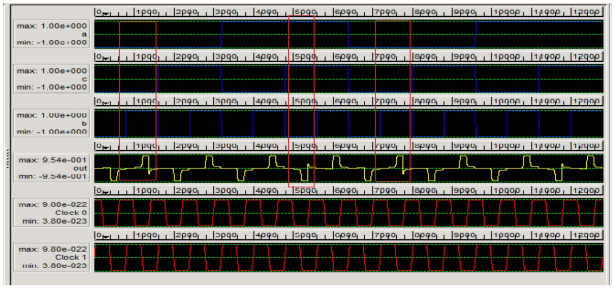
(b)

Fig. 13. (a) A QCA wire with multiple outputs at different points on it. (b) Simulation output waveform depicting the effect of delay on output due to the involvement of internal capacitances.

So, in a complex circuit it is very necessary to place sufficient number of cells of the same clock region as that of majority gates at the inputs of the majority gate. If the number of cells allotted to majority gate at its input of same clock region are few (i.e. only one cell of each input of majority gate) then the output may be undesired because at the same time polarization is developing in the input cells of majority gates as well as computation of the inputs is taking place. So, due to the delay in polarity development because of change in clock regions there is a chance of undesired output. This problem is shown in the Fig. 14(a) and, its simulated output waveform is shown in Fig 14(b). In the waveforms the undesired outputs are marked with red color.



(a)



(b)

Fig. 14. (a) Basic Majority gate depicting the role of tunneling barriers due to clock phase transition. (b) Simulation output waveform displaying the effect of tunneling barriers and input capacitances on the output waveform due to the clock phase transitions.

Also, if the polarization level of input cell is lower than the polarization of the fixed cell in majority gate then, the fixed polarity cell will drive the output even if majority gate gets sufficient number of cells at the inputs of the same clock region as that of majority gate.

V. SOLUTION TO THE PROBLEM FACED IN COMPLEX CIRCUITS

In above section, we have discussed about the various problem occurring in the complex circuit designing .This section is an endeavor to reach the possible solution to the problem identified above.

Firstly, that the power dissipates when the signal propagates to every next cell due to presence of tunneling resistance in each cell. So, we keep the minimum number of cells in order to maintain the least possible power dissipation and to decrease the area overhead. Also, in complex circuits the problem at the majority gates arises due to low polarization level of the inputs as compared to the polarization level of the fixed polarized cells because of the power dissipation caused. So, we propose that the polarization level of the fixed polarized cell should be scaled down from maximum polarization levels (i.e. +1 and -1) to the manageable polarization level in order to avoid the undesired dominance of fixed polarized cells of the majority gate.

Secondly, we saw that the transition of clock phase during propagation of signal from one clock region to another, causes a delay in developing the polarization in second clock region, as when first clock region is in hold state second is in switch state. We have also seen the undesired outputs due to this problem in Fig. 13(b) and 14(b). So as to remove this problem in a complex circuit, we give some cells at the input of majority gate same clock as that of majority gate which helps us to remove this problem. Because in this case, the inputs of majority gate will have proper potential for the computation and hence, it will give the desired output as the potential transition in cell and, majority gate computation occur at different instants of time.

VI. CONCLUSION

As we move towards more compact and high density chips, they become more vulnerable to errors. The parasitic effects play the major role in causing the chip errors which, at major times are undetectable. Once they make impact, and even if we detect the faults the losses are irreparable. Hence, it has become very important to know these errors and their causes before we fabricate any chip, else the chip will end up full of errors due to wrong computations, and signal losses. In above sections, we learned about delay and power dissipation and their causes. It is very easy to note that wrong computations and signal losses are majorly the result of power dissipation and delay and so it is very important to keep these factors in mind before we design or fabricate any chip using QCA.

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REFERENCES

[1] G. Azrul, "Sequential Circuit Design using Quantum-Dot Cellular Automata (QCA)" IEEE.

[2] Steven C. Henderson, " Incorporating Standard CMOS Design Process Methodologies into the QCA Logic Design Process" *IEEE transactions on nanotechnology,* vol. 3, no. 1, march 2004.

[3] D. Grier, "The innovation curve [moore's law in semiconductor industry]." *Computer*, vol. 39, pp. 8-10, feb. 2006.

[4] P. D. Tougaw and C. S. Lent, "Logical devices implemented using quantum cellular automata," *J. Appl. Phys.*, vol. 75, no. 3, pp.1818–1825, 1994.

[5] C. S. Lent, P. D. Tougaw, and W. Porod, "Bistable saturation in coupled quantum dots for quantum cellular automata," *Appl. Phys. Lett.*, vol. 62,p. 714, 1993.

[6] Sarah Tji Yan Chan, " Design of a 4-bit Ripple Adder Using Quantum-dot Cellular Automata (QCA)," *IEEE international conference on circuits and systems* 2013, pp. 33-38.

[7] K. Walus and G. Jullien, "Design Tools for an Emerging SoC Technology: Quantum-Dot Cellular Automata," *Proceedings of the IEEE,* vol. 94, no. 6, pp. 225-1244, June 2006.

[8] C. S. Lent, P. D. Tougaw, W. Porod and G. H. Bernstein, "Quantum Cellular Automata," *Nanotechnology,* vol. 4, no. 1, pp. 49-57, January 1993.

[9] L.S.Karthigai, " Design of Subtractor using Nanotechnology Based QCA ," *IEEE* , 2010.

[10] W. Manisha, " Design and Implementation of 4-Bit Arithmetic Logic Unit using Quantum Dot Cellular Automata," *3rd IEEE International Advance Computing Conference (IACC)* , pp. 1022-1029 , 2013.

[11] T. Rui , " QCA-Based Nano Circuits Design, " IEEE, pp. 2527-2530.

[12] C.Heumpil," Adder and Multiplier Design in Quantum-Dot Cellular Automata, " *IEEE transactions on computers,* vol. 58, no. 6, pp. 721-727, june 2009.

[13]] D.Kunal , "A Novel Approach of And-Or-Inverter (AOI) Gate Design for QCA, " *International Conference on Computers and Devices for Communication*, 2009.

[14] T.Mohammad, "A New Architecture for T Flip Flop using Quantum Dot Cellular Automata, " *IEEE* ,2011.

[15] A. Mehdi ," Design and Analysis of a Sequential Ring Counter for QCA Implementation, " *Proceedings of the International Conference on Computer and Communication Engineering*, 2008.

[16] H.Sara, " A Novel QCA Multiplexer Design, " Internatioal Symposium on Telecommunications ,2008.

[17] Kim A. Escobar, " Parallel Prefix Adder Design Using Quantum-dot Cellular Automata, " *IEEE* , 2013.