Design and Performance Analysis of Reversible Circuits Using 180nm Technology

DISSERTATION-II

Submitted in partial fulfillment of the requirement for the award of the Degree of

MASTER OF TECHNOLOGY
IN
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By

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Under the Guidance of

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(DECEMBER 2013)

CERTIFICATE

This is to certify that the Dissertation-I titled "Design and Performance Analysis of Reversible Circuit Using 180nm Technology" that is being submitted by " ***RITIKA JAIN***" is in partial fulfillment of the requirements for the award of MASTER OF TECHNOLOGY DEGREE, is a record of bonafide work done under my guidance. The contents of this report, in full or in parts, have neither been taken from any other source nor have been submitted to any other Institute or University for award of any degree or diploma and the same is certified.

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Examiner I **Examiner II**

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Lastly, I sincerely pay homage to Almighty God, Parents and Mr.Sanjay Kumar Singh for their blessings that aids as a source of energy and inspiration for me throughout the period.

Registration No. 11200061

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This is to certify that RITIKA JAIN bearing Registration no. 11200061 has completed objective formulation of Dissertation-I titled, **"Design and Performance Analysis of Reversible Circuits using 180nm Technology"** under my guidance and supervision. To the best of my knowledge, the present work is the result of her original investigation and study. No part of the report has ever been submitted for any other degree at any University.

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DECLARATION

I, Ritika Jain, student of Master of Technology under Department of Electronics & Communication of Lovely Professional University, Punjab, hereby declare that all the information furnished in this Dissertation-I report is based on my own intensive research and is genuine.

This report does not, to the best of my knowledge, contain part of my work which has been submitted for the award of my degree either of this university or any other university without proper citation.

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ABSTRACT

Reversible logic is of the flourishing importance to many futuristic technologies. A reversible circuit maps each input vector into a unique output vector. There should not be any information loss in the circuit, because it is proved that each irreversible bit operation dissipate kTln2 amount of energy, but there are so many fields such as cryptography, optical computing, DNA computing etc., where such kind of information loss augments the heat dissipation. As the circuits are getting more compact, soon a limitation to Moore's Law will be achieved hence further no more transistors can be mounted on a single chip. Therefore the next era of technology is transistor less circuits, in which the same operations which are performed now using FETs will be processed at atomic or molecular level. Like we have different techniques to design circuits using FETs such as GDI,PTL,CMOS etc. same functionality can be accomplished using transistor less technique also i.e. called Quantum Dot Cellular Automata(QCA).In this technique quantum dots are used for data or information propagation based on Coulomb's Law of force. The QCA cell consists of maximum of two electrons, these reside in potential well. The basic block of QCA is majority voter, in which QCA cells are arranged in such a manner so that majority votes will be transferred to the output. I have implemented fundamental reversible gates like FG,TG,PG using GDI, PTL, HDL code and QCA techniques. I have made a comparison also to understand the significance of QCA in a more lucid manner.

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LIST OF ABBREVIATIONS

CMOS	Complementary Metal Oxide Semiconductor
CNOT	Controlled NOT Gate
DNA	Deoxyribonucleic Acid
FET	Field Effect Transistor
FG	Feynman Gate
FRG	Fredkin Gate
GDI	Gate Diffusion Input
HDL	Hardware Descriptive Language
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type metal oxide semiconductor
PDP	Power Delay Product
PG	Peres Gate
PMOS	P-Type Metal Oxide Semiconductor
PTL	Pass Transistor Logic
QCA	Quantum Dot Cellular Automata
TG	Toffoli Gate
TR	Thapiyal and Ranganathan Gate

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CHAPTER 1. INTRODUCTION

Reversibility is a term defined as retaining the initial state of any system through its final state. Precisely it can be said as a system with no information loss. This can be simply understood by day to day examples, suppose consider chemical reactions. These reactions can be reversible or irreversible. In irreversible reactions reactants can not be retained through its products, means once formed product cannot be converted back to its raw materials. But in reversible equations reactants can be preserved through products, means nothing is lost. Reversible circuits also work on the same principle; more precisely if we are able to attain inputs back to each output combination then the circuit or system becomes reversible. This approach is generally unusual. Reversibility in circuits is a forecasting computing methodology in Quantum Computing, Optical Computing, nano-technology, DNA Technology and cryptography etc. Reversible computing can only be achieved through reversible gates. In these circuits unique output combination is generated for each unique input pattern, consequently no information is lost and when there is no information loss then according to Bennet circuit exhibits zero power degeneracy [6]. As it is proposed by Landauer that per irreversible bit operation contributes in kT ln2 amount of heat dissipation [5], but if circuits are made reversible then this loss can be oppressed.

Conditions for a gate to be reversible are as follows:

- Same input and output counts.
- Any kind of loop or feedback is not permissible.
- One to One mapping
- No Fan Out is allowed.

1.1 Motivation

Reversible logic is one of the most assuring research field in past few decades. As per irreversible bit operation yields in kTln2 amount of heat dissipation, so to obtain zero heat dissipation we need to make circuits reversible. As we have many applications like in cryptography and DNA computing where irreversible circuitry augments the total heat and power dissipated. Hence for zero energy dissipation we need to model reversible circuits. The other major aspect of reversibility is that only, reversible circuits can be used in Quantum Computers. Consequently reversible logic is demand for quantum computing.

1.2 Irreversible Classical Logic

Classical computation theory began in 1936 when Church and Turing independently published their explorations [19].

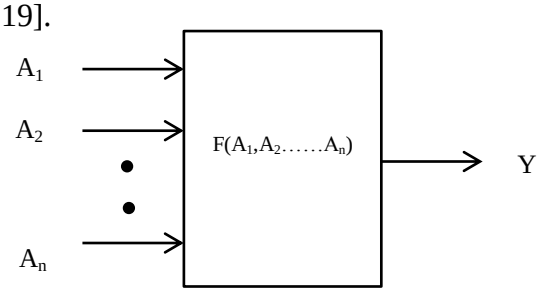


Fig. 1.1 Irreversible Logic

where $Y = F(A_1, A_2, \ldots, A_n)$ describes n discrete inputs. In this case $A_1, A_2 \ldots A_n$, and Y become binary variables, which will take one of two values either 0 or 1. Hence, the function $F(X_1, X_2, \ldots, X_n)$ is known as an n-bit Boolean function. It has been known that NOR & NAND are universal gates and we can implement any Boolean function using these two gates. Apart from this AND, OR, NOT are considered to be fundamental gates. The AND & OR gates have unequal inputs and outputs, while the NOT gate has only single input and output. Gate functions in traditional computing are generally represented by truth table. A truth table consists of all the probable combinations of inputs and their corresponding outputs.

Table 1.1 Conventional Logic Gates

AND			OR			XOR			NAND			NOR			XNOR		
A	**B**	**Y**	**A**	**B**	**Y**	**A**	**B**	**Y**	**A**	**B**	**Y**	**A**	**B**	**Y**	**A**	**B**	**Y**
0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1
0	1	0	0	1	1	0	1	1	0	1	1	0	1	0	0	1	0
1	0	0	1	0	1	1	0	1	1	0	1	1	0	0	1	0	0
1	1	1	1	1	1	1	1	0	1	1	0	1	1	0	1	1	1

Table 1.1 shows the functionality of conventional gates. Hence as the number of bits increases their input combinations also increases exponentially because an n bit Boolean function has 2^n patterns in its truth table. In irreversible logic there is no one to one mapping among inputs and outputs, it means they are not bijective in nature. No one can conclude individual input

combination for a particular output. As each operation in this logic is irreversible, therefore each irreversible bit operation will contribute in kTln2 amount of energy dissipation.

1.3 Reversible Logic

The concept of reversibility elevated in 1970s. There were two tempting concerns for physical reversibility and logical reversibility. A logic will be said physically reversible when no heat dissipation occurs during operation, because in this case there will be no irreversible bit operation, hence there will be no change in entropy. Other way around if we can reconstruct the inputs through outputs uniquely then the system will be termed as logical reversible. The logic for reversible computation will be analogous to that of Fig. 1.1 except there will be one to one mapping among inputs and outputs.

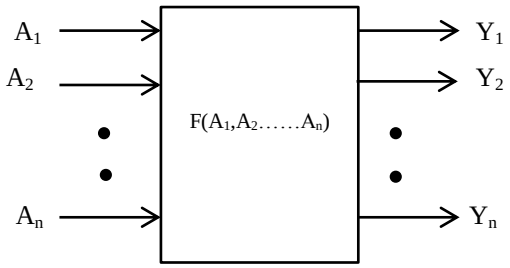


Fig. 1.2 Reversible Logic

The concept of both type of reversibility can be understood with a simple illustration of fundamental OR gate. As OR gate has two inputs and one output, hence it is very much clear that one of its input is completely washed off because we have single output, this removal of one input will turned into information loss to the system. This information loss will contribute in irreversible bit operation resulting in kT ln2 amount of heat dissipation, therefore OR gate is not physically reversible. According to the functionality of OR gate, output results high voltage or logic 1 in three cases, but by looking at the output one cannot predict the input combination for which circuit is giving logic 1, therefore OR gate is not logically reversible.

1.4 Quantum Computing

According to Moore's Law transistor counts on a processor keep on increasing to double every 18 months and area of chip is reduced to half. But there will be a limitation to Moore's Law also, it is predicted that by 2020 or 2030 the circuits will be measured on atomic scale. Therefore quantum computers are the next phase of computing which will exploit the power of atoms and molecules to perform computations. As the name suggests, quantum computing is entirely related to quantum physics. This computing involves the properties of nuclei and atoms. These properties of atoms make them to get composed as qubits on which quantum

computing takes place. These qubits are quantum bits. By interrelating qubits with each other, certain calculations can be executed exponentially faster than traditional computers. Conventional computers work on binary bits, either 0 or 1 but not both at the same time. It means conventional computers work on a single set of numbers at a time. On the other hand qubits are not at all like binary bits. Quantum computers execute operation on sequence of quantum mechanical states like spin of electrons. These spin may represent either 0 or 1, may represent a state in between 1 and 0 or may represent a combination of both the two states. Quantum computers can execute random operations concurrently; this property makes quantum computers to outperform than traditional computers of same dimension. Quantum computing is ideal for cryptography but not suitable for general purpose applications like email, word processing etc.

1.5 Principles of Quantum Computing

There are three fundamental principles which made quantum computing possible. Quantum computing merely a study of quantum physics in which a deep seated study is required , at atomic and subatomic level. The three basic ideologies are explained below to provide a crisp idea about the quantum computing.

1.5.1 Superposition

Superposition is a phenomenon of over imposing of quantum mechanical states on one another. Quantum superposition is an essential standard, which embraces an electron in all its probable arrangements concurrently. But when these states are measured, it doesn't give result regarding all possible states. It offers result to a single state or a general state which will the combination of all the probable arrangements.

1.5.2 Quantum Entanglement

Entanglement stands for a kind of trap or web, in which couple of particles is interrelated in a manner such that quantum state of each particle is characterized with respect to each other. Suppose measurement is taken on one particle of entangled couple and it finds to have anti-clockwise spin. Then surely other grouped particle will have clockwise spin, and then only these can be entangled. In a lucid manner both of the grouped particles will carry opposite spin and this can be measured by applying external force to the entangled group.

1.5.3 Parallelism

Quantum computer works on a million computations at once. As superposition of qubits give parallelism hence this will surely speed up the system. It is predicted that 30-qubit Quantum Computer can run at 10 teraflops, whereas conventional computers run at gigaflops.

1.6 Quantum Dots

Qubit can be atom, molecule, photon or ions. These qubits can be controlled some control devices like Quantum-dot which are tiny particles of a semiconductor materials traditionally selenides and sulfides of metal like cadmium (Cd),zinc (Zn).It ranges from 2 to 10nm in diameter that is about the width of 50 atoms. Because of small size quantum dots exhibits unique optical and electrical properties differently from bulk material. These tiny dots release photons under excitation which are noticeable to human eyes as light.

Wavelength of photons depends on material as well as magnitude of dot i.e. size. If the magnitude of dot is smaller then its radiation will be closed to blue end spectrum, on the other hand if magnitude of dot is larger then radiations will be closed to red end spectrum. The dots can be tuned to beyond visible light i.e. in Ultra Violet or Infra Red region.

In a more lucid manner quantum dot can be explained as a semiconductor nano-structure that limits the motion of electron present in conduction band or hole residing in valence band in all three dimensions. The imprisonment can be due to electrostatics potential or due to an interface between unlike semiconductor substantial. These dots have discrete quantized energy spectrum. Dots have larger band gap than bulk material, smaller dielectric constant. Size of dot of same material is directly proportional to rainbow colors.

Table 1.2 shows dot diameter & band-gap relation.

Table 1.2 Dot Diameter & Band-Gap

Material	Atoms	Band -Gap(eV)
GaAs (Bulk)	-	1.52
GaAs dot	933	2.8
GaAs dot	465	3.2

Hence it is winded up that change in color of light requires only deletion and addition of quantum dots. Quantum dot can hold only a limited number of electrons as compared to bulk material. Consequently, they are the natural way of handling single electrons and, single photons in case of opto-electronic devices. In order to display these novel properties, quantum dots must be just tens of nanometers in extent. This can be achieved using a so-called ‘self-organizing’ formation method [18].

1.6 Reversible Gates

As reversibility condition are mandatory for a gate to behave as reversible. All quantum circuits are by necessity reversible. It is also postulated that quantum computing used in quantum computers are required to have reversible circuits up to some extent Reversible gate is a basic cell of reversible circuit, which can be further extended to build large reversible circuits. In the literature till now many authors have proposed many reversible gates, though some of them are universal and widely used. To transform any irreversible logic function into reversible logic, few terms are needed to be looked before proceeding further.

- **Garbage Output:** The extra pins at the outputs are added to make a function reversible, these extra outputs are called garbage output. These are inserted just to maintain the reversibility of the logic. These pins are always added in outputs. Garbage outputs by explanation are considered to be don't cares [7].
- **Ancilla Bit:** The constant pins added in inputs to make equal input and output counts are called ancilla bits. These can take values of either 0 or 1. These bits play important role when we need to design cascaded circuits for the propagation of information.

1.6.1 Elementary Quantum Gates

Elementary quantum gates are the key elements for quantum computation. Qubit is the basic cell of a quantum computation.

- **Inverter (NOT):** This operates like a conventional NOT gate, inverts the input qubit.
- **Controlled inverter (CNOT):** In this aimed qubit is inverted if the source qubit is 1.
- **Controlled -V gate:** The V operation square root of NOT gate, since two successive V operations are equivalent to an inversion.
- **Controlled- V+ gate:** It is inverse of square root of NOT gate. When controlled-V gate and Controlled-V^+ gates are in successive order then , it results in identity matrix. All elementary gates are assumed to have unit cost [2]. Moreover, when a V or V^+ gate is connected to CNOT between two same qubits, the cost of the pair can be considered as a unit [18]. The symbols for elementary quantum gates are shown in Fig. 1.3.

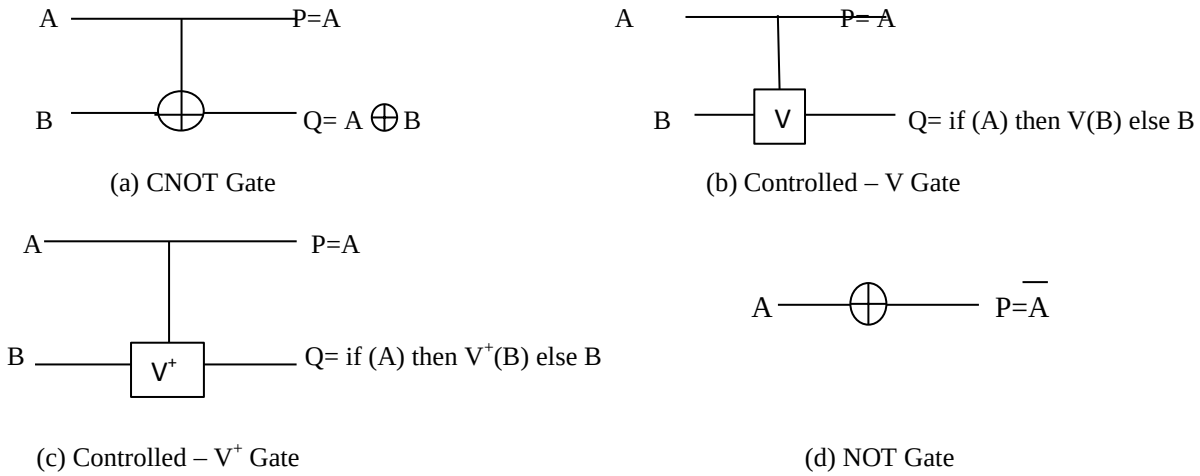


Fig. 1.3 Elementary Quantum Gates

1.6.2 Fundamental Reversible Gates

In this section I will explain briefly about the basic and fundamental reversible gates. The importance of reversible gate is that only a single gate can perform multiple functions simultaneously. Each reversible gate follows with truth table, multiple functions logic table, and quantum representation.

1.6.2.1 Feynman Gate

This gate can be constructed using on CNOT gate, and it will work like reversible XOR gate[16].

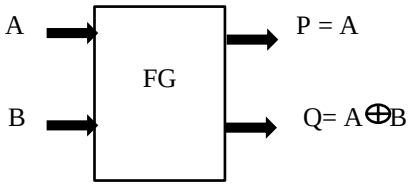


Fig. 1.4 Feynman Gate

The block diagram of Feynman Gate is shown in Fig. 1.4. Output P follows input A and Q performs XOR operation.

Table 1.3 Truth Table of FG

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 1.3 shows the functionality of Feynman gate. It is also called controlled- NOT gate. When A is high it will invert B at the output, else it will pass B signal to the output.

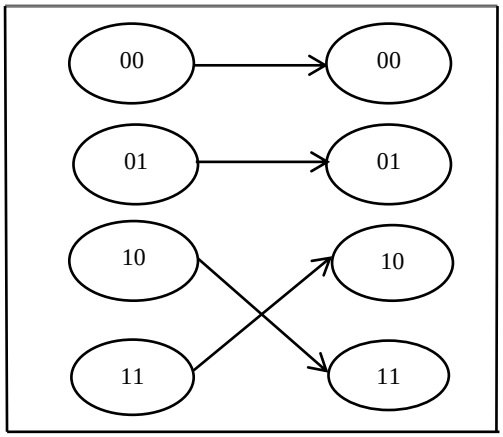


Fig. 1.5 Logical Reversibility of FG

Logical reversibility of FG is shown in Fig. 1.5, all four combinations of inputs result in unique output combinations.

1.6.2.2 Toffoli Gate

It is the first reversible gate invented in 1980 by T.Toffoli [8].This Gate is self reversible, because its twofold combination is the same as itself [9].It has three inputs and three outputs. The block diagram of Toffoli Gate is shown in Fig. 1.6, the outputs P and Q follow input A and B respectively, and R performs the required logic function.

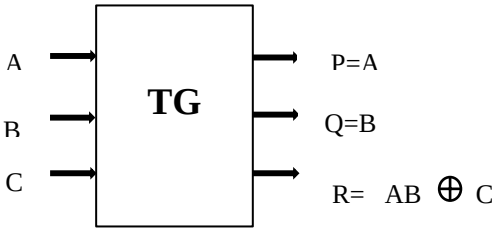


Fig. 1.6 Toffoli Gate

The truth table of Toffoli Gate is shown in Table 1.4 below. Truth table is used for describing behavior of any logic system; all the outputs are in same order as required according to logic.

Table 1.4 Truth Table of TG

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table 1.5 Multifunctional TG

S.No.	A	B	C	P	Q	R	Logic Functions
1	0	B	C	0	B	C	PASS LOGIC
2	1	B	C	1	B	$B \oplus C$	XOR
3	A	0	C	A	0	C	PASS LOGIC
4	A	1	C	A	1	$A \oplus C$	XOR
5	A	B	0	A	B	AB	AND
6	A	B	1	A	B	$\overline{AB}$	NAND

All the reversible gates are multi-functional because of their different output equations. This multi functionality can be achieved by putting different ancilla bits at different inputs. Single reversible gate can serve for different operations. Multi-functionality of Toffoli Gate is shown in Table 1.5.Logical reversibility of TG is shown in Fig.1.7, this proves one to one mapping among inputs and outputs.

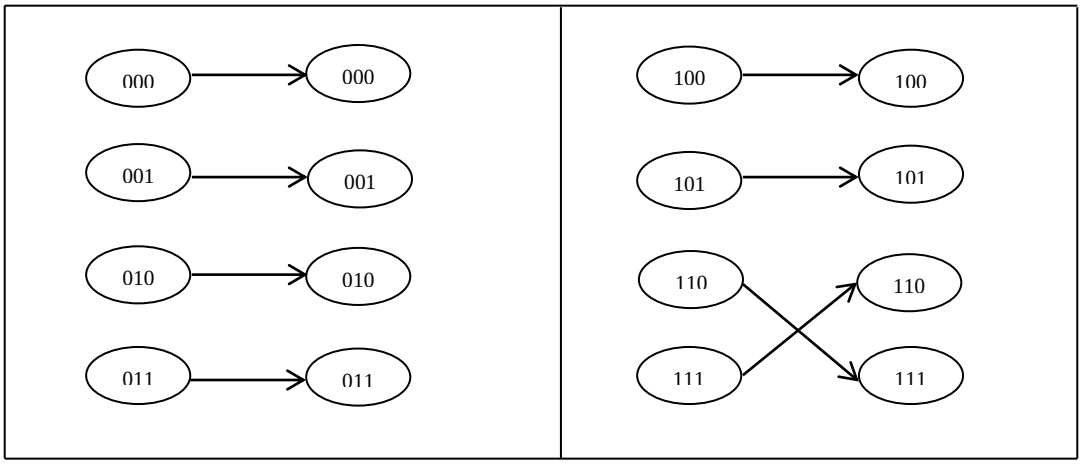


Fig. 1.7 Logical Reversibility of TG

1.6.2.3 Peres Gate

This is a combination of toffoli gate and Feynman gate [25]. It was invented in 1985.

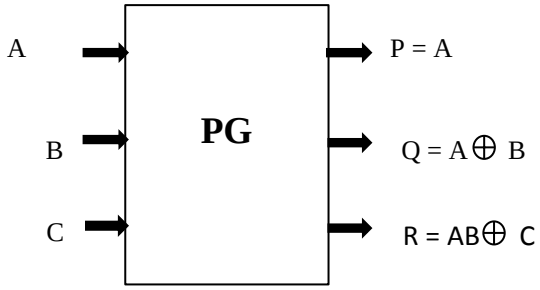


Fig.1.7 Peres Gate

The block diagram of Peres Gate is shown in Fig. 1.7, the outputs P follows input A, Q performs XOR operation and R performs the required logic operation.

Table 1.6 Truth Table of PG

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

The truth table of Peres Gate is shown in Table 1.6; all the outputs are in correct order according to the logic equations. Multi-functionality of Peres Gate is shown in Table 1.7. Peres Gate can work as a Half Adder unit.

Table 1.7 Multifunctional PG

S.No.	A	B	C	P	Q	R	Logic Functions
1	0	B	C	0	B	C	PASS LOGIC
2	1	B	C	1	$\overline{B}$	B⊕ C	NOT / XOR
3	A	0	C	A	0	C	PASS LOGIC
4	A	1	C	A	$\overline{A}$	A ⊕ C	NOT / XOR
5	A	B	0	A	A ⊕ B	AB	HALF ADDER
6	A	B	1	A	A ⊕ B	$\overline{AB}$	XOR / NAND

Logical reversibility of PG is shown in Fig.1.9; this proves bijective nature of inputs and outputs.

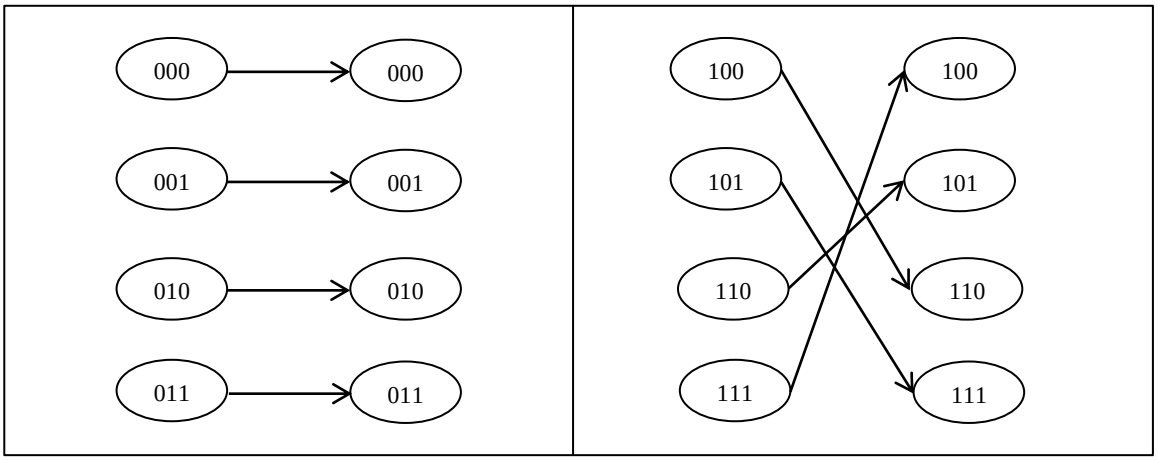


Fig. 1.9 Logical Reversibility of PG

1.8.2.4 Fredkin Gate

It is also called C SWAP gate. It swaps the last two bits if the 1st bit is 1, otherwise it will pass the value as same.

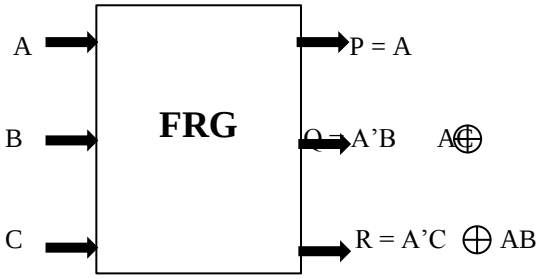


Fig. 1.10 Fredkin Gate

The block diagram of Fredkin Gate is shown in Fig. 1.10, the outputs P follows input A, Q and R performs the required logic operation. The truth table of Fedkin Gate is shown in Table 1.8; all the outputs are in correct order according to the logic equations.

Table 1.8 Truth Table of FRG

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Here A,B and C are the inputs and P,Q and R are outputs. Table 1.8 shows the entire possible outcome for different eight input patterns.

Table 1.9 Multifunctional FRG

S.No.	A	B	C	P	Q	R	Logic Functions
1	0	B	C	0	B	C	PASS LOGIC
2	1	B	C	1	C	B	PASS LOGIC
3	A	0	C	A	AC	A' C	AND
4	A	1	C	A	A'	A+C	NOT / OR
5	A	B	0	A	$A \oplus B$	AB	HALF ADDER
6	A	B	1	A	$A \oplus B$	$\overline{AB}$	XOR / NAND

Multi-functionality of Peres Gate is shown in Table 1.9, FRG gate as a single body can serve as a half adder. Logical reversibility of FRG is also shown in Fig. 1.11; this proves the unique one to one mapping among inputs and outputs.

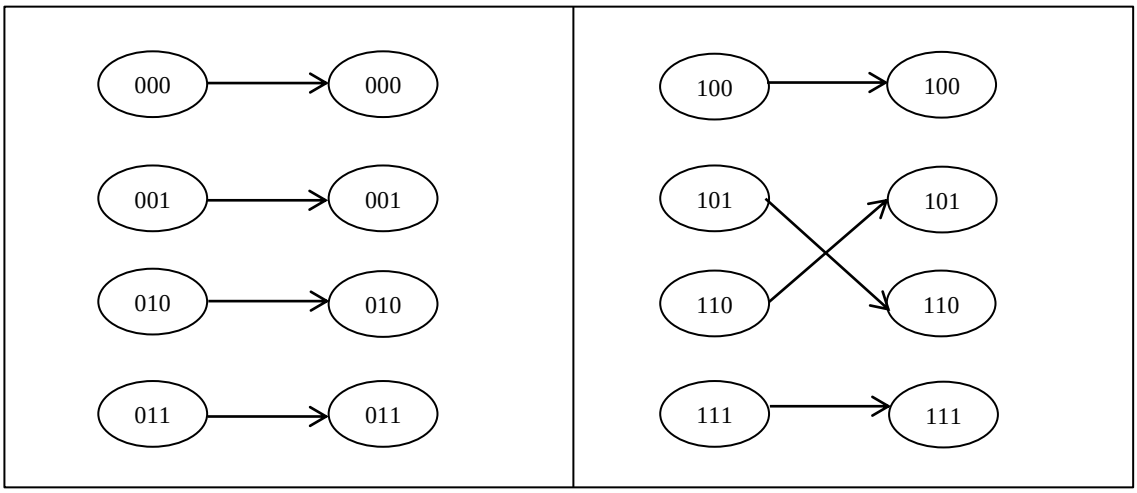


Fig. 1.11 Logical Reversibility of FRG

1.8.2.5 Other Reversible Gates

In the literature many reversible gates are proposed of three inputs and four inputs. Some of them are drawn below.

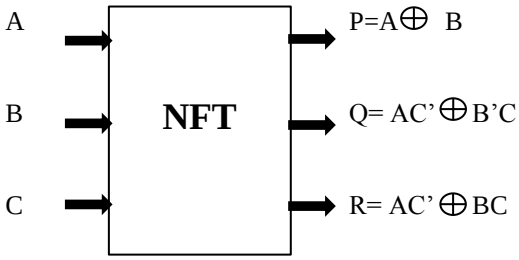


Fig. 1.12 NFT Gate

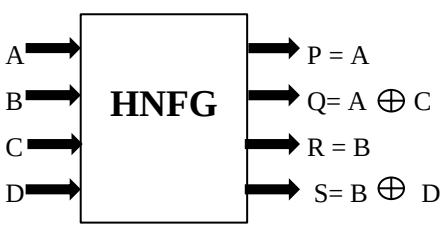


Fig. 1.13 HNFG Gate

CHAPTER 2. LITERATURE REVIEW

About 30 years back the concept of Reversible Logic came into picture. These logics are necessity of new era, as there is a restriction to Moore's law also, therefore technology has to think beyond this limitation and the solution is Reversible computing and Quantum Computing. This field grabbed the attention of researchers in mid 90's but this process is speeded up from 2000. A brief description about the techniques and present work are summarized to provide a crisp idea about the field.

Sarah T. Yanchan et.al.(2013) proposed a 4-bit ripple carry adder. This is designed by combining two different types of adders such as conventional ripple carry adder and carry look ahead adder. Basic principles of QCA and QCA based designs are illustrated. This proposed design uses five inputs majority voter [34].

Kim A. et.al. (2013) proposed a novel complex parallel prefix adder using Quantum-dot Cellular Automata. Further the proposed design is extended to construct 4-bit parallel prefix adder, this proposed design is compared with existing design in literature [37].

Thapliyal H. et.al.(2012) proposed a novel reversible sequential circuit which is absolutely testable for any kind of stuck-at-faults . These faults can be detected by applying two test patterns. Design of reversible edge triggered D flip flop is presented. Complete 100% fault coverage in QCA implementation of FRG is shown. A novel multiplexer conservative QCA gate is proposed. This proposed multiplexer based gate outperforms the existing gates in terms of testability. The proposed work has one loop hole that it can not detect multiple stuck-at-faults [15].

Navi K. et. al.(2012) put forward a novel seven input majority gate for QCA which performs better in terms of cell count, latency and complexity compared to existing majority voters. Moreover using this novel majority voter gate, four input OR & AND gates can be constructed in only two clock phases [22].

Thapliyal H. et.al.(2011) presented a novel reversible TR gate. This TR gate can serve as reversible half subtractor circuit. The proposed gate is designed using elementary quantum gates also, the quantum cost and delay is found to be four. This novel design outperforms the

existing reversible subtractors. Reversible full subtractor is also designed using novel TR gate with quantum cost of six. [16].

Sultana S. et.al. (2011) presented a reversible full adder and subtractor RCAS module with Peres gate and Feynman Gate in an effective way for 2's complement computation. Moreover an approach is proposed to detect overflow in 2's complement computation. But due to overflow detection ,quantum cost is increased by two because of addition of two CNOT gates[17].

Akeela R. et.al. (2011) postulated a novel building block for QCA design. A novel five input majority gate (MAJ_5) is proposed. Authors demonstrated its use in a bit-serial adder. The design of serial adder uses a smaller number of gates, wires and wire crossings. The authors presented a modified MAJ_5 gate with a greater fault tolerance. This gate can be easily interfaced with other gates in larger design [20].

Karthigai L. et.al.(2010) proposed a different subtractor designs based on QCA.Half and full subtractors are designed and simulated. This design can be implemented in various arithmetic logical applications in an efficient manner. The designed ALU using this new subtractor can be further utilized in nano processor[21].

Navi K. et.al.(2010) put forward a novel five input majority voter which reduces cell counts, area and uses conventional form of QCA cells. A novel full adder subtractor is designed using new five majority voter. This full adder requires two majority gates and two inverters which are constructed using diagonal cells [23].

K. Das et.al.(2009) stated that the logic and circuits in QCA are not measured with voltage level but measured by electron's polarity in cell. In this paper a new nano-structure of AOI with reduced area & efficient design is proposed. This design is constructed using Nand Nor Inverter and Majority Voter[35].

H. Cho et.al.(2009) demonstrated a design trade-off scheme in QCA which is dissimilar to traditional design methodology. Adder designs based on conventional design methodology are inspected in QCA technology. A new design for carry flow adder and serial parallel multiplier are proposed. This serial parallel multiplier is simulated for different operand sizes [36].

George I. et.al.(2007) discussed about five new research fields beyond CMOS. These novel & emerging fields are quantum physics, material science, condensed matter and nano-magnets. The most focusing field at present is single electron in quantum-dot[31].

H.Cho et.al.(2007) described the significance of QCA & its features like faster speed, smaller size & lower power consumption. The fundamental devices for QCA are wires, gates and memories. This paper proposes QCA design for ripple carry adder, carry look ahead adder and conditional sum adders[28].

J. Huang et.al.(2007) designed sequential circuits using QCA. This analysis involves fillip-flops and a new RS flip-flop is proposed and a novel algorithm is also proposed which assigns proper clocking zones to a sequential circuit[30].

G.H. Bernstein et.al.(2005) postulated about features of QCA like high density, high speed & low power computing. Magnetic interactions between nano-magnets can take place at room temperature. Authors predicted that, size of quantum dots play an important role in coupling[29].

Steven C. et.al.(2004) proposed a methodology of incorporating CMOS technology in developing QCA circuits. Using this approach QCA circuits can be developed and verified before they are realized at atomic or molecular level. A brief description of layout designing & simulation of QCA devices is presented. VHSIC models are developed to verify QCA circuits before the simulation at atomic level takes place [33].

Walus K. et.al.(2004) presented a novel design and simulation tool for Quantum-dot Cellular Automata. The tool is QCADesigner which works atomic level. A rapid and efficient tool was required for the adequate and proper simulation and design of QCA circuits. It should be noted that this tool is in its infancy, great efforts have to be put to enhance this further [24].

R. Zhang et.al.(2004) proposed a novel algorithm to reduce majority input gate counts required for processing three-variable Boolean function. This algorithm converts Sum-of-Product expression to majority logic. Further thirteen standard functions are introduced. By using this novel approach hardware requirements can be decreased [27].

Islam Md. R. et.al.(2003): introduced a novel approach to synthesis multi-rail reversible cascades structures with minimal garbage bits and reversible gates. A full adder constructed by three gates and two garbage outputs is proposed. This novel design minimizes critical path and avoids fan out [25].

M. Macucci et.al.(2003) investigated the behavior of QCA in Silicon-on-Insulator technology. The interaction between the upper & lower double dots is observed. The proposed & modified layout can be operated above 0.3 K temperature [32].

Wei Wang et.al.(2003) proposed a novel design of adder using Quantum-dot cellular automata, which requires only two inverters and three majority gates. The new algorithm reduces hardware requirement by 30 % of the existing design with same speed and clocking performance [26].

CHAPTER 3. DESIGN METHODOLOGY

Since the evolution of on chip integration, many designing techniques have been proposed till now. As the need of speed, performance is growing; more emphasis is given on fastest speed device. Moreover if speed is concerned then designer needs to focus on power dissipation as well, because if a device contributes in high heat dissipation then the device life span will be very less, which will not be considered as a optimum design. Therefore an engineer needs to maintain a balance between power and delay so that optimum PDP can be observed. The other way around the more promising field which a designer has to look after is area, as now a days every device is scaled down to get portable device, this is surely going to shrink space but the drawback of more power dissipation will be introduced. Consequently there would be a trade off always among power, delay and area. A designer needs to optimize each field to achieve optimal design. Below some of the widely, effectively used and novel emerging techniques are briefly explained.

3.1 CMOS

Metal oxide semiconductor field effect transistor (MOSFET) is a three terminal basic device same as bipolar junction transistor (BJT) having source, drain and gate. Moreover body of substrate is also considered as terminal in this. In PMOS the body is connected to VDD and in NMOS it is connected to GND for providing biasing to it. This working of MOSFET is same as FET. However MOSFET has much lower capacitance and much higher input impedance than FET. Complementary metal oxide semiconductor (CMOS) is a device in which both P-channel and N-channel MOSFETs are connected in push pull arrangements. It has the property of both the MOSFETs. The composition of PMOS transistor offers low resistance between its source and drain contacts when a low voltage signal is applied and offers high resistance when a high voltage signal applied at gate terminal. Other way around NMOS offers high resistance when a low voltage signal is applied and vice versa. We can design any circuit by deducing its Boolean function through CMOS technique. Complement of any function is designed using this.

3.2 Quantum Dot Cellular Automata

In contrast to electronics based on transistors, QCA does not work on the transport of electrons, but by the arrangement of electrons in a small limited area of only a few square nanometers. It is implemented by quadratic cells, therefore it is called QCA. Structure of basic QCA cell is shown in Fig. 3.1 in this small square precisely four potential wells are located; one well is

situated in each corner of QCA cell. The cell substrate can be constructed using semiconductors according to application. Electron Tunnel Junction is responsible for switching of electron from one potential well to another. In individual QCA cell exactly two electrons are sealed. These two electrons can only reside in the potential well.

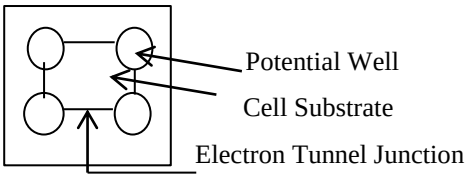


Fig. 3.1 Structure of QCA Cell

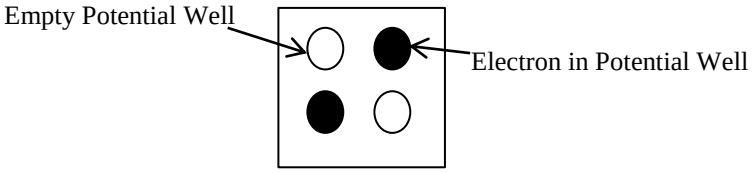
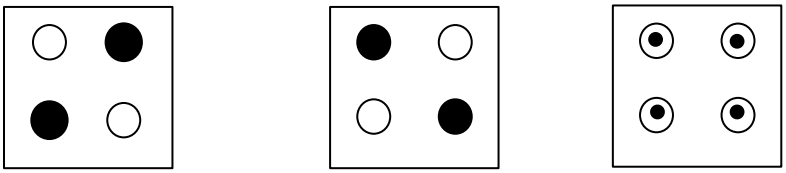


Fig. 3.2 Electrons in potential well

Fig. 3.2 shows a general arrangement of electrons in single QCA cell. There are two diagonals in a square, which means the electrons can dwell in exactly two possible variations in the QCA cell.



(a) Binary 1 (b) Binary 0 (c) Null Polarized

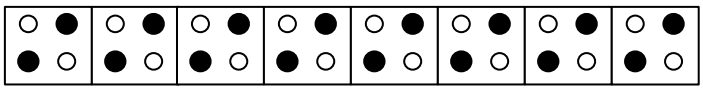
Fig. 3.3 Polarization in QCA Cell

It means each cell can be in two states. More precisely a high voltage is often interpreted as binary '1' and a low voltage as binary '0' shown in Fig. 3.3 (a) and 3.3 (b). Fig. 3.3 (c) shows a null polarized QCA cell which corresponds to no fixed polarization, according to input signal it will change its polarization.

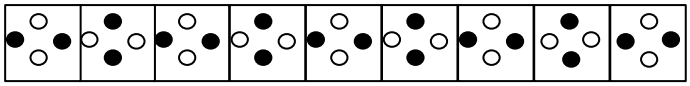
3.3.1 Information Flow in QCA

If two QCA cells are placed near to each other then it is possible to interchange their states, The QCA cell that has to transfer its state to a neighboring cell must have its tunnel junctions locked, and the tunnel junctions in the neighboring cell have to be exposed, to allow the electrons to travel through the tunnel junctions between the potential wells. As soon as they expose, the electrons in the neighboring cell are pushed by the Coulomb force of the previous cell as far away as possible. As they also are pushed away from each other, they will go into the

same potential wells as in the previous cell. As soon as the tunnel junctions are locked again, the transfer of the state is terminated [11].Binary information flows through QCA wire which can be designed in two ways such as 45˙ QCA wire and 90˙QCA wire are shown in Fig. 3.4



(a) 90˙ QCA Wire



(b) 45˙ QCA Wire

Fig. 3.4 QCA Wires

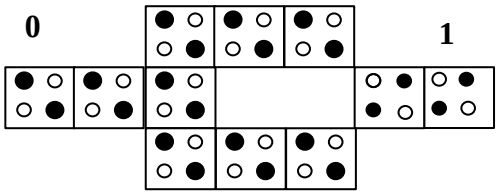
In 45˙ wire, the information propagation is altered at each cell, means the each successive cell inverts the incoming signal. Therefore if we want to propagate the original signal through 45˙ QCA wire, then we need to place odd number of QCA cells. This wire is useful when we need to make cross wire connections. But in 90˙ wire the same information is flown through out the wire.

3.3.2 Elementary QCA Gates

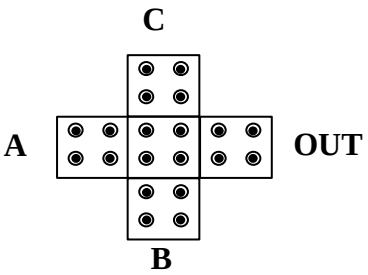
So far, we know how to decode and transfer information with QCA cells, but yet we deficit the possibility for computations. For QCA cells, the elementary gates are QCA inverter, three-input majority voter, five input majority voter and seven input majority voter. Following figure 3.5 shows all the basic QCA elementary gates. An inverter can be designed in QCA like shown in Fig.3.5 (a), this arrangement of cells result in highest polarization. Suppose '-1' polarization is applied to the input, then before reaching to the second last cell, due to electrostatic repulsion the position of electrons get changed, therefore we get inverted signal at the output.

Three input majority voter shown in Fig. 3.5(b), it takes three inputs A,B & C, and depending on the majority input voters the, output will take that value. Suppose, signal A and B have '+1' polarization but C has '-1' polarization, so according to majority voter condition '+1' will be transferred to the output Y.

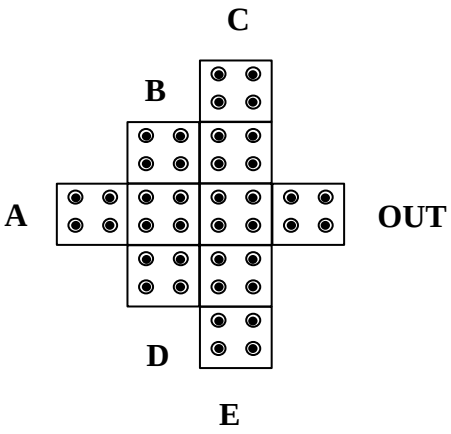
Similar working can be understood for five input majority voter and seven input majority voter shown in Fig. 3.5 (c) and Fig. 3.5 (d) respectively. The only difference is of number of inputs in majority voter, like five input majority voter consists of five inputs and seven input majority voter takes seven inputs.



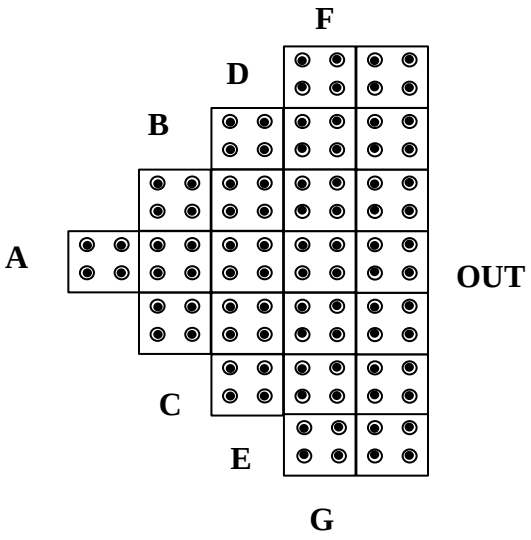
(a) QCA Inverter



(b) Three Input Majority Voter



(c) Five Input Majority Voter



(d) Seven Input Majority Voter

Fig. 3.5 QCA Gates (a) QCA Inverter (b) Three Input Majority Voter (c) Five Input Majority Voter (d) Seven Input Majority Voter

By using these majority gates one can deduce any logic function like AND, OR, XOR etc. just by polarizing any cell to a fixed value.

3.3.3 Clocking Scheme

As we know that Quantum -Dot Cellular Automata implementation does not require any power signal for its operation, all it needs is just proper clocking scheme. There are four different clocking zones, named as clock 0, clock 1, clock 2, clock 3 having different colors. The proper arrangement of these clocking is only responsible for exact results. Each clock signal is phase shifted by 90˙. Four clock signals are adequate to control the propagation of information in a QCA circuit [13][14].

These clocks synchronize as well as control the information propagation. These are the sources of power in QCA circuits. By using four phase clocking arrangement; QCA manages and propagates the information within the cells in a prescribed timing format. QCA cells are organized in a group having particular clock zone so that all the cells have same affecting field.

Each clock zone has four phases named as switch, hold, release and relax. These four phases play a significant role in information propagation.

- **Switch:** In this phase the electrons are affected by neighboring columbic charges as in this tunneling barrier is increased.
- **Hold:** In this the state achieved by electrons are not changed and tunneling hindrance is very high.
- **Release:** In this phase tunneling hindrance is started to slow down and cells are tied to their hold states.
- **Relax:** In this phase tunneling barrier is null and cells are free to acquire new values.

The following Fig. 3.6 shows the clocking scheme and Fig. 3.7 shows four different phases of each QCA clock.

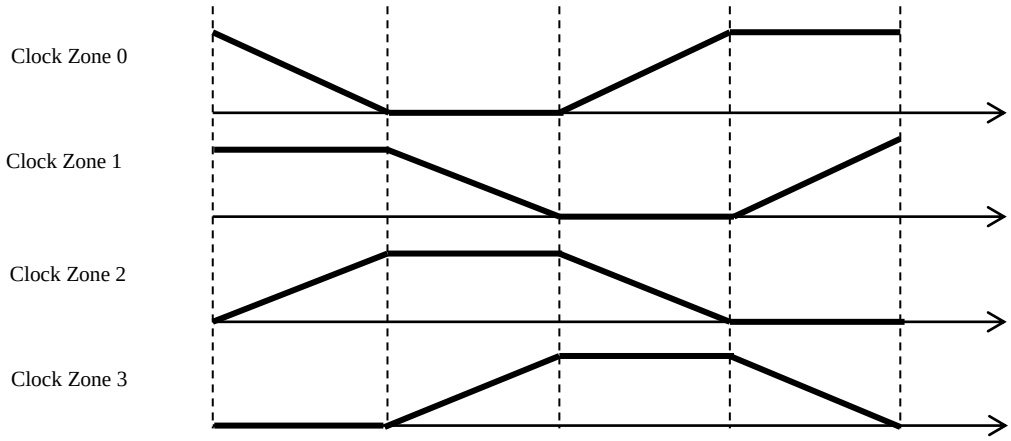


Fig. 3.6 Clocking Scheme in QCA

The four phase of a clock in shown below in Fig. 3.8, this is very significant feature of QCA clocking, according to this we need to place QCA cells so that proper flow of information is possible. In QCA when circuit becomes more complex, delay of the circuit may enhance because of more QCA cells and wire connections. Therefore it is very much important to group cells for each clock cycle for better propagation of information [36].

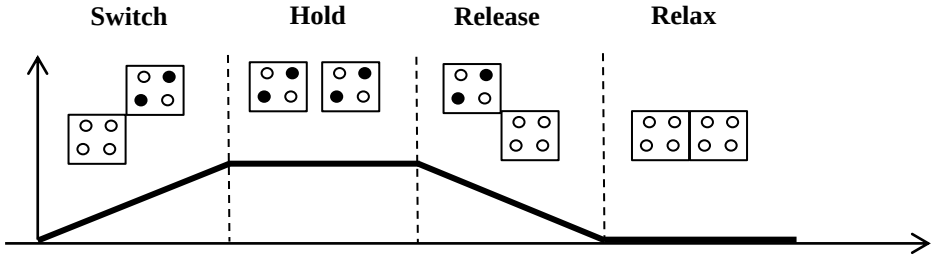


Fig. 3.7 Phase Description of a QCA Clock

It is mandatory to have proper clocking scheme, otherwise accurate results can not be achieved. These clocking scheme is responsible for design of QCA , this makes QCA distinctive from CMOS circuits [21][27-29].

CHAPTER 4. DESIGN & ANALYSIS

According to design flow rules we need tools for synthesis and simulation of design to verify the functionality of the design. Here, reversible circuits are designed and simulated using two different simulation tools. 1. Cadence, 2. QCADesigner 2.0.3.The brief description of each tool is explained below.

4.1 Simulation Environment

Design and simulation of reversible circuit is performed on two tools, entirely different from one another. As a performance analysis is to be done between existing CMOS technology and forecasting QCA technology, therefore same circuits are designed on two tools and performance is measured in terms of area.

4.1.1 Cadence Design System

It is an American EDA software and engineering company established in 1988.The company produces software for designing chips, system on chips (SOC) and printed circuit boards (PCB).As the circuits are more composite Cadence's approach is to meet designer's confronts and to support them in application driven approach. Following are the list of different products of Cadence:

- **Virtuoso Platform**: This includes schematic entry, circuit simulation, custom layout, physical verification and extraction etc.
- **Encounter Platform:** This includes tools for creating digital integrated circuits. In this design starts with Verilog net lists. this includes floor planning, placing and routing etc.

4.1.2 QCADesigner 2.0.3

It is a novel tool for Quantum-dot Cellular Automata. It is basically a layout designer tool in which layouts are drawn and simulated. Initially this tool was developed at ATIPS Laboratory, University of Calgary. The tool is written in C/C++ language. The main idea behind the working of QCA is the signal clocking [12]. There is a phase shift of 90 degree in each clock cycle, this is responsible for the appropriate signal propagation through QCA cells. The information is flown through each cell but not reserved, because each cell deletes its state after every clock cycle.

4.2 Design

Fundamental reversible gates are designed and simulated using CMOS technology on Cadence Virtuoso platform, QCA technology on QCADesigner 2.0.2. Each reversible gate is transformed into its equivalent Quantum cost using Quantum gate Implementation.

4.2.1 CMOS Implementation

Basic arithmetic gates AND, XOR used in reversible circuit designs using different techniques like Gate Diffusion Input, Pass Transistor Logic and Multiplexer are designed. Depending on transistor count, power dissipation and delay Pass transistor Logic is opted for designing XOR, AND gates as basic cell for reversible gate implementation in CMOS Technology. The schematics are shown in Fig. 4.1 and 4.2 below.

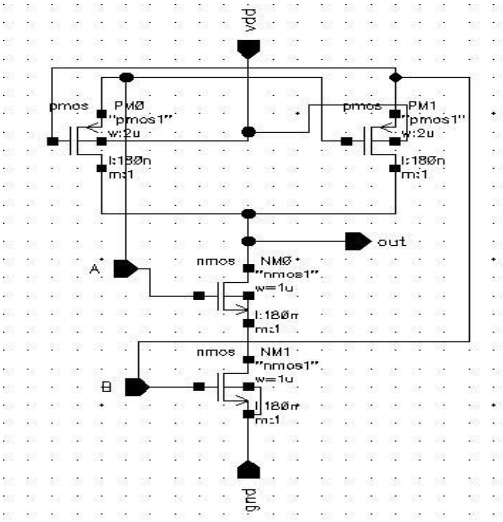


Fig. 4.1 Schematic of XOR Gate

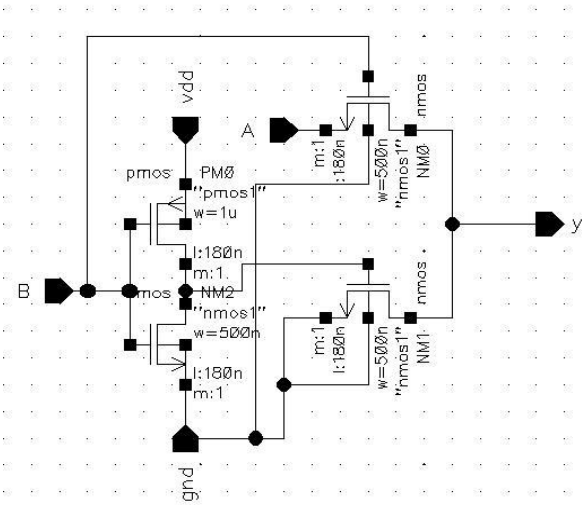
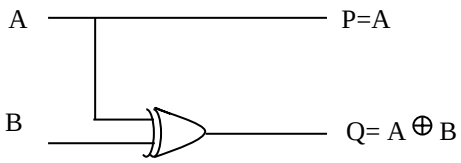


Fig. 4.2 Schematic of AND Gate

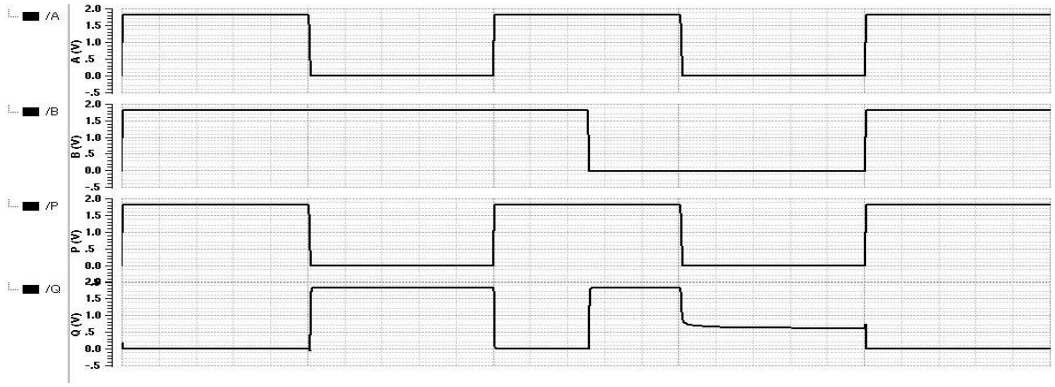
XOR gate is designed using four transistors, two nmos and two pmos. Futher AND gate is designed using four transistors, three nmos and one pmos. This section is subdivided into parts to show the implementation of each reversible gate using CMOS technology incorporating circuit diagram, output results and layouts.

4.2.1.1 Feynman Gate

It has a two inputs and two outputs. The circuit diagram of FG is shown in Fig. 4.3 (a).



(a) Circuit Diagram



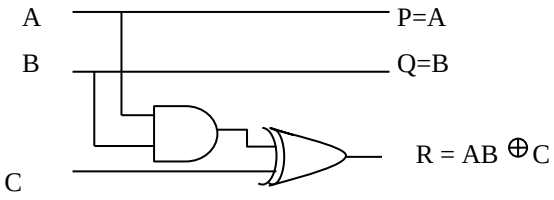
(b) Waveform

Fig. 4.3 Feynman Gate (a) Circuit Diagram (b) Waveform using CMOS Technology

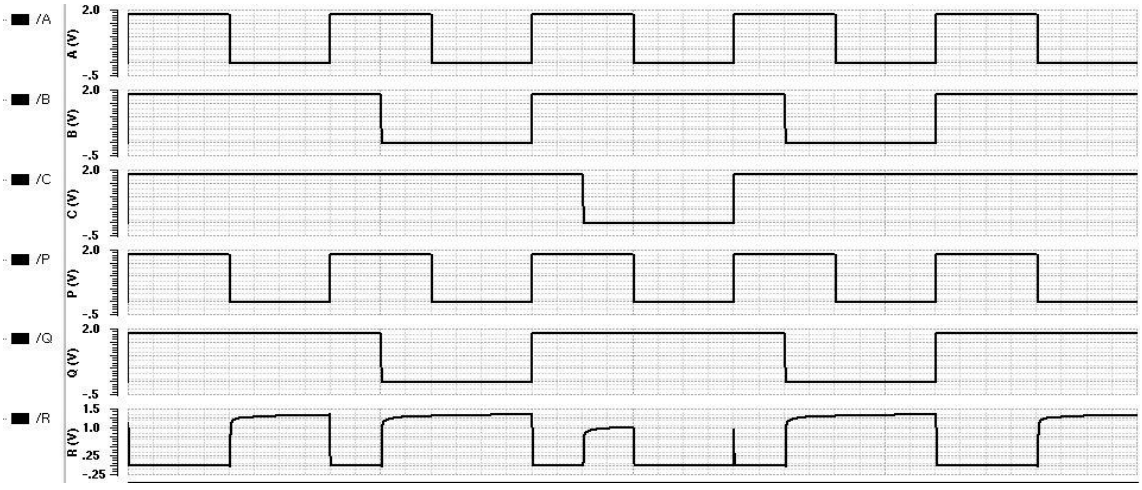
The output waveform is shown in Fig. 4.3 (b), output P follows input A, output Q performs XOR operation.

4.2.1.2 Toffoli Gate

It is a three input, three output gate. Output P,Q follow input A & B respectively. Output R takes A.B and C as input and performs XOR operation on both of them. The circuit diagram is shown in Fig. 4.4 (a).



(a) Circuit Diagram



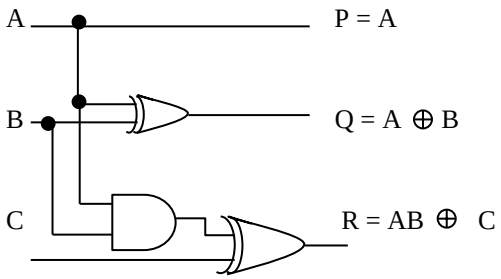
(b) Waveform

Fig. 4.4 Toffoli Gate using CMOS Technology

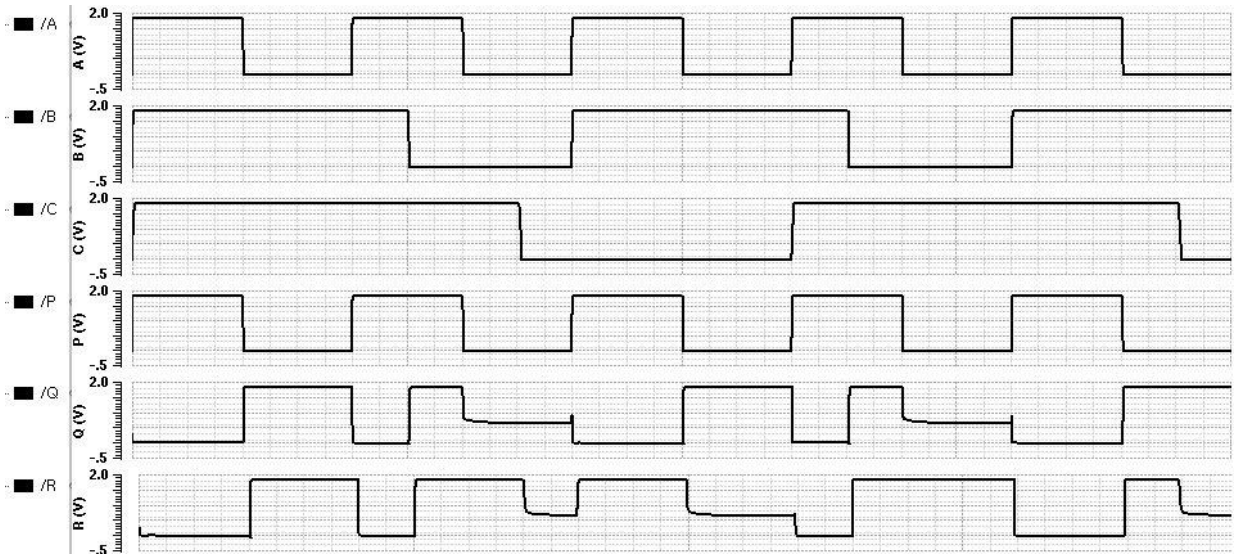
The waveform result of TG is shown in Fig. 4.4 (b), Outputs are following required logic functions.

4.2.1.3 Peres Gate

It is a 3 x 3 reversible gate. Output P follow input A ,Q performs XOR operation & R executes required logic function. The circuit diagram is shown in Fig. 4.5 (a).



(a) Circuit Diagram



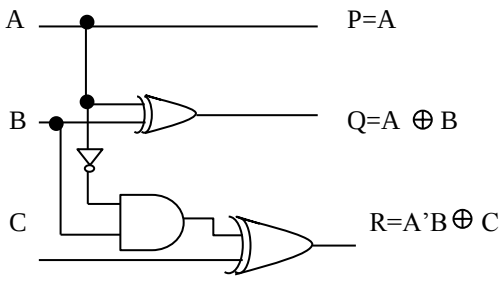
(b) Waveform

Fig. 4.5 Peres Gate (a) Circuit Diagram (b) Waveform using CMOS Technology

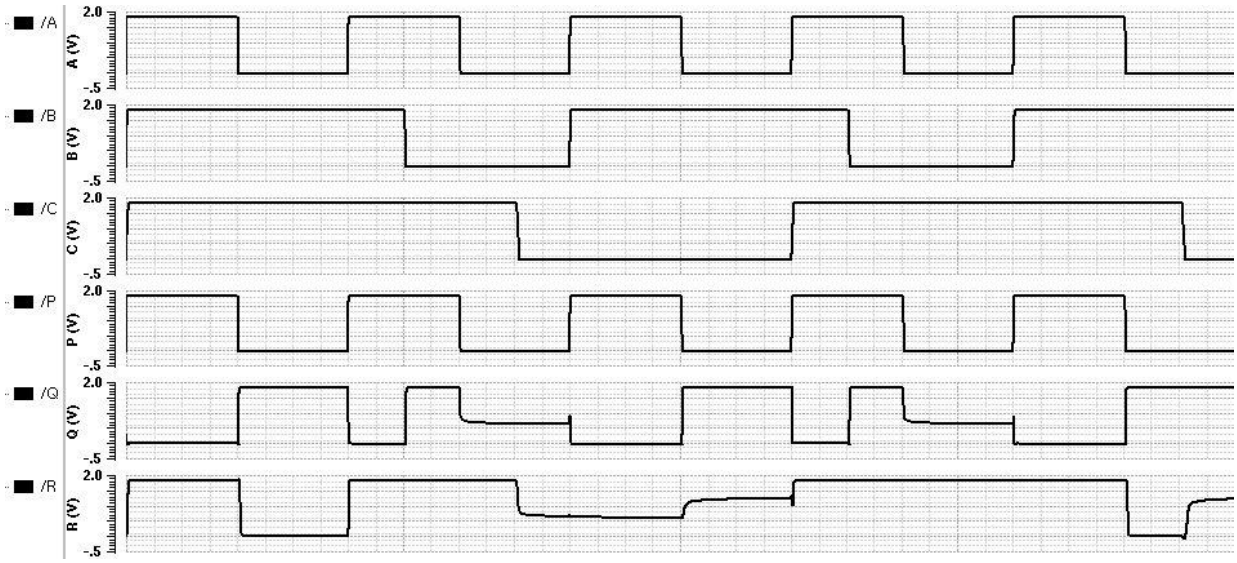
The waveform result of PG is shown in Fig. 4.5 (b), Outputs are following required logic functions.

4.2.1.4 TR Gate

It is a 3 x 3 reversible gate.It is mainly used for reversible subtraction operation.The circuit diagram is shown in Fig. 4.6 (a). The waveform result of TR is shown in Fig. 4.6 (b),



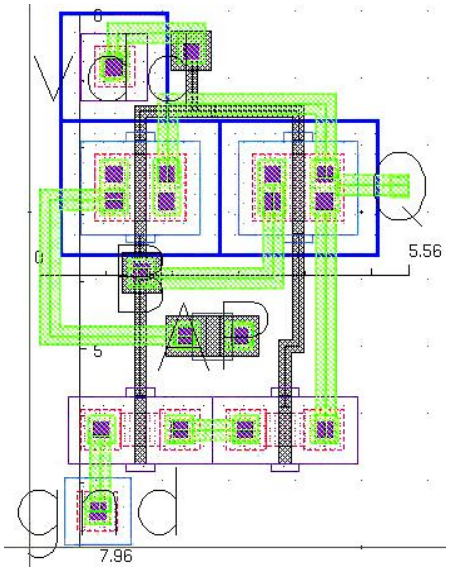
(a) Circuit Diagram



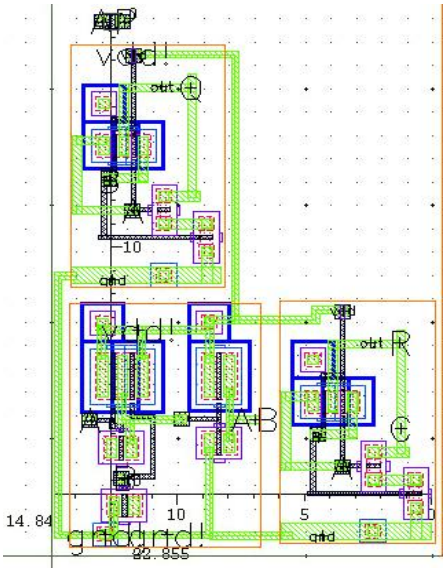
(b) Waveform

Fig. 4.6 TR Gate using CMOS Technology (a) Circuit Diagram (b) Waveform

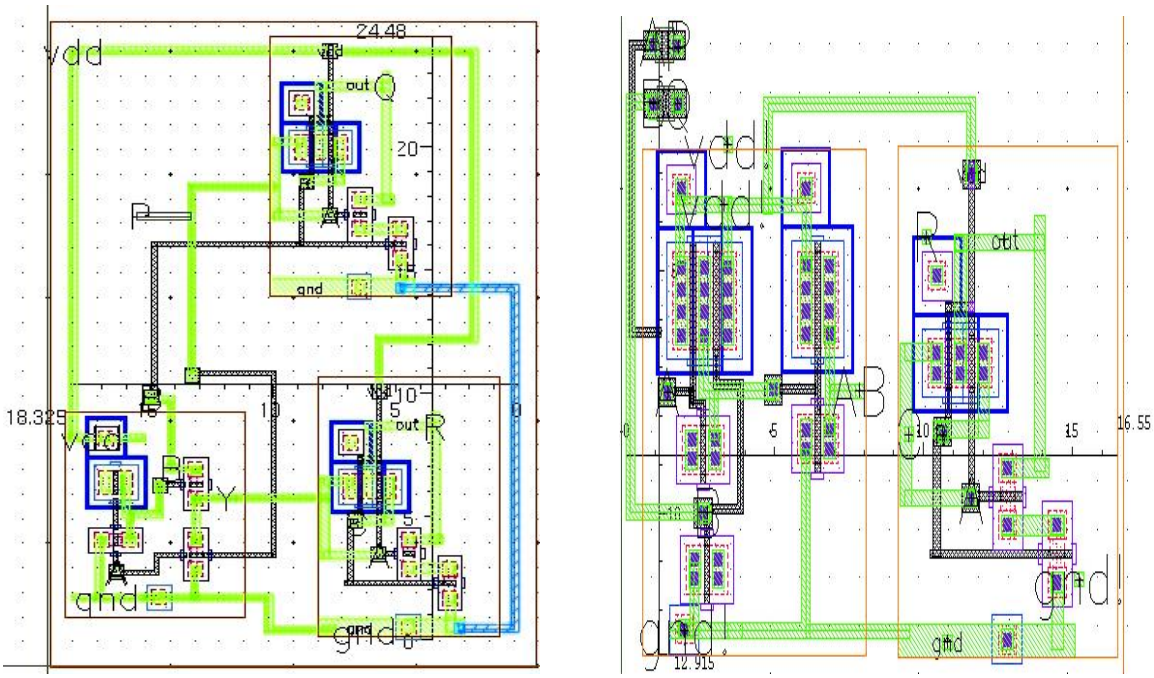
The layouts are shown below in Fig. 4.7 using CMOS technology, these layouts are generated through schematics.



(a) FG



(b) PG

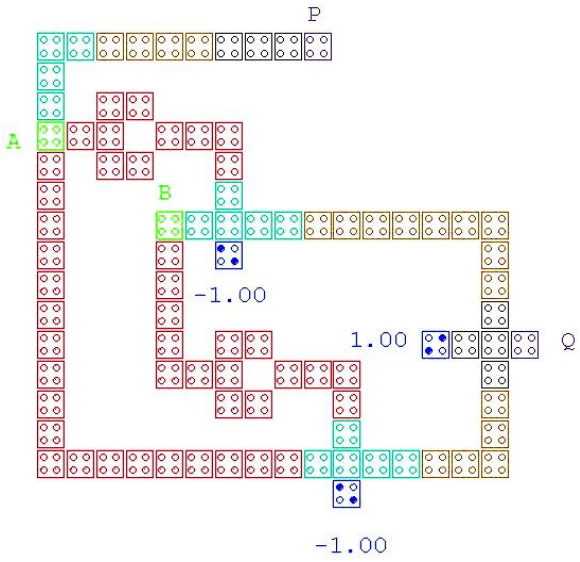


(c) TR Gate (d) TG

Fig. 4.7 Layouts using CMOS Technology (a)FG (b) PG (c) TR Gate (d) TG

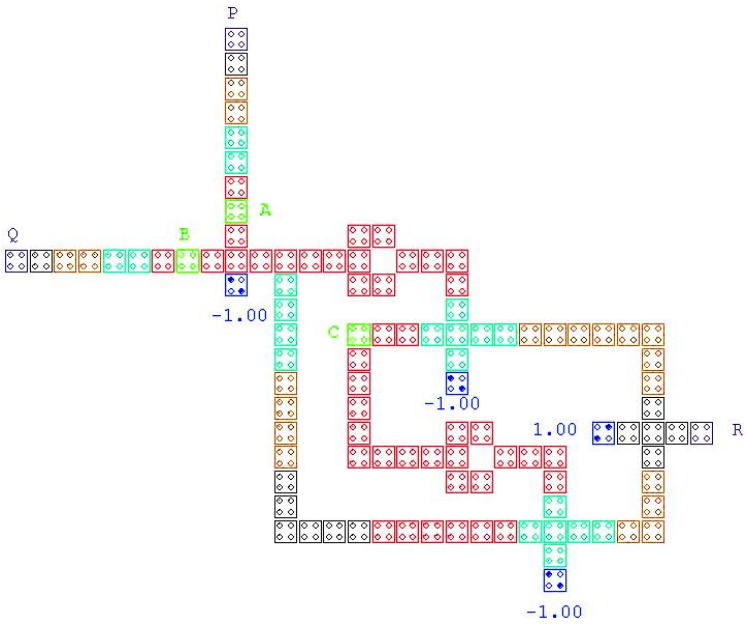
4.2.2 QCA Implementation

All fundamental reversible gates are again designed using Quantum- Dot Cellular Automata. The waveforms and layouts are presented below in Fig. 4.8.



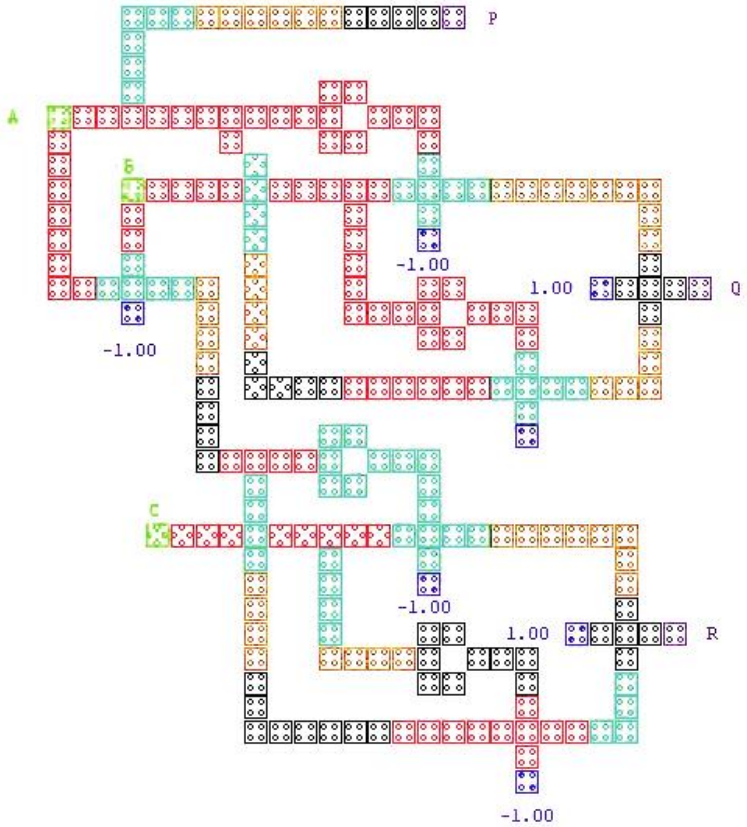
(a) Feynman Gate

The layout of Feynman Gate using QCA is shown in Fig. 4.8 (a) , FG is constructed using two inverters and three input majority voters.



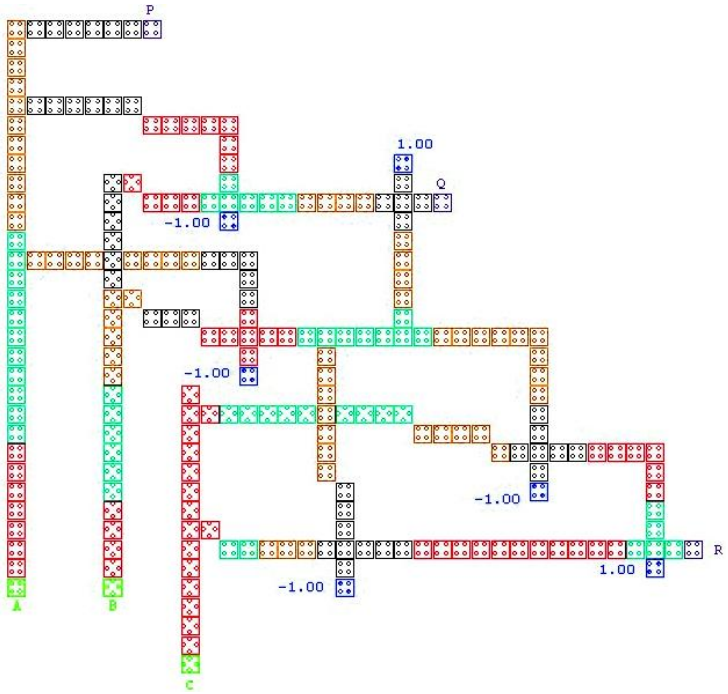
(b) Toffoli Gate

Layout of Toffoli Gate using QCA is drawn in Fig. 4.8 (b), it is constructed using four majority input voters and two inverters.



(c) Peres Gate

The layout of PG is shown in Fig. 4.8 (c), it is constructed using 7 majority input voters and four inverters.



(d) TR Gate

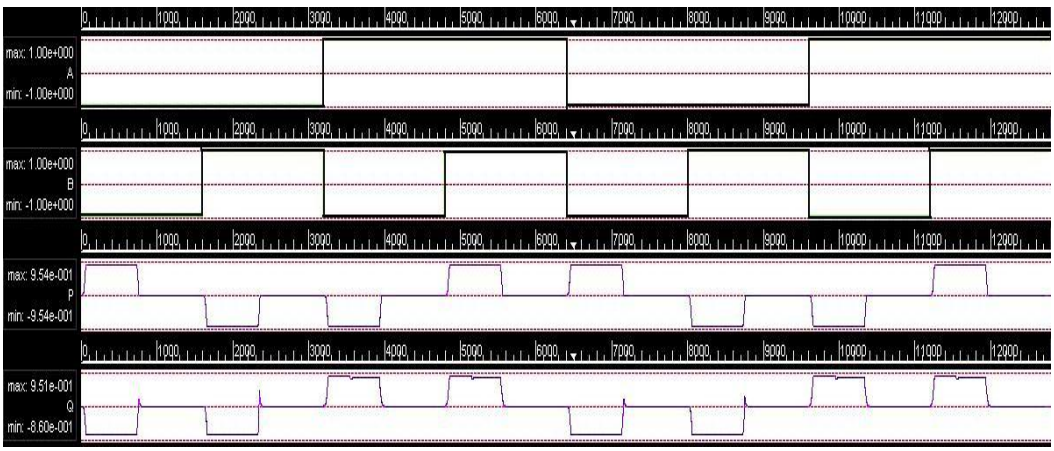
Fig. 4.8 Layouts of Reversible Gates using QCA

The clocking zones are described as follows:

- Pink : Clock Zone 0
- Blue : Clock Zone 1
- Brown: Clock Zone 2
- Black : Clock Zone 3

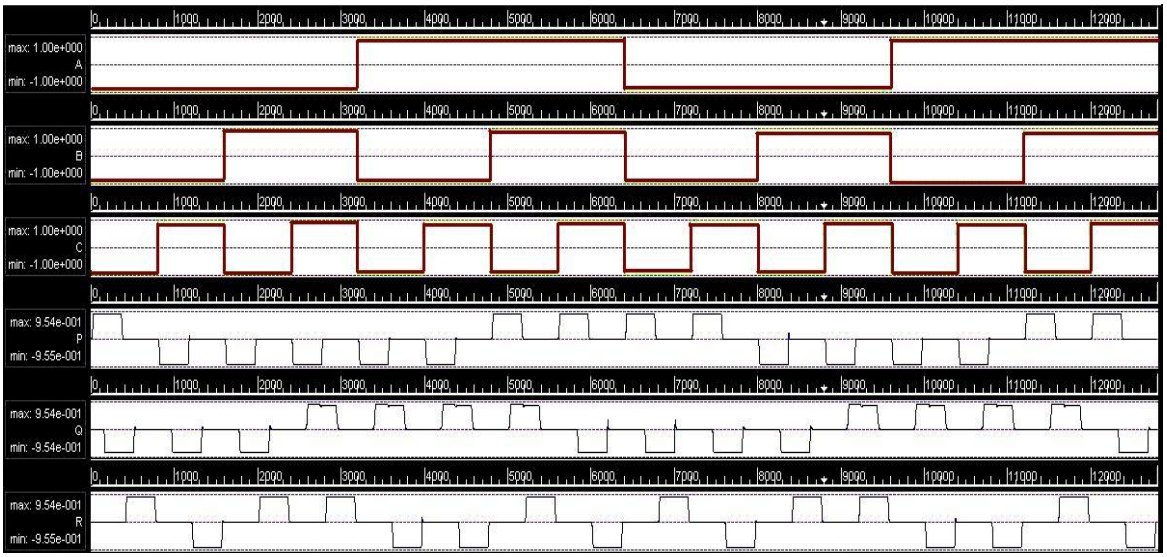
The layouts are drawn with a cell height & width of 18nm, Clock amplitude factor is 2, spacing between two cells is 2nm. All the layouts are drawn using a single layered structure. The crossovers in the layouts are made using 45 degree QCA wire.

The simulation results of QCA implementations are shown below in Fig. 4.9.

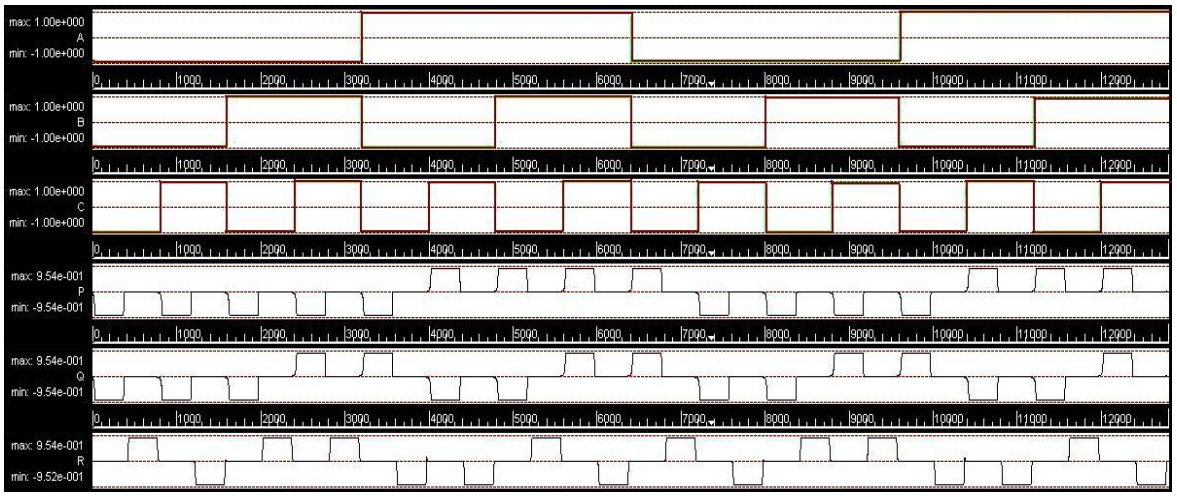


(a) Feynman Gate

(b) Toffoli Gate



(c) Peres Gate

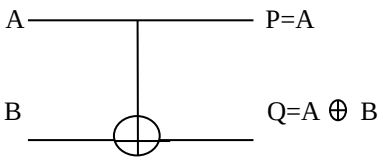


(d) TR Gate

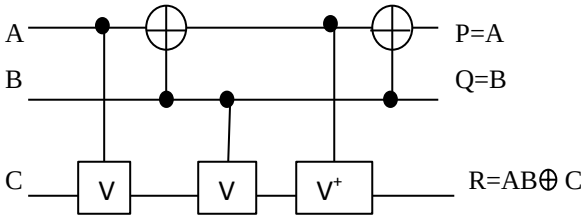
Fig. 4.9 Output Waveforms Using QCA

4.2.3 Quantum Gate Representation

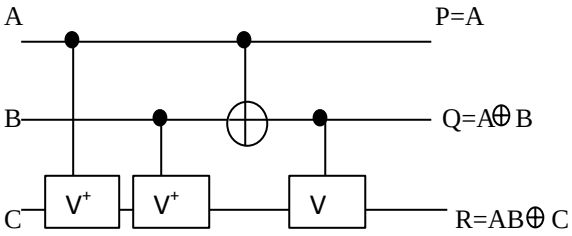
In this section, reversible gates are designed using elementary quantum gates in Fig. 4.10. As it is known that reversible circuit can only be used in quantum computers when they are made up of elementary quantum gates. Therefore it is very much necessary to represent reversible circuit into its quantum cost representation.



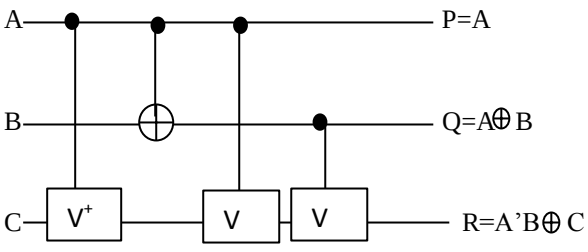
(a) Feynman Gate



(b) Toffoli Gate



(c) Peres Gate



(d) TR Gate

Fig. 4.10 Quantum Gate Representation of Reversible Gates

Fig. 4.10 (a) works as a controlled NOT gate, as already explained earlier. Quantum gate implementation of Toffoli Gate is shown in Fig. 4.10 (b), consider 110 input pattern, as the control pin of first V gate is high, it will invert C bit, both V and V^+ gates are in series and having control pin high , means will pass the C as it is. Hence we will get P=1, Q=0 and R=1 for input pattern 110.

4.3 Proposed Design

All the existing reversible gates work on a single operation like either these can be used as a reversible adder or reversible subtractor. But there is no circuit which could be used as both adder and subtractor. Here a novel reversible RSG Gate is proposed which can perform both the operations simultaneously. This novel circuit does not use any control pin for selecting addition or subtraction operation. The block diagram of this novel gate is presented below in Fig. 4.11. It is a 3x3 gate having A,B & C as inputs and P,Q & R as outputs.

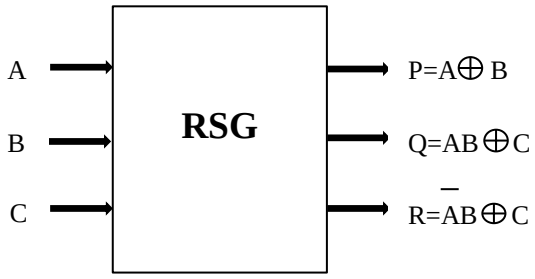


Fig. 4.11 Proposed RSG Gate

Table 4.1 shows the truth table of RSG gate. It shows correct results, according to equations of circuit. There are total eight input patterns and each pattern results in different and unique output pattern.

Table 4.1 Truth Table of RSG

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	0	1
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	0	1	0
1	1	1	0	0	1

Table 4.2 Multifunctional RSG

S.No.	A	B	C	P	Q	R	Logic Functions
1	0	B	C	B	C	$B \oplus C$	PASS LOGIC / XOR
2	1	B	C	B’	$B \oplus C$	C	NOT / XOR
3	A	0	C	A	C	C	PASS LOGIC
4	A	1	C	A’	$A \oplus C$	$\overline{A \oplus C}$	XOR / XNOR
5	A	B	0	$A \oplus B$	AB	A’ B	HALF ADDER & SUBTRACTOR
6	A	B	1	$A \oplus B$	$\overline{AB}$	B	XOR / NAND

Table 4.2 shows the multi-functionality of proposed RSG gate. This gate can perform as reversible half adder and reversible half subtractor simultaneously.

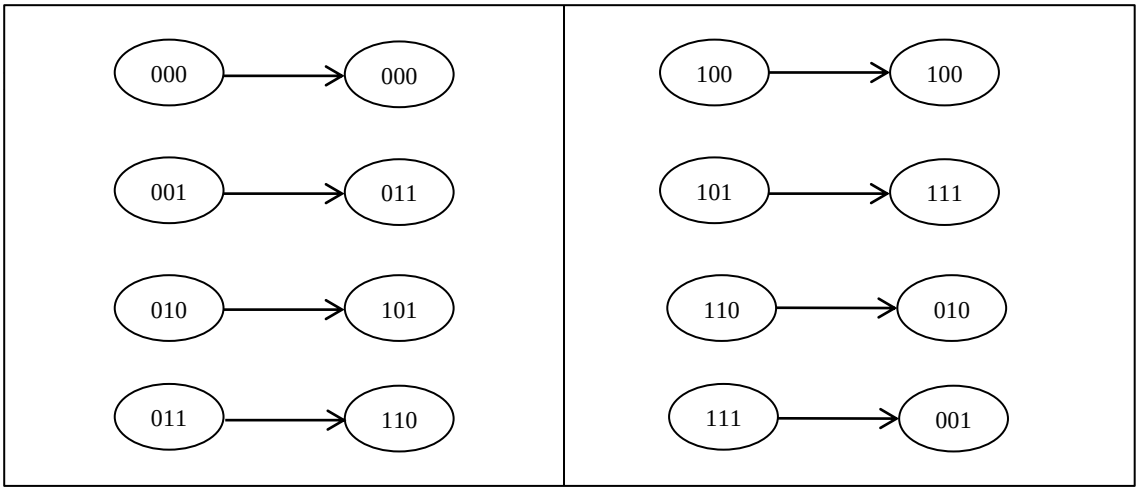


Fig. 4.12 Logical Reversibility of Proposed RSG Gate

The logical reversibility of RSG gate is proved in Fig. 4.12, this proves the unique one to one mapping among inputs and outputs.

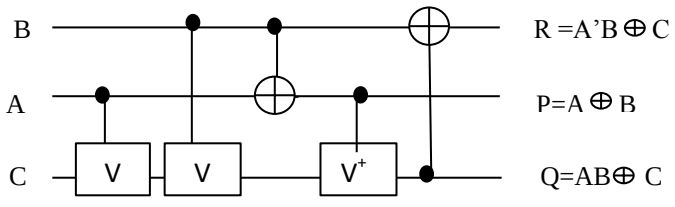


Fig. 4.13 Quantum Gate Representation of Proposed RSG Gate

The proposed RSG gate is also designed using elementary quantum gates shown in Fig. 4.13. For reducing the quantum cost, order of inputs and outputs are changed, but this will not affect the functionality of circuit. Though this way, quantum cost of circuit is reduced to five from

seven. The proposed gate is further used in designing 1 bit full adder and subtractor circuit. The block diagram and quantum gate representation are shown below in the Figure 4.14 and 4.15 respectively.

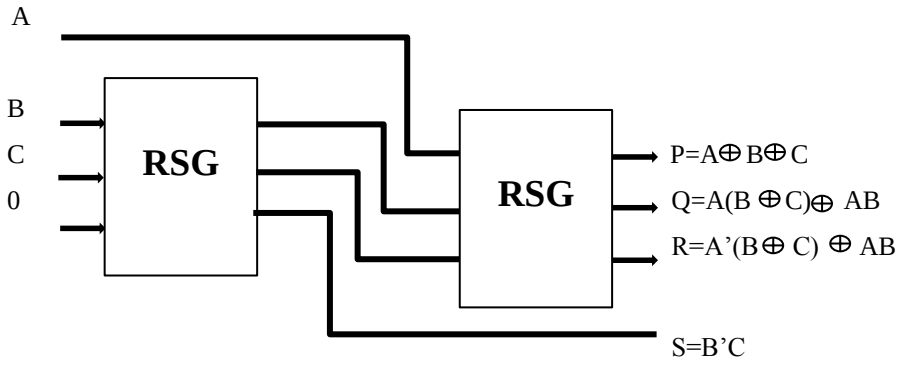


Fig. 4.14 Full Adder and Subtractor Design using Proposed RSG Gate

This gate can be worked as reversible i-bit full adder and subtractor with above mentioned diagram. In this case the circuit will generate sum, carry and borrow and one garbage output.

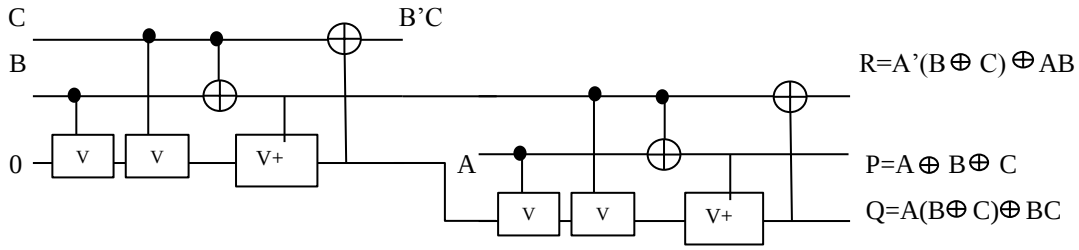


Fig. 4.15 Quantum Gate Representation of Full Adder using RSG

The quantum cost of reversible adder and subtractor circuit is ten, it is designed by combining two RSG gates in series with one another. In this also order of inputs and outputs are changed just to optimize the quantum cost. This will not affect the functioning of circuit. Here R represents borrow, P represents sum and Q is carry.

Proposed RSG gate is designed and simulated using two different technologies, the results and layouts are presented below. Following Fig. 4.16 shows the circuit diagram of RSG for QCA implementation. In QCA implementation RSG gate requires total of

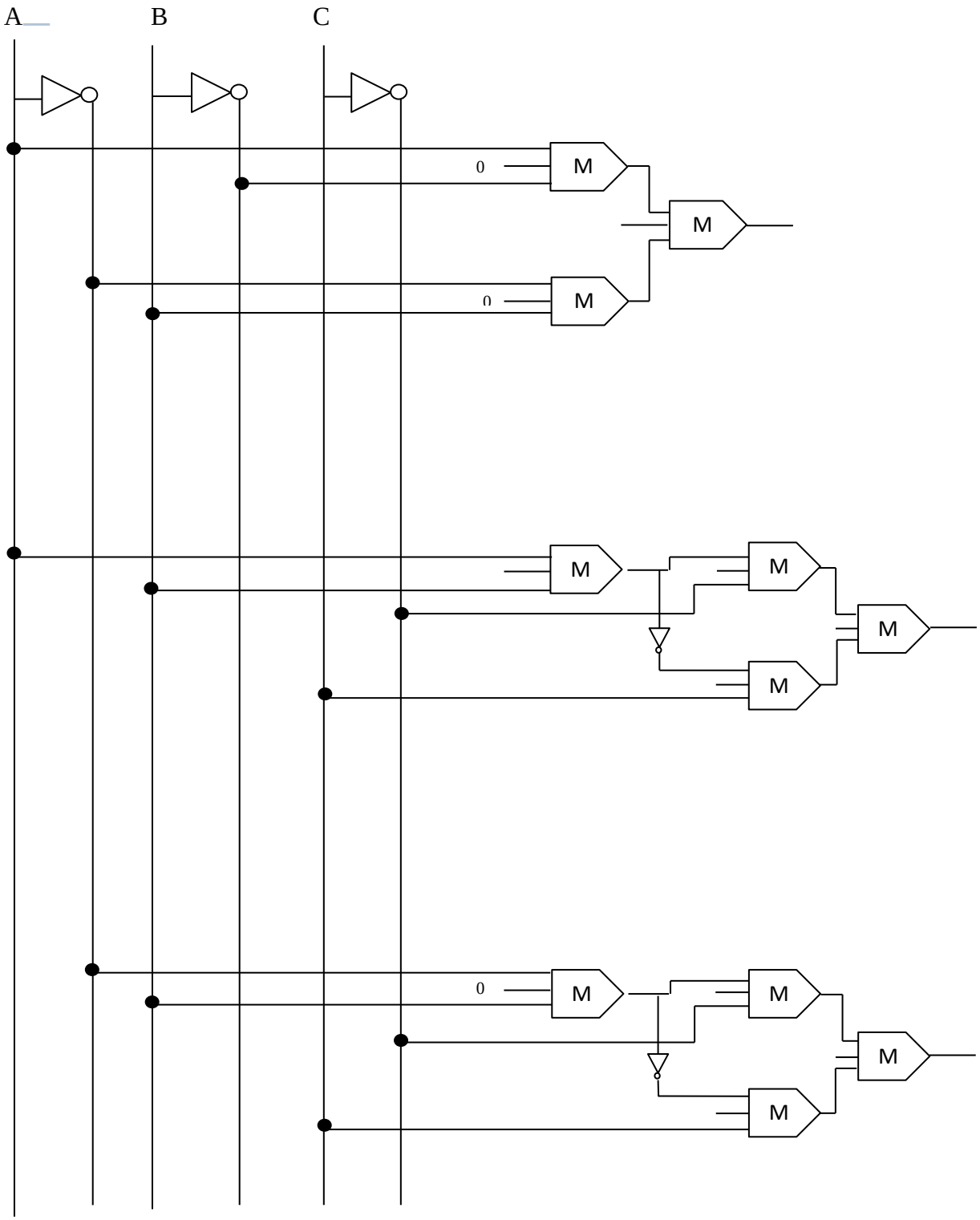
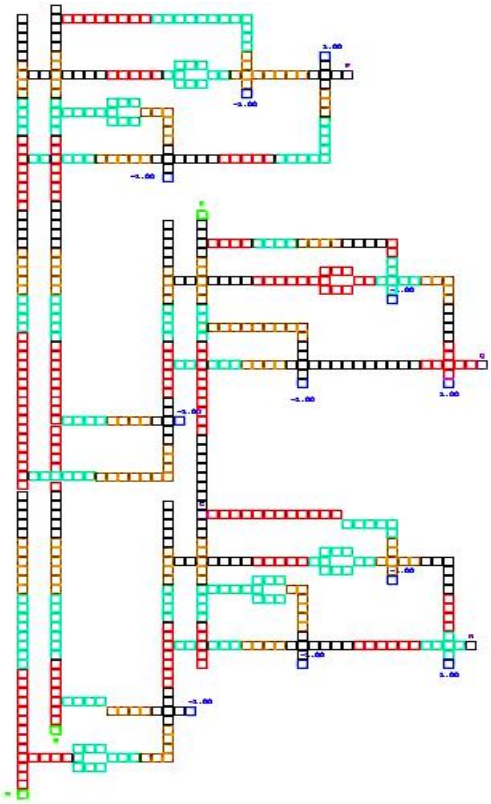
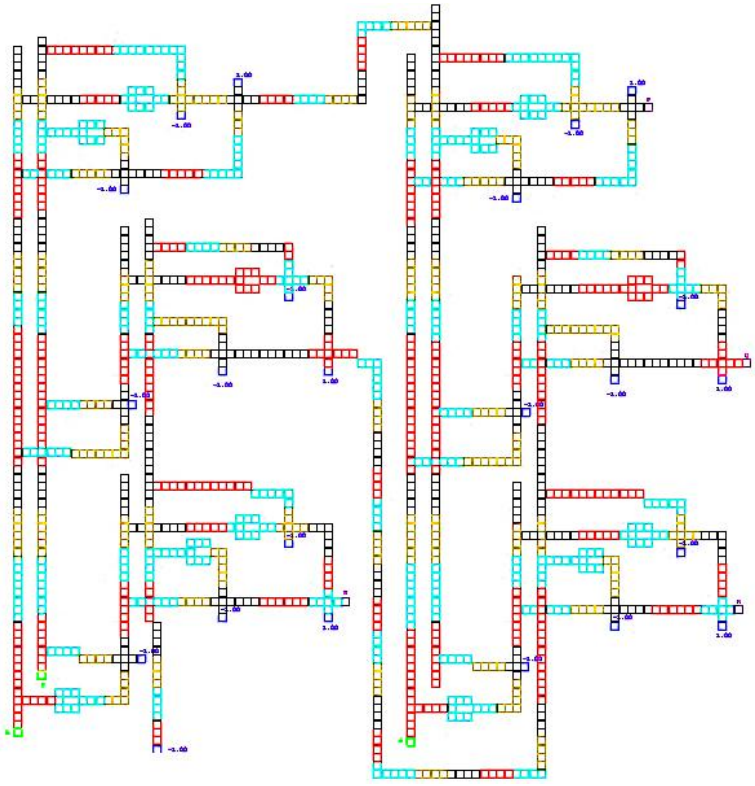


Fig.4.16 Circuit Diagram of Proposed RSG Gate for QCA Implementation



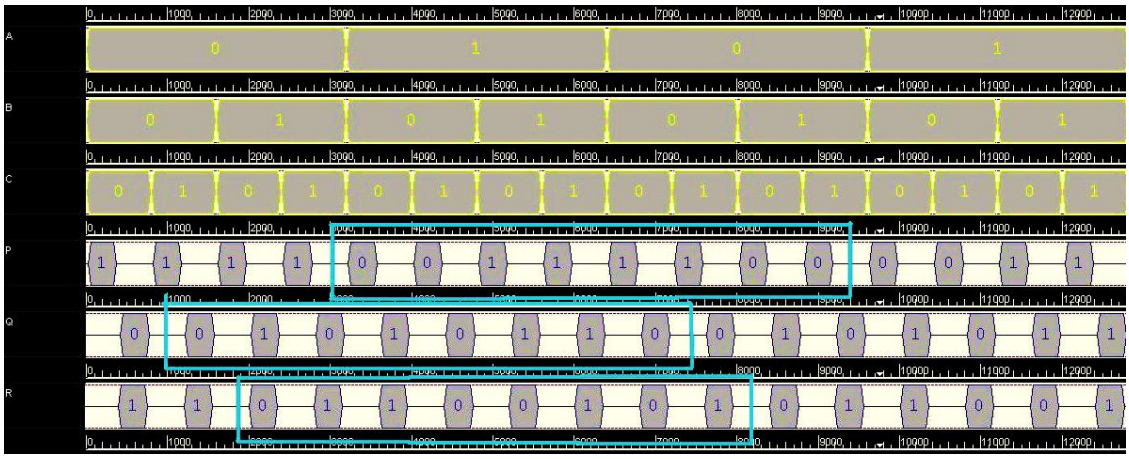
(a) RSG



(b) RSG Full Adder & Subtractor

Fig. 4.17 RSG Layouts using QCA

Above mentioned Fig. 4.17 (a) and (b) represents the layout of RSG and RSG full adder and subtractor circuit respectively. RSG gate is designed using eleven three input majority voter and six inverters.The output results are shown below in the Fig. 4.18. RSG waveform is shown in Fig. 4.18(a) with a clock latency of two. Fig. 4.18 (b) is output of full adder and subtractor design with clock latency of two.

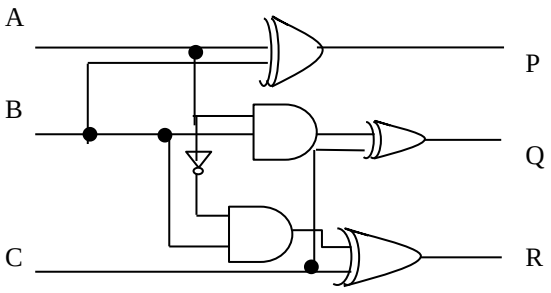


(a) RSG Waveform

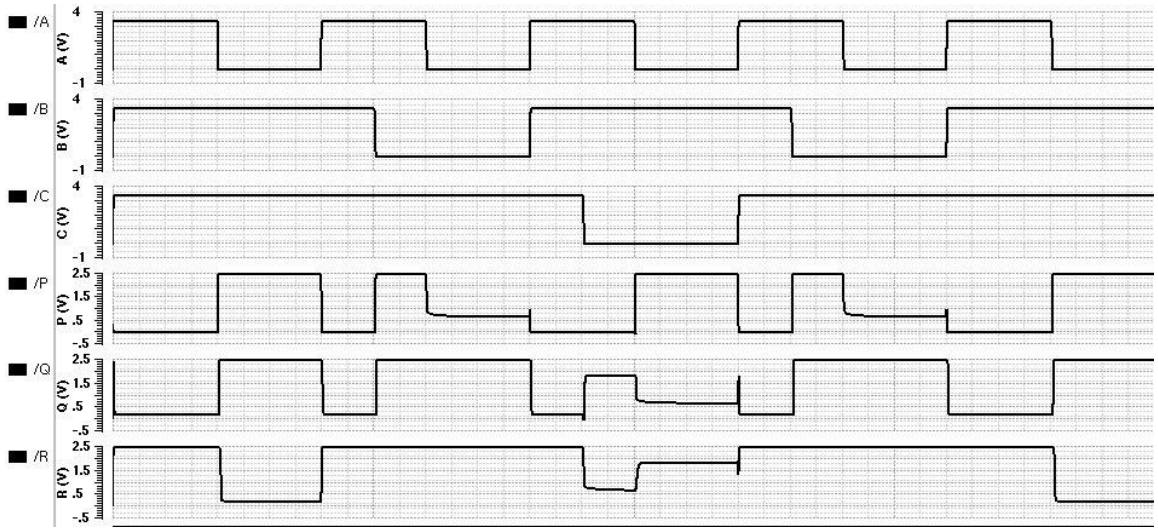
(b) RSG Full Adder & Subtractor Waveform

Fig. 4.18 Waveforms Using QCA

The circuit diagram for RSG gate using CMOS technology is shown in Fig. 4.19 (a), the output of circuit is shown in Fig. 4.19 (b).

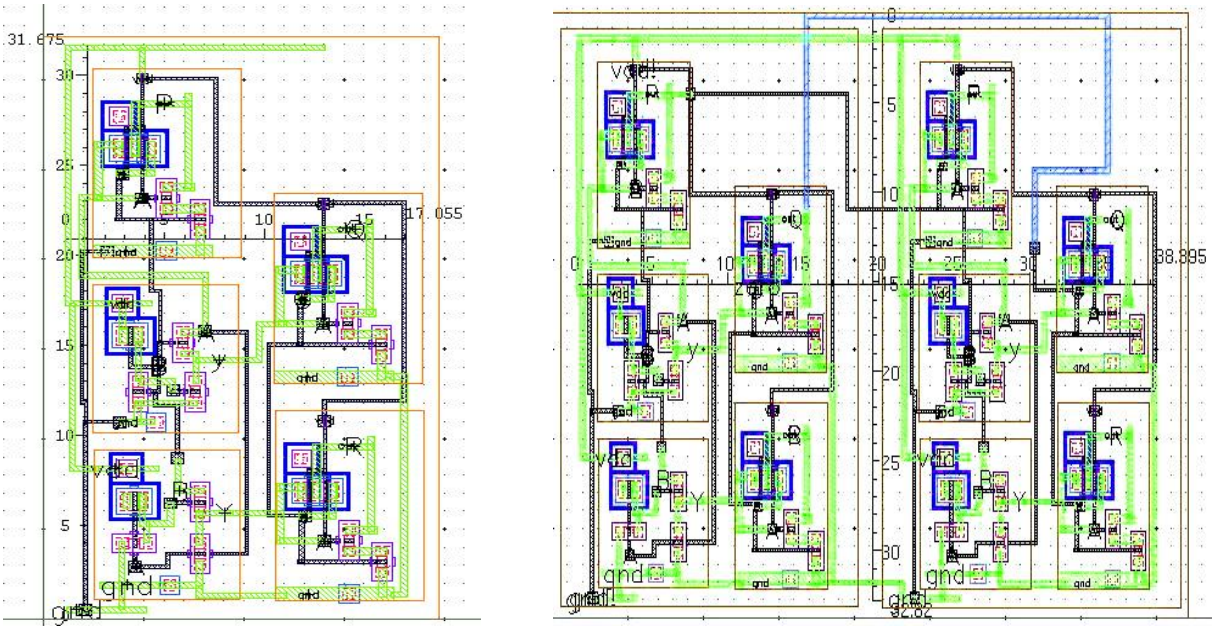


(a) Circuit Diagram of RSG for CMOS Implementation



(b) Waveform

Fig. 4.19 CMOS Implementation of RSG Gate



(a) RSG (b) RSG Full Adder & Subtractor

Fig. 4.20 Layouts using CMOS Technology (a) RSG (b) RSG Full Adder & Subtractor

The layouts are also drawn using CMOS technology in Fig. 4.20. Layout has no DRC errors.

4.4 Analysis

A comparative analysis of area in QCA with CMOS technology is presented. Further the novel proposed gate is compared with existing gates in literature on the ground of garbage output, quantum cost, and type of operations.

Table 4.3 Area comparison between CMOS and QCA

Gate	**CMOS**			**QCA**		
	Length (µm)	Width (µm)	Area $(\mu m)^2$	Length (nm)	Width (nm)	Area $(\mu m)^2$
FG	7.96	5.56	**44.25**	378.82	388	**0.15**
TG	12.91	16.55	**213.66**	509.28	606	**0.31**
PG	22.85	14.84	**339.09**	674.11	602.56	**0.41**
TR	24.48	18.32	**448.47**	726.33	741.29	**0.54**
RSG	31.67	17.05	**540**	1709.36	869.60	**1.49**
RSG FA-FS	32.82	38.395	**1260**	1898	1843	**3.50**

Table 4.3 shows area calculation of reversible gates in two techniques. The result shows tremendous reduction of area in QCA technology. In each case of reversible gate area is reduced to a great extent.

Table 4.4 Area Improvement in QCA

Gate	CMOS Area	QCA Area	% Improvement in Area
FG	44.25	0.15	**99.66**
TG	213.66	0.31	**99.85**
PG	339.09	0.41	**99.87**
TR	448.47	0.54	**99.87**
RSG	540	1.49	**99.72**
RSG FA-FS	1260	3.50	**99.72**

Table 4.4 shows percentage improvement of area in QCA technique. The results are remarkable and open a new door for the high density devices. QCA shows nearly 99 percent reduction of area, which is very much desired now a days.

Table 4.5 shows the comparison of proposed RSG gate with existing gates present in the literature. RSG gate outperforms to existing gates in terms of garbage output. Since its quantum cost is five, but garbage count is zero. Though NFT gate also has garbage output as zero but its quantum cost is six.

Table 4.5 Comparison of Reversible Gate

Gate	I / O Count	Quantum Cost	Garbage Output
TG	3	5	2
PG	3	4	1
FRG	3	5	1
NFT	3	6	0
TR	3	4	1
RSG	3	5	0

Table 4.6 Comparison in terms of Multi-functionality

Gate	NOR	OR	NOT	AND	NAND	XOR	XNOR	PASS	HA	HS	Operation Counts
TG	✗	✗	✗	✓	✓	✓	✗	✓	✗	✗	4
PG	✗	✗	✓	✓	✓	✓	✗	✓	✓	✗	6
FRG	✗	✓	✗	✓	✗	✗	✗	✓	✗	✓	4
NFT	✗	✓	✓	✓	✓	✓	✗	✓	✗	✗	6
TR	✗	✗	✓	✓	✗	✓	✓	✓	✗	✓	6
RSG	✗	✗	✓	✓	✓	✓	✓	✓	✓	✓	8

Table 4.6 shows a comparison among reversible gates on the ground of number of operations a gate can perform or in terms of multi-functionality. The results show that proposed RSG gate performs maximum of eight operations which makes it remarkable than other gates. Here HA refers to half adder and HS refers to Half subtractor. This is the only gate which performs both the operations simultaneously.

The above presented results are also depicted in graphical form shown below in Fig. 4.7 and 4.8.

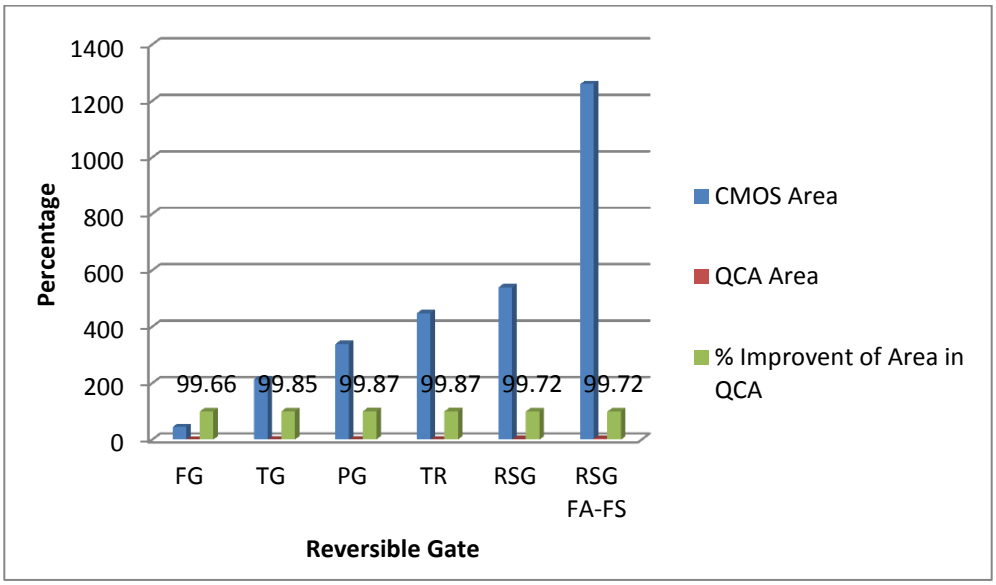


Fig. 4.7 Area Improvement in QCA

Fig. 4.7 shows the reduction of area in QCA technology in percentage. The graph shows as the complexity of circuit increases CMOS techniques require more area but QCA maintains the area requirement, does not increase rapidly like CMOS technique.

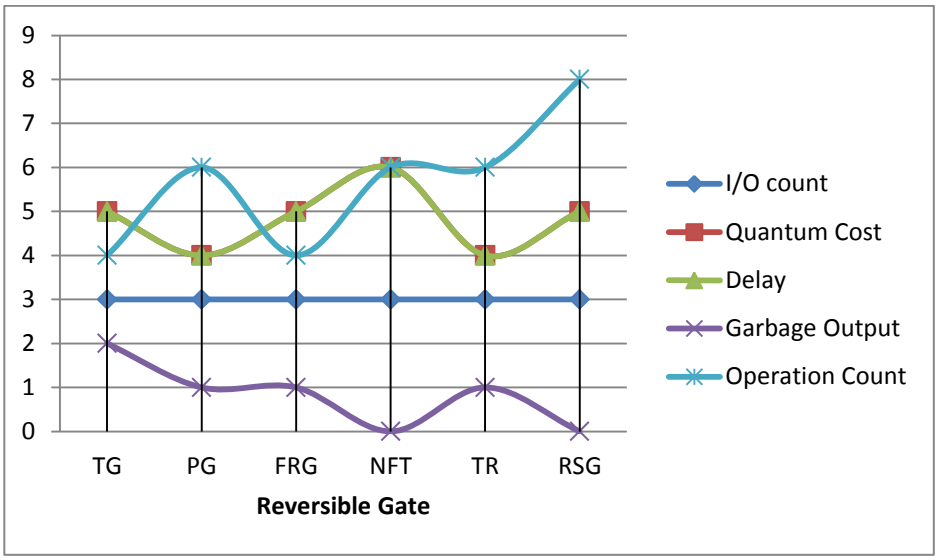


Fig. 4.8 Parameter Comparison among Reversible Gates

Fig. 4.8 shows the outperformer RSG gate. Graph depicts that RSG has maximum number of multi functional operation count of eight and garbage output as zero. For a good design we need to suppress garbage output to minimum and operation count to maximum, proposed RSG gate is fulfilling both the criterion.

CHAPTER. 5 CONCLUSION & FUTURE WORK

Implementation of fundamental reversible gates using three different approaches is presented. No such work on reversible circuit using CMOS technology and QCA is presented yet. As QCA shows a tremendous reduction in area, these results postulate that QCA is the forthcoming technique in coming ages, because the area improvement is nearly equal to 99% of current technology, if this is showing this much of reduction for small circuits, then surely this is going to improve the area for bigger circuits also. Hence more compact circuitry can be made with high density. The proposed design RSG can be a basic cell for many DSP circuits and ALU where both the operations are needed simultaneously. This can be a core block in arithmetic logical unit, because a single gate can perform both the operations hence the selection pins can be used for another operation in ALU. This proposed gate can be further used in designing reversible multipliers, carry look ahead adders, ripple carry adders and subtractors etc. The other way round, in this design a control pin is removed which further removes extra pin from the circuit. RSG gate has maximum number of operation count; therefore it can replace existing reversible gates in terms of multi-functionality. There is no any clear idea about calculation of power and delay in QCA circuits. More emphasis is needed on calculation of these parameters. Many more corners of designing are untouched like DRC, Optimization, Floor Planning in QCA the research is in progress.

REFERENCES

[1] John C. Gallop (1990)," SQUIDS, the Josephson Effects and Superconducting electronics"CRC Press,1990.

[2] A. Barenco and C. H. Bennett, et.al. (1995)" Elementary gates for quantum computation. Phys. Rev. A, 52(5),1995,pp.3457–3467.

[3] J. A. Smolin and D. P. DiVincenzo (1996),"Five two-bit quantum gates are sufficient to implement the quantum fredkin gate"Phys. Rev. A, 53(4),1996,pp.2855–2856.

[4] A. Turing (1936),"On computable numbers with an application to the Entscheidungs-problem," Proc. Lond. Math. Soc. Ser. 2, 42 ,1936, pp.230-65.

[5] R. Landauer , (1961),"Irreversibility and heat generation in the computational process",IBM J.Research and Development,vol.5, Dec.1961,pp.183-191.

[6] C. H. Bennett (1973), "Logical Reversibility of Computation," IBM Journal of Research and Development, vol.17 ,1973, 525-32.

[7] D.Grobe et.al.(2008),"Exact Synthesis Of Elementary Quantum Gate Circuits for Reversible Functions with Don't Cares", 38th international Symposium on Multiple valued Logic,2008.

[8] T.Toffoli (1980),"Reversible Computing,"MITLab for Computer Science,Tech.Rep.Tech memo MIT/LCS/TM-151,1980.

[9] S.Ankur et.al. (2011),"Realization of Reversible Logic DNA Computing",11th IEEE International conference on Bioinformatics and Bioengineering,2011.

[10] A. Morgenshtein et.al.(2002), "Gate-Diffusion Input (GDI): A Power efficient Method for Digital Combinatorial Circuits," IEEE Transactions on Very Large Scale Integration (VLSI) Systems,Vol. 10, No. 5, 2002.

[11] "Nano -Arch Online Quantum Dot Cellular Automata QCA", University of Erlangen- Nürnberg 2012.

[12] W.Konard et.al.(2004),"QCADesigner:A Rapid Design And Simulation Tool For Quantum-Dot Cellular Automata",IEEE Transactions on Nanotechnology,2004,pp 26-31.

[13] G. Toth and C. S. Lent (1999), "Quasi adiabatic switching for metal-island quantum-dot cellular automata", J. Appl. Phys., vol. 85, no. 5, Mar.1999,pp. 2977– 2984.

[14] K. Hennessy and C. S. Lent (2001),"Clocking of molecular quantum-dot cellular automata", J. Vac. Sci. Technol. B., vol. 19, no. 5, Sept./Oct.2001,pp. 1752 –1755.

[15] Thapliyal H. and Ranganathan N.et.al. (2012),"Design of Testable Reversible Sequential Circuits",IEEE Transactions on Very Large Scale Integration (VLSI)System,2012.

[16] Thapliyal H. and Ranganathan N. (2011),"A New Design of The Reversible Subtractor Circuit",11th IEEE International Conference on Nanotechnology,2011,pp.1430-1435.

[17] Sultana S. and Radecka K. (2011),"Reversible Adder/Subtractor with Overflow Detector",IEEE 54th International Midwest Symposium on Circuits and systems,2011,pp.1-4.

[18] www.toshiba-europe.com/research/crl/pig/index.htm.

[19] www.Sciencedaily.com/articles/q/quantum_dot.htm.

[20] Akeela R. and Wagh D.(2011),"A five Input majority Gate in Quantum-dot Cellular Automata",54th IEEE International Midwest Symposium on Circuit and Systems,2011,pp.1-4.

[21] Karthigai L. et.al. (2010),"Design of Subtractor using Nanotechnology Based QCA",IEEE International Conference on Communication Control and Computing technologies",2010,pp.384-388.

[22] Navi K. et.al.(2012),"A Novel Seven Input Majority Gate In Quantum-Dot Cellular Automata",IJCSI,vol. 9,1,2012,pp.84-89.

[23] Navi K. et.al. (2010),"Five-Input Majority Gate,a new Device for Quantum-Dot Cellular Automata",Journal of Computational and theoretical Nanoscience,vol. 7,2010,pp.1-8.

[24] Walus K. et.al.(2004),"QCADesigner:A Rapid Design and Simulation Tool for Quantum-Dot Cellular Automata",IEEE Transactions on Nanotechnology,vol. 3,1,2004,pp.26-31.

[25] Islam Md. R .et.al. (2003),"Reversible Logic Synthesis for Minimization of Full-Adder Circuit",Proc. Of thr Euromicro Symposium on Digital System Design,2003,pp. 50-54.

[26] W. Wang, K. Walus et. al. (2003), "Quantum Dot Cellular Automata Adders", IEEE Nano Conference, 2003.

[27] R. Zhang et. al. (2004), "A Method of Majority Logic Reduction for Quantum Cellular Automata," IEEE Transaction on Nanotechnology, vol. 3 , no. 4, pp. 443-450, Dec. 2004.

[28] Heumpil Cho et. al. (2007), "Adder Design and Analysis for Quantum Dot Cellular Automata", IEEE Transaction on Nanotechnology, vol. 6, no. 3, pp. 374-383, May 2007.
[29] G.H.Bernstein et.al. (2005), "Magnetic QCA System", Micro Electronics Journal, Elsevier, vol.36, pp. 619-624, 2005.
[30] J. Huang et.al. (2007), "Design of Sequential Circuits by Quantum-dot Cellular Automat", Microelectronics Journal, Elsevier, vol.38, pp.525-537, 2007.
[31] George I. et.al. (2007), "Research Directions in beyond CMOS computing", Solid State Electronics, Science Direct, vol. 51, pp. 1426-1431, 2007.
[32] M. Macucci et.al. (2003), "A QCA Cell in Silicon-on –Insulator Technology: theory & experiment", Super lattices & Microstructures, vol. 34, pp. 205-211, 2003.
[33] Steven C. Henderson et.al. (2004), "Incorporating Standard CMOS Design process Methodologies into the QCA Logic Design Process", IEEE Trans. On Nanotechnology, vol. 3, no. 1, march 2004.
[34] Sarah T. Yanchan et.al. (2013), "Design of a 4-bit Ripple Adder using Quantum-dot Cellular Automata (QCA)", IEEE International Conference on Circuits & Systems" pp. 33-38, sep 2013.
[35] K. Das et.al. (2009), "A Novel Approach of And-Or-Inverter (AOI) Gate design for QCA" , 4th International Conference on Computer & Devices for Communication , pp. 1-4, Dec. 2009.
[36] H. Cho et.al.(2009)," Adders & Multiplier Design in Quantum-Dot Cellular Automata", IEEE Transactions on Computer, vol. 58, no.6, pp. 721-727, June 2009.
[37] Kim A. et.al. (2013), "Parallel Prefix Adder Design using Quantum-dot Cellular Automata", 26th Symposium on Integrated Circuits & System Design, pp. 1-6, 2013.