Post Layout Simulation & Corner analysis on Folded Cascode Current Mirror Circuit

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Abstract
Current mirror is the basic building block in analog circuit design for providing the biasing voltage to so many components in the system. In this paper a high performance MOSFET current mirror in a folded cascode configuration is designed. The layout of the proposed circuit is also designed and its corner analysis is done with FF , FS ,SF and SS with varying temperature between -25°C to 80°C and this circuit works perfectly when going for fast fast (FF) simulation in these extreme ranges of temperatures.

Keyword: Current Mirror, Folded Cascode, Layout, Post-Layout-Simulation

I. INTRODUCTION

Post layout simulation is very important for any design as it gives us the clear picture of what is going to happen when including all the parasitic value, to do post layout of your design we need to compare the result of our file with the extracted view of your layout design and the result we got when we have compared these three different output varies a lot. The output AV_old_layout when compared with the schematic is 65.56% same which is a very large deviation of our result but when we compared our AV_new_layout with our schematic file we get to know that our design is 99.99% accurate which tells us that the layout design of any circuit can deviates or change the output when including the parasitic capacitance and resistance. So, designing of the layout should be very precious with less usage of any poly material as that might change our output.

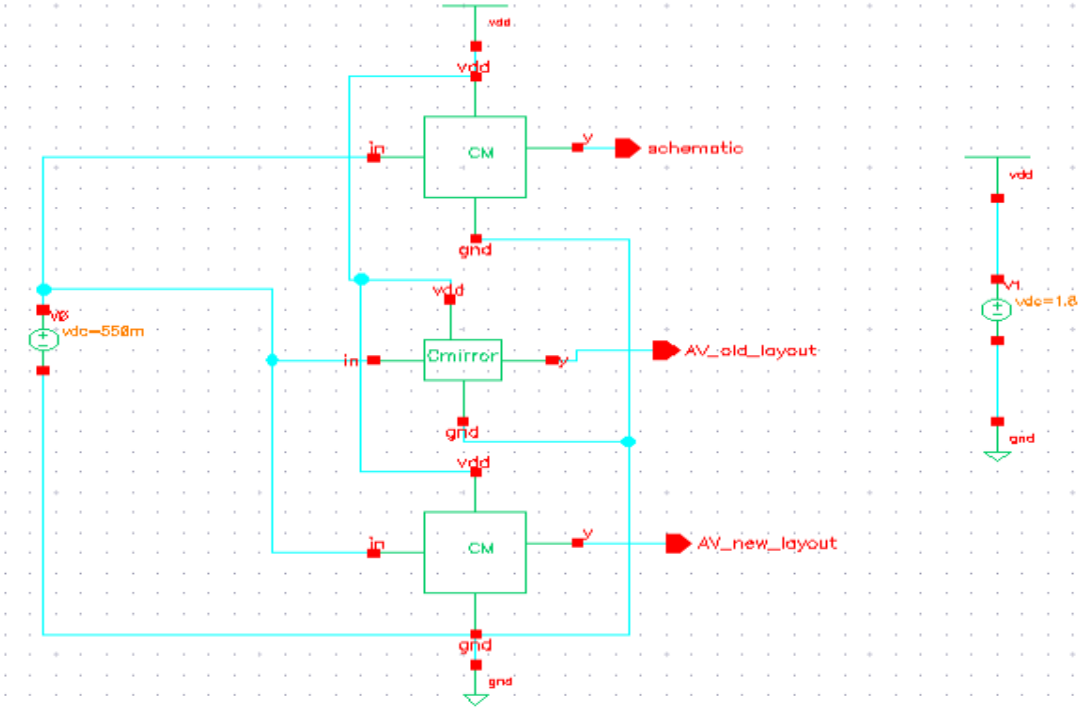

Fig. 1: Post layout simulation

II. POST LAYOUT SIMULATION

Post layout simulation results shows that there is quite a lot of deviation due to the parasitic value added due to metal and poly material so after designing the efficient layout of the circuit with less poly silicon material and less metals we can achieve exact ranges of value which we find in schematic and those values are exactly matched as shown in below figure 2.

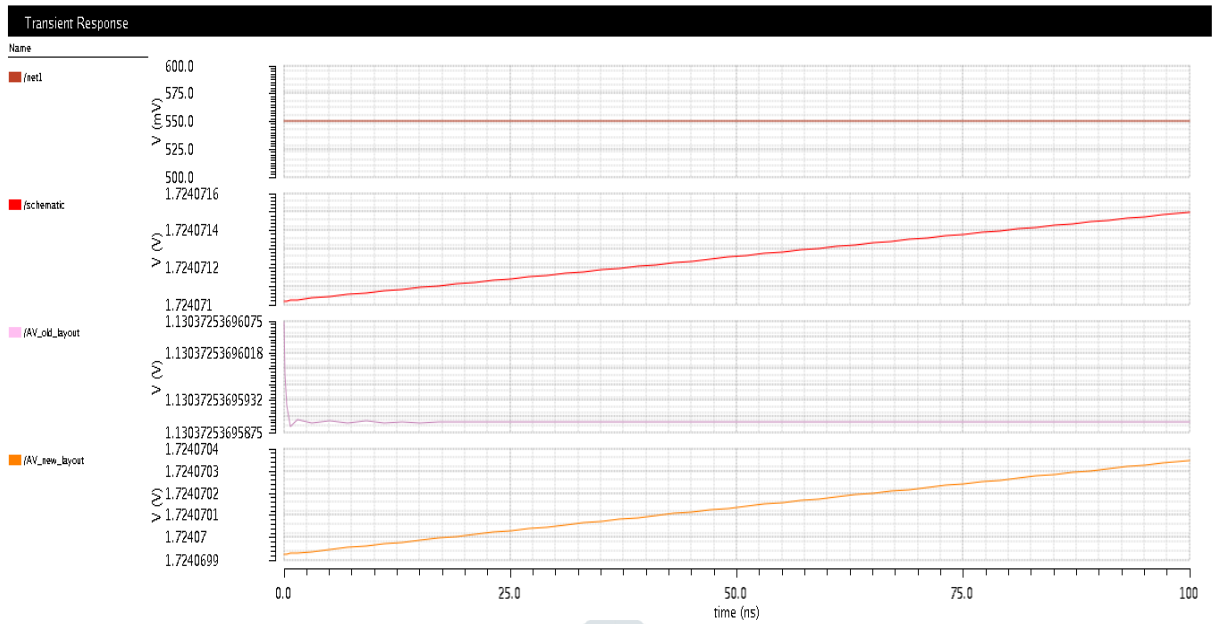

Fig. 2: Post layout simulation of current mirror.

From the above circuit we get to know that there is only 65.56% similarity of the design00 between schematic and the old layout design and when we have designed the efficient new design layout with less metal and poly material we have achieved 99.99% similarity output which is quite a good design of the circuit as shown in figure 2.

III. CORNER ANALYSIS

Corner analysis of the circuit is done to know the behaviour of the circuit with extreme changes of parameter that is due to manufacturing variations. When the chip is manufactured theoretically, we can predict yield as the process variation is constant but when we move in practical point these process variations varies around their ideal point which in result effect the total yield of the manufacturing. When working in schematic we basically deal with FEOL (Front end of line) which affect the performance of the circuit and second one is BEOL (back end of line) which will affect parasitic. So, corner analysis will tell us the performance generated due to variation expected due to process, voltage and temperature, and these results will tell us that the extreme change in the condition will my design will work or not. There are four corner FF, FS, SF and SS which will define my circuit behaviour. On doing the corner analysis on my circuit of folded cascade current mirror we get to know that there is lot of variation of the output with skewed corners that is FS. Corner analysis for FF, SS and SF is somewhat similar with less change in the output current values as shown below, Nominal is the one where there is no variation included.

Table 1: Corner Analysis without temperature

Serial Number	Type of Corner	Input current (A)	Output current (A)
1	Nominal (NN)	14.5516u	15.5339u
2	Fast-Fast (FF)	58.1041u	58.0899u
3	Fast-Slow (FS)	55.2225u	48.4381u
4	Slow-Fast (SF)	2.20703u	2.90588u
5	Slow-Slow (SS)	2.09532u	2.39805u

On doing the temperature variation of the circuit from -25°C to 80°C there is lot of variation in every corner except in FF as shown in table.

Table 2: Corner analysis with temperature

Serial Number	Type of corner Analysis	Input current (A)		Output current (A)	
		Temperature		Temperature	
		-25°C	80°C	-25°C	80°C
1	Fast-Fast(FF)	47.707u	65.747u	47.843u	65.737u
2	Fast-Slow(FS)	45.143u	62.629u	40.02u	54.49u
3	Slow-Fast(SF)	9333.27n	4.0413u	1.2811u	5.1868u
4	Slow-Slow(SS)	879.94n	3.8593u	1.0335u	4.3496u

IV. CONCLUSION AND FUTURE SCOPE

The proposed circuit uses folded cascode current mirror with the range 100m-600m voltage & perfect current mirroring at V_{bias}=550m V. The output resistance of the folded cascade current mirror came out to be 16.3M Ω. It's corner analysis is done with and without temperature variations and for fast-fast (FF) variation the circuit is showing less variation when adding the extreme temperature variation of -25°C and 80°C as shown in table 2. Its output voltage equation is derived that shows the involvement of reference current into the output voltage. Further this design can be used to implement any bigger circuit like in amplifier and can be act as a current source.

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