A Novel Low Power Hybrid Flip Flop Using Sleepy Stack Inverter Pairs

DISSERTATION

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By

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May 2014

CERTIFICATE

This is to certify that the Thesis titled "**Implementation Of Low Power and High Speed D Flip Flop**" that is being submitted by " ***D Helga Evangelene***" is in partial fulfillment of the requirements for the award of MASTER OF TECHNOLOGY DEGREE, is a record of bonafide work done under my guidance. The contents of this Thesis, in full or in parts, have neither been taken from any other source nor have been submitted to any other Institute or University for award of any degree or diploma and the same is certified.

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ACKNOWLEDGEMENT

The LORD (JESUS CHRIST) is good and his love endures forever;
His faithfulness continues through all generations.

Psalm 100 : 5

My humble prostration to the **Lord Almighty Jesus Christ** for His presence, guidance and providing me with His strength and wisdom in accomplishing my dissertation successfully.

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This is to certify that D Helga Evangelene bearing Registration no 11204543 has completed objective formulation of thesis titled, **"A Novel Low Power Hybrid Flip Flop Using Sleepy Stack Inverter Pairs"** under my guidance and supervision. To the best of my knowledge, the present work is the result of her original investigation and study. No part of the thesis has ever been submitted for any other degree at any University.

The thesis is fit for submission and the partial fulfillment of the conditions for the award of MTech degree.

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DECLARATION

I, D Helga Evangelene, student of MTech ECE under Department of Electronics and Communication Engineering of Lovely Professional University, Punjab, hereby declare that all the information furnished in this thesis report is based on my own intensive research and is genuine.

This thesis does not, to the best of my knowledge, contain part of my work which has been submitted for the award of my degree either of this university or any other university without proper citation.

Date : D HELGA EVANGELENE

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ABSTRACT

This paper presents a low power hybrid flip flop using sleepy stack inverter pair for retaining the logic level till the end of evaluation and pre-charge phase of the flip flop. The sleepy stack inverter pairs are efficient in leakage reduction and overall power dissipation as the technology scales down to 90nm and below. The performance of the proposed D flip flop is compared with the conventional flip flop which uses conventional static CMOS inverter pairs in cadence 90nm tool. It shows 32% reduction in total power consumed with 21% reduction in leakage power T flip flop, SR flip flop and JK flip flop were designed using the proposed D flip flop and its performance were compared with T flip flop, SR flip flop and JK flip flop designed using conventional D flip flop. The proposed flip flop is simulated with the supply voltage of 1.2V and 1.8V and compared. As the proposed flip flops have improved performance in terms of leakage power, total power and power delay product at high speed with moderate noise it can be widely used in high performance applications.

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CHAPTER 1

INTRODUCTION

Flip flops are widely used in synchronous sequential digital circuits. An efficient flip flop will have high clock frequency to increase the speed of the system. Due to increase in speed of the systems, there is a huge challenge for researchers today to meet out the large power consumed by the system. Flip flops consume two types of power. They are 1) Dynamic power dissipation which is due to switching activity and short circuiting [7], [10]. 2) Static power dissipation is due to the leakage current and reverse bias PN junction [10]. The leakage power is present at both runtime and off state. Even when the system is in off state the leakage current creates a scenario that the system is under operation. This leakage power is highly prevalent in deep sub micrometer (DSM) CMOS technology as the feature size gets reduced below 0.1micron. So the off state leakage power and runtime leakage power should be kept minimum. Flip flops can be designed by two ways namely dynamic logic style and static logic style. Dynamic style exhibits high speed and less area where as static design style exhibits low power. Leakage power reduction technique can be classified into two: 1. State destructive technique which does not retain exact logic state when the circuit is switched to other modes. 2. State saving technique which retains the exact logic state[9]. Here we explain the various types of flip flops along with introduction to various design issues such as power dissipation, leakage power reduction, noise and metastability.

1.1 SEQUENTIAL CIRCUIT

Sequential circuit is a type of digital circuit whose output depends on both present input and previous input signals. When a combinational logic circuit is included with a memory, a sequential logic circuit is designed. The memory can be a flip flop. Sequential logic circuits can be divided into two types:

a. Asynchronous sequential circuit

b. Synchronous sequential circuit

a. Asynchronous sequential circuit

A latch is an example of asynchronous sequential circuit. A latch is a transparent digital circuit. It is a level sensitive circuit. An input signal controls the

output. It has the Race over problem. D latch, SR latch are some of the examples of latches.

b. Synchronous sequential circuit

Flip flop is an example of synchronous sequential circuit. It is a non-transparent digital circuit. The clock input controls the output signal. Here reading of the input and writing of the output is two different functions unlike latches.

1.2 FLIP FLOP

A flip-flop is a bistable multivibrator. They are edge sensitive devices. They can be either positive edge sensitive or negative edge sensitive. When it is used in a finite state machine, the output not only depends on current input but also depends on current state that is the previous input. So it is used to count pulses and synchronization of signals. Various kinds of flip flops are D flip flop, T flip flop, SR flip flop and JK flip flop. T flip flop, SR flip flop and JK flip flop can be designed using a D flip flop.

1.2.1 D FLIP FLOP

It is a data or delay flip-flop. Q will be equal to D when clock is high. When the clock is at logic1, it reads the input. When the clock is at logic low, it writes the output. It acts as a delay flip flop when it gives some delay to any circuit when desired.

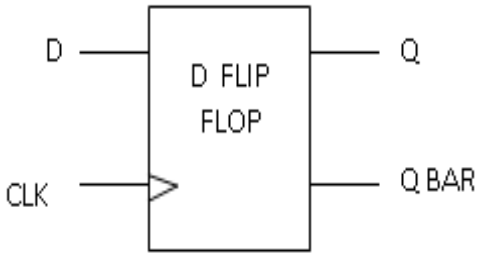

Fig 1.1 D Flip Flop

Characteristic equation : D=Q

Characteristic Table

Table 1.1 Characteristic Table of D flip flop

D	Q
0	0
1	1

1.2.1 T FLIP FLOP

The toggle flip flop changes its state when T input is high and clock input is strobed. It holds the previous value if T input is low. It can be designed using a D flip flop.

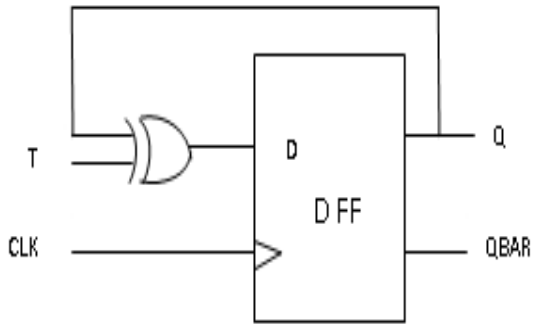

Fig 1.2 T Flip Flop

Characteristic equation : Q_{next} = TQbar + TbarQ

Characteristic Table

Table 1.2 Characteristic Table of T flip flop

T	Q	Q_{next}	COMMENTS
0	0	0	Hold state
0	1	1	Hold state
1	0	1	Toggle
1	1	0	Toggle

1.2.2 SR FLIP FLOP

It is a set reset flip flop. When the input S is at logic 1, the output is set to 0. When the input R is at logic 0, the output is reset.

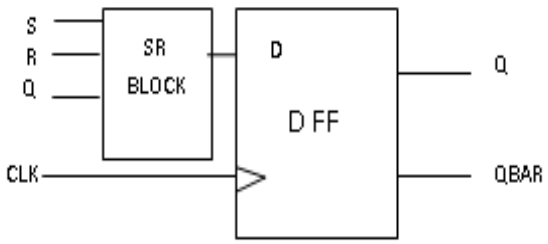

Fig 1.3 SR flip flop

Characteristic equation : $Q_{next} = S + (RbarQ)$

Characteristic Table

Table 1.3 Characteristic Table of SR flip flop

S	R	Q_{next}	COMMENTS
0	0	0	No change
0	1	0	Reser
1	0	1	Set
1	1	-	Invalid

1.2.2 JK FLIP FLOP

It is similar to SR flip flop with the exemption that it toggles when both the inputs J and K are 1.

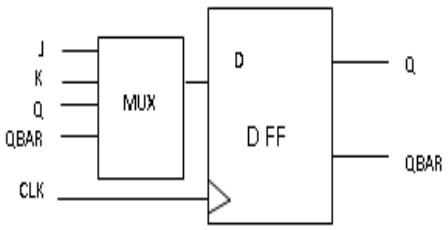

Fig 1.4 JK flip flop

Characteristic equation : $Q_{next} = JQbar + KbarQ$

Characteristic Table

Table 1.4 Characteristic Table of JK flip flop

J	K	Q_{next}	COMMENTS
0	0	Q	No change
0	1	0	Reset
1	0	1	Set
1	1	Qbar	Invalid

1.3 POWER DISSIPATION

Dynamic power dissipation (P_d) and static power dissipation ($P_{s)}$ contributes to the overall total power dissipation. Though dynamic power dissipation contributes maximum to the total power dissipation, in deep submicron technologies static power also gets increased unlike higher nanometer technologies. Dynamic power dissipation is due to switching activity. It depends on the frequency (f) , supply voltage (V_{dd}) and load capacitance (C_L) of the circuit [10]. The relation is given below.

$$Pd = f \, . C_L . V_{dd}^2$$

The static power dissipation depends on the leakage current ($I_{leakage}$) and the supply voltage (V_{dd}). The relation is given below.

$$Ps = I_{leakage} \ . V_{dd}$$

1.4 LEAKAGE POWER REDUCTION

Leakage power reduction is one of the main design criteria for any high speed application at standby mode. Sub threshold current is the main contribution to leakage power. The flow of current from source to drain even in standby mode increases the power dissipation. It can be reduced by using high threshold voltage transistor as sleep transistors. The threshold voltage of transistor is dependent on body bias. Normally the substrate of PMOS is conne+++cted to V_{dd} and substrate of NMOS is connected to gnd. This biasing is called as “Zero Body bias”. If the substrate of PMOS and NMOS are connected to bias voltage higher and lower than supply voltage and gnd, it is called “Reverse body bias”. This in turn increases the threshold voltage of the transistors. The relation between threshold voltage (V_t) and substrate voltage (V_{sb}) is given below :

$$Vt = V_t(0) \pm \delta\sqrt{(V_{sb} + 2\emptyset_F)} \text{ - } \sqrt{2\emptyset_F}$$

Where,

$$V_t(0) - threshold\ voltage\ when\ V_{sb} = 0$$

$\emptyset_F$ – constant $\qquad\qquad \delta = \ {(t_{ox}/\in_{ox})} \quad \sqrt{2\ q\ N_A\ \in_{si}}$

Leakage power can also be reduced by stack effect. When two or more transistors are stacked together, the reduction in power is more when they are switched off together.

1.5 NOISE

Noise is an important factor which has to be taken into consideration while reducing the power dissipation. The total noise in the design is represented in terms of noise spectral density with the unit V^2 /Hz. The noise spectral density gets decreased with increase in frequency. As frequency increases, power also gets increased. So there is less noise spectral density at high power. When noise margin of a design is improved, the power gets increased. So there is a need to maintain moderate noise even though the power is getting reduced. There are two types of noise : 1. Low frequency noise and 2. High frequency noise. Flicker noise and white noise are present in a MOSFET. The flicker noise is a low frequency noise which decreases with increase in frequency. The white noise is a high frequency noise which is constant throughout.

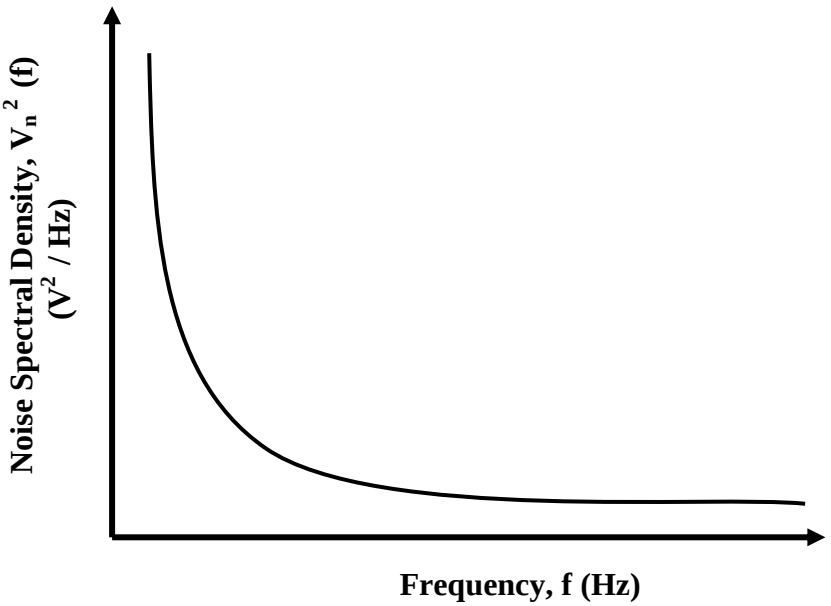

Fig.1.5 Noise Spectral density

1.6 METASTABILITY

A flip flop can be in two states: either in logic 1 or logic 0. If it goes to a state which cannot predicted to either 1 or 0 is called metastable state or quasi stable state. Metastability occurs when there is setup time and hold time violations, increased clock to Q delay and when the inputs changes in critical window. Metastable state cannot be completely removed, but can be reduced to some extent. The mean time between failure (MTBF) is used to find the time duration between two continuous failures. This state can

be avoided when the clock is period is large enough [16]. The MTBF can be calculated using the formula given below:

$$MTBF = 1/(f_{clk}\ f_d\ T_d\ )$$

where,

f_{clk} – *Clock frequency*

f_d – *Data frequency*

T_d – *setup time + hold time*

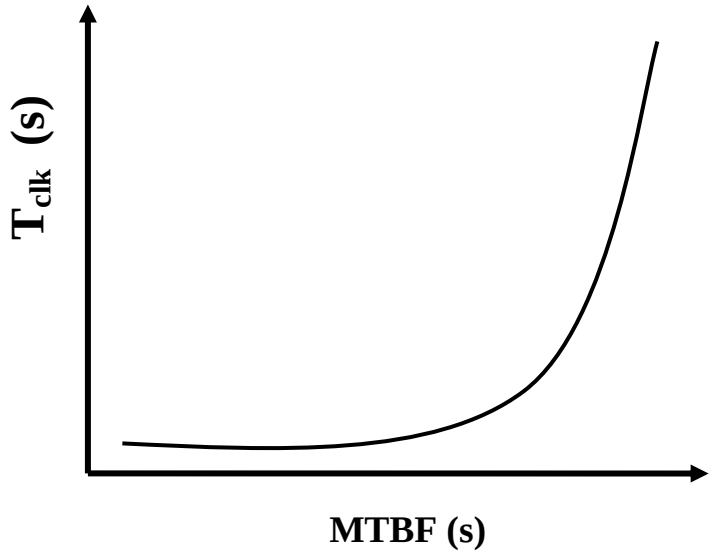

Fig. 1.6 Relation between MTBF and clock period.

1.7 MOTIVATION

The use of compact electronic gadgets is increasing in this scientific era. Though the gadgets are utilized for less time, the power consumption is more. Mobile phone is used by almost everyone in the world. Though we use for less time, it remains switched ON for the whole day. It utilizes power even at standby mode which decreases the charge in the battery. So even when the mobile phone is not in active mode, it still utilizes power. This power is called leakage power. This power is more in standby mode though it is negligible when compared to dynamic power. Another factor is the compactness of the technology. As technology features down to lower nanometer technologies below 0.1um, the leakage power gets increased. This made us to research on leakage power reduction in flip flops. As flip flops are the basic clock and storage

circuitry in all electronic gadgets, the power consumption should be given importance. So here we reduce the leakage power and total power of the flip flop with moderate noise by maintaining high speed[16].

1.8 THESIS ORGANIZATION

The thesis is organized as mentioned in the next page:

CHAPTER 2 : LITERATURE REVIEW. This chapter reviews the literature of various type of flip flops and leakage reduction techniques.

CHAPTER 3 : DESIGN METHODOLOGY. It includes the problem formulation, objective and design methodology.

CHAPTER 4 : DESIGN IMPLEMENTATION. It includes the implementation of conventional and proposed architectures and the transient analysis.

CHAPTER 5 : SIMULATION AND RESULTS. It includes the analysis of flip flop on following parameters- Power, Delay, Power delay product (PDP), Noise spectral density, and Mean time between failure (MTBF).

CHAPTER 6 : CONCLUSION. It concludes the thesis with the obtained results.

CHAPTER 2

LITERATURE REVIEW

Flip flops can be designed by three different design styles namely: 1. Static design style, 2. Dynamic design style and 3. Hybrid design style. The static design style consumes less power with larger delay. The dynamic design style consumes more power with high speed. It can be used for high speed applications. Here we consider hybrid design style where both static and dynamic design style are used which has the advantage of both the design styles. The dynamic style is used at its input and static style is used at its output. Some of the flip flops are reviewed below.

Kalarikkal Absel et al, September 2013 [8]**:** A hybrid flip flop with dynamic logic is used at its input and static logic is used at its output stage. This combination of both static and dynamic design style gives reduced power dissipation at high speed. The implementation of two dynamic nodes helps in decreasing the dynamic power consumption. Two back to back inverters are used which is designed in static CMOS style to hold the logic state. As these inverter pair is under operation throughout the evaluation and pre-charge phase of the flip flop, it tends to undergo larger run time leakage current. This makes the design to consume unnecessary power when technology shrinks down to 90nm and below. But it is easy to embed a logic in this type of design.

H. Patrovi et al, February 1996[1]: The Hybrid latch flip flop is a low power and low speed flip flop. It behaves like a transparent latch. It has soft clock edge. It does not allow clock skew. The process of latching takes place by overlapping phenomenon at its input. The low speed is due to large hold time in the design. The presence of series of NMOS transistor at its output is accountable for large delay in the circuit. Embedding logic into this design is not possible.

F. Klass set al, June 1998[2]: It is also a hybrid flip flop. It is designed to reduce the pipeline overhead. Embedding logic is possible in this design with small delay penalty.

O. Sarbishei et al, May 2007 [4]**:** This flip flop is designed based on Clock overlapping period. The overlapping can be 1-1 or 0-0. An inverter is used at the input side for clock overlapping. It is done by sizing one NMOS transistor of the inverter. It does not depend on load capacitance unlike hybrid latch flip flop where the inverters get increased with

load capacitance which increases area and power. So it increases the area and power in HLFF. This flip-flop has the lowest power-delay-product and consumes less area compared to other flip flops.

Vladimir Stojanovic et al, April 1991[7]: Various latches and flip flops were analysed using power, timing, PDP, transistor width parameters which affects the spedd of the design.

Nikola Nedovic et al, 2000 [6]: An improved form of Hybrid Latch Flip-Flop was designed here with increase in speed. Better soft-clock edge is achieved. Area is the trade off with increase in speed.

J. Yuan et al, January 1997[11]: New dynamic, semi static flip flops are proposed. They are of two types: differential and Non differential. In differential type of flip flop, both inverting and non-inverting inputs are fed to the circuit. The power delay product is greatly reduced than the conventional ones. The total number of transistors used is reduced. Clock loads are minimized in new differential flip flops by using only n-type transistors in place of p-latches which increases the speed of the circuit.

A. Hirata et al, June 2005[12]: The Cross Charge-control Flip-Flop (XCFF)is a hybrid flip flop which has two dynamic nodes. It reduces the power consumption in the design. Embedding a logic is not possible in this flip flop design.

Y.-F. Tsai, et al, June 2000[13]: The leakage reduction can be done by 3 ways. They are by using proper input output vectors, increasing the threshold voltage and decreasing the supply voltage.

Rajani H.P et al, August 2012[14]: This technique uses dual threshold voltage transistors. It uses high threshold voltage transistors as sleep transistors in pull up and pull down networks which decreases the leakage power at standby mode by removing the connection of the sleep transistors to V_{dd} and gnd.. The high threshold voltage is given by reverse body biasing technique. This decreases the sub-threshold current. But it takes large wake up time to come back to its normal active mode. Delay is the trade off in this technique.

N. Hanchate et al, 2004[15]**:** This technique uses the concept of "stack effect" to reduce leakage power. When two or more transistors are switched OFF together, there is greater decrease in leakage power due to disconnection to V_{dd} and gnd. As it has high internal resistance present, the sub-threshold current is reduced to a greater extent.

Jun Cheol Park et al, November 2006[9]: Leakage reduction technique reduces the leakage current at both run time of the system as well as during standby mode of the system. It uses multiple threshold voltage transistors and stack effect to fulfill the objective. This technique is the combination of both sleep transistor technique and forced stack technique. It is a state saving technique. It uses high threshold transistors as sleep transistors and another transistor connected in parallel to the sleep transistor. The stack effect is obtained by connecting low threshold transistors to these parallel transistors. The leakage reduction is achieved at sleep mode by stack effect and sleep transistors. The wake up time is not present as it saves the state even though when it moves from active mode to sleep mode.

Omid Sarbishei et al, February 2010[5]**:** The flip flop benefits from the overlap period. It may be 1-1 or 0-0 overlap of clock and its inverted outout. It gives negative setup time which increase the speed of the flip flop.

David Rennie et al, August 2012[16]: Metastability behavior quarto flip flop was discussed. Metastable state is measured using mean time between failures. MTBF increases with decrease in resolution time constant.

David Li et al, 2011 [17]**:** The various design constraints for designing a metastable hardened flip flop was discussed. A metastable hardened flip flop should have optimum power and delay. The metastability power delay product (MPDP) is calculated to achieve this instead of calculating PDP.

CHAPTER 3

DESIGN METHODOLOGY

3.1 PROBLEM FORMULATION

In the Deep Sub Micron technology era, the static power dissipation is increasing with decrease in area and increase in speed. Even though when electronic equipment is not in use but is switched ON, it tends to leak enormous amount of power continuously. Here in conventional flip flop design, the total power has to be reduced in terms of static leakage power and thereby decrease the total power also. So we consider a specific part of the design to achieve this reduction in power. The inverter pairs are the targeted part of the flip flop design to reduce static leakage power.

When we employ leakage reduction technique, it utilizes high threshold voltage transistors. High threshold voltage transistors decrease the speed of the system. So the power and speed are inversely proportional to each other. So there is a need of low power at high speed for the design.

With this problem formulated, we propose a new flip flop design which employs sleepy stack inverter pair for reduction in total power in terms of static leakage power at high speed with moderate noise.

3.2 OBJECTIVE

- To design T flip flop, SR flip flop and JK flip flop using conventional D flip flop for the performing functions like toggling, set, reset etc..
- To design a Low power Hybrid D Flip Flop using “Sleepy stack inverter pairs” to achieve less leakage power at lower nanometer technology (90nm) in consideration with following parameters:
    - Low leakage power
    - Low total power
    - Maintaining the same speed
    - Low PDP
    - Moderate noise

- To design T flip flop, SR flip flop and JK flip flop using proposed D flip flop for the function of toggling, set reset etc and compare them with conventional flip flops.

3.3 DESIGN METHODOLOGY

To achieve the above mentioned objective a proper channelized design procedure and analysis have to be done. So the design gets started with front end design of schematic and ends up with the back end design of layout with simulations. The step by step procedure is depicted in the flow chart given in Fig 3.3.

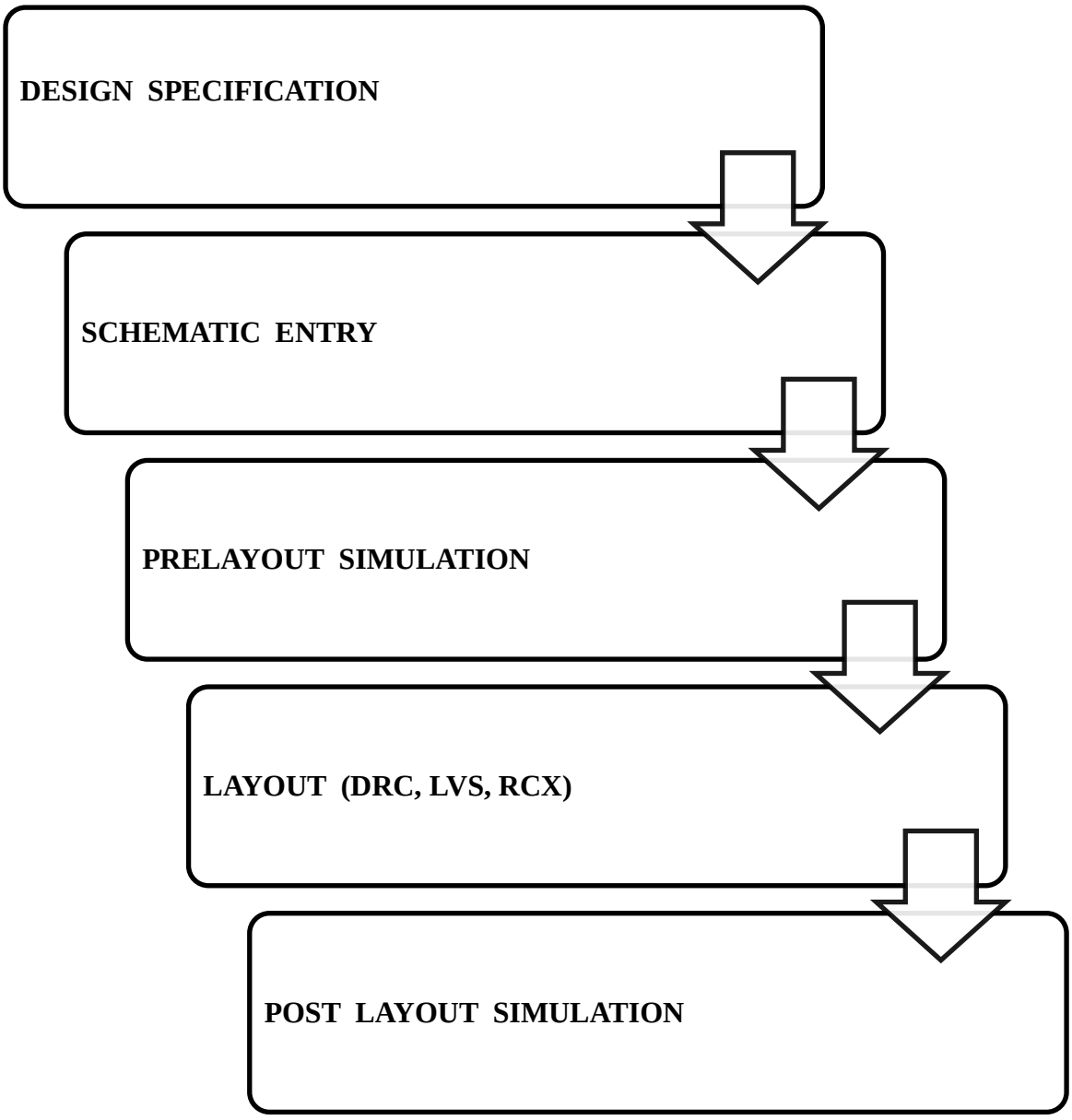

Fig 3.1 Design Flow

The first step toward the design flow of the design is the design specification. Specify the required parameters to be taken into consideration while designing. Specify the required speed and power and maximum possible frequency range. With these design specifications, the design is implemented in cadence spectre 90nm tool. The schematic is drawn. The pre-layout simulation is performed using ADE window. Transient analysis and noise analysis were performed. The following parameters were calculated using the calculator in cadence tool : Total Power, Leakage power, Delay, Noise spectral density. Then the layout is drawn using cadence virtuoso 90nm tool LAYOUT XL window. The DRC rules were checked out. The LVS is performed and it states that Schematic and LVS matches. Then RC parameters were extracted using RCX in cadence assura 90nm tool. With this the test circuit is post simulated to check if it matches the pre-layout simulation results.

3.4 SIMULATION TOOL

Cadence Spectre 90nm was used to design the schematic and analyze various simulations. It has pmos_hvt and nmos_hvt in gpdk90 library. These two transistors act as high voltage transistors in the proposed design. They have an additional Phvt and Nhvt layer mask over source and drain of pmos and nmos to increase the threshold voltage of the transistor. Transient analysis and Noise analysis were done in ADE environment. The output waveform and maximum frequency is obtained through transient analysis. The noise spectral density for varying frequency is analyzed using noise analysis. The parameters calculated through the tool calculator were total power, delay, power delay product and leakage power.

Cadence Virtuoso 90nm was used to draw the layout of the design. The pmos_hvt and nmos_hvt transitor layout do not have integrated option for body type due to DRC rules. The DRC rules were checked and layout vs schematic (LVS) were matched.

Cadence Assura 90nm was used to generate the av_extracted file of the design. The RCX option was used to generated this file.

CHAPTER 4

DESIGN IMPLEMENTATION

4.1 CONVENTIONAL D FLIP FLOP DESIGN (DDFF)

DDFF is the latest highly efficient hybrid flip flop. Fig 4.1 shows the schematic of DDFF. It has the dynamic design style at its input side and static design style at its output side. At the input side, dynamic logic style is used with a PMOS and 3 NMOS transistors connected in series. It has two dynamic logic nodes [8] X1B and X2 to reduce dynamic power dissipation. The output is designed using static design style. The inverter pairs INV1-2 and INV3-4 are designed using static CMOS design which is used for latching at evaluation and pre-charge phases. As these inverter pairs are under operation throughout the two phases of the flip flop, it tends to undergo larger run time leakage current. Not only run time leakage, even when the flip flop is not at work that is at standby mode it tends to leak current. This makes the design to consume unnecessarily more power when technology shrinks down to 90nm and below.

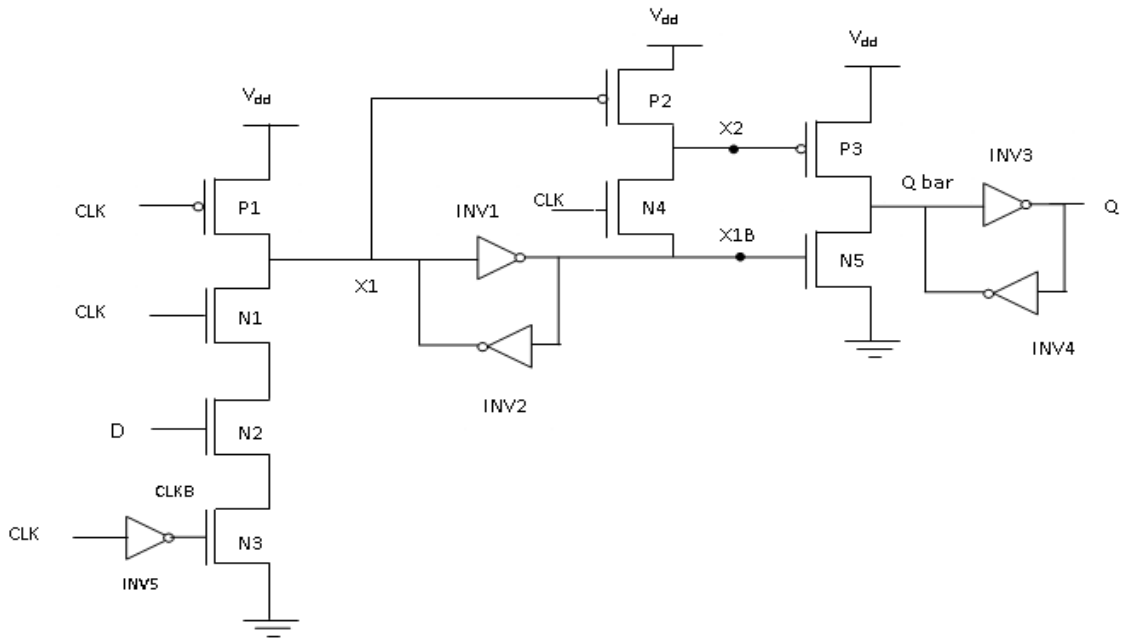

Fig 4.1 Schematic of Conventional D flip flop (DDFF)

The static CMOS inverter consumes more leakage power at standby mode and at active mode. Though the structure is simple with very less area and high speed,

when it is used in deep submicron technologies the sub threshold current is maximum. This increases the leakage power and total power.

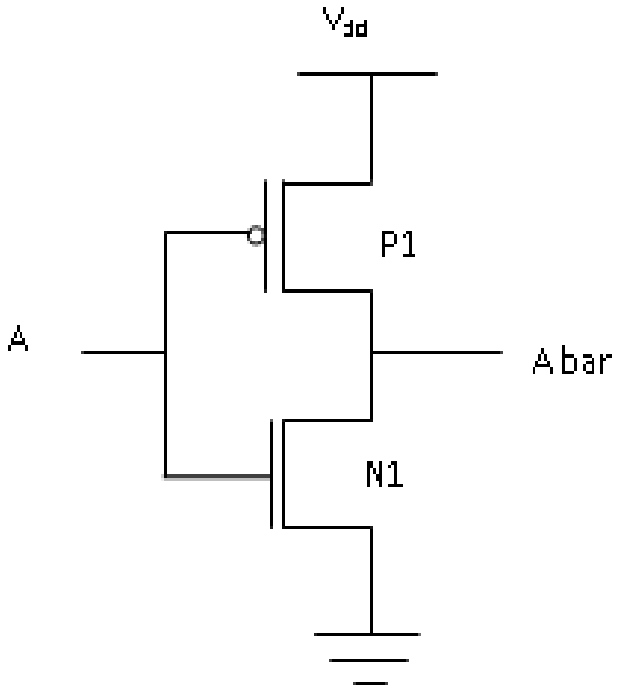

Fig 4.2 Schematic of static CMOS inverter

4.1.1 OPERATION

It operates in two phases: 1) Evaluation Phase 2) Pre-charge phase.

1) *Evaluation phase[8]*

In this phase CLK=1. If the input D=1, then X1 node is discharged through the path N1,N2,N3. The logic value at X1 will be zero. This latching occurs only during 1-1 overlap of CLK and CLKB[4],[5],[8]. The logic value 0 is maintained at X1 by the inverter pair INV1 and INV2 till the evaluation phase gets over. The node X1B is high throughout the evaluation phase and Q bar discharges to 0. The output Q is maintained by the inverter pair INV3 and INV4 till next evaluation phase occurs. The node X2 is high when D is high throughout the evaluation phase. If the input D=0, then X1 node will be at logic 1 and X2 node will be in logic low. Q bar will be charged through P2. The node X2 remains low till the end of the evaluation phase.

2) *Precharge phase[8]*.

In this phase CLK=0 and D can be either 1 or 0. It can also be called as holding mode. The X1 node remains high and X1B will be low. N1 stops the entry of next

value of D until the end of pre-charge phase. So the previous output will be held till the next evaluation phase occurs.

This design has negative setup time and positive hold time[8]. It has short transparency period which is due to 1-1 overlap of CLK and CLKB[8]. This overlap eliminates race through problem. Here the inverter pair INV1,INV2 and INV3,INV4 were designed using normal static CMOS style. As these inverter pair is under operation throughout the two phases of the flip flop, it tends to undergo larger run time leakage current. This makes the design to consume unnecessary power when technology shrinks down to 90nm and below. The schematic implementation of the above design in cadence spectre 90nm is shown in Fig 4.1 below.

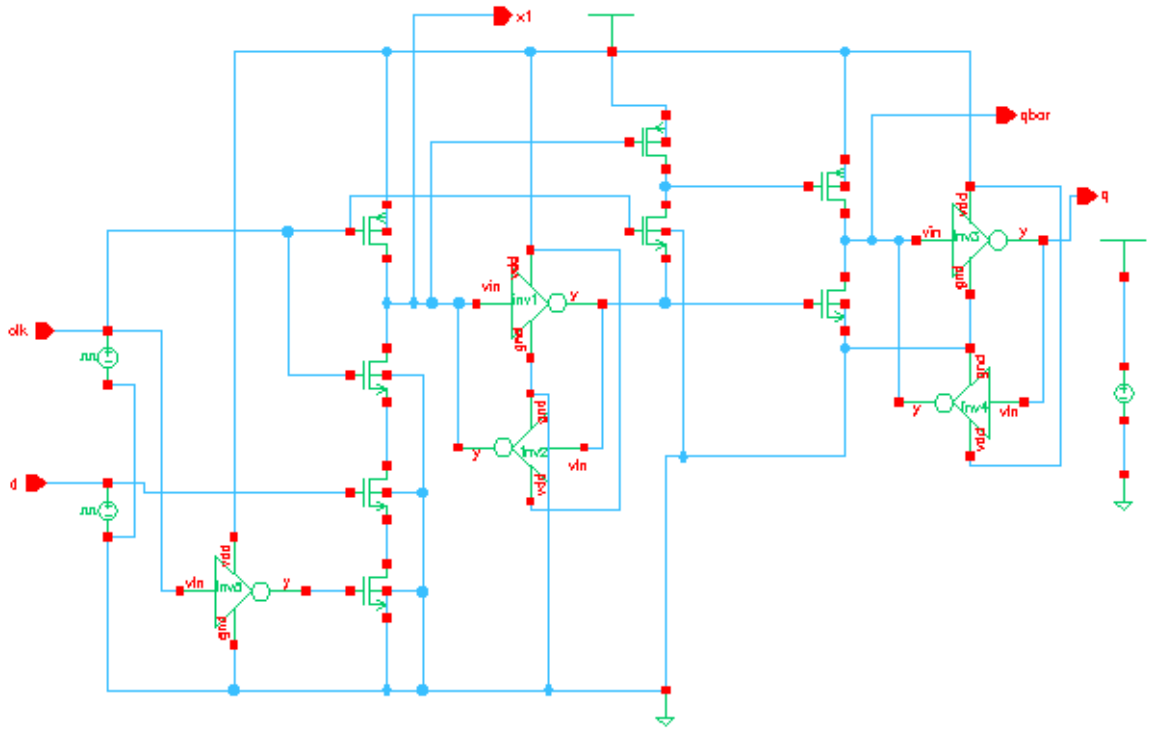

Fig 4.3 Implemented Schematic of Conventional D flip flop (DDFF) in cadence spectre 90nm

4.1.2 TRANSIENT ANALYSIS

The transient analysis of the conventional flip flop is shown in Fig 4.3 below. It works at maximum clock frequency range of 2GHz. The time period of the data d is taken as 8.5ns. When the clock is positive edge triggered, the data is latched and written at the output. It holds this input state at its output q till the end of the clock period.

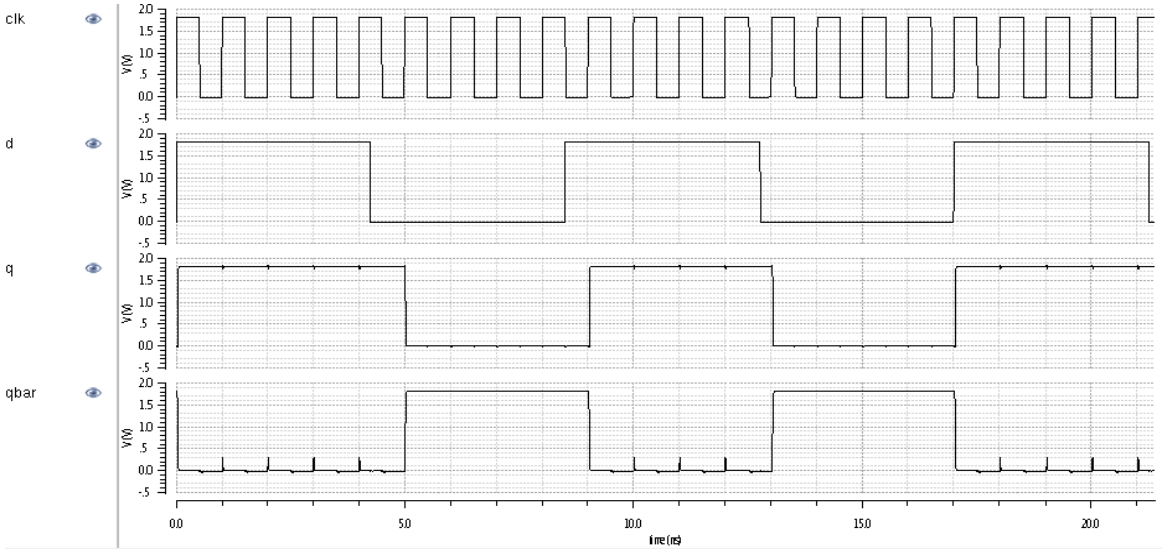

Fig 4.4 Transient analysis of conventional D flip flop (DDFF).

4.1.3 LAYOUT

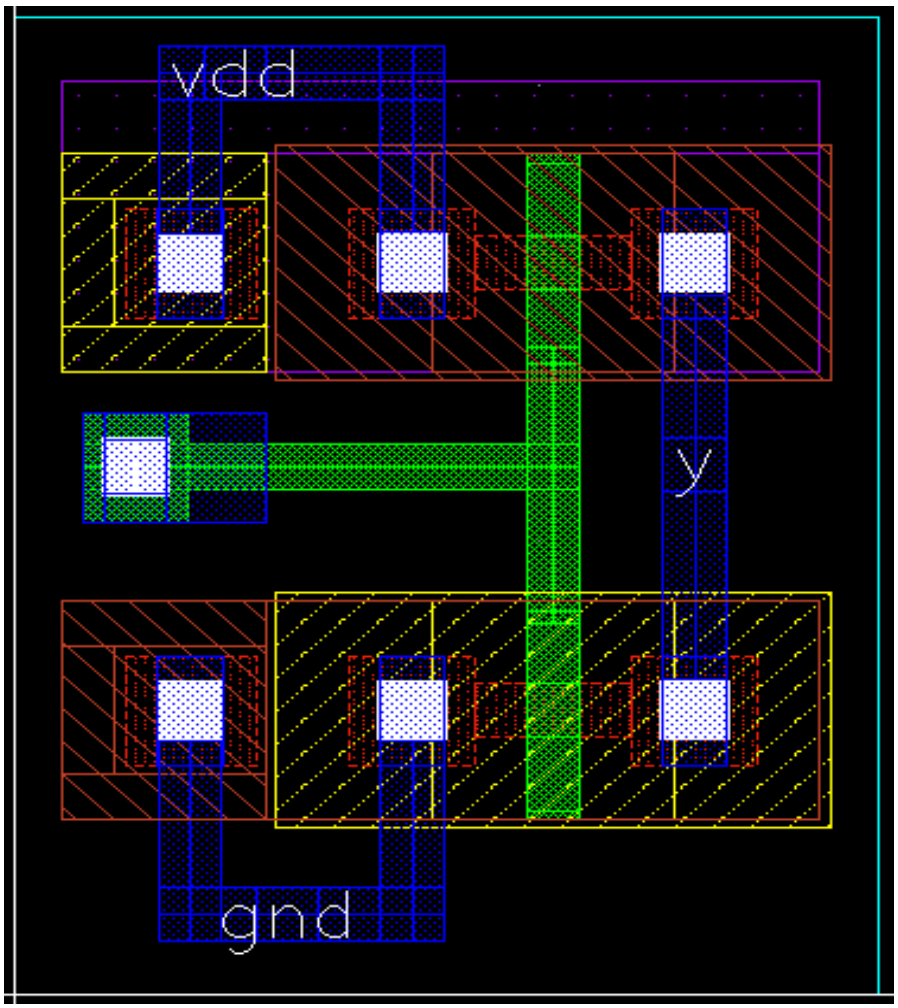

Fig 4.5 Layout of conventional static CMOS inverter

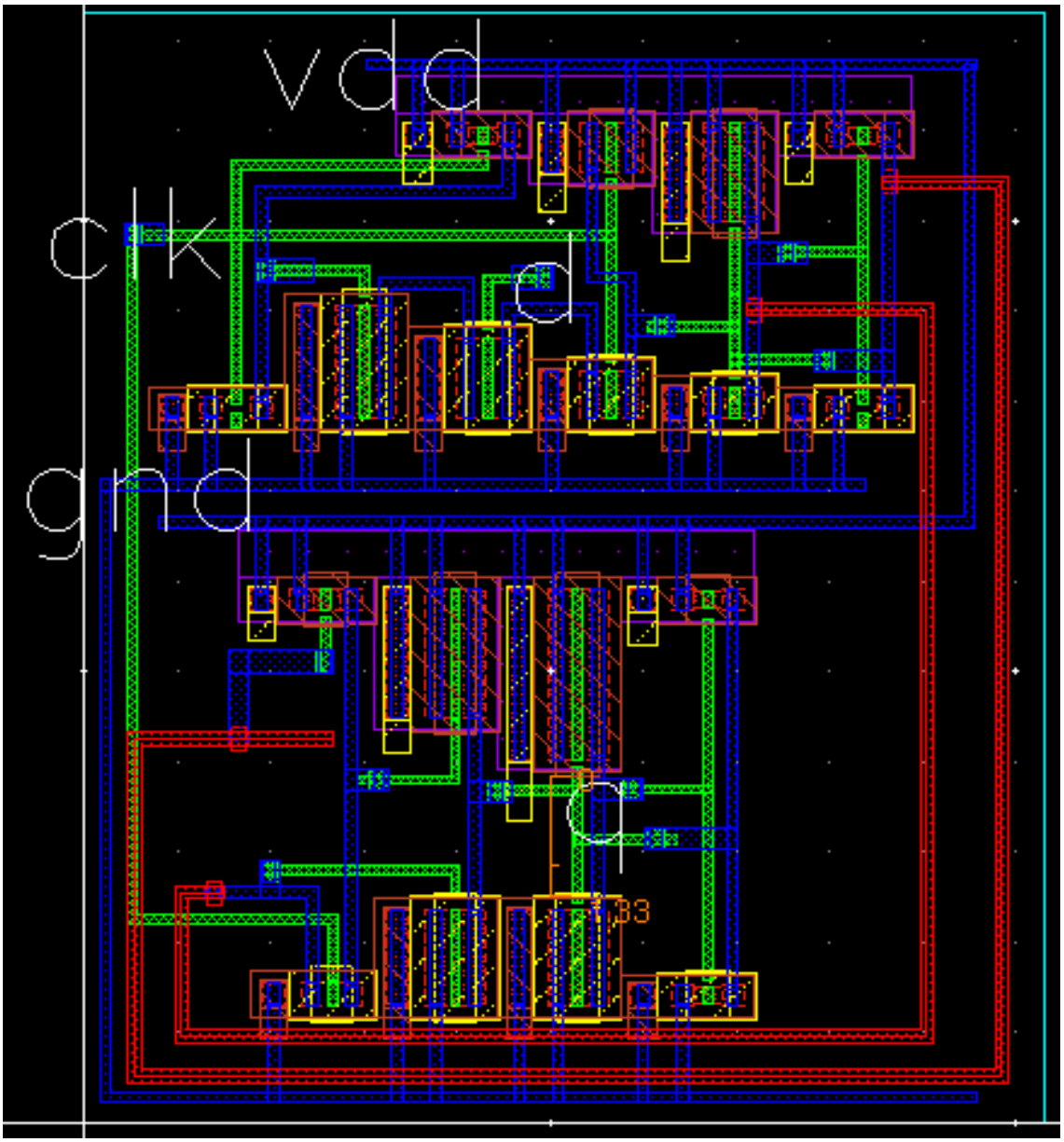

Fig 4.6 Layout of conventional D flip flop (DDFF)

The layout of the conventional static CMOS inverter and conventional D flip flop (DDFF) is shown in Fig 4.4 and Fig 4.5. In both the layouts, the transistors NMOS and PMOS have the detached body type. The design of D flip flop is planned in such a way that two rows of PMOS and NMOS transistors are placed for better routing purposes. The supply and ground rail is placed as L shaped structure above and below NMOS and PMOS transistors. The DRC check has no errors. The layout and schematic got matched. The RCX was performed and av_extracted file containing capacitance and resistors were generated.

4.2 CONVENTIONAL T FLIP FLOP DESIGN

The T flip flop was designed using conventional D flip flop. An XOR gate is placed at the input of N2 NMOS transistor. This is designed by using the excitation table and characteristic equation of T flip flop as given in Table 1.2 of chapter 1.

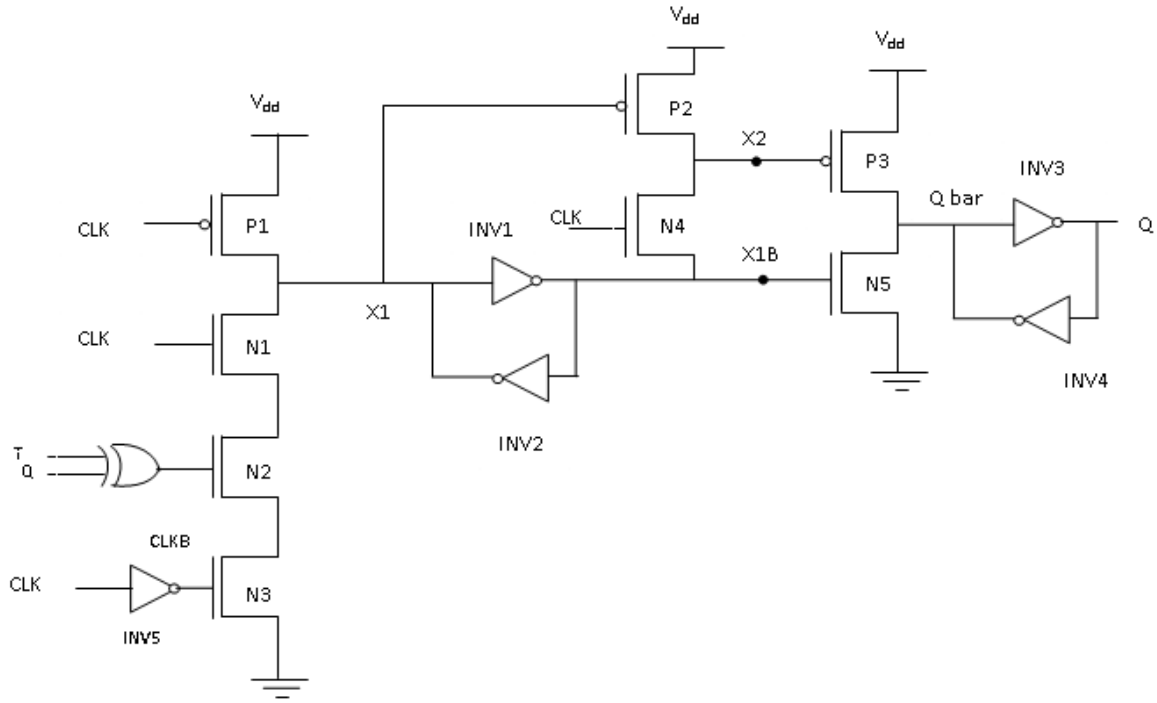

Fig 4.7 Schematic of conventional T flip flop

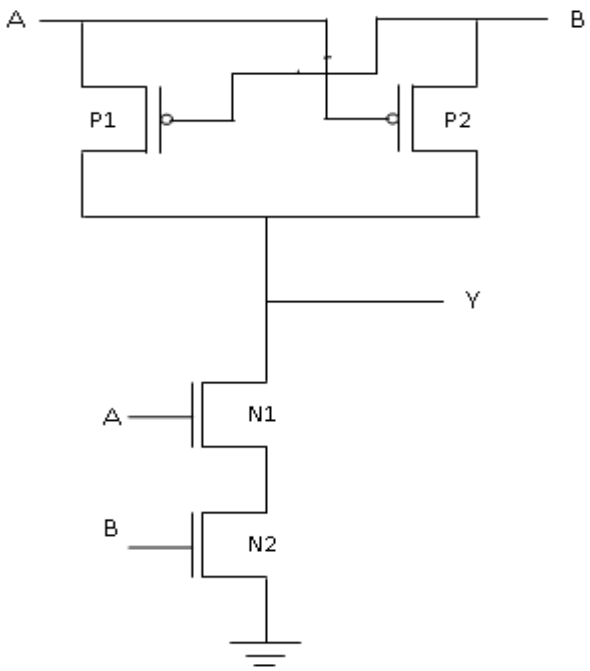

Fig 4.8 Schematic of XOR gate using PTL

4.2.1 OPERATION

The inputs of an XOR gate are ‘t’ and ‘q’ where is given as feedback to the XOR gate. Here we designed the XOR gate using PTL logic to reduce area. Though PTL logic does not give strong 0 and strong 1, the two dynamic nodes helps in getting the strong 0 or 1 at its output. So it does not distort the output of the flip flop. When clock is positive edge triggered with input t=1, then the output toggles. If the input t=0, then the output maintains the previous state. It acts as an XOR gate. It has greater dynamic power dissipation due to toggling.

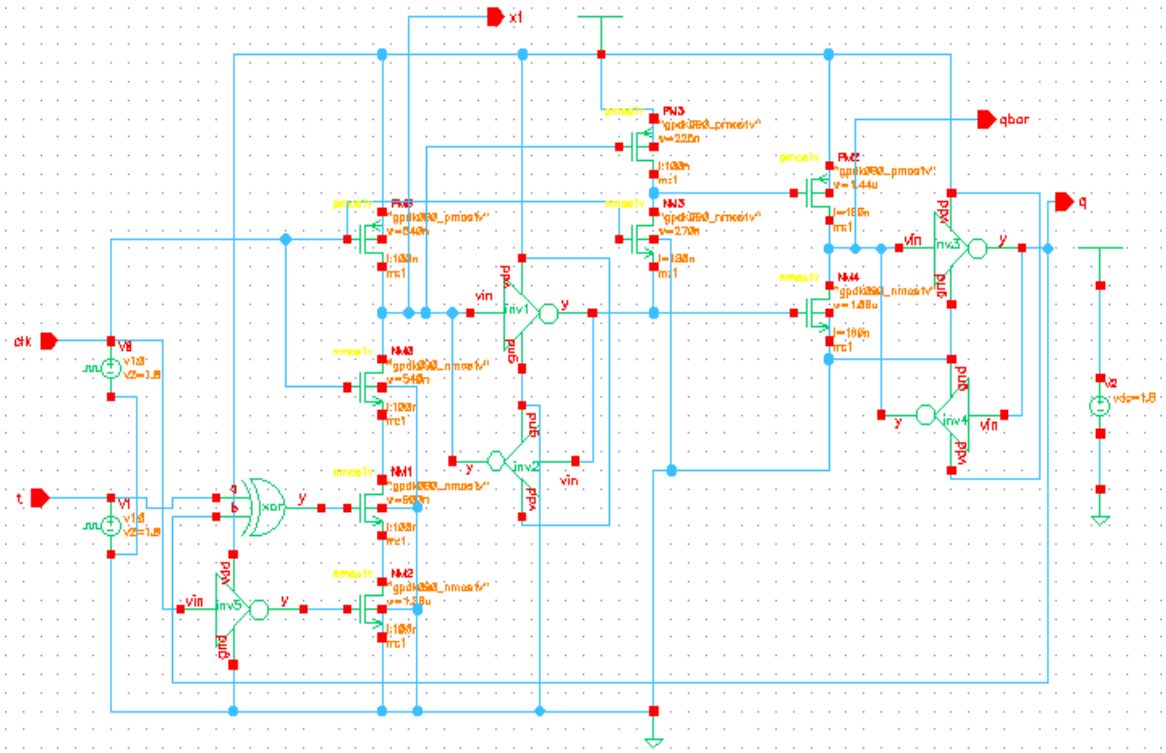

Fig 4.9 Implemented Schematic of Conventional T flip flop in cadence spectre 90nm

4.2.2 TRANSIENT ANALYSIS

The transient analysis of the conventional T flip flop is shown in Fig 4.8 below. It works at maximum clock frequency range of 2GHz. The time period of the data T is taken as 8.5ns. When the clock is positive edge triggered, the data is latched and written at the output. It holds this input state at its output q till the end of the clock period. The output gets toggled when input t=1 and holds the previous state when input t=0 if clock is positive edged triggered.

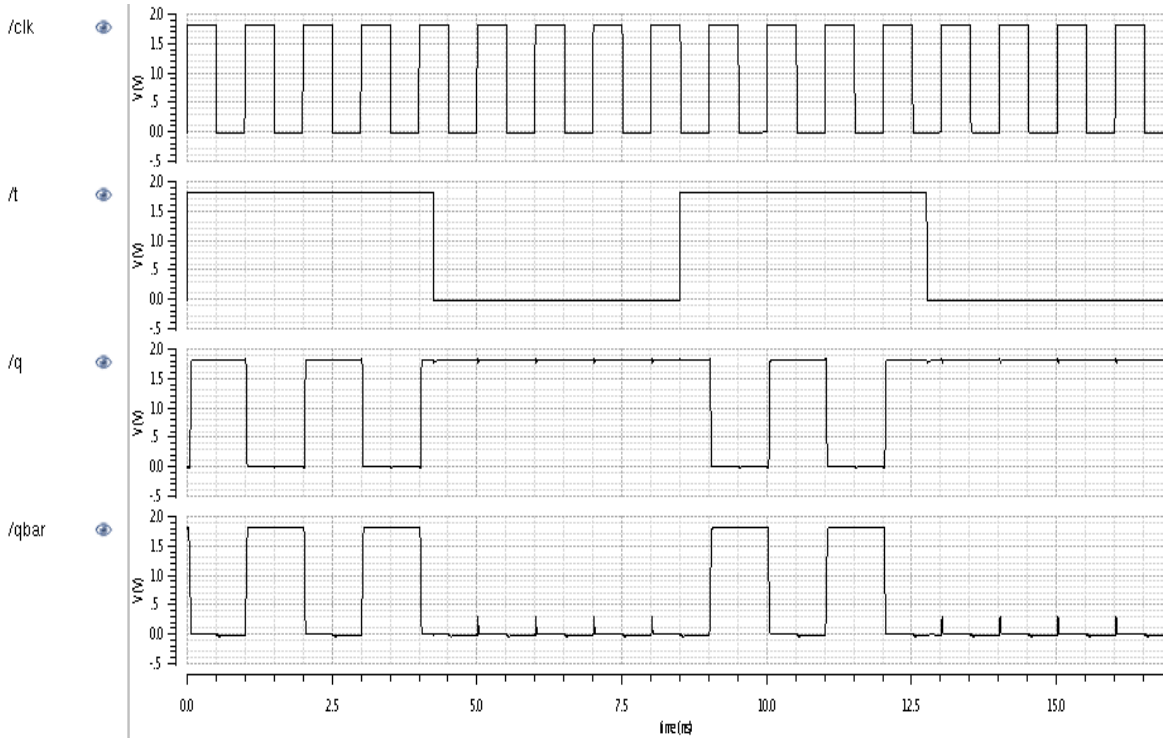

Fig 4.10 Transient analysis of conventional T flip flop.

4.3 CONVENTIONAL SR FLIP FLOP DESIGN

The SR flip flop was designed using conventional D flip flop. An S+RbarQ block is placed at the input of N2 NMOS transistor. This is designed by using the excitation table and characteristic equation of SR flip flop as given in Table 1.3 of chapter 1.

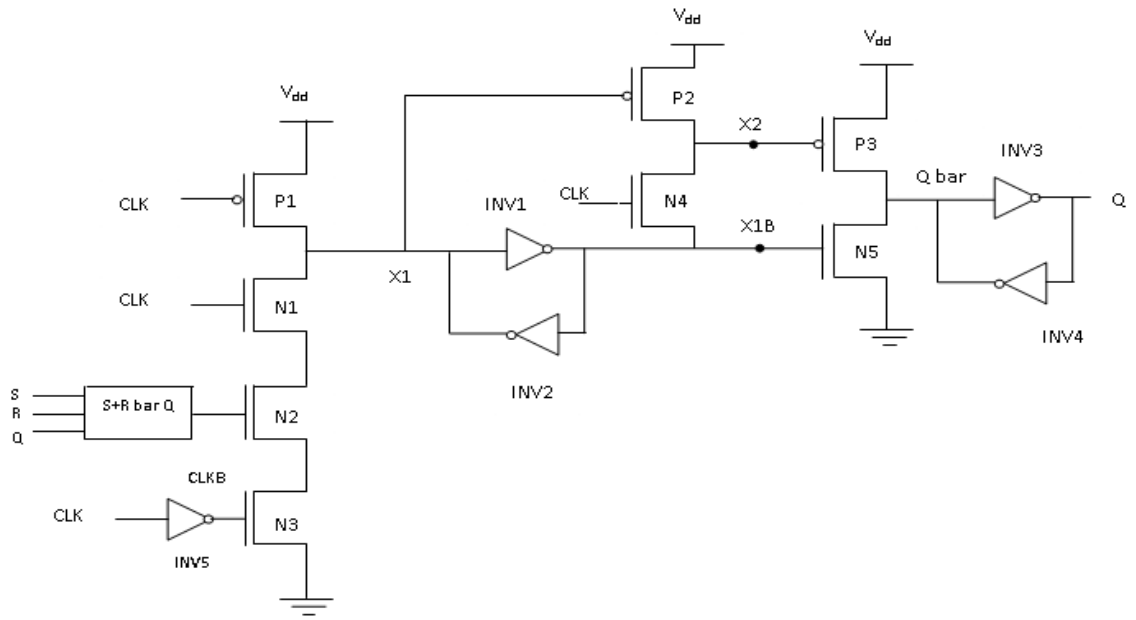

Fig 4.11 Schematic of conventional SR flip flop

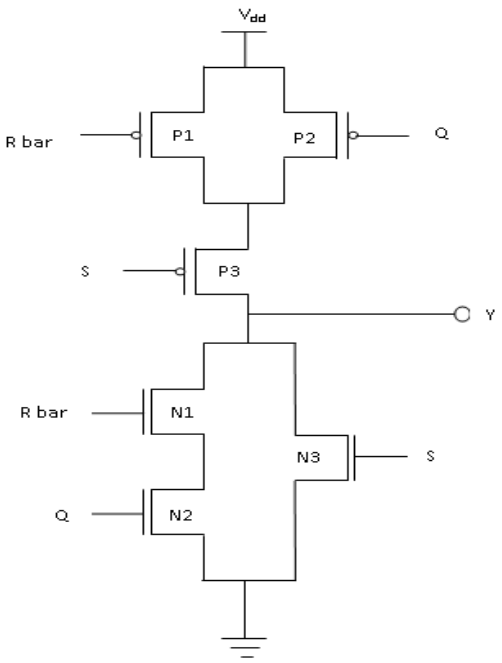

Fig 4.12 Schematic of S+RbarQ block

4.3.1 OPERATION

The inputs of S+RbarQ block are ‘S’, ‘R’ and ‘Q’ where Q is given as feedback to the XOR gate. Here we designed the S+RbarQ block using static CMOS technique. When clock is positive edge triggered with input S=1 and R=0, then the output is set. If the input R=1 and S=0 then the output is reset. If both S and R are equal to 0, there is no change. If both are 1, it is an undefined state.

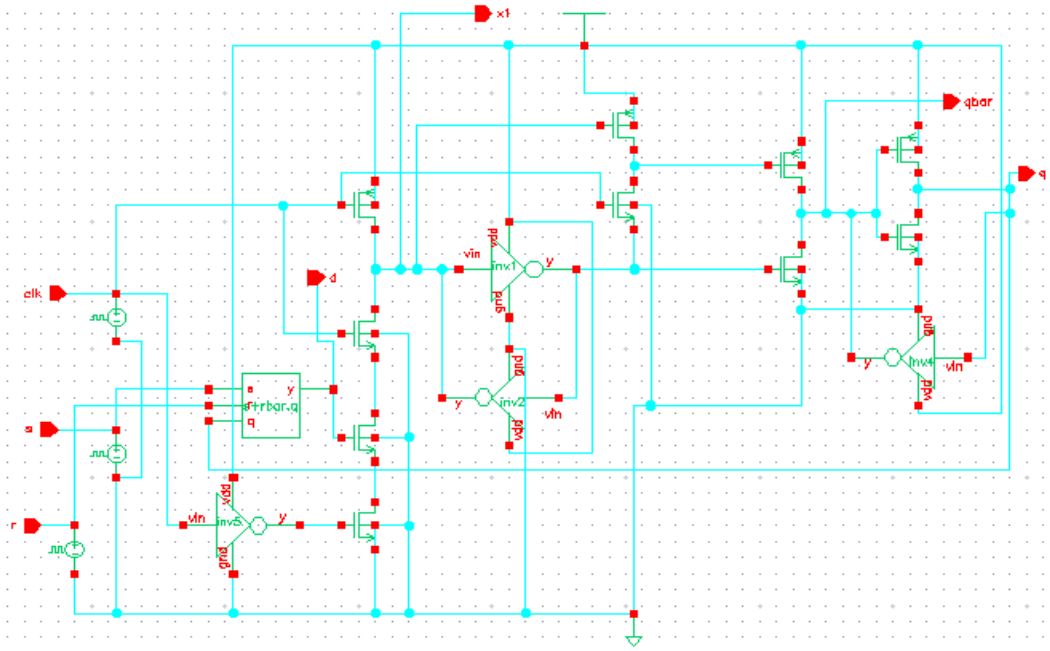

Fig 4.13 Implemented Schematic of Conventional SR flip flop in cadence spectre 90nm

4.3.2 TRANSIENT ANALYSIS

The transient analysis of the conventional SR flip flop is shown in Fig 4.12 below. It works at maximum clock frequency range of 2GHz. The time period of the data S and R are taken as 8.5ns and 4.5 ns. When the clock is positive edge triggered, the data is latched and written at the output. When clock is positive edge triggered with input S=1 and R=0, then the output is set. If the input R=1 and S=0 then the output is reset. If both S and R are equal to 0, there is no change.

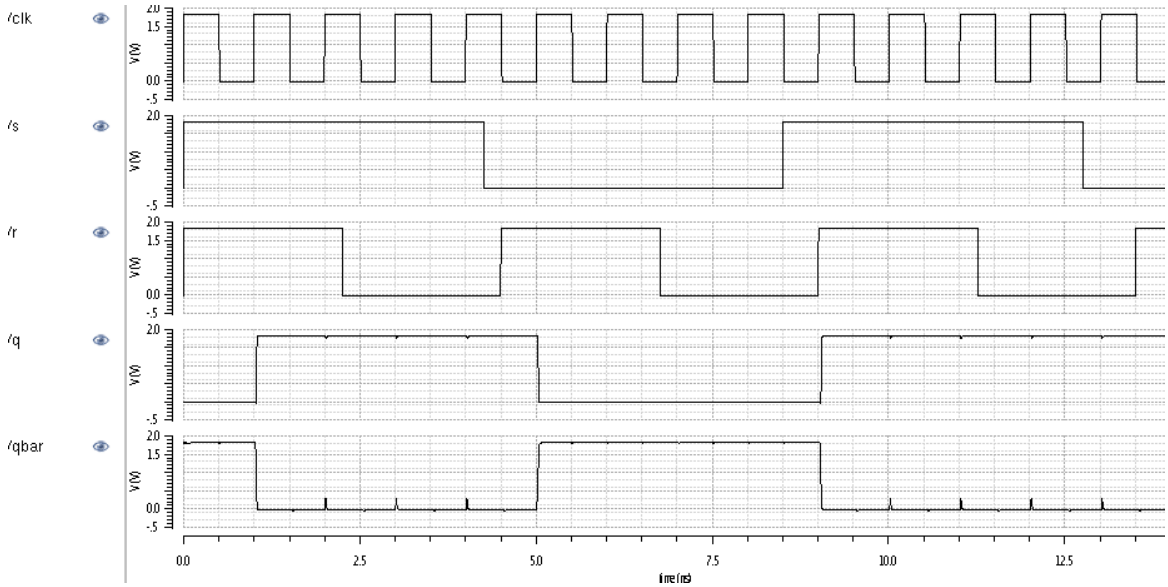

Fig 4.14 Transient analysis of conventional SR flip flop.

4.4 CONVENTIONAL JK FLIP FLOP DESIGN

The JK flip flop was designed using conventional D flip flop. A MUX is placed at the input of N2 NMOS transistor. This is designed by using the excitation table and characteristic equation of SR flip flop as given in Table 1.3 of chapter 1.

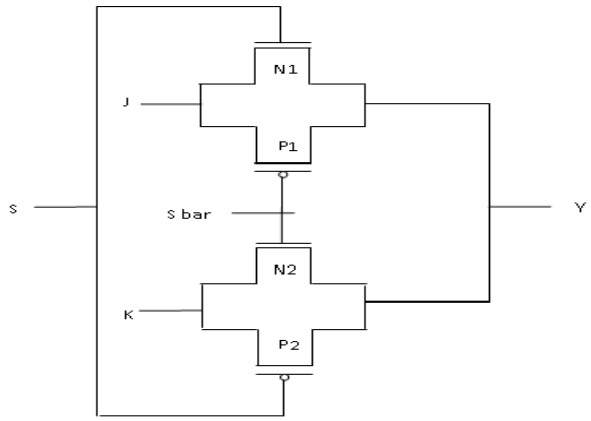

Fig 4.15 Schematic of Multiplexer

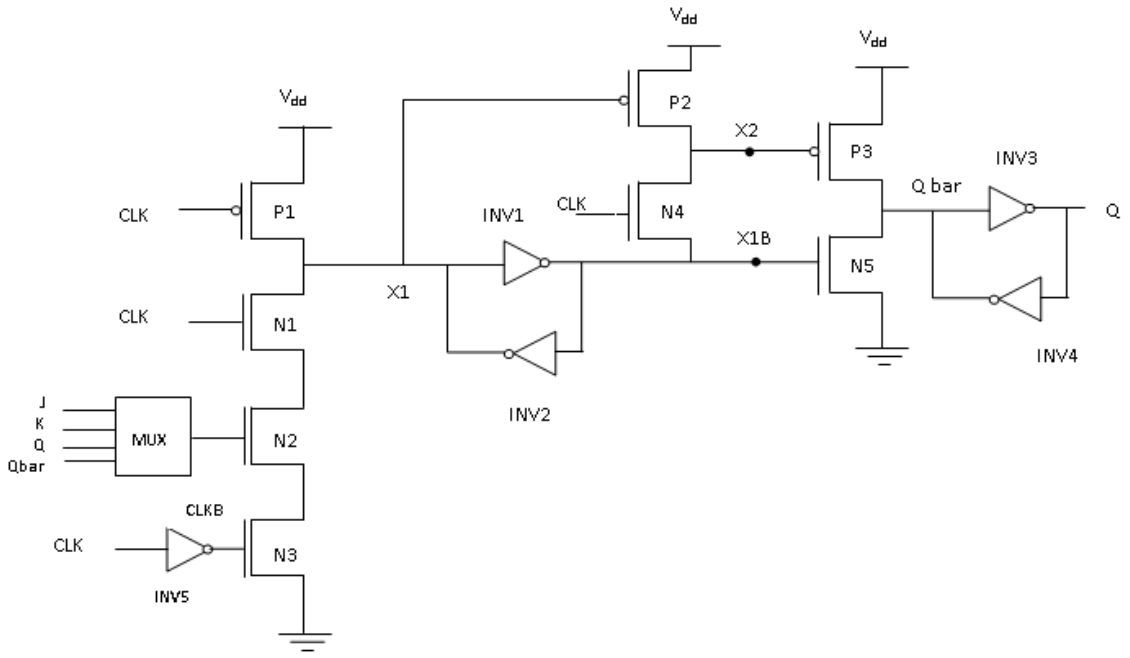

Fig 4.16 Schematic of conventional JK flip flop

4.4.1 OPERATION

The inputs of mux block are 'J', 'K' and 'Q' where Q is given as feedback to the mux. Here we designed the MUX block using transmission gate technique. When clock is positive edge triggered with input J=1 and K=0, then the output is set. If the input J=1 and K=0 then the output is reset. If both J and K are equal to 0, there is no change. If both are 1, it toggles.

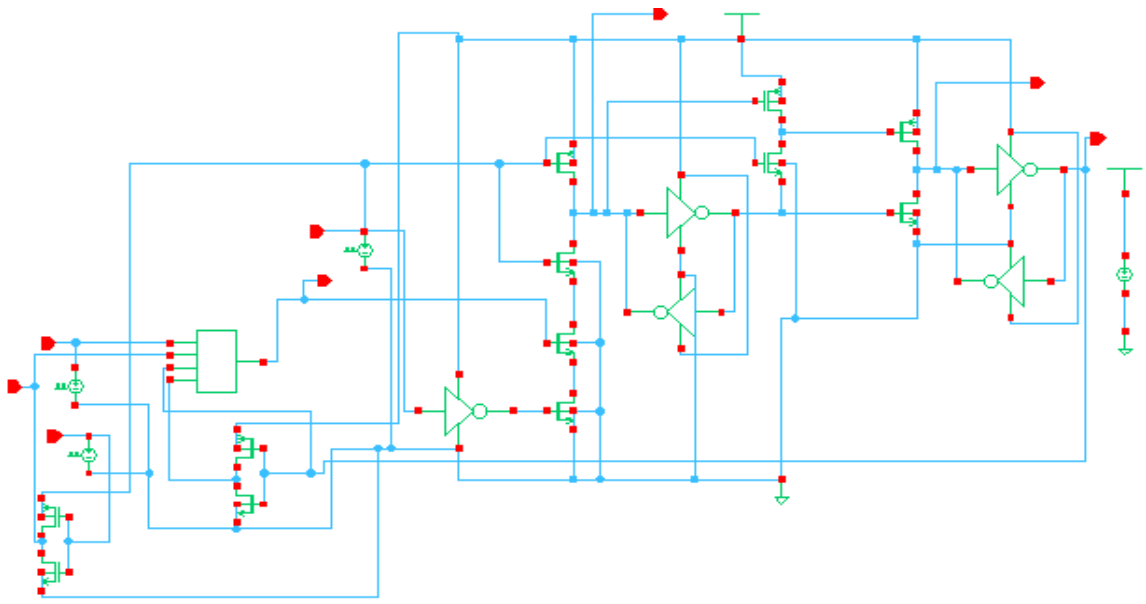

Fig 4.17 Implemented Schematic of Conventional JK flip flop in cadence spectre 90nm

4.4.2 TRANSIENT ANALYSIS

The transient analysis of the conventional JK flip flop is shown in Fig 4.16 below. It works at maximum clock frequency range of 2GHz. The time period of the data J and K are taken as 8.5ns and 4.5 ns. When the clock is positive edge triggered, the data is latched and written at the output. When clock is positive edge triggered with input J=1 and K=0, then the output is set. If the input J=1 and K=0 then the output is reset. If both J and K are equal to 0, there is toggles.

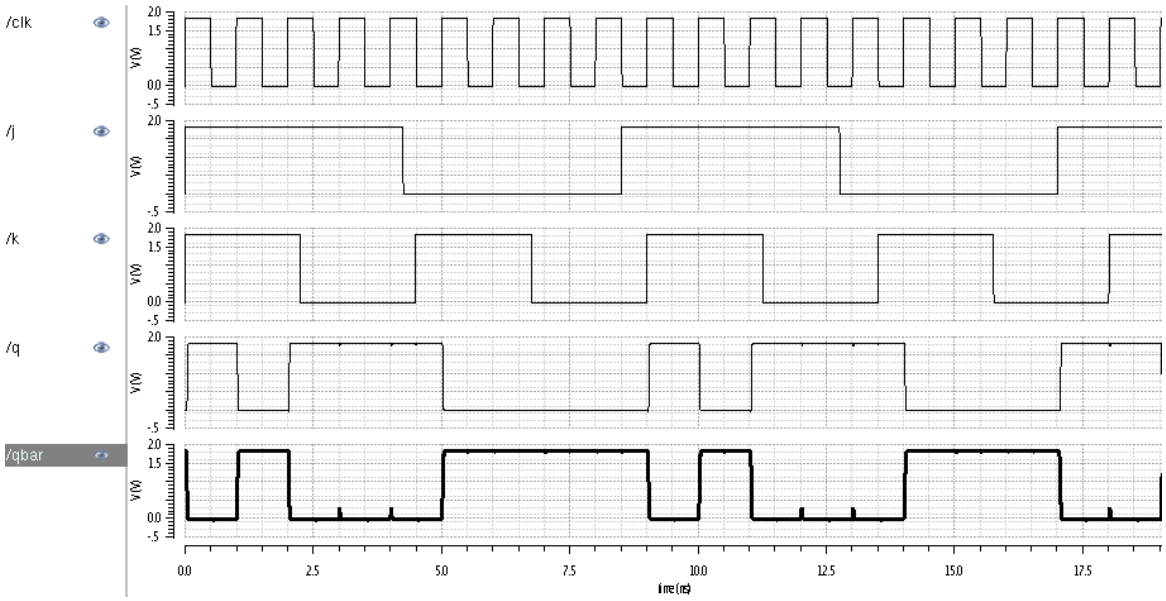

Fig 4.18 Transient analysis of conventional JK flip flop.

4.5 PROPOSED D FLIP FLOP DESIGN

The proposed flip flop is highly efficient low power hybrid flip flop. Fig 4.17 shows the proposed flip flop. At the input side, dynamic logic style is used with a PMOS and 3 NMOS transistors connected in series. It has two dynamic logic nodes X1B and X2. The output is designed using static design style. In the proposed flip flop architecture the inverter pairs INV1-2 and INV3-4 are designed using leakage power reduction technique known as sleepy stack technique. The static CMOS inverters in conventional DDFF is replaced by sleepy stack inverters because as feature size scales down below 0.1u, leakage power gets increased. When a static CMOS inverter is used in low feature size technology, the supply voltage gets reduced which in turn reduces the threshold voltage[6]. The transistor used were low threshold voltage one. So there is greater risk of leakage current in this case. Short channel length and change in gate length

also pave way for higher leakage. This sleepy stack technique is the combination of sleep transistor technique and forced stack technique. It uses high threshold voltage transistors and stack effect to reduce the leakage power [9]. The sub-threshold current is reduced by stack effect and the high voltage transistors connected to V_{dd} and gnd. The high threshold voltage transistors are reverse body biased in circuit level to increase its threshold voltage. In device level, a layer of phvt and nhvt is present in source and drain of PMOS and NMOS train to reduce the leakage from source to drain.

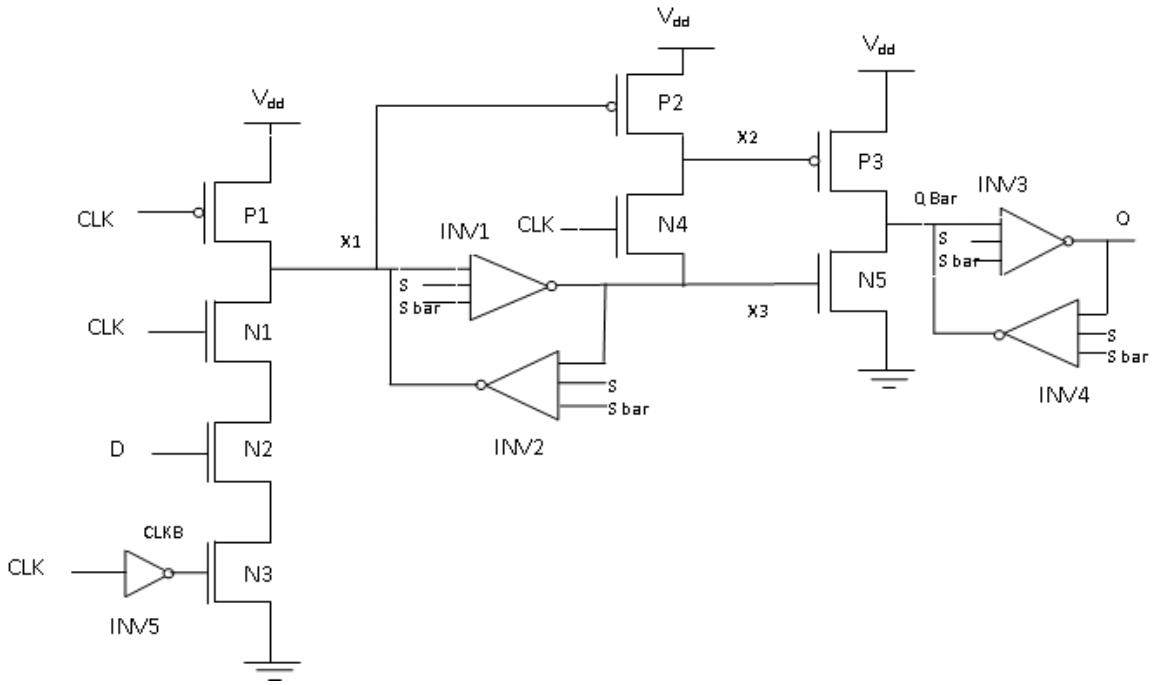

Fig 4.19 Schematic of proposed D flip flop

4.5.1 OPERATION

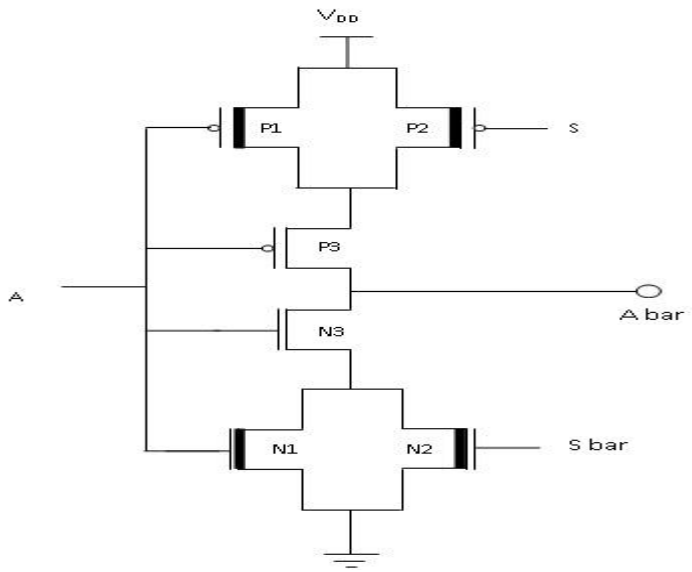

Fig 4.20 Schematic of sleepy stack inverter

The sleepy stack inverter is shown in the fig.4.18. P1,P2, N1,N2 are high threshold voltage transistors. P3 and N3 are low threshold voltage transistors. P2 and N2 are sleep transistors. It operates on two modes. 1) active mode 2) sleep mode

1) Active mode

In active mode , S=0 and Sbar=1. The sleep transistors are switched ON throughout this mode. It has faster switching time. As sleep transistors are switched on throughout, it passes the logic values from source to drain and directly into the low V_{th} transistors regardless of the status of transistors which are parallel to sleep transistors[9].

2) Sleep mode

In sleep mode, S=1 and Sbar=0. The sleep transistors are switched OFF. Though they are switched OFF, the transistors parallel to sleep transistors helps in maintaining exact logic state of the design. Reduction in leakage power is achieved by two ways. Firstly high V_{th} transistors parallel to sleep transistors are used to block the leakage current. Secondly by stack effect created by P1,P3 and N1,N3 transistors. When two or more transistor which are stacked together are turned off simultaneously, there is greater reduction in leakage current. This effect is called as stack effect. Suppose when A=1, the stacked NMOS transistors N1,N3 are switched ON and stacked PMOS transistors P1,P3 are switched OFF. Thus the stacked PMOS do not allow any leakage current to pass through. Though there is large leakage power reduction, area is a trade off[9].

When this sleepy stack inverter pair is used in the flip flop, the overall leakage power reduction of the flip flop can be achieved by operating the flip flop in sleep mode. The total power is also reduced which can be obtained by running the flip flop in active mode. This proposed flip flop also operates as like DDFF in evaluation and precharge phase. The latching of input takes place at evaluation phase and holding of the output takes place in prechage phase. The overlapping period (T_{ov}) of the flip flop is set as 61ps with supply voltage of 1.8V. Hold time of logic 0 (T_{hold0}) is observed to be 24ps. Hold time of logic 1 (T_{hold1}) is observed to be 35ps. The race around problem is overcome by the 1-1 overlap of CLK and CLKB.

4.5.2 TRANSIENT ANALYSIS

The transient analysis of the proposed D flip flop is shown in Fig 4.19 below. It works at maximum clock frequency range of 1GHz. The time period of the data d is taken as 8.5ns. When the clock is positive edge triggered, the data is latched and

written at the output. It holds this input state at its output q till the end of the clock period. When S=1 and Sbar=0, it gives reduced leakage power reduction at standby mode without wakeup cost.

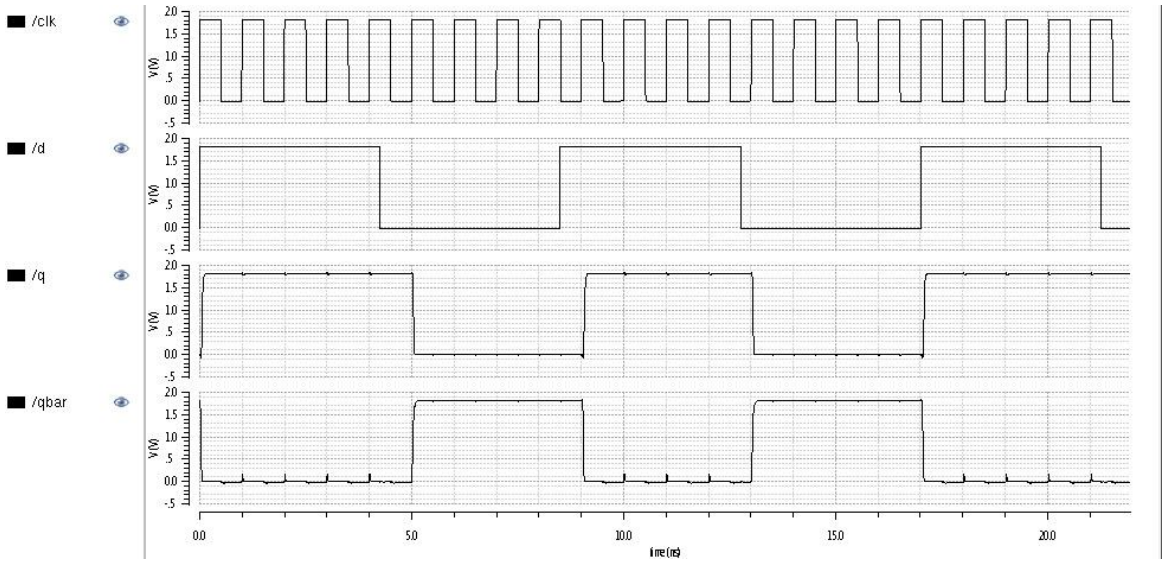

Fig 4.21 Transient analysis of proposed D flip flop.

4.5.3 LAYOUT

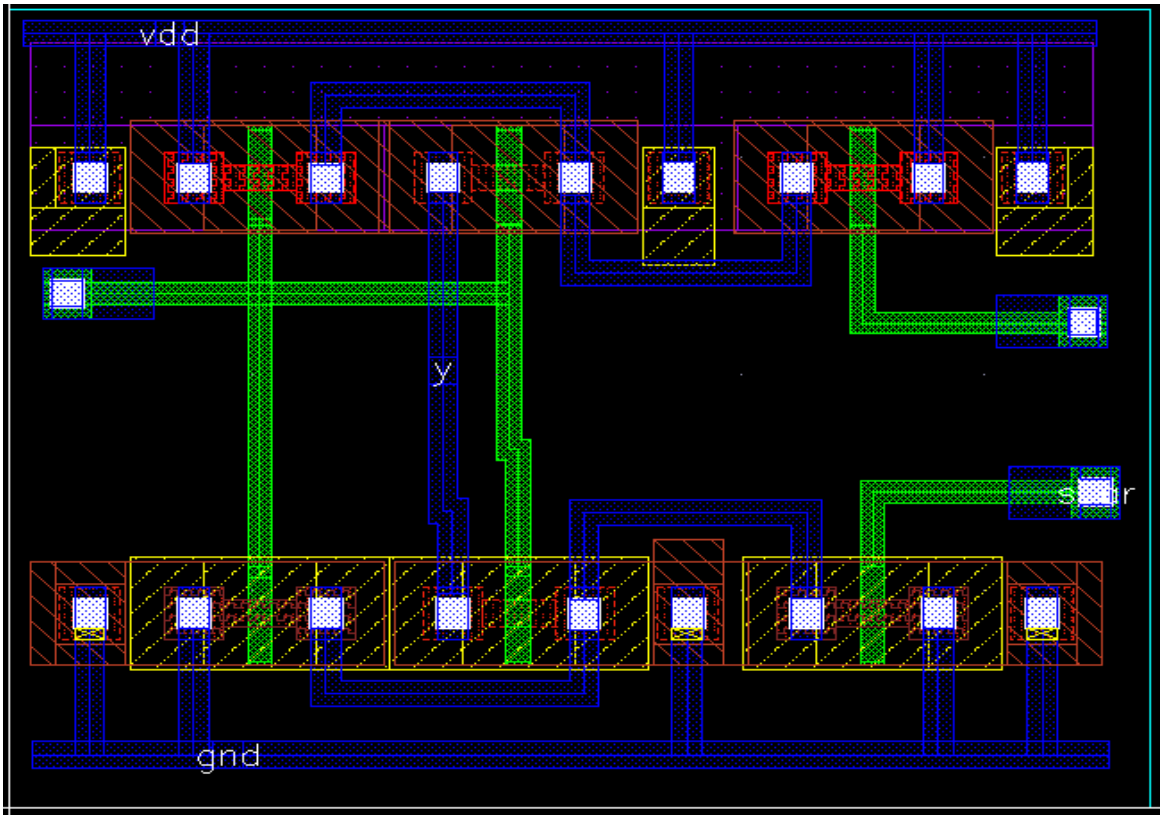

Fig 4.22 Layout of sleepy stack inverter

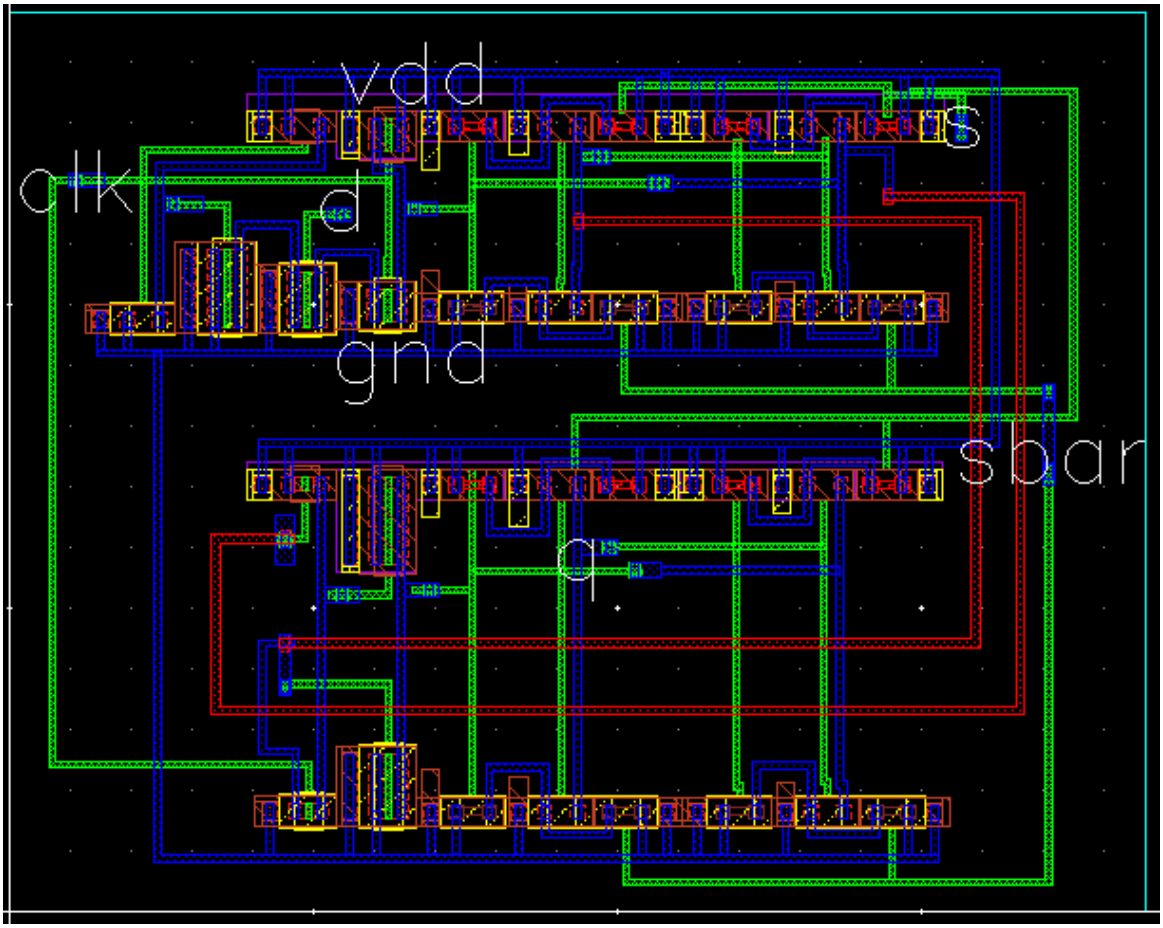

Fig 4.23 Layout of proposed flip flop

The layout of the sleepy stack inverter and proposed D flip flop are shown in Fig 4.19 and Fig 4.20. In both the layouts, the transistors NMOS and PMOS have the detached body type. The design of D flip flop is planned in such a way that two rows of PMOS and NMOS transistors are placed for better routing purposes. The supply and ground rail is placed as L shaped structure above and below NMOS and PMOS transistors. The DRC check has no errors. The layout and schematic got matched. The RCX was performed and av_extracted file containing capacitance and resistors were generated. The area of proposed flip flop is greater than conventional one which is the trade off.

4.6 PROPOSED T FLIP FLOP DESIGN

The proposed T flip flop was designed using proposed D flip flop. The XOR gate designed for conventional is used here also. It works at active and sleep mode. The remaining operation of the flip flop is same as conventional one working at

evaluation and precharge phase. It operates at low power than conventional T flip flop.The schematic and transient analysis is shown below.

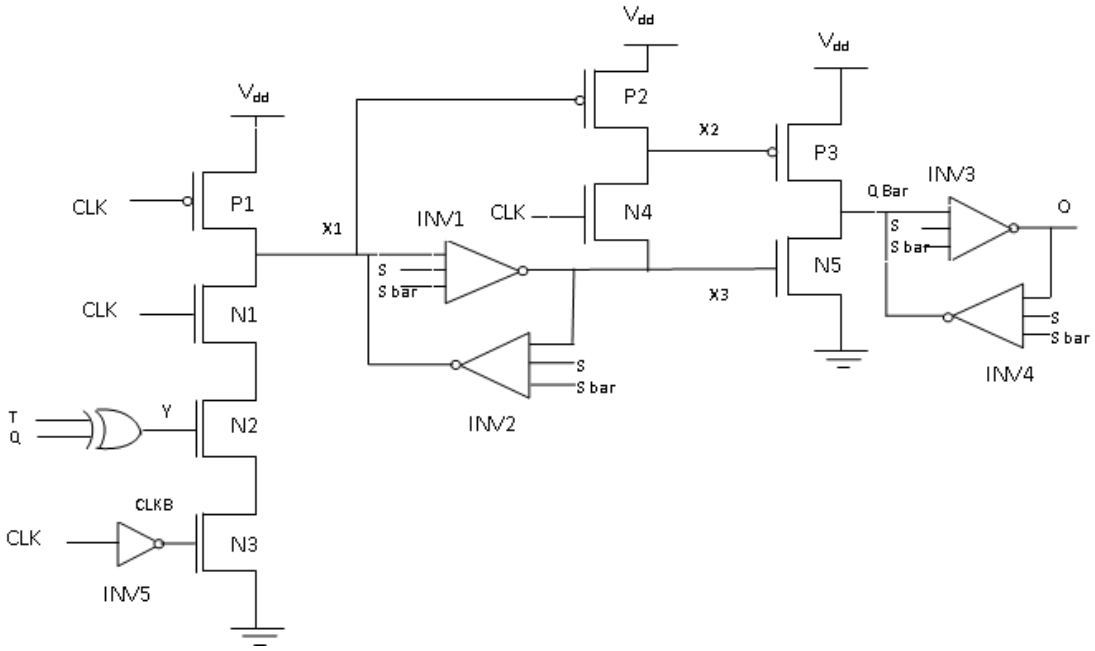

Fig 4.24 Schematic of proposed T flip flop

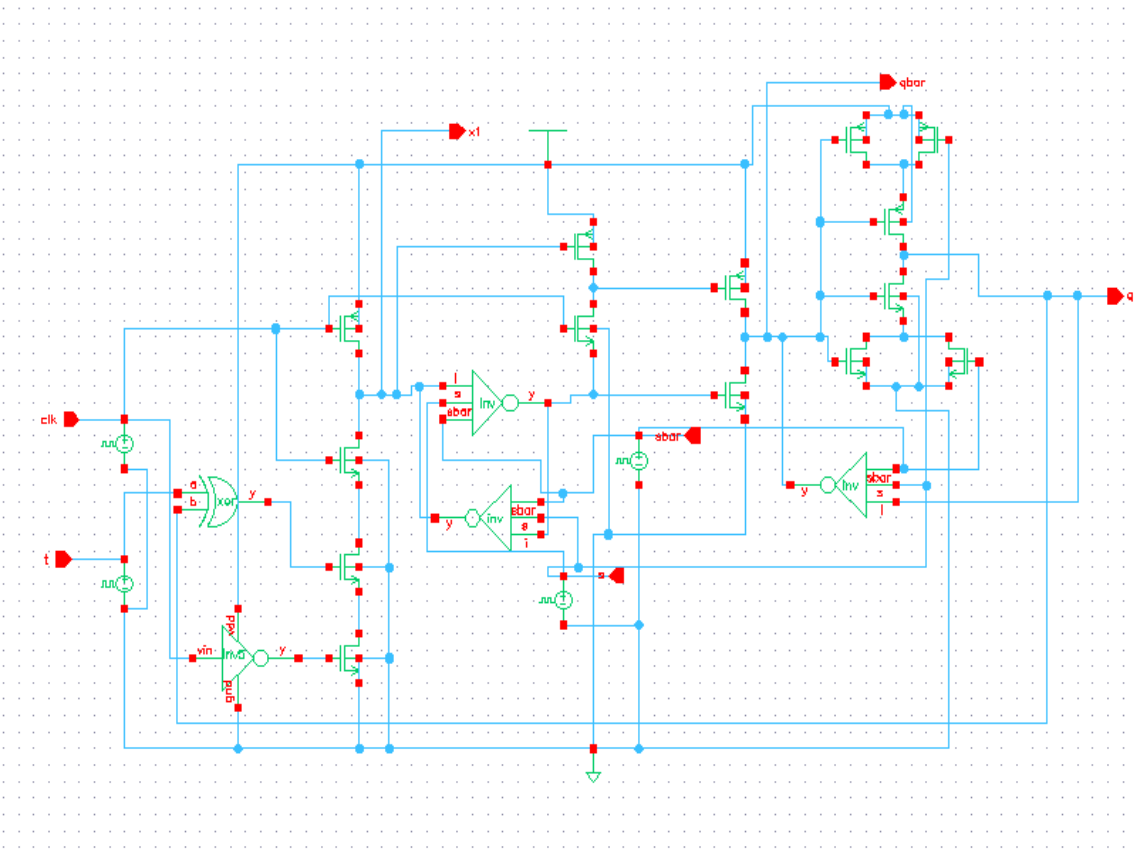

Fig 4.25 Implemented Schematic of proposed T flip flop in cadence spectre 90nm

4.6.1 TRANSIENT ANALYSIS

The transient analysis of the proposed T flip flop is shown in Fig 4.21 below. It works at maximum clock frequency of 1GHz. The time period of the input t is taken as 8.5ns. When the clock is positive edge triggered, the flip flop toggles. It holds this input state at its output q till the end of the clock period. When S=1 and Sbar=0, it gives reduced leakage power reduction at standby mode without wakeup cost.

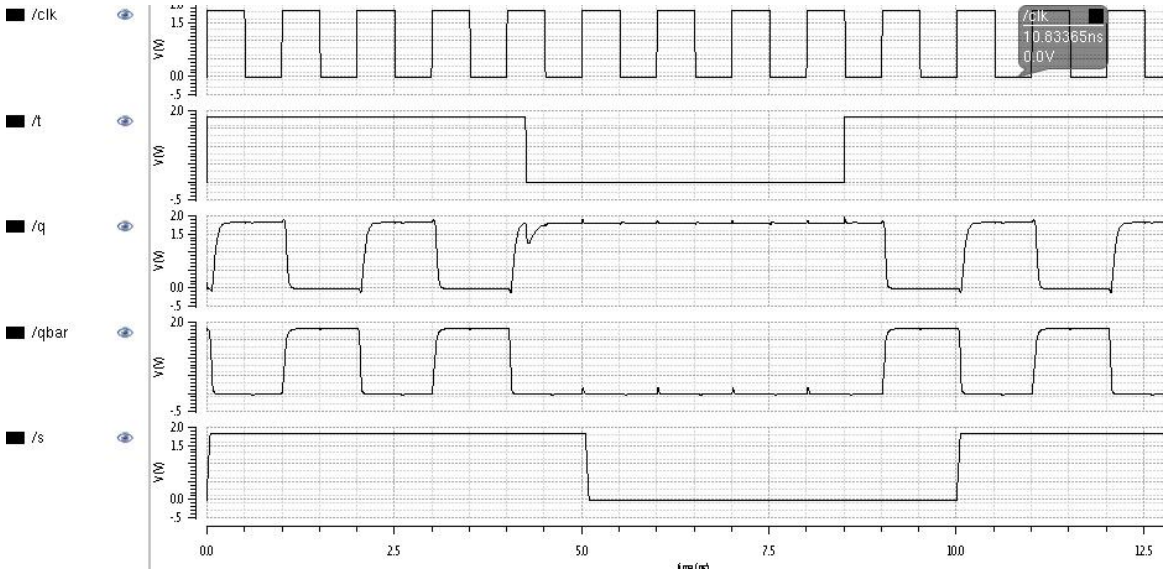

Fig 4.26 Transient analysis of proposed T flip flop

4.7 PROPOSED SR FLIP FLOP DESIGN

The proposed SR flip flop was designed using proposed D flip flop. The S+RBARQ block designed for conventional is used here also. It works at active and sleep mode. The remaining operation of the flip flop is same as conventional one working at evaluation and pre-charge phase. The schematic and transient analysis is shown in Fig 4.24 below. It operates at low power than conventional SR flip flop.

4.7.1 TRANSIENT ANALYSIS

The transient analysis of the proposed SR flip flop is shown in Fig 4.26 below. It works at maximum clock frequency of 1GHz. The time period of the input S and R are 8.5ns and 4.5ns is taken as 8.5ns. When the clock is positive edge triggered, the flip flop toggles. It holds this input state at its output q till the end of the clock period. When S=1 and Sbar=0, it gives reduced leakage power reduction at standby mode without wakeup cost.

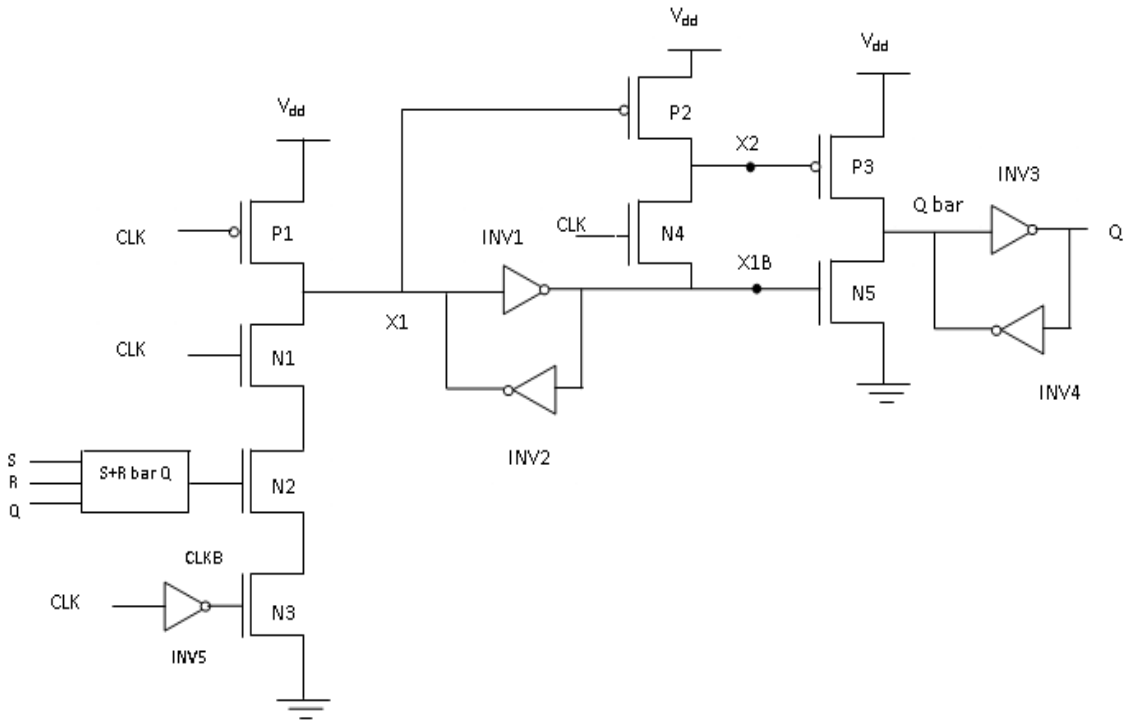

Fig 4.27 Schematic of proposed SR flip flop

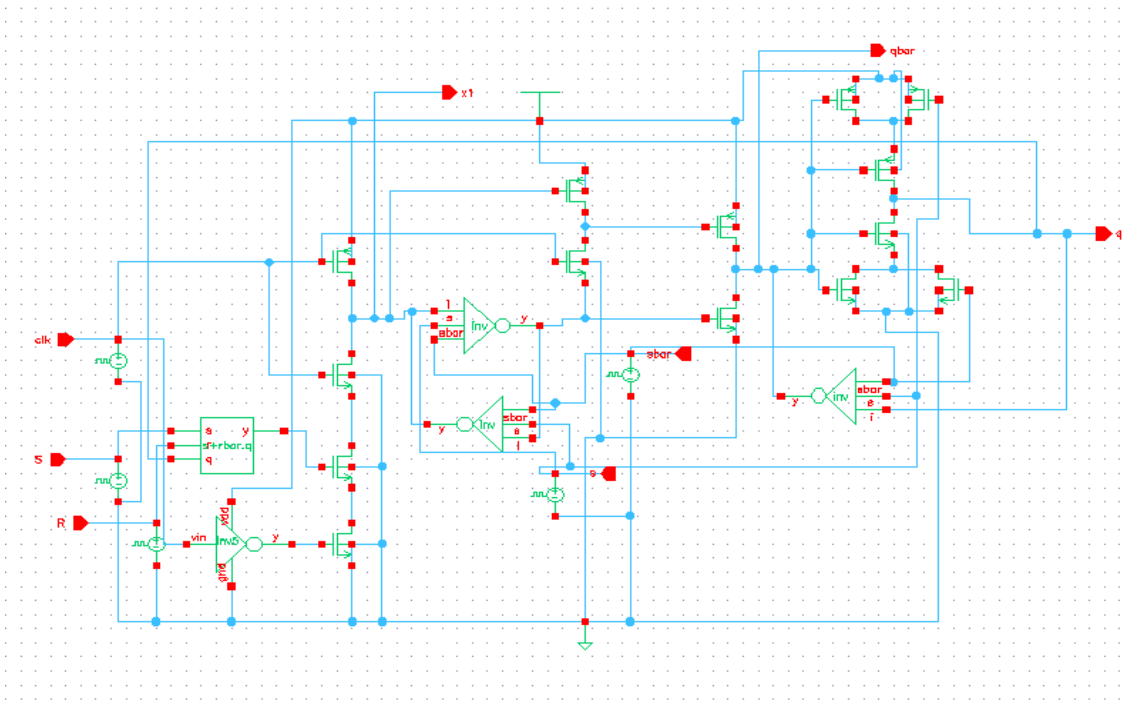

Fig 4.28 Implemented Schematic of proposed SR flip flop in cadence spectre 90nm

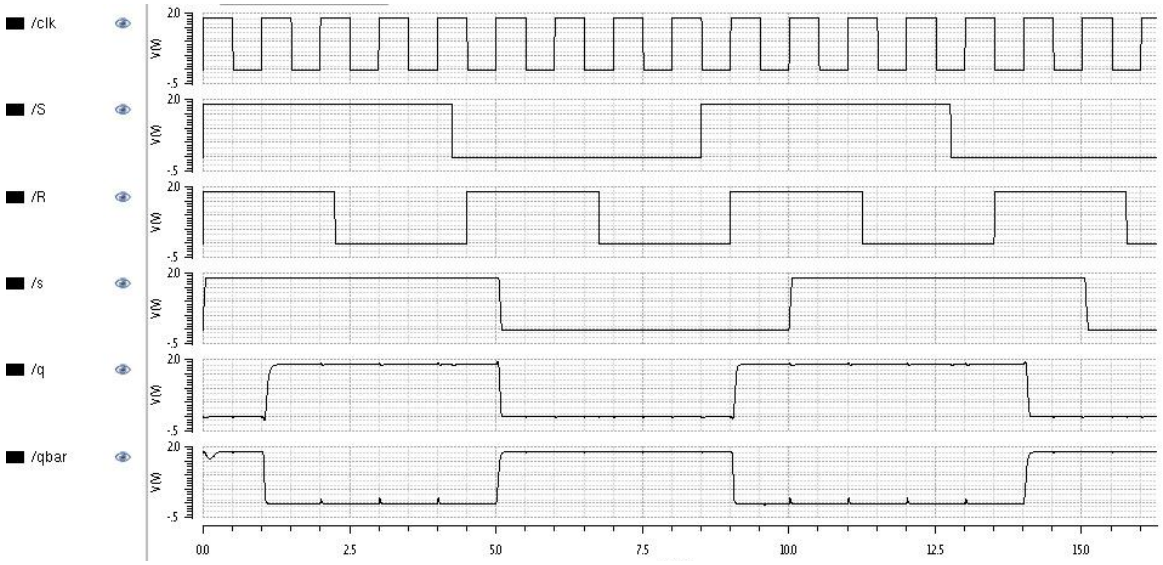

Fig 4.29 Transient analysis of proposed T flip flop

4.8 PROPOSED JK FLIP FLOP DESIGN

The proposed JK flip flop was designed using proposed D flip flop. The MUX block designed for conventional is used here also. It works at active and sleep mode. The remaining operation of the flip flop is same as conventional one working at evaluation and pre-charge phase. The schematic and transient analysis is shown in Fig 4.27 below. It operates at low power than conventional JK flip flop.

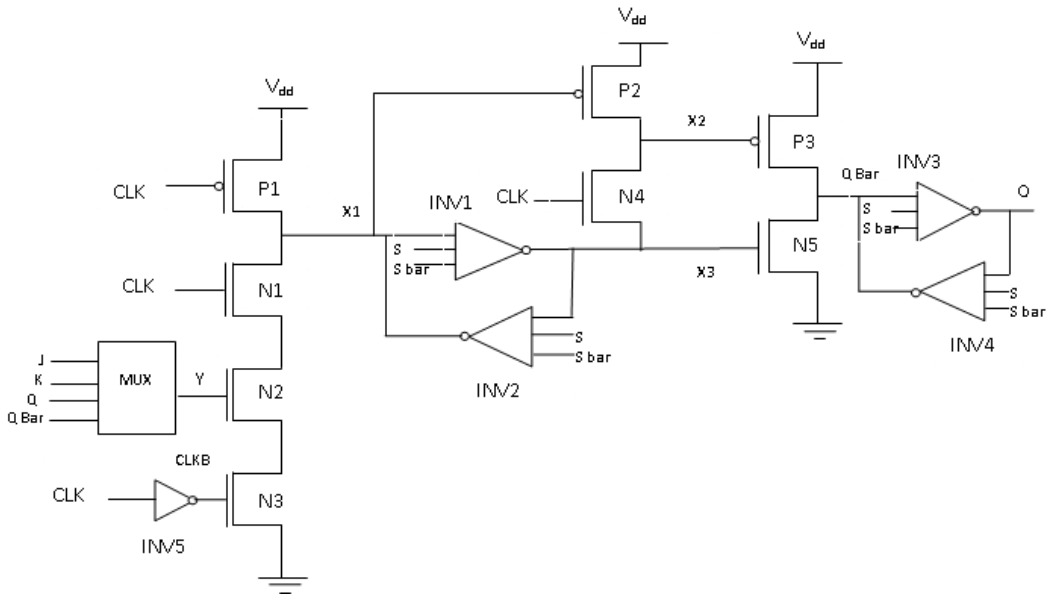

Fig 4.30 Schematic of proposed JK flip flop

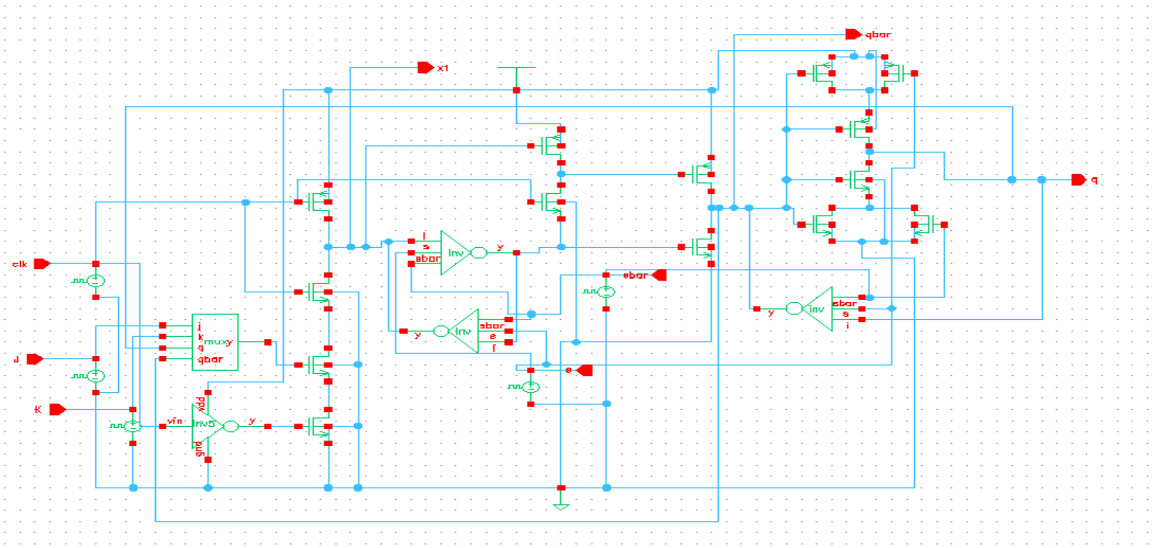

Fig 4.31 Implemented Schematic of proposed JK flip flop in cadence spectre 90nm

4.8.1 TRANSIENT ANALYSIS

The transient analysis of the proposed JK flip flop is shown in Fig 4.28 below. It works at maximum clock frequency of 1GHz. The time period of the input J and K are 8.5ns and 4.5ns. When the clock is positive edge triggered, the flip flop toggles. It holds this input state at its output q till the end of the clock period. When S=1 and Sbar=0, it gives reduced leakage power reduction at standby mode without wakeup cost.

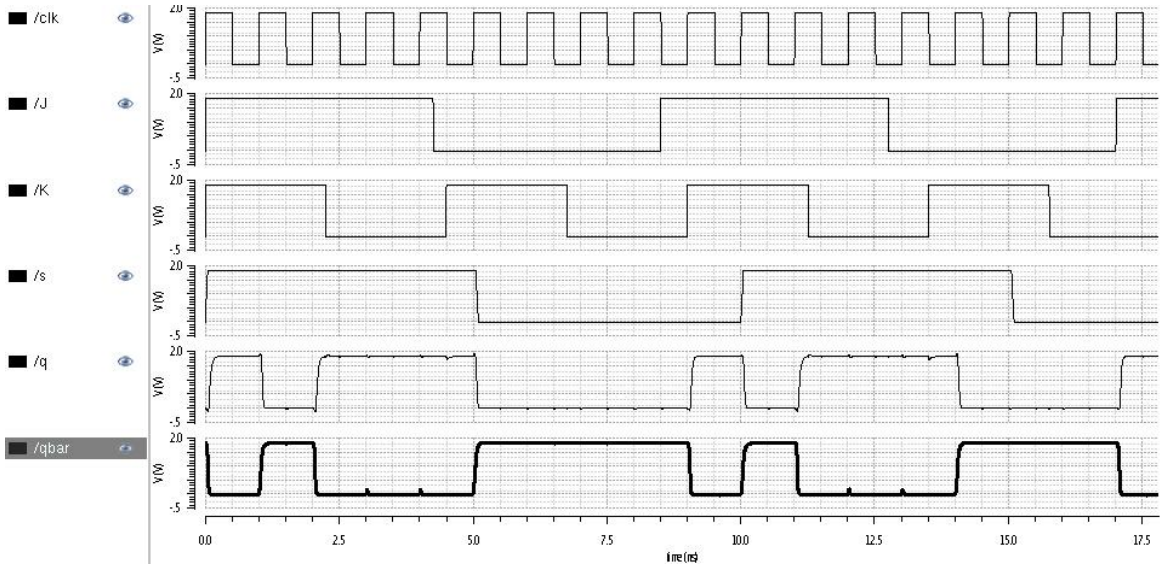

Fig 4.32 Transient analysis of proposed T flip flop

Thus the implementation of various conventional and proposed flip flops was explained elaborately with the help of schematic, transient analysis and layout.

CHAPTER 5

SIMULATION AND RESULT ANALYSIS

The conventional and proposed architecture were simulated in cadence 90nm tool and following analysis were done:

1. Transient Analysis
2. Analysis based on supply voltage
3. Analysis based on data activity
4. Analysis based on input vectors
5. Noise analysis
6. Metastability

The following parameters were taken into consideration for the above mentioned analyses:

1. Leakage power
2. Total power
3. Delay
4. Power delay product (PDP)
5. Noise spectral density
6. Mean time between failure (MTBF)

5.1 TRANSIENT ANALYSIS

The transient analysis of static CMOS inverter and sleepy stack inverter and the transient analyses of both conventional and proposed flip flops are with exact output with required amplitude of 1.8V and 1.2V. The output waveforms were shown in Chapter 4. Table 5.1 and Table 5.2 shows the comparison of inverters, conventional and proposed flip flops at a supply voltage of 1.8V. The input frequency of inverter is 100MHz and the clock frequency is 1GHz and Time Period of Data of D flip flop and T flip flop is 8.5ns. The clock frequency is 1GHz and time period of 2 data inputs for SR flip flop and JK flip flop are 8.5ns and 4.5ns. The time period for sleep transistor inputs S and Sbar is 10ns. The transient analysis is done based on following parameters:

- Leakage Power (μW)
- Total Power (μW)
- Delay (ns)

- PDP (fJ)

5.1.1 COMPARATIVE ANALYSIS OF INVERTERS

Table 5.1 Comparative Analysis of Inverters

TYPE OF INVERTER	LEAKAGE POWER (nW)	TOTAL POWER (nW)
CMOS	**482**	**414**
Sleepy Stack	**0.064**	**356.8**

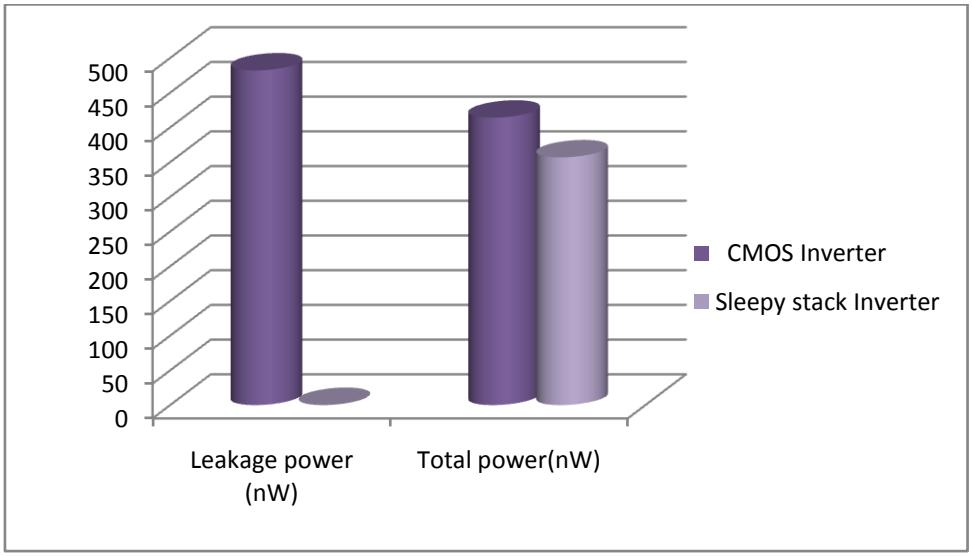

Fig 5.1 Comparative analysis of inverters

The above comparison shows that there is larger decrease in leakage power in sleepy stack inverter compared to CMOS inverter. There is 99% reduction in leakage power in sleepy stack in comparison with CMOS inverter. There is 14% reduction in total power. So we infer following from the above comparison:

- When there is increase in threshold voltage (sleep transistor effect), there is decrease in leakage power and total power.
- When two or more transistors are cut off together (stack effect), there is greater decrease in power.

Thus Sleepy stack Inverter is best when compared to CMOS in terms of low leakage power and total power.

5.2 COMPARATIVE ANALYSIS OF FLIP FLOPS

Table 5.2 Comparative Analysis of flip flops at a supply voltage of 1.8V

PARAMETERS	D FLIP FLOP		T FLIP FLOP		SR FLIP FLOP		JK FLIP FLOP	
	CONVENTIONAL	PROPOSED	CONVENTIONAL	PROPOSED	CONVENTIONAL	PROPOSED	CONVENTIONAL	PROPOSED
LEAKAGE POWER (µW)	3.378	2.31	3.7	2.37	4.89	3.5	4.32	3.263
TOTAL POWER (µW)	63.25	50	93.55	78.9	69.42	56.74	73.84	63.96
DELAY (nS)	4.62	4.617	2.61	2.606	4.123	4.112	2.6175	2.6145
PDP (FJ)	292.21	230.85	244.16	205.61	286.22	233.31	193.27	167.22

Table 5.3 Comparative Analysis of flip flops at a supply voltage of 1.2V

PARAMETERS	D FLIP FLOP		T FLIP FLOP		SR FLIP FLOP		JK FLIP FLOP	
	CONVENTIONAL	PROPOSED	CONVENTIONAL	PROPOSED	CONVENTIONAL	PROPOSED	CONVENTIONAL	PROPOSED
LEAKAGE POWER (µW)	0.372	0.25	0.372	0.254	0.516	0.335	0.484	0.365
TOTAL POWER (µW)	24	17.51	22.37	21.21	25.99	19.15	26.66	21.84
DELAY (nS)	4.922	4.961	3.409	3.42	4.922	4.99	3.423	3.5
PDP (FJ)	118.128	86.86711	76.259	45.1773	127.922	95.55	91.257	65.23

5.1.2.1 LEAKAGE POWER

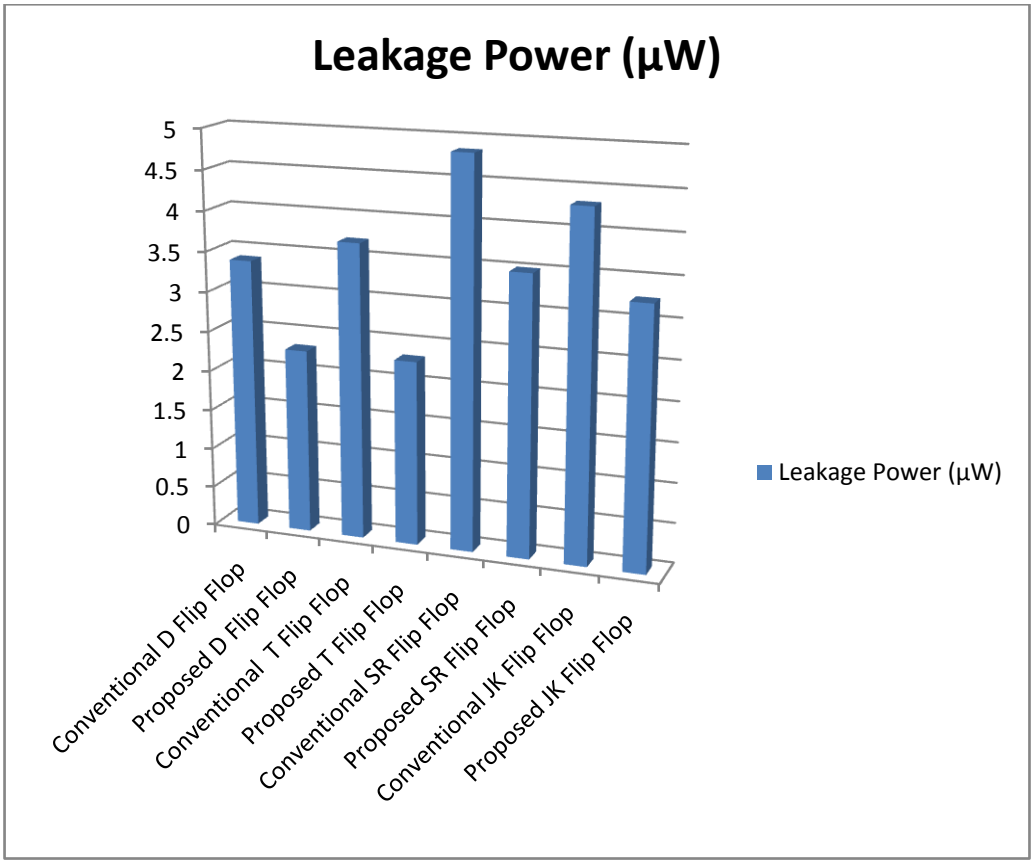

Fig 5.2 Comparative analysis of flip flop based on leakage power.

The above comparison shows that there is larger decrease in leakage power in proposed flip flop compared to conventional flip flop. There is 32%, 38%, 28%, 24% reduction in leakage power in proposed D flip flop, T flip flop, SR flip flop and JK flip flop. D flip flop consumes least leakage power. SR flip flop consumes maximum leakage power as the S+(RbarQ) block is designed using static CMOS technique. So we infer following from the above comparison:

- When there is increase in threshold voltage (sleep transistor effect), there is decrease in leakage power and total power.
- When two or more transistors are cut off together (stack effect), there is greater decrease in power.

Thus proposed flip flop consumes less leakage power compared to conventional flip flops and D flip flop consumes least leakage power and SR flip flop consumes maximum leakage power.

5.1.2.2 TOTAL POWER

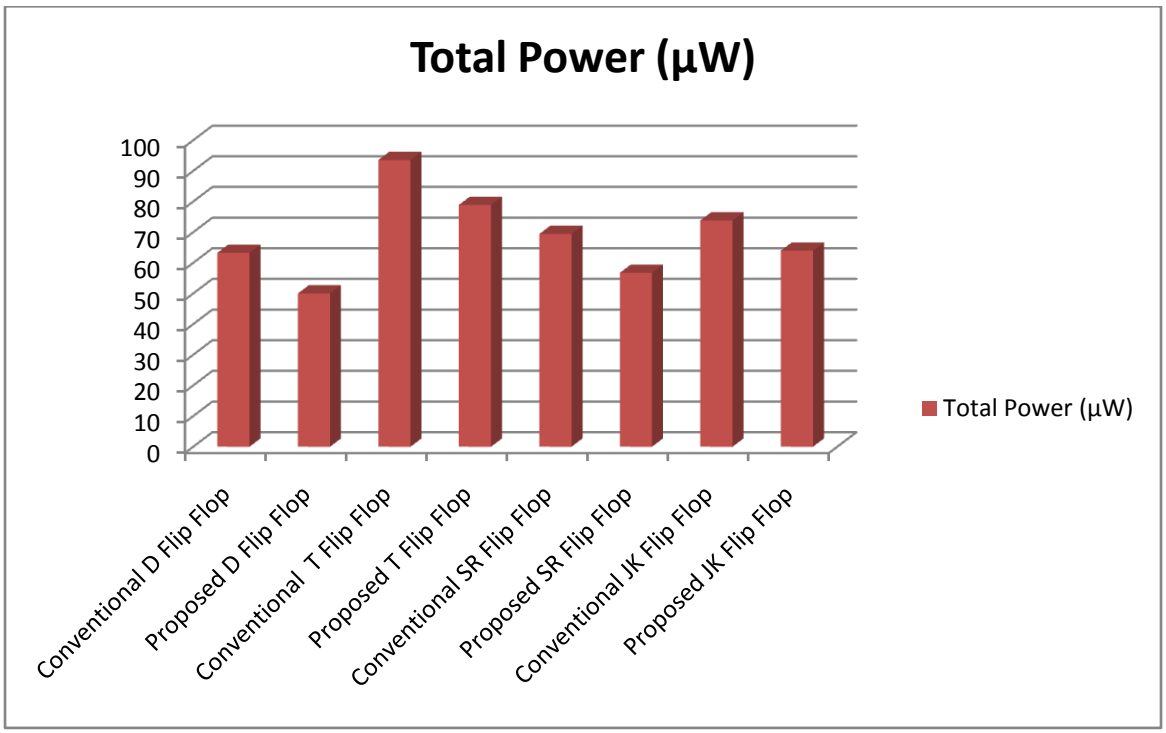

Fig 5.3 Comparative analysis of flip flop based on total power.

The above comparison shows that there is larger decrease in total power in proposed flip flops compared to conventional flip flops. There is 21%, 15%, 18%, 13.3% reduction in total power in proposed D flip flop, T flip flop, SR flip flop and JK flip flop. D flip flop consumes least total power. T flip flop consumes maximum total power due to toggling effect which accounts for greater dynamic power dissipation. So we infer following from the above comparison:

- Leakage power contributes more to total power in deep sub micron (DSM) technologies.
- When there is increase in threshold voltage (sleep transistor effect), there is decrease in total power.
- When two or more transistors are cut off together (stack effect), there is greater decrease in power.

Thus proposed flip flop consumes less total power compared to conventional flip flops and D flip flop consumes least total power and SR flip flop consumes maximum leakage power.

5.1.2.3 DELAY

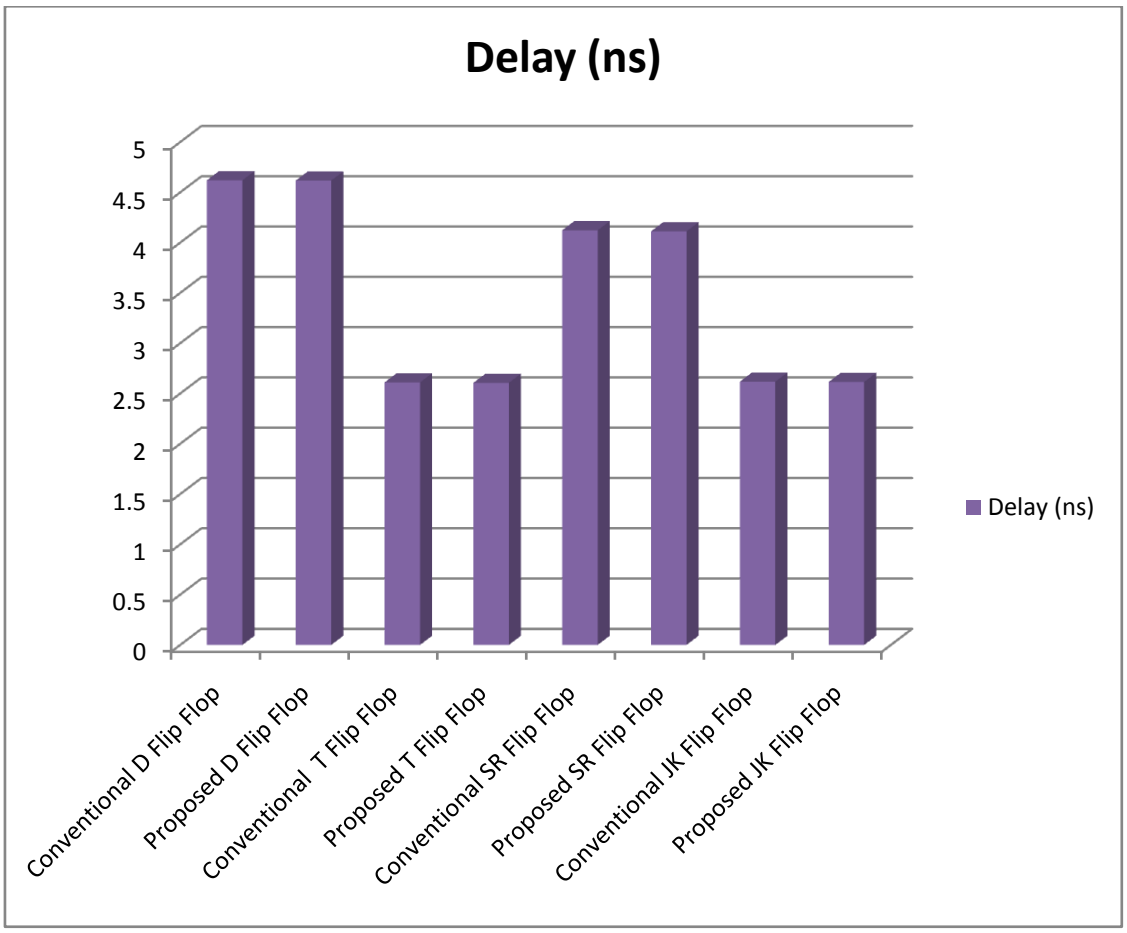

Fig 5.4 Comparative analysis of flip flop based on delay.

The above comparison shows that delay is almost maintained in proposed flip flops compared to conventional flip flops. It is because of increase in threshold voltage. There is 6%, 2%, 3%, 0.003% reduction in delay in proposed D flip flop, T flip flop, SR flip flop and JK flip flop. D flip flop has maximum delay due to absence of feedback from Q. JK flip flop has least delay because of feedback from Q and use of multiplexer. So we infer following from the above comparison:

- When there is increase in threshold voltage (sleep transistor effect), there is increase in delay but it is maintained by increasing the supply voltage.

Thus proposed flip flop maintains the delay as in conventional flip flop though there is greater chance of increase in delay. JK flip flop has minimum delay and D flip flop has maximum delay.

5.1.2.1 Power Delay Product (PDP)

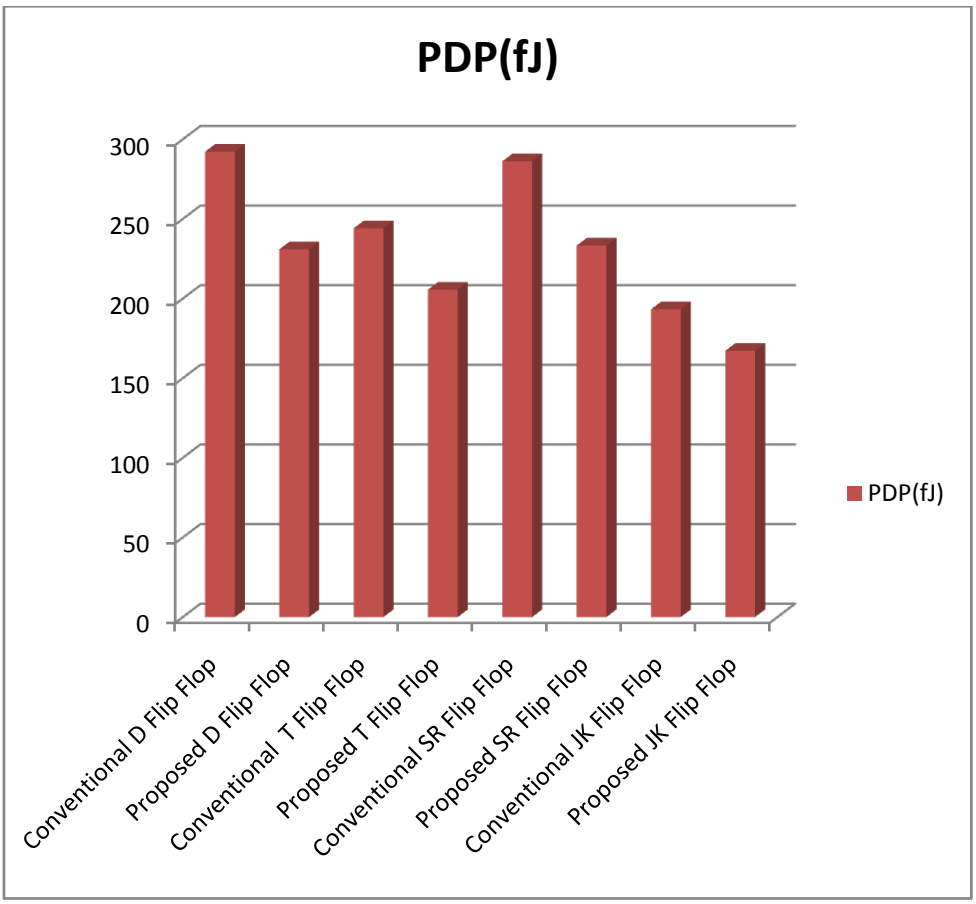

Fig 5.5 Comparative analysis of flip flop based on PDP.

The above comparison shows that there is decrease in PDP in proposed flip flop compared to conventional flip flop. There is21%, 16%, 18%, 13% reduction in PDP in proposed D flip flop, T flip flop, SR flip flop and JK flip flop. JK flip flop hast least PDP due to less delay. D flip flop has maximum delay due to larger delay. So we infer following from the above comparison:

- When there is decrease in total power there is decrease in PDP though delay is no reduced to expected range but the speed is maintained.

Thus proposed flip flop consumes less PDP compared to conventional flip flop. D flip flop has maximum PDP and JK flip flop consumes maximum leakage power.

INFERENCE : In the proposed design , leakage power, total power, PDP is reduced with maintaining the same delay. Thus it can be used for high speed applications with low power.

5.2 ANALYSIS BASED ON SUPPLY VOLTAGE

This analysis is based on effect of supply voltage on total power and delay. The supply voltage used to measure total power and delay are 1.2V and 1.8V. The comparative analysis of flip flops under various parameters at 1.8V and 1.2V supply voltage is given in Table 5.2 and Table 5.3. This analysis is done for all conventional and proposed flip flops.

5.2.1 TOTAL POWER vs SUPPLY VOLTAGE

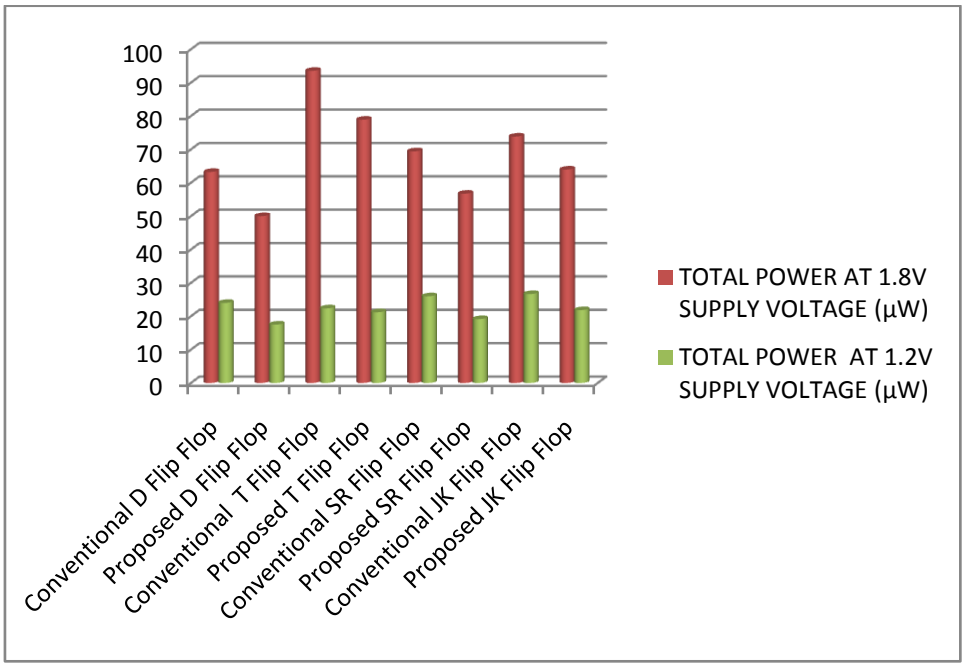

Fig 5.6 Comparative analysis of flip flop based on Total Power and Supply voltage

The above chart shows the variation in total power with respect different supply voltages. There is decrease in 62%, 76%, 62%, 64% in total power in conventional D, T, SR, JK flip flops when a supply voltage of 1.2V is used. There is there is decrease in 64%, 73%, 66%, 66% in total power in proposed D, T, SR, JK flip flops when a supply voltage of 1.2V is used. The power consumed is less in 1.2V supply voltage than in 1.8V supply voltage.

From the above observation it is inferred that total power is directly proportional to the supply voltage. As there is a need of low power, the supply voltage can be reduced.

5.2.2 DELAY vs SUPPLY VOLTAGE

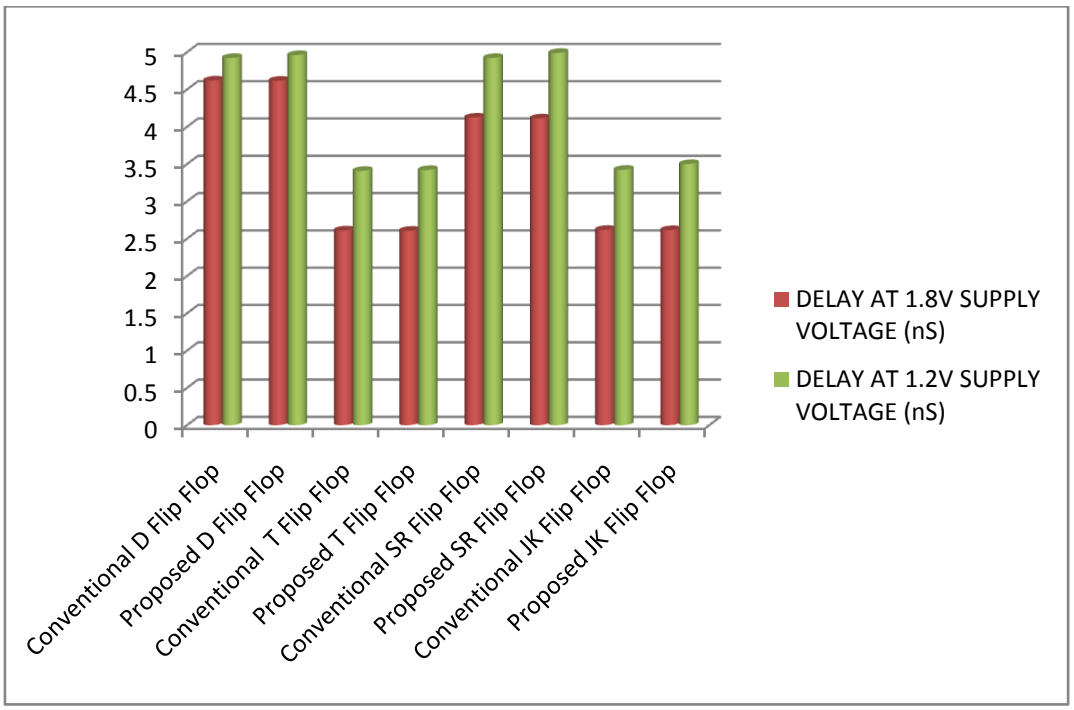

Fig 5.7 Comparative analysis of flip flop based on Delay and Supply voltage

The above chart shows the variation in delay with respect to different supply voltages. There is decrease in 6%, 23%, 16%, 23% in delay in conventional D, T, SR, JK flip flops when a supply voltage of 1.2V is used. There is there is decrease in 7%, 24%, 18%, 25% in delay in proposed D, T, SR, JK flip flops when a supply voltage of 1.8V is used. The power consumed is less in 1.2V supply voltage than in 1.8V supply voltage.

From the above observation it is inferred that delay is inversely proportional to the supply voltage. If supply voltage is less, then current flowing through also gets reduced as both are directly proportional. So charging of capacitance does not takes place fast enough which increases the delay. So supply voltage should be large enough to increase the speed of the circuit.

INFERENCE : Supply voltage is directly proportional to total power and inversely proportional to delay. So in order to have low power for high speed applications, the supply voltage should be kept moderate to balance both power and delay.

5.3 ANALYSIS BASED ON DATA ACTIVITY

This analysis is based on power consumption at various data activities by D flip flop. The Table 5.4 shows the total power consumed at various data activities.

100% data activity - 1010101….sequence

50% data activity - 11001100….sequence

25% data activity - 11110000….sequence

0% data activity - 1111….sequence or 0000…sequence

Table 5.4 Total power dissipated at different data activities by D flip flop

Flip flops	**Total power (µW)**			
	100%	***50%***	***25%***	***0%***
Conventional	76.96	73.2	63.17	14.35
Proposed	76.67	82.68	58.97	13.65

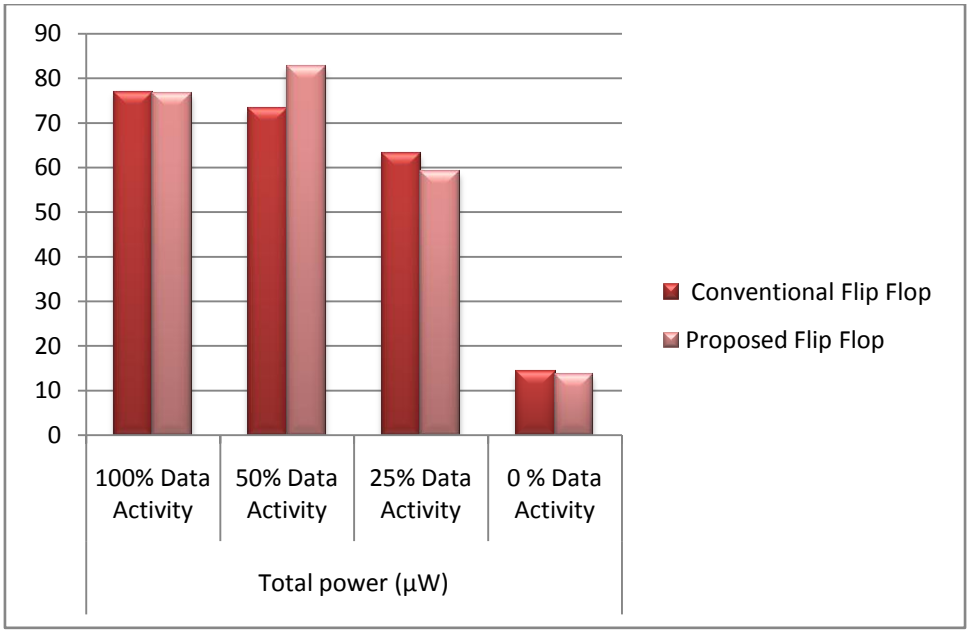

Fig 5.8 Total power at various data activities of a D flip flop

INFERENCE :The proposed flip flop dissipates less power in all data activities except in 50% data activity.0

5.4 ANALYSIS BASED ON INPUT OUTPUT VECTORS.

In this analysis, the input vectors CLK and D of D flip flop are varied at all possible combinations and the leakage power is calculated. The Table 5.5 shows the change in leakage power at various combinations of input vectors.

Table 5.5. Leakage power of d flip flop at various input-output levels

Flip flops	**Leakage power (µW)**			
	CLK=0		***CLK=1***	
	D=0 Q=0	***D=1 Q=1***	***D=0 Q=0***	***D=1 Q=1***
Conventional	3.378	4.359	2076	2307
Proposed	2.311	3.293	0.057	905.4

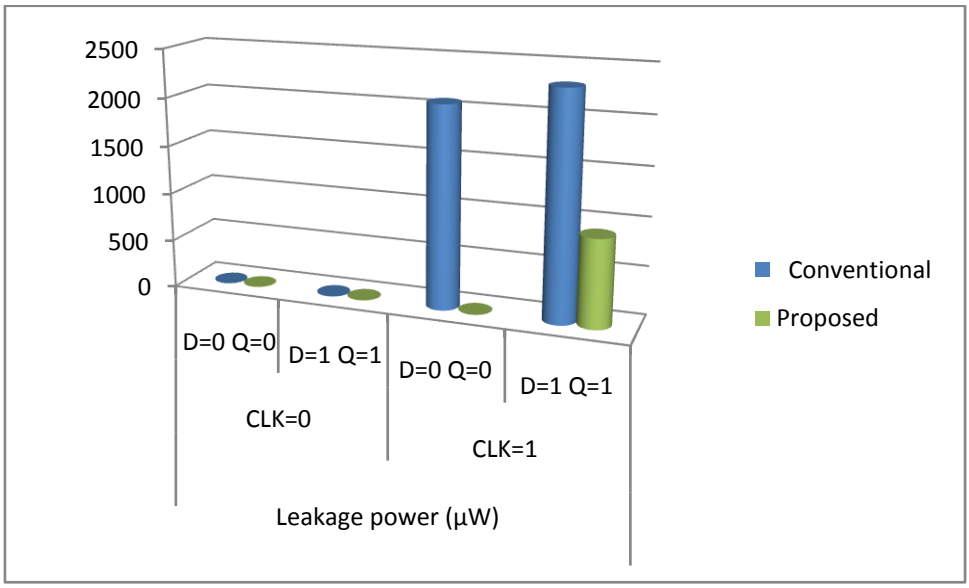

Fig 5.9 Leakage power at various input output vectors of a D flip flop

The leakage power of the D flip flop is less when the input output vectors are D=0, CLK=0, Q=0. It is maximum when D=1, CLK=1, Q=1. When the system is in stand-by mode, the input output vectors which gives less leakage power can be set to decrease the power

INFERENCE : Thus leakage power depends also on the input output vectors. Choose the vector which give less leakage power at standby mode.

5.5 NOISE ANALYSIS

This analysis is used to calculate the overall output noise of the proposed flip flop in terms of Noise Spectral Density (V^2 /Hz). Noise spectral density shown in Fig 5.1 below is in terms of voltage which varies with frequency. Here we compare Noise spectral density with respect to following parameters:

- Frequency
- Supply voltage
- Total power

5.5.1 NOISE SPECTRAL DENSITY vs FREQUENCY

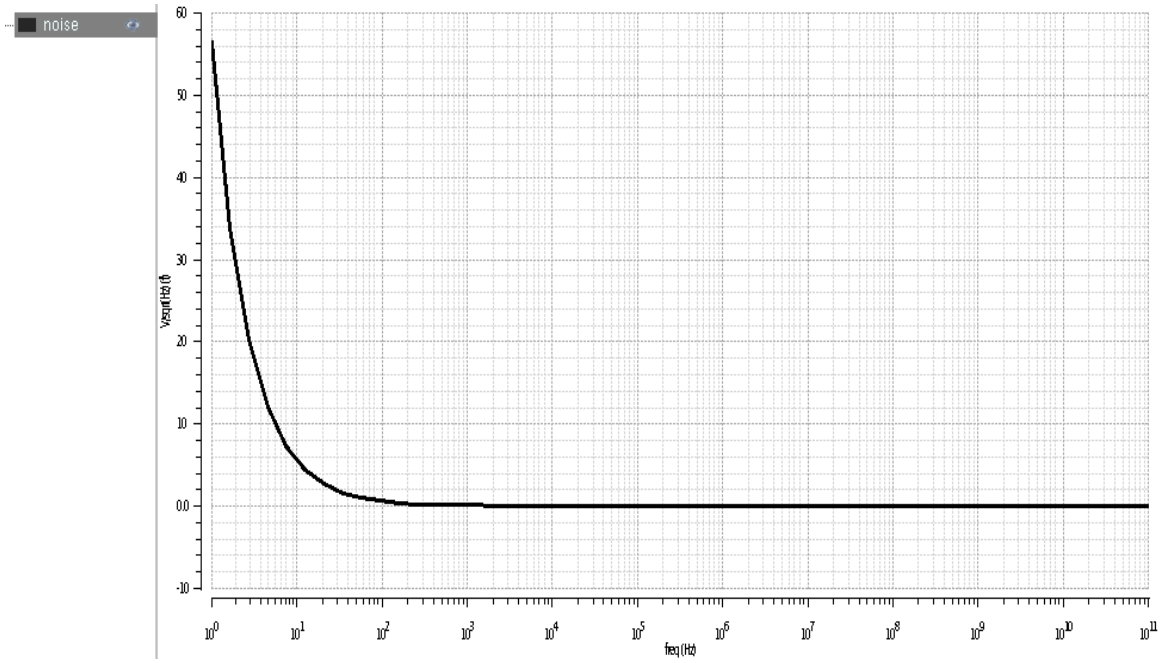

Fig 5.10 Noise spectral density of Proposed Flip Flop.

From the above graph it is evident that when frequency increases, the noise spectral density decreases. The high frequency noise is called as white noise and low frequency noise is called as flicker noise in MOSFET. Here the flicker gets decreased with increase in frequency that is why it is called as 1/f noise. White noise is constant throughout. Thus frequency is inversely proportional to noise spectral density.

5.5.2 NOISE SPECTRAL DENSITY vs SUPPLY VOLTAGE AND POWER

From the ADE window the Noise spectral density is calculated by varying the supply voltage. Table 5.6 shows the noise spectral density vs Supply voltage.

Table 5.6 Noise spectral density vs Supply voltage

SUPPLY VOLTAGE (V)	NOISE SPECTRAL DENSITY (V^2/Hz)
1.8	$1.259*10^{-16}$
1.2	$1.550*10^{-16}$
1	$1.841*10^{-16}$

The noise spectral density increases with decrease in supply voltage. So to maintain a moderate noise, the supply voltage should be taken into consideration. So if supply voltage is increased then power also gets increased and noise remain low. So noise is more prevalent in low power application.

INFERENCE : To maintain moderate noise in a system the supply voltage should be selected wisely so that neither power nor noise will get increased. The high frequency noise is constant. The low frequency noise gets decreased with increase in frequency.

5.6 METASTABILITY

The metastability can be measured in terms of mean time between failure (MTBF). MTBF is the average time between two successive failures. As clock frequency increases, the MTBF gets decreased. It also depends on the critical window that setup time and hold time. The time period of the clock should be large enough to avoid metastability to some extent. It cannot be removed completely.

Table 5.7 Clock Frequency vs MTBF

CLOCK FREQUENCY (GHz)	MTBF (ns)
2	0.51
1	1.01
0.001	1010

Thus the six different analyses were done and drawn some conclusions.

CHAPTER 5

CONCLUSION

A novel low power hybrid flip flop was designed using sleepy stack inverter pairs. The following conclusions were made from the analysis of results:

- 99% reduction in leakage power was observed in sleepy stack inverter compared with CMOS inverter.
- The leakage power was reduced to 32%, 38%, 28%, 24% in proposed D, T, SR and JK flip flops.
- The total power was reduced to 21%, 15%, 18%, 13.3% in proposed D, T, SR and JK flip flops.
- The PDP was reduced to 21%,16%, 18%, 13% in proposed D, T, SR and JK flip flops.
- The delay is maintained as in conventional case as there was high risk of increasing the delay due to use of high threshold voltage transistors.
- The leakage power is minimum when D=0, CLK=0 AND Q=0. When the system is in standby mode, the above input output vector can be set to reduce leakage power.
- Noise should be kept moderate as it increases with decrease in supply voltage.
- Area gets increased in proposed flip flop which is the trade off in the design.

Thus the Proposed flip flop is well suitable to be used in low power application and during standby mode maintaining the high speed without any cost of wake up time.

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