"DESIGN AND IMPLEMENTATION OF FOLDED CASCODE CURRENT MIRROR FOR HIGH OUTPUT RESISTANCE AND WIDE VOLTAGE SWING"

DISSERTATION-III

Submitted in partial fulfillment of the

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Electronics & Communication Engineering

By

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MAY 2018

CERTIFICATE

This is to certify that the Dissertation-III titled "**Design and implementation of folded cascade current mirror for high output resistance and wide voltage swing**". That is being submitted by "**Manendra Singh**" in partial fulfillment of the requirements for the award of Master of Technology, is a record of bonafide work done under my guidance. The content of this report, in full or in parts, have neither taken from any other source nor have been submitted to any other Institute or university forward of any degree or diploma and the same is certified.

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Objective of the Thesis is satisfactory/unsatisfactory

Examiner I **Examiner II**

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Last but not least, I would like to thank God for the strength that keeps me standing and for the hope that keeps me believing that this report would be possible. I would also thank the staff members of the department of Electronics and Communication engineering who have been very patient and co-operative with us.

DECLARATION

I, Manendra Singh, student of Master of Technology under Department of Electronics and Communication Engineering of Lovely Professional University, Punjab, hereby declare that all the information furnished in this dissertation-III report is based on my own intensive research and is genuine. This dissertation-III, to the best of my knowledge, does not contain any work which is not done by me.

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ABSTRACT

Current mirror is the basic building block in analog circuit design for providing the biasing voltage to so many components in the system. Current mirror is used in various application where low voltage analog circuit design is needed like in any of the portable devices so that battery lifetime can be increased . In this thesis, work a high performance MOSFET current mirror in a folded cascode configuration is designed to achieve a high output resistance ,operating in wide range of supply voltage . The design has both n and p type MOSFET for current feedback between gate and source in order to achieve a constant drain current . In the discussed circuits i have found out the range of currents for which the circuit is showing amplification and mirroring effect. The design is implemented and it's mathematical model is been analyzed to know the output voltage from the circuit in respect to the reference current using small signal model analysis of the circuit. I have designed the layout of the circuit and it's post layout simulation is also analyzed by optimizing the layout design of the circuit. The output resistance values is much higher then the previously designed circuit. It's corner analysis is done with FF , FS ,SF and SS with varying temperature between -25°C to 80°C and this circuit works perfectly when going for fast fast (FF) simulation in these extreme ranges of temperatures.

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CHAPTER 1

INTRODUCTION

In a various application like biomedical operates on very low voltage which needs a very high output impedance current mirror. The current mirror is the circuit that implements the principle that if a gate-source voltage of two uniforms MOS transistors is same then their channel current flowing would be equal. In the current mirror, we generate a current reference so to copy that current in various current sources in the system. Various advancement in the technology of CMOS design integrated most of the circuits in the same chip who all are working on very low supply voltage like radio frequency processor and various sensor like temperature and baseband signal processing circuit require very low voltage supply. Getting a very large impedance and wide output range and swing is the important parameter when working on the very low input voltage.

The current mirror is the circuit used where the operating voltage required to turn on the circuit is very low as in case of biomedical applications. In the current mirror, we need high output impedance so to drive more circuitry from it. In the discussed paper they have worked on increasing the high output voltage swing and high impedance current mirror.

The Current mirror is a circuit which has the principle that V_{gs} gate-source voltage of two similar MOS transistors is identical then its channel current should be same. In the current mirror, we generate a current reference so to copy that current in various current sources in the system. So now how we do that current reference equal to the output current is done by making the gate-source voltage in the two transistors equal VDS1=VDS2.

1.1 SIMPLE CURRENT MIRROR

The basic idea here is for a MOSFET if current (Id) = f (VGS), where function denotes the functionality of ID versus VGS, then VGS = f^{-1} (ID). Then if the transistor is biased through IREF then VGS= f^{-1} (IREF). Thus voltage is put into the source-gate terminal then derived current

$$Iout = f\, f^{-1}(IREF) = IREF$$

$$\text{Iref} = \frac{1}{2}\text{un cox}(\frac{\text{w}}{\text{l}})^1(V_{gs} - \text{vth})^2$$

$$\text{Iout} = \frac{1}{2}\text{un cox}(\frac{\text{w}}{\text{l}})^2(V_{gs} - \text{vth})^2$$

$$\text{Iout} = \frac{\left(\frac{\text{w}}{\text{l}}\right)^2}{\left(\frac{\text{w}}{\text{l}}\right)^1}\text{Iref}$$

Current mirror usually has the same length for all of the transistor so to minimize the error. In the above discussed current mirror we have neglected the channel length modulation but in practice, there is an error in copying the current due to the involvement of drain-source voltage

$$\text{ID1} = \frac{1}{2}\text{un cox}(\frac{\text{w}}{l_1})(\text{vgs} - \text{vth})^2(1 + \lambda\text{vds1}) \text{ and}$$

$$\text{ID2} = \frac{1}{2}\text{un cox}(\frac{\text{w}}{l_2})(\text{vgs} - \text{vth})^2(1 + \lambda\text{vds2})$$

$$\text{So hence } \frac{ID2}{ID1} = \frac{\left(\frac{\text{w}}{\text{l}}\right)^2}{\left(\frac{\text{w}}{\text{l}}\right)^1}\frac{(1+\lambda\text{vds2})}{(1+\lambda\text{vds1})}$$

So in order to minimize the consequence of channel length modulation cascade current source is used, the Vbias voltage Vb is so chosen that the voltage $V_y = V_X$ then the output current Iout tracks Iref with accuracy but this accuracy is obtained at the cost of voltage

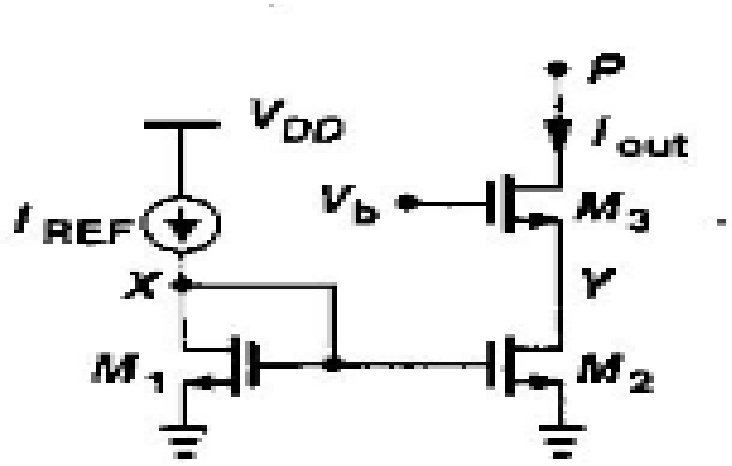

Fig-1.1 Simple current mirror

Head room that is consumed by the M3 transistor. So now how to generate the Vb so that V_y= V_X so from transistor M3 we have Vb - V_{gs3} = V_X or Vb = V_X+V_{gs3}. This shows that if gate source voltage is adjoin to V_X , the necessitate value of Vb can be acquired by this.

If an additional diode connected load is added M0 in series of M1 which create the voltage of Vn = V_{gs0}+Vx. so proper dimension of M0 and M3 will make V_{g3} =V_{g0}. Now connecting Vn to the gate terminal of M3. We get V_{gs0}+V_X = V_{gs3}+V_y.

Thus if the W/L aspect ratio of M3 by M1 is equal to W/L ratio of M2 by M1 then we can say that V_{gs3}= V_{gs0} and V_X = V_y. So the simple current has advantages like the output current is exact replica of the input current or some multiple times the input current. Another advantages of a simple current mirror is that the output impedance is high but not up to the mark. So the disadvantage of it is the impedance and the output current is not accurately tracked by the reference current.

If the current mirror is ideal than if the V_{ds} changes than I0 should not change as the output impedance of the ideal current mirror is infinite. We calculate output impedance by$\frac{\Delta Vo}{\Delta Io}$. So even though VO is changing Io should not change according to the principle hence $\Delta Vo/0$ is infinite and hence the output resistance of current mirror comes out to be infinite. So to have the output impedance increased we move on to next type of current mirror that is cascode current mirror.

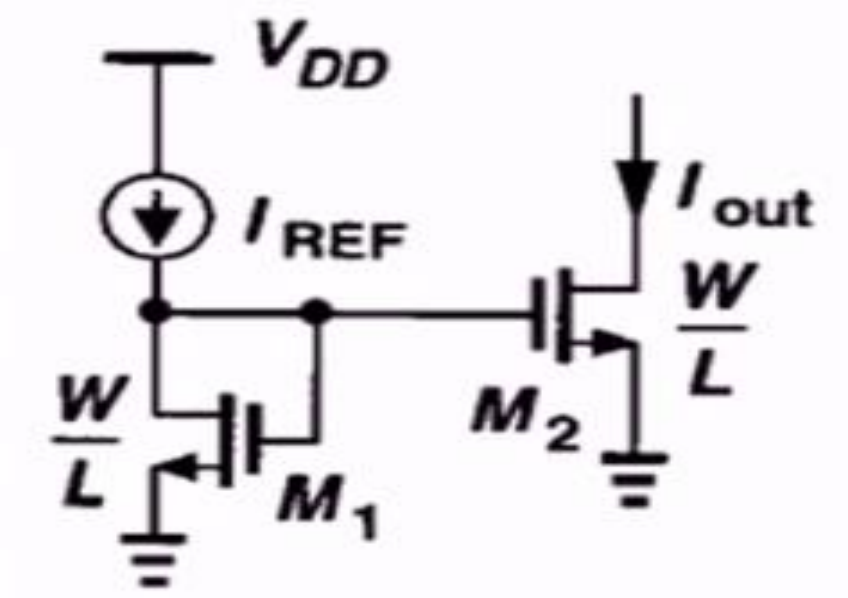

Fig 1.2 Current mirror

As both the mos are identical then Iref = Iout but as V_{gs1}= V_{ds1} = V_{gs2} but V_{ds2} is not equal to V_{gs2} because of the additional circuit connected to M2 transistor. V_{ds1} is not equal to V_{ds2} because of the channel length modulation and hence Iref ≠ I0 So I0 does not track out Iref accurately. So to remove this limitation we move to cascade current mirror. To make V_{ds1}= V_{ds2} we move to cascode current mirror.

The above limitation can be removed by making the drain to source voltage equal so to do so we connect one more transistor to the gate of the M2 transistor as shown.

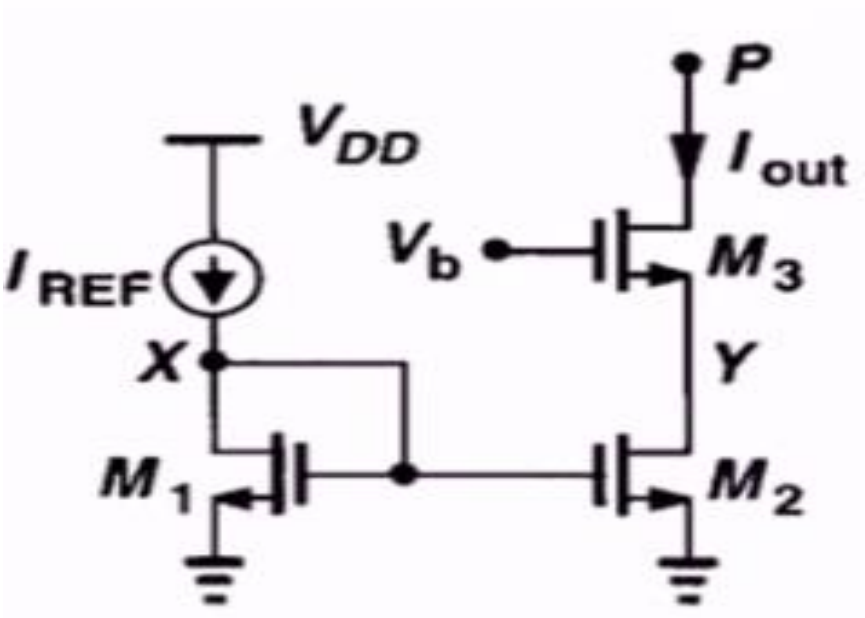

Fig 1.3 Modified simple current

So now in the shown fig if we make V_Y and V_X are made equal to each other than the problem of CLM can be solved so V_b is so chosen that can make V_Y equal to V_X and to do so V_b = V_{gs3} + V_X . Now there is one more modification done by connecting one more transistor to M1 side as shown in cascode current mirror.

1.2 CASCODE CURRENT MIRROR

So why we are using cascode current mirror because of extinguishing the result due to channel length modulation (CLM) and increase the yield impedance.

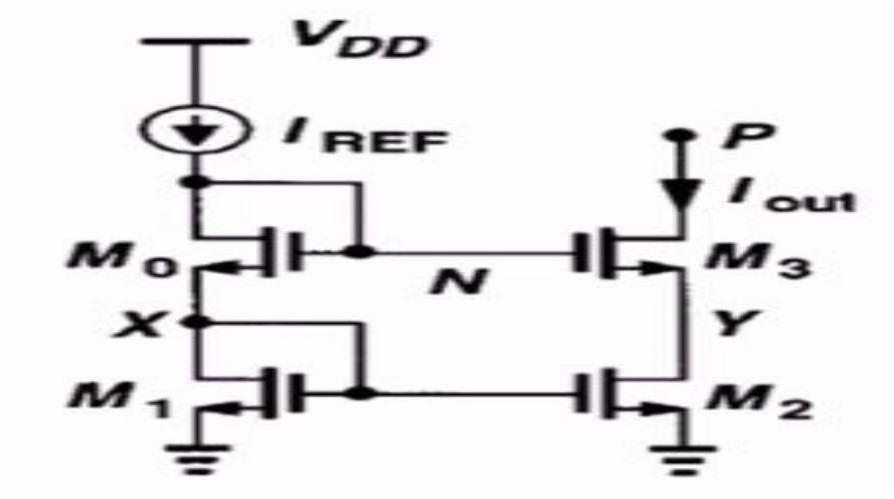

Fig 1.4 Cascode current mirror

At node N we give Vbias to both of the gate of M0 and M3 transistor to makeV_{gs0} equal toV_{gs3}. So voltage at both the side is V_{gs0}+Vx = V_{gs3} +Vy Now to make both of them equal proper dimension of the transistor is taken $\frac{W}{L_3}$*$\frac{W}{L_0}$= $\frac{W}{L_2} * \frac{W}{L_1}$ which gives $V_{gs0} = V_{gs3}$.

Now the output impedance can be calculated by drawing the small signal model so that is drawn by one simple principle that is if any mosfet is diode-connected and fed by a constant current then it behave like a constant DC potential. So as shown in fig a constant current is flowing in M0 AND M1 so they both act like a constant DC potential. So its small signal model is as shown.

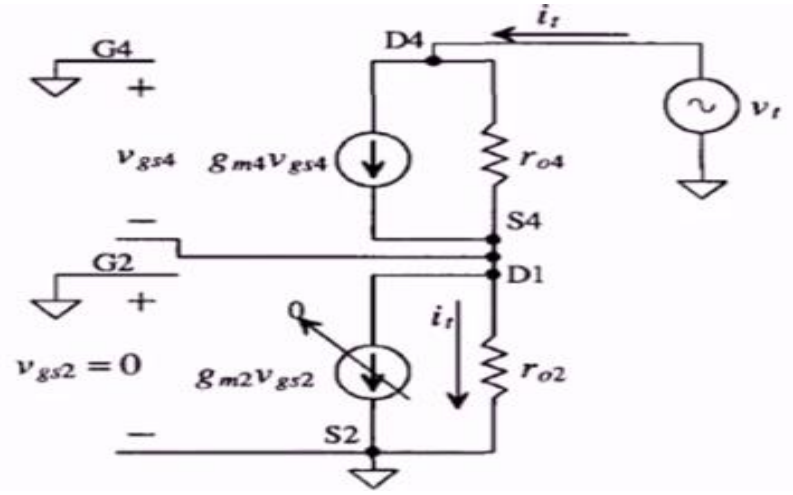

Fig 1.5 Small signal of cascode current mirror.

And output impedance of the circuit is vt/it so current is given by.

$$I_t = gm_4 v_{gs4} + \frac{v_t - (-v_{gs4})}{ro_4}$$

$$v_{gs4} = I_t * ro_2$$

So substituting the value of V_{gs4} in I_t , we get the equation.

$$\frac{v_t}{I_t} = ro_4 (1 + gm_4 * ro_2) + ro_2$$

$$R_0 = gm_4 * r_o^2$$

So small signal model of cascode is as shown. Here V_{gs2} is zero as voltage across M2 is zero as M1 is shorted as it acts like a DC voltage so that makes $g_{m2} * V_{gs2}$ equal to zero. So from the above equation we get to know that the total output resistance shown by the circuit is gm times the resistance, hence the output impedance of a modified cascode current mirror is very high with respect to simple current mirror whose resistance is R_{ds}. So finally we can say that the cascode current mirror is used to overcome channel length modulation and for high output resistance. But for the advantages we have some disadvantage to the circuit that is the swing of the output signal is very less as the swing is defined as Vdd – Vomin here Vomin is the minimum voltage required for the transistors to be in saturation mode. Ideally, Vomin for the cascode circuit is 2(V_{gs} -Vt) but from the circuit we, get Vomin higher than the ideal which is 2V_{gs} -Vt, which is Vt times higher than the ideal voltage.

1.3 WILSON CURRENT MIRROR

So now we move to next type of current mirror with wide current swing and high output resistance we have Wilson current mirror which use negative feedback.

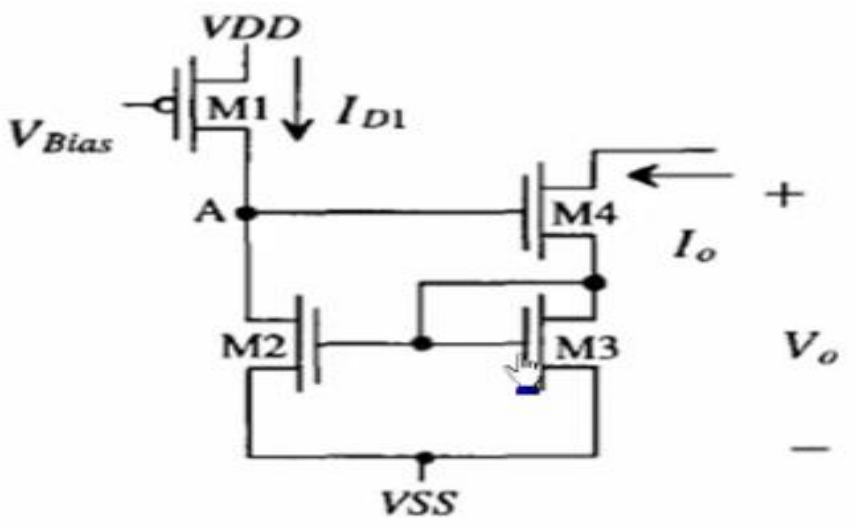

Fig 1.6 Wilson current mirror.

So here because of negative feedback, drain current is stabilized. Here M3 is diode connected and provide the feedback to M2 transistor. Here Io is stabilized and the output resistance is somewhat higher than the cascode current mirror.

$$\text{Ro} = r_0 + g_{m2} * r_0^2/2$$

CHAPTER 2

LITERATURE REVIEW

Zushu Yan et.al.[1] : In this paper they basically has worked on for better power and area with enhancement of gain, GBW by using nested current mirror which is significantly used in various LCD application. They used nested current mirror technology for a single type stage amplifier to have sustainable enhancement of a DC gain, slew rate and GBW. They have used 4-step and 3-step NCM amplifier and was fabricated using 180nm technology. In the first 3-step process they have achieved 72db DC gain and .0028-.27 MHz GBW and $>80^0$ phase margin. In the other 4-step NCM they have achieved more efficient result that is 84db DC gain with 0.013-1.24 MHz of GBW and $>62^0$ phase margin over with the power 3.6µW over 1.2 supply voltage. They basically introduced the NCM amplifier that has single stage with enhanced design flexibilities to optimize results in gain, GBW and slew rate.

Jun Zhou et.al. [2] : In this paper, they are implementing the voltage level shifter for energy efficient and fast operation with wide –range of voltage converting from a very low subthreshold voltage to I/O voltage. The proposed shifter has used modified Wilson current mirror which gives them significantly improved parameter over power and delay utilization which gives us a large voltage to convert from , they have implemented in 180nm CMOS technology and improves leakage power, switching energy and delay by up to 29×, 19×, 3× respectively , when we convert .3V to voltage ranging from .6V to 3.3V or more precisely this work has 1.03 FO4 delay parametyer with , 39 f Joule of energy/ transition and 160 pW leaked power when we convert .3 to 1.8 V. The proposed circuit has good response when scaling the input voltage and has very low sensitivity to temperature, process changing.

Seungwoo Jung et.al. [3]: In this paper, they have investigated the response of single-event transient (SET) answering of different current mirror which are been designed in C-SiGe HBT using SOI technology. They examined the feasibility in the inverse-mode to lesson the single event effect. So according to the result discussed they observe the operation of this current mirror in extreme- environment. First current mirror NPN circuit was preferred in spite of the cascode current mirror NPN because of the large SET tolerance compared to the cascade current mirror with respect to lower peak transient, the smaller area across the HBTs

and the shorter settling time. But if the higher output impedance is required then cascade current mirror is preferred but it then now has a low output swing. Second, if we use PNP SiGe circuit, then NPN SiGe HBTs in the making of a current mirror circuit then the ac transient of the input and output is shorter. The inverse-mode PNP current mirror can mirror the Iref current on the output terminal by correct mirror- ratio.

Sinan Li and S. Y. Ron Hui.[4] In this paper, they have examined that the imbalance of the current in light –emitting diode LED string arranged in parallel it can cause large current and excessive stress on LED's and that can reduce the life of the system. The paper explained that how and why the existing current mirror circuit is not perfect and cope up in open fault LED circuit and then proposed the self-configured current mirror circuit that withstand the open circuit problem in LED system with Parallel LED string. The open circuit problem here means that the LED system will be functioning if one of the LED string is switched off. They have tested the same using 75W LED system with three parallel string.

Shien-Chun Luo et.al.[5] In this paper they have proposed a different Wilson current mirror for the application level shifter which is used to convert sub-threshold voltage into standard input voltage, this paper has the operating range from subthreshold to input supply voltage. The proposed structure has the hybrid combination of modified Wilson current mirror and CMOS gates. The proposed circuit is simulated and verified using 65nm technology. The minimum voltage that can be operated using this is 300mV or 200mV. The area consumed by it is 4.2µm.

A.J. Lopez-Martin et.al. [6] :In this paper, they have proposed the AB current mirror which has improved parameter like high output impedance, low in out impedance, low power consumption, good current handling capability. They have used a passive component like a capacitor in their circuitry to examine the current mirror circuit, they have also used the cascade current mirror technique to achieve the higher output impedance but here the swing of the output in low. They have achieved the input resistance of 15.79ohm and output resistance of 650.8 M ohm with a bandwidth of 97.58MHz from the previous result which is their input resistance17.61ohm and output resistance of 11.73M ohm with a bandwidth of 96.97MHz which was almost equal to the proposed work. The presented work has more no of the transistor as compared to previous work so the area is significantly more as compared to previous work.

GF paulik et.al. [7] In this paper, they have derived the mathematical model of a differential amplifier having a current mirror as a load. They have examined the DC output voltage with respect to input voltage, current gain and early voltage. Previously VO output voltage does not consider the base current which causes the mismatch in the result examined practically and theoretically. So they have found out the output voltage considering the base current, supply voltage, and gain. The derivation says that the with a change in the Vo value will have an inverse relation with gain and Vo will reach a maximum of one. The result shows the consistent result with PSpice and LT spice simulation.

Long Xing Shi et.al. [8] : In this paper, they have implemented a mixer that requires the characteristic of a current mirror to get linearity. The proposed circuit has current mirror embedded in the switched pair, the mixer is implemented using 180nm CMOS technology, with the frequency band of .5 to 3GHz. The measured result has a gain of 9.5dB, 10dbm and having a noise figure 16.5dB. This result indicates that the mixer is used in a very low voltage communication application like OFDM and CDMA receiver. The power and die area of a mixer is 5.4mW and $0.1mm^2$ with 1.5V supply voltage.

Si Nan Li et.al. [9]: In this paper, the problem of imbalance current is resolved by using the self-configurable mirroring circuit. In simple mirror circuit one Iref current is selected and according to it other current sources can have a mirroring current but a self-configurable mirror circuit will dynamically confirm best current branch and make it a reference current for the circuit .The principle has a transistor-based circuit that balance the current and can be operated in both linear and saturation mode. The proposed control circuit don't need an additional power supply on the control circuitry of it. Proposed circuit can be made more precise by using an op-amp circuitry in the design. The design also gives the low cost and more current balance with very less power consumption which is 2.5% of the total supply voltage. This paper provides the solution to reduce the imbalance of the current in multi-string LED system.

R.A. MacLachlan et.al. [10]: In this paper, they have discussed that the new way of quad layouting the current mirror circuit will make it almost unconcerned to temperature. As cascode mirror is used for the high output impedance then the quad layout of the cascade current mirror is theoretically and practically examined and found that the output impedance of the cascode is not remarkably overripe by the change in temperature value if quad layout is

done. This layout will make the changes equal on both the side hence making the transistor identical so there is no influence on the output resistance in current mirror on changing the temperature of the proposed circuit.

S. Lee et.al.[11] :In this paper they have designed a band gap reference circuit, the error due to mismatch of temperature the current output core a current mirror incorporated in the circuit. The experimental result shows output voltage achieves by the circuit is 497.2mV at 25° C having the temperature coefficient of 28.3ppm /°C between -40°C to 80°C, the area occupied by the circuit is 0.0337mm² and dissipates 276.6pW with a input voltage 1.2V. So to reduce the error by the difference in the temperature for the output device and BGR device they proposed this paper.

C. Laoudias et.al. [12]In this letters they have proposed the LVACM that can be adjustable according to the change as there is mismatching of the various parameter, a desired feature of current mirror is hard to get so many adjustable current mirrors is proposed so this paper offers the low-voltage capability of operation, using only NMOS transistor biased and bidirectional adjustment of the gain parameter. Here the current gain is not electronically adjusted instead the aspect ratio will determine the gain of the circuit so-called programmable gain.

Mehdi Saberi et.al. [13] : In this paper, they have proposed a very low power level shifter which uses Wilson current mirror to shift the sub-threshold supply voltage to above threshold voltage. The proposed circuit uses modified Wilson current mirror with inverter head with a different gate voltage for PMOS and NMOS transistor that start to reduce the power utilized by the circuit. The proposed work is simulated on 180nm CMOS technology with a shifting value from .35V to 1.8V and having a propagation delay of 47.9ns with a power consumption of 29nW and a power-delay product of 11fJ for 1MHz of the input signal. The proposed circuit uses a diode-connected transistor that reduces the power consumption of the circuit with a very low level of shifting capacity as compare to other work.

Mohan Julien et.al. [14]: In this paper they have formalized to evaluate the active-input current circuit. The active-input current circuit uses negative feedback to enlarge the bandwidth for improving the settling time we have shown that going further with larger output current dynamic or greater current copy accuracy involves a decrease of the maximum

speed reachable before going unstable. Using this formalism to quantify this limit will let designers easily discard or validate this solution for their current source architectures.

Dongwoo Ha et.al.[15][23]: In this paper they have implemented the high order temperature compensated current bandgap reference for automotive application where they used one BGR to produce concave upward and concave downward which are combined to have highly précised current, also uses a different resistor to compensate temperature coefficient due to the resistor. The circuit operates in wide temperature range of -40°C to 150°C, with 3,3 V power supply and BGR provide the voltage of 861mV with a temperature coefficient of 75ppm/°C, with an area of 0.0249mm².

Kriangkrai Sooksood et.al. [16]: In this paper, a bulk driven simple and cascode current mirror is desined, this technology of bulk driven is used to reduce the threshold voltage limitation. Highly accurate characteristics is achieved through negative feedback over a large range of current. The proposed circuit implemented in CMOS 180nm technology with a supply voltage of 1V, and with the headroom value of 0.11V and 0.16 V for simple and cascade bulk driven mirror. Current range achieved has a range of 10nA - 100µA is achieved with 11% current unmatched for simple current mirror and 0.2% maximum error for cascade current mirror.

Nidhi Bansal et.al. [17] In this paper they have discussed over the current subtractor according to modified Wilson current mirror having a stabilized output without any error, the design is implemented using PMOS transistor with a negative feedback. The proposed circuit has a wide application and used in various analog circuitry like op-amp, oscillators. The design is implemented using cadence virtuoso180nm CMOS technology with input voltage of .8V the circuit implemented has a wide operating range from 0nA to 600µA and has a high output impedance in mega ohms and low input impedance. The percentage error is less than 1.82% .

Sven Lütkemeier et.al. [18] In this paper, they have implemented the level shifter that can easily shift and subthreshold voltage to a significant above the threshold value. The circuit uses the Wilson current mirror and does not require a static current flow and thus can save a static power. The circuit is implemented using 90nm CMOS technology and works

significantly well for a supply voltage of 100mV to 1 V. the design has a propagation delay of 18.4ns with a static power of 6.6nW. The energy per transition is 93.9fJ.

Raguvaran.E et.al. [19]: In this paper, they have implemented the current mirror having a high output impedance when operating in the very low current. The circuit samples out the output current to have a good output resistance with good voltage range. The circuitry has its output resistance $g_m * r_{out}$ times the resistance achieved from super Wilson current mirror circuit. The circuit works well for a very low input current in µ range from 5µA to 40µA due to the diode connected PMOS. All the other circuit discussed here does not work well in low input current due to the presence of negative leakage current. The mirroring error is less than 1% for 5 to 40uA current range. The proposed circuit can be used in various application that require high output impedance working on a very low currents.

N. Raj et.al.[20]: In this letter, they have implemented the cascode current mirror which can be self-biased a low voltage, the high-performance self-biased bulk driven methodology is used and the work validation is approved by small signal analysis over conventional way of self-biasing the circuit. In this letter, they have achieved high bandwidth with low input impedance and high output impedance with the operating range of 0- 200µA. In this paper, it is observed that the input impedance of the circuit reduces by four times and bandwidth increases by three times. The simulation is been carried out in HSpice using 180nm CMOS technology.

Christoph Tzschoppe et.al.[21] In this paper, they have designed the advanced current mirror using the series or parallel connected transistor for the application where low voltage is required as in case of portable devices. They showed that the implemented technique has two times the output resistance compared to the simple current mirror and 50 times the cascade current mirror output resistance. They described the whole concept of the transistor connected in the series with analytical equation.

CHAPTER 3

SCOPE OF STUDY

As the technology is advancing we are moving on a world where we need to work in application like mobile's , smart phone, smart LED, Rocket science , Space technologies, Medical applications and many more and there is one thing in common that they all need to achieve three things less power consumption, less delay of the circuit and less area . So in a various application like biomedical operates on very low voltage which needs a very high output impedance current mirror. The current mirror is the circuit that implements the principle that if a gate-source voltage of two uniforms MOS transistors is same then their channel current flowing would be equal. In the current mirror, we generate a current reference so to copy that current in various current sources in the system. Various advancement in the technology of CMOS design integrated most of the circuits in the same chip who all are working on very low supply voltage like radio frequency processor and various sensor like temperature and baseband signal processing circuit require very low voltage supply. Getting a very large impedance and wide output range and swing is the important parameter when working on the very low input voltage.

So the high output resistance will be very benifical for the circuit , as having the high output resistance will have more fan out which will be benificial to drive more circuit connected to it. Current mirror is a circuit which has the principle that V_{gs} gate-source voltage of two similar MOS transistors is identical then it's channel current should be same. In the current mirror, we generate a current reference so to copy that current in various current sources in the system. So now how we do that current reference equal to the output current is done by making the gate-source voltage in the two transistors equal .

Designing the layout of the circuit will give us the picture of how much area does my circuit will occupies and how my circuit would behave when all the parasitic of the circuit would be add to it. When working on or fabricating the IC there are varies issues due to process variation or due to mismatch which can make our desired output wrong, so all these analysis should be done to know the actual yield of the circuit to get how my circuit would actually behave on the hardware part.

CHAPTER 4

RESEARCH METHODOLOGY

4.1 CURRENT MIRROR

A circuit used in most of the analog circuit to provide the biasing voltage to turn on the different component of the circuit. Basic simple current mirror can be implemented using PMOS or NMOS based on the application. A basic current mirror has two MOSFT and they work on a simple principle that if their gate to source voltage is same than the current passing through the transistor is equal.

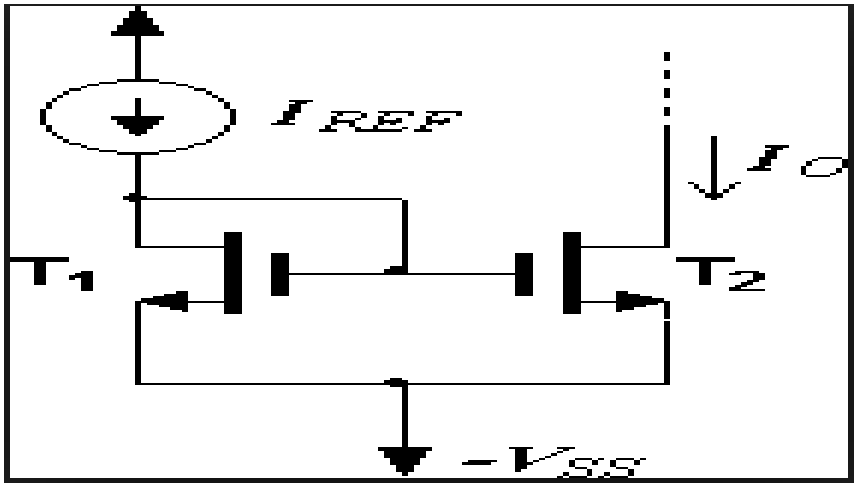

Fig 4.1 Simple current mirror

So as shown in the above fig that T1 is in saturation mode means the drain to source voltage is greater than equal to gate to source voltage and cause T2 to be in saturation

Current in a transistor is given by

$$\mathrm{I} = \frac{1}{2}\mu\mathrm{n}\ \mathrm{cox}\left(\frac{\mathrm{w}}{L_1}\right)\left(V_{gs} - \mathrm{vth}\right)^2$$

If we include channel length modulation then the equation become

$$\mathrm{I} = \frac{1}{2}\mu\mathrm{n}\ \mathrm{cox}\left(\frac{\mathrm{w}}{L_1}\right)\left(V_{gs} - \mathrm{vth}\right)^2(1+\lambda V_{ds1})$$

Where V_{ds1} is drain to source voltage,V_{gs} gate to source voltage, $\frac{\mathrm{w}}{L_1}$ is the width to length ratio, λ is channel length modulation constant.

Now according to the current mirror circuit we have and excluding channel length modulation current through T1 transistor is given by.

$$I_{ref} = \frac{1}{2}\mathrm{un}\ \mathrm{cox}\left(\frac{\mathrm{w}}{L_1}\right)\left(V_{gs1} - \mathrm{vth}\right)^2$$

And the current through T2 transistor is given by

$$I_0 = \frac{1}{2}\text{un cox}\left(\frac{\text{w}}{L_2}\right)\left(V_{gs2} - \text{vth}\right)^2$$

So now as the principle says that the gate to source voltage has to be equal then considering the action of output current to input current we have

$$\frac{I_0}{I_{ref}} = \frac{\left(\frac{\text{w}}{L_2}\right)}{\left(\frac{\text{w}}{L_1}\right)} * \frac{\left(V_{gs1} - \text{vth}\right)^2}{\left(V_{gs2} - \text{vth}\right)^2}$$

So as V_{gs1} and V_{gs2} is equal then the ratio become $I_0 = \frac{\left(\frac{\text{w}}{L_2}\right)}{\left(\frac{\text{w}}{L_1}\right)} * I_{ref}$.

So from this above equation we get to know that if the two transistor are identical having same W/L ratio then the I_0 current can easly track out the I_{ref} current and hence the basic operation of current mirror is achieved.

Now if we include channel length modulation in the equation then

$$\frac{I_0}{I_{ref}} = \frac{\frac{1}{2}\mu\text{n cox}\left(\frac{\text{w}}{L_1}\right)\left(V_{gs1} - \text{vth}\right)^2(1 + \lambda V_{ds1})}{\frac{1}{2}\mu\text{n cox}\left(\frac{\text{w}}{L_1}\right)\left(V_{gs2} - \text{vth}\right)^2(1 + \lambda V_{ds2})}$$

From the above equation it difficult to make I_{ref} equal to I_0 as now the ration depends on the drain to source voltage also.

4.2 CASCODE CURRENT MIRROR

so now we move to next type of transistor that is cascode transistor where the problem of this channel length modulation is resolved by making this drain to source voltage equation. So now to have high impedance as it will make the current constant regardless of the change in the output voltage and to resolve the problem faced in simple current mirror we move to cascode current mirror.

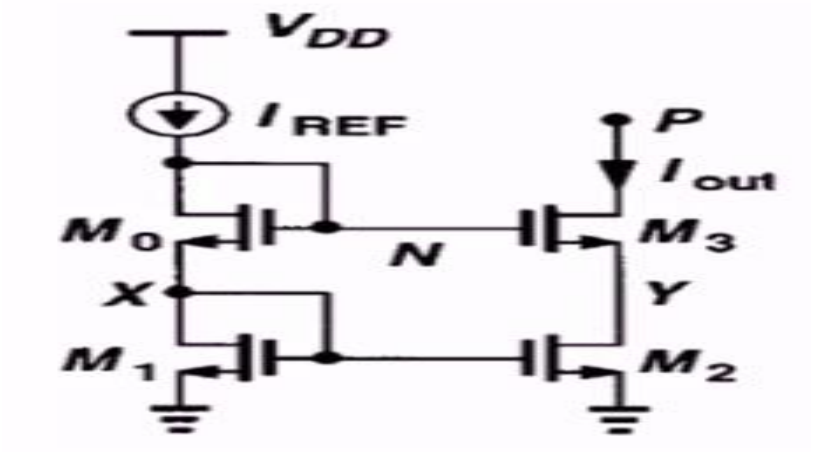

Fig 4.2 Cascode current mirror

Now At node N we give Vbias to both of the gate of M0 and M3 transistor to make V_{gs0} equal to V_{gs3}.

So voltage at both the side is V_{gs0}+Vx = V_{gs3} +Vy

Now to make both of them equal proper similar dimension of the transistor is taken

$\frac{W}{L_3}*\frac{W}{L_0}=\frac{W}{L_2}*\frac{W}{L_1}$

Which gives $V_{gs0} = V_{gs3}$ and hence finally $V_X = V_Y$ so hence CLM problem is removed as now drain voltage of both the transistor is same by using cascode current mirror. Now calculating the output resistance of the cascade circuit we draw its simple small signal model as shown below.

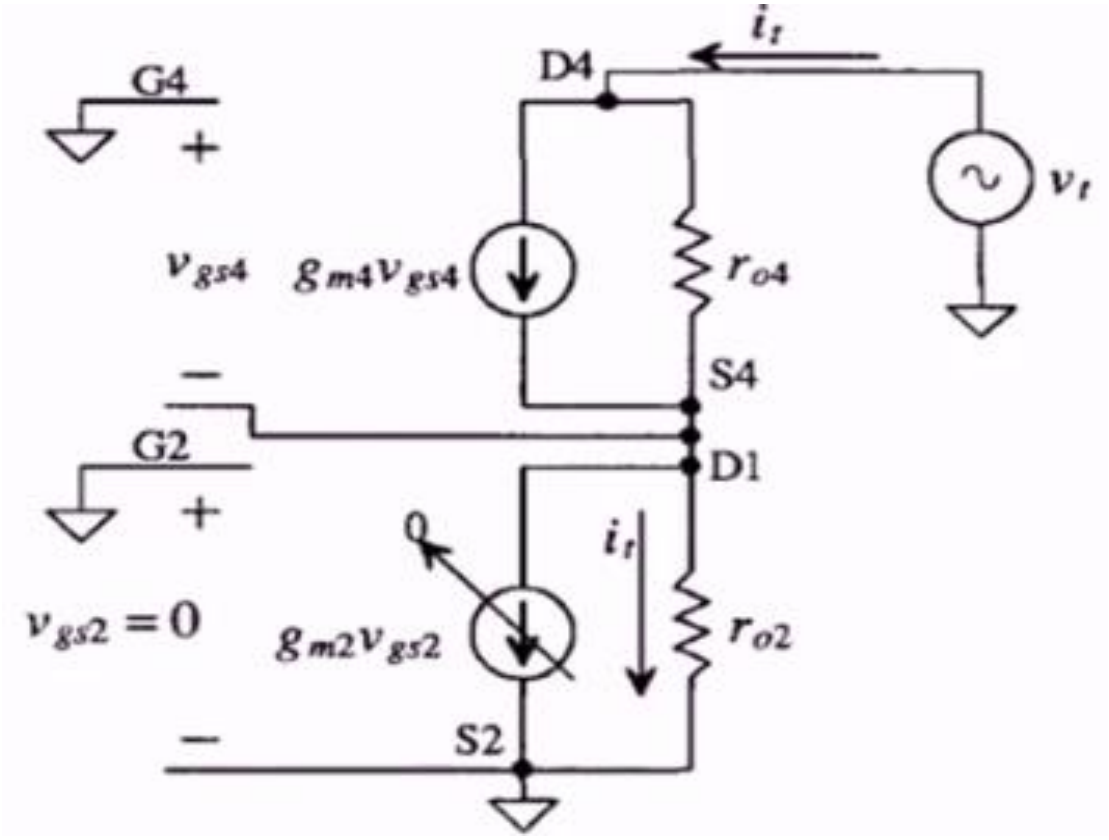

Fig 4.3 Cascode current mirror small signal.

Now the output impedance of the circuit is given by $\frac{V_t}{I_t}$

So total current flowing through the drain to source is given by the equation and

$$I_t = gm_4 v_{gs4} + \frac{v_t - (-v_{gs4})}{ro_4}$$

$$v_{gs4} = I_t * ro_2$$

So substituting the value of V_{gs4} in I_t , we get

$$\frac{v_t}{I_t} = ro_4(1 + gm_4 * ro_2) + ro_2$$

$$R_0 = gm_4 * r_o^{\,2}$$

So the resistance here is large than the simple current mirror by $g_m * r_0$ times hence this resistance is large. Now talking about the swing of the voltage in cascade transistor that is the only limitation in this mirror as swing is defined as the Vdd – Vomin. And here Vomin is large than the required minimum voltage. Vomin is the minimum voltage required for the transistors to be in saturation mode. Ideally, Vomin for the cascode circuit is 2(V_{gs} -Vt) but from the circuit we, get Vomin higher than the ideal which is 2V_{gs} -Vt, which is Vt times higher than the ideal voltage. So now how we can reduce the Vomin we can simply do one thing is that we can resize the input transistor in such a way that we can get Vomin as 2(V_{gs} –Vt) or 2ΔV where ΔV is called the over drive voltage.

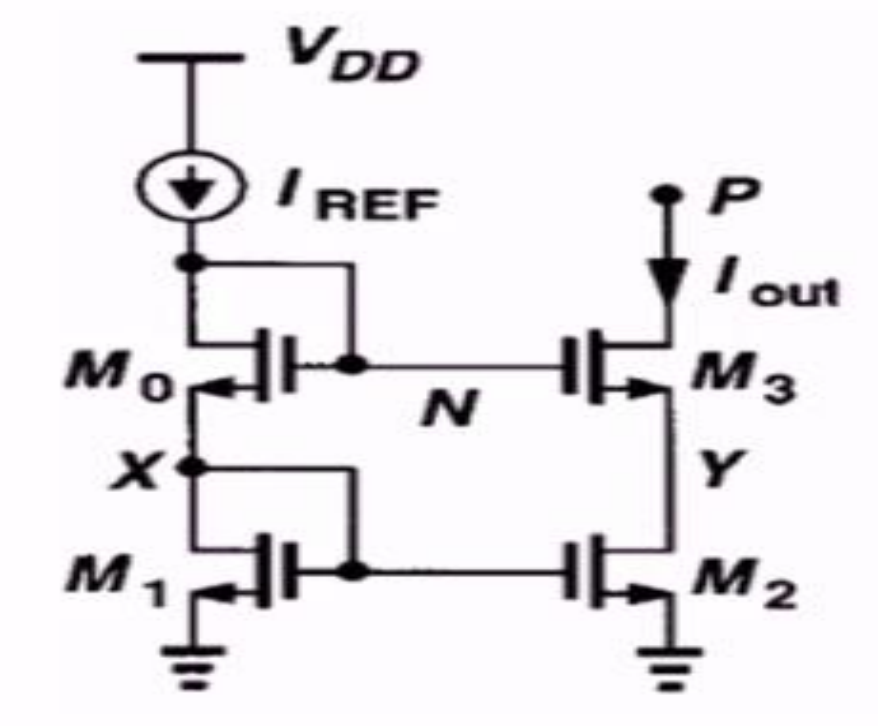

Fig 4.4 Cascode current mirror

4.3 MODIFIED CASCODE CURRENT MIRROR

Now Vomin we are getting is $2V_{gs}$ –Vt now if we can somehow provide the M3 transister V_{gs} + Vt at the gate terminal then we can get Vomin as 2ΔV. So this problem can be solved b

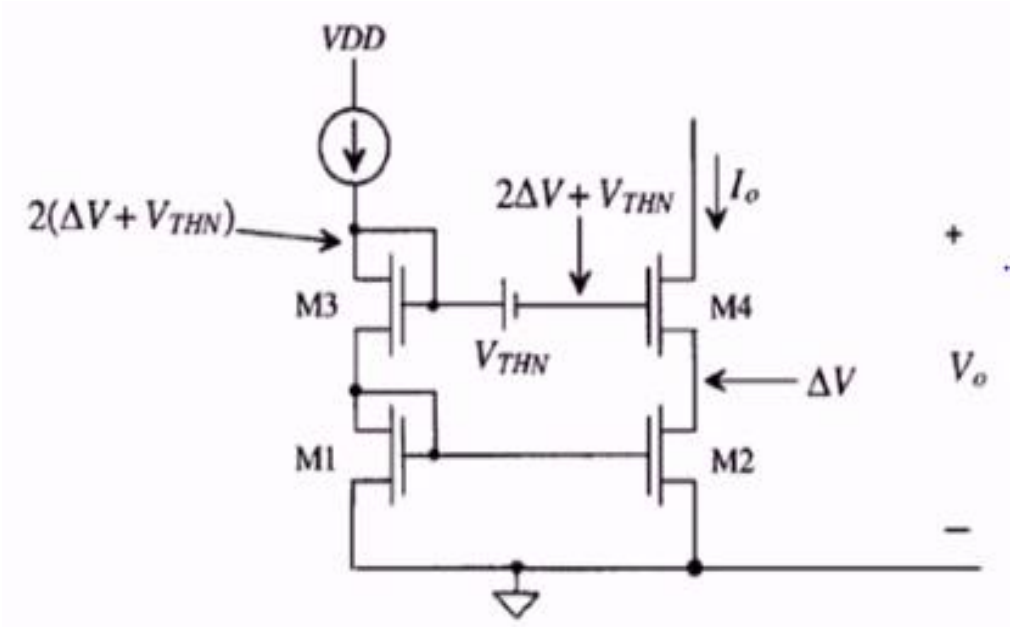

Fig 3.5 Modified cascode current mirror

Now if we modify the circuit as we resize the width of the transistor then also this problem can be resolved.

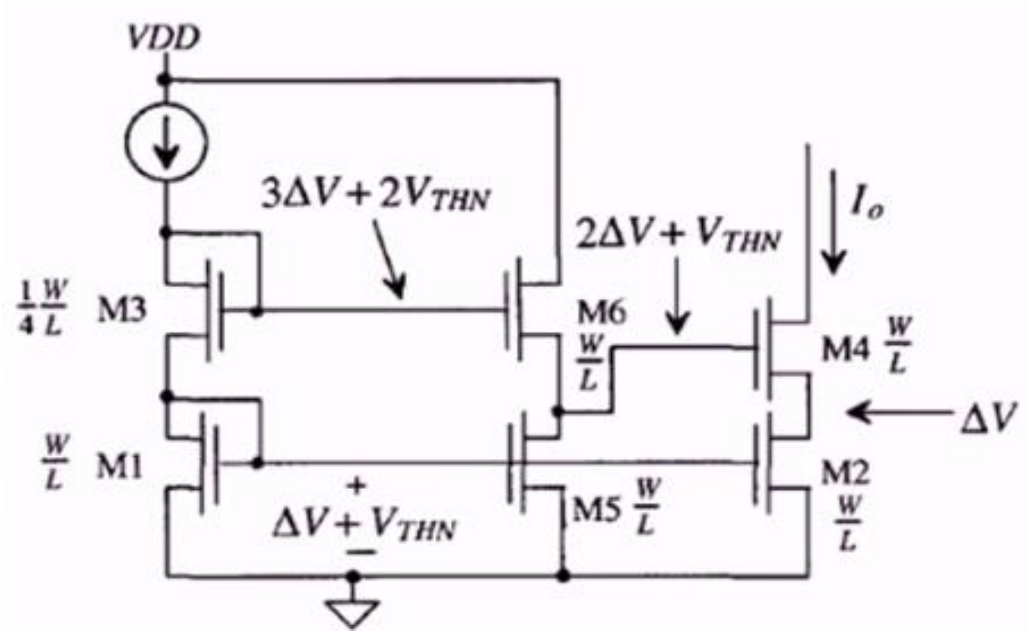

Fig 4.6 Modified cascode current mirror

4.4 WILSON CURRENT MIRROR

So now we move to next type of current mirror with wide current swing and high output resistance so we have Wilson current mirror which use negative feedback.

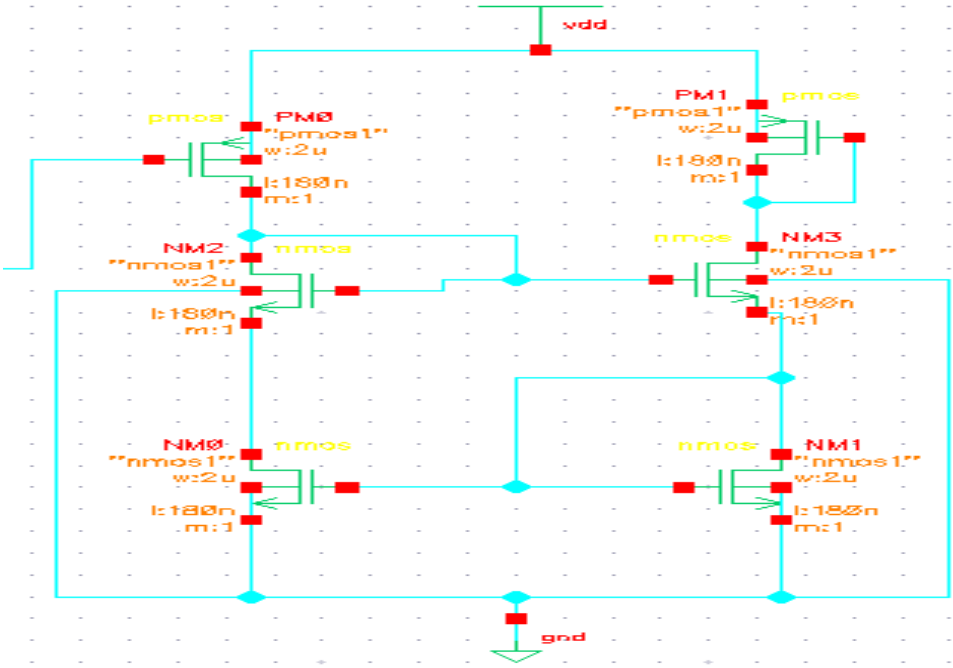

Fig 4.7 Wilson current mirror

From the fig it can be decided that the Wilson current mirror is similar to cascode current mirror but here with negative feedback. Here 6 transistor is used to implement the circuit where PM0 act like a current source and PM1 act like a load resistance or act like a diode and is always in saturation mode. Now the gate voltage at NM3 transistor will make some current to flow through and NM1 is in saturation mode then suppose current flowing through that branch is I_3 as both the transistor NM1 and NM0 are identical with same gate to source voltage so I_2 current will be flowing through NM0 transistor hence the output transistor NM1 makes equal current I_2 to flow through input transistor.

CHAPTER 5

MATHEMATICAL MODELLING

The proposed circuit is the combination of both the PMOS and NMOS where most of the MOSFET works in saturation region and are diode connected. It has seven transistor including the load and current source MOSFET. The base paper implemented was designed with the help of BJT but here we have considered all MOSFET as MOSFET has various advantages over BJT like input resistance in high in MOSFET which is desirable for the amplifier, easy to manufacture, MOSFET much smaller than BJT, less noisy than BJT. So these all advantages make MOSFET more use full than BJT. Now the circuit is shown below in fig-

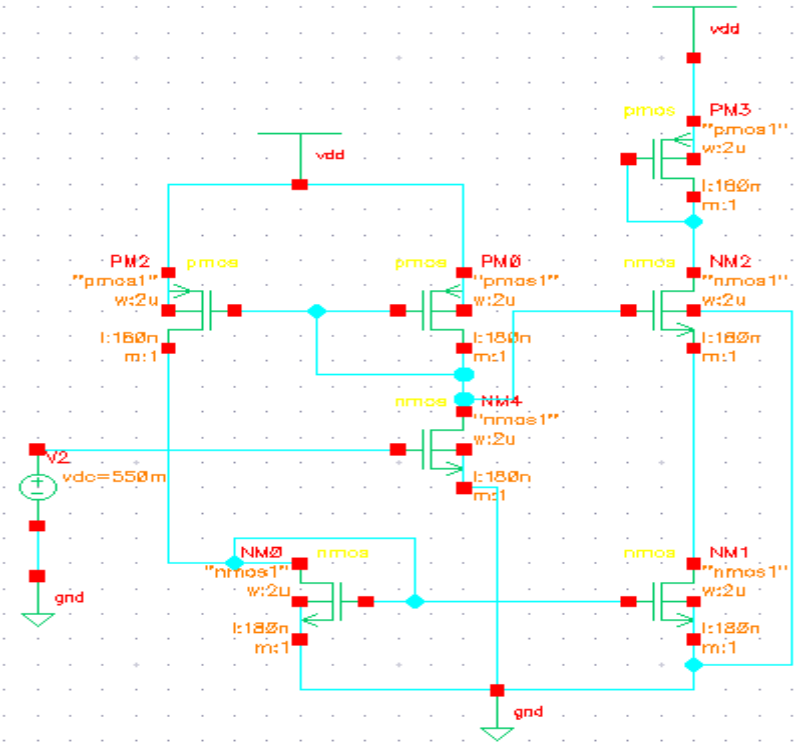

Fig 5.1 Folded cascode current mirror.

In the circuit shown PM3 MOSFET act as a driving load which act like a diode working in a saturation region always. The transistor NM0, PM0 also work as a simple diode connected, basically in comparison to simple cascode current mirror from fig-5.1, we are folding the NM MOSFET here into PM2 and PM0. So a small signal model is needed to know the analysis where transistor NM0, PM0, PM3 will be simple act like a diode and easily replaced by simple resistance value in a small signal model. So basic small signal for the same is drawn

for the transistor NM1, NM2, PM2. NM2 transistor will act like a current source and will provide the reference current which is going to be mirrored to the NM2 drain terminal.

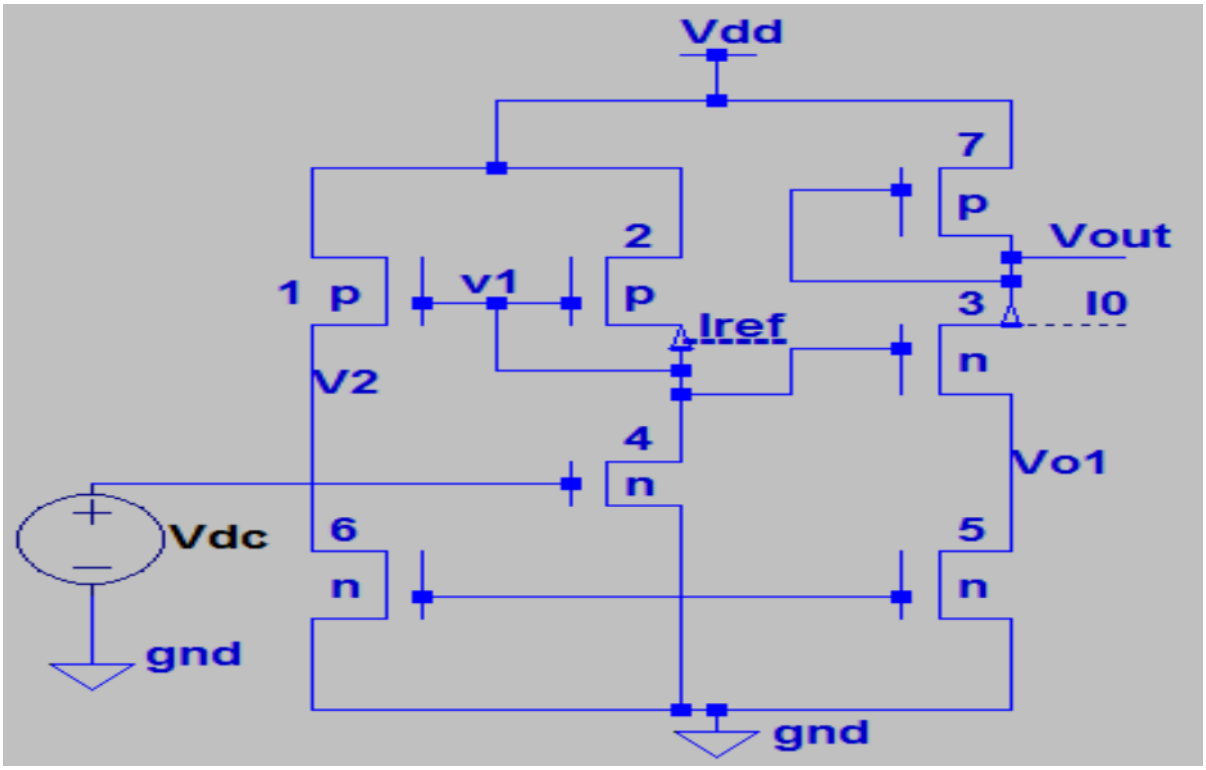

Fig 5.2 Folded cascode current mirror.

Its small signal model is as shown below

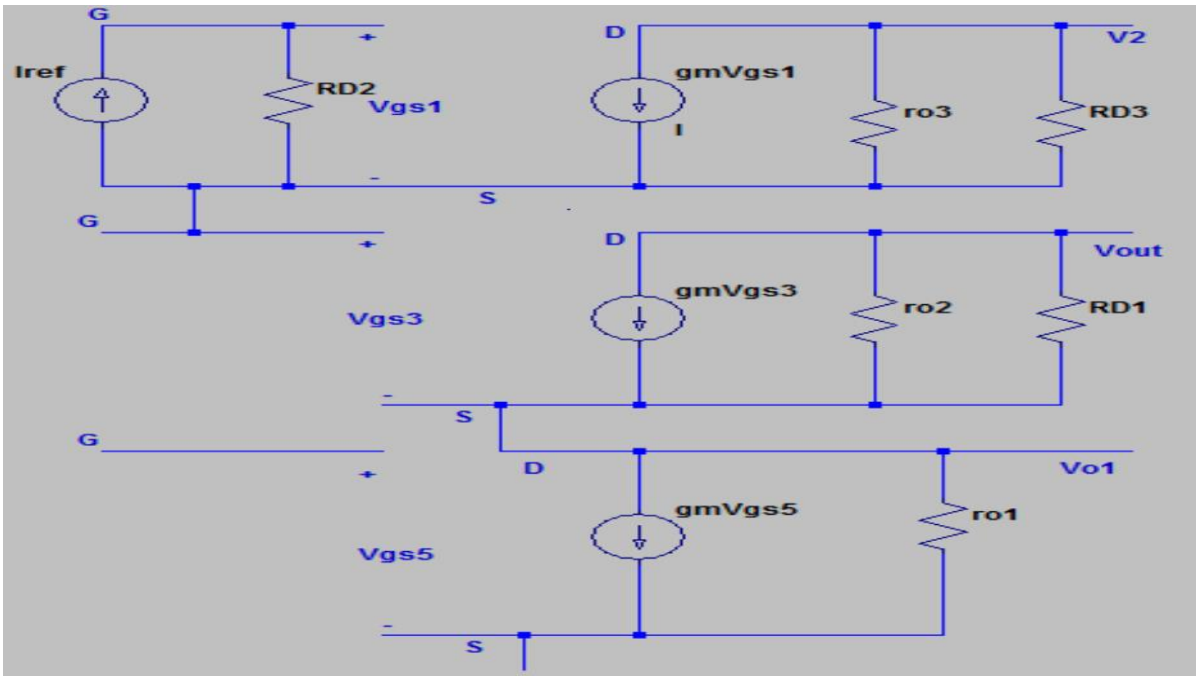

Fig 5.3 Small signal model of folded cascode current mirror.

So basic idea for me to solve this is by coming from the output side to the input side so we have transistor no 5 and 3 at the output side of the circuit. Then considering the 5 transistor we have voltage across drain to source of 5 transistor is

$$Vo_1 = g_m * r_{01} * V_{gs5} \quad \text{.....Eq-1}$$

And the current through the 3 transistor is given by

$$\frac{V_{out} - V_{o1}}{\frac{r_{02} * R_{d1}}{r_{02} + R_{d1}}} + g_m * V_{gs3} = 0 \quad \text{.....Eq-2}$$

Now from the circuit we get to know that the value of gate to source voltage for 3 transistor is

$$V_{gs3} = V_{g3} - V_{s3}$$
$$V_{gs3} = V_1 - V_{01} \quad \text{.....Eq-3}$$

Now we can substitute the value of Vgs3 in equation no 2 we will get the V_{out} value as

$$V_{out} = V_{O1}\left[1 + g_m\left(\frac{r_{o2} * R_{d1}}{r_{02} + R_{d1}}\right)\right] - V_1\left[\frac{r_{o2} * R_{d1}}{r_{02} + R_{d1}}\right] \quad \text{.....Eq-4}$$

Now considering the above small signal for transistor no 1 we get.

Current in the gate terminal is given by

$$I_1 = g_m * V_{gs1} + \frac{V_2}{\frac{r_{03} * R_{d3}}{r_{03} + R_{d3}}} \quad \text{.....Eq-5}$$

And current in the drain side is given by

$$I_2 = I_{ref} + \frac{V_{gs1}}{R_{d2}}$$

Here $V_{gs1} = V_1$.

So $V_1 = R_{d2}(I_2 - I_{ref})$ ……Eq-6

Then substituting the value of V1 to equation.

$$I_1 = g_m * V_1 + \frac{V_2}{\frac{r_{03} * R_{d3}}{r_{03} + R_{d3}}}$$ ……Eq-7

Now substituting the value of V1 in equation no-7 and finding the value of g_m in respect to I_{ref} is given by.

$$g_m = \frac{I_1 + \frac{V_2}{\frac{r_{03} * R_{d3}}{r_{03} + R_{d3}}}}{R_{d2}(I_2 - I_{ref})}$$

Now this g_m is in terms of I_{ref} so now substitute this value of g_m into the eq-4 which is the the output voltage.

So now the output voltage of the transistor in term of I_{ref} is given by.

$$V_{out} = V_{O1}\left[1 + \left[\frac{I_1 + V_2\left(\frac{r_{03} + R_{d3}}{r_{03} * R_{d3}}\right)}{R_{d2}(I_2 - I_{ref})}\right]\left(\frac{r_{o2} * R_{d1}}{r_{o2} + R_{d1}}\right)\right] - V_1\left[\frac{r_{o2} * R_{d1}}{r_{o2} + R_{d1}}\right]$$

So we get to know the output voltage is related on so many parameter, there can be another way of defining the circuit. The overall output voltage Vout in term of the reference voltage is defined.

CHAPTER 6

WORK DONE

So as the topic is current mirror I have decided to work from the basic simple current mirror and analysis the practical implementation of the circuit, and knowing what actually is happening in the circuit. So I have used cadence virtuoso 180nm CMOS technology to design my current mirror.

6.1 SIMPLE CURRENT MIRROR CIRCUIT

Starting from the simple current mirror technique vary basic requirement of a current mirror is that the gate to source voltage for the transistor should be equal. So that same amount of current can be flown from the drain terminal of the MOSFET. So basic simple current mirror circuit has a current source and a two identical transistor having same body to source voltage so as shown in the figure below.

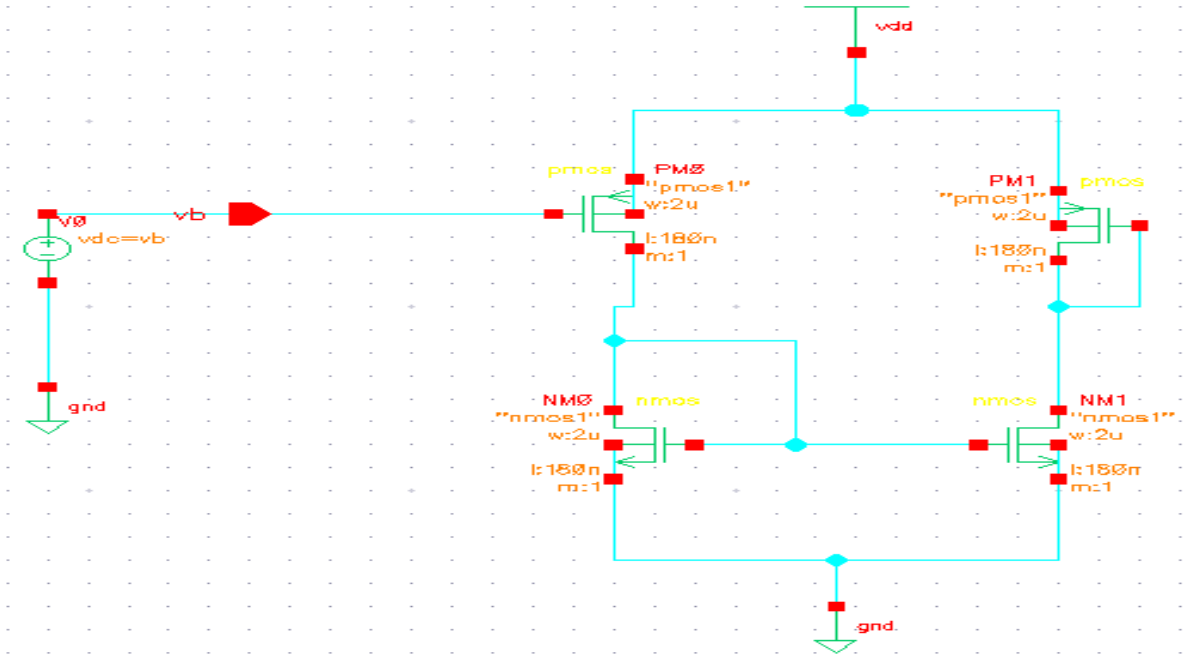

Fig 6.1 Simple current mirror circuit.

The circuit shown has four transistor, two NMOS and two PMOS transistor, where PM0 transistor is used as a current source and it provide the reference current to the circuit. So now as the body of both the NMOS is same the gate to source voltage for both the transistor is same which make I_0 current to flow through the PM1 transistor which act like a diode connected load or simply as a resistor and hence mirroring of the reference current is achieved.

Now as the above circuit is implemented the basic idea of how the basic current mirror work is done is clear. So no calculating the output impedance of the circuit can be easly calculated by V=IR formula. The result shown here is not much more accurate due to the presence of channel length modulation. So to reduce it and to get more précised mirroring current I have implemented a cascode current mirror.

6.2 CASCODE CURRENT MIRROR CIRCUIT

Cascode current parameter is much more accurate than the simple current mirror so basically due to CLM effect the current is not mirrored properly due to which we moved to other way of designing the current mirror by cascode circuit. The basic idea here is to make the drain to source voltage equal so that no mismatch of current will be their. Now as shown in the figure below.

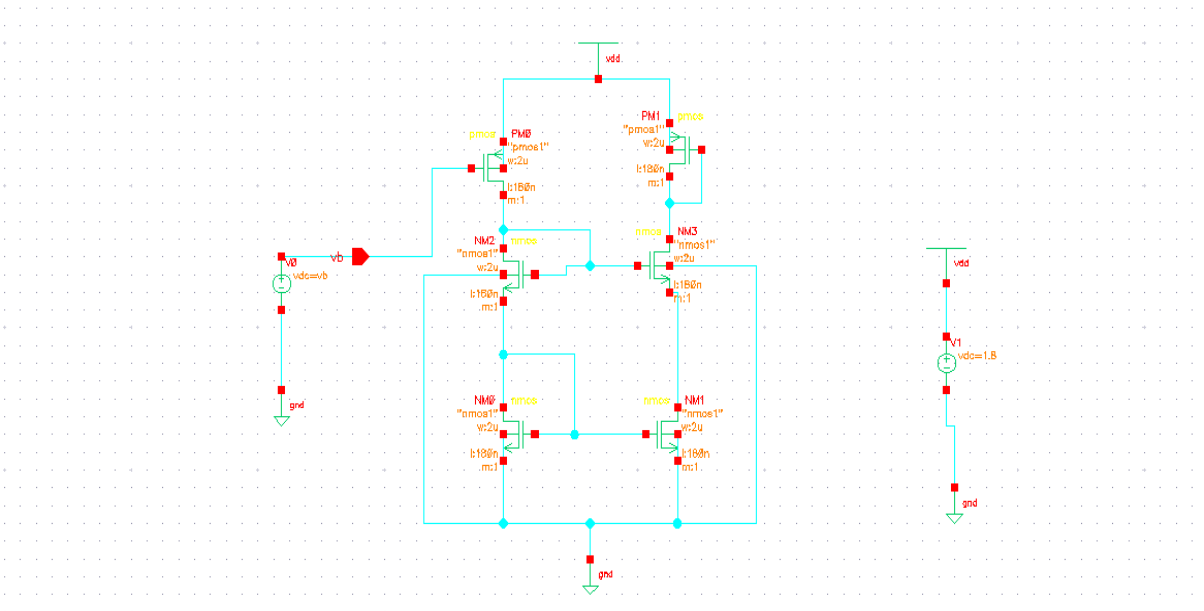

Fig 6.2 Cascode current mirror circuit

As shown in the above fig the cascode current mirror has two identical branch having total 6 transistor to the circuit , where PM0 provide or act like a current source and PM1 act like a diode connected load or simply a resistor . Now main role is of NM2 and NM3 transistor, if they both are identical as assumed then the gate to source voltage is same for both the transistor which further makes drain to source voltage identical and so the CLM problem is reduced in it and now the output current accurately tracks out the reference current. Now we

move to other modified current mirror circuit called a Wilson current mirror which is introduce to overcome the limitation of cascode current mirror that is the swing of the output voltage is less.

6.3 WILSON CURRENT MIRROR CIRCUIT

So basic idea we are implementing on the Wilson current mirror is that it uses negative feedback to make drain current to stabilize. Here the negative feedback means that the output branch parameter will be feedback to the input branch. One more important parameter analysed here is that the Wilson current mirror resistance value is somewhat similar to that of cascode current mirror circuit. As shown in fig below

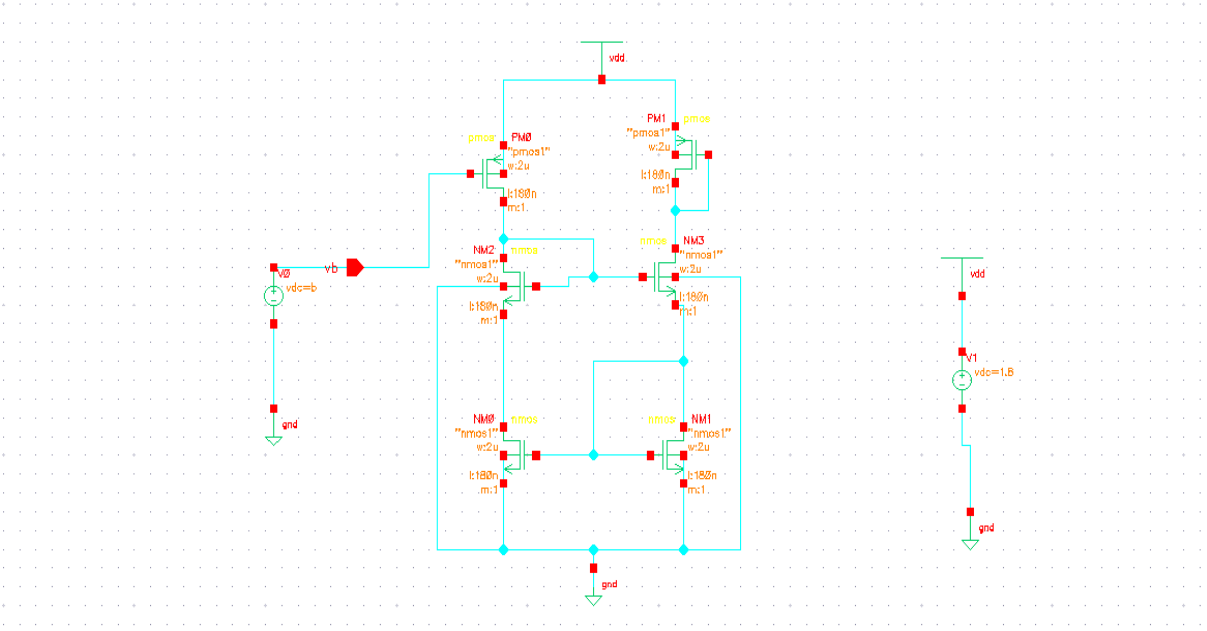

Fig 6.3 Wilson current mirror circuit.

From the fig above it can be decided that the Wilson current mirror is similar to cascode current mirror but here with negative feedback. Here 6 transistor is used to implement the circuit where PM0 act like a current source and PM1 act like a load resistance or act like a diode and is always in saturation mode. Now the gate voltage at NM3 transistor will make some current to flow through and NM1 is in saturation mode then let current flowing through that branch is I_3 as both the transistor NM1 and NM0 are identical with same gate to source

voltage so I_2 current will be flowing through NM0 transistor hence the output transistor NM1 makes equal current I_2 to flow through input transistor.

6.4 CURRENT MIRROR SUBTRACTOR CIRCUIT

Now I have implemented the current subtractor based on the Wilson current mirror to analysis the parameter and the result came out is similar to the paper who have implemented this. The current operating range for the circuit is ranging from 0nA to 600µA. Now this Wilson circuit is the combination of simple current mirror and the modified current mirror. Simple current mirror is used to amplify. The subtracted current by an amplification factor A which depend on the aspect ratio of the transistor.

The circuit implemented has all the transistor working in the saturation mode and the transistor that form the simple current mirror are supposed to be exact identical to each other so that no mismatch of the subtracted current is their the circuit is fully implemented using PMOS transistor .

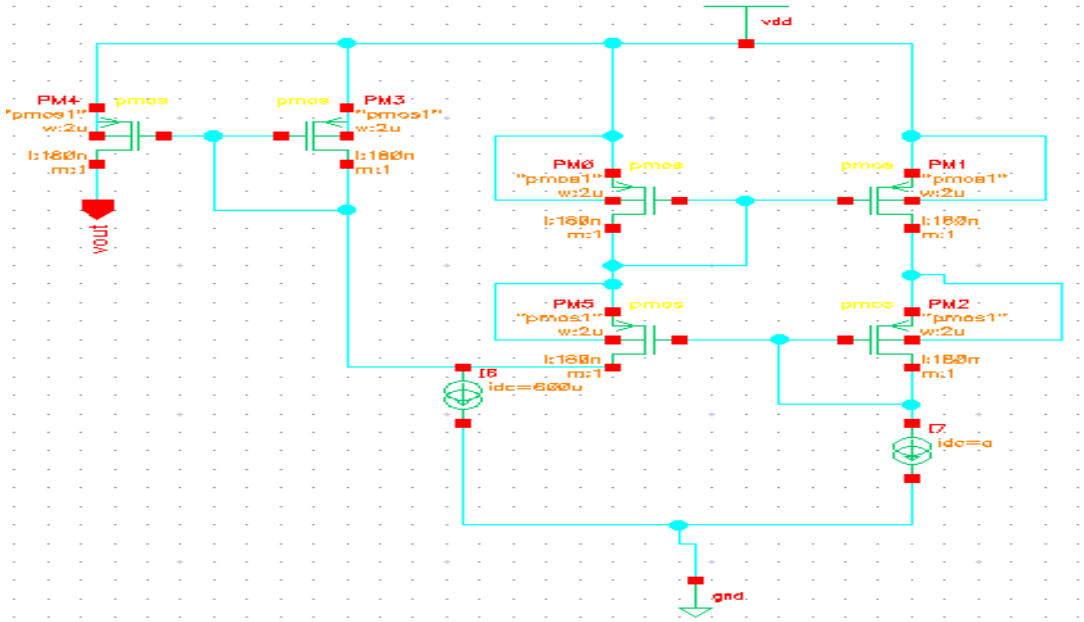

Fig 6.4 Current mirror subtraction circuit

So here PM4 and PM3 form the simple current mirror and PM0, PM1, PM2, PM5 form the Wilson current mirror that is the I2 current from PM2 tranister would be copied to the drain of PM5 transister and using KVL the current flowing through PM3 transister will be the

subtraction current that can be further mirrored to PM4 transister and amplified according to the aspect ratio, here PM4 and PM3 are assumed exact identical.

6.5 LOW VOLTAGE SUPER WILSON CURRENT MIRROR

After this a low voltage current mirror is designed that is working like a Wilson current mirror and has a cascade design in it so I have implemented the circuit and the current is perfectly mirrored with good range of values.

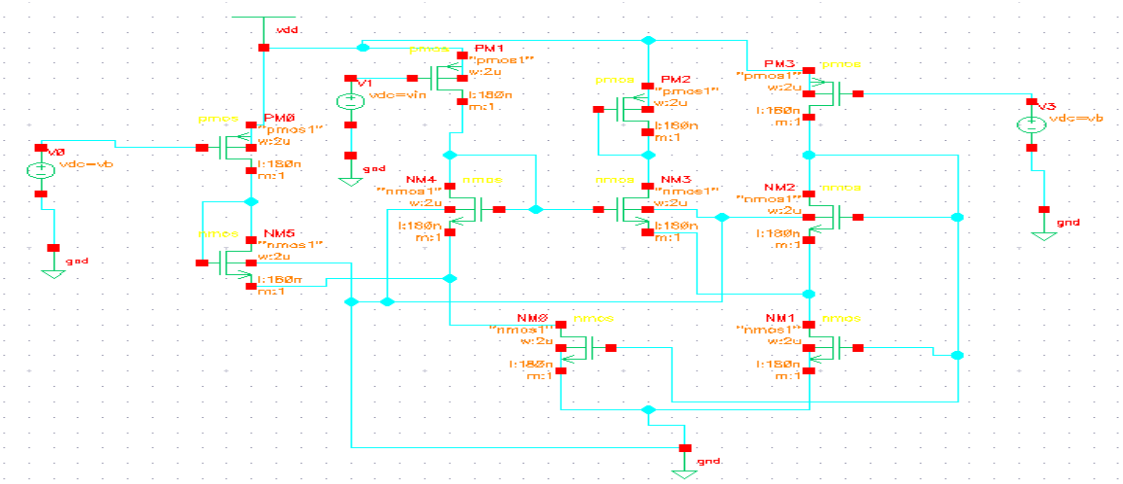

Fig 6.5 Super Wilson current mirror circuit.

6.6 MODIFIED WILSON CURRENT MIRROR CIRCUIT

In this design topology of a cascode current mirror is used , the output resistance is somewhat higher than the remaining circuit drawn but way much similar to cascade impedance value the circuit shown .

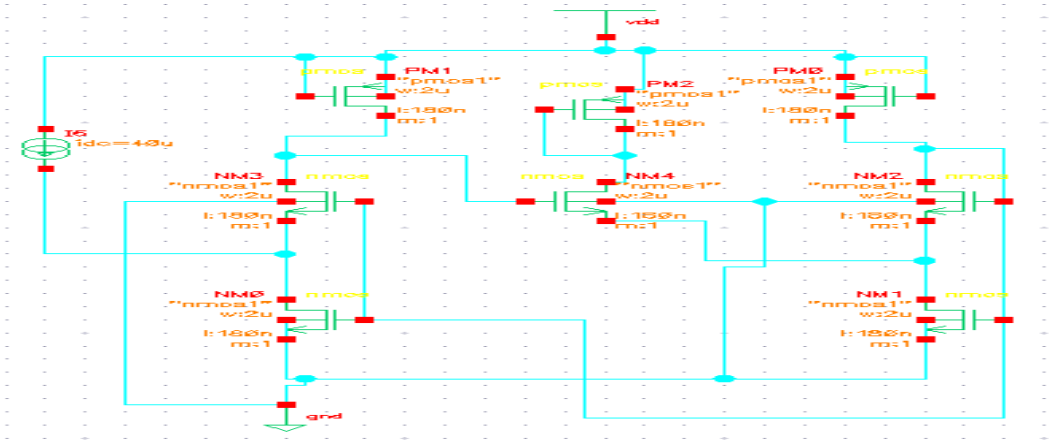

Fig 6.6 Modified Wilson current mirror circuit.

6.7 FOLDED CASCODE CURRENT MIRROR CIRCUIT

After analysing all the current mirror circuit and the modified one's that are showing good mirroring effect and high output resistance value I came to conclusion to implement the modified cascade current mirror that can have high input resistance and a wide swing .so the circuit diagram of the proposed circuitry in this paper is shown below which is showing good mirroring across the wide range of current with the high output impedance value , the mathematical modelling for the same is described in the above section .

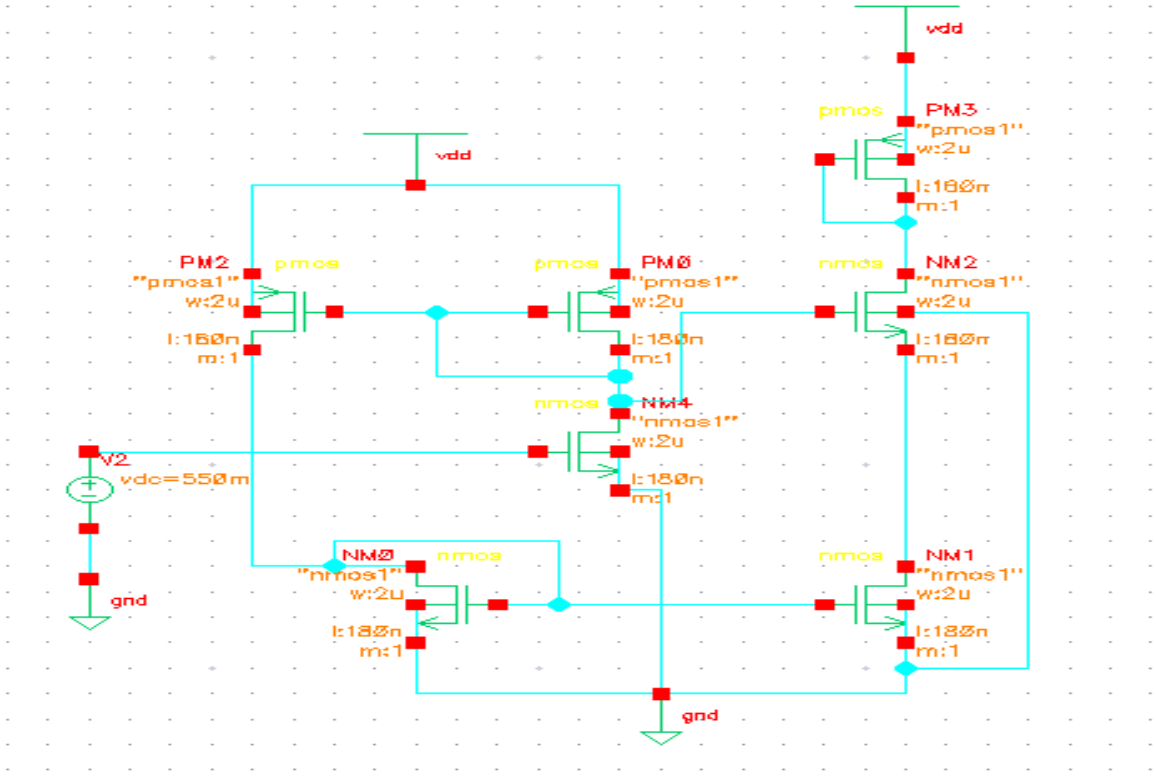

Fig 6.6 Folded cascode current mirror circuit.

The proposed circuit is a simple 7 transistor modified cascode current mirror, the base paper for this circuit is implemented in the BJT which is showing very efficient result according to output resistance as 71M ohm with the impedance bandwidth product of 2.8 ohm at 1mA output current with 1.8V input supply voltage. This MOSFET circuit implemented has the range from 100m – 800m Voltage with the exact mirroring value at 550M V. The result and discussion of the circuit is shown in next chapter.

6.8 LAYOUT DESIGN OF THE CURRENT MIRROR CIRCUIT

Layout of the current mirror is been drawn to analyse the change in the output current by including all the parasitic value like capacitor and resistance due to metals and polysilicon material, we can calculate the total amount of capacitance and resistance value by applying the basic networking rules . Designing the circuit and doing its layout design is a complete different work as there are two rules that should be matched by the design one is lamda rule and other one is micron rule. In lamda rule everything is expressed in term of lamda like 2λ or 3λ and lamda various according to the technology. After designing the layout we have to check down the DRC, LVS and A_VC which extract the parasitic values from it. DRC is the design rule check which deals with checking the design rule as per standards defined then comes the LVS which is layout v\s schematic which will compare that the connection of both the design is matched or not and then comes the A_VC which will extract all the parasitic values of the metal and poly material used in the design. Designing of the layout is the art where we have to arrange the components in such a way that it should uses minimum area with all the other design rule followed with it. If we have to consider the design approximately the area is equivalent to the product of the number of mosfet used and the total width of the CMOS. Designing of the circuit and connecting the components using metal need very precious connection , same material wire cannot cross each other or overlap each other at that time we require a second metal and a via to connect it, same way we need poly to metal or metal to poly via to connect two different material . After running out DRC and LVS we extract the parasitic values from the design and we get the new file named AV-extracted file which shows all the values given to all the metal and poly material used, by analyzing it I get to know that the polysilicon material used has more resistance value as compare to metal which will affect the overall current flowing in the design so to have a efficient layout we have to minimize the use of poly material and minimize the metal length of the connection. Designing the layout in analog world is quite a complex task as every connection is drawn manually and we have to consider which component is to placed where, and parallel we have to consider all the design rules and to minimize the area under which my circuit is drawn which will directly affect the cost of the chip.

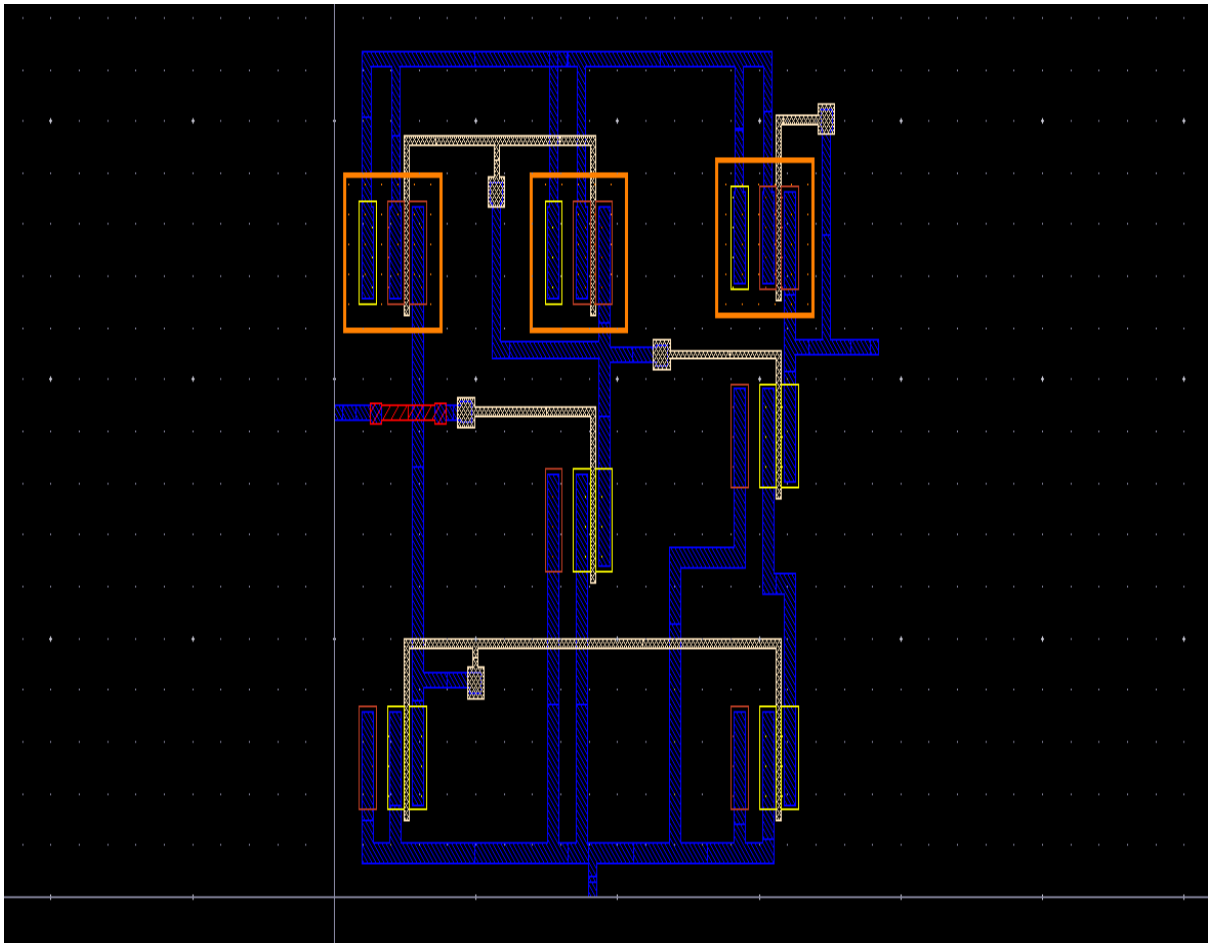

Fig6.7- Layout of CM

In the above fig is the layout design of the folded cascade current mirror where i have used 2 metal and a poly to connect all the terminal of the cmos. Blue color material is my metal one, and the red color material is the metal two which I have used so that same type of material should not overlap as that will short the connection. On designing the layout of CM we can see their as soo much gap between the component and there is large number of poly material used which will directly increase the resistance value of the overall circuit so we can reduce the poly material by manually arranging the component so the distance between the design should be minimum where poly material is used. So we have again design the circuit by considering and compressing the area of previously designed layout , new design is shown in next page where all the connection is made such a way that there should be very less poly material used and second is the metal length should be less, and the solution of minimizing the metal used can be done by starching the pin of VDD and GND which will directly reduce metal used , If we have to find out the area we can manually calculate it by placing the pointer on X-axis and Y- axis and then multiplying the total area under the circuit which will

include spacing between the component but if we have to calculate the area used by the component without spacing and all , then directly multiply the width of the component with the number of component used in designing of the circuit. In designing the folded cascade current mirror I have used total 7 component with the width of 2micro meter each which will give us the area as 14 micro meter of only the component without connections.

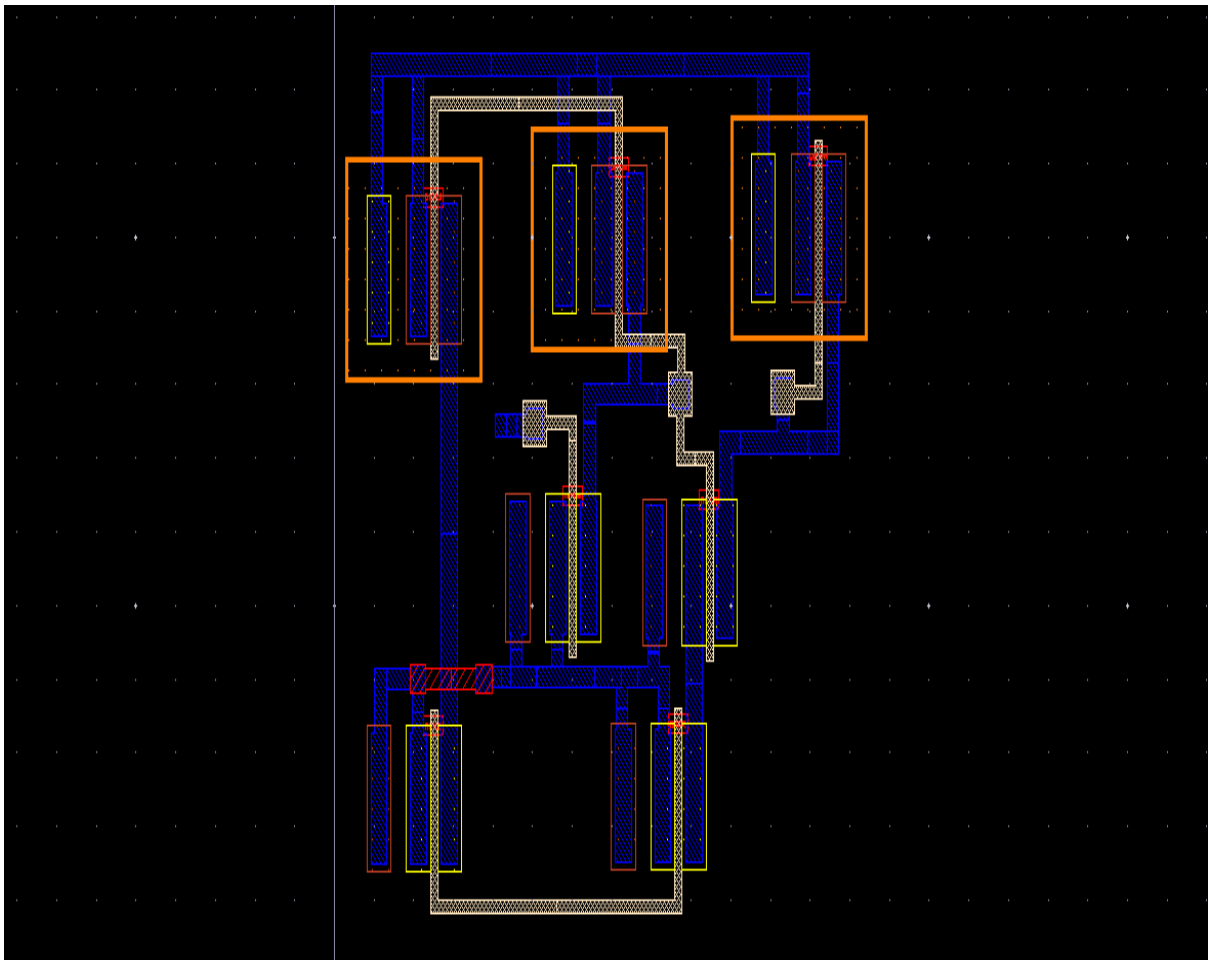

Fig6.8 –Modified layout design of CM

In the above shown circuit this is the most efficient design one can make as it has very less poly material used as compare to previous design and the metal used is also very less. So to know that our physical circuit or the layout is efficient or not we go for post layout simulation where we have to consider three different block of same architecture and then comparing simply the schematic, and other two file of the layout as shown in fig-6.9.

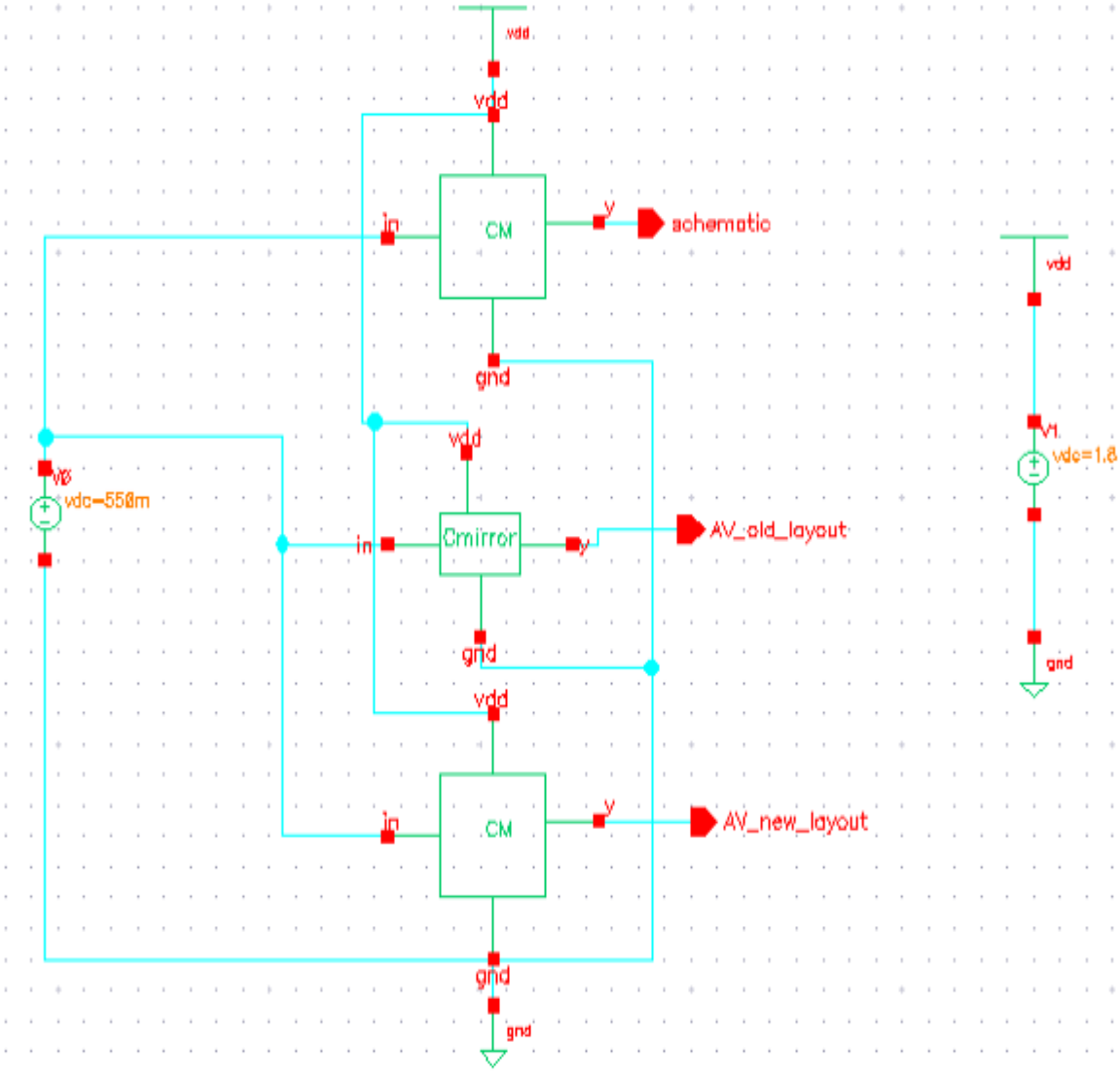

Fig 6.9- Post layout simulation

Post layout simulation is very important for any design as it gives us the clear picture of what is going to happen when including all the parasitic value, to do post layout of your design we need to compare the result of our file with the extracted view of your layout design and the result i got when i have compared these three different output varies a lot. The output AV_old_layout when compared with the schematic is 65.56% same which is a very large deviation of our result but when we compared our AV_new_layout with our schematic file we get to know that our design is 99.99% accurate which tells us that the layout design of any circuit can deviates or change the output when including the parasitic capacitance and resistance. So designing of the layout should be very precious with less usage of any poly material as that might change our output.

CHAPTER 7

RESULT AND DISCUSSION

The implemented circuit has been analysed in cadence virtuoso 180nm technology with a analysis. In all the circuit a range of value is tested to know the correct biasing voltage that is going to mirror to mirror the circuit.

7.1 Simple current mirror.- Parametric analysis is done from the range .3V to 1.8 V with 10 steps as you can see from the points that the different values of current is been matched but as we know that in simple current mirror the current is not matched perfectly because of CLM effect.

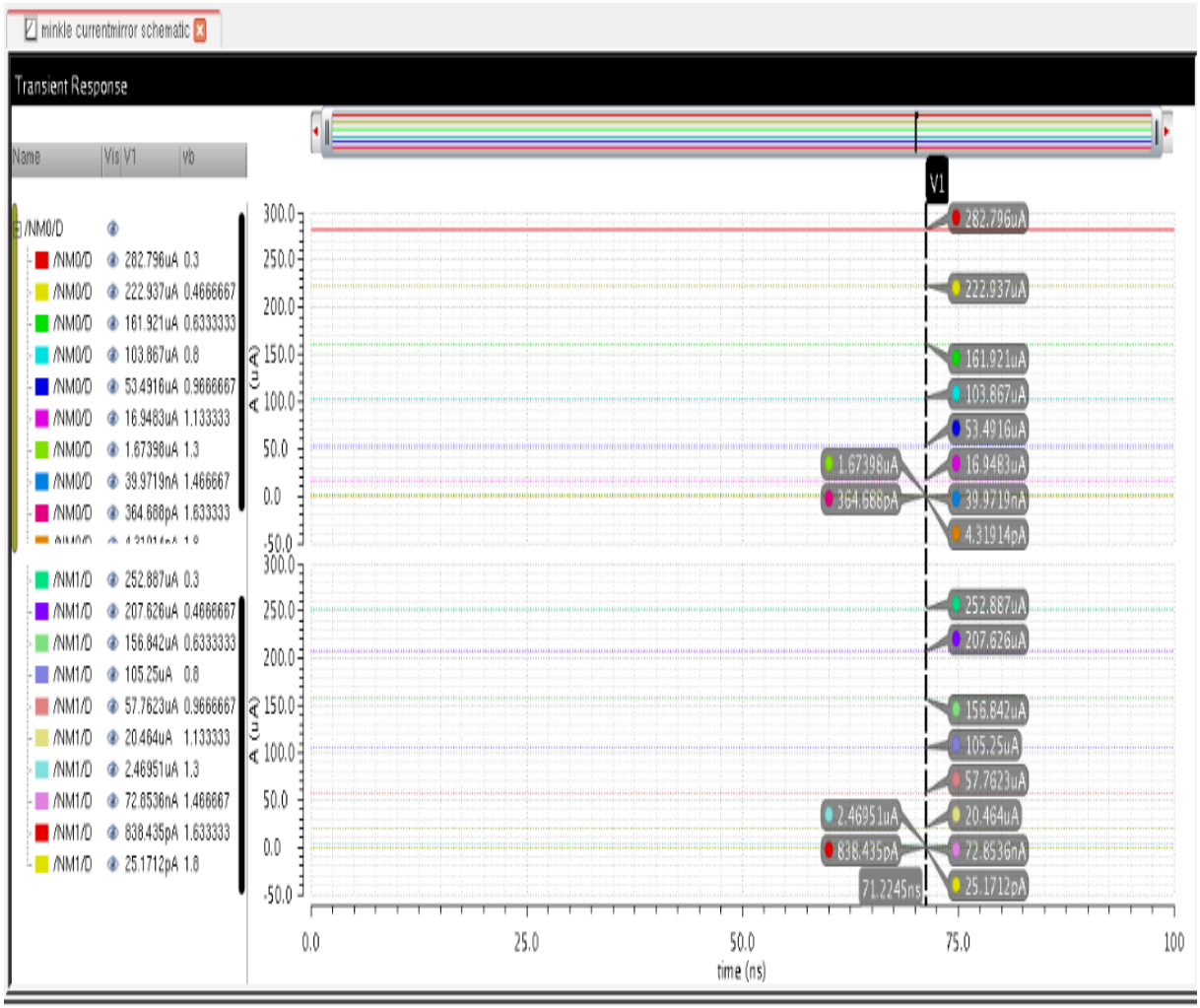

Fig7.1 Simple current mirror.

7.2 Simple cascode current mirror – Parametric analysis is done from same .3V to 1.8V with considering 10 steps. Value of current shown here is more précised with respect to the value of simple current mirror analysis. As in cascode current mirror there is involvement of current mirror circuit to it. It shows that exact mirroring effect when the biasing voltage is equal to .8 voltage for the implemented circuit.

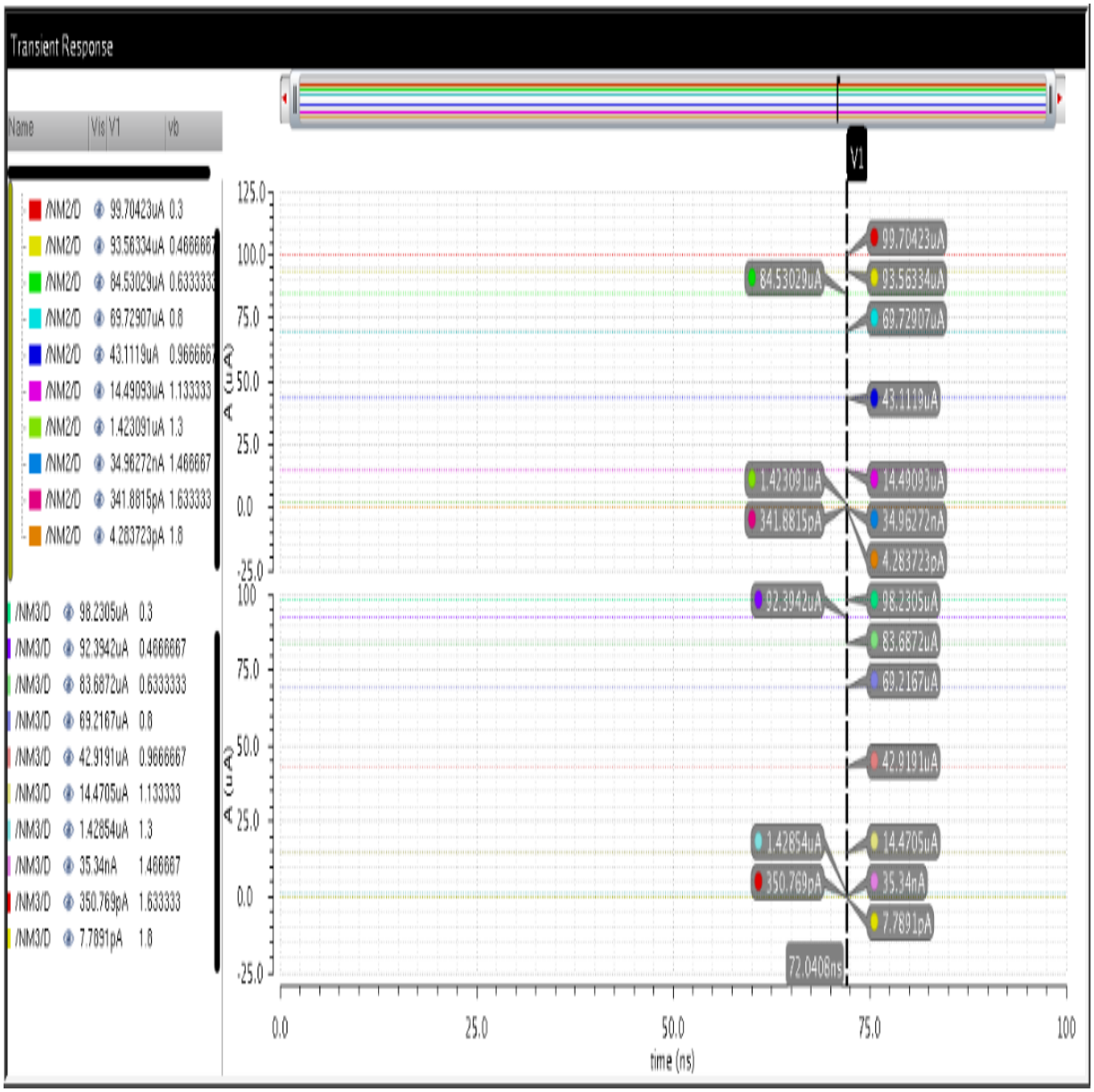

Fig 7.2 Cascode current mirror.

7.3 Wilson current mirror circuit. - Parametric analysis done from the range .3V to 1.8V. and by parametric analysis through these analysis we get to know that for same range of biasing voltage from .3 to 1.8 V Wilson current mirror shows the exact output for various ranges of biasing voltage, it has more précised current value data from cascode and simple current mirror circuit.

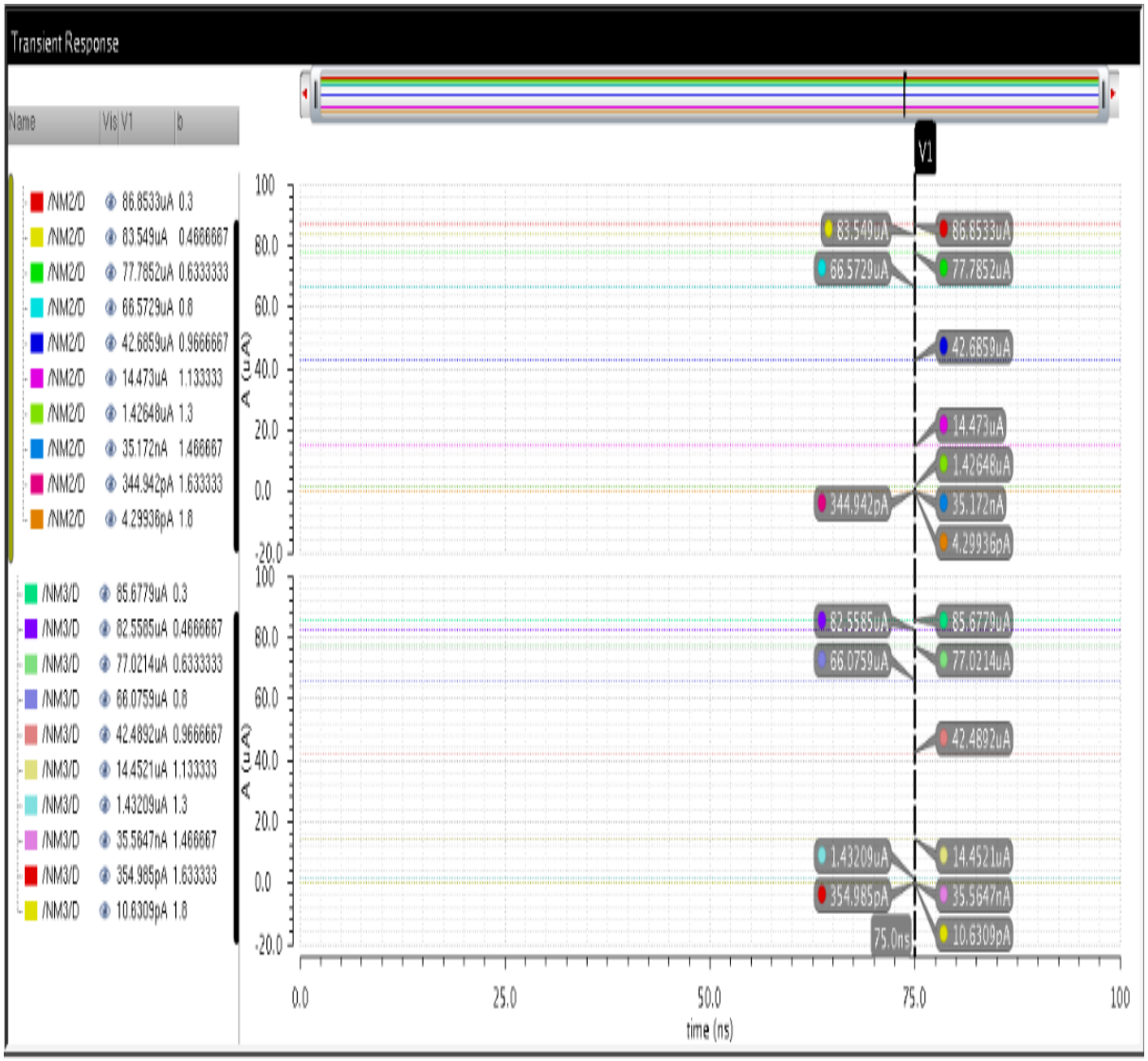

Fig7.3 Wilson current mirror

7.4 Proposed Folded cascode current mirror. - Parametric analysis between 100m to 600m voltage range is showing the exact output for the proposed circuit. The range of values for biasing is shown and the exact biasing voltage found out is 550m V.

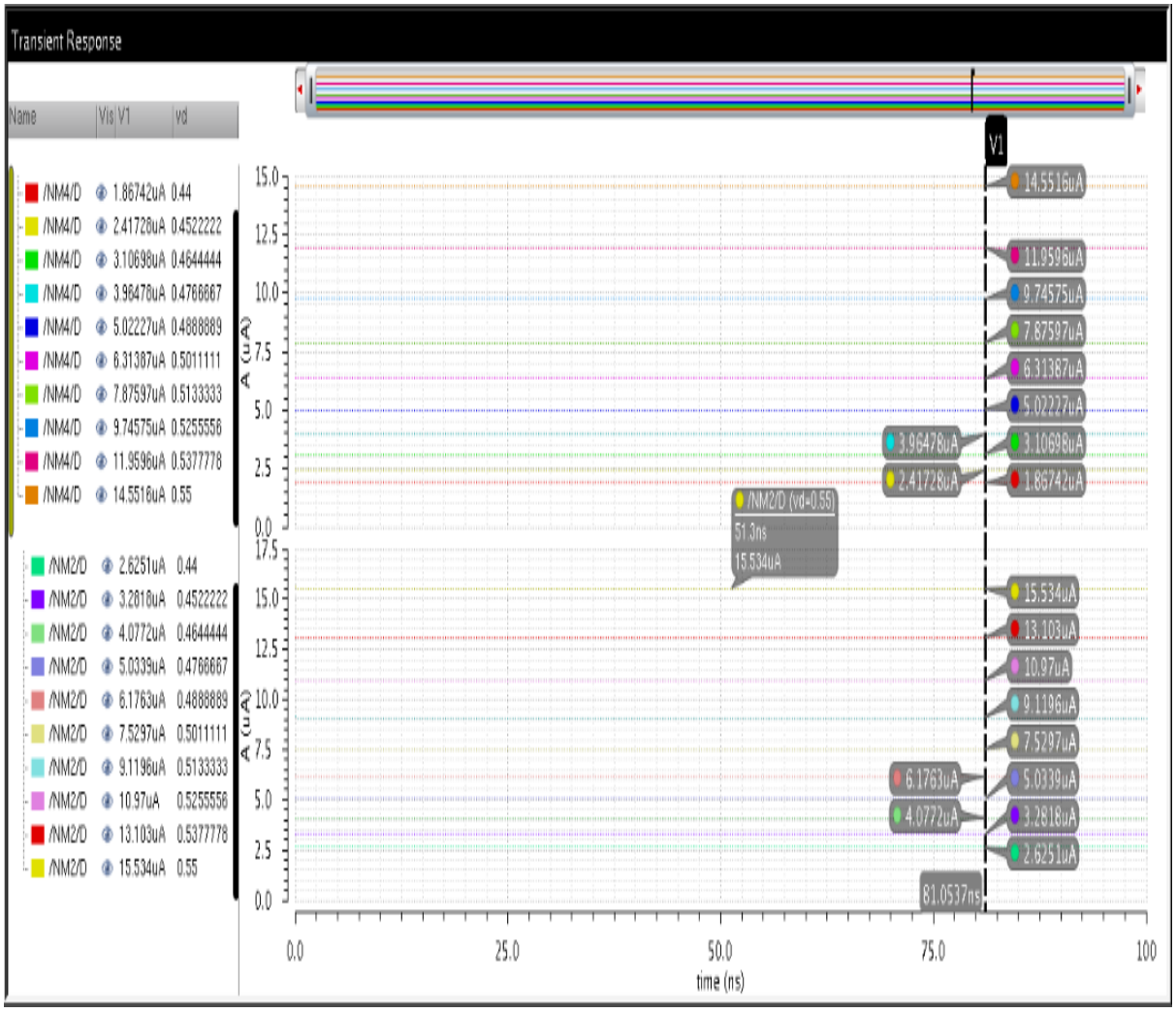

Fig 7.4 Proposed folded current mirror.

So as shown in the fig above the ranges of values for which this cascode current mirror is working approximately ranges from 400m V to 550mV. The power dissipated of the CMOS Folded cascade current mirror comes out to be 83.66 uW which in comparison to Wilson current mirror is less as it values came out to be 240.6 uW. The power dissipated decreases on decreasing the technology from 180nm to 45nm and it comes out to be 7.17 uW.

7.5 Output Resistance of the current mirror

Calculating the output resistance from the circuit differ as the technology varies as the resistance v/s current graph is shown below we get to know that the output resistance of the designed circuit is equal to $1.63*10^{4}\Omega$ and its highest value is when the value of current is .5029u A.

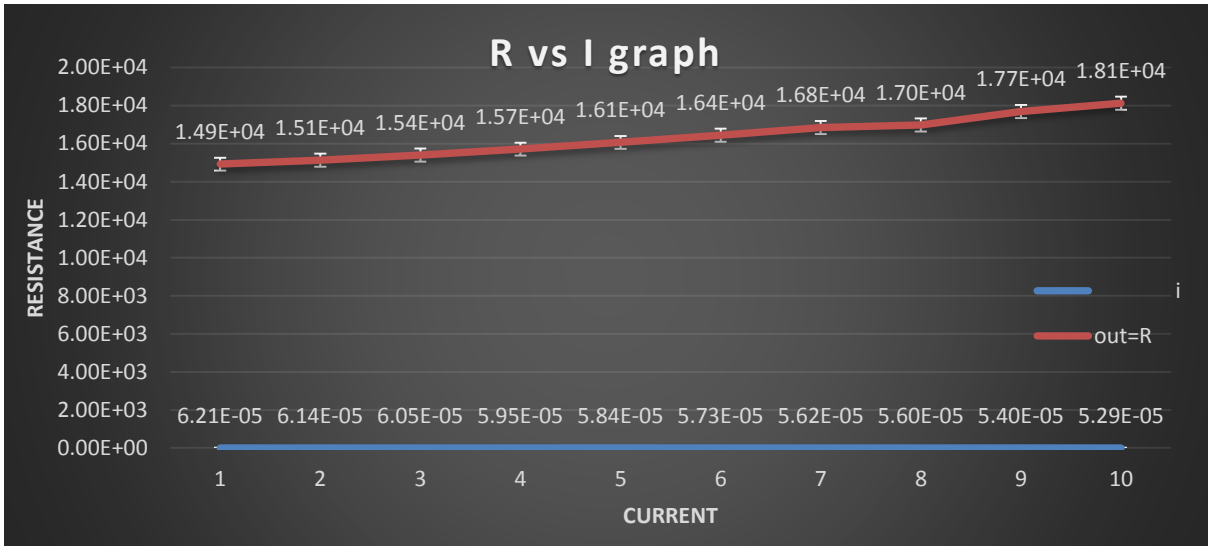

Fig-7.5 Resistance v\s current graph of 180nm.

For 45nm technology the mirroring of the circuit is done around 470mV biasing voltage with a supply voltage of 1.8V. Average output resistance of the 45nm technology for a current mirror circuit came out to be 1.33 M Ω.

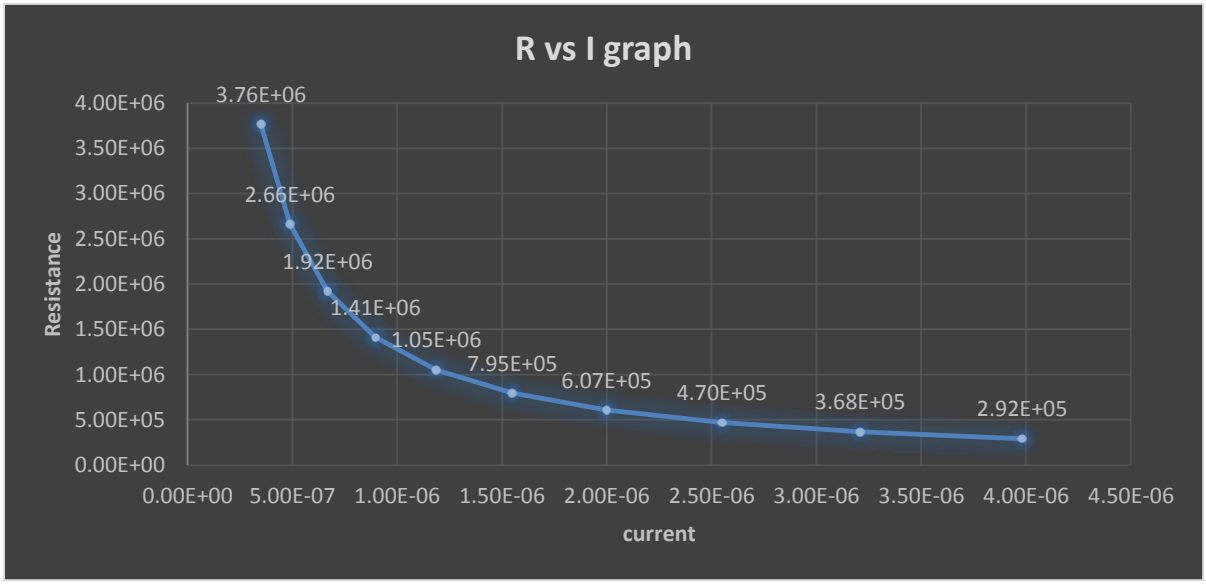

Fig-7.6 Resistance v\s current graph of 45nm.

7.6- Post layout simulation

Post layout simulation results shows that there is quite a lot of deviation due to the parasitic value added due to metal and poly material so after designing the efficient layout of the circuit with less poly silicon material and less metals we can achieve exact ranges of value which we find in schematic and those values are exactly matched as shown in below fig-7.7

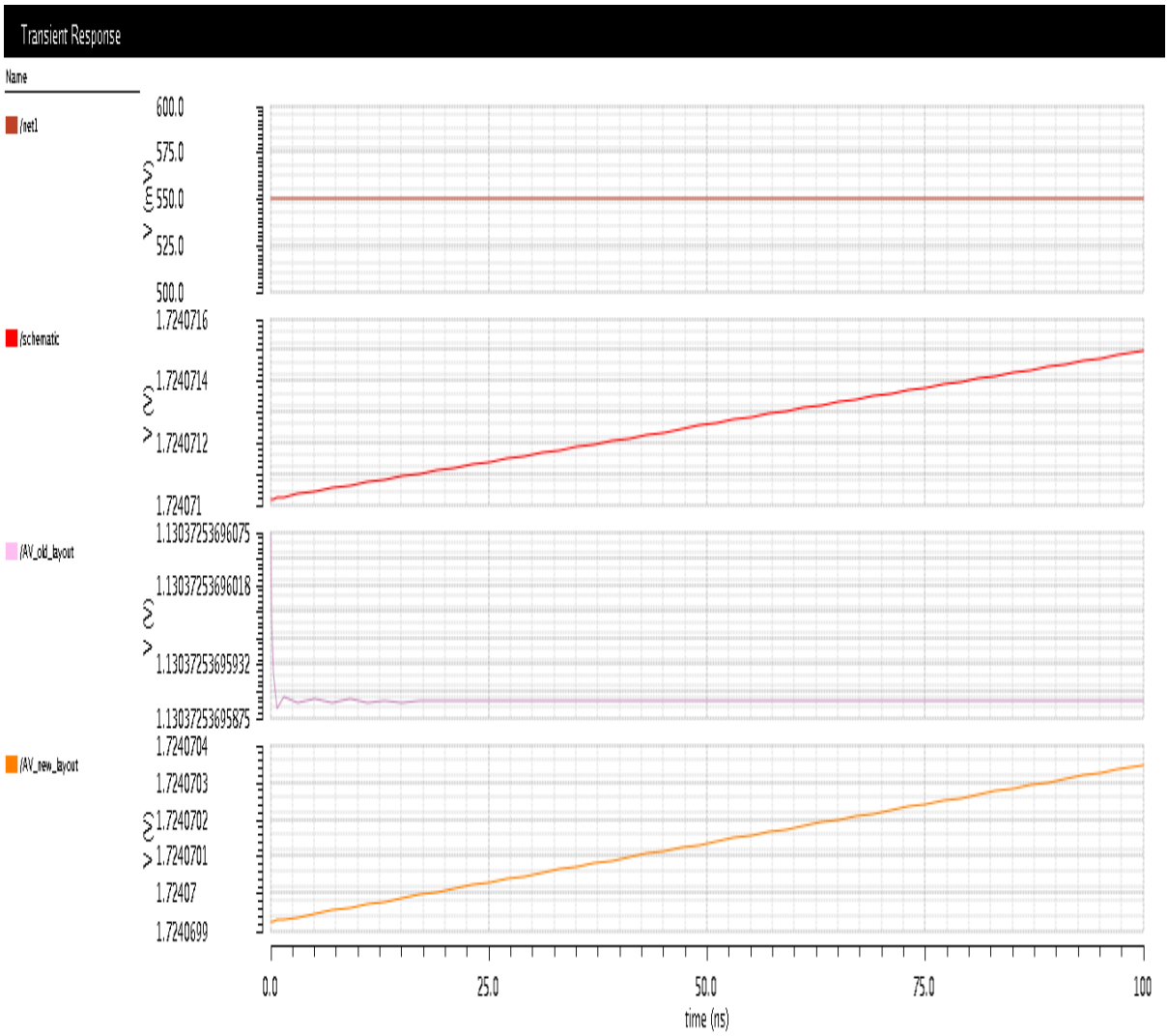

Fig-7.7 Post layout simulation of current mirror.

From the above circuit we get to know that there is only 65.56% similarity of the design00 between schematic and the old layout design and when we have designed the efficient new design layout with less metal and poly material we have achieved 99.99% similarity output which is quite a good design of the circuit as shown in fig7.7.

7.7 Corner Analysis

Corner analysis of the circuit is done to know the behavior of the circuit with extreme changes of parameter that is due to manufacturing variations. When the chip is manufactured theoretically we can predict yield as the process variation is constant but when we move in practical point these process variation varies around their ideal point which in result effect the total yield of the manufacturing. When working in schematic we basically deals with FEOL (Front end of line) which affect the performance of the circuit and second one is BEOL (back end of line) which will affect parasitic. So corner analysis will tell us the performance generated due to variation expected due to process, voltage and temperature , and these result will tell us that the extreme change in the condition will my design will work or not. There are four corner FF, FS, SF and SS which will define my circuit behavior. On doing the corner analysis on my circuit of folded cascade current mirror i get to know that their is lot of variation of the output with skewed corners that is FS. Corner analysis for FF , SS and SF is somewhat similar with less change in the output current values as shown below, Nominal is the one where there is no variation included .

Table-1 Corner Analysis without temperature.

Serial Number	Type of Corner	Input current (A)	Output current (A)
1	Nominal (NN)	14.5516u	15.5339u
2	Fast-Fast (FF)	58.1041u	58.0899u
3	Fast-Slow (FS)	55.2225u	48.4381u
4	Slow-Fast (SF)	2.20703u	2.90588u
5	Slow-Slow (SS)	2.09532u	2.39805u

On doing the temperature variation of the circuit from -25°C to 80°C there is lot of variation in every corners except in FF as shown in table.

Table-2 Corner analysis with temperature

Serial Number	Type of corner Analysis	Input current (A)		Output current (A)	
		Temperature		Temperature	
		-25°C	80°C	-25°C	80°C
1	Fast-Fast(FF)	47.707u	65.747u	47.843u	65.737u
2	Fast-Slow(FS)	45.143u	62.629u	40.02u	54.49u
3	Slow-Fast(SF)	9333.27n	4.0413u	1.2811u	5.1868u
4	Slow-Slow(SS)	879.94n	3.8593u	1.0335u	4.3496u

CHAPTER 8

CONCLUSION AND FUTURE SCOPE

In this thesis work ,I learned that a current mirror can be used in various analog circuit where low voltage application is needed as the devices now a days are much more portable so should work on low voltage to consume the battery consumption. A brief idea of how a current mirror is going to behave in different short of input biasing voltage is been discussed. All current mirrors have different short of range for which the current in the circuit is mirrored to another branch, from the study we get to know that the cascode current mirror is having good range of values mirrored with respect to other type of current mirror with having high output impedance it's resistance value is $g_m * r_0$ times the value shown by simple current mirror. The proposed circuit uses folded cascode current mirror and been used in a range from 100m to 600m voltage , with exact mirroring the current when Vbias provided to current source is equal to 550m V. The output resistance of the folded cascade current mirror came out to be 16.3M Ω. It's corner analysis is done with and without temperature variations and for fast-fast(FF) variation the circuit is showing less variation when adding the extreme temperature variation of -25°C and 80°C as shown in table 2. It's output voltage equation is derived that shows the involvement of reference current into the output voltage. Further this design can be used to implement any bigger circuit like in amplifier and can be act as a current source.

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