Folded Cascode Current Mirror & It's Layout Design

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Abstract
Current mirror is used in various application where low voltage analog circuit design is needed like in any of the portable devices so that battery lifetime can be increased. In this paper a high performance MOSFET current mirror in a folded cascode configuration is designed to achieve a high output resistance, operating in wide range of supply voltage. We have designed the layout of the proposed circuit and the output resistance values of the proposed circuit are much higher than the previously designed circuits.

Keyword: Current Mirror, Folded Cascode, Layout, Cadence Assura

I. INTRODUCTION

After analysing all the current mirror circuit and the modified one's that are showing good mirroring effect and high output resistance value, we came to conclusion to implement the modified cascade current mirror that can have high input resistance and a wide swing. So the circuit diagram of the proposed circuitry in this paper is shown below which is showing good mirroring across the wide range of current with the high output impedance value.

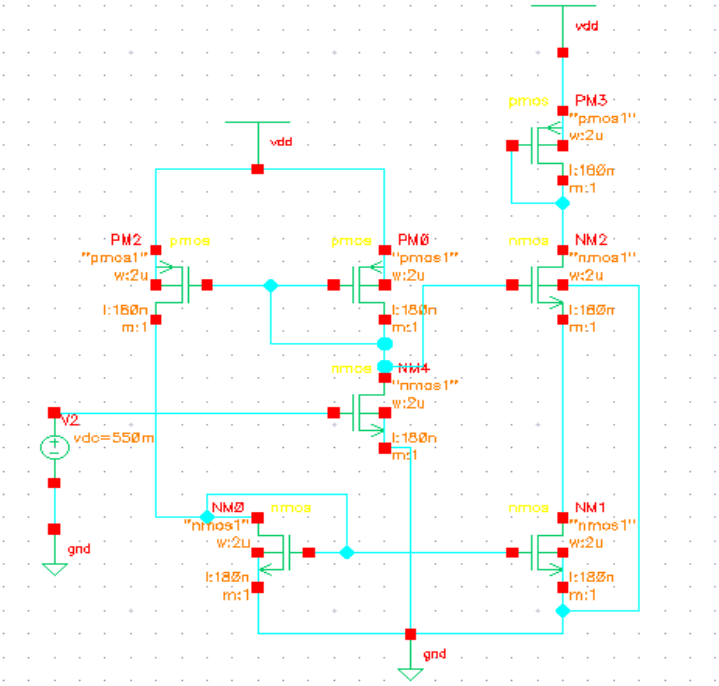

Fig. 1: Proposed Folded cascode current mirror circuit.

The proposed circuit is a simple 7 transistor modified cascode current mirror, the base paper for this circuit is implemented in the BJT which is showing very efficient result according to output resistance as 71M ohm with the impedance bandwidth product of 2.8 ohm at 1mA output current with 1.8V input supply voltage. This MOSFET circuit implemented has the range from 100m – 800m Voltage with the exact mirroring value at 550M V.

II. LAYOUT DESIGN OF THE CURRENT MIRROR CIRCUIT

Layout of the current mirror is been drawn to analyse the change in the output current by including all the parasitic value like capacitor and resistance due to metals and polysilicon material, we can calculate the total amount of capacitance and resistance value by applying the basic networking rules. Designing the circuit and doing its layout design is a completely different work as there are two rules that should be matched by the design one is lamda rule and other one is micron rule. In lamda rule everything is expressed in term of lamda like 2λ or 3λ and lamda varies according to the technology. After designing the layout, we have to check down the DRC, LVS and RCX which extract the parasitic values from it. DRC is the design rule check which deals with checking the design rule as per standards defined then

comes the LVS which is layout v\s schematic which will compare that the connection of both the design is matched or not and then comes the RCX which will extract all the parasitic values of the metal and poly material used in the design. Designing of the layout is the art where we have to arrange the components in such a way that it should uses minimum area with all the other design rule followed with it. If we have to consider the design approximately the area is equivalent to the product of the number of MOSFET used and the total width of the CMOS. Designing of the circuit and connecting the components using metal need very precious connection , same material wire cannot cross each other or overlap each other at that time we require a second metal and a via to connect it, same way we need poly to metal or metal to poly via to connect two different material . After running out DRC and LVS we extract the parasitic values from the design and we get the new file named AV-extracted file which shows all the values given to all the metal and poly material used, by analysing it we get to know that the polysilicon material used has more resistance value as compare to metal which will affect the overall current flowing in the design so to have an efficient layout we have to minimize the use of poly material and minimize the metal length of the connection. Designing the layout in analog world is quite a complex task as every connection is drawn manually and we have to consider which component is to placed where, and parallel we have to consider all the design rules and to minimize the area under which my circuit is drawn which will directly affect the cost of the chip.

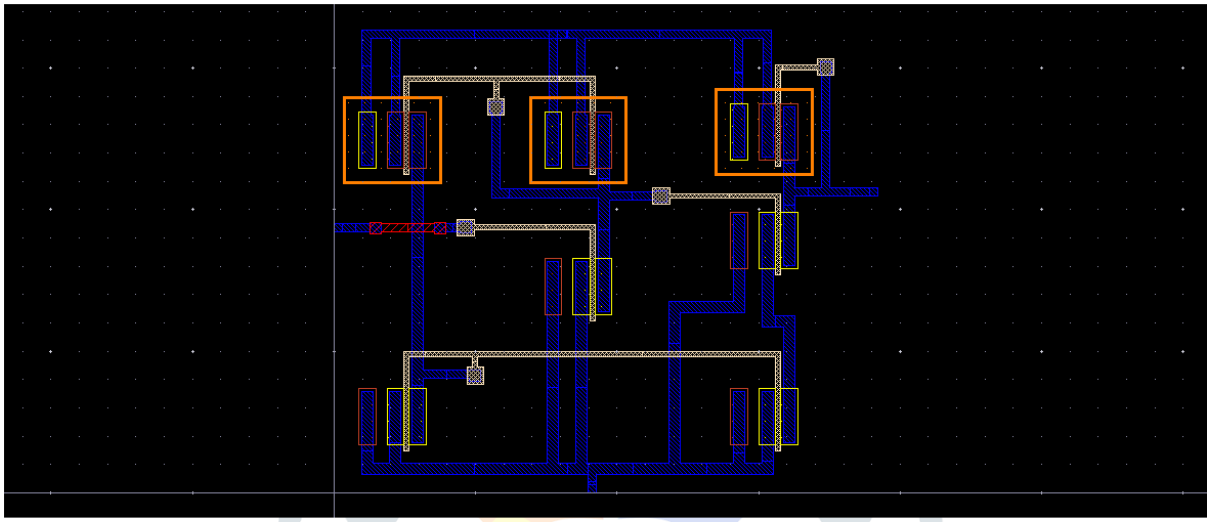

Fig. 2: Layout of CM

In the figure 2, the layout design of the folded cascade current mirror where we have used 2 metal and a poly to connect all the terminal of the cmos. Blue color material is my metal one, and the red color material is the metal two which we have used so that same type of material should not overlap as that will short the connection. On designing the layout of CM we can see their as soo much gap between the component and there is large number of poly material used which will directly increase the resistance value of the overall circuit so we can reduce the poly material by manually arranging the component so the distance between the design should be minimum where poly material is used. So we have again design the circuit by considering and compressing the area of previously designed layout , new design is shown in next page where all the connection is made such a way that there should be very less poly material used and second is the metal length should be less, and the solution of minimizing the metal used can be done by starching the pin of VDD and GND which will directly reduce metal used , If we have to find out the area we can manually calculate it by placing the pointer on X-axis and Y- axis and then multiplying the total area under the circuit which will include spacing between the component but if we have to calculate the area used by the component without spacing and all , then directly multiply the width of the component with the number of component used in designing of the circuit. In designing the folded cascade current mirror, we have used total 7 component with the width of 2micro meter each which will give us the area as 14 micro meter of only the component without connections.

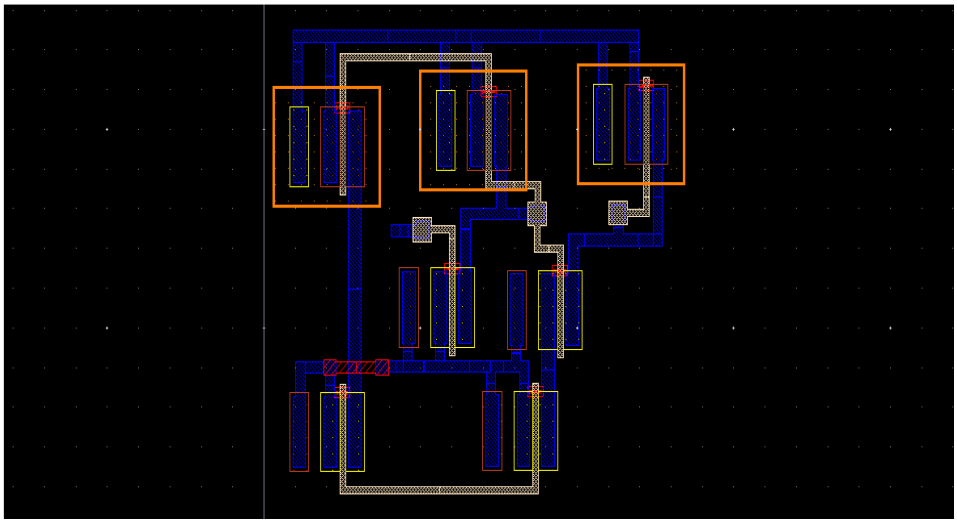

Fig. 3: Modified layout design of CM

The figure 3, shows the most efficient design one can make as it has very less poly material used as compare to previous design and the metal used is also very less. So, to know that our physical circuit or the layout is efficient or not we go for post layout simulation where we have to consider three different block of same architecture and then comparing simply the schematic, and other two file of the layout as shown in fig-6.9.

The Parametric analysis between 100m to 600m voltage range is showing the exact output for the proposed circuit. The range of values for biasing is shown and the exact biasing voltage found out is 550m V.

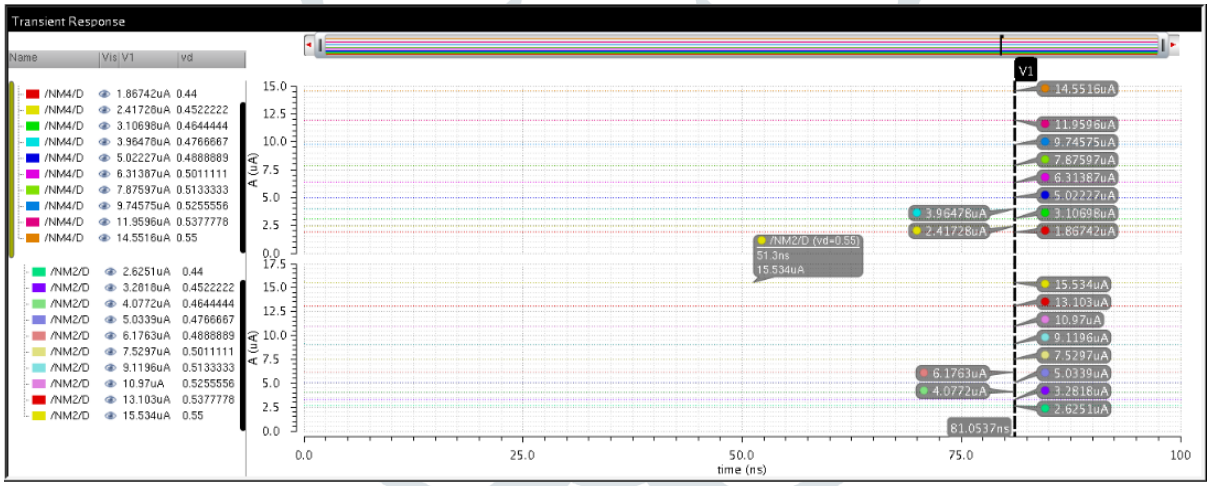

Fig. 4 Proposed folded current mirror parametric analysis

The figure 4 shows ranges of values for which this cascode current mirror is working approximately ranges from 400m V to 550mV. The power dissipated of the CMOS Folded cascade current mirror comes out to be 83.66 uW which in comparison to Wilson current mirror is less as it values came out to be 240.6 uW. The power dissipated decreases on decreasing the technology from 180nm to 45nm and it comes out to be 7.17 uW.

III. OUTPUT RESISTANCE OF THE CURRENT MIRROR

Calculating the output resistance from the circuit differ as the technology varies as the resistance v/s current graph is shown below we get to know that the output resistance of the designed circuit is equal to 1.63*104Ω and its highest value is when the value of current is .5029u A.

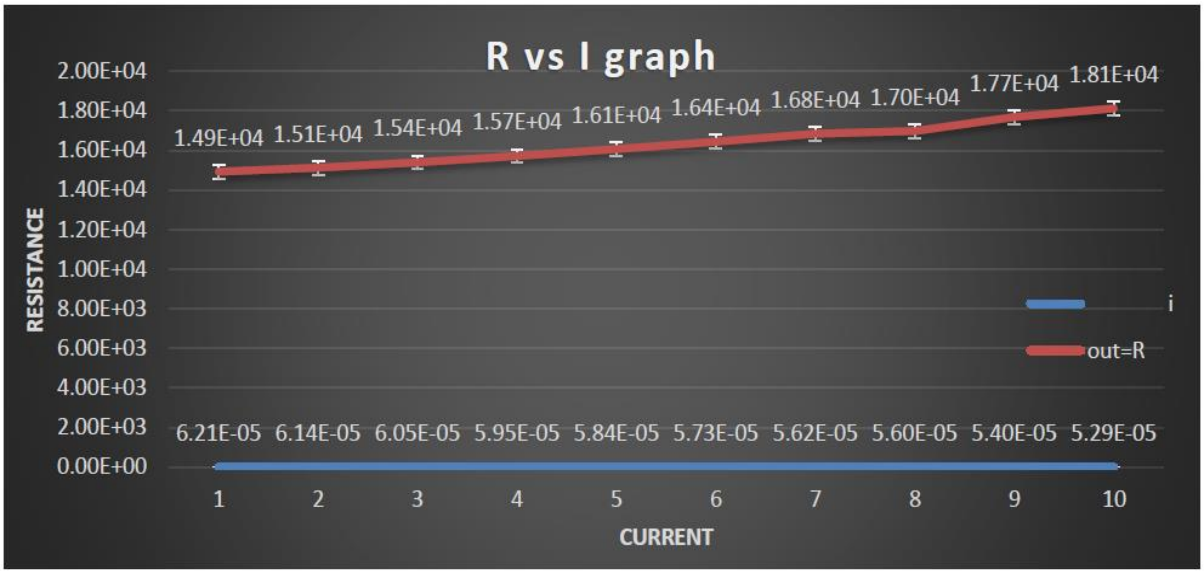

Fig. 5: Resistance Vs current graph of 180nm.

For 45nm technology the mirroring of the circuit is done around 470mV biasing voltage with a supply voltage of 1.8V. Average output resistance of the 45nm technology for a current mirror circuit came out to be 1.33 MΩ.

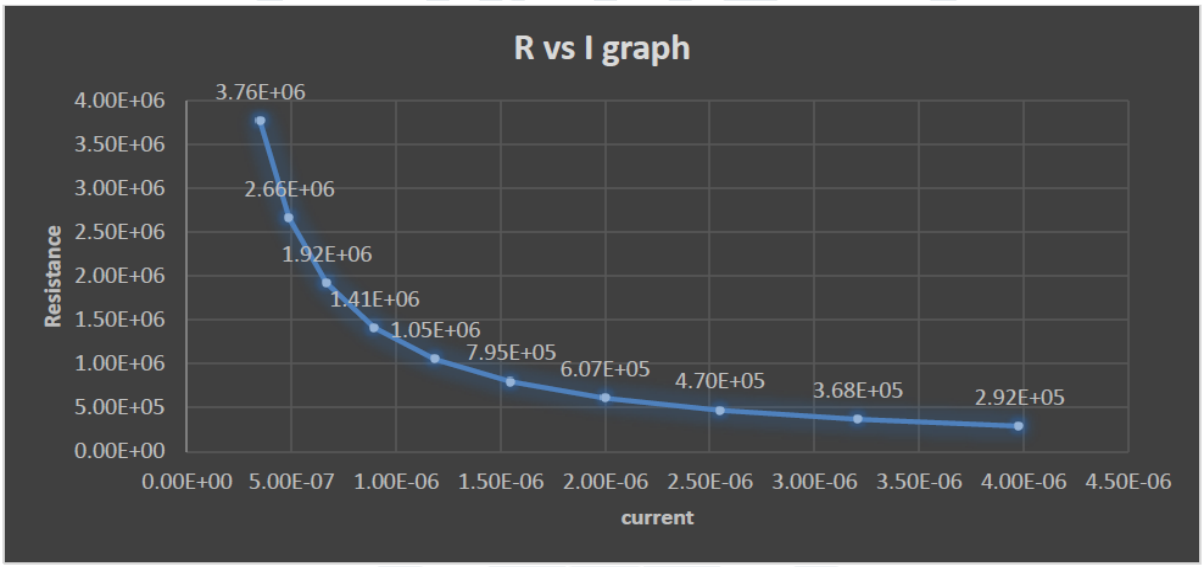

Fig. 6: Resistance Vs current graph of 45nm.

IV. CONCLUSION

In this paper a high performance MOSFET current mirror in a folded cascode configuration is designed to achieve a high output resistance, operating in wide range of supply voltage. we have designed the layout of the circuit and its post layout simulation is also analysed by optimizing the layout design of the circuit. The output resistance values are much higher than the previously designed circuits.

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