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DESIGN & IMPLEMENTATION OF A NOVEL LOW POWER HYBRID FULL ADDER CIRCUIT

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Abstract: In this paper 1-bit hybrid full Adder is implemented using complementary metal-oxide-semiconductor (CMOS) logic and pass transistor logic. The circuit is implemented using Cadence Virtuoso tool in 180nm technology. Performance parameters like power and layout area were compared with existing designs such as complementary pass transistor logic, transmission gate adder, transmission function adder and so on. For 1.8V supply static power consumption 477.3 pW and average power consumption is 3.617 µw which is comparatively lower than the existing designs. Even layout is implemented and its DRC, LVS and RC extraction is done. In comparison to the existing designs this design is better in terms of power and layout.

Key Words: low power, hybrid design, Cadence Virtuoso, Layout design

1. INTRODUCTION

Usage of battery operated portable devices is increasing day by day in daily life like take case of cellular phones, personal digital assistants (PDAs) and many other applications where power consumption is basic concern nowadays. As full adder is one of the basic building block of every circuit so it is main area of focus for many researchers over the years [2],[3].Different logic styles like transmission gate logic, Pass transistor logic, conventional CMOS logic,GDI logic have their own advantages as well as disadvantages to implement 1-bit full adder [4]-[10].Designs can be classified into two categories: 1. Static style and 2.Dynamic style. Static style full adders are generally more reliable with less power requirement as compared to the dynamic style full adders.

Standard static complementary metal-oxide-semiconductor (CMOS),dynamic CMOS logic, complementary pass transistor logic (CPL) [4],[5] and transmission gate full adder (TGA)[6],[7] are most important logic design styles in conventional domain. Many adders use more than one logic style that is hybrid-logic design style [8]. Hybrid logic style use features of different designs for improving the performance.

Advantage of standard Complementary style based adders (28 transistors) is its robustness against voltage scaling and transistor sizing while on the other hand its disadvantage is requirement of many buffers and high input capacitance. Another complementary type design is mirror adder with maximum carry propagation delay inside the adder is relatively small as compared to the standard CMOS full adder. On the other hand CMOS shows good voltage swing restoration employing 32 transistors [4],[5] but CPL is not a good choice for low power applications because

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of its high switching activity, high transistor count and static inverters. The main disadvantage of CPL is its voltage degradation which was addressed in TGA with 20 transistors [6],[7].14 transistor Vesterbacka [9] uses hybrid logic style. Similarly hybrid pass-logic with static CMOS (HPSC) output full adder was proposed by Zang [10]. In such HPSC circuits XOR and XNOR functions were generated by pass transistor logic using 6 transistors and using CMOS module to produce outputs of full swing but at the cost of increased transistor count and reduction in speed.

Main objective of this paper is to reduce the power consumption of the full adder as compared to already existing full adders. The circuit is implemented in 180nm technology in cadence virtuoso. For 1.8 V power supply and overall time period of 100ns static power is 477.3 pW and average power consumption was coming out to be 3.6 µW. After this layout of the proposed design was implemented and it's DRC, RCX, LVS and RC extraction was done.

This paper is divided into further 5 sections. In the 2nd section includes design approach of proposed full adder in which internal structure has been explained means its modules and how these modules are implemented and change done in proposed structure. In the 3rd section operation of proposed full adder means how it working and initial conditions have been discussed like overall time period and period for which each input signal is running etc.It also includes comparative study of proposed full adder with different full adders which were proposed previously. It also includes width and length ratios of different transistors used in structure. In the 4th section details of layout has been discussed and how it is better than other layouts. Finally in the end conclusion is given.

2. DESIGN APPROACH OF PROPOSED FULL ADDER

Basically full adder consists of 3 modules as shown in figure 1.Module 1 basically for implementation of XNOR circuit. Module 2 is for generation of SUM output using XNOR circuit whereas Module 3 is for carry generation.

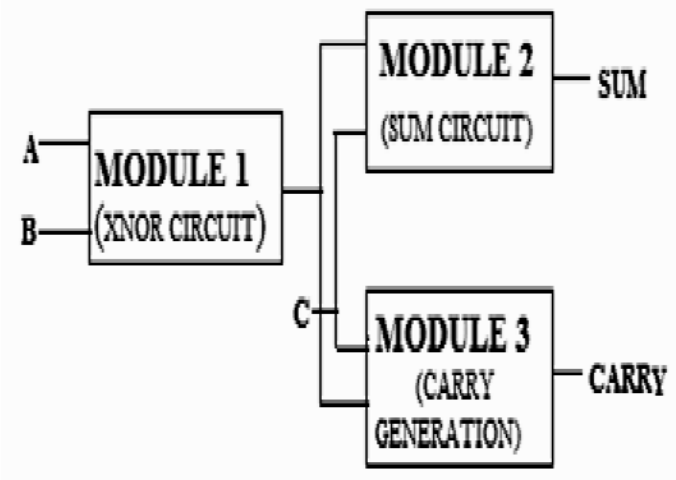

Figure. 1 Schematic structure of proposed full adder

2.1 Design of XNOR circuit

XNOR module is main module of full adder so if power consumption of this module is reduced. So, if power consumption of this module can be reduced then overall power consumption can be reduced. In this circuit basically XNOR circuit has been use implement the whole circuit.[1]

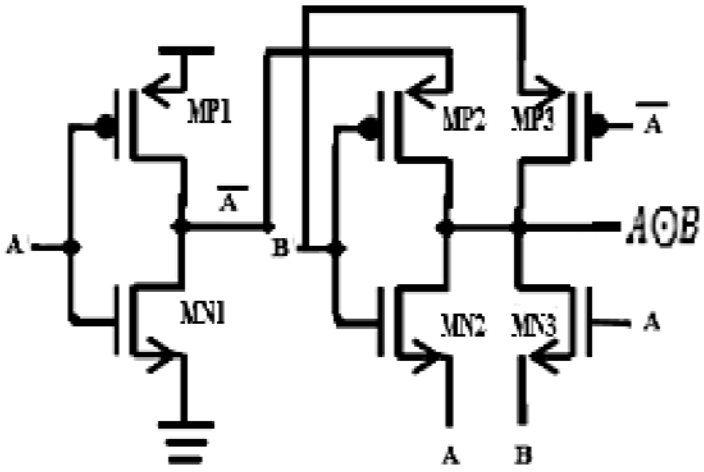

Figure. 2 XNOR module

XNOR circuit is reduced by the use of weak inverters formed by transistors Mp1 and Mn1 as shown in *figure* 2.Even full output swing of is guaranteed by Mp3 and Mn3 as shown in figure 2.Many topologies of XOR/XNOR circuit have been studied in [6] and [11]-[13]. In this circuit basically XNOR module is implemented using modified form of PTL logic i.e DPL logic so that switching will be reduced and even power consumption will be less as compared to existing XNOR modules. Even after implementing XNOR module XOR can be implemented using inverter. This circuit is implemented in such a way so that output swing will be more.

2.2 Modified carry block

In this circuit basically modification in carry block is done to reduce the power consumption. In this circuit carry block is implemented by doing a change in the carry block. Carry block is implemented by PTL logic in a different way so as reduce the power consumption.

Table 1
Carry implementation using XOR & XNOR

A	*B*	*C*	$(A \oplus B)C$	$(A \odot B)A$	*CARRY*
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	1	0	1	1

So, from *table* 1 it is very well clear that carry implementation can be done by addition of (A xor B) C and (A xnor B) A so it can be even implemented using PTL logic. So, in this way carry part can be modified.

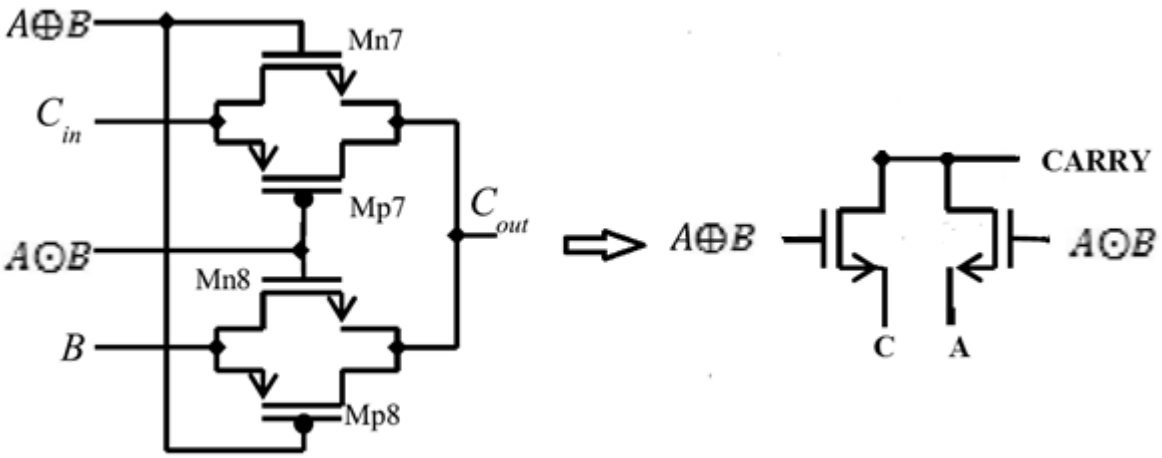

Figure. 3 Modified carry generation module

This carry module is implemented by using a totally different logic as XNOR and XOR have already been implemented. As by multiplying (A xor B) with C and by multiplying (A xnor B) with input A carry part can be implemented using above given truth table. This circuit is implemented using PTL logic. So, in this way new carry generation module is able to reduce the power consumption as compared to existing designs. As power consumption of carry generation module is reduced in this way overall power consumption of whole circuit is reduced. Overall circuit with reduced power dissipation is given in *figure* no.4.

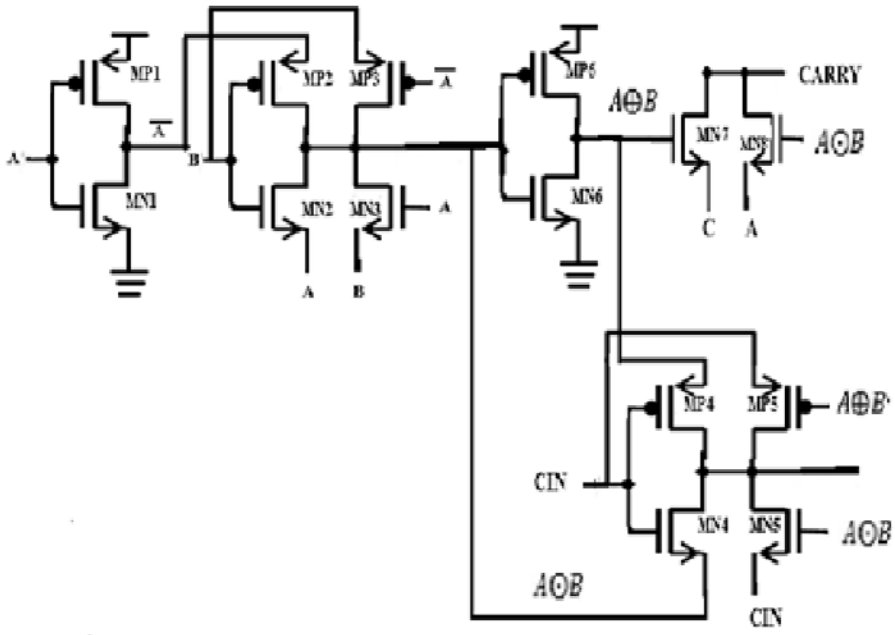

Figure 4. Detailed structure of proposed full adder cell

3. OPERATION OF PROPOSED FULL ADDER

Figure 4 represents the detailed structure of proposed full adder cell. Sum part of full adder is implemented using XNOR modules. The inverter comprises of transistors Mp1 and Mn1 will generate A' which can be used to design the controlled inverter using Mp2 and Mn2.output of this inverter is XNOR of A and B. But because of the problem of voltage degradation Mp3 and Mn3 are introduced. Sum function implemented by second stage containing pmos transistors (Mp4, Mp5

and Mp6) and nmos transistors (Mn4, Mn5 and Mn6). Similarly carry is implemented by using nmos transistors (Mn6 and Mn7).Circuit given in fig.4 is implemented using 180nm technology in Cadence virtuoso. This circuit was implemented at 100ns overall time period using initial conditions as given in *table* below.

Table 2.
Initial conditions for proposed full adder

Input signal B	*Input signal A*	*Input signal C*
Voltage 1 = 0 V	Voltage 1 = 1.8 V	Voltage 1 = 1.8 V
Voltage 2=1.8 V	Voltage 2 = 0 V	Voltage 2 = 0 V
Period=50 ns	Period=30 ns	Period=25 ns
Pulse width=25 ns	Pulse width=15 ns	Pulse width=12.5 ns

For given conditions static power of proposed circuit was coming out to be 477.3 pW and average power consumption was coming out to 3.6µW which is comparatively less as compared to existing designs. Given circuit is working properly from voltage 1.25V-1.8V

Table 3.
Transistor sizes of proposed full adder cell in 180 nm technology

Transistor name	*Width(W)(nm)*	*Length(L)(nm)*
Mn1, Mn6	400	180
Mp1, Mp6	800	180
Mn2, Mn3	400	180
Mp2, Mp3	800	180
Mn4, Mn5	400	180
Mp4, Mp5	400	180
Mn7, Mn8	400	180

Table 4.
Simulation results of full adders in 180nm technology with supply voltage of 1.8V

Design	*Average power consumption (µW)*	*Transistor count*	*References*
Bhattacharya	4.1563	16	[1]
CPL	7.17985	32	[4],[5]
TFA	8.2491	16	[18]
TGA	8.4719	20	[6],[7]
14 T	12.7217	14	[9]
10 T	14.3449	10	[21]
HPSC	6.3798	22	[10]
Majority based	6.3227	—	[20]
24T	15.91	24	[2]
FA_HYBRID	5.978	24	[3]
FA_DPL	19.56	22	[17]
FA_SR-CPL	20.78	20	[17]
Proposed	3.617	14	Present

4 LAYOUT OF PROPOSED FULL ADDER DESIGN CELL

Layout of proposed full adder circuit is made inside Cadence tool is as given in *figure* 5.After making layout DRC, LVS, RCX and RC extraction was done and this circuit is giving proper DRC, LVS, RCX and AV extraction.

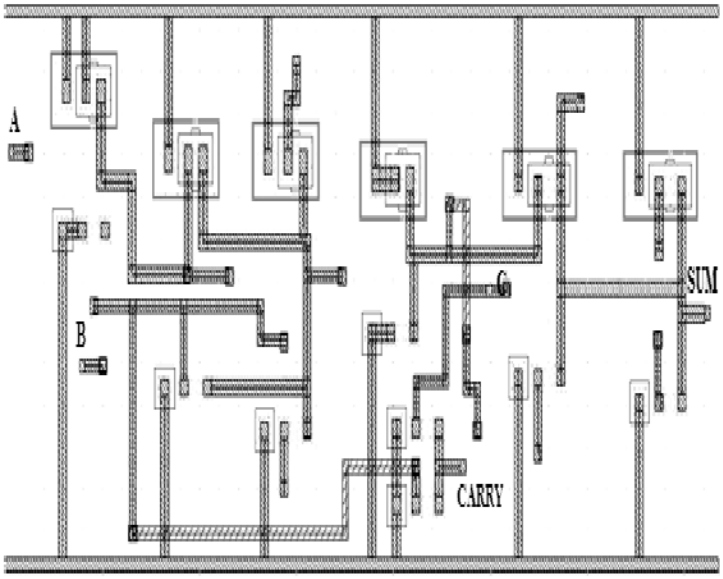

Figure. 5 Layout Design of Proposed Full Adder

Advantage of this layout over the already existing layouts is that in this layout only Metal 1 and a little bit of metal 2 is used. So, number of interconnects in this layout will be very less. Area of this layout design is 496μm^2. So, this circuit is better in terms of layout also.

5. CONCLUSION

The proposed full adder has average power consumption of 3.61μW and after finding its critical path delay is coming out to be 18.745ns. This proposed structure is better in terms of layout because of less number of metal wires used in layout. This circuit is working properly from 1.25 V to 1.8 V.

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