DISSERTATION REPORT

ON

DESIGN AND IMPLEMENTATION OF PIPELINED AND BLOCK ENABLED MULTIPLIER ACCUMULATOR (MAC) UNIT

Submitted in partial fulfillment of the requirements for the award of degree

Master of Technology

In

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Submitted by

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DECLARATION

I, Amarveer Kaur Dhindsa hereby declare that the work being presented in the dissertation report entitled "**DESIGN AND IMPLEMENTATION OF PIPELINED AND BLOCK ENABLED MULTIPLIER-ACCUMULATOR (MAC) UNIT**", by me in partial fulfillment for the requirements for the award of degree of Master of Technology in ECE at Lovely Professional University, Jalandhar is an authentic record of my own work carried out under the supervision of Mr. Raj Kumar Sarma, Assistant Professor, School of Electronics and Electrical Engineering, during January to May, 2016.

Dated:

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It is certified that the above statement is correct to the best of my knowledge and belief.

Date:

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CERTIFICATE

This is to certify that the dissertation report entitled, "DESIGN AND IMPLEMENTATION OF PIPELINED AND BLOCK ENABLED MULTIPLIER- ACCUMULATOR (MAC) UNIT" being submitted by Amarveer Kaur Dhindsa, in partial fulfillment of M.Tech in ECE is the result of her original study and research carried out by her under my supervision. To the best of my knowledge, the content of this report does not form a basis for the award of any previous degree to anyone else.

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ABSTRACT

Multiply-Accumulate (MAC) unit is the core of all high performance digital signal processors used in applications like speech processing and transmission in digital mobile phones, seismic data processing, audio signal processing etc. To achieve high performance digital signal processing systems, high speed MAC unit with low power consumption is a key to the improved overall performance.

To optimize the design constraints like speed and power for improved performance, the constituent blocks of MAC like multiplier, adder etc. has to be amended. The optimization can be done at different levels of abstraction. The work done so far in this field has been limited to digital approach which optimizes the designs at the algorithmic level.

The idea of the present research work here is to design pipelined and block enabled MAC architecture in analog design environment (Virtuoso). As the design is handcrafted each individual block can be modified at schematic level to optimize the unit as a whole. A block enabled MAC unit increases the overall power efficiency of the design. The pipelined architecture increases the speed of the MAC operation by fetching the data in advance. The synchronous buffered pipeline architecture has been used to perform the entire MAC operation in single clock cycle which makes it feasible to be used in real time applications.

The blocks of the MAC has been modified to reduce the transistor count and hence to optimize the layout area, which in turn reduce parasitic and contribute to lower power consumption and higher speed operation.

Table of Contents

Table of Figures

List of Tables

CHAPTER 1 INTRODUCTION

1.1 General

Real world continuous analog signals are numerically manipulated using digital signal processors (DSP) usually to filter, measure or compress. The computational power of DSPs applied to signal processing has many benefits over processing in analog for numerous applications such as error detection and error correction as well as compression in transmission [1].

A large number of mathematical operations are performed repeatedly and quickly on series of data samples by DSP algorithms. Most operating systems and general purpose microprocessors can successfully execute DSP algorithms but because of power efficiency constraints, they are not suitable for use in handy devices such as PDAs and mobile phones [2]. However, the rapid growth of portable electronics has introduced the major challenges of low power and high throughput for VLSI design engineers. For actual time signal handling, MAC unit having high speed and high throughput is desired to achieve high performance DSP system [3].

In calculating or processing, especially in the digital signal processing applications, the multiply accumulate involves the significant operations usually as the multiplications and/or accumulations. The MAC operation is the core computational kernel in digital signal processing architectures. It controls the speed of the whole system as it is critical path.

The main objective of our research is to explore the various pipelined and block enabled MAC architectures and designs which are resourcefully suitable for the execution of the high throughput signal processing algorithms and also to attain the low power consumption. The digital signal processing systems are always concerned with the speed and throughput rates. Firstly, a 2 bit MAC unit is designed with apt geometries to produce optimized parameters like power, area and delay. Similarly, then the 8 bit MAC unit is designed and synchronized for the low power using the pipelined and block enabled architecture. These optimized unit become the vital building block for the applications such as audio and speech signal processing, audio and video compression, digital image and seismic data processing, transmission in digital phones, investigation and regulation of industrial processes, medical imaging as CAT and MRI scans,

speech processing and video encoding in the digital signal processing. A range of different approaches are available for the design of the multiplier and adder for MAC operations. The conventional MAC unit consists of multiplier and register accumulator that contains the sum of the preceding product with the present one. The basic operation of MAC is to compute the product of two numbers x_i and y_i and add the result to the previously stored result from the last multiplication as given below:

$$F = \sum_{i=0}^{n-1} x_i y_i$$

where i denotes the range of the values.

Due to the rise in portable electronic devices, low power schemes have become most important concern as the restricted energy of the battery operated portable devices puts the constraint on the power consumption. Hence the main inspiration is to design various pipelined and block enabled MAC architectures to achieve high speed and block enabling techniques to achieve low power consumption.

The further sections are structured as follows. The first section familiarizes the complete MAC unit, explaining each block individually. Second and third section discusses the block enable and pipeline techniques respectively.

1.2 MAC Unit

Multiply-Accumulate Unit is inevitable part of digital signal processors performing high speed operations like filtering, convolutions etc. The inputs to the MAC are fetched from a particular location in memory that is addressed and applied to the multiplier block, which performs the multiplication of two input numbers and the result is given to the adder block which accumulates the result and stores the result into a memory location (register) after accumulation. This complete MAC operation is to be realized in a single clock cycle [4].

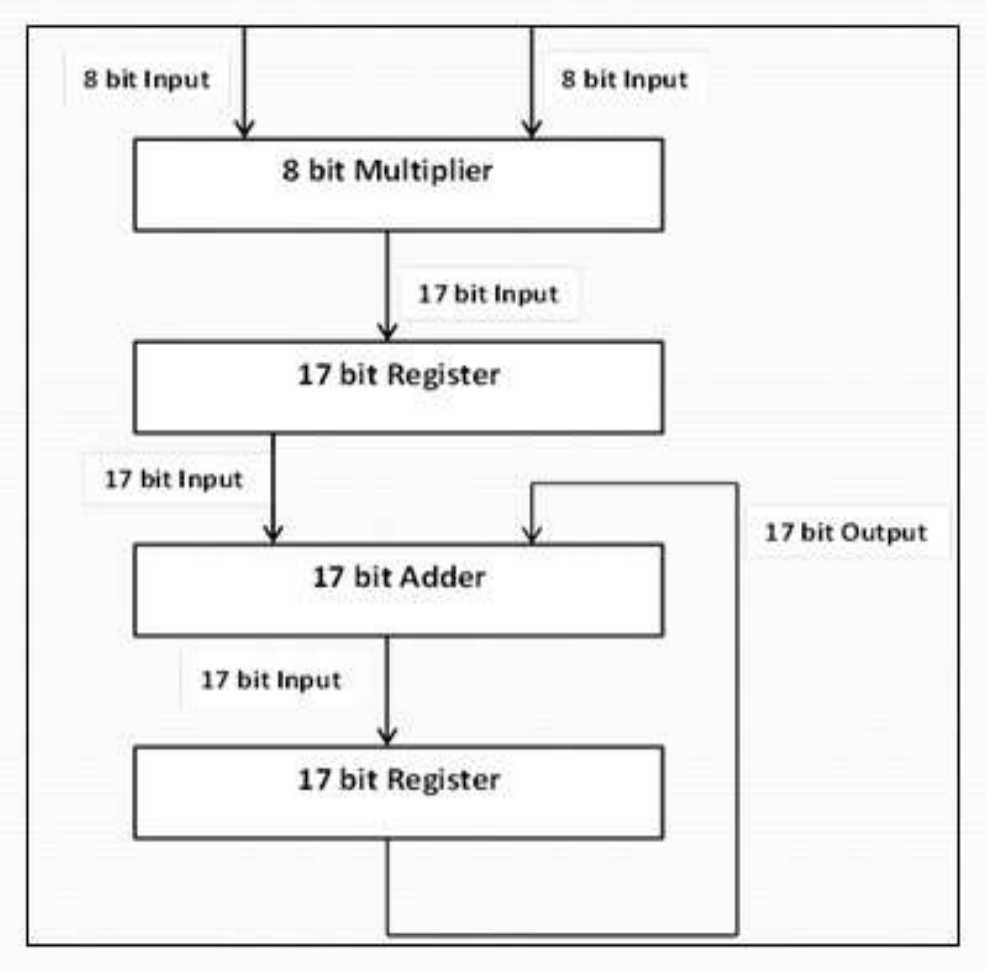

Figure 1.1: 8-bit MAC unit

The key components of MAC unit are multiplier to multiply the inputs, adder to accumulate the result and registers to store results intermediately.

1.2.1 Multiplier

In most of the signal processing algorithms, multiplication is a fundamental operation. Multipliers usually have huge area, long dormancy and eat considerable power. System performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Hence, optimizing the speed of the multiplier is a major concern for our design. However area and speed are usually the conflicting constraints to improve the speed in larger circuits. Low power VLSI circuits have become imperative measures for crafting the energy proficient electronic designs for high performance portable devices.

Multipliers are the vital creation for designing an energy efficient processor where a multiplier design picks the efficiency of digital signal processors. An extensive research work has been done on low power multipliers with different area-speed constraints.

Australian Computer Scientist Chris Wallace recommended a fast technique to perform multiplication in 1964 [5]. The hardware needed to execute this style of multiplication is large but the delay is almost ideal. The delay is proportional to log (N) for column compression multipliers where N is the word length.

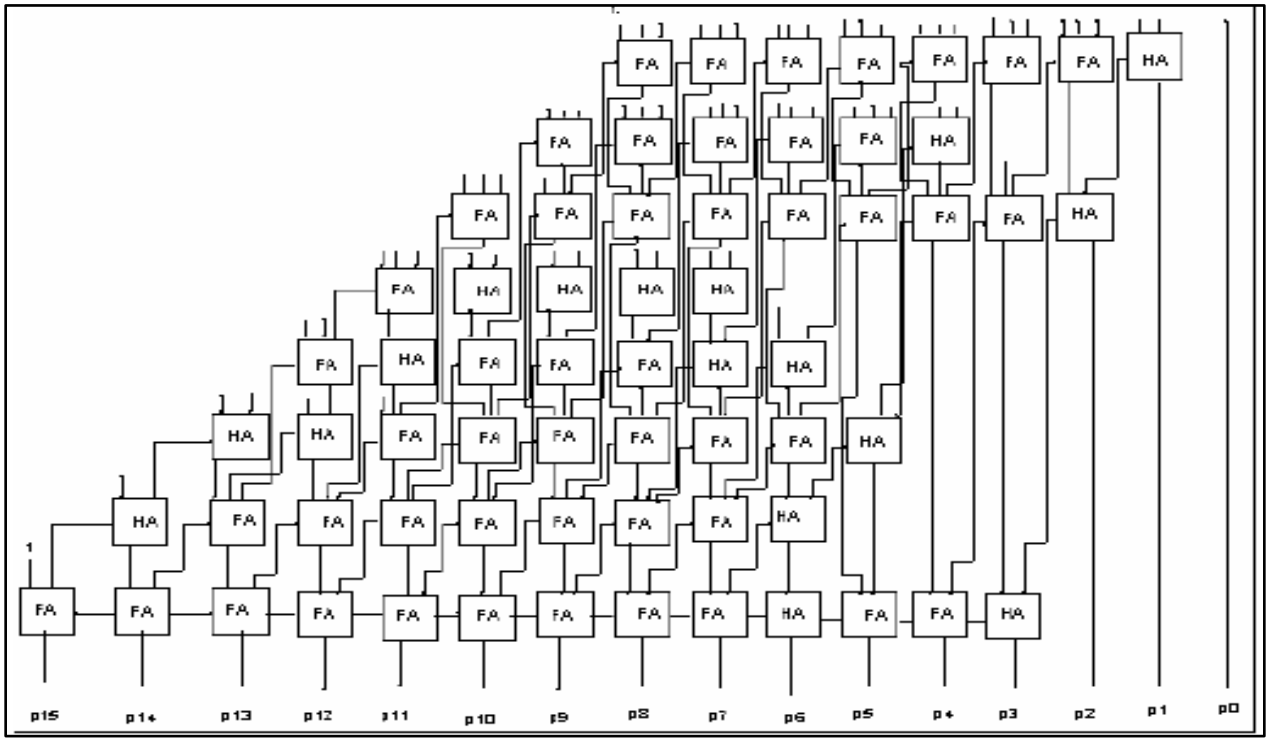

Figure 1.2: 8-bit Wallace tree multiplier

For high speed multiplication, this architecture is used where layout regularity is not the main concern. Due to the logarithmic height not the linear in word size, the Wallace tree multiplier is quicker than a simple array multiplier. The Wallace tree multiplier is chosen because of the minimum PDP and a slight increase in the no. of transistors as compared to the advantages. The comparison is given in the table below [6].

Multiplier Type	Logic Style	Delay (ns)	Power (µW)	PDP (fJ)	No. of transistor
Array	CMOS	8.300	10.73	89.06	384
	CPL	4.337	24.70	131.82	368
	DPL	4.667	19.72	92.03	448
Tree	CMOS	4.247	10.68	45.35	384
	CPL	4.105	23.61	125.25	368
	DPL	4.526	19.87	89.93	448

Table 1.1: Comparisons of performance parameters for different logic styles

The Wallace tree multiplier for 8 bit multiplication has been designed and validated in Virtuoso using 90nm technology.

1.2.2 Accumulator

An accumulator is a register in which in-between logic and arithmetic outcomes are stored. If there is no register like an accumulator, it would be indispensable to inscribe the outcome of each calculation e.g. addition, multiplication, shift, etc. to main memory, possibly only to be read right back again for use in the next operation because mathematical operations often take place in a stepwise manner, using the results from one operation as the input to the next. As the technology used for the bulky main memory is slower but cheaper than that used for a register access to main memory is sluggish than access to a accumulator i.e. register.

The basic element constituting an accumulator or a register is a D-flip flop which can store a single bit of information. Two AND gates with clock input are also used. Hence, the register cell has three inputs write/read select, previous output and D. The output is Q. The figure below shows the single bit register [7].

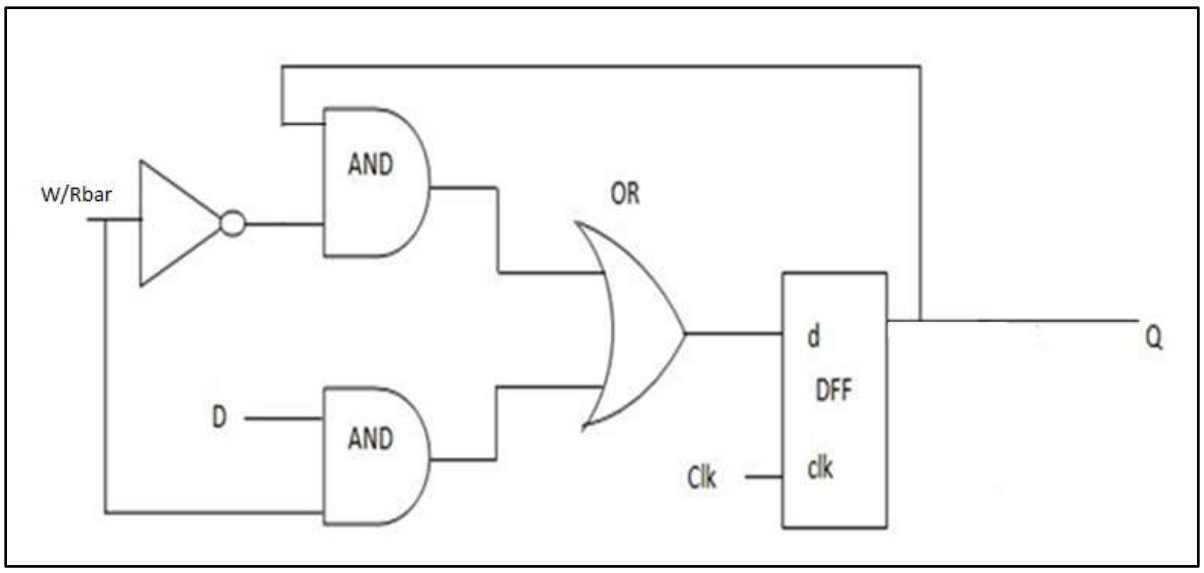

Figure 1.3: 1-bit Register

Whenever write select is logic 1, the value available at the D input is stored in the register. If the read select signal is logic 1, then the stored value is passed to the output via a tristate buffer. 4 bit registers using above circuit has been implemented in Virtuoso gpdk090 and validated by transient analysis.

1.2.3 Adder

An adder also known as summer is a logic circuit which adds two numbers. Adders are unavoidable part of logic circuits as they are not only used for addition but also to calculate the addresses, increment operations, table indices etc. Most common adders operate on binary numbers although they can be constructed for BCD, excess -3 etc. Adders are of two types:

- **Half Adder:** It executes addition of two 1-bit binary numbers and the output is Sum and Carry values. For 2-bit Wallace tree multiplier implementation and further for 8-bit multiplier half adder will be used. Also to implement 5 bit adder first block is of half adder in our design.
- **Full Adder:** It performs addition operation on 3 1-bit numbers. It takes into account the carry input also. Most of the n-bit adder architectures utilize full adders. For e.g. 5 bit ripple carry adder is used to validate the circuit performance for 2 bit MAC.

However for implementation of adder for the present research a hybrid full adder design will be utilized. In this design both CMOS logic and transmission gate logic is used.

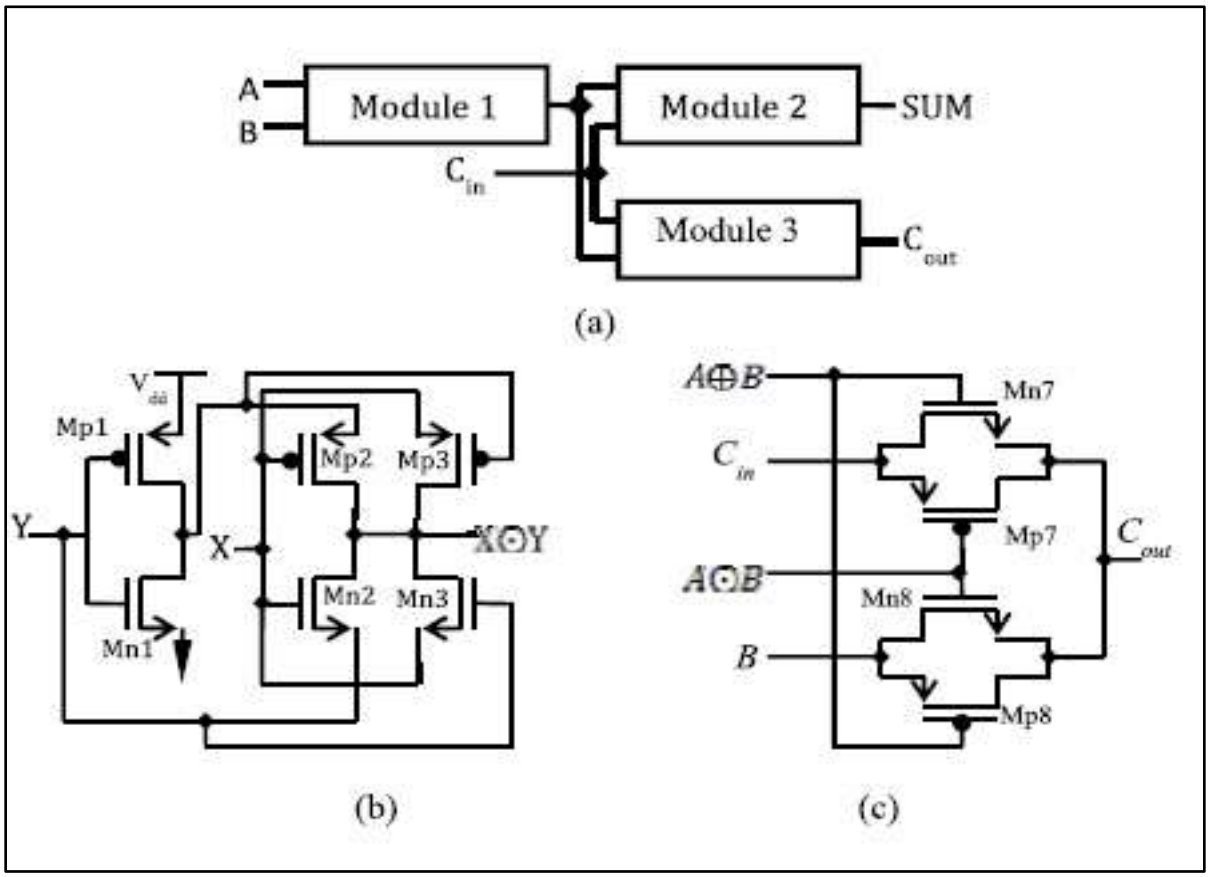

Figure 1.4: Hybrid Full Adder

This design is aimed at the optimization of both power and delay, minimizing the power delay product (PDP). The PDP of this design is only 0.931fJ for 1-bit adder as compared 10T FA PDP of 1.902 fJ [8].

1.3 Block Enabled Technique

As the feature size is scaled down, low power is the most critical issue in today's VLSI design. Block Enabling is one of the most elegant and classic technique for reduction of dynamic power, a major contributor in total power consumption of any VLSI circuit.

$$P_{dynamic} = P_{internal} + V_{dd}^2 . f_{clk} . \alpha . c_l$$

where V_{dd} is the supply voltage, f_{clk} is the clock frequency, α represents the switching activities at nodes and c_l represents load capacitances [9].

Block enabling technique facilitates saving of electrical power used by digital signal processors by reducing the switching activity α. It ensures power saving by turning on a functional logic block only when required. For this first, we have to discover out the delay for each block in block enabling technique. Every block is turned on only after the calculated delay. The successive blocks are deactivated until the inputs are available thus saving power.

1.4 Pipelined Architecture

The basic idea comes from everyday life. For example, water pipe continuously sends water without waiting for the water previously sent to be out. This leads to reduction in critical paths. In DSPs pipelining either reduces the power consumption at the same speed or increases the clock speed. In the buffered and synchronous pipelined architectures, "pipeline registers" are interleaved in-between functional stages, and are clocked synchronously. The time between each clock signal is set such that when the registers are clocked, the data written to them is the final result of the preceding stage [7].

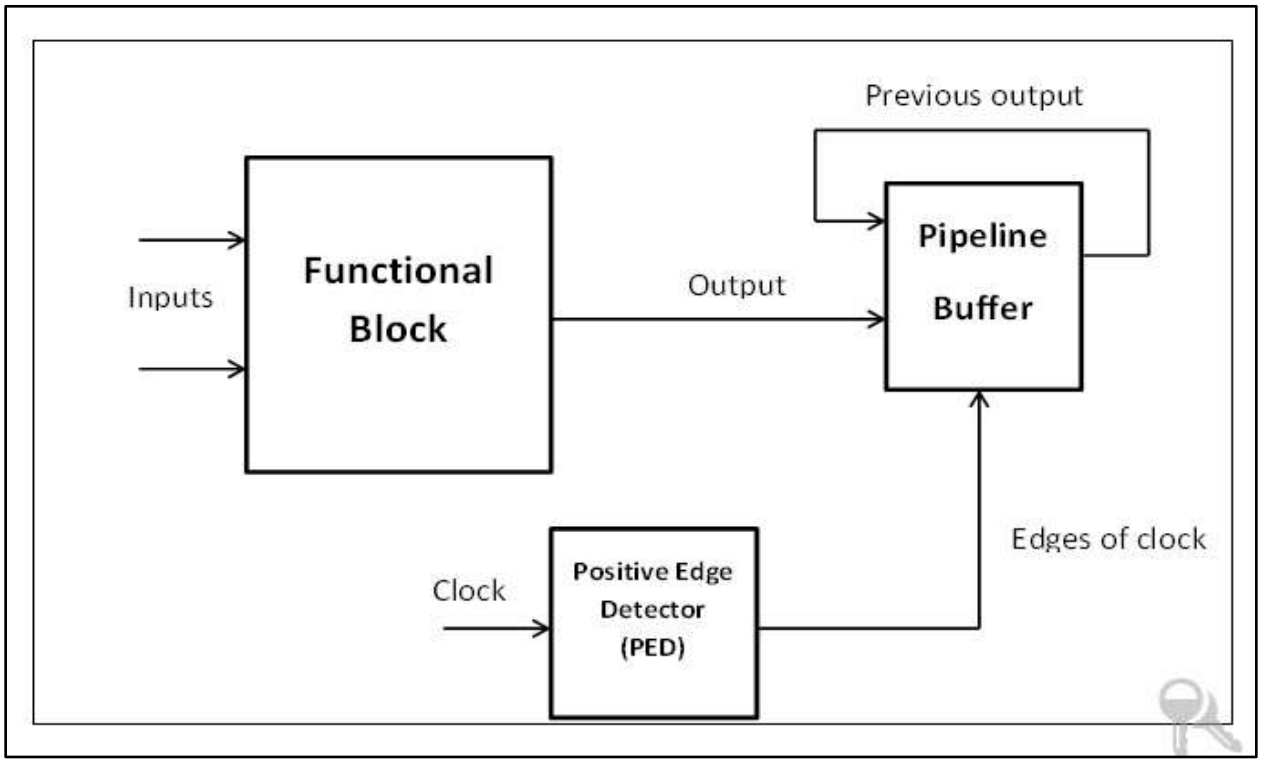

Figure 1.5 Pipelined and Block enabled Architecture

CHAPTER-2 REVIEW OF LITERATURE

2.1 Introduction

This chapter discusses the detailed review of literature undertaken by the researchers so far for Multiplier Accumulator unit. This chapter presents basic concepts and proposed theories of the papers studied for the purpose of research work.

2.2 Literature Review

Many journals, conference papers and articles related to the research work taken have been studied. Their ideas and procedures are described below.

N. Jithendra Babu *et.al,* 2015 [10]: In this paper fixed point and floating point MAC architectures were proposed. The design was implemented in Cadence Virtuoso and the performances of the suggested structural designs were analyzed using the cadence spectre tool. Power delay product (PDP), power and delay of each individual block and the entire MAC unit were calculated using Cadence transient analysis simulations.

Avisek Sen *et.al,* 2013 [7]: The research paper explored the proposal of low power 8 x 8 bit MAC using block enabling technique to decrease the power dissipated. The MAC unit was realized in 130 nm process technology in CMOS and the entire unit was clocked at 200 MHz with 1.5V supply voltage. Block enabling technique turns off the block when there are no inputs available and turns the blocks on after the premeditated delay to perform normal operation.

Teffi Francis *et.al,* 2013 [11]: In his research paper the motive was to optimize power and delay of Braun Multiplier by using Bypassing Technique. The delay was reduced using Ripple Carry Adders (RCA) in the last phase of full adders by improved adders. Various CMOS implementation techniques such as Double Pass Transistor Logic (DPL) and Transmission Gate (TG) and other logic styles were implemented in 130nm technology.

Ashish B. Kharate *et.al,* 2013 [12]: This paper explored the new MAC design which used the pipelining technique and clock gating technique to reduce the overall power of MAC unit to be used in digital FIR filters. Every block was analyzed for its performance. At first, 1-bit MAC

was crafted and the analyses for power were done so that n-bit MAC unit can be created and the total power consumption can be estimated. The MAC units designed in this work were intended for filter realizations in high speed digital signal processing application.

P.Jagadesh *et.al,* 2013 [13]: The research paper proposed the design of high performance 64 bit MAC. The modified Wallace Tree Multiplier was used to implement multiplier and the adder used in this design was Carry Save Adder. The MAC implementation was done in digital environment with Verilog-HDL and synthesis was done using the Cadence RTL compiler in 180nm library. The entire unit operates at 217 MHz and the power dissipation estimated was 177.732 mW. This design is intended for high performance processor which requires large number of bit operations.

Deepak S. *et.al,* 2012 [14]: In this research paper, new multiplier architecture was proposed which reduced the number of partial products by 25%. This multiplier design was used along with diverse adders to implement MAC (Multiply Accumulate) unit. After the analysis and comparison with different parameters of array and booth multipliers, it was found that the proposed multiplier has the lowest propagation delay compared to its counterparts.

Aditya Kumar Singh *et.al,* 2012 [6]: In this research paper, AND gate using different logic styles was realized and 4 x 4 unsigned array and tree multiplier architecture were designed using these different AND gate realizations and 1-bit full adders. The average power, delay and PDP of 4 x 4 bit multiplier realizations following various logic styles were simulated in T-spice of Tanner EDA tool with 5V supply voltage and 25°C temperature in 150nm technology. It was witnessed that the CMOS implementation consumed the lowest power among CPL, DPL and other logic styles. Also, Wallace tree multiplier displayed the minimum PDP.

Shanthala S. *et.al,* 2009 [15]: The research paper focused on the design a MAC unit in 180 nm process technology. Different architectures of multipliers and 1-bit static and dynamic adders were implemented. Spice code was written to test the correct functionality of MAC. The design was crafted in schematic composer from Virtuoso from bottom to top level. The power dissipation came out to be 50.26nW and 3*1.05 mm^2 area. The latency of the design was 6 clock cycles.

A.Abdelgawad *et.al* 2007, [16]: In this paper, the critical delays and hardware complexities of the traditional MAC were studied, to implement the area-efficient and low delay MAC. The proposed MAC design used binary trees created using a modified 4:2 compressor circuits. To optimize the speed, modified compressors were avoided in the critical path. The stimulation was done for 8 bit, 16 bit and 32 bit MAC architecture. The results illustrated that the proposed design reduced the area by 6.25%, 3.2% and 2.5% and increased the speed by 14%, 16% and 19% respectively.

Uma *et al.*, 2012 [17]: This present paper stressed on the choice of selecting trades offs of delay, power and area of different adder topologies for optimum design. The different topologies considered and analyzed were Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Carry Skip Adder, Carry Save Adder (CSA) and many more. The analysis for area, power and delay were done at 120nm technology file using Micro Wind tool. The comparisons between different topologies were done using above mentioned parameters.

Duvvuri Divya *et al.*, 2012 [18]: This research work proposed the design of reversible full adder circuits. These circuits were further used to design 4 bit Ripple Carry Adder and subtractor using the reversible logic. Cadence RTL compiler was used to do the analysis for the power dissipation and delay using the proposed design.

Madhusmita Mahapatro *et al.*, 2010 [19]: The goal of this research paper was to find an alternative for all the basic irreversible logic gates for designing full custom layouts. The proposed gates were designed at 250nm technology and by using those gates they have designed 4-bit binary parallel adder and multiplier circuit using the reversible logic.

Maii T. Emam *et al.*, 2010 [20]: In this research work, two novel designs of adder and subtractor were proposed using reversible logic. The first design used the two's complement logic for the implementation of adder/subtractor. The second design used the novel reversible gate logic for the design implementation of reversible adder/subtractor unit and further this unit was applied to design a ripple adder or subtractor.

Farshad Moradi *et al., 2009* [21]: The research work proposed in this paper exploits two new ideas for full adder topologies to reduce power dissipation. Sense Energy Recovery Full adder (SERF) and Gate Diffusion Input (GDI) were used with different full adder topologies to

enhance the power performance of the circuits. Different full adders deigns were compared with each other and the power consumption was reduced to 62% in SERF Design and 86% in GDI full adder design.

Vahid Foroutan, *et al.*, 2008 [22]: In this research the concept of majority function was exploited for the low power design. The XOR gates were eliminated where it was time consuming. The adder circuit was implemented using two level dynamic zipper techniques. The proposed design produced the substantial reduction of power dissipation in the complete circuit leading to the best power delay product (PDP).

Helga Evangelene *et al.*, 2014 [23]: The research work presented proposed a novel hybrid low power flip-flop which used the sleepy stack inverters. The sleepy stack flip-flop was then compared with the conventional Dual Dynamic Flip Flop (DDFF) in the Cadence 90nm technology. The proposed flip-flop was also used for the implementation of other flip-flop circuits like T, SR and JK. These flip-flops were compared with conventional flip-flops of DDFF for their performance evaluation.

Kalarikkal Absel *et al.*, 2013 [24]: In this paper a new Hybrid flip-flop and embedded flip-flop were proposed so as to eliminate the capacitance present at precharge node. The key was to decrease the pipeline overhead. The design was implemented in the 90nm UMC process and compared with the other implementations in terms of area, speed and power dissipation.

Jun Cheol Park *et al.*, 2006 [25]: In this research a new technique known as sleepy stack was proposed for low power CMOS circuit designing. Sleepy stack design uses the sleep signal along with the conventional signals. During the sleep mode, a logic state is retained to achieve the lower leakage power. The design technique can be useful to generic circuits and the power leakage can be reduced consequently providing the engineers a new method of handling the leakage power issue.

CHAPTER-3 DESIGN METHODOLOGY

3.1 Hypothesis

To design and implement a Pipelined Block enabled 8 bit Multiplier Accumulator unit (MAC) using the Cadence Virtuoso which performs entire operation in single clock cycle. Also do the power and delay analysis for comparison with the standard MAC unit in 90 nm technology.

3.2 Objective

- To design the analog circuits for the various subunits of multiplier and accumulator (MAC) unit.
- To analyze the power and delay of the overall proposed MAC unit and do its comparison with the conventional MACs.
- To synchronize the complete unit such that the entire operation is performed in single clock cycle, thus resulting in efficient speed for the digital signal processors and reduced power consumption.
- To enable the blocks of MAC in such a manner that when there is no inputs available they are turned off to decrease the dynamic power consumption of the overall unit.
- To do the comparison of the current research with the digital implementation(Verilog code) of the MAC unit.

3.3 Tool

Cadence: The merger of Solomon Design Automation (SDA) systems and ECAD, Inc. founded Cadence Design Systems, Inc. in 1988. During the tenure of first CEO Joseph Costello, Cadence became the largest electronic design automation company producing software to design chips, PCBs as well as IP cores for memories, SoC, interfaces etc. [26]. Cadence products mainly focus on FPGA and ASIC designs for custom, analog, digital and mixed signal applications. Few of them are Encounter platform, Virtuoso Platform, Incisive Platform, Palladium Series, OrCad/PSpice etc.

Cadence Virtuoso: Cadence Virtuoso is a platform that provides tools for designing full-custom integrated circuits (ASIC) which includes schematic capture, behavioral modeling (Verilog AMS), and simulation of circuit, custom layout of chip, verification at physical level, extraction and back-annotation. Cadence® Virtuoso® Analog Design Environment (ADE) is the advanced environment for design and simulation giving designers access to a new parasitic approximation. It has different process technologies available; however 90nm Generic Process Design Kit (GPDK090) has been used for the present research. The process technology and necessary information to do the device-level design in the Cadence environment is contained in the PDK.

3.4 Proposed Work Plan with Timelines

During pre-dissertation, literature review was done. In dissertation-I, 2-bit Wallace tree multiplier was implemented with block enabled and pipelined architecture. The 4-bit output of the multiplier was stored on the pipelined 4 bit register implemented using D flip-flops with read and write enable. 5-bit ripple carry adder was designed to validate the MAC operation. Then a final pipelined register of 5 bits was designed to store and output the final result of MAC operation. Positive edge detection (PED) block was designed in the Virtuoso environment. Buffering technique was implemented as described above to allow pipelining. Block enabling and pipelining architecture was validated by implementing the circuits on 4 cascaded buffers. Entire design has been implemented in 90nm technology. In dissertation-2, 8-bit MAC unit has been designed and implemented in Virtuoso which performs the entire MAC operation in a single clock cycle. The 8 bit Wallace tree multiplier multiplies two 8 bit numbers and the 16 bit result is stored on the intermediate 16 bit register for quicker access to the results usually immediately as the main memory is much slower. This result along with the previous output of the MAC is given as input to the hybrid adder which uses both transmission gate and CMOS logic. This adder adds the two 16 bit numbers and the output of 17 bits is stored on the next register for immediate access for the next operation.

The above MAC operation is completed in single clock pulse. The delay of 500ps is introduced after each block to maintain setup and hold time violations in check. The overall time required to calculate the MAC operation is 1.5ns.

3.5 Problem Formulation

MAC unit performs the important mathematical operations in the digital signal processing systems. Since, the DSPs speed is decided by the MAC unit speed, the main consideration of the research done in last few years has been focused to boost the speed of MAC.

Also, as DSPs are inevitable in portable electronics, a constraint on power consumption forces to optimize the energy efficiency. Therefore power dissipation is another major concern in the MAC operation. The power dissipation depends on the transistor count. Therefore, the power dissipation can be reduced by decreasing the no. of transistors also optimizing the area.

Finally, the last consideration is the speed of the overall functional unit of the MAC. This can be achieved by using the efficient multipliers and accumulators. Also as the entire operation is synchronized with single positive edge triggered global clock, the speed is enhanced whereby decreasing the power consumption by enabling block enabling technique.

Also for real time application of any design the unit must be synchronized with the global clock of the entire chip. This synchronization is achieved in this design of MAC unit which can be synchronized with the global clock of DSP.

3.6 Problem Rectification

- **Power**

  The power dissipation is directly proportional to the area covered by the circuitry. Hence the power can be reduced by reducing the area of the circuit and also by using the low power components. In this handcrafted design the multiplier, adder blocks have designed for smaller power and delay. Also using the block enabling technique we can turn on only the required circuitry i.e. when the actual inputs to the block are available. These delay values are calculated using the setup and hold timing checks.

- **Area**

  The area is a major concern in any of the analog circuit design. The area can be reduced by reducing the no. of transistors in the circuit design. By reducing the transistor count and playing with the W/L ratio of the transistors' the area of the circuit can be reduced. In this research the blocks used are such that the optimum PDP is achieved with the minimum required transistor count.

- **Speed**

  The speed of the MAC is a very important design parameter for high speed system operation. The speed can be increased using the efficient multipliers and accumulators in the design. The synchronous buffered and pipelined architecture increases the speed of overall MAC by fetching data in advance. Buffered architecture allows for the faster access to the data because of the intermediate registers as the fetching of data from the main memory will be very slow, hindering the performance of MAC unit.

CHAPTER-4 RESULTS AND CONCLUSION

4.1 Scope of the Study

MAC unit is the core of all digital signal processing applications involving convolution, filtering etc. DSPs are indispensable part of most battery operated devices available today e.g. laptops, smartphones, calculators etc. These devices usually have restraint on the performance due to the limited power. Hence it becomes imperative for present research to enhance the power performance of the MAC whereby increasing the speed is an added advantage. The present research uses the different architectures for individual blocks of MAC to decrease the power consumption and also pipelining and block enabling techniques are used to boost its performance further. The design is implemented at schematic level in Cadence Virtuoso and is apt for real time applications as the whole unit is synchronized and the entire MAC operation is performed in 1.5ns.

4.2 Experimental Work

MAC unit consists of three main modules: multiplier, adder and registers connected in order described earlier. The schematic designed in the 90nm technology in Virtuoso has been shown below. This contains four blocks. The first block is 8 bit multiplier, second block is 16 bit register, third is 17 bit hybrid full adder and the final block is 17 bit register.

All the blocks seen in the schematic below are the symbols of the actual design which are explained one by one.

Multiplier

This symbol is an 8 bit Wallace tree which works on the positive edges of the clock. Whenever the positive edge of the clock is detected output is latched to the output port of the multiplier otherwise the previous value is latched.

The Wallace tree architecture uses the AND gate for partial product calculations and the 8 standard half adder and 48 hybrid full adders has been used to design this multiplier connected in the order described in the chapter 1. The schematic entry for the same is shown below.

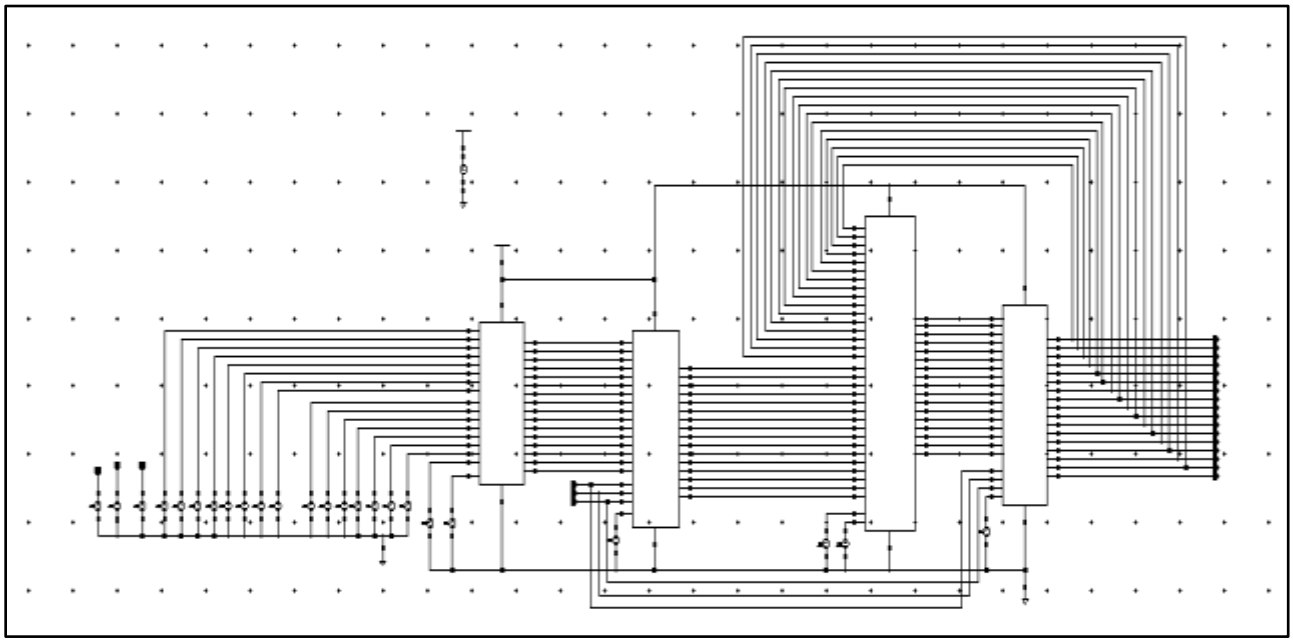

Figure 4.1: 8 bit MAC schematic in Virtuoso

The first block is the multiplier symbol which is given two 8 bit binary numbers as input. These inputs are given as Vpulse signals. The symbol which is hierarchal successor of Wallace tree multiplier symbol along with the PED block and the latch is shown below in fig 4.3.

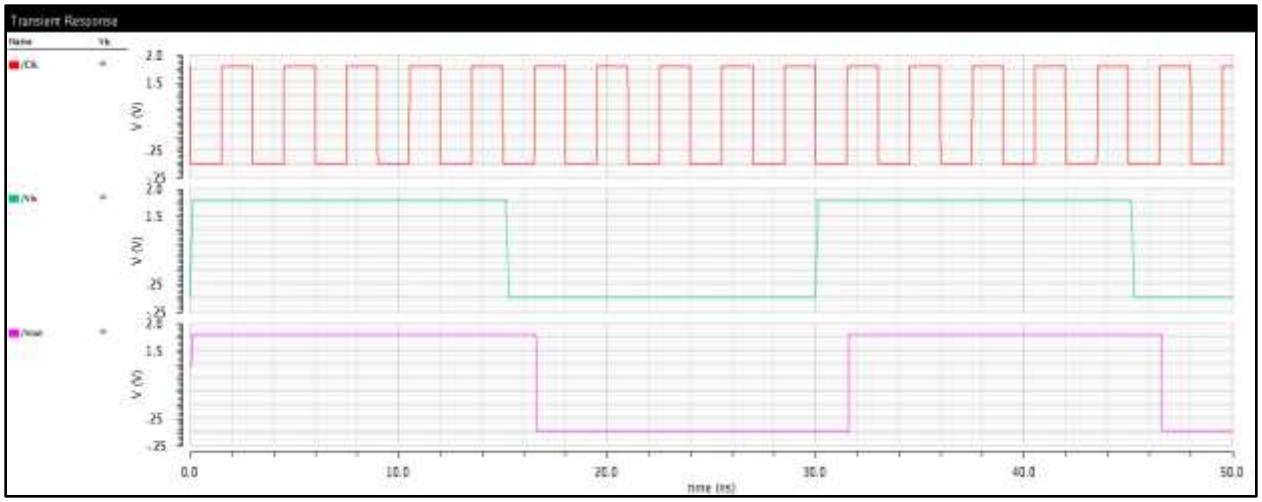

Figure 4.2 Transient response of PED block in ADE L

The waveform above shown verifies the working of PED.

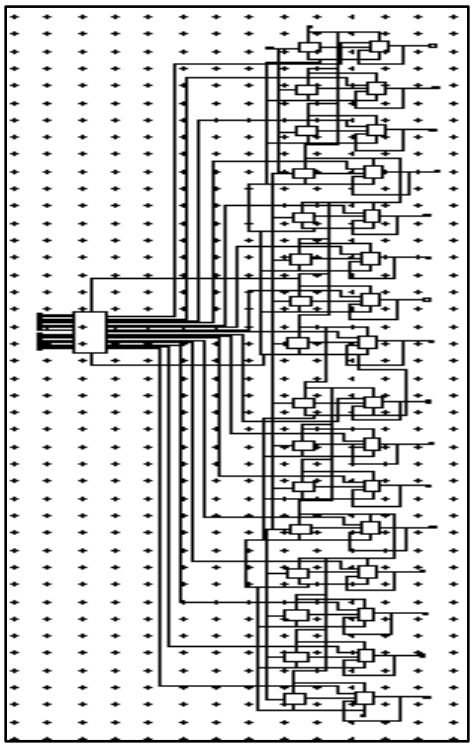

Figure 4.3: Multiplier with positive edge detector and latch

The block first shown is Wallace tree multiplier whose schematic is shown below.

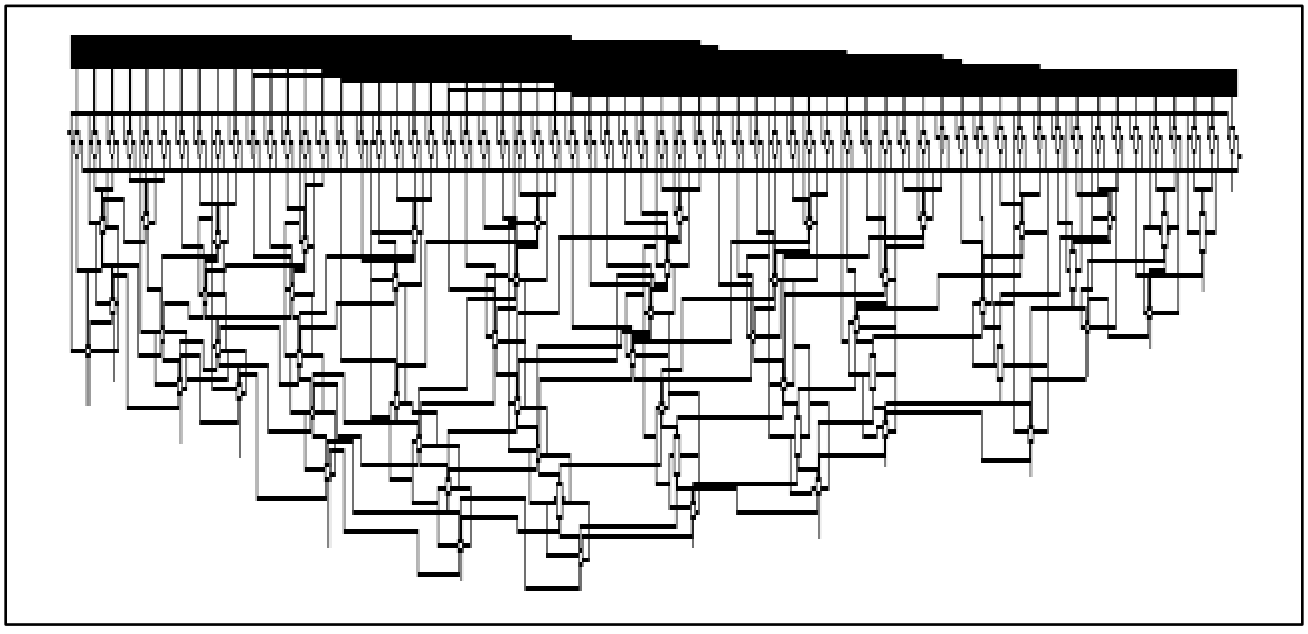

Figure 4.4: 8 bit Wallace tree multiplier schematic

The PED block is the positive edge detector block. The input to this block is the clock pulse given as Vpulse with rise time and fall time of 25ps. The block detects the clock pulse and the output of the block is the high logic only for the positive edges of the clock signal.

Register

After multiplier next block is 16 bit register. Also 17 bit register is used for storing the final result of MAC. The symbol of the 17 bit register is shown below.

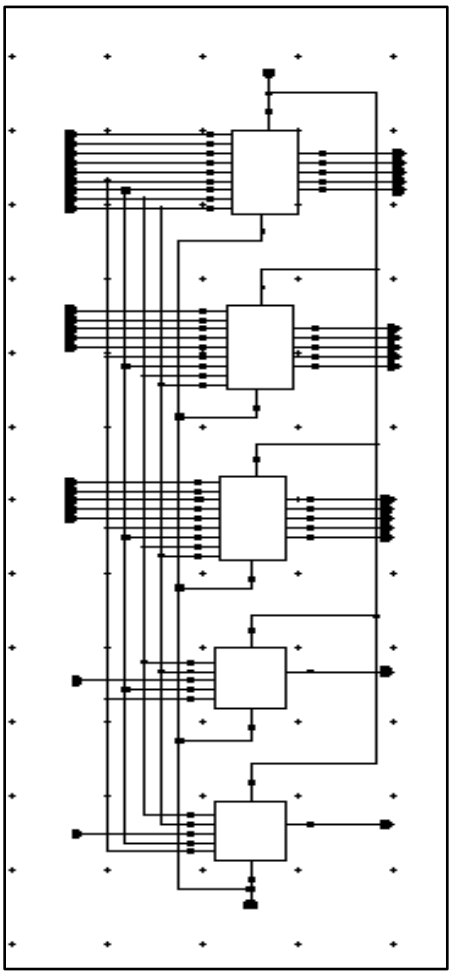

Figure 4.5: 16-bit Register Schematic

This symbol further contains 5 bit symbol register whose schematic entry is shown below. These registers can store 5 bit of information. These, three no. are connected in series to make 16 bit register.

The 5 bit register symbol contains five 1-bit registers which can store a single bit of information.

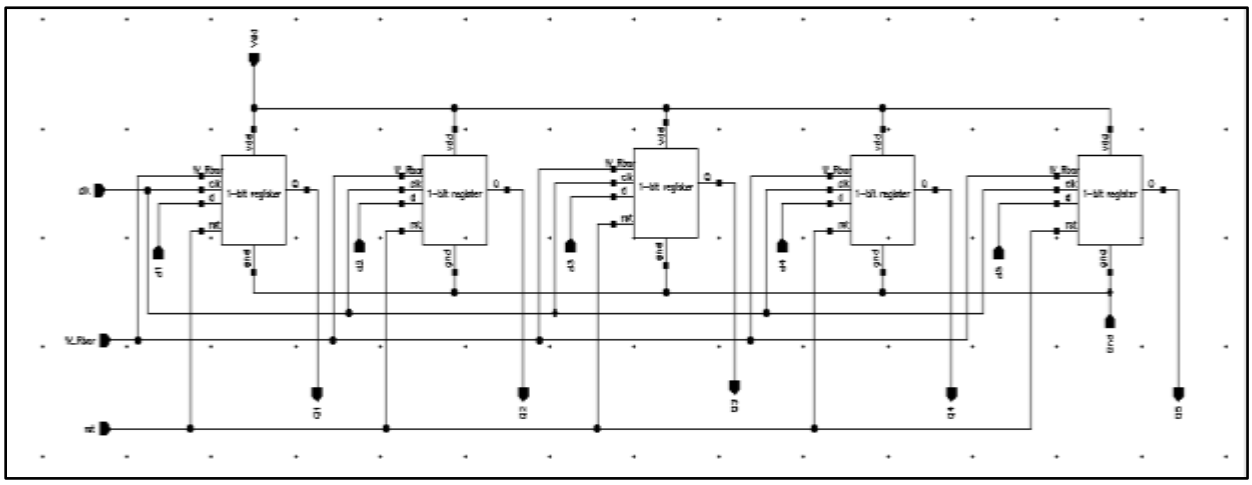

Figure 4.6: 5-bit Register Schematic

The 1 bit register contains two AND gates and 1 OR gate. The storage element used is the sleepy stack D flip-flop. The AND gates are used for signal gating. Whenever the clock pulse is high and W/Rbar = 1, the data available at the input is latched to the output.

However for W/Rbar = 0, the data previously written is read back. Also whenever the clock is low previous data is latched.

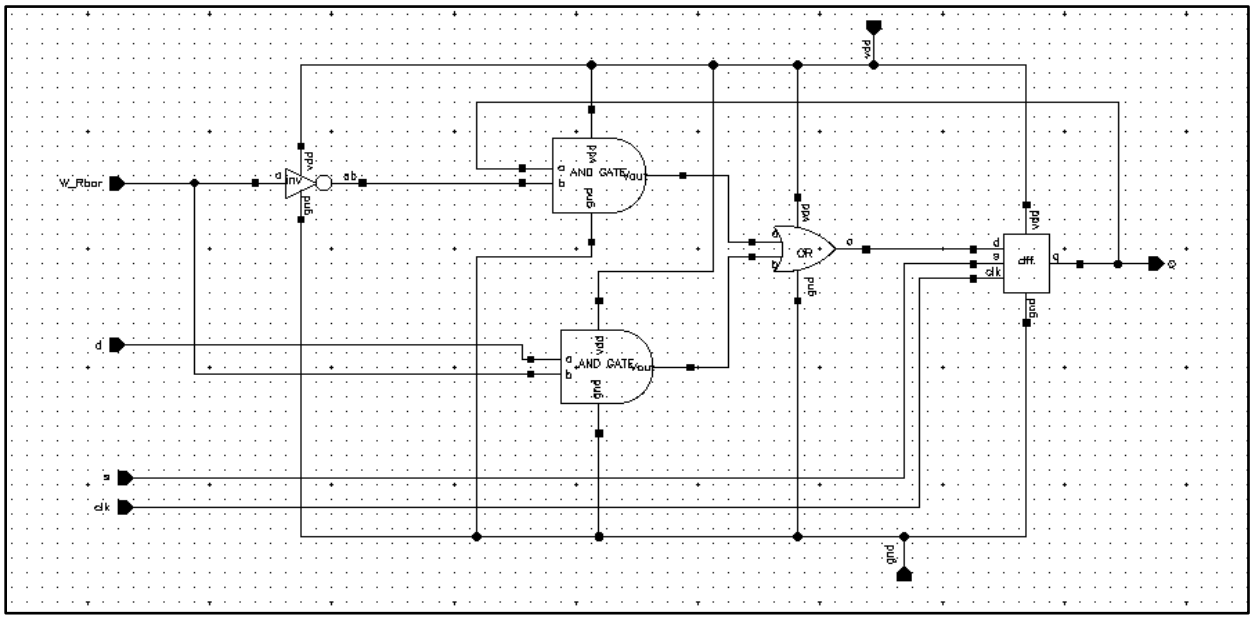

Figure 4.7: 1 bit register schematic

Finally, the D flip-flop used is using sleepy stack inverter architecture. The schematic entry for the flip-flop is shown below.

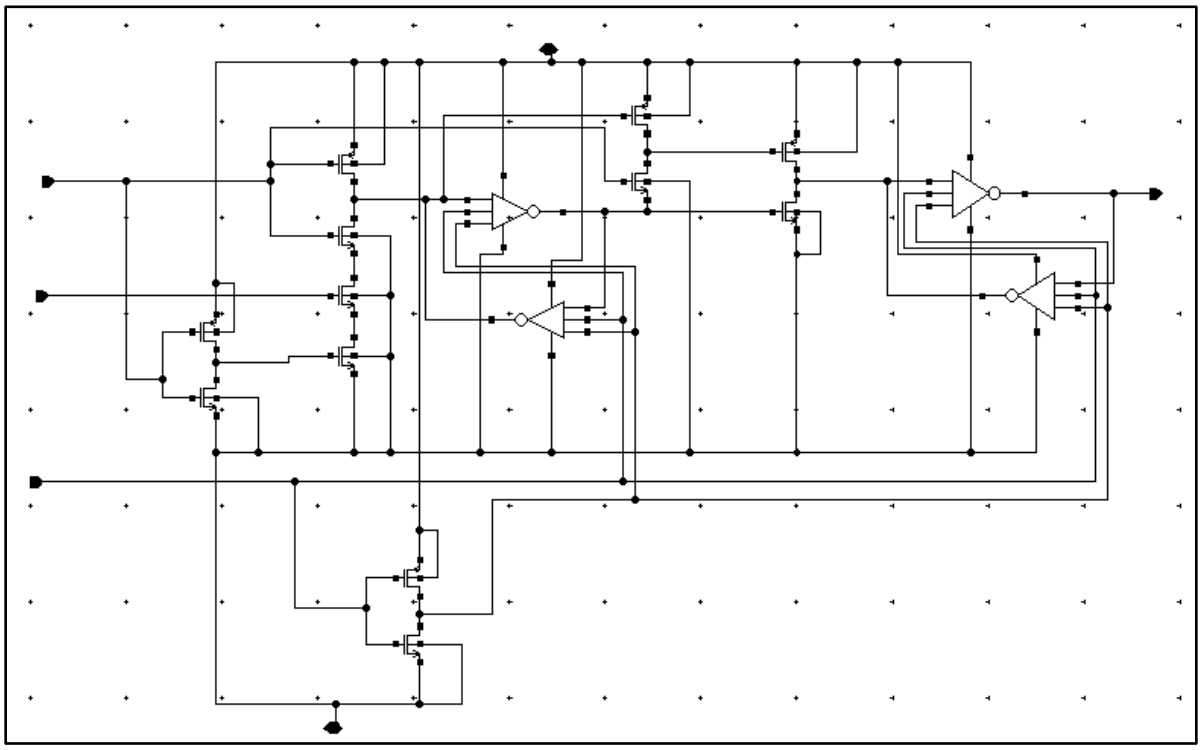

Figure 4.8: D flip-flop implemented using sleepy stack inverters

The D flip-flop uses the sleepy stack inverter. This design uses the additional sleep transistors which are controlled by sleep signal. Whenever the sleep = 0, the sleep transistors are turned off to reduce the leakage power and also the present state is saved. The transistors between the sleep transistors are neither connected to Vdd or gnd directly, hence the leakage power reduction.

When the sleep = 1, the sleep transistors are turned on and the inverter operates as a normal inverter. The schematic entry for the same is shown below.

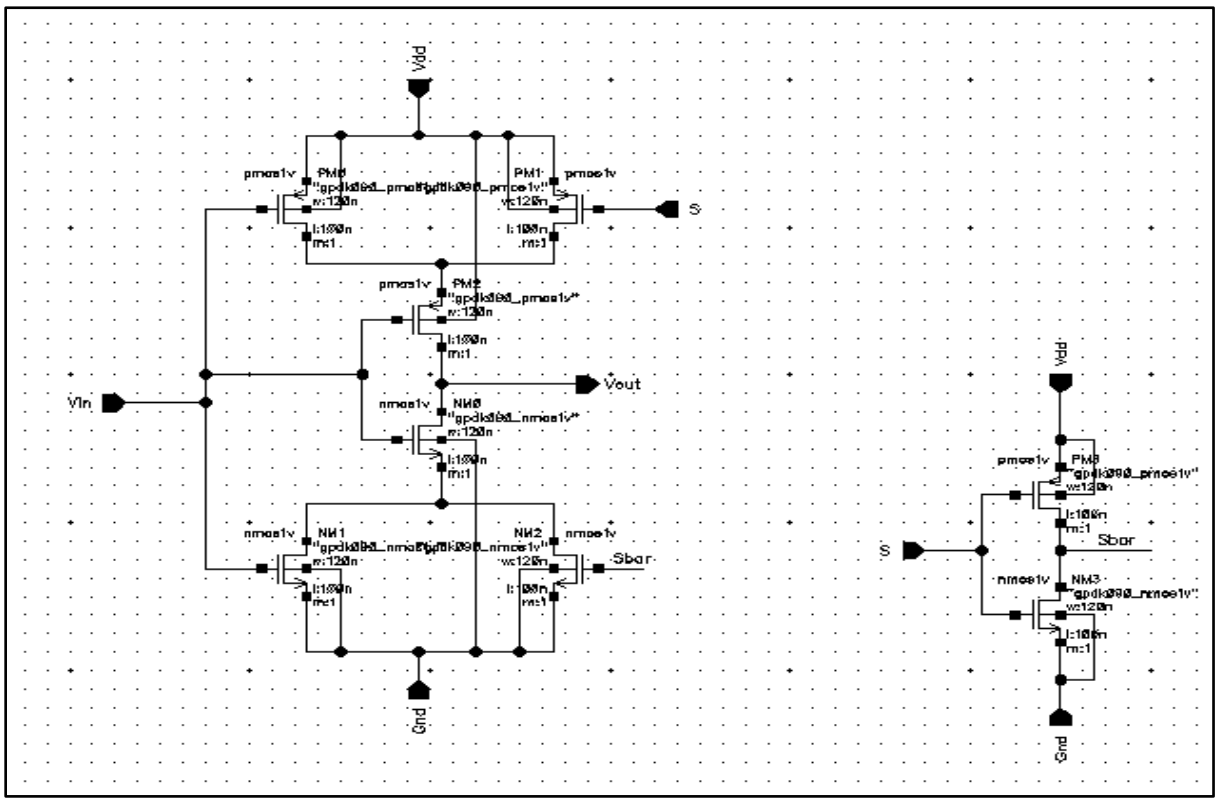

Figure 4.8: Sleepy stack inverter implementation in Virtuoso

Adder

The next block is the 17 bit adder block. Its schematic is as shown below. The adder is 17 bit whenever two 16 bit numbers are added the maximum result will be 17 bits.

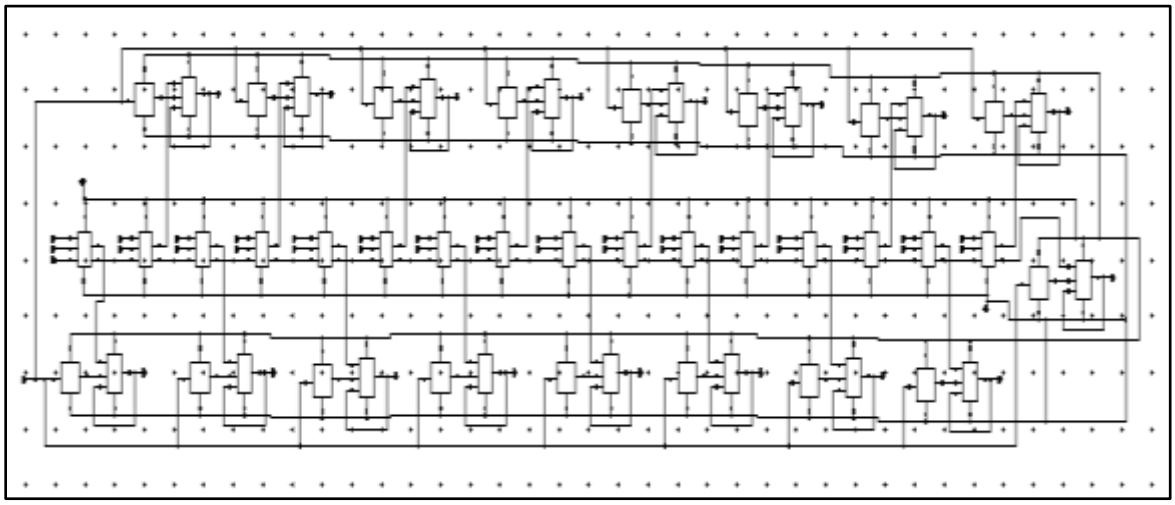

Figure 4.9: 17 bit full adder schematic

The design uses 17 hybrid full adder blocks with PED and latch. Latch circuit is used to get the previous data when the positive edges of clock are not present. The schematic of the latch circuit is shown below.

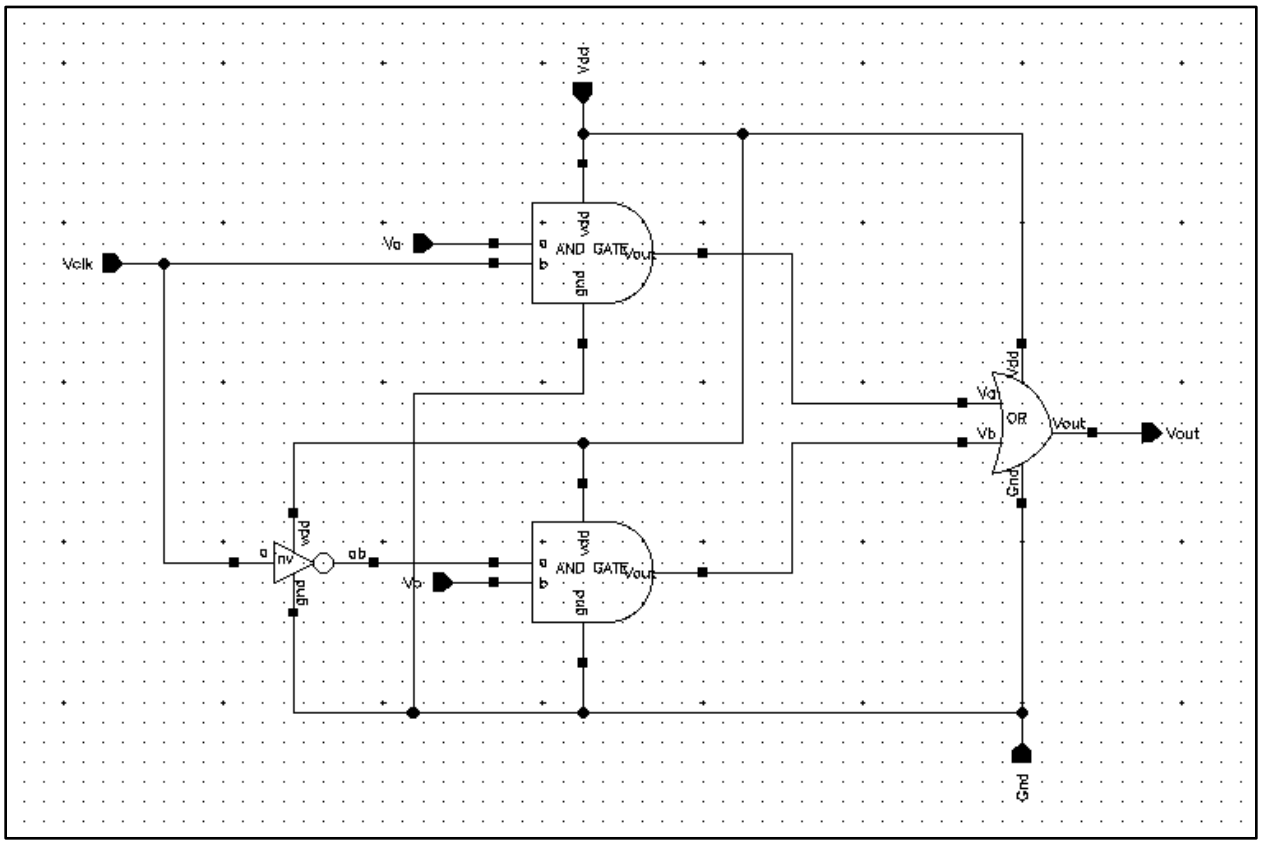

Figure 4.10: Latch schematic view in Virtuoso

The hybrid full adder is implemented using both the CMOS and transmission gate technique. The XOR and XNOR function for sum output is implemented separately and carry output is generated using separate transmission gate module.

The sum block uses the CMOS inverters and GDI (Gate Diffusion Input) technique to generate the sum output.

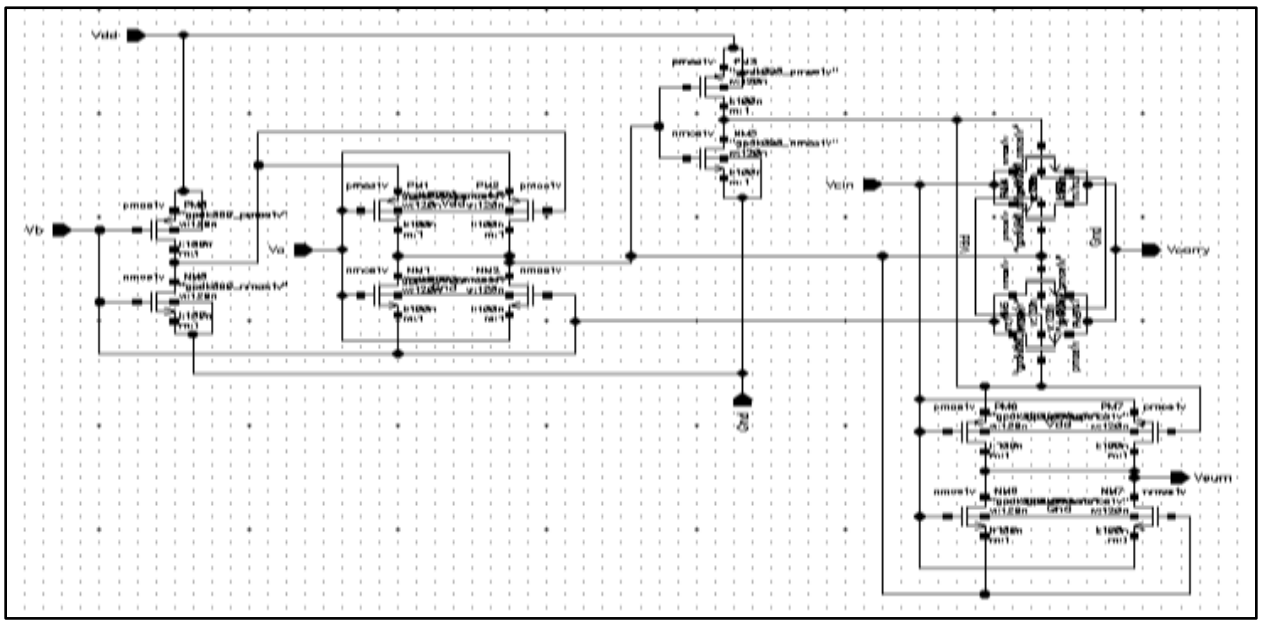

Figure 4.11: Hybrid full adder schematic

Positive Edge detector block has been designed to detect positive edges of the clock. Each block has been synchronized with clock and the outputs are buffered. All blocks have been designed to work at positive clock edges using PED block.

The complete architecture has been pipelined using synchronous buffers. The buffer has been incorporated in the design to latch the previous values when the clock is zero. Block enabling and pipelining architecture has been validated by implementing the circuits on 4 cascaded buffers.

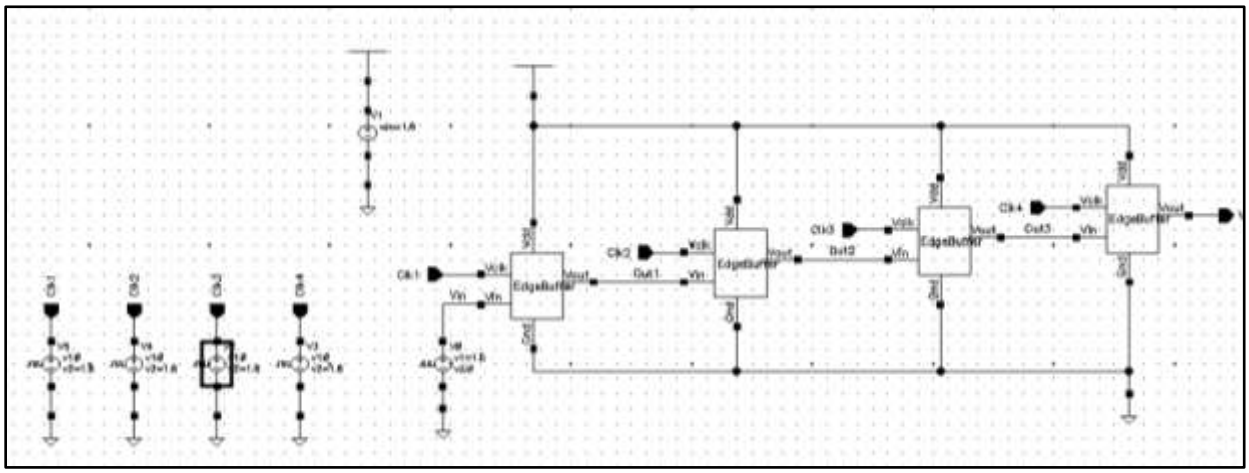

Figure 4.12: Circuit using buffers to validate sync buffered pipelined architecture

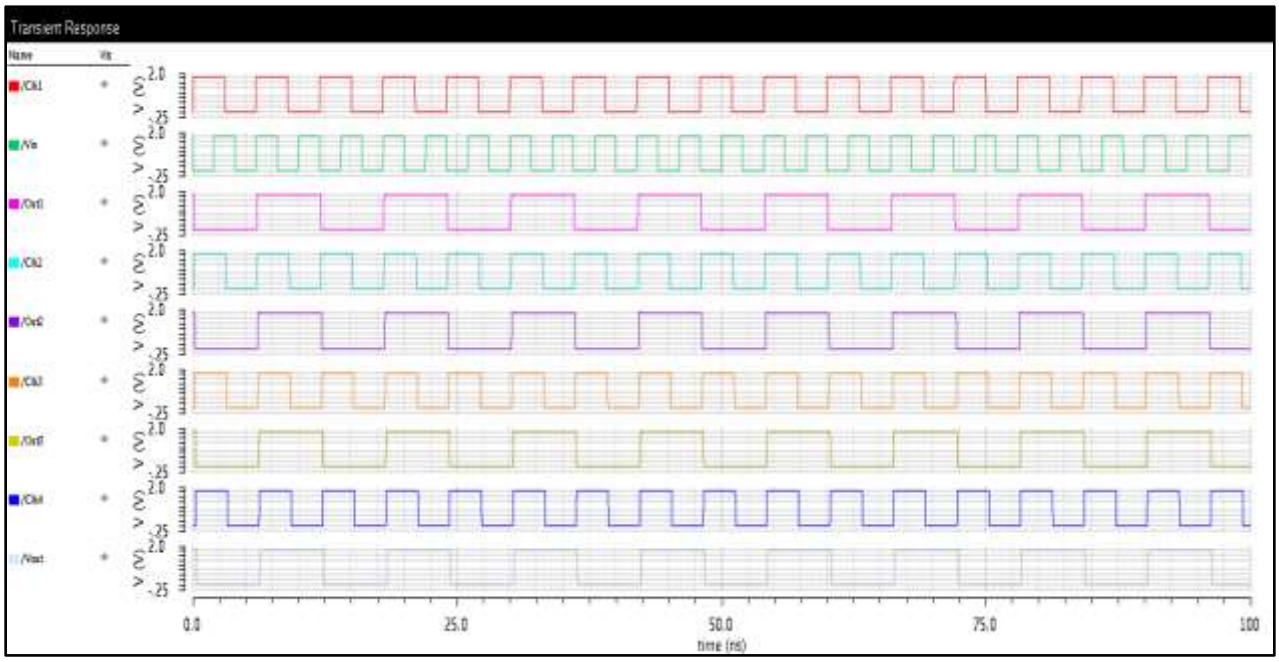

Figure 4.13: Transient response of the test circuit

To discuss the advantages of the implementation in analog environment, the design was also implemented in digital using Xilinx ISE 9.2i and also the detailed analysis was done using Cadence NCSim. The RTL obtained for the 8 bit MAC after synthesis done in NCSim is shown below.

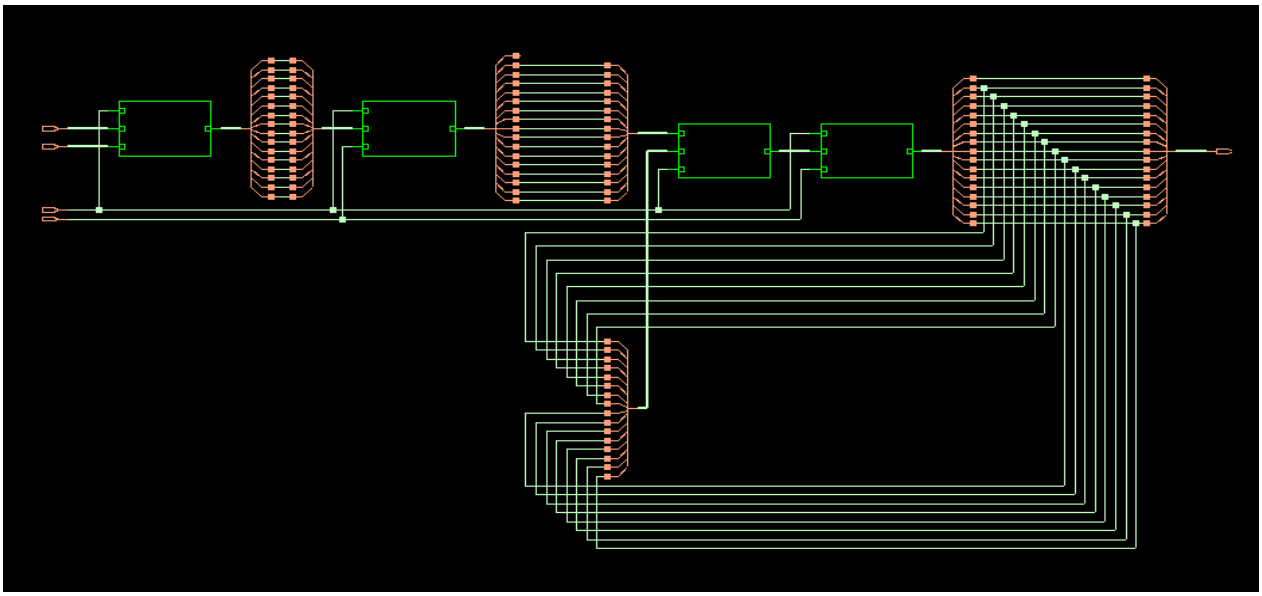

Figure 4.14: RTL view of 8 bit MAC in NCSim

4.3 Results

The 8 bit MAC unit implemented in Cadence Virtuoso in 90nm technology is validated for its correct operation by doing transient analysis. The transient analysis simulation time taken is 25ns. Simulation times longer than 25ns were taking a long time as the no of outputs to be plotted were large.

The two 8 bit inputs given to the MAC unit are 01001011 available as a0-a7 and 01010001 available as b0-b7 for the simulation windows shown below. This number is multiplied in the multiplier block, whose 16 bit output is 1011110111011 shown on the lines m1-m16.

This result is then stored in the register on the positive edges of the clock. The data saved is available on the lines r1-16. This result then serves as the input for the adder block where the previous output of the MAC is added with the current one.

For the first instance the previous output is taken as 1111111111111111. This was achieved by resetting the registers for 4ns so as to achieve stable values on all the lines i.e. logic 1.

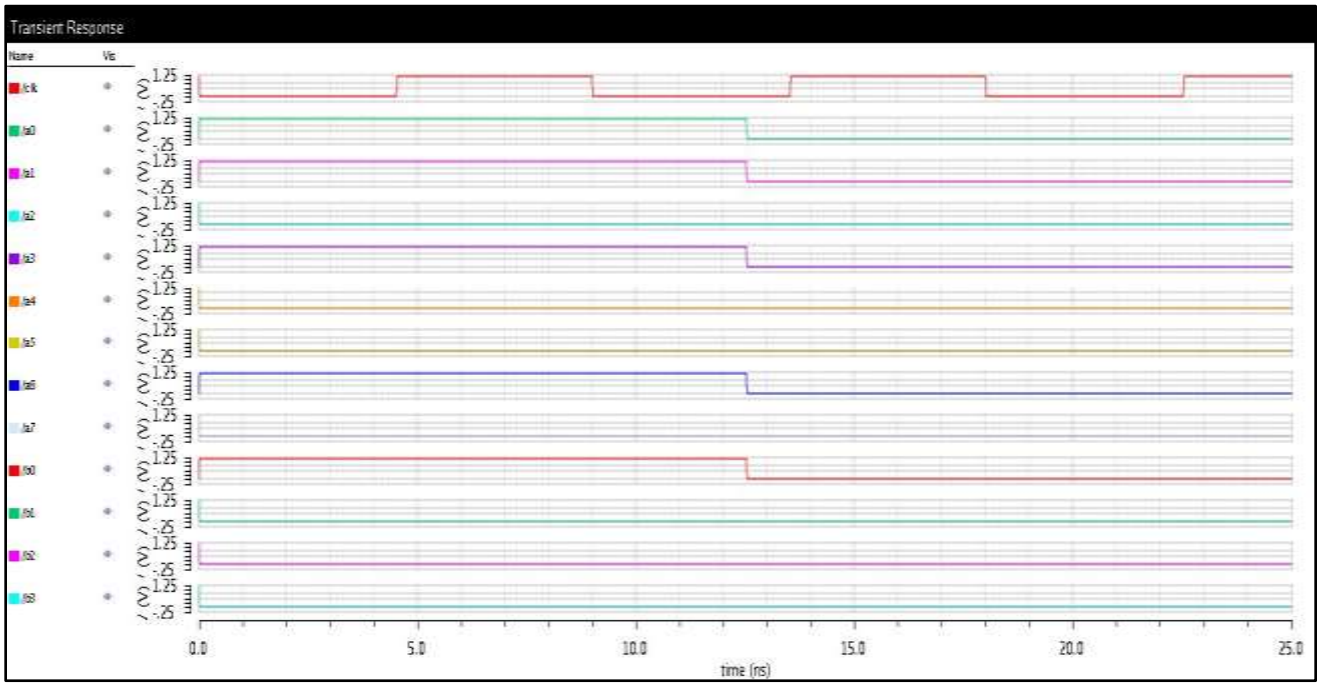

Figure 4.15: Simulation window 1 for 8 bit MAC

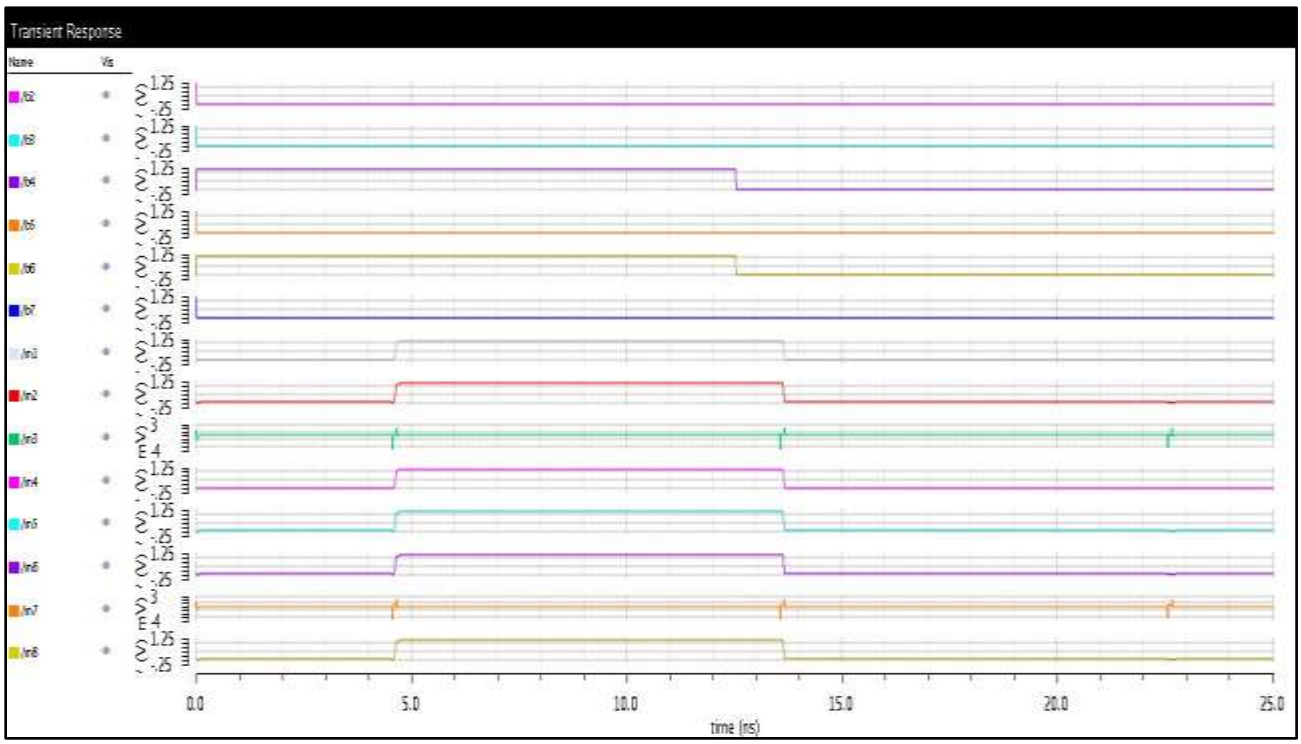

Figure 4.16: Simulation window 2 for 8 bit MAC

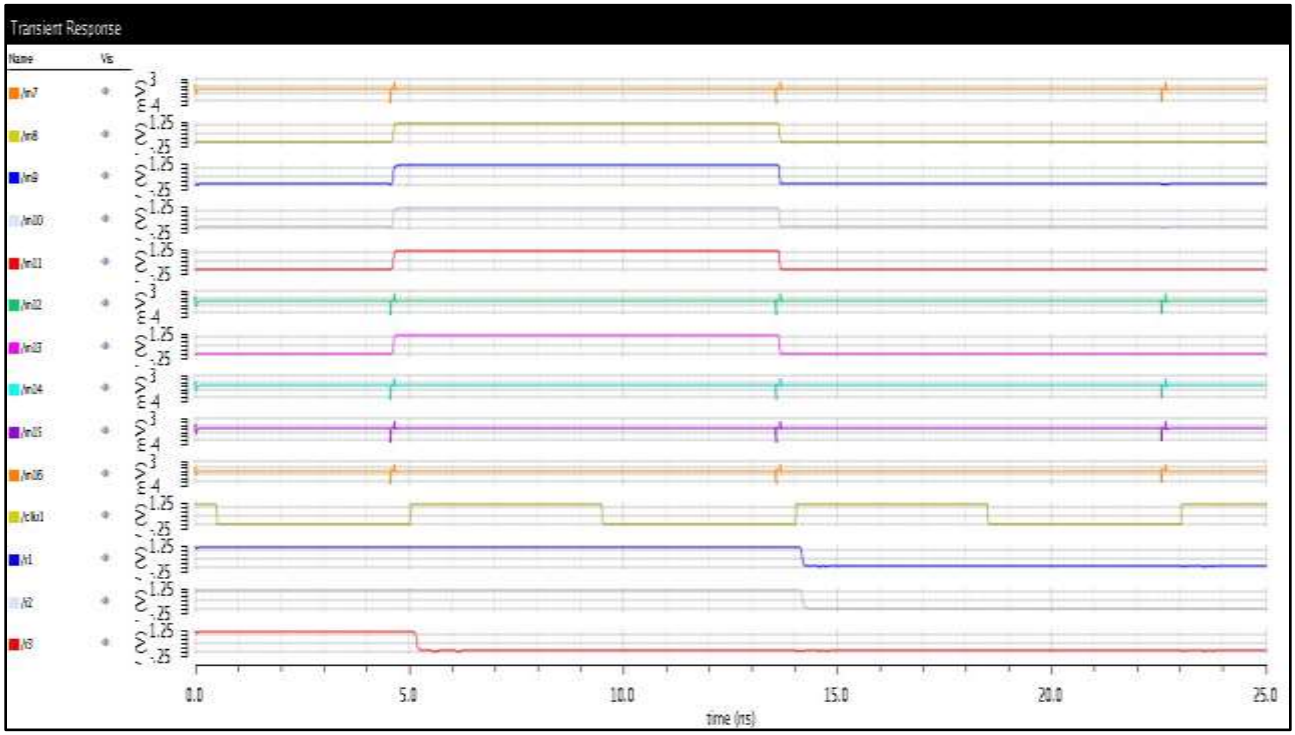

Figure 4.17: Simulation window 3 for 8 bit MAC

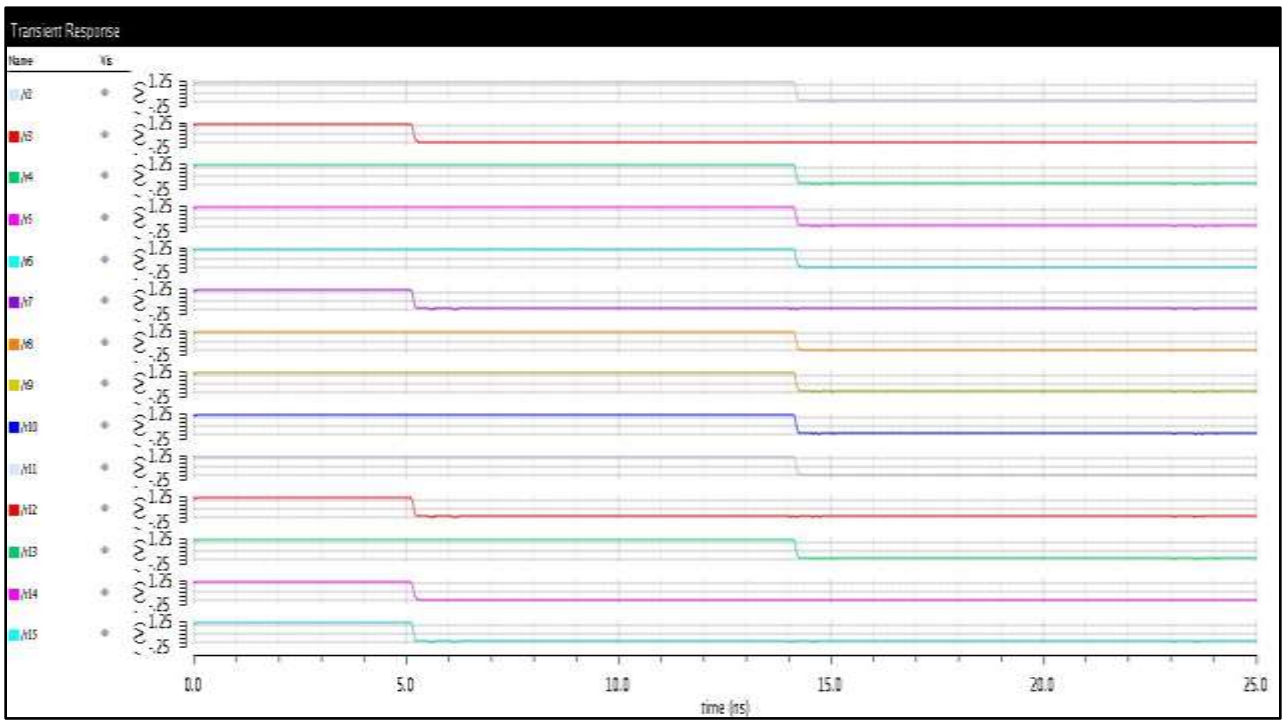

Figure 4.18: Simulation window 4 for 8 bit MAC

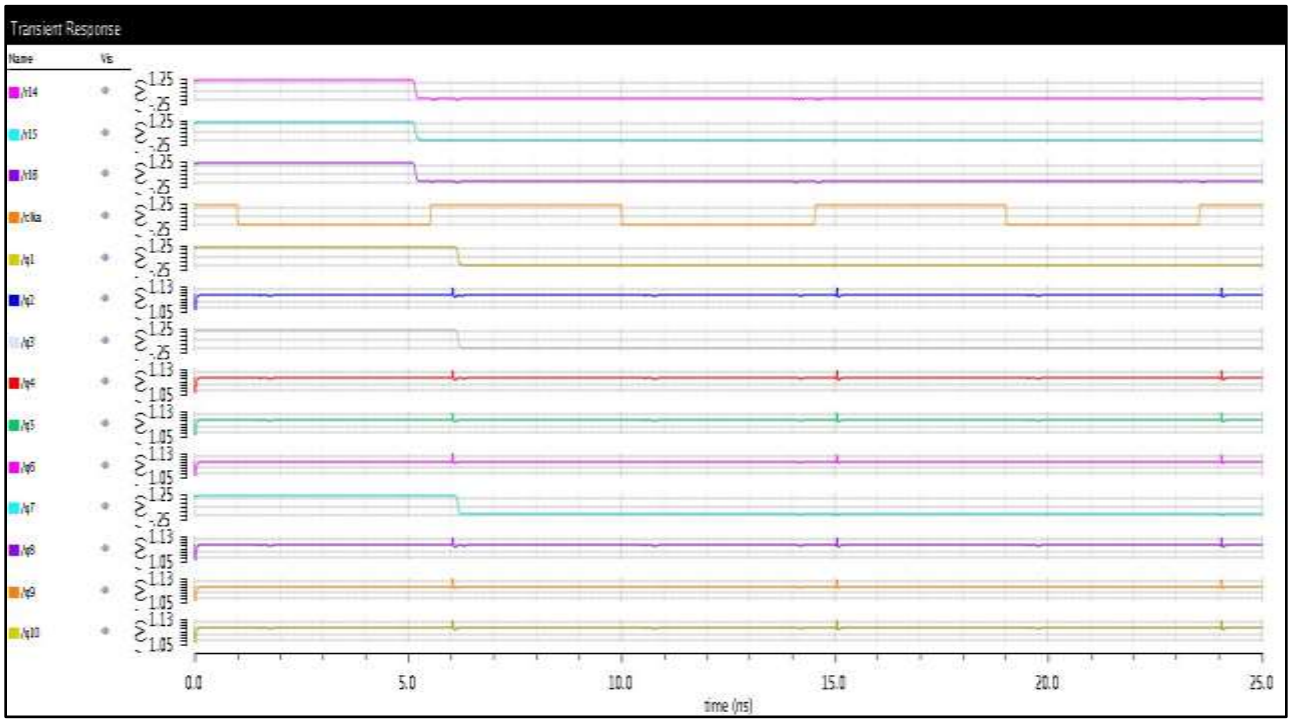

Figure 4.19: Simulation window 5 for 8 bit MAC

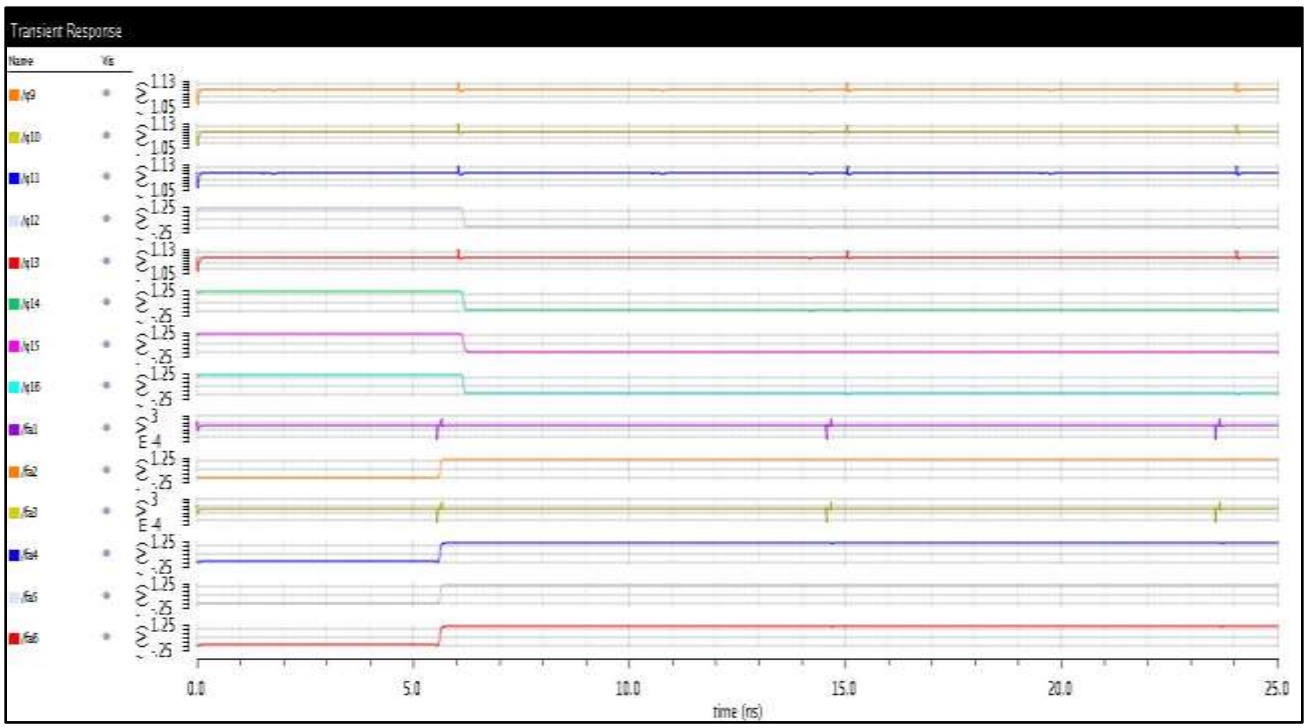

Figure 4.20: Simulation window 6 for 8 bit MAC

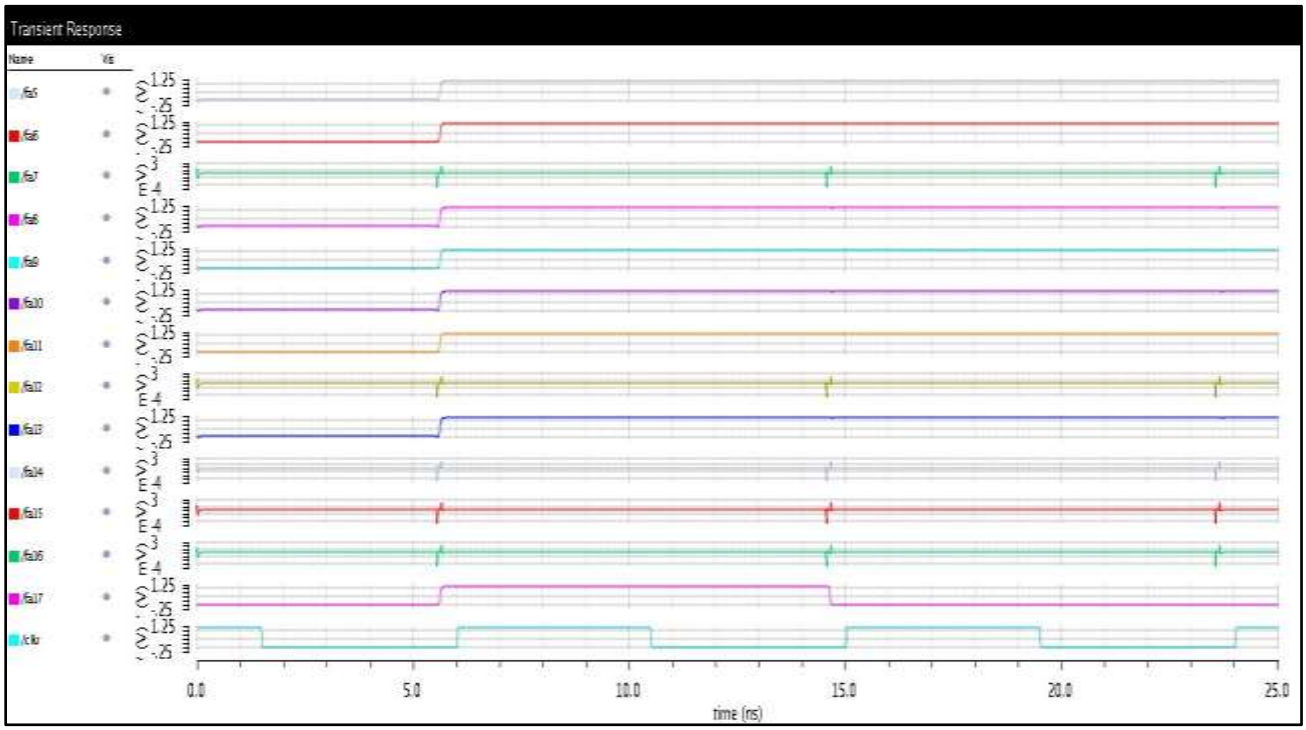

Figure 4.21: Simulation window 7 for 8 bit MAC

Finally the addition is performed on the positive edges of the clock and the 17 bit result obtained after adding 1011110111011 and 1111111111111111 is 17 bit binary number 10001011110111010. This is available on lines fa1-fa17. This is then saved on the register lines shown by the q1-q17.

To validate the each block's correct functionality, they have been simulated separately using their test circuits. The simulations for 8 bit multiplier run for 25ns is shown below.

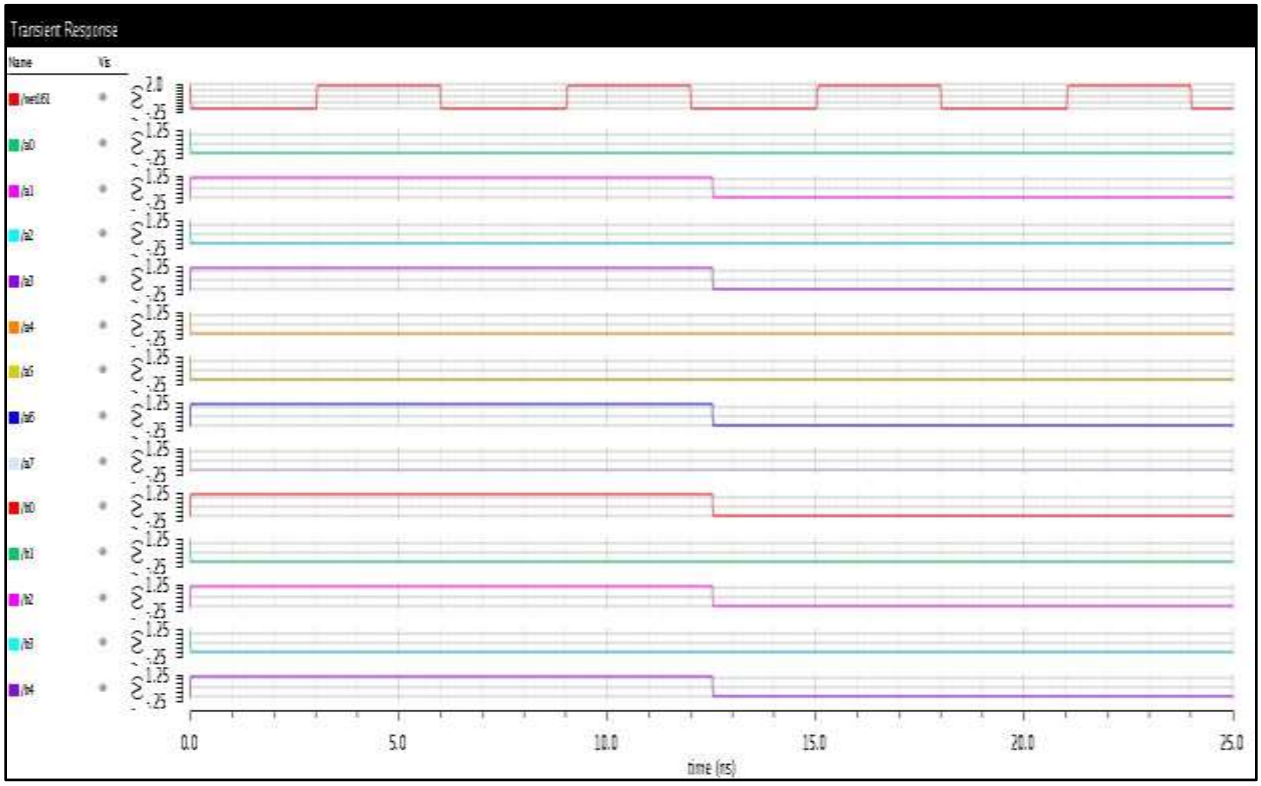

Figure 4.22: Simulation window 1 for 8 bit multiplier

The simulation results show that the input to the multiplier block is two 8 bit binary numbers 01001010 and 01010101 detected on first positive edge. When multiplied the result comes out to be 16 bit binary 0001100010010010 which is verified in the above results.

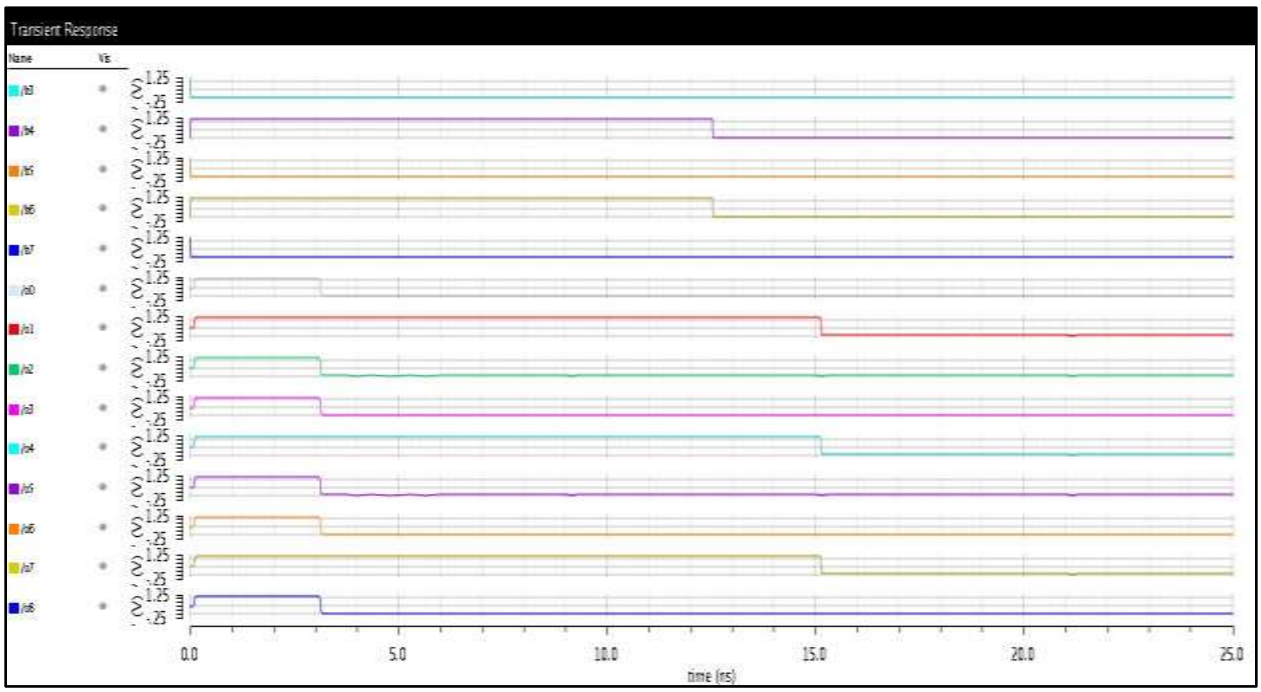

Figure 4.23: Simulation window 2 for 8 bit multiplier

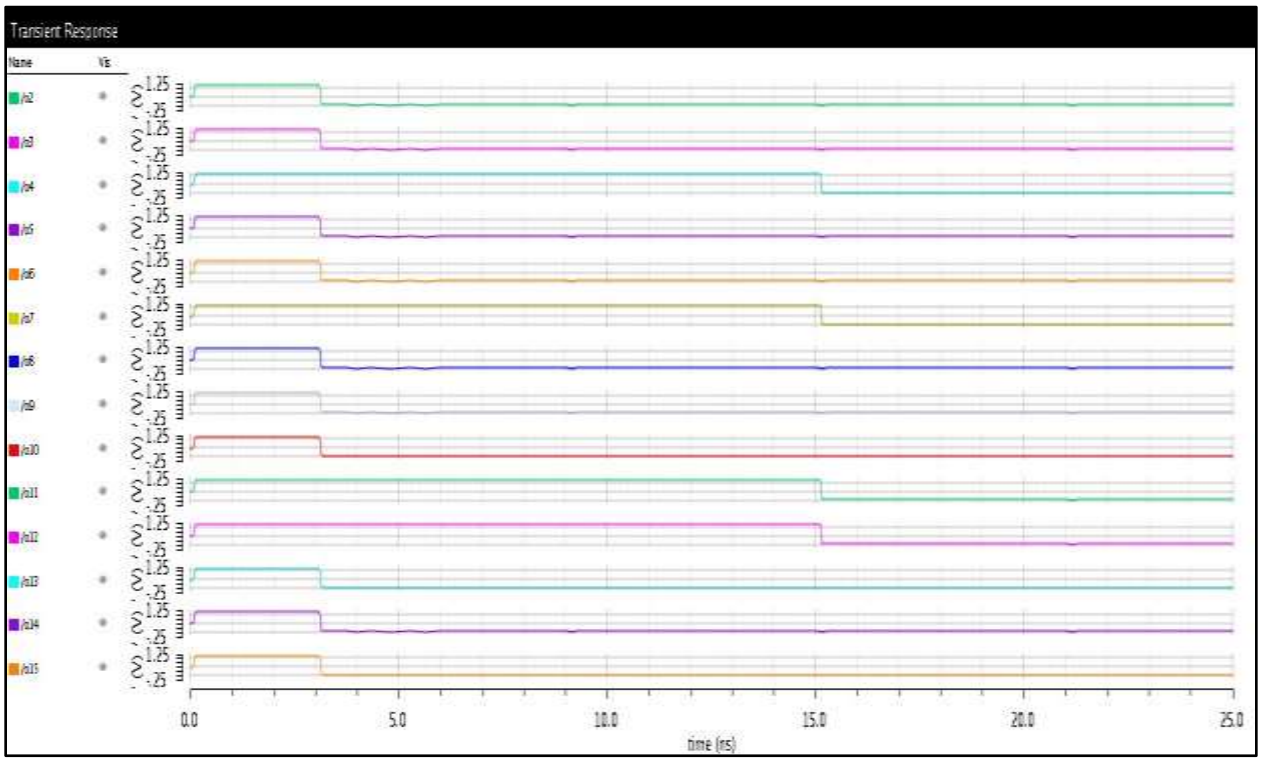

Figure 4.24: Simulation window 3 for 8 bit multiplier

Similarly the results can be verified for 17 bit full adder. The simulation for transient analysis was done for 25ns. The simulation window results are shown below.

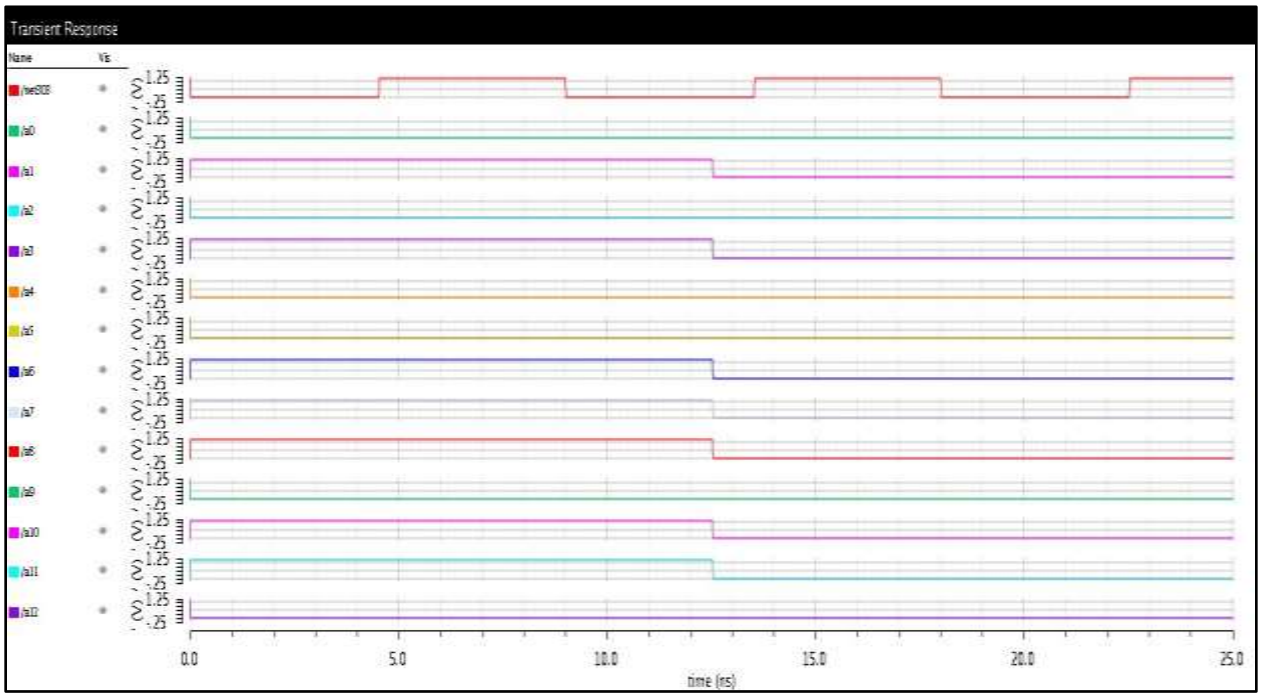

Figure 4.25: Simulation window 1 for 17 bit adder

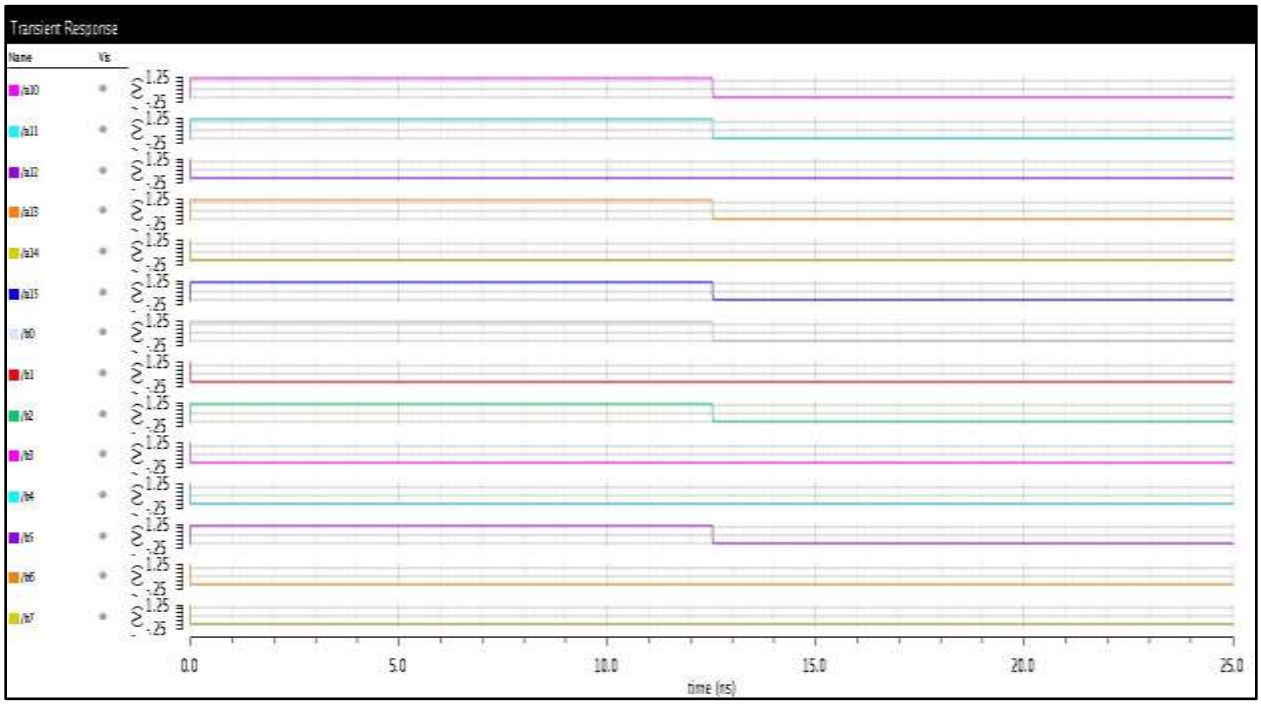

Figure 4.26: Simulation window 2 for 17 bit adder

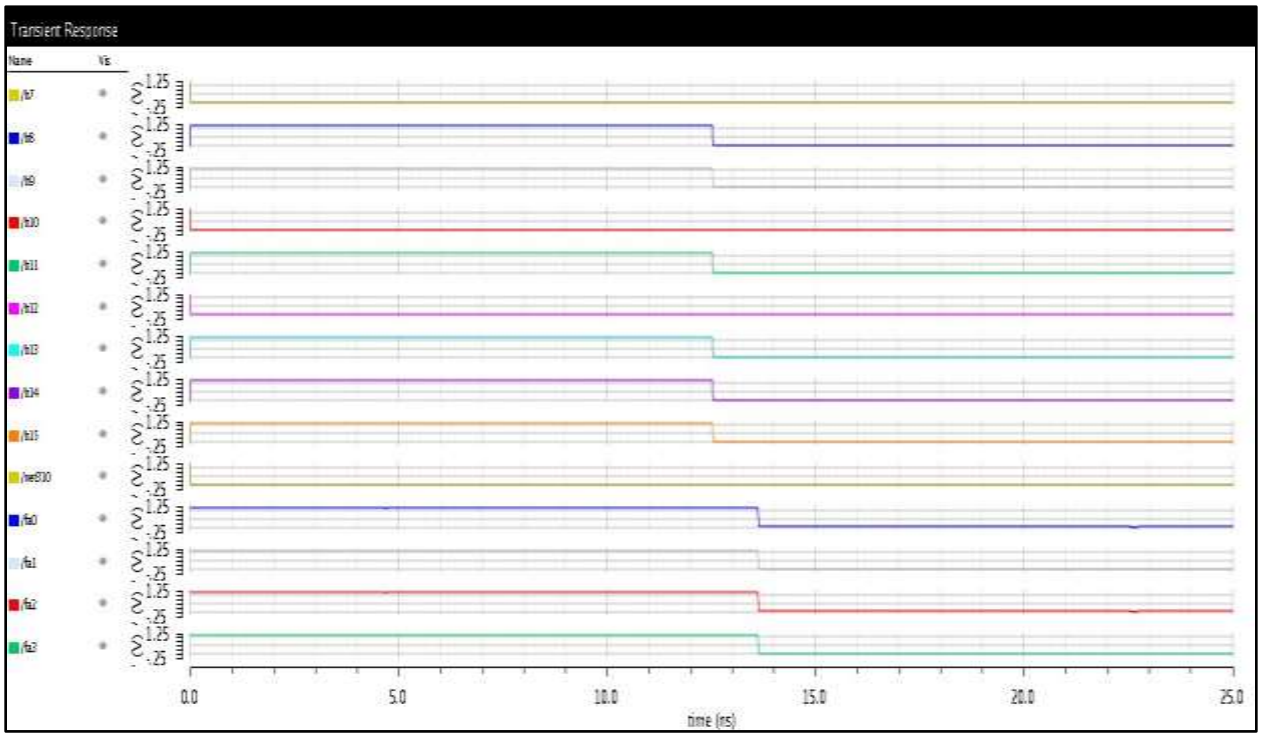

Figure 4.27: Simulation window 3 for 17 bit adder

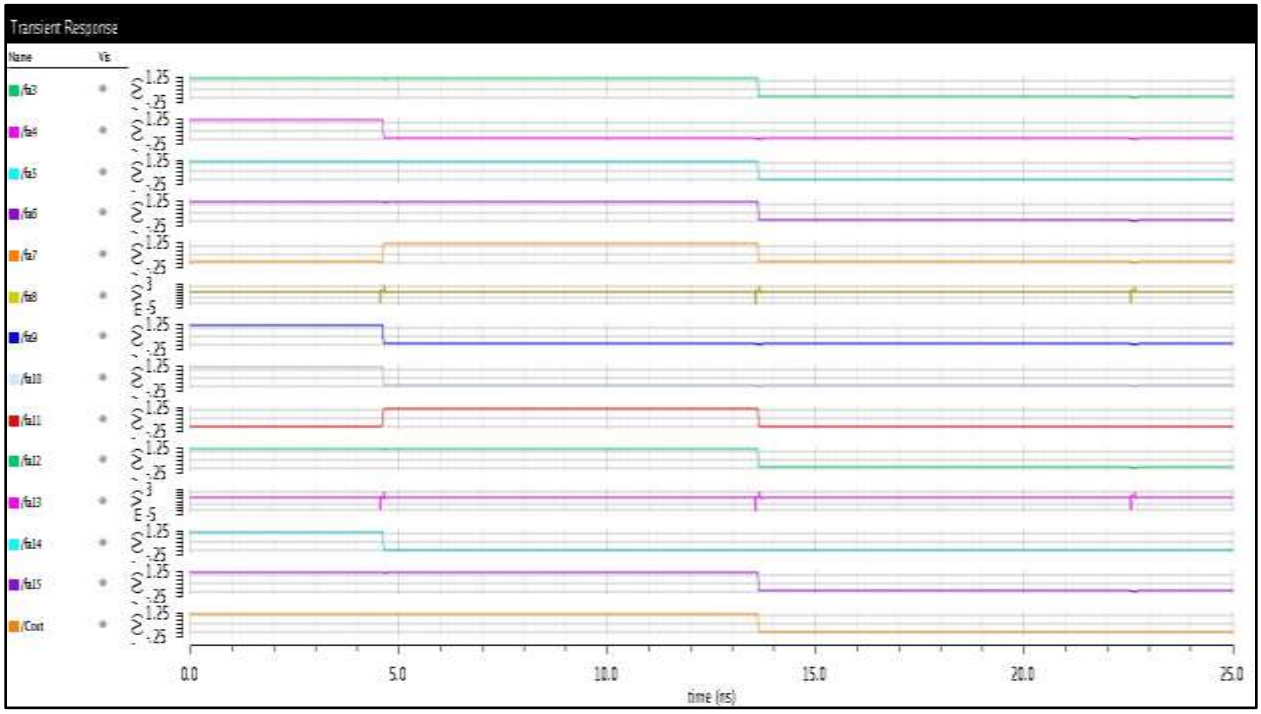

Figure 4.28: Simulation window 4 for 17 bit adder

The input to the adder is two 16 bit numbers given as 1010110111001010 and 1110101100100101 and the result is 17 bit binary number 11001100011101111 on first positive edge of the clock. Similarly the output can be validated for register block the simulation results for 17 bit register are shown below.

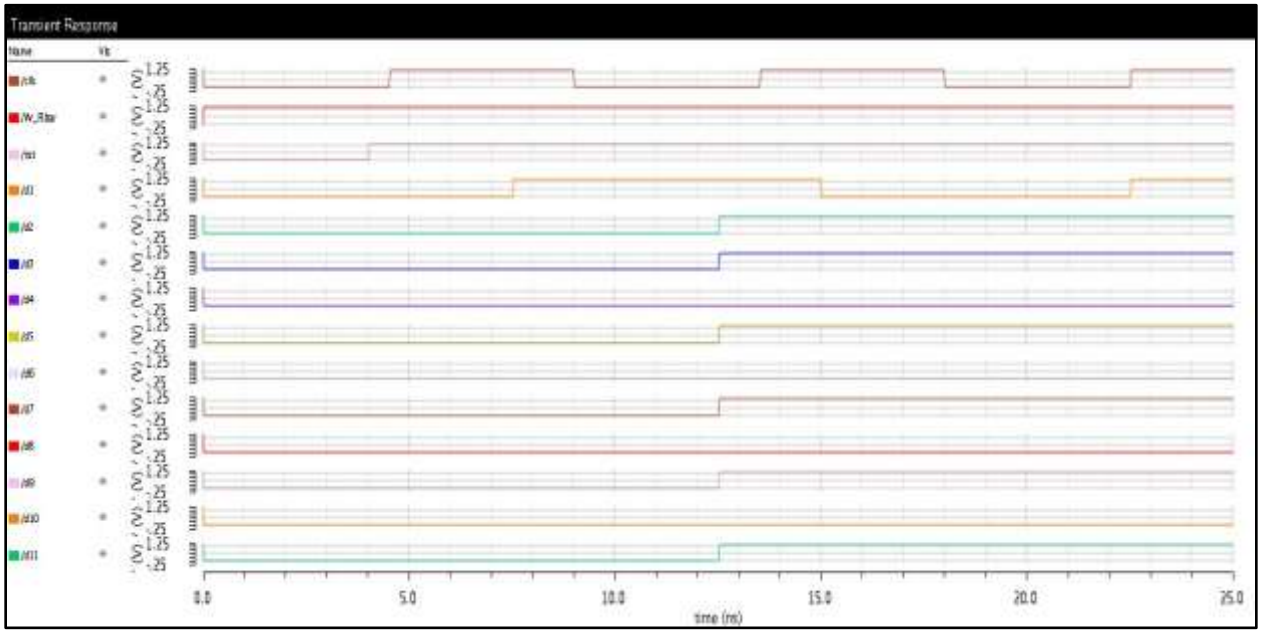

Figure 4.29: Simulation window 1 for 17 bit register

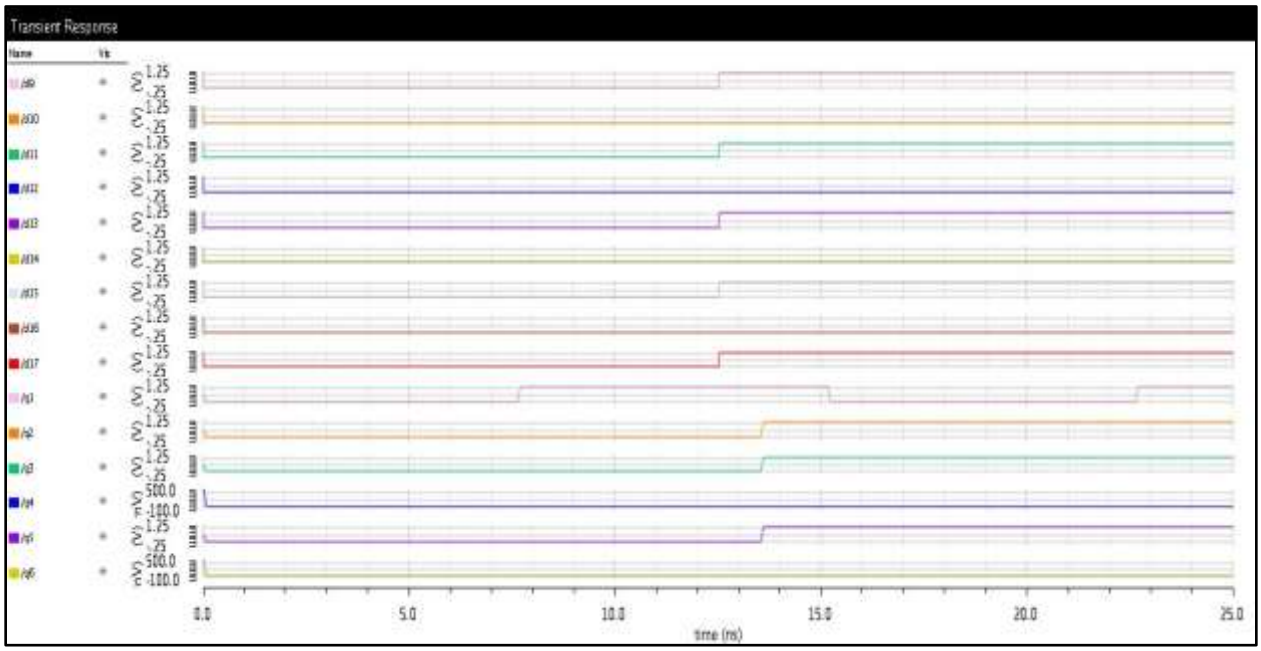

Figure 4.30: Simulation window 2 for 17 bit register

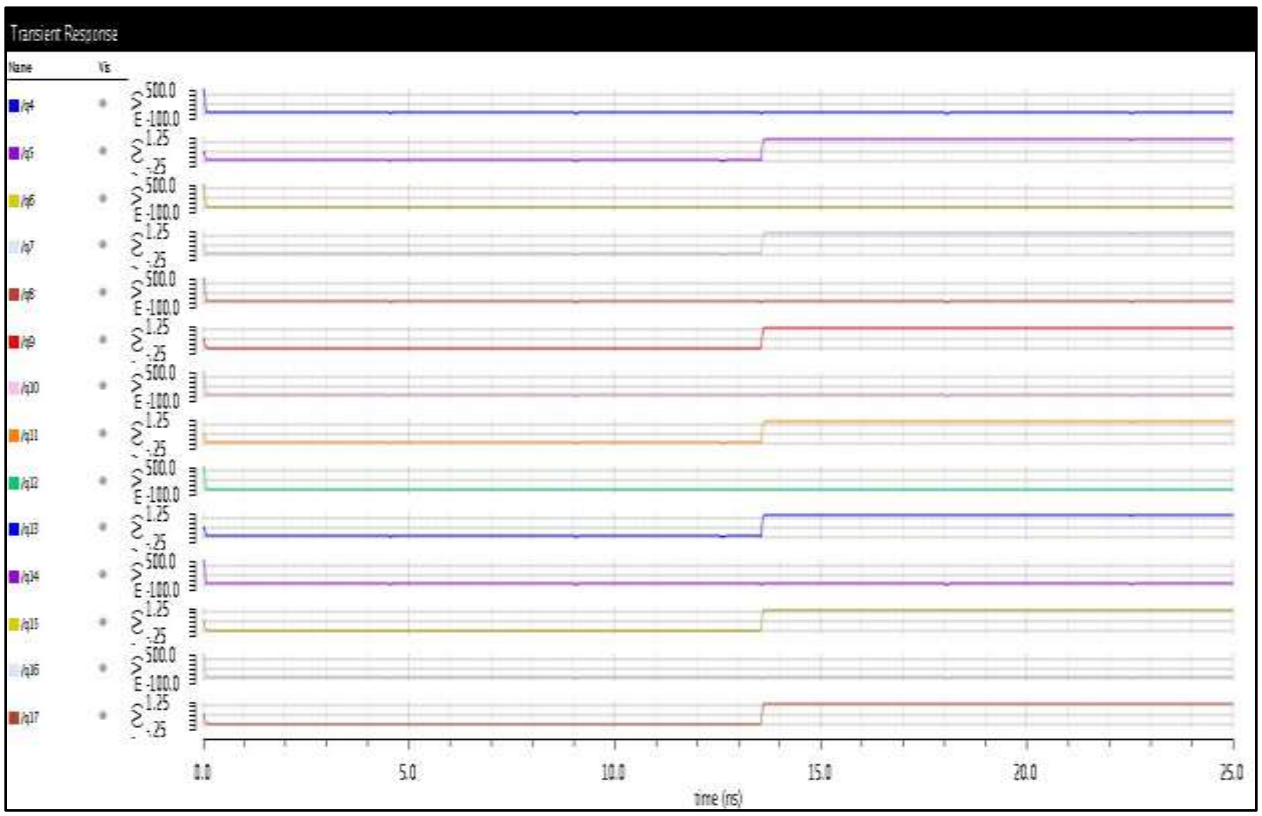

Figure 4.31: Simulation window 3 for 17 bit register

The input given to the register is 17 bit binary and the result is same 17 bit binary on the positive edges of the clock at the output port.

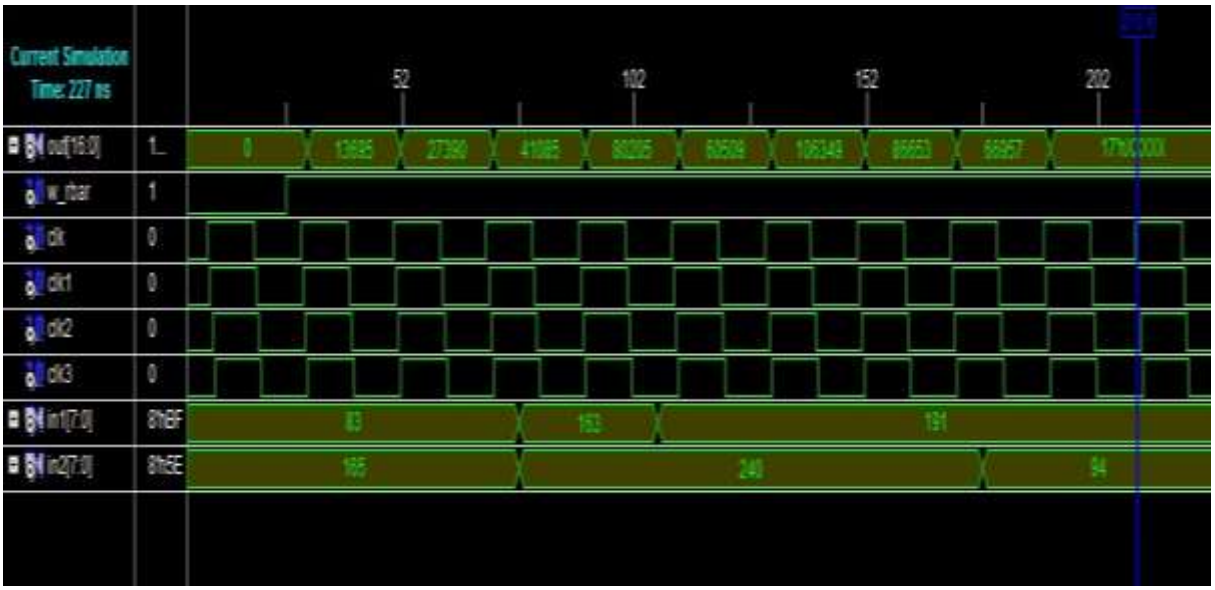

Figure 4.32: Simulation results for 8 bit MAC in NCSim

The simulation results for 8 bit MAC in Cadence NCSim are shown below. The results show that on every positive edge of clk, in1 and in2 are multiplied and the result is available on the out port after addition with the previous number on every positive edge of clk3.

The power analysis for each individual block has been performed to calculate the power, however the delay analysis could not be performed as the no. of intermediate signals were very large. The calculations are stated in the table given below.

Block	Simulation time	Supply Voltage	Power Estimated
8 bit multiplier	10ns	1.1V	147.6 µW
16 bit register	10ns	1.1V	18.03 µW
17 bit adder	10ns	1.1V	77.95 µW
16 bit register	10ns	1.1V	19.11 µW

Table 4.1: Power analysis of each block of 8 bit MAC

Also the analysis was performed for the complete MAC unit for power in both Cadence Virtuoso and the Cadence NCSim. The results obtained are shown below in the table.

Block	Simulation Time	Supply Voltage	Power Estimated
8 bit MAC in NCSim	10 ns	0.9 V	468.756 µW
8 bit MAC in Virtuoso	10 ns	0.9 V	122.1 µW
8 bit MAC in NCSim	10 ns	1.1 V	642.736 µW
8 bit MAC in Virtuoso	10 ns	1.1 V	228.3 µW

Table 4.2: Power analysis and comparison of Virtuoso and NCSim designs

As seen from the above results, the power has been reduced 2.5 times to 3.5 times in analog design as compared to the digital design. The significant reduction in power has been achieved due to the fact that the individual blocks can be modified at the lower levels of abstraction i.e. at the schematic level whereas; in digital counterpart the modifications can be done only at the

algorithmic level i.e. highest level of abstraction. Therefore, the analog design environment served as the better platform for the low power design than digital counterpart.

4.4 Conclusion

MAC, the heart of many DSP applications, must be low power and high speed to meet the consumer desires from a portable electronic device. The modifications at the higher level of abstraction i.e.at algorithmic level are not sufficient enough to meet present requirements of low power. Therefore the present research work has been focused on changing the design of MAC at lower levels of abstraction i.e. at schematic level. The results have been fascinating showing 2.5 to 3.5 times power reduction as compared to the digital design implementation. The present work has been carried out in Cadence Virtuoso 90nm technology. The handcrafted design has been synchronized with the global clock for the use of design in real time applications. Each block performs on the positive edges of the clock.

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