Design & Performance Analysis of Hybrid Adders for High Speed Arithmetic Circuit

DISSERTATION

Submitted in partial fulfillment of the requirement for the award of the Degree of

MASTER OF TECHNOLOGY
IN
Electronics & Communication Engineering

By

Rajkumar Sarma

Under the Guidance of

Veerati Raju (Asst. Prof.)

School of Electronics Engineering
Lovely Professional University
Punjab
MAY 2012

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THESIS

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CERTIFICATE

This is to certify that the Thesis titled "Design & Performance Analysis of Hybrid Adders for High Speed Arithmetic Circuit" that is being submitted by "***Rajkumar Sarma***" is in partial fulfillment of the requirements for the award of MASTER OF TECHNOLOGY DEGREE, is a record of bonafide work done under my guidance. The contents of this Thesis, in full or in parts, have neither been taken from any other source nor have been submitted to any other Institute or University for award of any degree or diploma and the same is certified.

Project Supervisor

(Name of the Organization)
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The Thesis is satisfactory / unsatisfactory

Examiner I **Examiner II**

ABSTRACT

Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as application-specific DSP architectures and microprocessors. In addition to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation, etc. So low power, lesser delay Adder cell design is of great interest for the designer. In this work two different Adder cells using Gate Diffusion Technique (GDI) & PTL-GDI technique are presented. GDI technique allows reducing power consumption, propagation delay and low PDP (power delay product) whereas Pass Transistor Logic (PTL) reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. The performance of GDI & PTL techniques, which is found to be much more power efficient in comparison with existing design technique, are presented in this work. The significance of these designs is substantiated by the simulation results obtained from Cadence Virtuoso 180nm environment. The Delay and Power Consumption is calculated using Cadence tools. The Delay, Power Consumption and PDP of the proposed designs are compared with the existing design techniques. Finally the overall performances are plotted and discussed in detail.

ACKNOWLEDGEMENT

I would never have been able to finish my dissertation without the guidance of my thesis supervisor, support from friends, and support from my family.

I would like to express my deepest gratitude to my guide, Mr. Veerati Raju (Asst. Prof), for his excellent guidance, caring, patience, and providing me with an excellent atmosphere for doing research. He taught me lot about the subject as well as about the Cadence Virtuoso tool. These words will not be sufficient to thank him for his guidance and support. I would like to thank Mr.Tummala Anil Chowdary (Asst. Prof) for his constructive opinion regarding the thesis work. I would like to express my gratitude to Mr. Rajeev Patial (COD) for advising me and encouraging me to do my thesis work in VLSI domain.

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I would also like to thank my parents & family. They were always supporting me and encouraging me with their best wishes.

Last but not the least, the one above all of us, the omnipresent God, for answering my prayers for giving me the strength to plod on despite my constitution wanting to give up and throw in the towel, thank you so much Dear Lord.

(To be signed by the student)

Reg. No. 11013091

CERTIFICATE

This is to certify that "Rajkumar Sarma" bearing Registration no. "11013091" has completed thesis titled, "Design & Performance Analysis of Hybrid Adders for High Speed Arithmetic Circuit" under my guidance and supervision. To the best of my knowledge, the present work is the result of his original investigation and study. No part of the thesis has ever been submitted for any other degree at any University.

The thesis is fit for submission and the partial fulfillment of the conditions for the award of M.Tech in ECE.

Signature and Name of the Research Supervisor

Designation

School

Lovely Professional University

Phagwara, Punjab.

Date :

DECLARATION

I, Rajkumar Sarma, student of M.Tech under Department of Electronics & Communication Engineering of Lovely Professional University, Punjab, hereby declare that all the information furnished in this thesis report is based on my own intensive research and is genuine.

This thesis does not, to the best of my knowledge, contain part of my work which has been submitted for the award of my degree either of this university or any other university without proper citation.

Date : Signature and Name of the student

Registration No. .....

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LIST OF ABBREVIATIONS

Abbreviation	Full Form
MOS	Metal Oxide Semiconductor
CMOS	complementary metal oxide semiconductor
TSMC	Taiwan Semiconductor Manufacturing Corporation
PTL	Pass Transistor Logic
GDI	Gate Diffusion Input
CPL	complementary pass-transistor logic

PUN	Pull UP Network
PDN	Pull Down Network
MUX	Multiplexer
PDP	Power Delay Product

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CHAPTER 1

Introduction

Full adders are fundamental units in various circuits, especially in circuits used for performing arithmetic operations such as compressors, comparators, parity checkers, and so on. Full adders are often in the critical paths of complex arithmetic circuits for multiplication and division. These in turn form the core of any system and thereby influence the overall performance of the entire system. Enhancing the performance of the full adder can significantly affect the system performance. As mentioned in [5], figure 1.1 shows the power consumption breakdown in a modern day high-performance microprocessor. The datapath consumes roughly 30% of the total power of the system. Adders are an extensively used component in datapaths and, therefore, careful design and analysis is required for these units to obtain optimum performance.

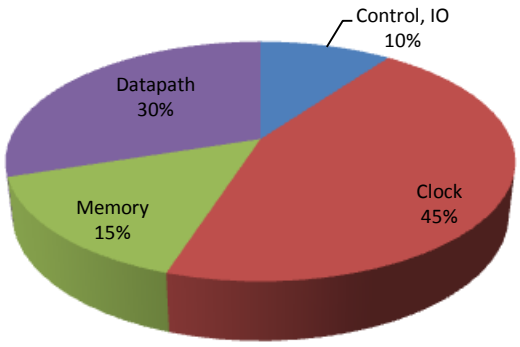


Figure 1.1: Power consumption by various units [5]

On the other hand as we can see from the Figure 1.1 clock signals are consuming 45% of the total power, which is very high in fact. As power dissipation has become one of the most important constraints in the design flow of modern processors, clock-gating and stand-by operational modes have been implemented for these systems in order to disable the transitioning activity at internal nodes of the intended low-power module. Clock-gating is a technique that reduces dynamic power dissipation by selectively stopping the clock signal to portions of the circuit that are inactive at certain periods of time, and it can be applied to different hierarchical levels. Therefore, under this common scenario, it has become extremely

important to consider the power consumption of any proposed module when there are non-transitioning input data or there is no clock signal activity.

Very often, the utmost integrated circuit performances are restricted by how best the arithmetic operators are implemented in the cell library provided to the designer for the synthesis. As the complexity of arithmetic circuits grows with increasing processor bus width, energy consumption is becoming more important now than ever due to the increase in the number and density of transistors on chip and faster clock. Different CMOS logic styles have evolved for the development of cell libraries. They are likely to perpetuate the ability to further reduce the cost-per-function and improve the performance of integrated circuits. With the lowering of threshold voltage in ultra deep submicron technology, lowering the supply voltage appears to be the most eminent means to reduce power consumption. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles. For example the goal to extend the battery life span of portable electronics is to reduce the energy expended per arithmetic operation, but low-power consumption need not necessarily implies low energy. To execute an arithmetic operation, a circuit can consume very low power by clocking at extremely low frequency but it may take a very long time to complete the operation.

1.1 Objective:

1. To analyze Delay and the Power Consumption in 0.18 µm Hybrid Adders
2. To design a reduced delay and optimized power consumption Hybrid Adder

1.2 Review of Literature:

Several low-power and high-performance 1-bit hybrid Full Adder cells have been reported in the literature. In this work five state-of-the-art hybrid Full Adder Cells, (which were reported to have better performance than others are reviewed and analyzed. The adders considered in this work were designed using conventional implementing methods, i.e. they use only transistors and no use input capacitors.

- **Monico Linares Aranda et al:(Sept 2001) [1]:** In this paper the most interesting topologies of one-bit hybrid full adders, are analyzed and compared by the author for speed, power consumption, and power-delay product. The investigation has been carried out with properly defined simulation set up and input pattern on a Mentor Graphics environment using a TSMC 180 nm CMOS process. Performance has been also compared for different supply voltage values.

- **Radhakrishnan,D:(Feb 2001) [6]:** A formal design procedure for realizing a minimal transistor CMOS pass network XOR-XNOR cell, that is fully compensated for threshold voltage drop in MOS transistors, is presented by the author. This new cell can reliably operate within certain bounds when the power supply voltage is scaled down, as long as due consideration is given to the sizing of the MOS transistors during the initial design step. It uses only six transistors for the combined XOR-XNOR cell and can operate reliably when the supply voltage is scaled down, as long as the voltage is not allowed to fall below double of threshold voltage. A low transistor count full adder cell using the new XOR-XNOR cell is also presented. The circuit diagram of Radhakrishnan Adder is shown in figure 1.2.

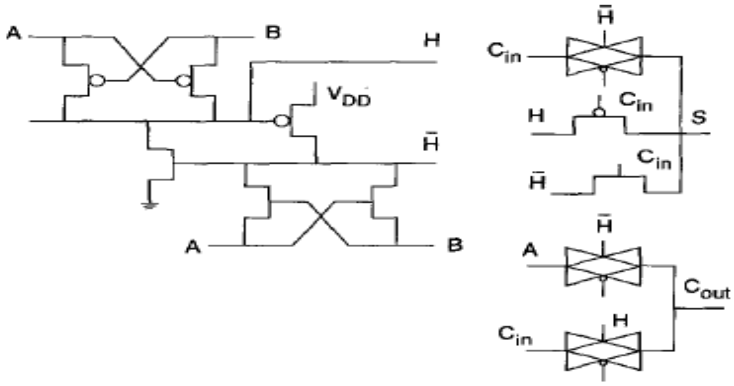


Figure 1.2: D. Radhakrishnan Adder [6]

- **C.-H. Chang, J. Gu, and M. Zhang:(june 2005) [3]:** The Chang adder has 26 transistors and it utilizes a modified low-power XOR/XNOR circuit. In this circuit worst case delay problems due logic transitions are solved by adding more transistors; however, these additional transistors increase the power consumption of the full adder cell. The circuit diagram of Chang Adder is shown in figure 1.3.

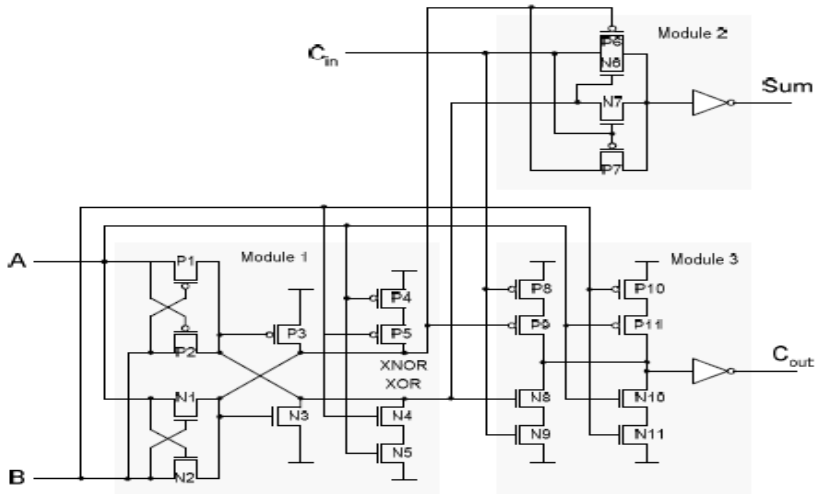


Figure 1.3: Chang adder [3]

- **M. Aguirre H., M. Linares A., and M. Salim M:.(Aug. 2005) [4]:** The Aguirre adder utilizes the Swing-Restored Complementary Pass-Transistor style and an alternative logic structure in order to obtain balanced paths which is based on the multiplexing of the Boolean functions XOR/XNOR and AND/OR, to obtain the SUM and CARRY outputs, respectively. The circuit diagram of Aguirre Adder is shown in figure 1.4.

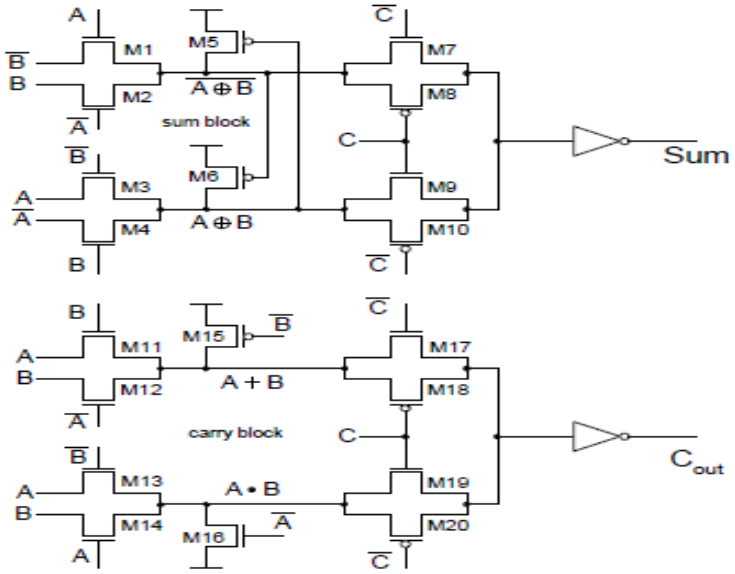


Figure 1.4: Aguirre adder [4]

- **Goel S., Kumar A. and Magdy A. Bayoumi:(Dec. 2006) [5]:** The Goel adder uses a XOR–XNOR circuit that produces balanced full-swing outputs. It has high-speed operation due to the cross-coupled PMOS Pull-up transistors providing the intermediate signals quickly and a hybrid- MOS output stage with a static inverter at the output. The circuit diagram of Goel Adder is shown in figure 1.5.

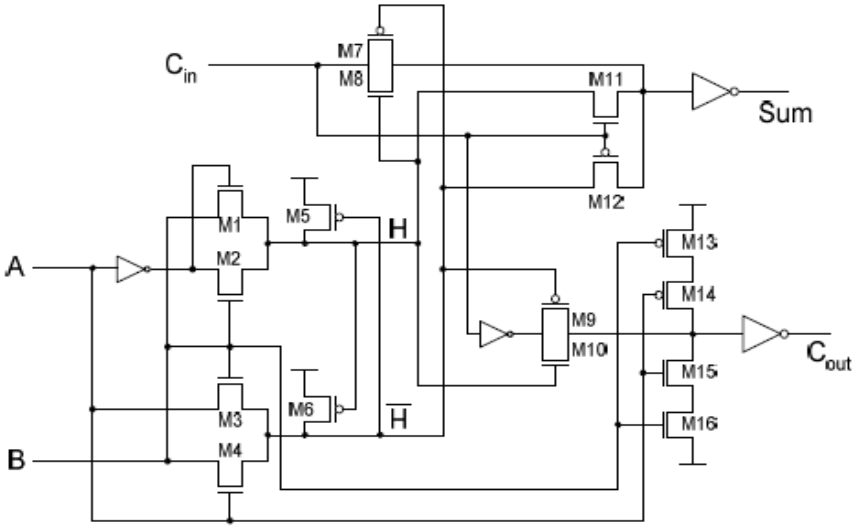


Figure 1.5: Goel adder [5]

- **Agarwal S, Pavankumar V K, Yokesh R.:(2008) [2]:** The Agarwal adder uses the CPL logic. This adder is mainly composed by NMOS transistors with pull–up PMOS transistors to obtain full swing output voltage. Due to positive feedback and use of NMOS transistors, the circuit is inherently fast. This adder has a balanced structure with respect to generation of 'SUM' and 'CARRY OUT' signals. This helps in simultaneous arrival of signals in tree structured circuits. The circuit diagram of Agarwal Adder is shown in figure 1.5.

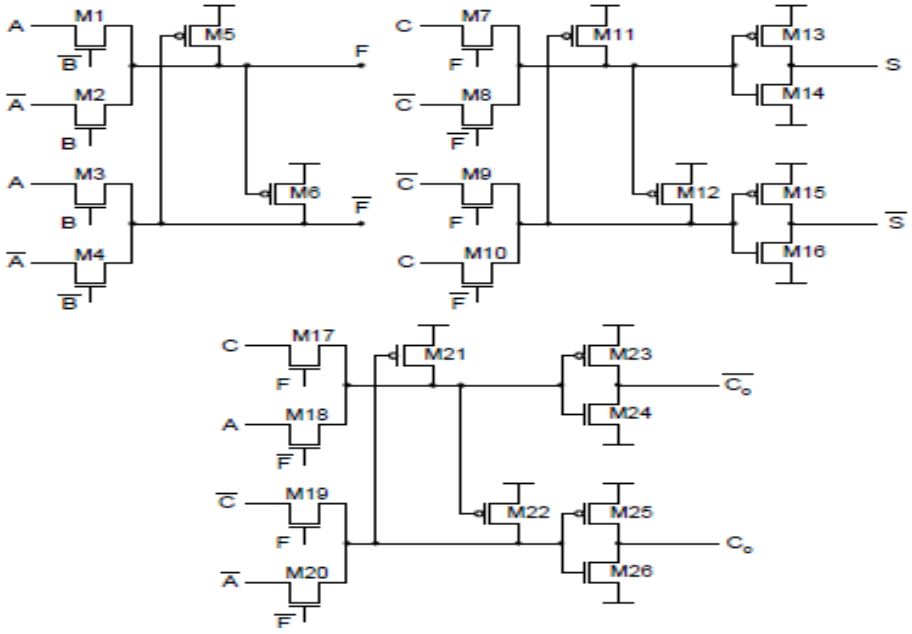


Figure 1.6: Agarwal adder [2]

- **A. Morgenshtein, A. Fish, and I. A. Wagner (2001) [10]:** GDI (Gate Diffusion Input) - a new technique of low power digital combinatorial circuit design is described. This technique allows reducing power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. A detailed design methodology is described. Performance comparison with traditional CMOS and PTL design techniques is presented. The different methods are compared with respect to the layout area, number of devices, delay and power dissipation. Several logic circuits have been implemented in various design styles. Their properties are discussed, simulation results are reported.

- **A. K. Nishad, R. Chandel (2011) [11]:** An analysis of XOR gate designed using Gate Diffusion Input (GDI) technique is presented in this work. Comparative investigations are also carried out for XOR gates designed using conventional, low power as well as GDI techniques. SPICE simulations verify the results. The analysis shows that at 100MHz, circuit designed using GDI technique consumes 73.79%, 73.61%, and 46.64% less power compared to conventional, CPL and DPL technique.

CHAPTER 2

Introduction to Several Logic styles

Several logic styles have been used in the past to design full adder cells. Each design style has its own merits and demerits. Classical designs of full adders normally use only one logic style for the whole full-adder design. One example of such design is the standard static CMOS full adder. As mentioned in [5], this full adder is based on regular CMOS structure with conventional pull-up and pull-down transistors providing full-swing output and good driving capabilities. The main drawback of static CMOS circuits is the existence of the PMOS block, because of its low mobility compared to the NMOS devices. Therefore, the PMOS devices need to be sized up to attain the desired performance. The input capacitance of a static CMOS gate is large because each input is connected to the gate of at least a PMOS and an NMOS device. This is another reason for speed degradation of static CMOS gates.

Another very popular design is Pass Transistor Logic design. As discussed in [6], when an NMOS or PMOS is used alone as an imperfect switch, we sometimes call it a Pass Transistor. PTL reduces the numbers of transistors used to make different logic gates, by eliminating excess amount of transistor. Transistors are used here as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages (Vdd).

Another conventional adder is the complementary pass-transistor logic (CPL). It provides high-speed, full-swing operation and good driving capability due to the output static inverters and the fast differential stage of cross-coupled PMOS transistors. But due to the presence of a lot of internal nodes and static inverters, there is large power dissipation. The layout of a CPL cell is also not as straightforward as a static CMOS cell due to its irregular transistor arrangement.

Transmission gate logic circuit is a special kind of pass-transistor logic circuit. It is built by connecting a PMOS transistor and a NMOS transistor in parallel, which are controlled by complementary control signals. Both the PMOS and NMOS transistors will provide the path to the input logic “1” or “0,” respectively, when they are turned on simultaneously. Thus, there is no voltage drop problem whether the 1 or the 0 is passed through it. The main disadvantage of transmission gate logic is that it requires double the number of transistors of the standard pass-transistor logic or more to implement the same circuit. Smaller transistor

count adder circuits have been proposed, most of which exploit the non full swing pass transistors with swing restored transmission gate techniques.

From the above discussion it is seen that different logic style has different merits and demerits. Moreover the main problem that is been faced by Hybrid adder circuits are power dissipation and time delay. On the other hand power dissipation and time delay somehow interrelated to each other as we have seen above. I have gone through a few hybrid adders (Aguirre Adder, Chang Adder, Goel Adder, Agarwal Adder etc.) where they have worked on power dissipation and time delay. So my focus on this paper will be on to reduce the delay as well as to optimize the power dissipation.

2.1. Switch Models for CMOS Transistors

CMOS technology employs two types of transistor: n-channel and p-channel. The two differ in the characteristics of the semiconductor materials used in their implementation and in the mechanism governing the conduction of a current through them. Most important to us, however, is the difference in behavior of the two types of transistor. We will model this behavior using switches controlled by voltages corresponding to logic 0 and logic 1. Such a model ignores complex electronic devices and captures only logical behavior.

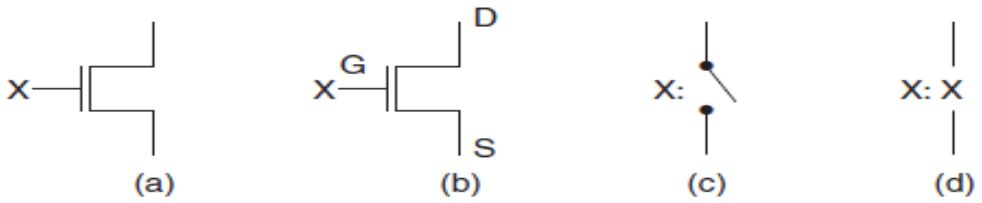


Figure 2.1: n-channel transistor

The symbol for an n-channel transistor is shown in Figure 2.1(a). The transistor has three terminals: the gate (G), the source (S), and the drain (D), as shown in Figure 2.1(b). The voltage applied between G and S determines whether a path for current to flow exists between D and S. If a path exists, we say that the transistor is ON, and if a path does not exist, we say that the transistor is OFF. The n-channel transistor is ON if the applied gate-to-source voltage is H and OFF if the applied voltage is L. Here we will make the usual assumption that a 1 represents the H voltage range and a 0 represents the L voltage range. The notion of whether a path for current to flow exists is easily modeled by a switch, as shown in Figure 2.1(c). The switch consists of two fixed terminals corresponding to the S and D terminals of the transistor. In addition, there is a movable contact that, depending on its position, determines whether the

switch is open or closed. The position of the contact is controlled by the voltage applied to the gate terminal G. Since we are looking at logic behavior, this control voltage is represented on the symbol by the input variable X on the gate terminal. For an n-channel transistor, the contact is open (no path exists) for the input variable X equal to 0 and closed (a path exists) for the input variable X equal to 1. Such a contact is traditionally referred to as being normally open, that is, open without a positive voltage applied to activate or close it. Figure 2.1(d) shows a shorthand notation for the n-channel switch model with the variable X applied. This notation represents the fact that a path between S and D exists for X equal to 1 and does not exist for X equal to 0.

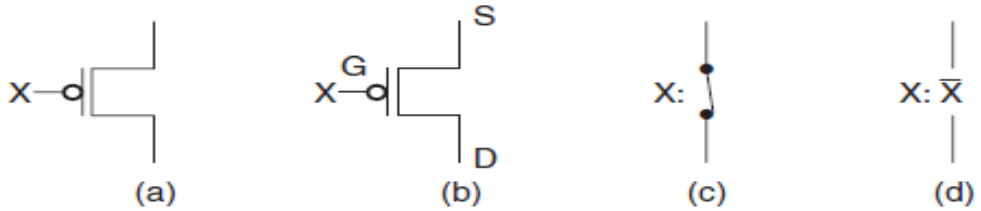


Figure 2.2: p-channel transistor

The symbol for a p-channel transistor is shown in Figure 2.2(a). In Figure 22.(b), the positions of the source S and drain D are seen to be interchanged relative to their positions in the n-channel transistor. The voltage applied between the gate G and the source S determines whether a path exists between the drain and source.

Note in Figure 2(a) that the negation indicator or bubble appears as a part of the symbol. This is because, in contrast to the behavior of an n-channel transistor, a path exists between S and D in the p-channel transistor for input variable X equal to 0 (at value L) and does not exist for input variable X equal to 1 (at value H). This behavior is represented by the model in Figure 2.2(c), which has a normally closed contact through which a path exists for X equal to 0. No path exists through the contact for X equal to 1. In addition, the shorthand notation of the p-channel switch model with variable X applied is given in Figure 2.2(d). Since a 0 on input X causes a path to exist through the switch and a 1 on X produces no path, the literal shown on the switch is X' instead of X.

2.2 Complementary CMOS

A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN). The Figure shows a generic N input logic gate where all inputs are distributed to both the pull-up and pull-down networks. The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output

to VSS when the output of the logic gate is meant to be 0. The PUN and PDN networks are constructed in a mutually exclusive fashion such that one and only one of the networks is conducting in steady state. In this way, once the transients have settled, a path always exists between VDD and the output F, realizing a high output ("one"), or, alternatively, between VSS and F for a low output ("zero"). This is equivalent to stating that the output node is always a low-impedance node in steady state.

In constructing the PDN and PUN networks, the following observations should be kept in mind:

- A transistor can be thought of as a switch controlled by its gate signal. An NMOS switch is on when the controlling signal is high and is off when the controlling signal is low. A PMOS transistor acts as an inverse switch that is on when the controlling signal is low and off when the controlling signal is high.

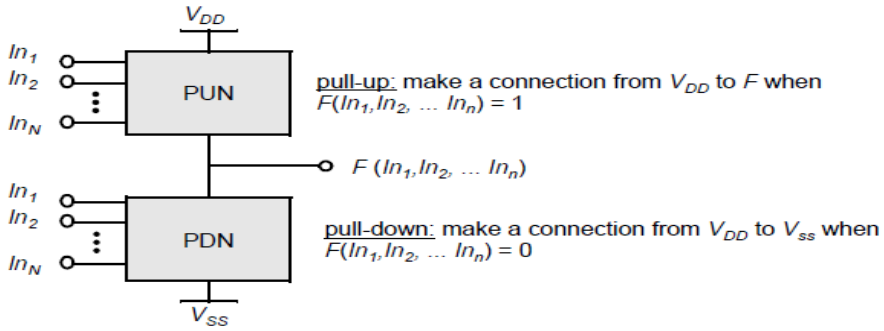


Figure 2.3: Pull-up connection & Pull-down connection

- The PDN is constructed using NMOS devices, while PMOS transistors are used in the PUN. The primary reason for this choice is that NMOS transistors produce "strong zeros," and PMOS devices generate "strong ones". To illustrate this, consider the examples shown in Figure 2.4. In Figure 2.4(a), the output capacitance is initially charged to VDD. Two possible discharge scenarios are shown. An NMOS device pulls the output all the way down to GND, while a PMOS lowers the output no further than |VTp| — the PMOS turns off at that point, and stops contributing discharge current. NMOS transistors are hence the preferred devices in the PDN. Similarly, two alternative approaches to charging up a capacitor are shown in Figure 2.4(b), with the output load initially at GND. A PMOS switch succeeds in charging the output all the way to VDD, while the NMOS device fails to raise the output above VDD-VTn. This explains why PMOS transistors are preferentially used in a PUN.

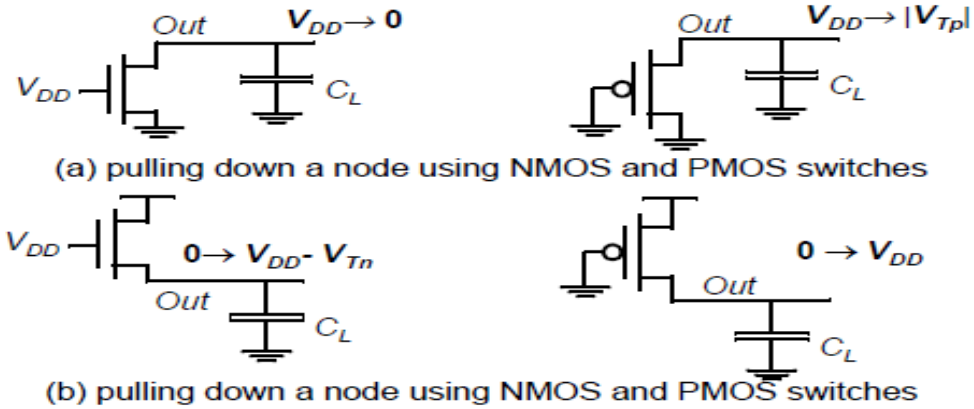


Figure 2.4: NMOS & PMOS as pull-up & pull-down transistor

- A set of construction rules can be derived to construct logic functions (Figure 2.5). NMOS devices connected in series corresponds to an AND function. With all the inputs high, the series combination conducts and the value at one end of the chain is transferred to the other end. Similarly, NMOS transistors connected in parallel represent an OR function. A conducting path exists between the output and input terminal if at least one of the input is high. Using similar arguments, construction rules for PMOS networks can be formulated. A series connection of PMOS conducts if both inputs are low, representing a NOR function (A.B = A+B), while PMOS transistors in parallel implement a NAND (A+B = A·B.

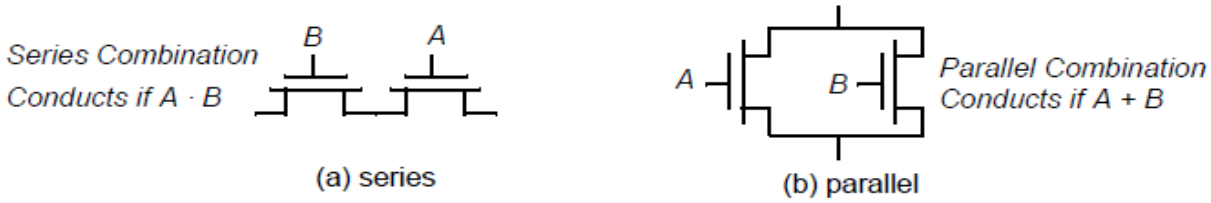


Figure 2.5: Series & Parallel Combination

- Using De Morgan's theorems ((A + B) = A·B and A·B = A + B), it can be shown that the pull-up and pull-down networks of a complementary CMOS structure are dual networks. This means that a parallel connection of transistors in the pull-up network corresponds to a series connection of the corresponding devices in the pull-down network, and vice versa. Therefore, to construct a CMOS gate, one of the networks (e.g., PDN) is implemented using combinations of series and parallel devices. The other network (i.e., PUN) is obtained using duality principle by walking the hierarchy, replacing series subnets with parallel subnets, and parallel subnets with series subnets. The complete CMOS gate is constructed by combining the PDN with the PUN.

2.3 Pass Transistor

A pass transistor is an NMOS (PMOS) transistor with the signal input fed to the source and the signal output taken from drain. A pass network is an interconnection of a number of pass transistors to achieve a particular switching function. In the case of an NMOS transistor, logic '1' at the gate passes the input from source to drain and logic '0' opens the source to drain path. A PMOS transistor exhibits similar behavior with a control signal of logic level 0. If signals X(x) and Y are connected to the gate and source of an NMOS (PMOS) transistor, respectively, then it is denoted as X(Y) and read as 'X passing Y. When both an NMOS and a PMOS transistor are connected in parallel to pass the signal Y, the circuit is referred to as a CMOS transmission gate. As shown in [6] the logic symbols and the pass logic expressions for the above three types of pass gates are shown in figure 2.6.

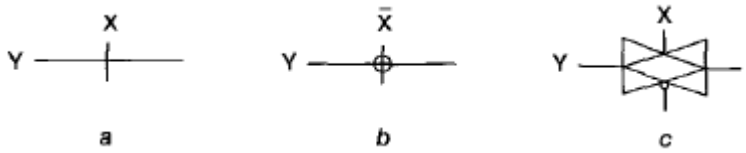


Figure 2.6: pass transistors symbols

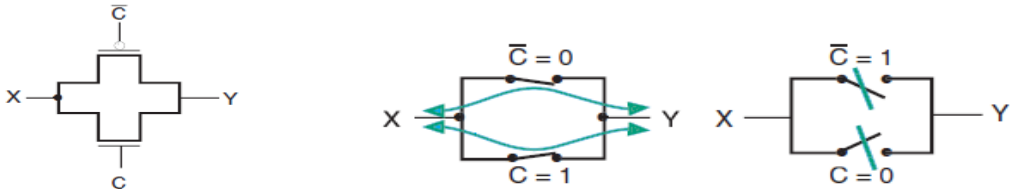
a. NMOS transistor X(Y)

b. PMOS transistor X(Y)

c. Transmission gate X(Y)

2.4 Transmission Gate Logic

Besides primitive and complex gates, there is one additional transistor circuit frequently used in CMOS logic. This circuit is the transmission gate (TG). It has its own symbol and is often included in gate-level logic circuit diagrams. A transmission gate is used as an electronic switch for making a connection between two points in a circuit. It consists of an n-channel transistor and a p-channel transistor in parallel, as shown in Figure 2.7(a). The two types of transistor are used because the p-channel transistor passes 1 (H) well and the n-channel transistor passes 0 (L) well. Figure 2.7(b) is the switch model for the transmission gate.



a b

Figure 2.7: Transmission gate and Switching model structure

2.5 GDI (Gate Diffusion Input)

GDI method is based on the use of a simple cell as shown in Figure 2.8**.** At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences: **(1)** GDI cell contains **3** inputs - G (common gate input of nMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of nMOS). **(2)** Bulks of both nMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard p-well CMOS process, but can be successfully implemented in twin-well CMOS or SO1 technologies.

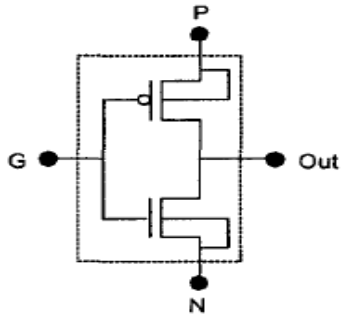


Figure 2.8: Basic GDI cell

Table 2.1 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions as discussed in [10]. Most of these functions are complex (6- 12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only 2 transistors per function) in GDI design method.

N	P	G	Out	Function
'0'	B	A	$\bar{A}$B	F1
B	'1'	A	$\bar{A}$+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}$B+AC	MUX

Table 2.1: Various logic functions of GDI cell for different input configurations

CHAPTER 3

Full-Adder Categorization

Hybrid-CMOS full-adder cells can be broadly classified into three categories depending upon their structure and logical expression of the Sum output. The SUM and CARRY (Cout) outputs of a 1-b full adder generated from the binary inputs A,B, and Cin can be generally expressed as

SUM = (A XOR B XOR Cin)

CARRY= A.B + Cin.(A XOR B)

These outputs can be expressed in many different logic expressions and, thereby, determine the structure of the circuit. Based upon these different logic expressions, many full-adder cells can be conceived. Moreover, the availability of different modules, as discussed earlier, provides the designer with more choices for a 1-b adder implementation. We classify the different possible structures for full adders into three broad categories.

These are as follows.

3.1 XOR-XOR based Full Adder:

Here two XOR cells are used for sum and 2:1 MUX is used for carry calculation. As it can be observed from figure 3.1, in module 1, 2 input XOR gate is used where A & B are the inputs and H is the output. In module 2, again 2 input XOR gate is used where H & Cin are the inputs and SUM is the output. In the case of CARRY, Cin and A are taken as two inputs of 2:1 MUX and the select line is taken as the output of module 1 i.e. H.

SUM = (A XOR B XOR Cin) = (H XOR Cin)

CARRY= A.H' + H.Cin

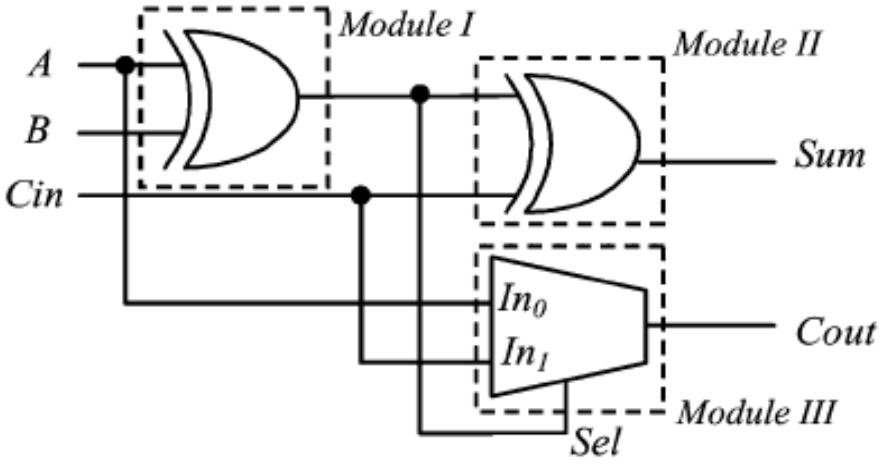


Figure 3.1: XOR-XOR based full adder

3.2 XNOR-XNOR based Full Adder:

Here two XNOR cells are used for sum and 2:1 MUX is used for carry calculation. As shown in figure 3.2, two XNOR cell and one 2:1 MUX is used for this operation. In module 1, 2 input XNOR gate is used where A & B are the inputs and H is the output. In module 2, again 2 input XOR gate is used where H & Cin are the inputs and SUM is the output. In the case of CARRY, Cin and A are taken as two inputs of 2:1 MUX and the select line is taken as the output of module 1 i.e. H.

SUM= ((A XOR B)' XOR Cin)' = (H' XOR Cin)'

CARRY= A.H' + H.Cin

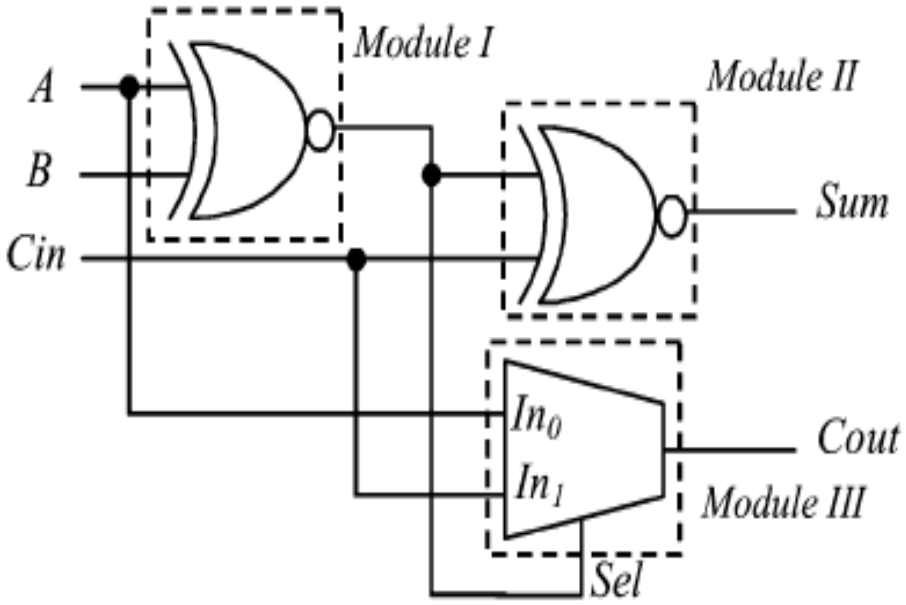


Figure 3.2: XNOR-XNOR based full adder

3.3 Centralized Full Adder:

Here one XOR, one XNOR and one 2:1 MUX is used for sum and a separate 2:1 MUX is used for carry calculation. Here in module 1, one XOR cell & one XNOR cell is used where the inputs are A & B and the select line is Cin. The outputs of both the cells are given as input to the module 2. The output of module 2 is SUM. In the case of CARRY, A & H are used as inputs of Module 3 and Cin is used as the select line. The overall circuit diagram is shown in the figure 3.3.

SUM = (H XOR Cin) = H.Cin' + H'.Cin

CARRY= A.H'+ Cin.H

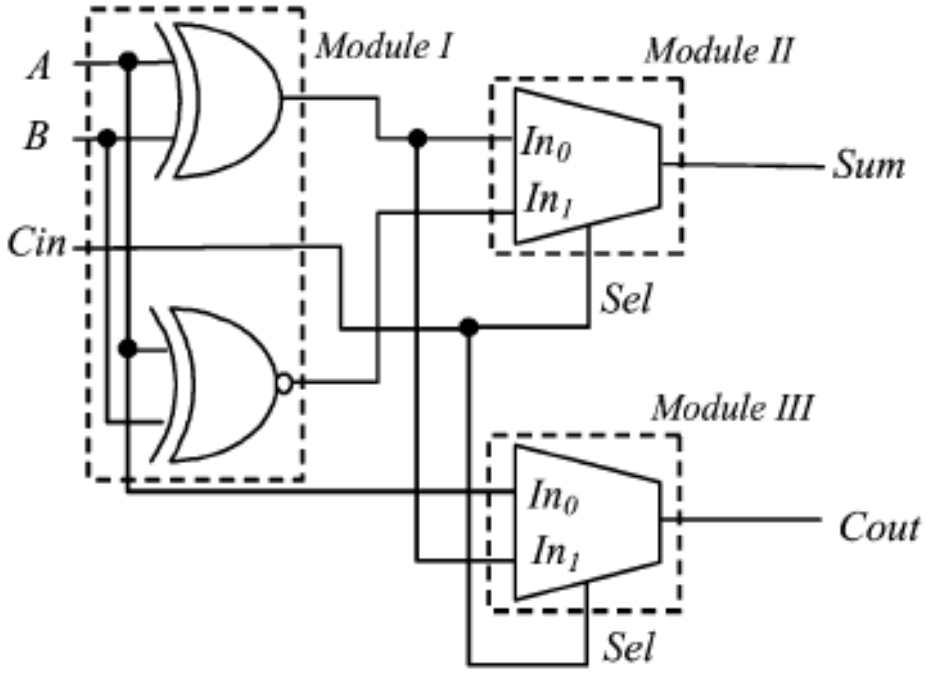


Figure 3.3: Centralized full adder

CHAPTER 4

4.1 Tools for Data Collection & Simulation

4.1.1 Introduction to Cadence Virtuoso:

Designed to help users create manufacturing-robust designs, Cadence® Virtuoso® Analog Design Environment is the advanced design and simulation environment for the Virtuoso platform. It gives designers access to a new parasitic estimation and comparison flow and optimization algorithms that help to center designs better for yield improvement and advanced matching and sensitivity analyses. By supporting extensive exploration of multiple designs against their objective specifications, Virtuoso Analog Design Environment sets the standard in fast and accurate design verification.

4.1.2 Features/Benefits of Virtuoso:

- Reduced learning curve with a simulator-independent environment
- Maximum efficiency in the script-driven mode
- Accelerated debug process using a variety of built-in analog analysis tools
- Facilitated design correction via easy comparison of pre- and post-parasitic extracted designs
- Quick detection of circuit problems via a clear visualization cockpit

4.1.3 Simulation Environment

All the adders are designed and simulated in Cadence Virtuoso 180nm technology. Their performances are measured in different supply voltages such as 3V, 1.8V and 0.8V at 100MHz. The delay was measured from 50% of the input voltage swing to 50% of the output voltage swing. Mainly three parameters are compared in this analysis; they are Delay, Power Consumption and Power Delay Product (PDP).

In order to have a fair comparison, all the simulated circuits are prototyped at optimum transistor sizing. The transistor sizes of all the simulated circuits have been included in the figures. In the circuits, the numbers depict the width (W) of the transistors with the minimum feature size as 2µm.

4.1.4 Implementation of XOR gate using NOR & NAND

Implementation of XOR gate using NOR & NAND are the very basic fundamental designs. Complementary CMOS logic is been used here. Firstly the inverter symbol is been

designed and the same design is been used for XOR gate implementation. Figure 4.1 shows the schematic diagram of the XOR gate using NOR and Figure 4.2 shows the schematic diagram of the XOR gate using NAND. Figure 4.3(a) & (b) shows the input-output waveforms using NOR & NAND respectively. XOR implementation using NOR & NAND gate can done by simplifying the XOR Boolean equation.

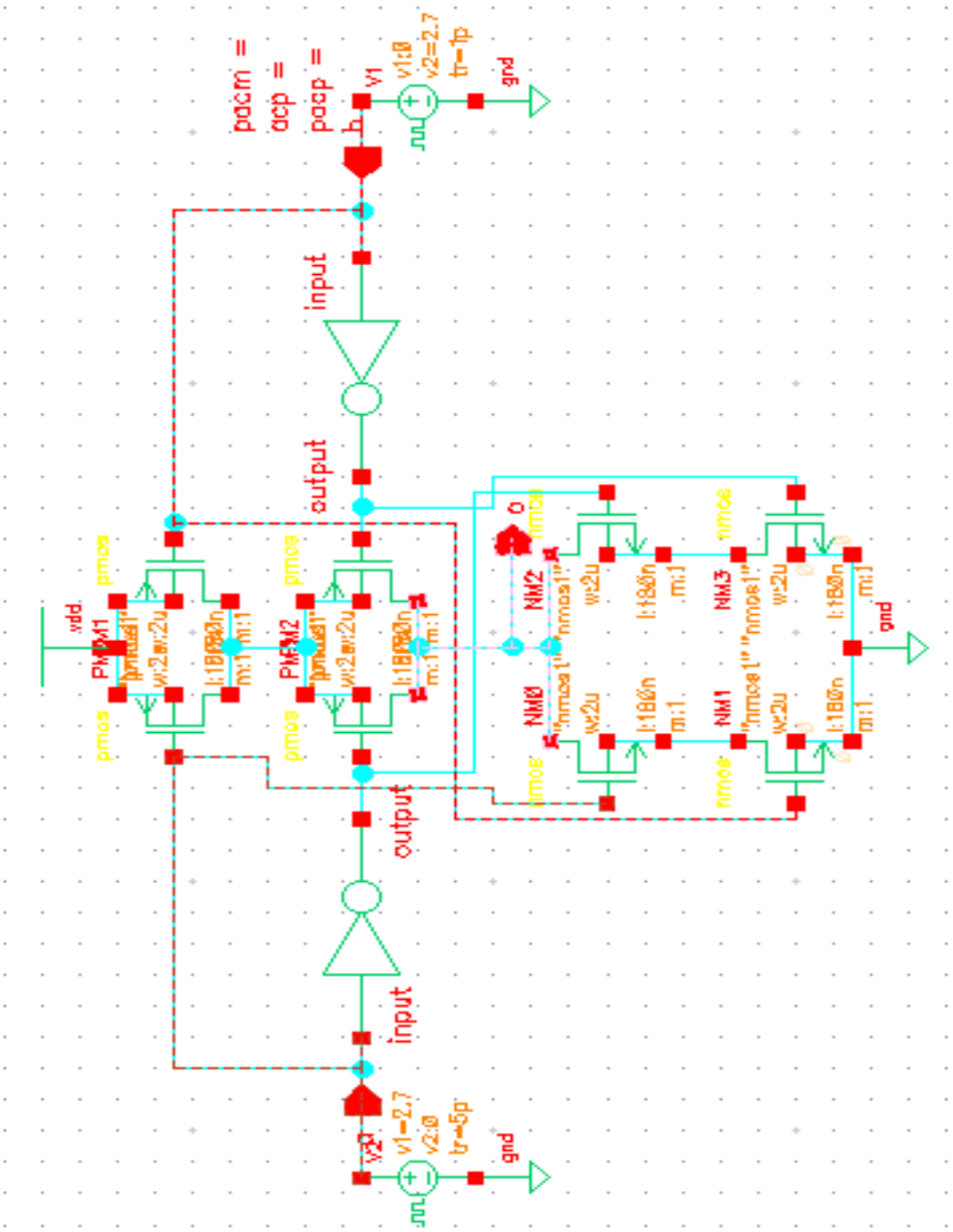


Figure 4.1: Schematic diagram of XOR gate using NOR

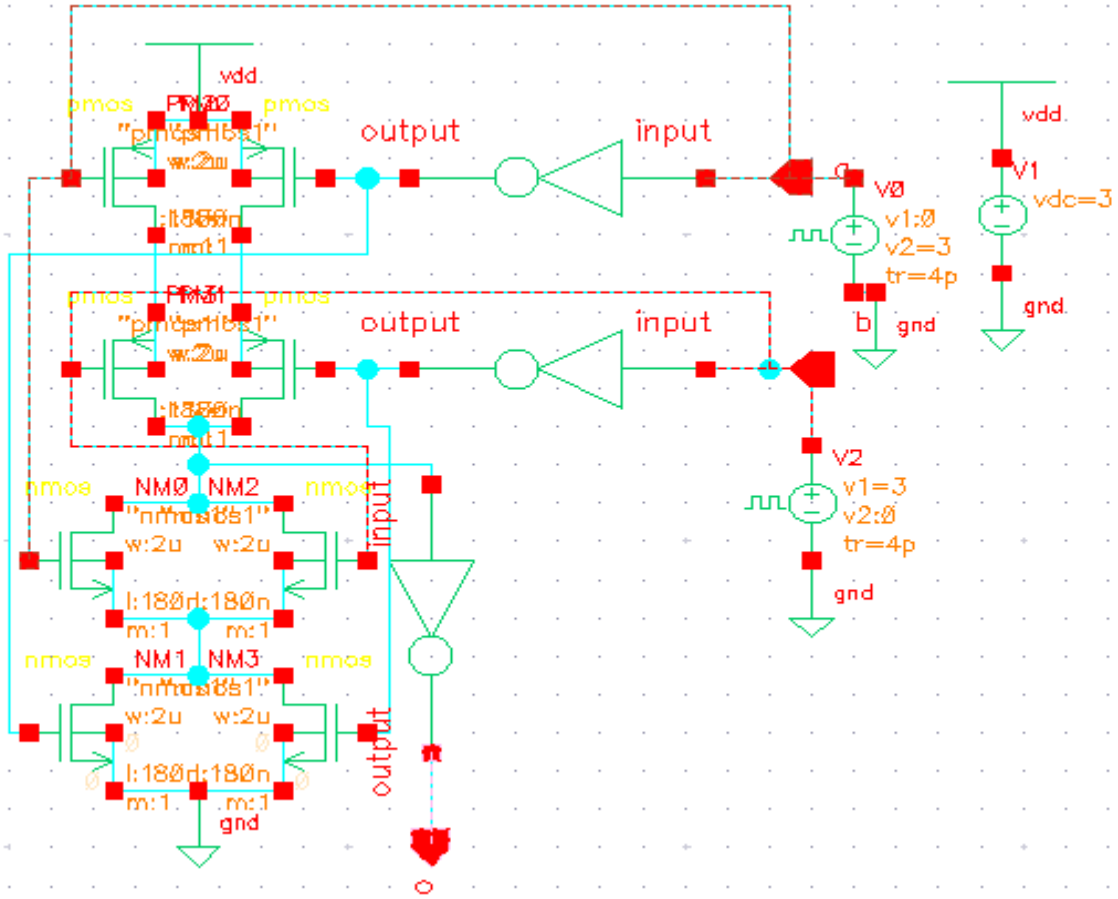
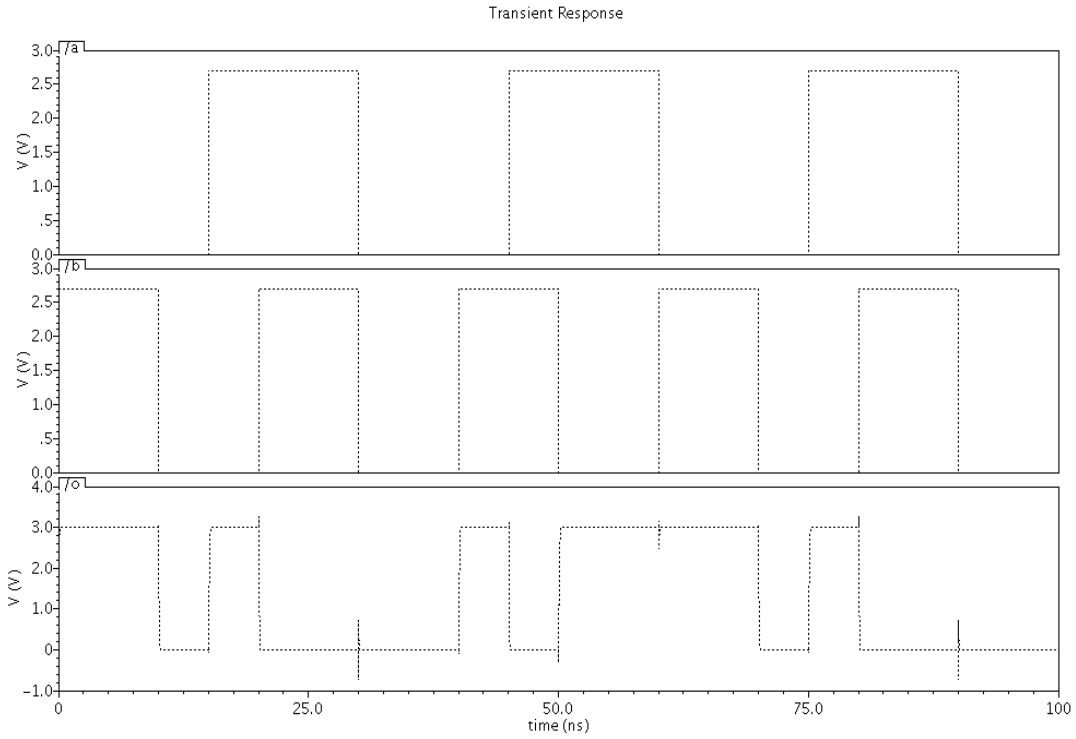
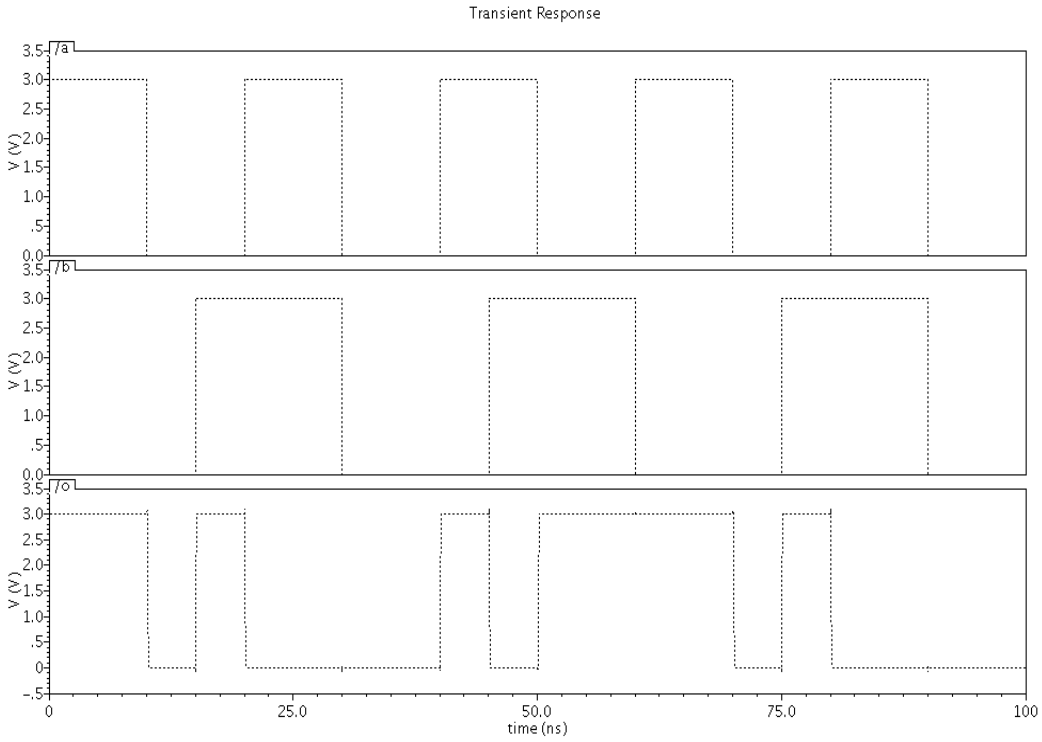


Figure 4.2: Schematic diagram of XOR gate using NAND



(a)



(b)

Figure 4.3(a) & (b): The input-output waveforms XOR using NOR & NAND respectively

4.1.5 Implementation of D. Radhakrishnan Adder:

The Radhakrishnan Adder is been implemented [6] using Pass Transistor logic. The total number of transistors used is 14. Pull-up and Pull-down networks are used to provide strong 0 and strong 1. This circuits promises to provide a full-swing output voltage but if we reduce the supply voltage below 1 V the performance degrades significantly. However the delay is found to be 19.03 ps at 3 V supply voltage. The implemented circuit & output waveforms are shown in figure 4.4 & figure 4.5 respectively.

4.1.6 Implementation of Goel Adder:

Unlike Radhakrishnan Adder instead of using three PMOS and three NMOS, as mentioned in [5], in Goel Adder four NMOS transistors are used and two pull-up PMOS transistors are used. Due to the presence of more charge carrier in NMOS transistor this is faster than Radhakrishnan Adder. But as the number of transistor count increases the delay also increases at the final output. The number of transistor used here is 22 and the delay is found to be 55.68ps at 3V supply voltage. The implemented circuit & output waveforms are shown in figure 4.6 & figure 4.7 respectively.

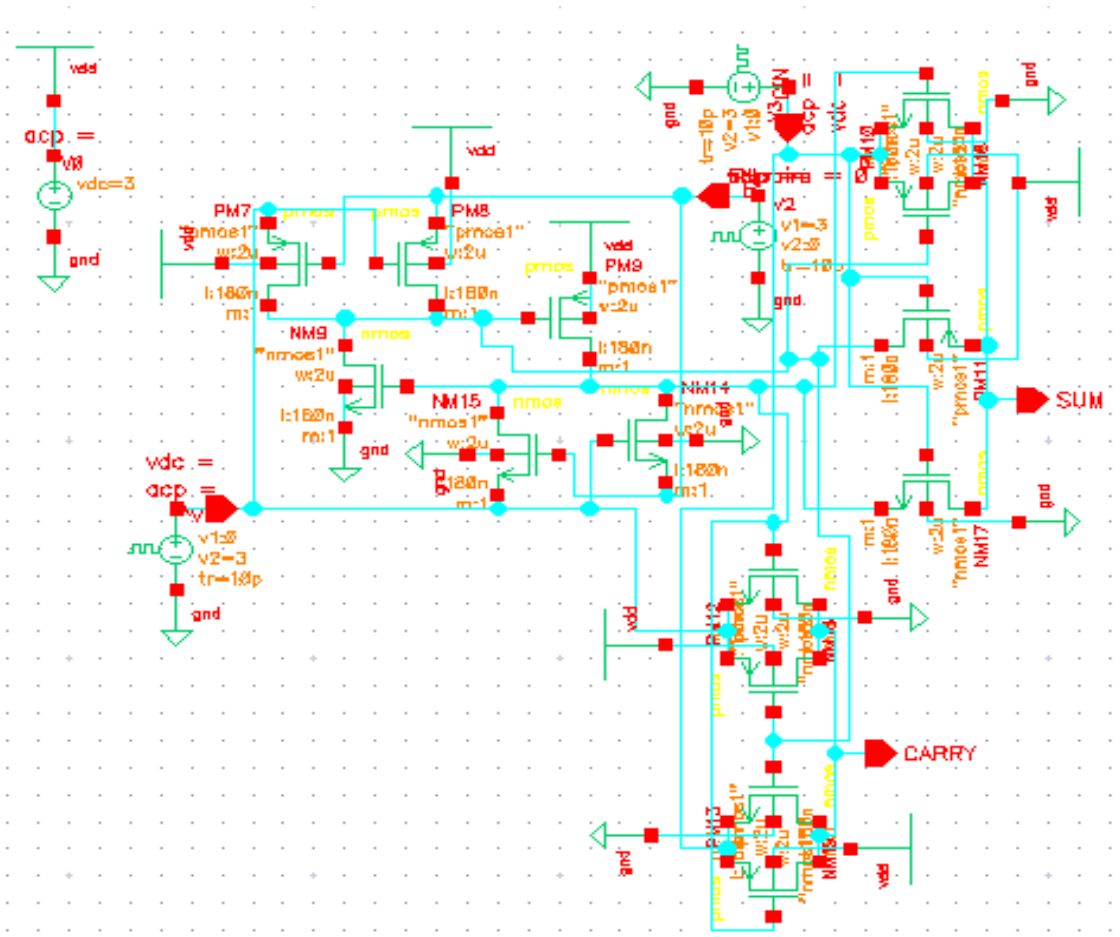


Figure 4.4: Implementation of D. Radhakrishnan Adder

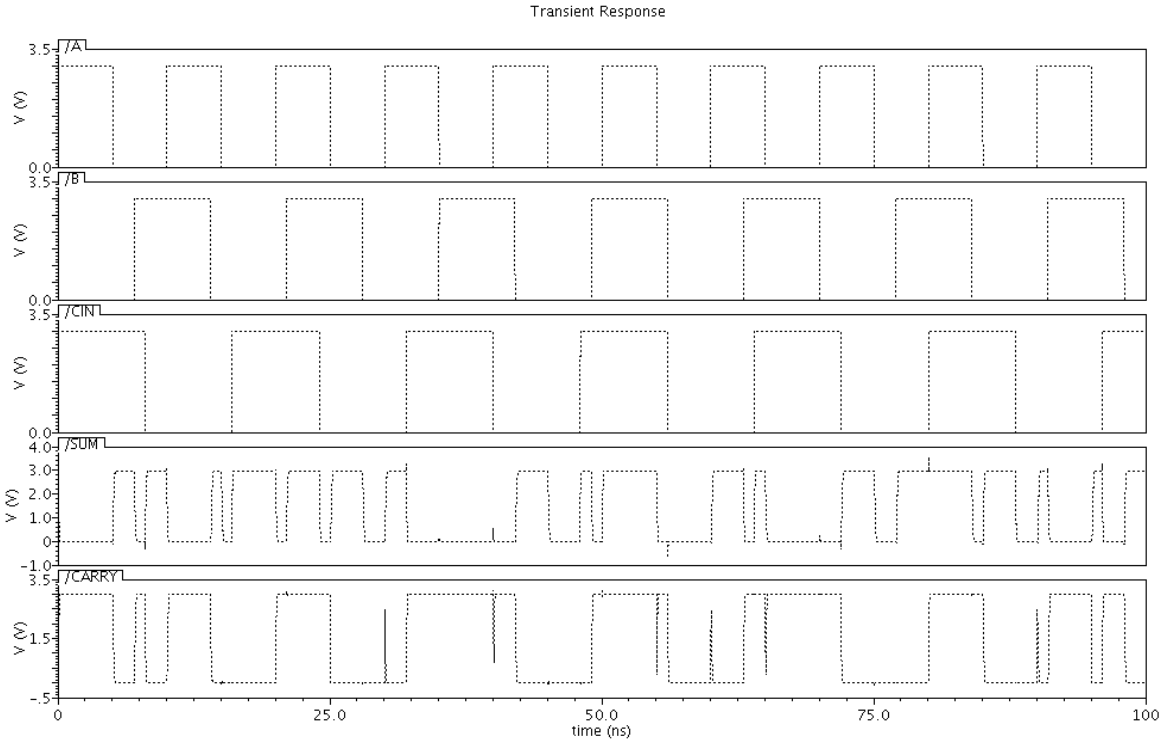


Figure 4.5: Radhakrishnan Adder output curve

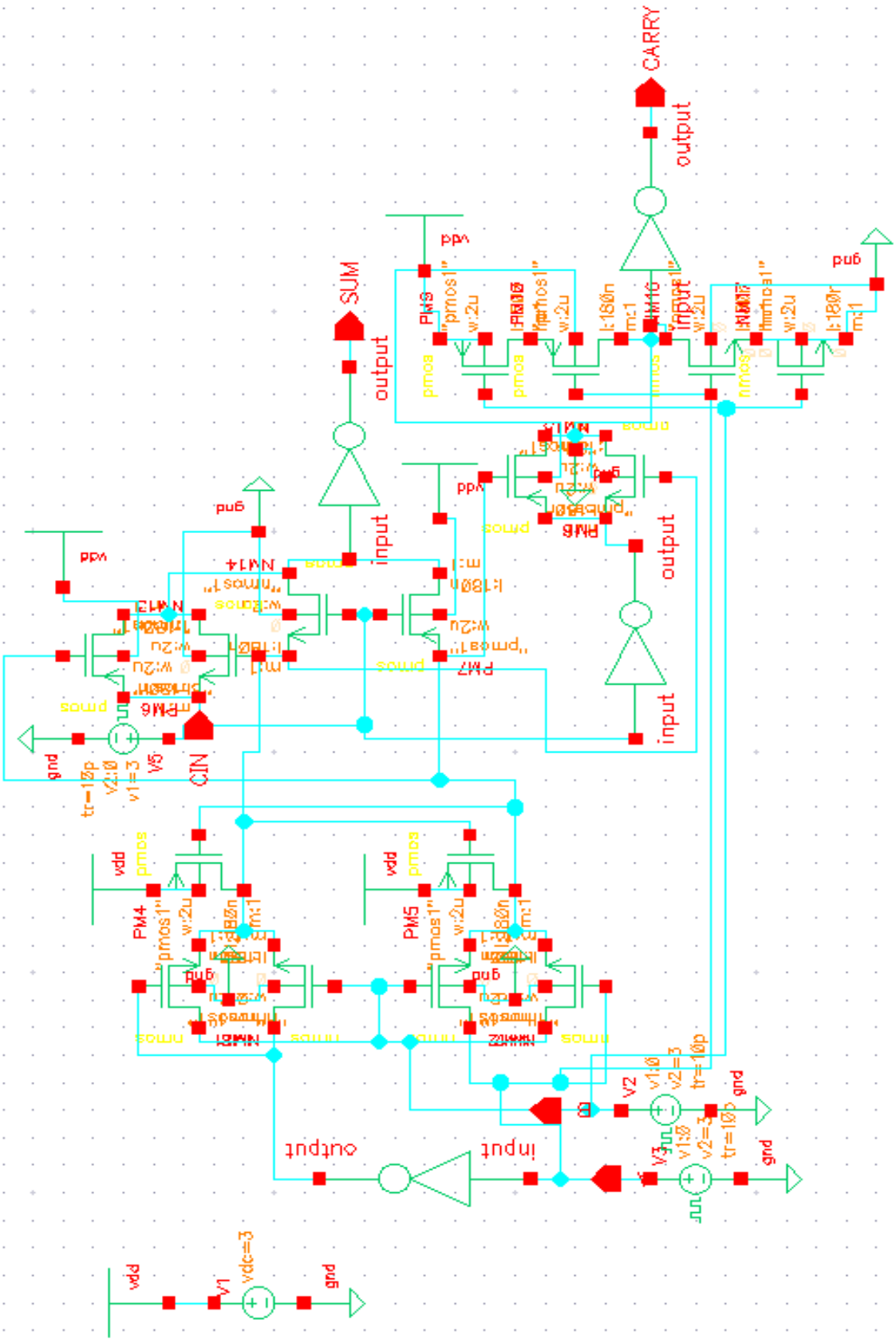


Figure 4.6: Goel Adder implementation

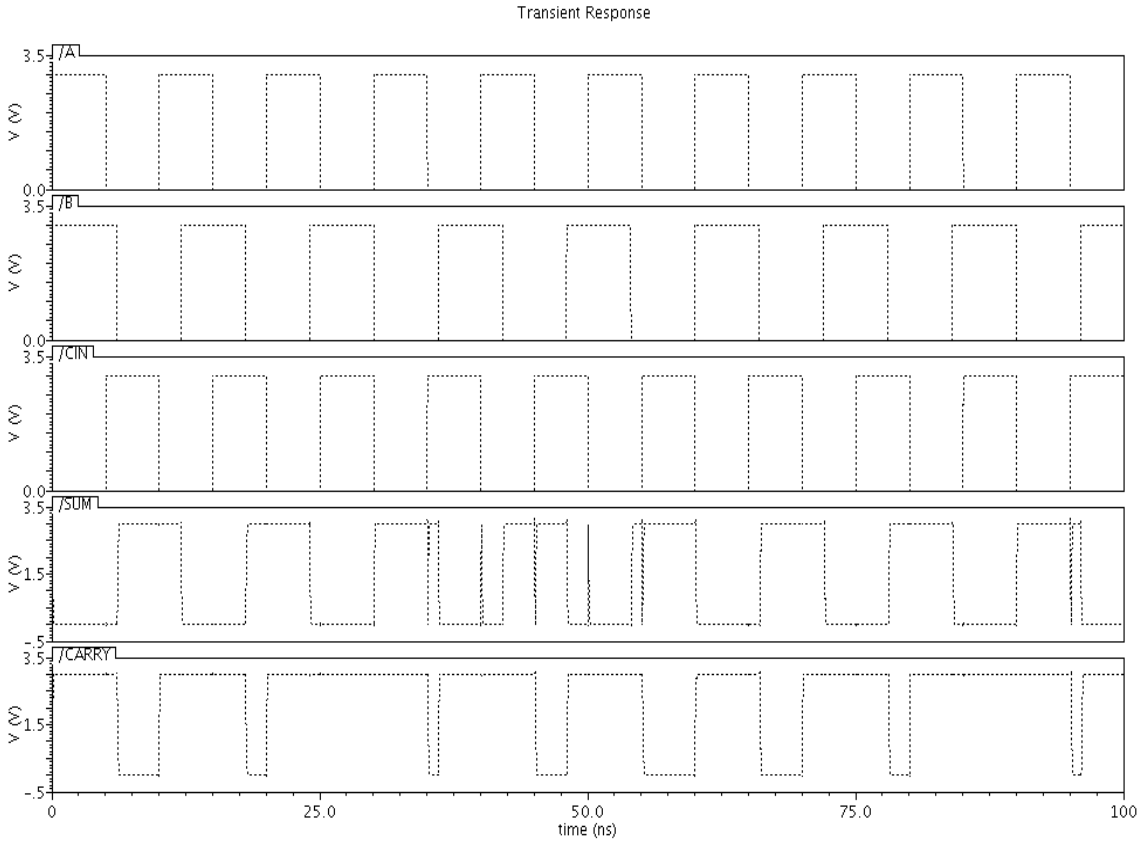


Figure 4.7: Goel Adder output curve

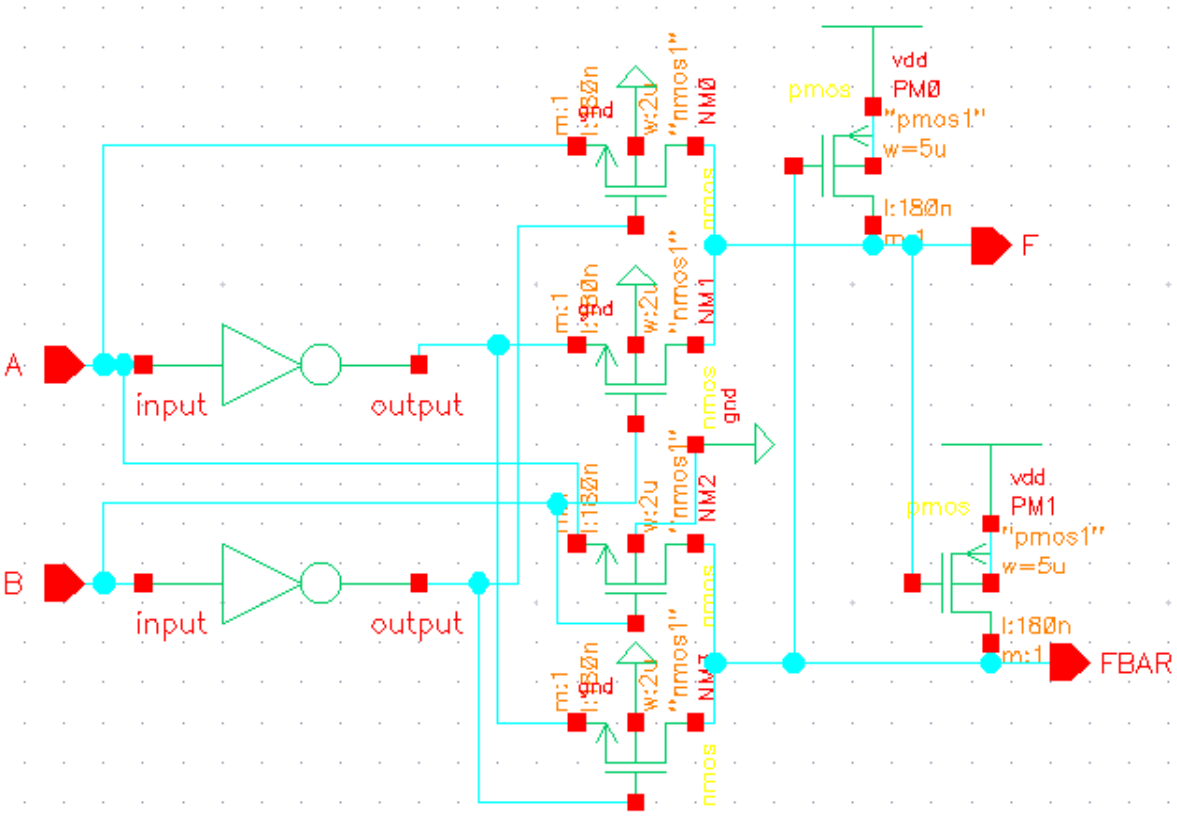


Figure 4.8: Symbol for Agarwal Adder (F & FBAR)

4.1.7 Implementation of Agarwal Adder:

As mentioned in [1], the numbers of transistor in this adder is very high. There are totally 32 transistors are used and the delay is found to be 59.13 ps at 3 V supply voltage This adder has a balanced structure with respect to generation of 'SUM' and 'CARRY OUT' signals. This helps in simultaneous arrival of signals in tree structured circuits. One symbol is been created to design the circuit. Four NMOS transistors and two PMOS pull up transistors are used in the symbol design. The symbol design, the design circuit & the output curves are shown in figure 4.8, figure 4.9 and figure 4.10 respectively.

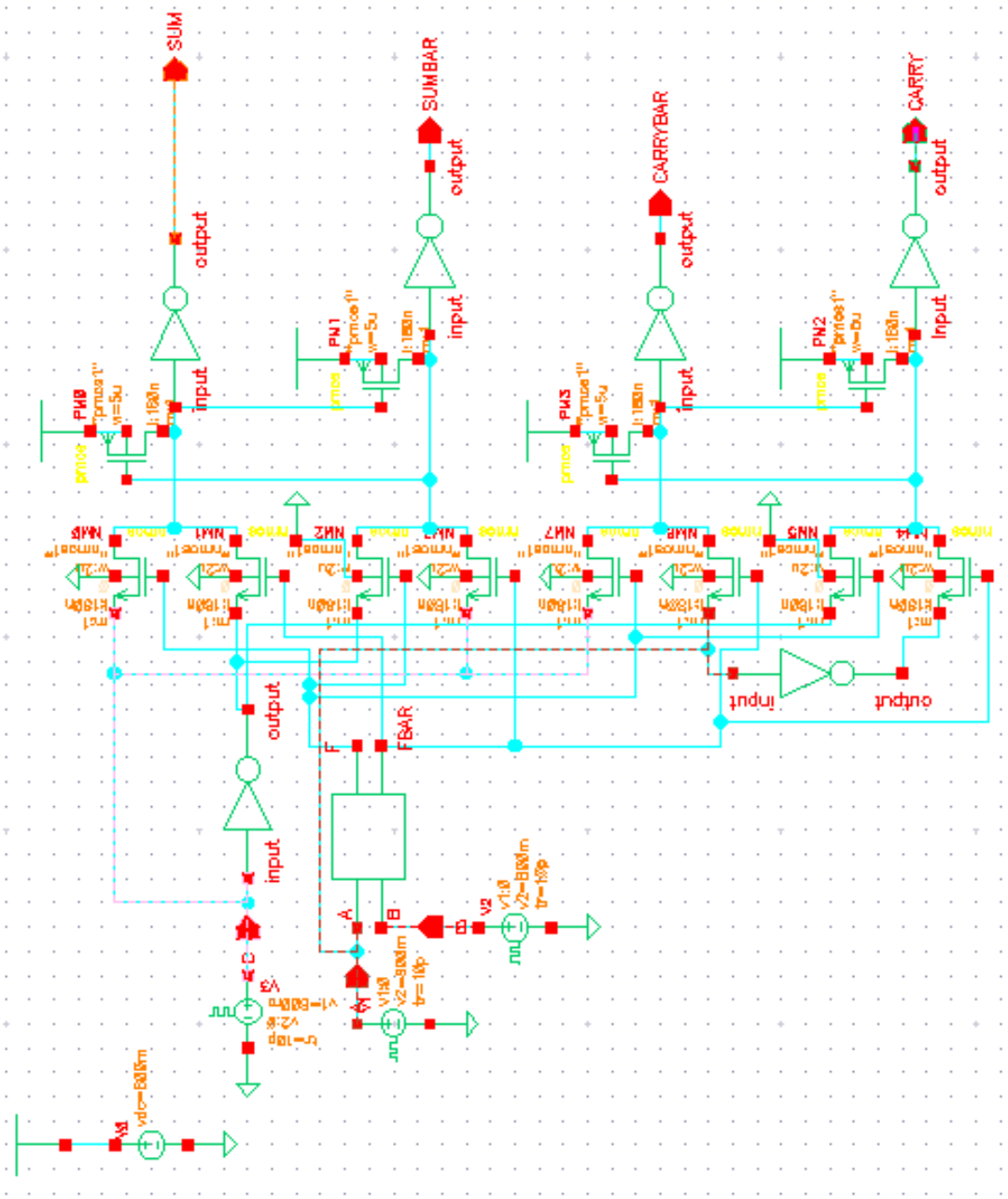


Figure 4.9: Implementation Agarwal Adder

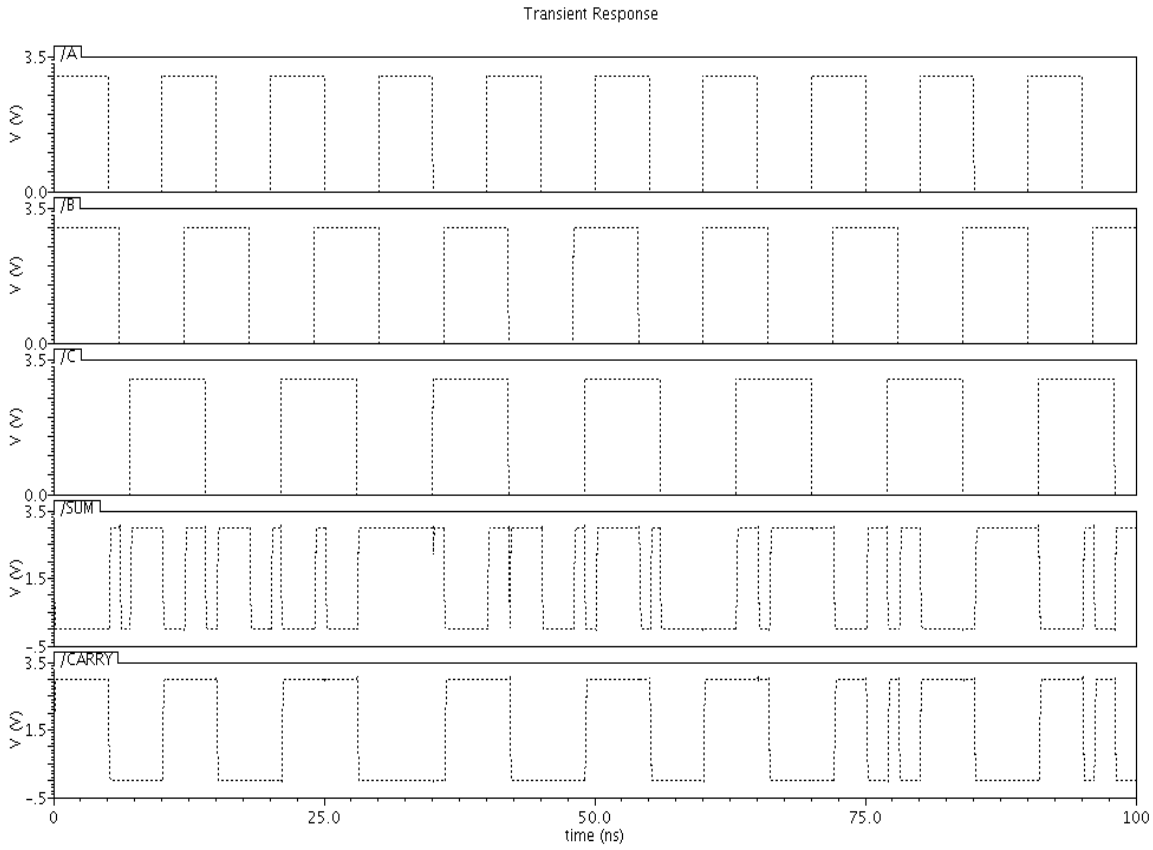


Figure 4.10: Agarwal Adder output curve

4.1.8 Implementation of Chang Adder:

The number of transistor used here is 26 and delay is found to be 28.99ps at 3 V supply voltage. But if the supply voltage is reduced below 1 V the adder shows wrong logic characteristics moreover the delay is very high below 1 V. It is designed as it is mentioned in [3]. The design circuit & the output characteristic curves are shown in Figure 4.11 & figure 4.12 respectively.

4.2Proposed Adders

The designs are based on XOR-XOR based full adder style. The basic SUM as well as CARRY functionality is as follows:

H=A XOR B

SUM=H XOR Cin

CARRY=H'A + HCin

4.2.1 Proposed PTL-GDI Adder

In this design the SUM cell is designed using Pass Transistor Logic (PTL) and the CARRY cell is designed using Gate Diffusion Technique (GDI). Firstly the H function is been

generated using two PMOS and two NMOS transistors and then using Cin and H as input the SUM function is obtained. The SUM cell is designed using PTL technique as it is shown in figure 4.13. The total number of transistor used is eight to obtain the SUM cell.

The CARRY cell is designed using GDI technique as shown in figure 4.14. The GDI cell is similar to inverter cell. The only difference is instead of connecting the source of the PMOS to the VDD and source of NMOS to the GND, two different inputs are provided through the sources of PMOS and NMOS. For CARRY calculation again H is used as input to the Gate and A & Cin variables are connected to the Source of PMOS and NMOS respectively. The XOR symbol design, the design circuit & the output characteristic curves are shown in Figure 4.16, figure 4.17 & figure 4.18 respectively.

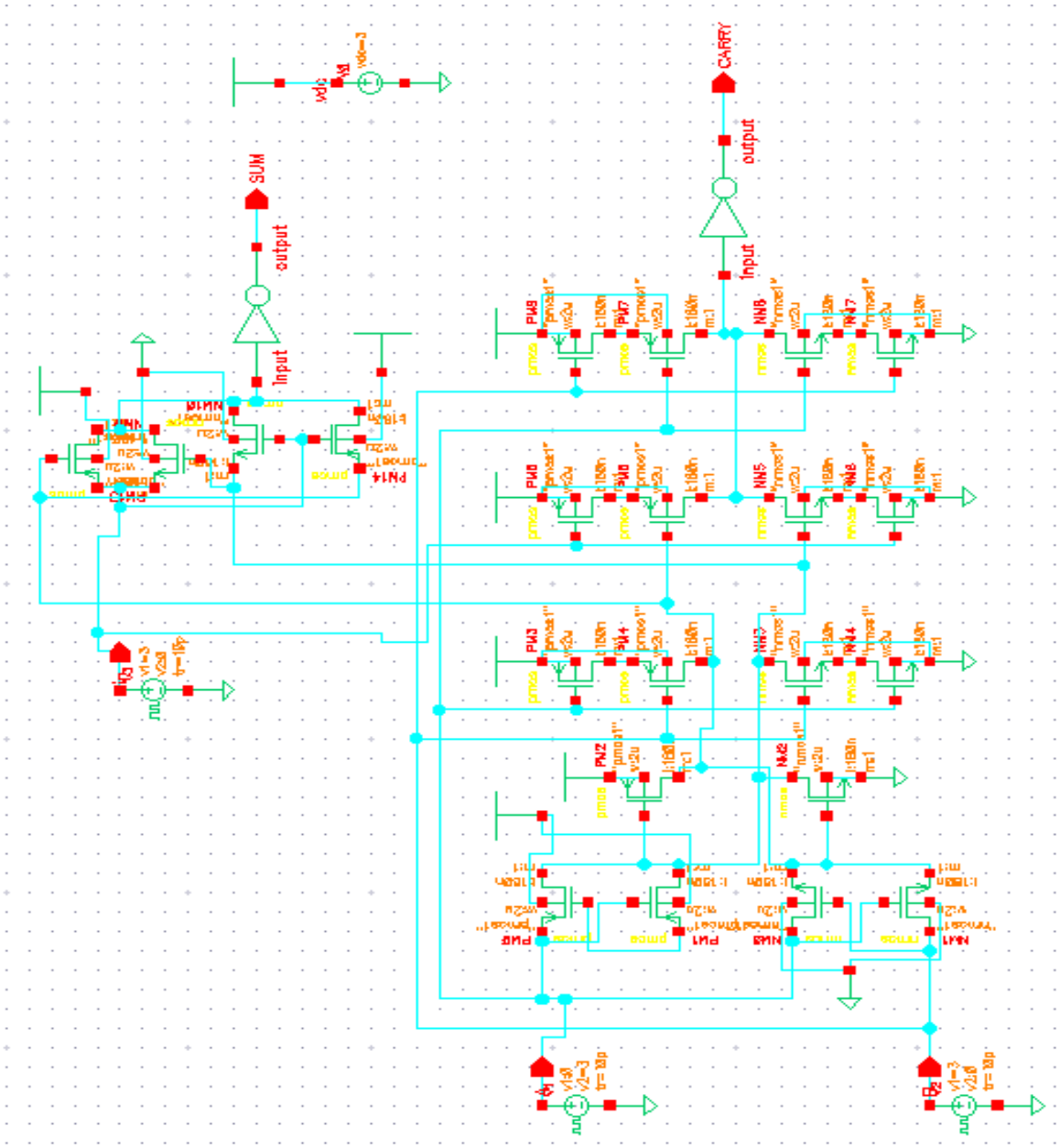


Figure 4.11: Implementation of Chang Adder

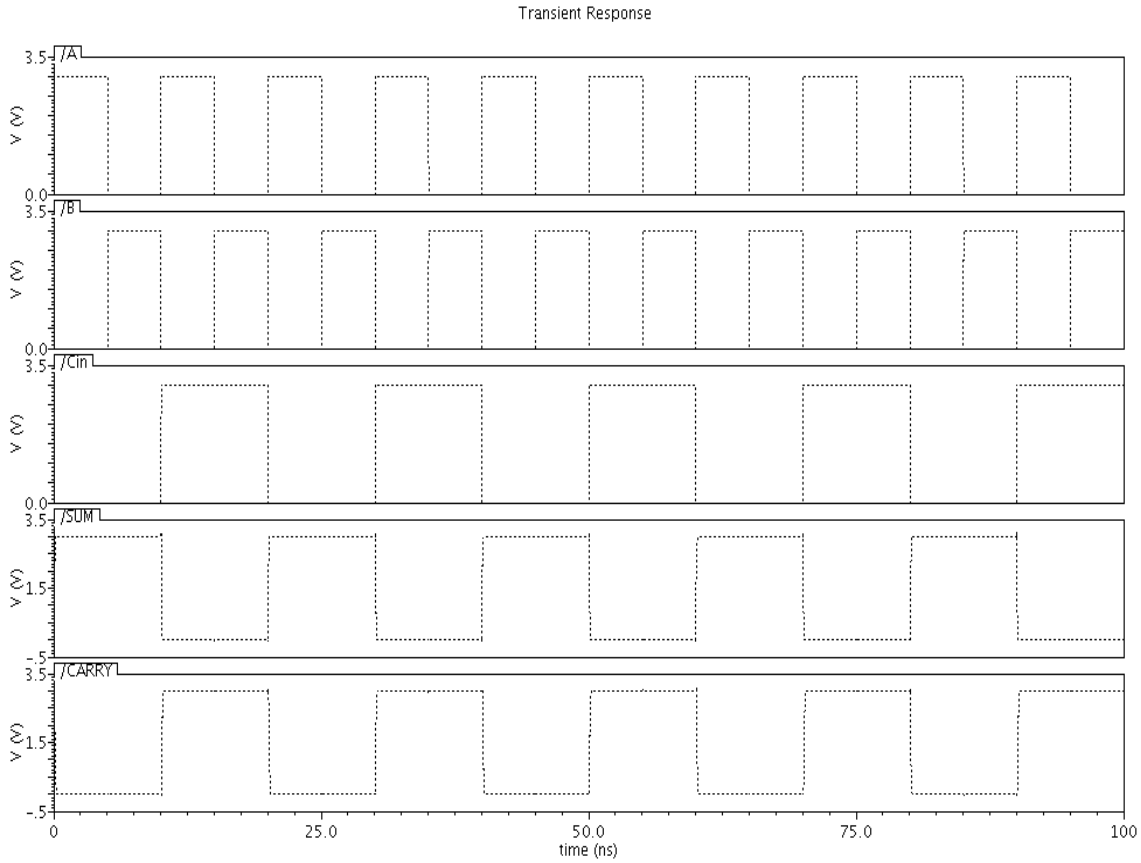


Figure 4.12: Chang Adder output curve

4.2.2 Proposed GDI Adder

In this design the SUM as well as CARRY cell is been designed using GDI technique. It needs totally 8 transistors to implement the SUM cell, as shown in the figure 4.15. Firstly H function i.e. XOR is implemented using GDI technique and then using this H function as input, the overall SUM as well as CARRY cell is been implemented. The CARRY cell design is similar to the CARRY cell of the Proposed PTL-GDI Adder and it is shown in figure 4.14. The design circuit & the output characteristic curves are shown in Figure 4.19 & figure 4.20 respectively.

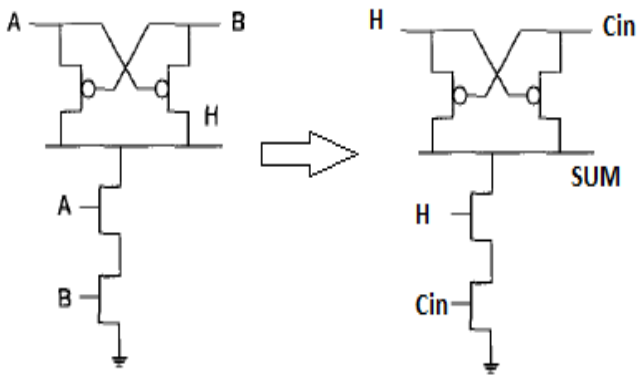


Figure 4.13: Proposed PTL-GDI based SUM cell

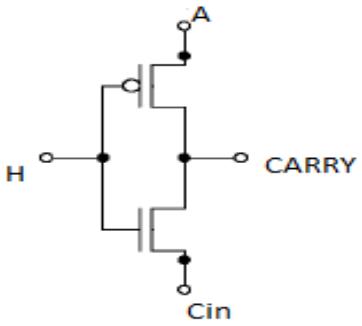


Figure 4.14: CARRY cell for both the design

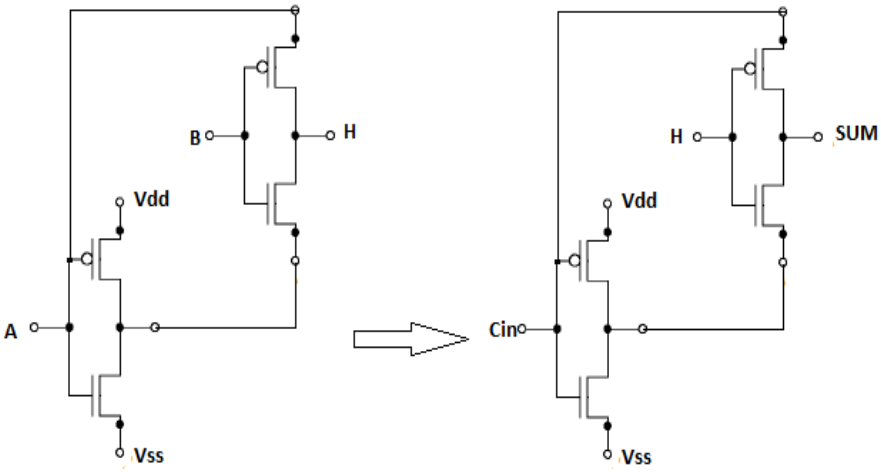


Figure 4.15: Proposed GDI based SUM cell

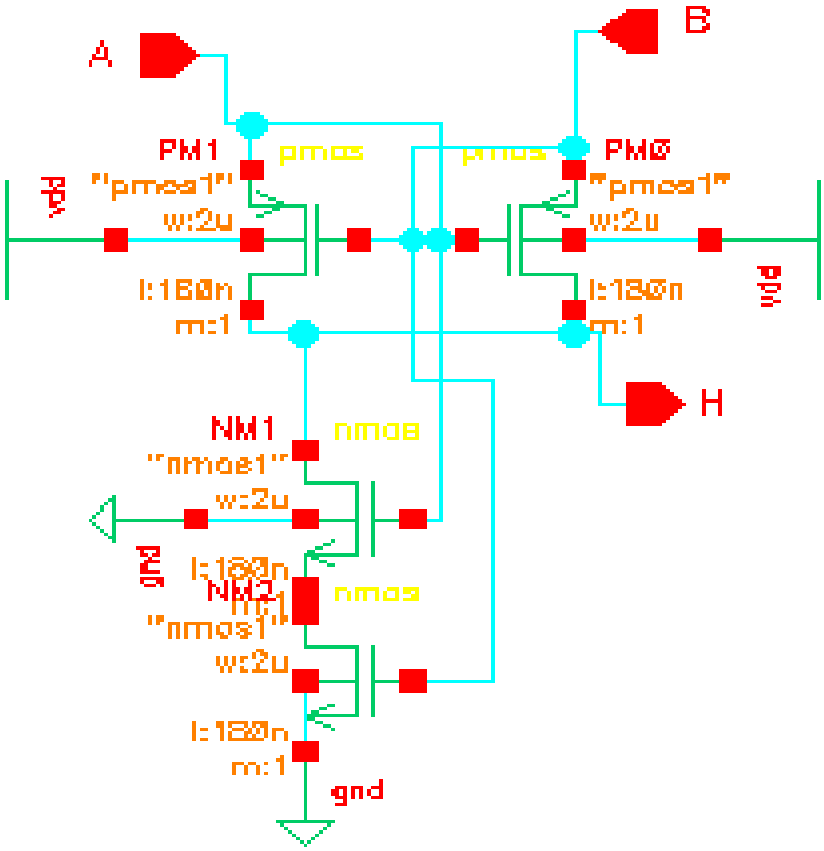


Figure 4.16: Implementation of XOR symbol for Proposed PTL-GDI Adder

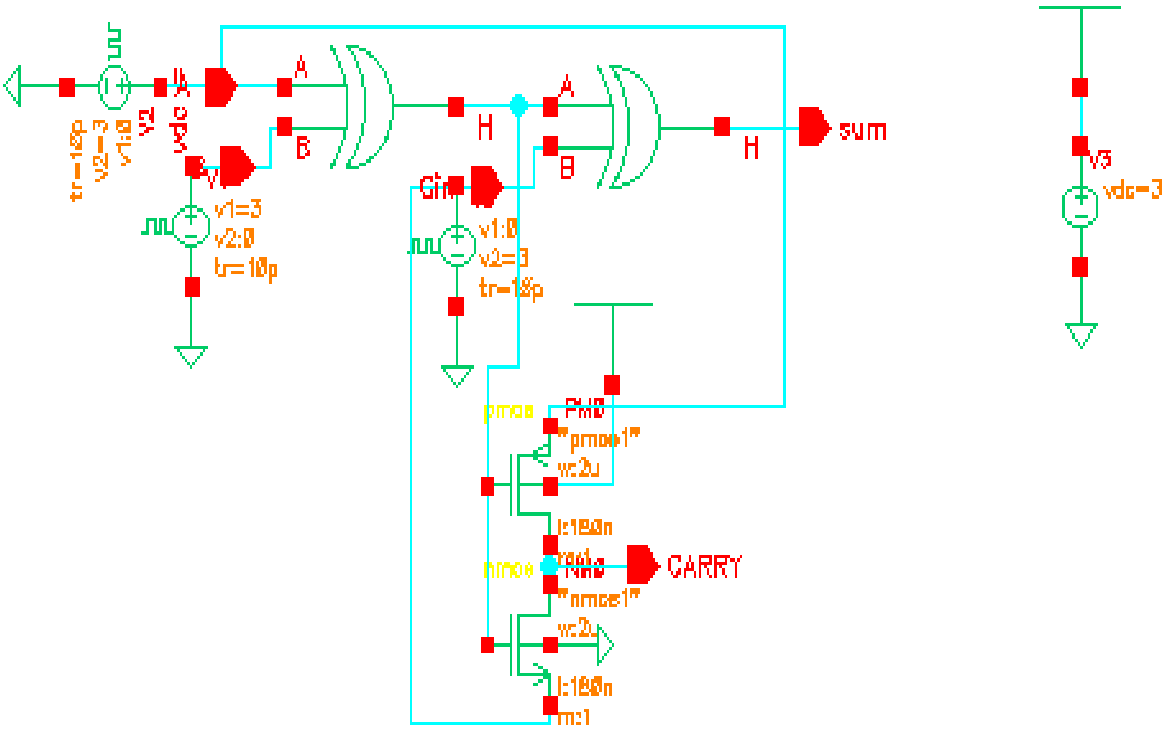


Figure 4.17: Implementation of Proposed PTL-GDI Adder

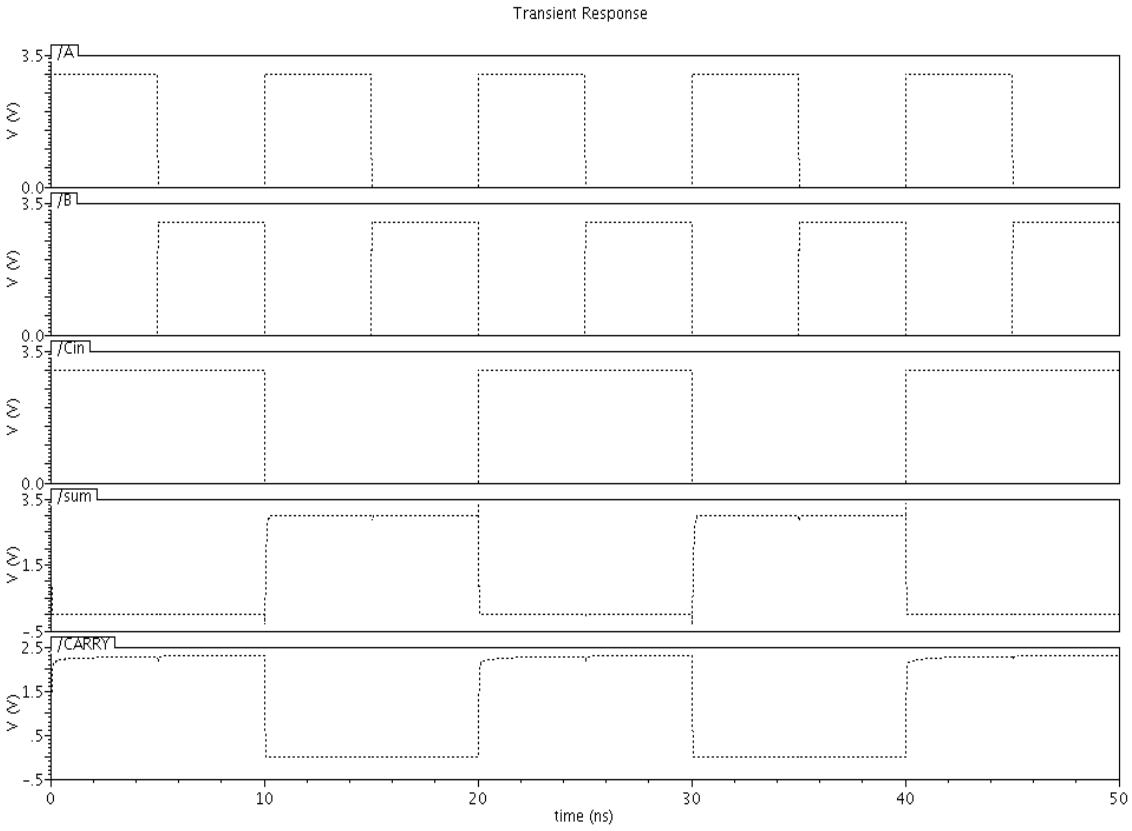


Figure 4.18: Waveform of Proposed PTL-GDI Adder

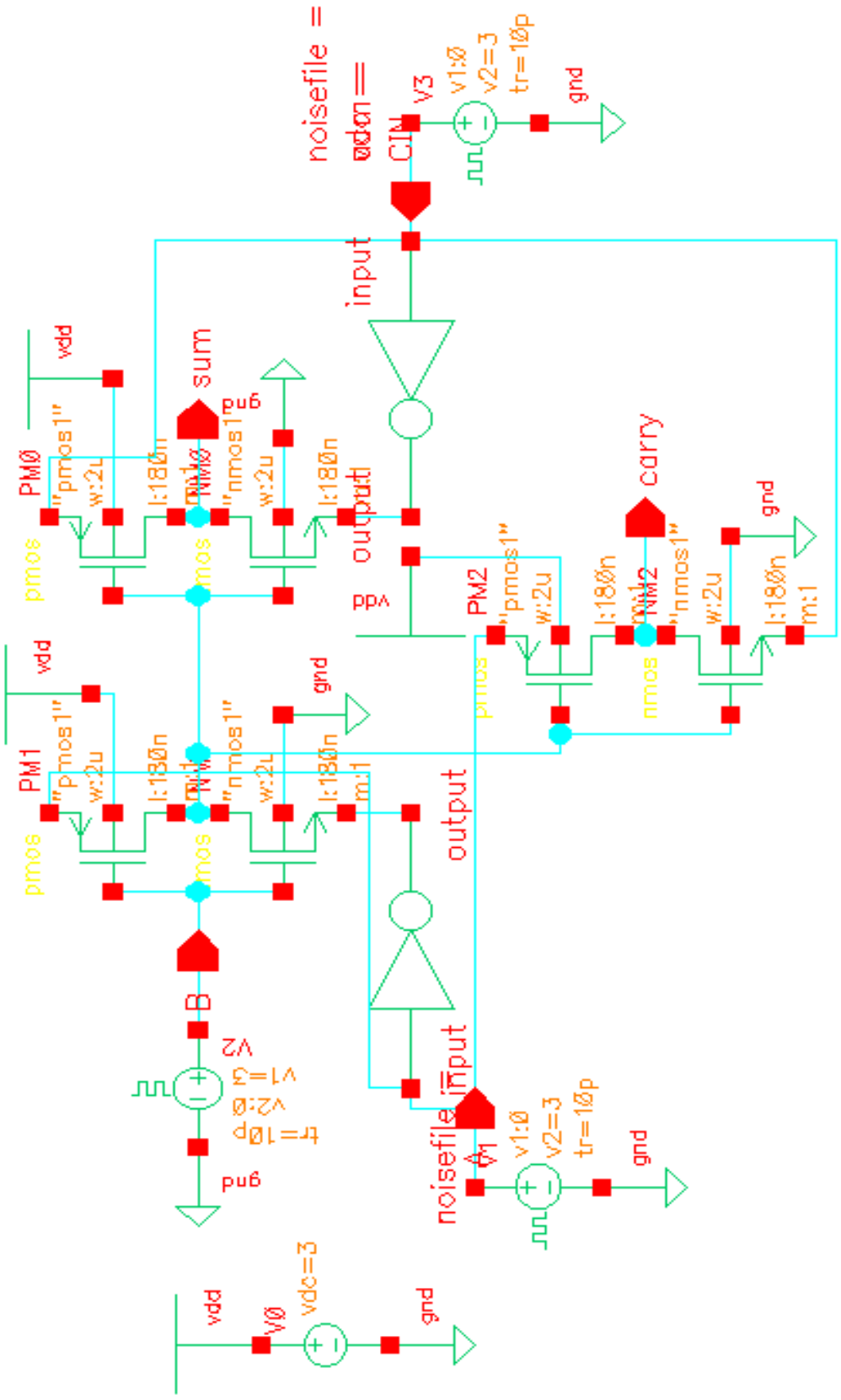


Figure 4.19: Implementation of Proposed GDI Adder

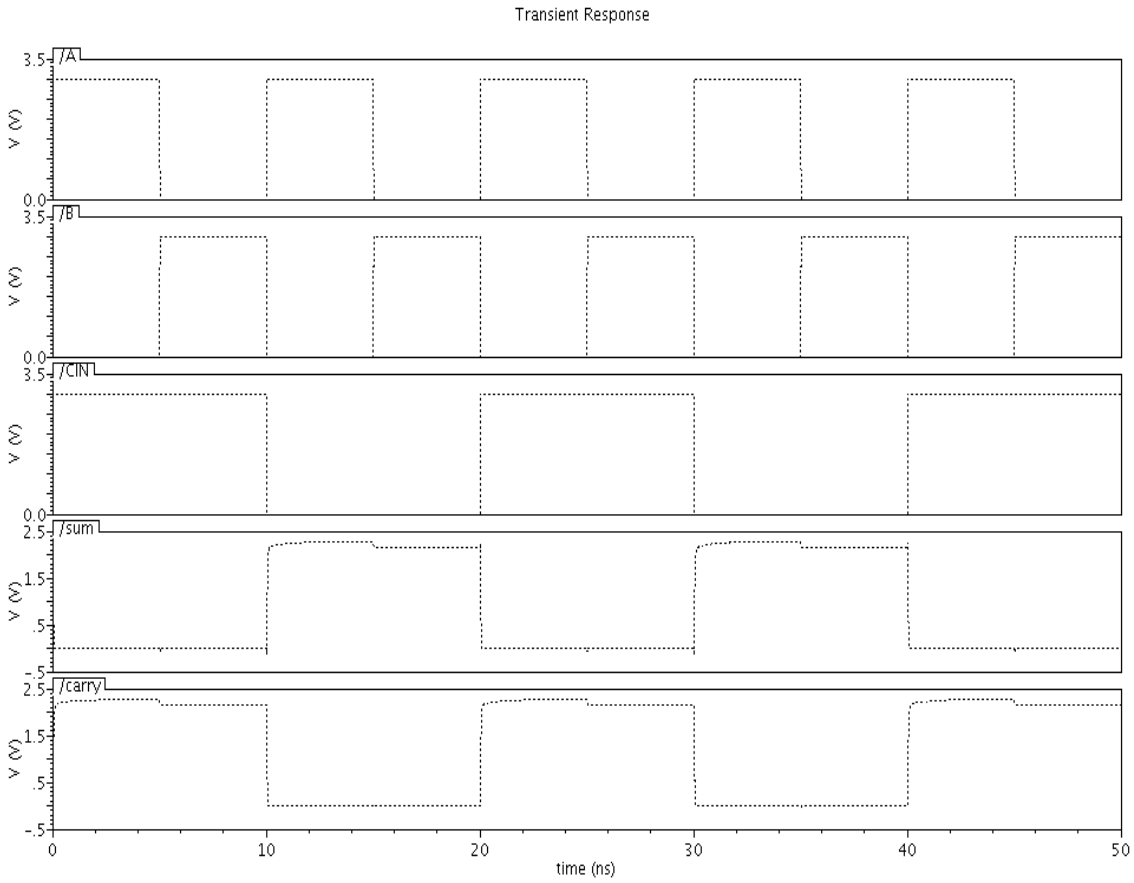


Figure 4.20: Waveform of Proposed GDI Adder

CHAPTER 5

Simulation results and discussion

By optimizing the transistor sizes of the full adders considered, it is possible to reduce the delay of all adders without significantly increasing the power consumption, and transistor sizes can be set to achieve minimum PDP. All adders were designed with minimum transistor sizes initially and then simulated. To achieve minimum PDP, an iterative process of redesigning and transistor sizing after post-layout simulations was carried out.

Comparison of full adders designed to achieve minimum PDP is discussed below. In particular, three subsections refer to delay, power, and PDP respectively. In each subsection, effect of varying supply voltage is considered.

5.1 Number of Transistor Used

The basic goal of an adder circuit is to produce correct logic characteristics with minimum number of transistors in order to produce lesser delay and optimum power consumption. As it is a basic concept that if the number of transistor decreases the delay as well as power consumption decreases. So our main motive was to reduce the number of transistor in our proposed design. Table 5.1 shows the number of transistors used for different Adders.

NUMBER OF TRANSISTORS			
SL NO	**ADDER**	**NMOS**	**TOTAL**
1	RADHAKRISHNAN	7	14
2	AGARWAL	19	32
3	CHANG	12	26
4	GOEL	11	22
5	PROPOSED PTL-GDI	5	10
6	PROPOSED GDI	5	10

Table 5.1: Number of Transistor used in various adders

5.2 Delay Comparison

As delay is the major issue to determine the characteristics of the design, our one main goal was to reduce the delay. The values of delay obtained for different Vdd values of 0.8V, 1.8V

and 3V. To make the comparison easier, Table 5.2 shows the delay values of different adders at 3V, 1.8V & 0.8V.

DELAY(pico second)				
SL NO	**ADDER**	**3V**	**1.8V**	**0.8V**
1	RADHAKRISHNAN	19.03	25.02	103.1
2	AGARWAL	59.13	79.74	448.3
3	CHANG	28.99	46.99	974.5
4	GOEL	55.68	92.4	746.6
5	PROPOSED PTL-GDI	17.13	23.29	93.69
6	PROPOSED GDI	13.8	19.39	88.35

Table 5.2: Delay comparison of different adders

As we can see from table 5.1 and table 5.2 that when the number of transistors decreases the delay also decreases. The delay is found to be very high in the case of Agarwal as well as Goel Adder. Worst performer is Agarwal Adder at 3V Vdd. But when the supply voltage decreases to 1.8V & 0.8V the worst performer is Goel Adder. Moreover in the case of Radhakrishnan Adder, Goel Adder & Chang Adder distorted outputs are generated at 0.8V Vdd (i.e. when the supply voltage decreases beyond some threshold value these adders are found to produce unexpected output).

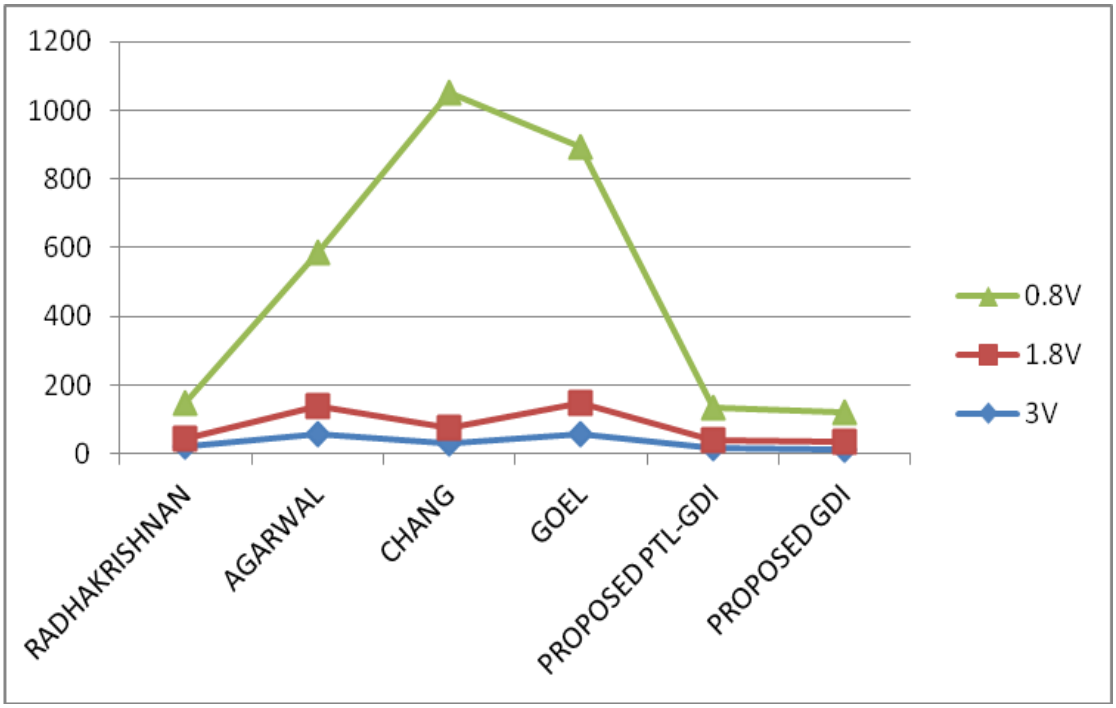


Figure 5.1: Delay plot of different adders at different supply voltages

Now considering the proposed designs i.e. Proposed PTL-GDI Design & Proposed GDI design, the number of transistors used here is comparatively very less. On the other hand the delay is also very low at different supply voltages for both the designs. Moreover both the proposed design produces correct logic characteristics even when the supply voltage is reduced to 0.8V. Looking at the table it can be easily understood that even though the number of transistors used for the proposed design are same but proposed GDI is found to be more delay efficient.

From the delay plot in Figure 5.1 it is very clear that as the supply voltage drops below the threshold voltage (in general $V_{dd}/2$), delay increases drastically. Even in this comparison too when the supply voltages are 1.8V & 3V it does not affect much in the curve but as the supply voltage reduces to 0.8V it creates a heavy delay in the circuit.

5.3 Power Comparison

The average power dissipation is evaluated under different supply voltages. Table 5.3 tabulates the values at 3V, 1.8V & 0.8V. Among the conventional existing full adders, clearly CPL has the highest power dissipation. The CPL adder dissipates the most power because of its dual-rail structure and high number of internal nodes in its design. Therefore, the CPL topology should not be used if the primary target is low power dissipation.

POWER CONSUMPTION(micro watt)				
SL NO	**ADDER**	**3V**	**1.8V**	**0.8V**
1	RADHAKRISHNAN	12.28	4.044	312.4 pw
2	AGARWAL	186.3	70.7	14.62
3	CHANG	100.8	26.67	43.09 nw
4	GOEL	876.5	228.7	12.13
5	PROPOSED PTL-GDI	2.779	1.097	225.3 pw
6	PROPOSED GDI	3.19	1.054	119.6 pw

Table 5.3: Power comparison of different adders

In the comparison table as we can see, Goel Adder consumes a huge amount of power. Even though the numbers of transistor used for Agarwal Adder is maximum, its power consumption is found to be very less with respect to Goel Adder. The proposed PTL-GDI design consumes lesser power in comparison with Radhakrishnan Adder even though the numbers of transistors used is only four more in Radhakrishnan Adder. Comparing the Proposed PTL-GDI Adder with Proposed GDI Adder, the power consumption of Proposed GDI Adder is found to be

more at 3V. But as the supply voltage decreases Proposed GDI Adder is found to be best performer in the comparison table.

Figure 5.2 shows the power consumption chart of different adders at different supply voltages. The graph itself justifies that at high supply voltage the power consumption is more. However high supply voltage creates a very negligible effect in Proposed PTL-GDI Adder & Proposed GDI Adder.

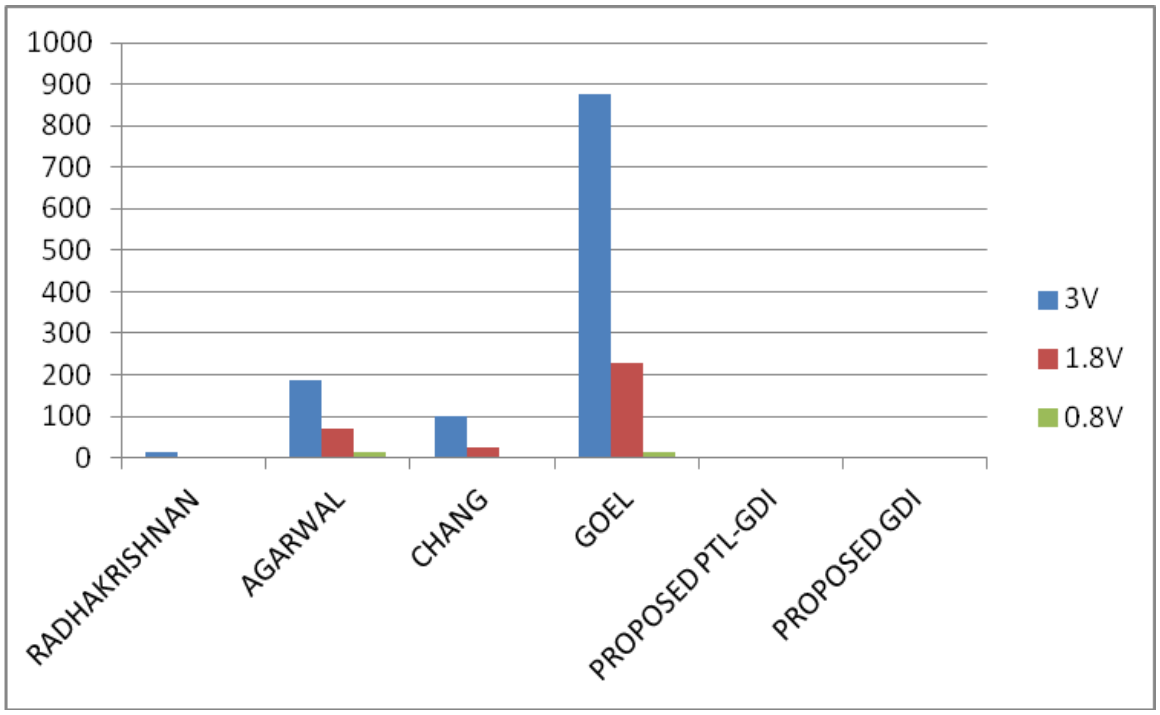


Figure 5.2: Power Consumption chart of different adders at different supply voltages

5.4 PDP Comparison

The PDP is a quantitative measure of the efficiency of the tradeoff between power dissipation and speed, and is particularly important when low-power operation is needed. The values of PDP are evaluated under different supply voltages are tabulated in Table 5.4.

POWER DELAY PRODUCT(PDP)				
SL NO	**ADDER**	**3V**	**1.8V**	**0.8V**
1	RADHAKRISHNAN	0.233 fj	0.101 fj	32.2 zj
2	AGARWAL	11.016 fj	5.613 fj	6.554 fj
3	CHANG	2.922 fj	1.253 fj	0.042 fj
4	GOEL	48.803 fj	21.13 fj	9.056 fj
5	PROPOSED PTL-GDI	0.048 fj	0.026 fj	21.11 zj
6	PROPOSED GDI	0.044 fj	0.020 fj	10.57 zj

Table 5.4: PDP comparison of different adders

The PDP is measured in Femto joule (fj) and Zepto Joule (zj). The Goel Adder has the maximum PDP even though the numbers of transistor used in Goel Adder is lesser than Agarwal Adder. Though the Chang Adder is found to be best in the literature [1] (with respect to PDP), both Proposed PTL-GDI Adder & Proposed GDI Adder are having very less PDP in different supply voltages.

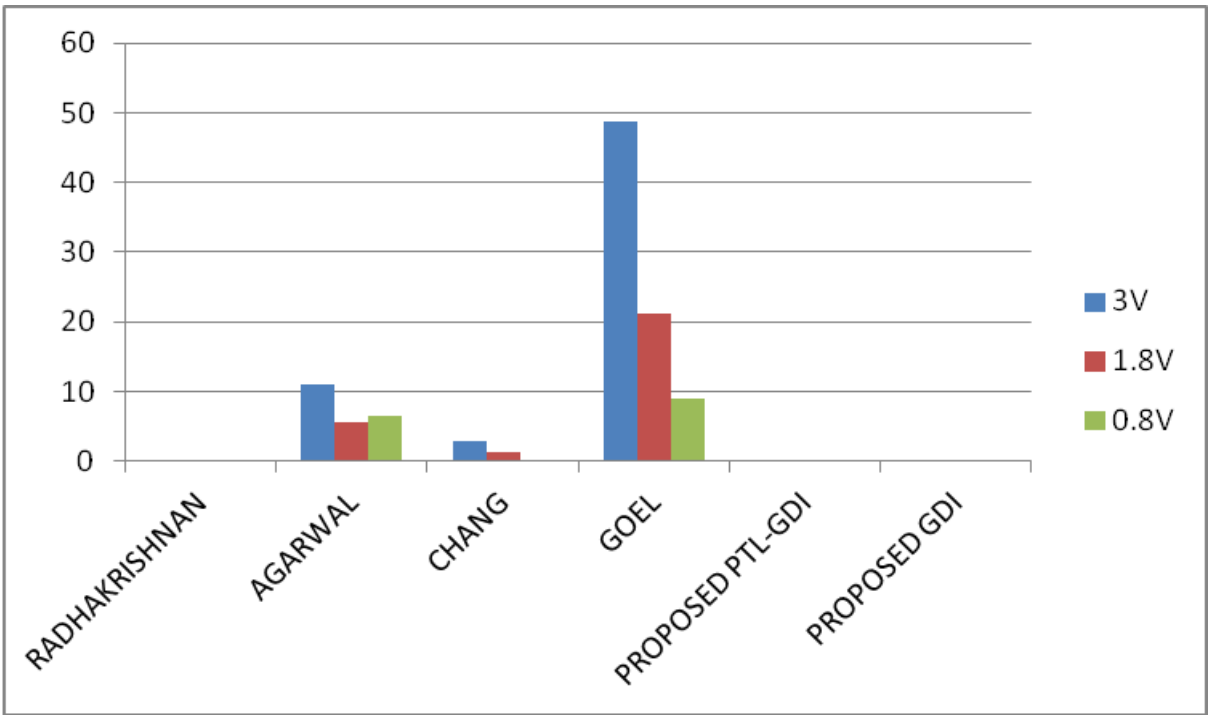


Figure 5.3: PDP comparison of different adders at different supply voltages

Figure 5.3 shows the PDP comparison chart of different adders at different supply voltages. Goel Adder is found to be the worst performer at three different supply voltages. Agarwal Adder, Chang Adder & Radhakrishnan Adder are comparatively found to be good performer than Chang Adder. However the Proposed PTL-GDI Adder & Proposed GDI Adder are the best performer at in PDP comparison too.

From the table 5.3 we can see that the Radhakrishnan Adder, Proposed PTL-GDI Adder & Proposed GDI Adder consumes very less power so their performances are plotted separately at 3V & 1.8V. 0.8V V_{dd} is not considered because the values are very less for all the three adders. It can be inferred from the plot that at 3V supply voltage proposed PTL-GDI Adder is the best performer. On the other hand Proposed GDI is the best performer the best one in 1.8V supply voltage.

PDP plot for Radhakrishnan Adder, Proposed PTL-GDI Adder & Proposed GDI Adder at 3V & 1.8V V_{dd} are shown in figure 5.5, as these adders PDPs are very less (refer table 5.4). As because at 0.8V V_{dd} the PDP is very less it is not been plotted. Comparing the chart we can infer that Proposed PTL-GDI Adder and Proposed GDI Adder both are performing equally.

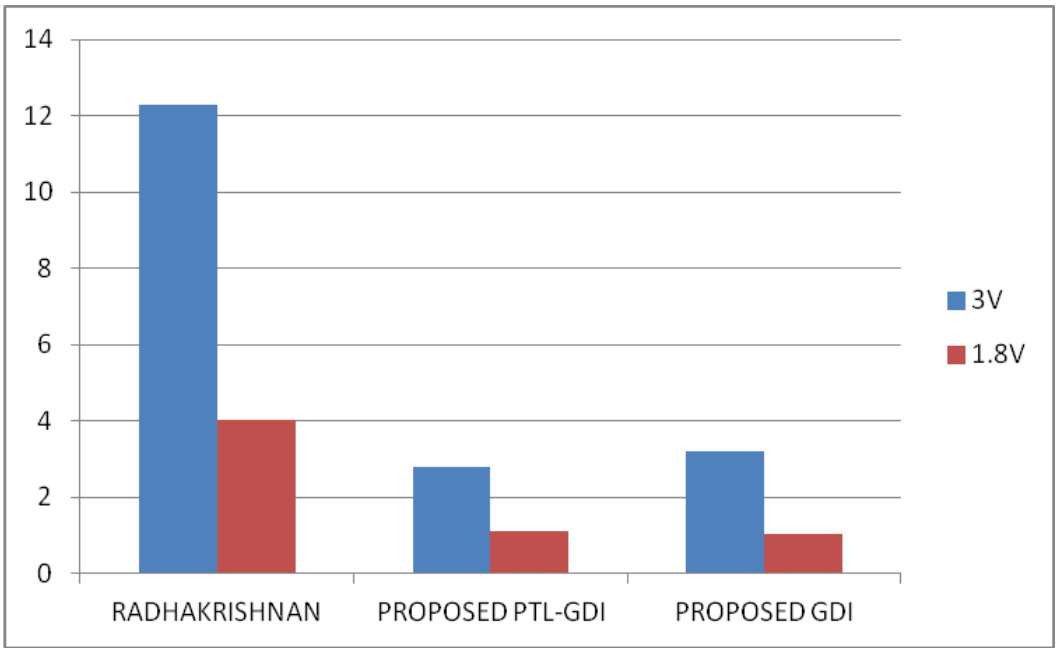


Figure 5.4: Power Consuption of Radhakrishnan, Proposed PTL-GDI & Proposed GDI Adder at 3V & 1.8V V_{dd}.

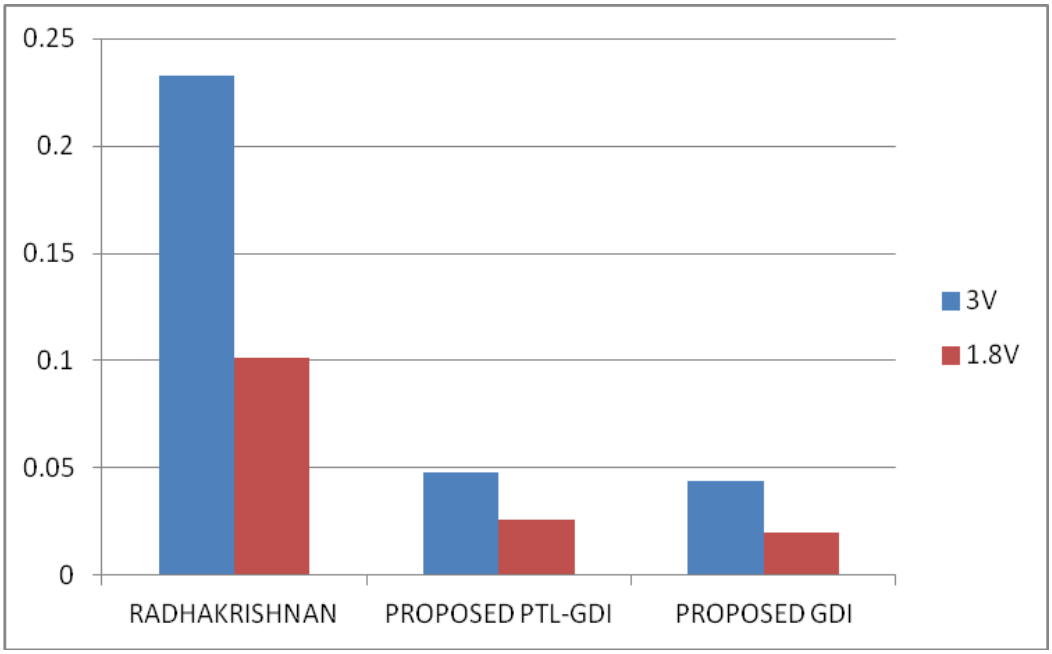


Figure 5.5: PDP of Radhakrishnan, Proposed PTL-GDI & Proposed GDI Adder at 3V & 1.8V V_{dd}.

CHAPTER 6

Conclusion

Hybrid design style gives more freedom to the designer to select different modules in a circuit depending upon the application. Using the adder categorization and hybrid design style, many full adders can be conceived. In this thesis work two novel full adders are designed using GDI design as well as PTL-GDI design style are presented that targets low PDP. The proposed hybrid full adders have better performance than most of the standard full-adder cells owing to the novels design modules proposed in this work. It performs well with supply voltage scaling. From the comparison table it can be inferred that both the proposed designs are good performer at different supply voltage conditions. However both the designs have their own advantages. They are:

1) If the supply voltage is above the threshold voltage (for example 3V), it is suggested to use Proposed PTL-GDI Adder.
2) If the adder is to be used in a wide range of supply voltages (for example 0.8V-3V), it is suggested to use the Proposed GDI design.
3) Considering Delay into account both the designs are found to be best in different supply voltages.

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