DESIGN & IMPLEMENTATION OF HYBRID FULL ADDER FOR ARITHMETIC AND LOGICAL OPERATIONS

DISSERTATION

Submitted in partial fulfillment of the

Requirement for the award of degree

Of

MASTER OF TECHNOLOGY

IN

ECE

By

MANPREET KAUR (11101915)

Under the esteem guidance of

Mr.Rajkumar Sarma

(Assistant professor)

School of Electronics and Communication Engineering

Lovely Professional University

Punjab

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CERTIFICATE

This is to certify that dissertation titled ***"Design & implementation of hybrid full adder for arithmetic and logical operations"*** is submitted by ***"Manpreet kaur"*** is in partial fulfillment of the requirement for the award of ***MASTER OF TECHNOLOGY DEGREE(ECE) ,*** is a record of bonafide work done under my guide ***Mr.Rajkumar Sarma .*** The content of this dissertation, in full or in parts, have neither taken from any other source nor have been submitted to any other institute or university for award of degree and same has been certified.

MR.RAJKUMAR SARMA

ASSISTANT PROFESSOR

(LOVELY PROFESSIONAL UNIVERSITY)

Objective of the thesis is satisfactory/unsatisfactory

EXAMINER 1 ***EXAMINER 2***

ACKNOWLEDGEMENT

I would like to thank *LOVELY PROFESSIONAL UNIVERSITY* for giving me an opportunity to use their resources and work in such a challenging environment. I am grateful to the individuals who contributed their valuable time towards my dissertation work.

I wish to express by sincere and heart full gratitude to my guide *Mr. Rajkumar Sarma*, Assistant Professor, who guides me to take up this dissertation work in synchronization with global trends in scientific approach. Even I am very thankful to my parents and friends who supported me in ups and downs of my life.

MANPREET KAUR

Registration no. 11101915

CERTIFICATE

This is to certify that *MANPREET KAUR* bearing *registration no. 11101915* has completed her dissertation-2 work on the title ***"DESIGN & IMPLEMENTATION OF HYBRID FULL ADDER FOR ARITHMETIC AND LOGICAL OPERATIONS"*** under my guidance & supervision. To the best of my knowledge, the present work is the result of her original investigation & study.

MR. RAJKUMAR SARMA

Assistant professor

Lovely Professional University

Phagwara, Punjab

Date:

CANDIDATE DECLARATION

I, ***MANPREET KAUR*** student of *MASTER OF TECHNOLOGY (ECE)* under department of *ELECTRONIC ENGINEERING of LOVELY PROFESSIONAL UNIVERSITY, PUNJAB,* hereby declare that all the information furnished in this dissertation report is based on my own intensive research and it is genuine.

This dissertation does, to the best of my knowledge, contain part of my work which has been submitted for the award of my degree.

Date

MANPREET KAUR

Registration No. 11101915

ABSTRACT

This thesis focuses mainly on hybrid adder in which adder implementation is done using different techniques. As adder is the most basic fundamental unit for every digital circuit like digital signal processors. So, adder is an important topic for researchers in which research can be done to improve whole digital circuit. In this thesis basically optimized adder circuit is implemented in terms of PDP.As nowadays power and delay are of more concern as compared to area because size of transistors is decreasing day by day. Hybrid adder implementation is done inside Cadence Virtuoso using 180nm technology. Even its layout is designed in Cadence Spectra and its DRC, LVS and RC extraction is done. After this multiple bit adders are implemented using optimized hybrid full adder.

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ABBREVIATIONS

ALU……..……..Arithmetic logical unit

DSP……..…….……..Digital signal processing

RCA…….……Ripple carry adder

CMOS……...Complementary metal oxide semiconductor

PMOS…….P-type metal oxide semiconductor

NMOS……N-type metal oxide semiconductor

PTL……Pass transistor logic

CPL…….....Complementary pass-transistor logic

DPL……...…….. Double pass-transistor logic

DVL……..…….……. Dual value logic

GDI……..…….Gate diffusion input

VLSI……..…...Very large scale integration

CHAPTER 1

INTRODUCTION

Addition is one of the foremost and fundamental logic carried out in digital circuits. An adder is a very basic digital logic circuit that performs addition of numbers. In many computers as well as processors adders are being used in arithmetic units as well as other parts of the processors. They are used for calculating table indices, addresses, and increment as well as decrement operations.

Mostly adders generally operate on the binary numbers. Adders are also used for many numerical representation like excess 3 and binary coded decimal.

Now adders are classified into 2 categories:

- Single bit adders
- Multiple bit adders

1.1 Single bit adders

1.1.1 Full adder using basic universal gates.

a) Using nand gate

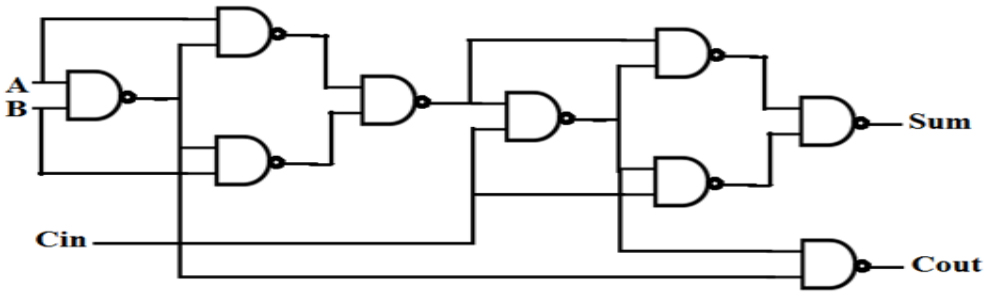

Figure.1.1.1 (a): Full adder using nand gates

(b) using nor gates

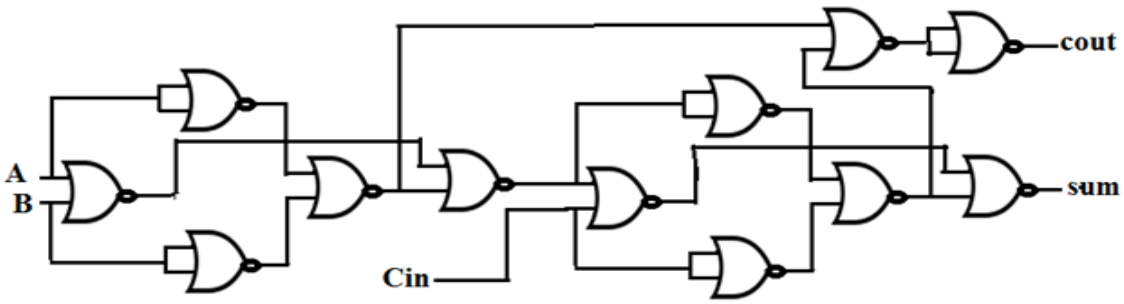

Figure 1.1.1(b) : Full adder using NOR gates

1.1.2. Implementation of full adder using half adders.

Table 1.1: Truth table of half adder

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

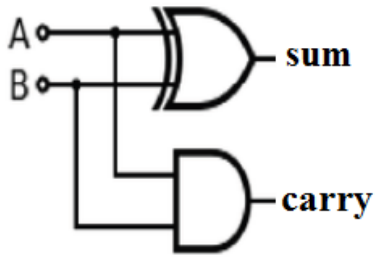

Figure 1.1.2.Circuit diagram of half adder

Full adder can be implemented using half adders and we can implement half adder by using various circuits like xor gate & and gate. And by using this half adder we can implement full adder.

Table 1. 2: Truth table of full adder

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

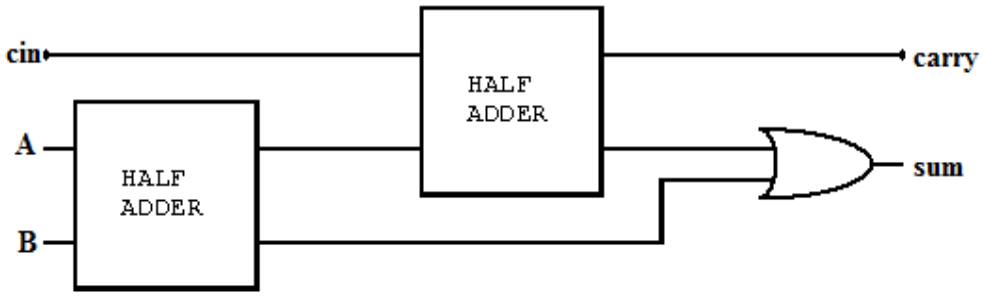

Figure 1.1.3: Implementation of full adder by using half adder

1.2. Multiple bit adders.

1.2.1 Ripple carry adder

Ripple carry adder is implemented using multiple full adders. For making N bit Ripple carry adder we need to use N number of full adders. Carry of each previous full adder will be input carry to the next full adder. So, as in this adder each carry bit "ripples" to the next full adder this adder is known as ripple carry adder. Layout of this type of adder is simple which allows fast design time. However this type of adder is relatively slow as compared to the other full adders because each full adder must wait for carry input to be calculated from previous full adders.

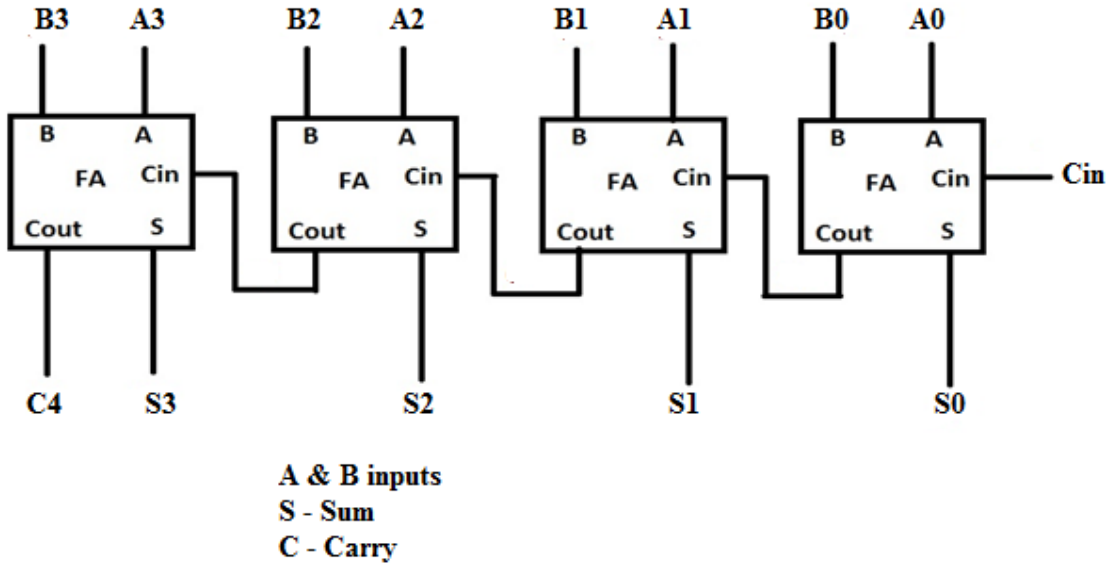

Figure 1.2.1: Ripple carry adder

1.2.2 Carry save adder

To add M numbers(each no. N bit wide) we need to first of add 2 no.'s and then we need to add their sum with next number and so on. So, this requires M-1 additions and total delay of O(M lg N).Using carry save adder delay can be reduced further using carry save adder.

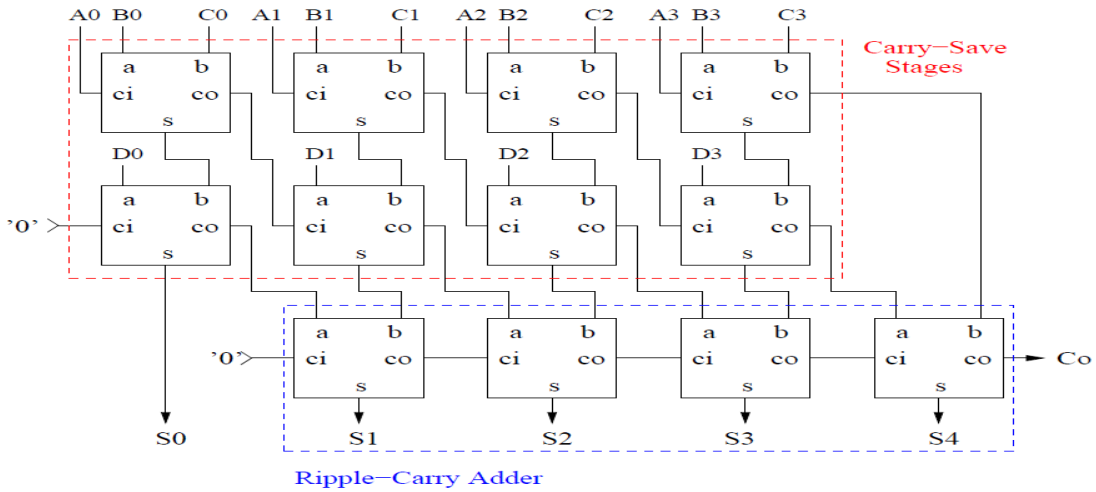

Figure 1.2.2: Carry save adder

In this type of adder suppose we addition of 3 numbers is required in that case first of all we need to add 1st two numbers and then their sum will be added into 3rd number conventionally.

carry:		1	1	2	1	
x:		1	2	3	4	5
y:		3	8	1	7	2
z:	+	2	0	5	8	7
sum:		7	1	1	0	4

But in case of carry save adder we need to add all the three numbers in single time and their carry & sum will be calculated separately.

x:		1	2	3	4	5
y:		3	8	1	7	2
z:	+	2	0	5	8	7
s:		6	0	9	9	4

x:		1	2	3	4	5
y:		3	8	1	7	2
z:	+	2	0	5	8	7
c:		1	0	1	1	

After this carry and sum need to be added.

s:		6	0	9	9	4
c:	+	1	0	1	1	
sum:		7	1	1	0	4

1.2.3 Carry select adder

Carry select adder basically consists of two ripple carry adders and a multiplexer. In case of Ripple carry adder two cases will be taken in first case assumption will be carry = 0 and in second case carry will be = 1.So, two pairs of ripple carry adders will be used in first case input carry will be 0 and in second case input carry will be 1.So, their will be 2 pair of results i.e. Sum and carry twice. After that correct sum and carry will be calculated by using multiplexer using initial input carry as select line of multiplexer.

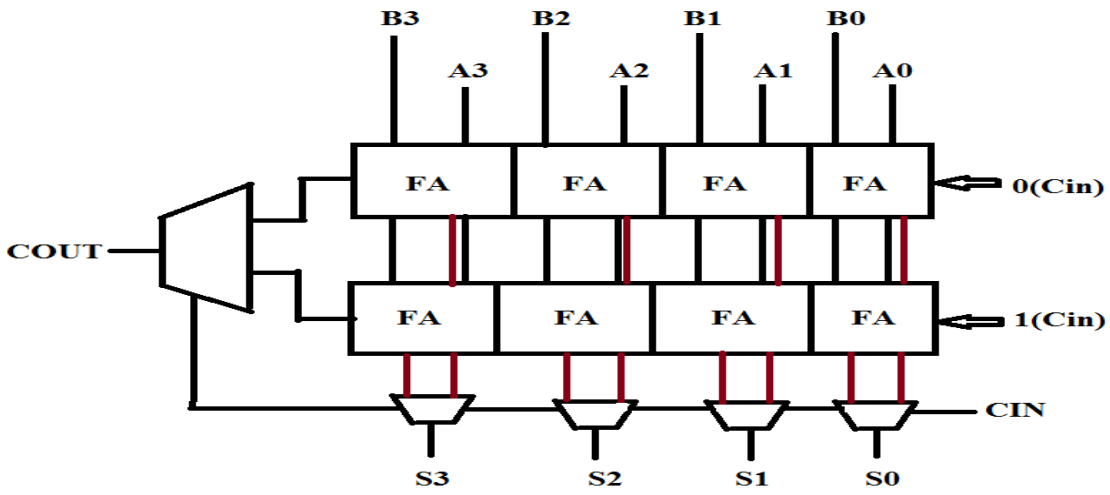

Figure 1.2.3: carry select adder

1.3. Different techniques to implement basic full adder

So, there will be different kind of design techniques using those techniques we will be going to implement our circuit. As each and every technique has certain advantages and disadvantages we will try to figure out those:

To understand the basic concepts take example of **and** gate logic and implement and gate with different techniques:

1.3.1.CMOS technique

For implementation of and logic y= (a.b)

Rules :(a) Pmos above and Nmos below

(b) Non of the true form can be implemented using Cmos technique.

(c) In case of sum Pmos will be in series and Nmos will be in parallel while in case of product pmos in series and Nmos in parallel.

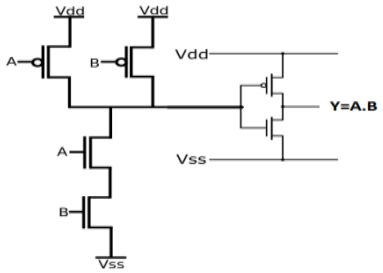

Figure 1.3.1:Implementation of and gate using conventional CMOS technique

1.3.2. Transmission gate

Rules: Nmos and Pmos will be in front of each other (Cmos switch in case of Verilog). For implementing y=a.b

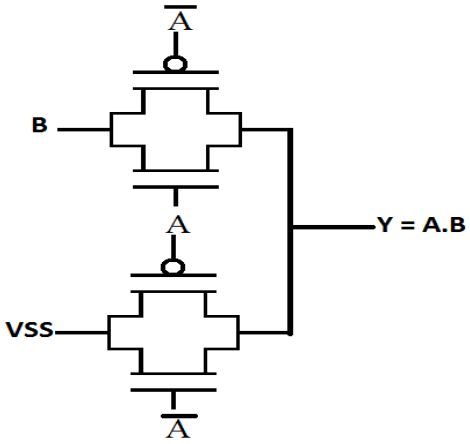

Figure 1.3.2 : transmission logic and gate

1.3.3. PTL (pass transistor logic)

Passing one variable with respect to other. For y = a.b only one transistor will be required to represent.

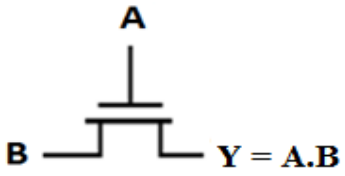

Figure 1.3.3: PTL logic and gate

Pass transistor logic families

Types of pass transistor logic families:

- CPL
- DPL
- DVL

1.3.3.1. Complementary pass transistor logic

Complementary pass transistor logic contains inputs/outputs in complemented form, CMOS inverter output and NMOS pass transistor network. Circuit is implemented as a tree using pull up and pull down branches. Due to the threshold voltage drop of Nmos transistor degrade of high level of pass transistor output nodes, CMOS inverters will be used to restore output signals. This technique is used in high speed operation because of reduced transistor count and low input capacitance.

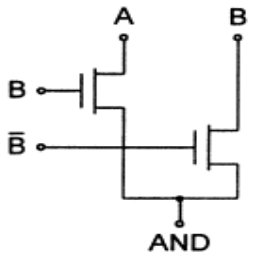

Figure 1.3.3 (a): CPL logic and gate

1.3.3.2 .Double pass transistor logic

For removing the problem of noise margin in CPL,two pmos branches are added in N-tree DPL.

Due to addition of Pmos branches input capacitance will increase. Due to its symmetrical arrangement speed degradation will arise because of increased loading. Advantage of double pass transistor logic will be full output swing without any voltage degradation.

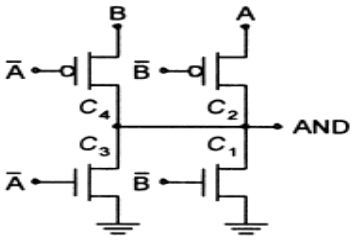

Figure 1.3.3 (b): DPL logic and gate

1.3.3.3. Dual value logic (DVL)

Main limitation of DPL logic is usage of more number of transistors than required so DPL is redundant. To remove this problem of redundancy a new technique is introduced from DPL that is DVL. It has reduced transistor count along with full voltage swing operation of DPL.DVL can be obtained from DPL by following 3 steps.

- Eliminate redundant branches

- Rearrangement of Signal (resize)
- Selection of the faster halves.

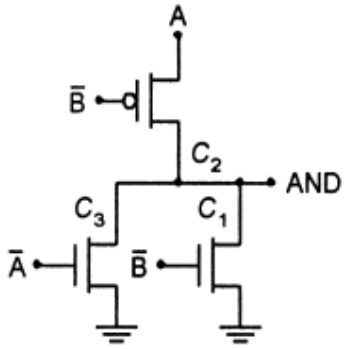

Figure 1.3.3(c): DVL logic and gate

1.3.4. GDI (gate diffusion input) technique: A GDI cell consists of one Nmos and Pmos exactly like inverter but instead of passing Vdd and Gnd we will pass signals. But difference is instead of passing Vdd and Gnd we will pass signals.

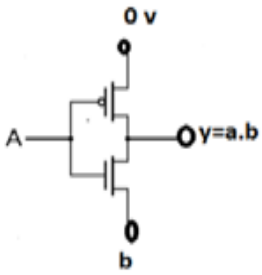

Figure 1.3.4: Implementation of and using GDI technique

Advantages and disadvantages of these techniques

For simple units like y=~ (a.b) transmission technique is not better but simple cmos technique will be better. But if suppose y=(a.b+c).d+e then transmission technique will be better than cmostechnique.PTL logic and GDI techniques are easy way to design a circuit but they are having problem of strong 1 and strong 0.because pmos will not be able to pass strong 1 but it can pass strong 0 and nmos cannot be passing strong 1 but it can pass strong 0. So, no. of glitches will be more.

1.4. Applications of adder

In our day to day life such as mobiles, phones,laptops,personal computers etc. are equipped with microprocessors that contain ALU. As a part of ALU adders are responsible for carrying

out computations in determining floating point calculations memory address generation, and index and other similar type of operations required in DSP processors in which large amount of visual and voice signals are processed at very high speed. Due to this reason DSP processors require complex adder circuits.

Today wireless communications are digitized and conditioned in the the DSP, that requires too much computation power for having a complete control over analog signals. Choosing the best adder out of them will consume less power and will be more energy efficient at low supply voltage.

CHAPTER 2

SCOPE OF STUDY

Design parameters in VLSI design

- **Power**

  The power dissipation is directly proportional to the area covered by the circuitry. Hence the power can be reduced by reducing the area of the circuit and also by using the low power components.

- **Area**

  The area is a major concern in any of the analog circuit design. The area can be reduced by reducing the no. of transistors in the circuit design. By reducing the transistor count and playing with the W/L ratio of the transistors' the area of the circuit can be reduced.

- **Speed**

  The speed of the adder is a very important design parameter for high speed system operation.

By implementing full adder using half adder i.e using standard or any other conventional technique in that case there are no. of disadvantages like

- No. of transistors will be more due to that while IC fabrication number of chips used will be more but in VLSI we try to minimize area as much as possible .
- Secondly, power consumption and delay will be more but our main constraints are to reduce power as well as delay.

So, here comes the scope of study as according to Moore's law transistor size is decreasing day by day as now we are even VLSI companies are working on 22 nm technology. So, even if no. of transistors on single chip will increase there is a great need to reduce our power and delay. So, scope of study is to reduce power and delay.

CHAPTER 3

OBJECTIVES OF THE STUDY

- To design hybrid full adder with reduced power consumption.
- To design a hybrid full adder with reduced delay.
- To design layout of hybrid full adder.
- To design multiple bit adders.

CHAPTER-4

LITERATURE REVIEW

In this chapter literature review related to topic of research has been discussed. I have read many research papers like journals and conference papers related to my topic of research and few of those papers are given below. This chapter is about basic concept of the papers which I have studied.

Bhattacharyya P. et.al 2014[1]: In this paper 1-bit full adder is implemented using hybrid logic employing both transmission gate logic and complementary- metal-oxide-semiconductor (CMOS) logic. The design was implemented for 1 bit as well as 32 bit full adder. Circuit is implemented using Cadence Virtuoso tool in 180 & 90 nanometer technology. Power, delay, layout area & otherPerformance parameters are compared with existing techniques. In terms of power and speed as compared to existing designs of full adder, proposed circuit is better.

Aguirre-Hernandez M. et.al 2011[2]: Two high speed and low power full adder cells are designed with pass-transistor logic & alternative internal logic styles that lead to reduction in PDP. All the full adders are designed in 0.18μm CMOS technology and were tested using complete test bench which will be used for measuring current taken from inputs of full adder, in addition to the current provided from the power-supply. Circuit exhibits an average PDP advantage of 80%, with only 40% of relative area and outperforms its counterparts shown from Post-layout simulations.

Wairya S. et.al 2011 [13]: In this paper relative study of full adder circuits with low power, low voltage & high speed is carried out. 4 transistor circuit design full adder circuits are combined to form a single unit on the basis of XOR-XNOR .This technique will make the logic design less complex as well as it will be helpful for reduction of power expenditure and delay. Noise analysis show that it can work at high frequency and low temperature. The design is implemented in Cadence Virtuoso.

Zavarei M.et.al2011 [14]: Based on novel XOR XNOR circuit this hybrid full adder will generate full swing outputs and will be best as compared to its counterparts as it will show 28% improvement in power delay product. This proposed full adder circuit is designed on the

basis of improvement in PDP and it will provide full swing output along with good driving capability.

Aranda M.et.al2010 [9]: In this paper comparsionand analysis for power usage, speed and power delay product has been carried out for topologies of 1 bit full adder. Performance comparison is done by providing different different input voltages. According to the results of simulation adder of Chang is better as per as power dissipation is concerned while on the other hand Aguirre adder is best as it can even work at low power supply.

Moaiyeri M.et.al2009 [10]: In this paper 2 full adders are implemented using entirely new concept of majority not function. This function will be implemented with the help of static cmos inverter and capacitors.

This circuit design will make the full adder more simple & regular. Even this design will improve the performance of full adder and improve its capability of being driven. This design of full adder is tested in 0.18µm CMOS technology for 3 different input voltages. According to the simulation results this adder will be better as per as power dissipation and power delay product (PDP) are concerned.

Alioto M. et.al 2007[3]: In the case of cascaded full adders very high speed carry calculation is proposed in this paper. As compared to the traditional cascaded full adders in this paper implementation of adder is done by using transmission gate logic and mixed dynamic logic. According to analysis it is clear that with the addition of transmission gate full adders in between the dynamic full adders will not be going to violate timing constraints. For getting achievable performance comparison of conventional domino full adder chains and proposed technique is done. Without the degradation of energy and without any area constraint proposed approach is better than latter domino logic by more than 30% as shown from Post layout simulations in a 90-nm CMOS technology.

Tung C.et.al2007 [11]: In this paper new hybrid full adder is proposed having new 3 input XOR gate. This adder consists of static CMOS logic and pass transistor logic (PTL).Main motive of the design is high driving capability along with less power consumption and delay. Among other adders selected for comparison this circuit has fastest response of carry signal and minimum power dissipation. Because of low power and delay both XOR function and full adder can be incorporated in system on chip.

Chang C.et.al2005 [5]: Main motive of work is to look into PDP results and area of low voltage full adders in various CMOS logic designs for tree structured arithmetic circuits. This hybrid full adder can work on extremely low voltage. For improving the switching delay problem cogenerated XOR and XNOR modules are improved. At 0.18-µm CMOS process technology the circuits are optimized for energy efficiency. Proposed full adder exhibits strong drivability at output, full swing at output and even balanced outputs. Layout design is compact. So, this is best design as energy consumption is less and area is minimum.

Chang C.et.al 2003[4]: PDP is directly related to expenditure of energy per cycle of operation of arithmetic circuit. So, by reduction of input voltage PDP can be reduced. In this paper noble design of 1 bit full adder is implemented with by the generation of XOR & XNOR outputs at the same time along with circuit to restore the swing so that this circuit can even operate at ultra low voltage. This proposed circuit exhibits strong drivability, balanced outputs and full swing at output. Proposed circuit is better in terms of PDP and less amount of energy consumption.

Goel S. et.al2003 [6]: This paper is basically about new technique for designing a circuit that is tolerant to noise & can work at low voltage along with this energy efficiency should be maintained. Proposed circuit is more tolerant to noise and have less power consumption as well as PDP. Even it is more reliable and energy efficient. Even at input voltage starting from 0.6V to 3.3V the circuit proves to be faster and works successfully.

Tien Bui H. et.al2002 [7]: Using XOR & XNOR in addition to techniques that are already existing a new design of 41 new 10 transistor has been proposed inside this paper. Simulation is done using HSPICE.Almost all the adders newly proposed at high frequencies consume less power but 3 of them are very fast along with this they consume 10% power less when compared to 28 and 10 transistor CMOS adders. Main drawback in proposed full adders is loss of threshold voltage.

Wang J.et.al1994 [8]: Two new methods of designing XOR and XNOR circuits are discussed in this paper. The first method uses least no. of transistors but second one improves the performance by increasing no. of transistors. Simulation is done using HSPICE.

D.Radhakrishnan et.al2001 [15]: In this paper a new design is discussed having minimum number of transistors for XOR XNOR cell and having less voltage drop. Even when power

supply and voltage is reduced this circuit can work within certain limits. In this paper new design of XOR & XNOR for full adder is introduced with less number of transistors.

Vesterbacka M.et.al1999 [12]: In this paper a new design of 6 transistor XOR circuit is presented which is giving both the outputs at same time that is XNOR output in complemented form. Using this circuit 14 transistor full adder is proposed which exhibits full voltage swing. Layout is implemented inside 0.35μm technology. Simulation is carried out using HSPICE.

CHAPTER 5

EQUIPMENTS, MATERIALS AND EXPERIMENTAL SETUP

Cadence: The merger of Solomon Design Automation (SDA) systems and ECAD, Inc. founded Cadence Design Systems, Inc. in 1988. During the tenure of first CEO Joseph Costello, Cadence became the largest electronic design automation company producing software to design chips, PCBs as well as IP cores for memories, SoC, interfaces etc.Cadence products mainly focus on FPGA and ASIC designs for custom, analog, digital nand mixed signal applications.

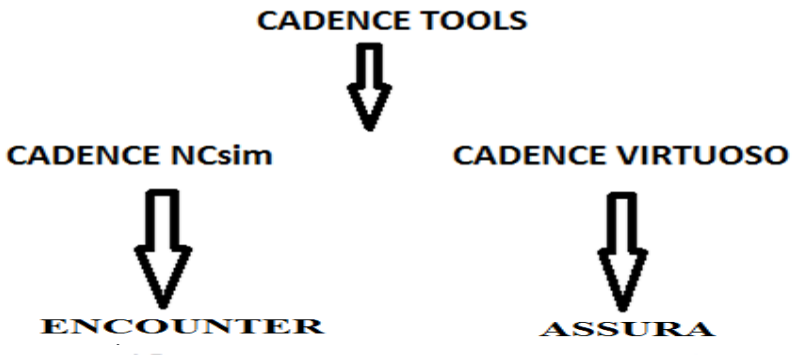

Figure 5.1: cadence tools

Among these tools cadence NCsim is basically for digital design and Cadence Virtuoso is for analog designing.

Cadence NCsim: This tool is basically used for digital design in which coding need to be done using Verilog language.In case of digital design first of all coding is done with tool such as Cadence NCsim then simulations will be done and then synthesis. Flow is simple: RTL,then gate ,then implementation.

Incisive enterprise simulator is widely used tool in digital design which is adding into technology to support the verification. It is being used for the verification purpose from system Level,RTL level & gate Level. This tool is used for simplification of effort during debugging and when it will make short the debugging time by separation of the design failure. Then it sorts and group these failures so that action & selection will be easy. For an SoC it supports mixed signal and low power debugging.

Tool used: Cadence virtuoso

Technology used: 180nm technology

Cadence Virtuoso: This tool is used for designing full custom integrated circuits that includes schematic design, behavioral modeling, simulation of circuit, layout designing, physical verification then extraction & back annotation. Cadence® Virtuoso® Analog Design Environment is an advanced design and simulation environment that gives the access to a new parasitic estimation designer. 180nm Generic Process Design Kit (GPDK180) has been used. A PDK contains the process technology and needed information to do device level design inside the Cadence environment.

CADENCE VIRTUOSO OVERVIEW

Schematic designing inside Cadence Virtuoso tool is very easy and fast that includes design assistants. At transistor and gate level well defined libraries for each and every component makes it fast. For the connection of various devices routing is possible. Even for complex and large designs hierarchy editor is their without any maximum number of levels used.

Features/Benefits

- Speed up design entries
- For maintaining consistency it enables the addition of design constraints into schematic design.
- Can check the circuit under various design conditions
- User friendly tool for execution of various commands.

Custom design flow

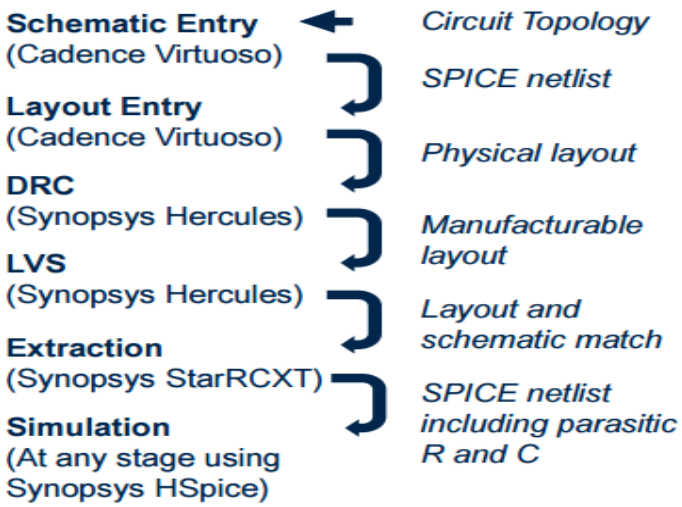

Figure 5.2: custom design flow

CHAPTER 6

EXPECTED OUTCOMES

In this implementation main expected outcomes are

- To minimize power.
- To minimize delay of the circuit.
- To make layout efficiently.
- To design energy efficient multiple bit adders.

CHAPTER-7

EXPERIMENTAL WORK

7.1. Design approach of proposed full adder

Basically full adder consists of 3 modules as shown in figure 7.1.Module 1 basically for implementation of XNOR circuit. Module 2 is for generation of SUM output using XNOR circuit whereas Module 3 is for carry generation.

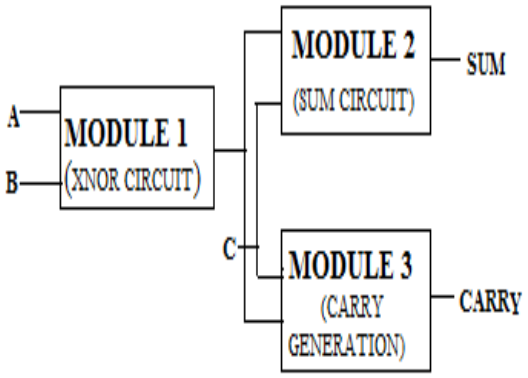

Figure.7.1. Schematic structure of proposed full adder

7.1.1. Design of XNOR circuit

XNOR module is main module of full adder. So, if power consumption of this module can be reduced then overall power consumption can be reduced. In this circuit basically XNOR circuit has been use implement the whole circuit. [1]

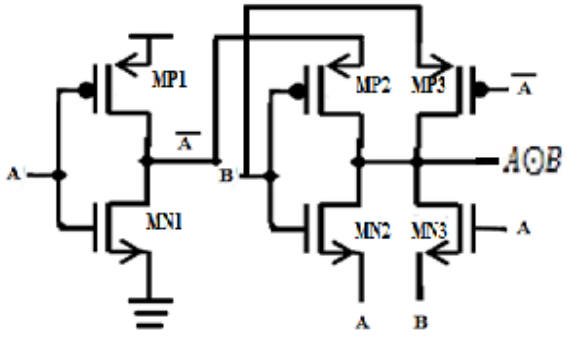

Figure.7.1.1 XNOR module

XNOR circuit is reduced by the use of weak inverters formed by transistors Mp1 and Mn1 as shown in *figure* 7.1.1.Even full output swing is guaranteed by Mp3 and Mn3 as shown in figure 7.1.1.Many topologies of XOR/XNOR circuit have been studied in [5] and [6]-[8]. In

this circuit basically XNOR module is implemented using modified form of PTL logic i.e DPL logic so that switching will be reduced and even power consumption will be less as compared to existing XNOR modules. Even after implementing XNOR module XOR can be implemented using inverter. This circuit is implemented in such a way so that output swing will be more.

- **Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit implementation.[1]**

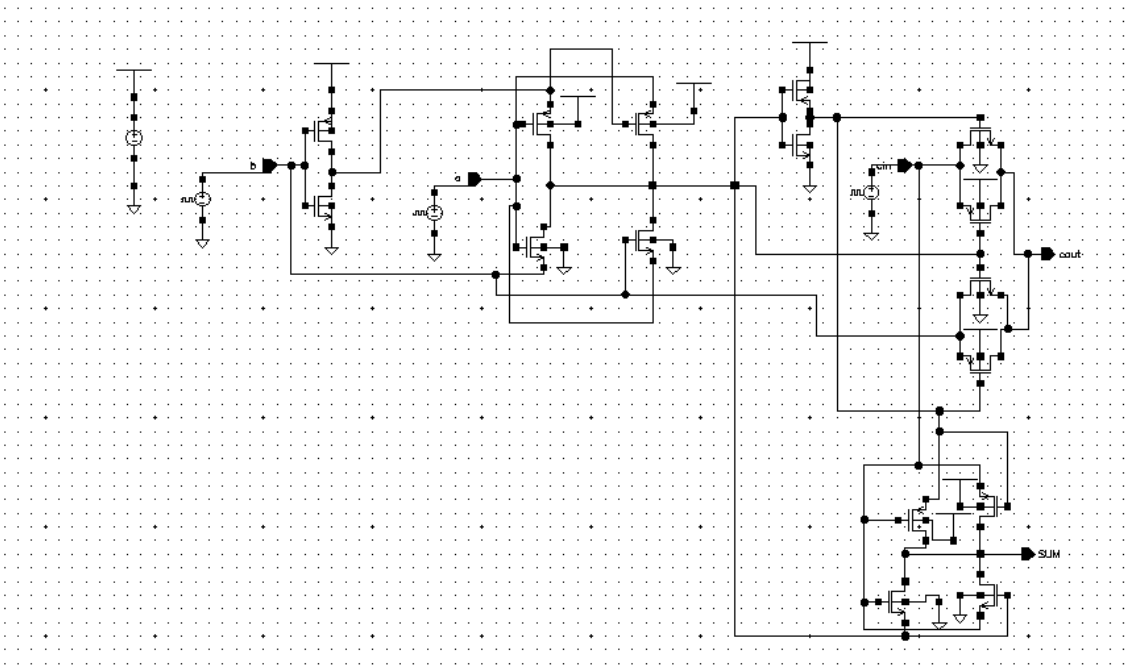

Figure 7.1.2: Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit implementation

Output after implementing given design is given below:

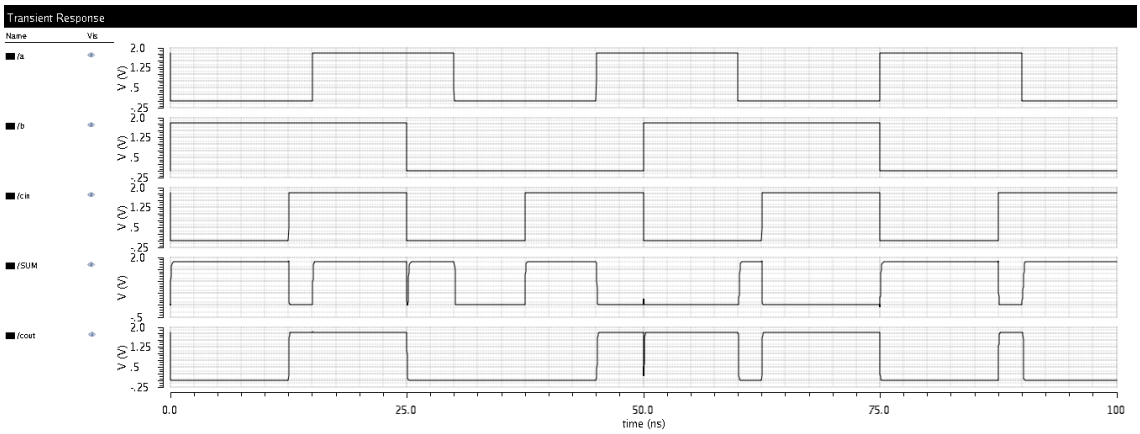

Figure 7.1.3: Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit output

7.2. After implementing this circuit a new circuit is proposed having modification in carry part.

In circuit proposed by bhattacharya basically modification in carry block is done to reduce the power consumption. In this circuit carry block is implemented by doing a change in the carry block. Carry block is implemented by DPL logic in a different way so as reduce the power consumption.

Table 7.1 : Carry implementation using XOR & XNOR

A	B	C	$\langle A \oplus B \rangle C$	$\langle A \odot B \rangle A$	CARRY
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	1	0	1	1

So, from *table 7.*1 it is very well clear that carry implementation can be done by addition of (A xor B) C and (A xnor B) A so it can be even implemented using DPL logic. So, in this way carry part can be modified.

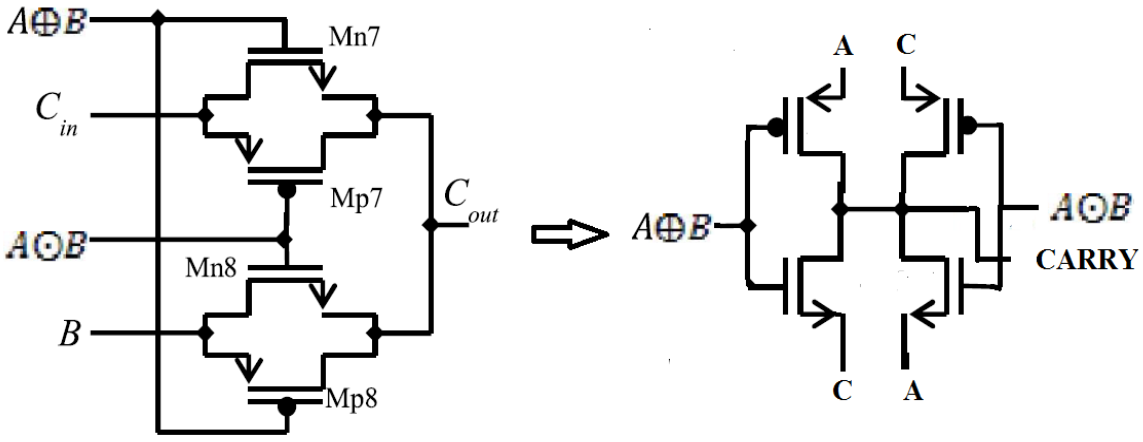

Figure 7.2.1: modified carry part

Implementation inside Cadence Virtuoso

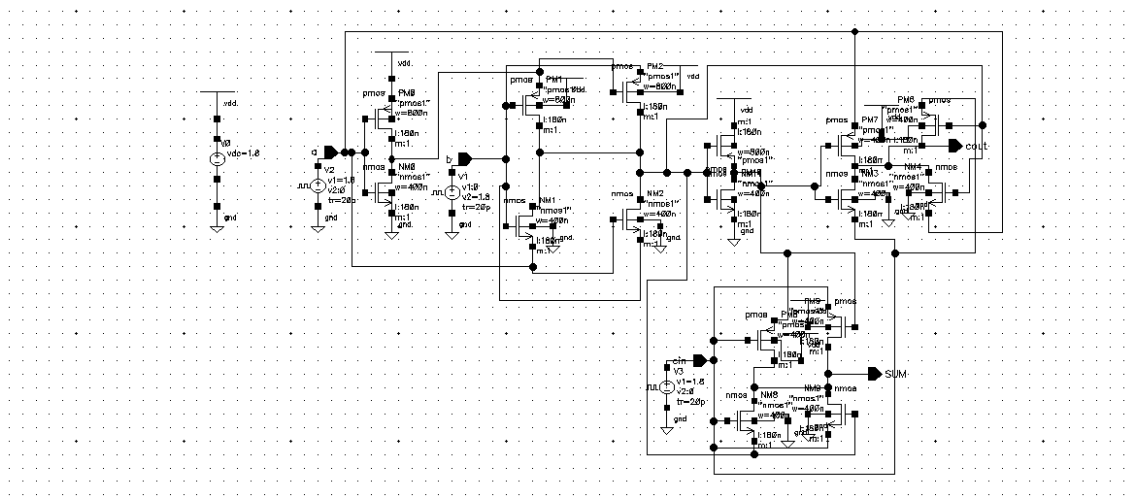

Figure 7.2.2: modified carry implementation in Cadence

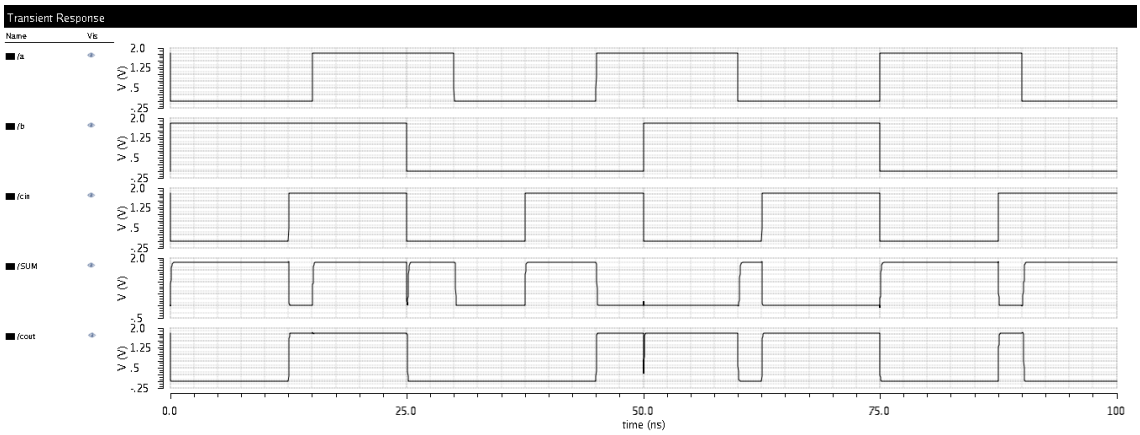

Figure 7.2.3: output after modifying carry part

7.3. After doing some change in xor circuit implemented in Cadence Virtuoso.

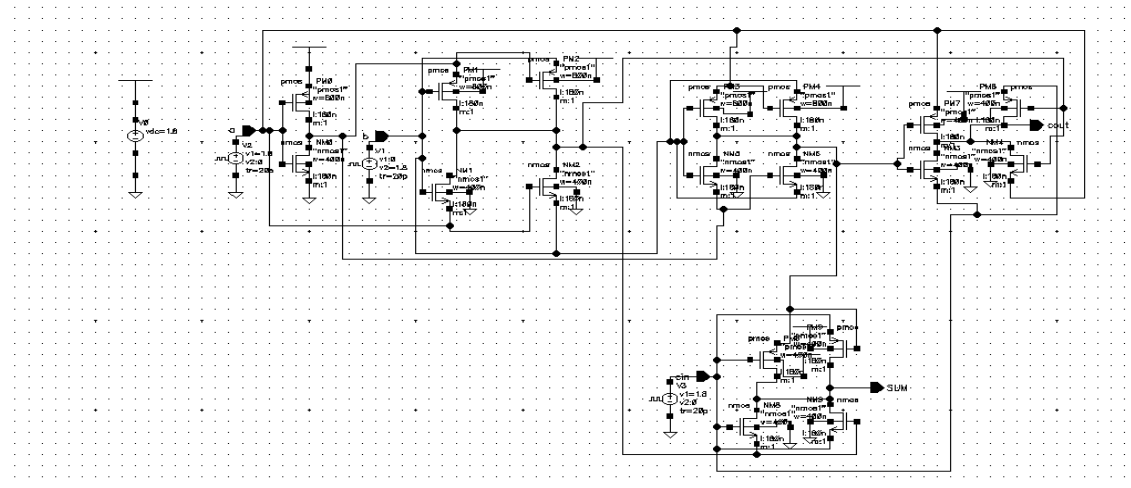

Figure 7.3.1: Schematic design after changing Xor circuit

Output after implementing circuit with modified xor circuit.

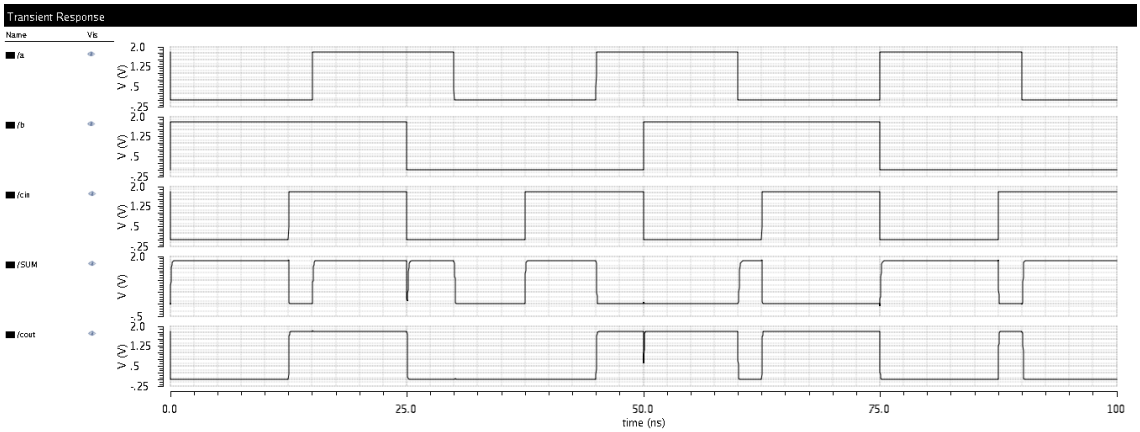

Figure 7.3.2: Output after implementing circuit with modified xor circuit.

7.4. Final optimized circuit with reduced power dissipation.

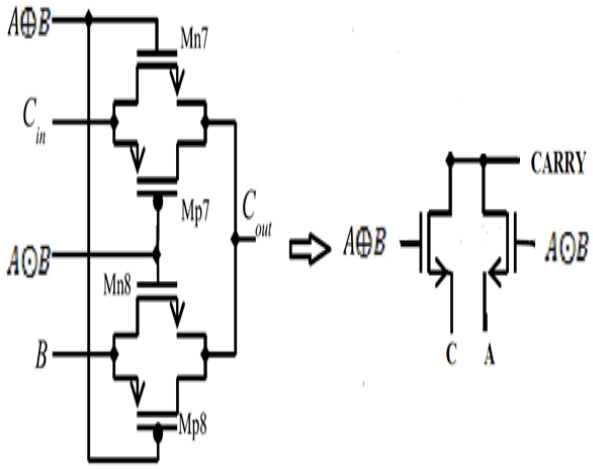

Figure.7.4.1 Modified carry generation module

This carry module is implemented by using a totally different logic as XNOR and XOR have already been implemented. As by multiplying (Axor B) with C and by multiplying (A xnor B) with input A carry part can be implemented using above given truth table. This circuit is implemented using PTL logic. So, in this way new carry generation module is able to reduce the power consumption as compared to existing designs. As power consumption of carry generation module is reduced in this way overall power consumption of whole circuit is reduced. Overall circuit with reduced power dissipation is given in *figure* no.7.4.2.

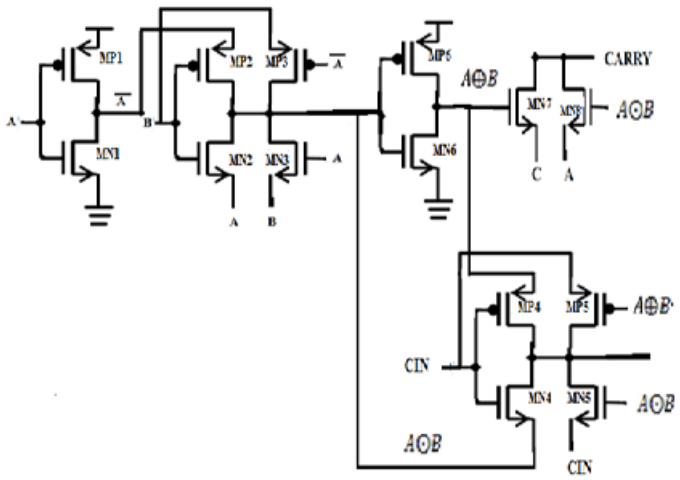

Figure 7.4.2. Detailed structure of proposed full adder cell

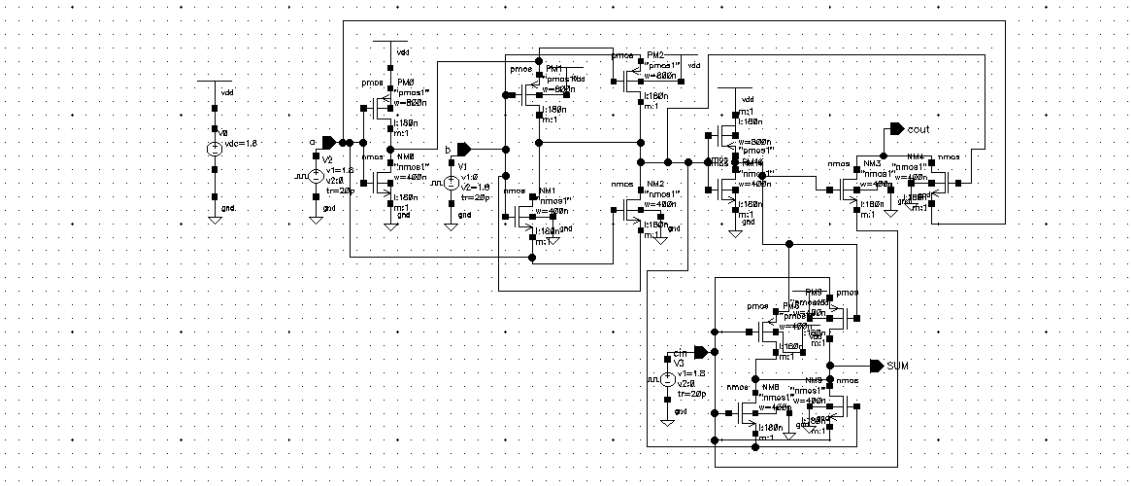

Figure 7.4.3: schematic of optimized circuit

Output of optimized circuit

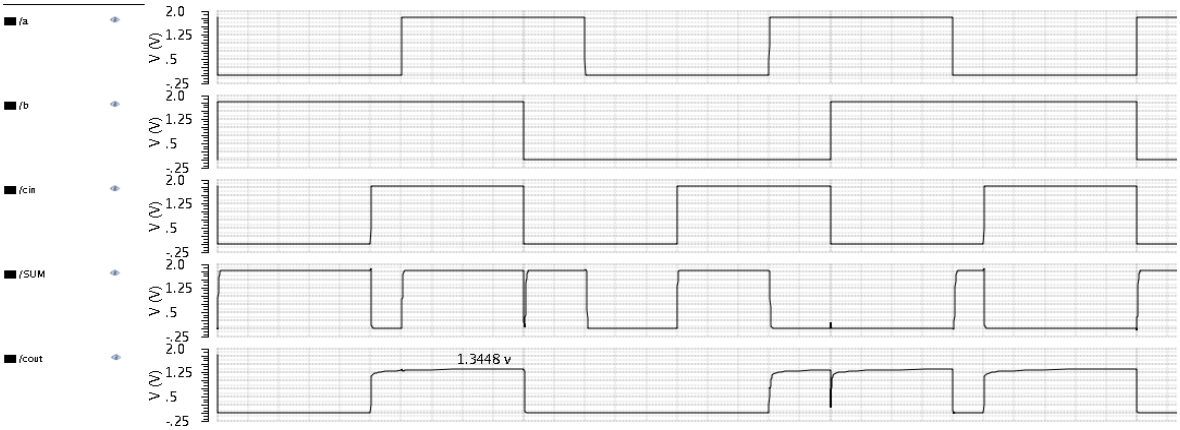

Figure 7.4.4: output of optimized circuit

- **Operation of proposed full adder**

Figure 7.4.2 represents the detailed structure of proposed full adder cell. Sum part of full adder is implemented using XNOR module. The inverter consists of transistors Mn1 and Mp1 will generate A' which can be used for the designing of the controlled inverter using Mn2 and Mp2.output of this inverter is XNOR of A and B. But because of the problem of voltage degradation Mp3 and Mn3 are introduced. Sum function implemented by second stage containing pmos transistors (Mp4, Mp5 and Mp6) and nmos transistors (Mn4, Mn5 and Mn6). Similarly carry is implemented by using nmos transistors (Mn6 and Mn7).Circuit given in fig.4 is implemented using 180nm technology in Cadence virtuoso.

Table 7.2: Transistor sizes of proposed full adder cell in 180 nm technology

Transistor name	Width(W)(nm)	Length(L)(nm)
Mn1,Mn6	400	180
Mp1,Mp6	800	180
Mn2,Mn3	400	180
Mp2,Mp3	800	180
Mn4,Mn5	400	180
Mp4,Mp5	400	180
Mn7,Mn8	400	180

7.5. Layout of proposed full adder design cell

Layout of proposed full adder circuit is made inside Cadence tool is as given in *figure* 7.5.After making layout DRC, LVS, RCX and RC extraction was done and this circuit is giving proper DRC, LVS, RCX and AV extraction.

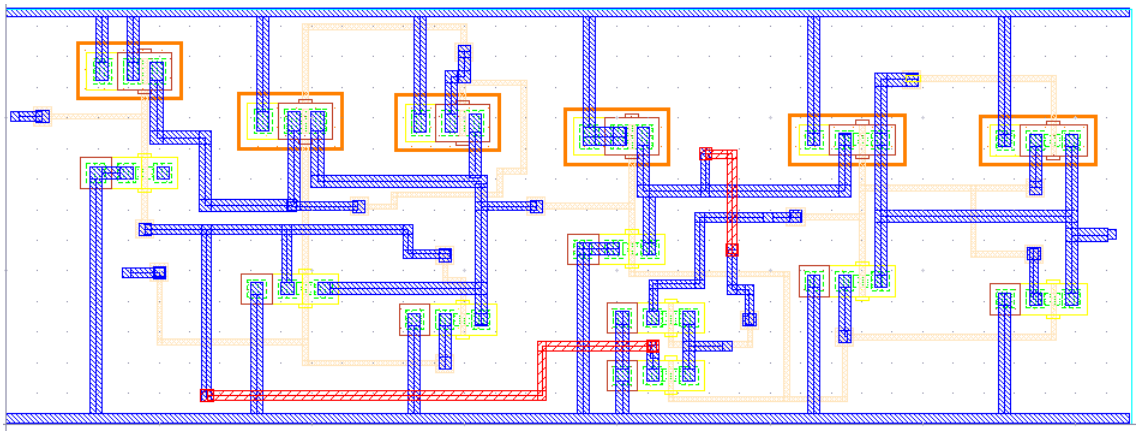

Figure 7.5 layout design of proposed full adder

Advantage of this layout over the already existing layouts is that in this layout only Metal 1 and a little bit of metal 2 is used. So, number of interconnects in this layout will be very less. Area of this layout design is 496μm^2. So, this circuit is better in terms of layout also.

7.6. Implementation of multiple bit full adders using optimized hybrid full adder

8 bit ripple carry adder,carry save adder and carry select adders are implemented inside cadence virtuoso using optimized 1 bit full adder.

7.6.1. Ripple carry adder

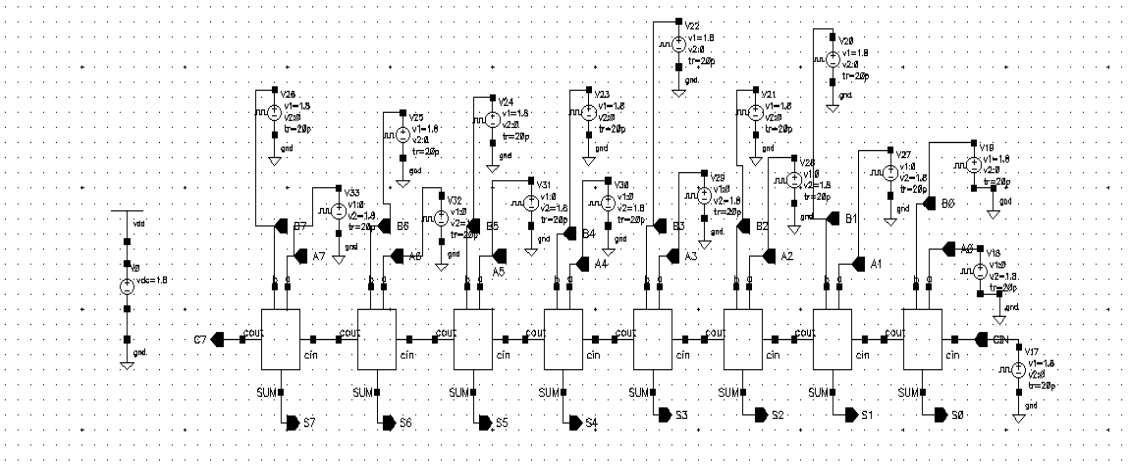

Figure 7.6.1: Ripple Carry Adder

7.6.2.Carry select adder

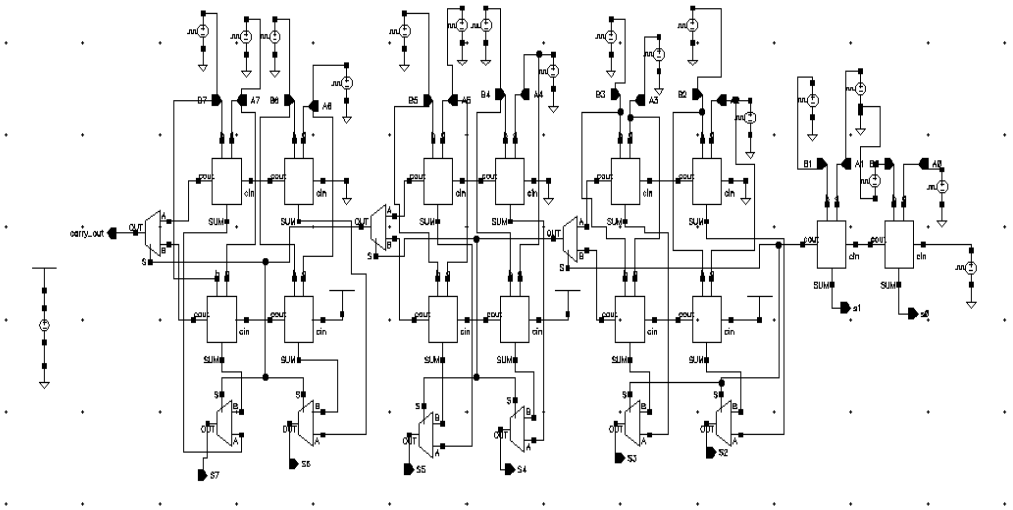

Figure 7.6.2: Carry select adder

7.6.3.Carry save adder

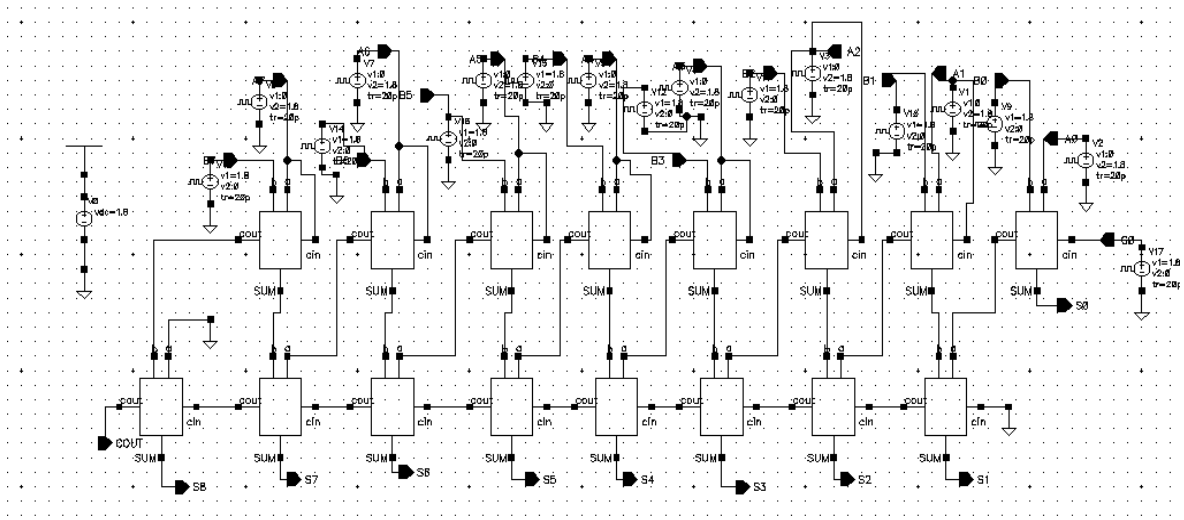

Figure 7.6.3: Carry save adder

CHAPTER 8

RESULTS AND DISCUSSION

Tool used: Cadence Virtuoso

Technology used : GPDK180 nm technology

First of all initial conditions for implementing all the circuits was kept same .In the starting bhattacharya paper was implemented and its analysis was done. Analysis of circuit given in *figure 7.1.2*.

Table 8.1: Input conditions for circuit in figure 7.1.2 i.e Bhattacharya circuit

VDC=1.8 V Overall time period=100 ns

Input signal B	Input signal A	Input signal C
Voltage 1 = 0 V	Voltage 1 = 1.8 V	Voltage 1 = 1.8 V
Voltage 2=1.8 V	Voltage 2 = 0 V	Voltage 2 = 0 V
Period=50 ns	Period=30 ns	Period=25 ns
Pulse width=25 ns	Pulse width=15 ns	Pulse width=12.5 ns

After doing its analysis outputs were noted down static and average power and PDP was calculated as given below**.**

Table 8.2 : Analysis of circuit given in figure 7.1.2 i.e Bhattacharya circuit

Static power consumption=496.7 pW average power consumption=3.996 µW

Delay calculation			Power delay product (PDP in feri)
Input	**output**	**Delay calculated**	**PDP**
A	sum	1.271 ns	5.041
A	carry	13.78 ns	55.10
B	sum	18.70 ns	74.72
B	carry	6.2535 ns	24.988
C	sum	47.25 ps	0.1885
C	carry	12.515 ns	50.01

After implementing bhattacharya circuit further carry part was modified by implementing carry part with DPL logic so that PDP can be reduced by keeping all the input conditions same. Analysis of circuit given in *figure 7.2.2* with modified carry logic.

Table 8.3: Input conditions for circuit in figure 7.2.2 i.e after doing modification in carry circuit

VDC=1.8 V Overall time period=100 ns

Input signal B	Input signal A	Input signal C
Voltage 1 = 0 V	Voltage 1 = 1.8 V	Voltage 1 = 1.8 V
Voltage 2=1.8 V	Voltage 1 = 0 V	Voltage 2 = 0 V
Period=50 ns	Period=30 ns	Period=25 ns
Pulse width=25 ns	Pulse width=15 ns	Pulse width=12.5 ns

Its static and average power consumption & PDP was calculated as given in table.

Table 8.4 : Analysis of circuit given in figure 7.2.2 i.e after doing modification in carry circuit

Static power consumption=528.5 pW **average power consumption=4.164 µW**

Delay calculation			Power delay product (PDP in feri)
Input	**output**	**Delay calculated**	**PDP**
A	sum	1.272 ns	5.296
A	carry	13.77 ns	57.338
B	sum	18.75 ns	78.075
B	carry	6.2539 ns	26.0412
C	sum	48.31 ps	0.2011
C	carry	12.515 ns	52.11

After implementing this modified circuit modification was done in Xor circuit instead of implementing Xor circuit from Xnor using inverter Xor was implemented using DPL logic and then its analysis was done.Analysis of circuit implemented in *figure 7.3.1*

Table 8.5:Input conditions for circuit in figure 7.3.1 i.e circuit after doing changes in xor

VDC=1.8 V **Overall time period=100 ns**

Input signal B	Input signal A	Input signal A
Voltage 1 = 0 V	Voltage 1 = 1.8 V	Voltage 1 = 1.8 V
Voltage 2=1.8 V	Voltage 1 = 0 V	Voltage 2 = 0 V
Period=50 ns	Period=30 ns	Period=25 ns
Pulse width=25 ns	Pulse width=15 ns	Pulse width=12.5 ns

Static and average power consumption was noted down and PDP was calculated which is given below.

Table 8.6 : Analysis of circuit given in figure 7.3.1 i.e circuit after doing changes in xor

Static power consumption=446.8 pW **average power consumption=4.28 µW**

Delay calculation			Power delay product (PDP in feri)
Input	**output**	**Delay calculated**	**PDP**
A	sum	1.271 ns	5.439
A	carry	13.765 ns	58.914
B	sum	18.745 ns	80.2286
B	carry	6.2549 ns	26.77
C	sum	53.45 ps	0.228
C	carry	12.515 ns	53.564

After doing analysis of all these circuits a final circuit with reduced power consumption was proposed after implementing carry part using PTL logic and its analysis was done. Analysis of circuit implemented in *figure 7.4.3*.

Table 8.7: Input conditions for circuit in figure 7.4.3 i.e implementation using PTL logic

VDC=1.8 V **Overall time period=100 ns**

Input signal B	Input signal A	Input signal C
Voltage 1 = 0 V	Voltage 1 = 1.8 V	Voltage 1 = 1.8 V
Voltage 2=1.8 V	Voltage 1 = 0 V	Voltage 2 = 0 V
Period=50 ns	Period=30 ns	Period=25 ns
Pulse width=25 ns	Pulse width=15 ns	Pulse width=12.5 ns

Static and average power calculation was done and PDP was noted which is given below.

Table 8.8 : Analysis of circuit given in figure 7.4.3 i.e implementation using PTL logic

Static power consumption=477.3 pW **average power consumption=3.617 µW**

Delay calculation			Power delay product (PDP in feri)
Input	**output**	**Delay calculated**	**PDP**
A	sum	1.271 ns	4.597
A	carry	13.77 ns	49.806
B	sum	18.745 ns	67.801
B	carry	1.251 ns	4.524
C	sum	46.965 ps	0.169
C	carry	12.52 ns	45.28

Analysis of multiple bit adders

After proposing a new hybrid full adder as shown in *figure 7.4.3* with reduced PDP.This circuit was used for implementing multiple bit full adders. Implementation of 8 bit ripple carry adder, carry select adder and carry save adder was carried out. Almost for all the

multiple bit adders initial conditions were kept same so that comparison can be done between different adders.

- **For Ripple carry adder**

Initial conditions for implementing ripple carry adder are as shown in table given below and its analysis was carried out. Static and average power consumption was calculated for this adder. Critical path for delay calculation was carried out.Input signals A0 = A1 = A2… were kept same. In the same way B0 = B1 = B2… were kept equal for analysis.Ripple carry adder is one of the basic adder among all of the multiple bit adders.

Table 8.9 : Analysis of ripple carry adder

Overall time period=10ns		
Input signal A(A0,A1……...)	**Input signal B(B0,B1,……...)**	**Input Signal Cin**
V1=0 V	V1=1.8 V	V1=1.8 V
V2=1.8 V	V2=0 V	V2=0 V
Time period=5 ns	Time period=4 ns	Time period=5 ns
Rise time=20 ps	Rise time=20 ps	Rise time=20 ps
Fall time=20 ps	Fall time=20 ps	Fall time=20 ps

Static power consumption=2.9104 nW

Average power consumption = 272.9 μW

Dynamic power consumption = 272.897μW

Critical path delay=2.1055 ns

- **Carry select adder**

Initial conditions for implementing carry select adder are as shown in table given below and its analysis was carried out. Static and average power consumption was calculated for this adder. Critical path for delay calculation was carried out. Input signals A0 = A1 = A2… were kept same. In the same way B0 = B1 = B2… were kept equal for analysis. Rest Cin signals will be same as that of input signal like Cin1=A1,Cin2=A2 and so on. In case of carry select adder delay will be minimum as in this case we try to select the carry with help of mux.

Table 8.10 : Analysis of carry select adder

Overall time period=10ns		
Input signal A(A0,A1……...)	**Input signal B(B0,B1,……...)**	**Input Signal Cin**
V1=0 V	V1=1.8 V	V1=1.8 V
V2=1.8 V	V2=0 V	V2=0 V

Time period=5 ns	Time period=4 ns	Time period=5 ns
Rise time=20 ps	Rise time=20 ps	Rise time=20 ps
Fall time=20 ps	Fall time=20 ps	Fall time=20 ps

Static power consumption=5.51121 nW

Average power consumption = 1.184 mW

Dynamic power consumption = 1.1 mW

Critical path delay=1.8935 ns

- **Carry save adder**

Initial conditions for implementing carry save adder are as shown in table given below and its analysis was carried out. Static and average power consumption was calculated for this adder. Critical path for delay calculation was carried out.Input signals A0 = A1 = A2… were kept same. In the same way B0 = B1 = B2… were kept equal for analysis. This adder will used to reduced the no. of computations.

Table 8.11 : Analysis of carry save adder

Overall time period=10ns		
Input signal A(A0,A1……...)	**Input signal B(B0,B1,……...)**	**Input Signal Cin**
V1=0 V	V1=1.8 V	V1=1.8 V
V2=1.8 V	V2=0 V	V2=0 V
Time period=5 ns	Time period=4 ns	Time period=5 ns
Rise time=20 ps	Rise time=20 ps	Rise time=20 ps
Fall time=20 ps	Fall time=20 ps	Fall time=20 ps

Static power consumption=5.82 nW

Average power consumption = 582.6 µW

Dynamic power consumption = 582.5µW

Critical path delay=5.8005 ns

Delay for carry select adder is minimum while on the other hand average power consumption for ripple carry adder is minimum because of less number of transistors used in case of ripple carry adder.

CHAPTER 9

SUMMARY AND CONCLUSION

From experimental work and its analysis it is clear that the last circuit i.e circuit in figure 7.4.3 with 2 transistors in carry part is best as per as power dissipation is concerned. So, in that case PDP will also be less as compared to remaining adders. But in that case voltage drop is there that will be future work to be solved. This circuit is working for different supply voltages from 1.25V – 1.8V.

Table 9.1: Comparsion result of already existing full adders with proposed adder

Design	Average power consumption (μW)	Transistor count
Bhattacharya	4.1563	16
CPL	7.17985	32
TFA	8.2491	16
TGA	8.4719	20
14 T	12.7217	14
10 T	14.3449	10
HPSC	6.3798	22
Majority based	6.3227	__
24T	15.91	24
FA_HYBRID	5.978	24
FA_DPL	19.56	22
FA_SR-CPL	20.78	20
Proposed	3.617	14

Proposed layout will be better as compared to already existing layouts. Advantage of this layout over the already existing layouts is that in this layout only Metal 1 and a little bit of metal 2 is used. So, number of interconnects in this layout will be very less. Area of this layout design is $496\mu m^2$. So, this circuit is better in terms of layout also.

Among multiple bit adders each adder has certain advantages and disadvantages so according to requirement we will be going to choose one particular adder according to application in which it is required.

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