DESIGN AND IMPLEMENTATION OF BAUGH-WOOLEY MULTIPLIER USING QCA

DISSERTATION-II

Submitted in partial fulfillment of the
Requirement for the award of the

Degree of

MASTERS OF TECHNOLOGY
IN
Electronics & Communication Engineering

By
Damodar Krishan
11001574
Under the Guidance of

Mr. Rajkumar Sarma
Assistant Professor
SECE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINNERING
LOVELY PROFESSIONAL UNIVERSITY
Phagwara-144411, Punjab (India)
APRIL 2015

PAC form

CERTIFICATE

Certified that this Dissertation-2 Report entitled "**Design and Implementation of Baugh-Wooley Multiplier using QCA"** submitted by **Damodar Krishan** having registration number **11001574,** student of Electronics and Communication Engineering Department, Lovely Professional University, Phagwara, Punjab in the partial fulfillment of the requirement for the award of Masters of Technology (Electronics and Communication Engineering) Degree of LPU, is a record of student's own study carried under my supervision and guidance.

This report has not been submitted to any other university or institution for the award of any degree.

Name of Supervisor

ABSTRACT

In this Thesis we focused upon the Design and Implementation of 8-bit Baugh-Wooley multiplier in Quantum Cellular Automata (QCA). And the tool for this purpose was QCA 2.0.3 which was designed by researchers of British Columbia University. We start with the design of various regular basic gates in Quantum logic using Inverter and Majority Voter (MV) or Majority gate like NAND, NOR, XOR, NOT and some combinational circuits like Half Adder, Full Adder et al. designed in QCA tool. Than we start with the design and analysis of Baugh-Wooley multiplier with its basic literature review and its Mathematical calculation for 8-bit multiplier. It can be observed that the circuit consists primarily of several full-adders so a good full-adder solution in QCA directly contributes to the efficiency of the Baugh-Wooley multiplier. A full-adder can be realized in QCA with three majority gates and one inverter. Finally we design in QCA and analyze the simulated result for the trade-off such as Area, Clock delay, Cell count etc. The design was found to be efficient than the existing design of multiplier.

ACKNOWLEDGEMENT

I am grateful to Lovely Professional University for giving me an opportunity to be involved in such kind of Thesis work. This subject allowed me to implement all my learning and knowledge skills which were quite interesting.

I have taken efforts in this Dissertation-II report. However, it would not have been possible without the kind support and help of many individuals and organization. I would like to extend my sincere thanks to all of them.

I am highly indebted to Mr. Rajkumar Sarma for his guidance and constant supervision as well as for providing necessary information regarding the report, research work & also for their support in completing my Dissertation-II.

We would like to express our gratitude towards our parents & member of lovely professional university for their kind co-operation and encouragement which help us in completion of this.

We would like to express our special gratitude and thanks to all our friends for their support.

Damodar Krishan

11001574

DECLARATION

I hereby certify that the work, which is being presented in the report entitled "DESIGN AND IMPLEMENTATION OF BAUGH-WOOLEY MULTIPLIER USING QCA" in partial fulfillment of the requirement for the award of the Degree of Masters of Technology submitted to the institution is an authentic record of my own work carried out during the period January 2015 to April 2015 under the supervision of Mr. Rajkumar Sarma.

Damodar Krishan
Date: April 2015
11001574 Signature of student

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CHAPTER 1
INTRODUCTION

1.1 Overview

In VLSI system the energy proficient multiplier plays a vital role as with the increasing requirement for computing as well as communication system. For the multiplication of two's complement numbers, the primary multiplier either follows the concept of Baugh-Wooley or the Booth multiplication algorithm [2]. As the DSP algorithms like DCT, digital filters and wavelet transformation all these work under the concept of point-to-point multiplication along with fixed-width and getting the least fault n-bit output of the n x n multiplier can be generated [3]. When the fault compensation is let off then faults are being executed by the past methods. In current scenario some new techniques are formulated for achieving the parameters as least error and low area. Where, in the minimization and approximation of faults are taken into account individually such that the compensation bias would not be enough to generate error [1].

Algorithms such as FIR, IIR and FFT are required DSP based calculation which solely depends on the design of the multiplier and these are the standard sub-parts of digital processors and also used in ASIC based DSP processors. As many DSP based task which works in real time need to perform multiple tasks in a fast manner with the demise in power along with area [2]. Since due to time complexity the array multiplier has effected from delay having large size of operand and with the complexity in space of $O(n^2)$, and requires n2 cells for multiplication and the result will increase in size and power for large operands [2]. As Wallace tree multiplier has a drawback as hardware complexity, need large routing area. So, this technique is not apt for VLSI Design of multipliers [2]. The core use of demise in hardware with Booth can be recombine with Wallace tree for product of half-done and also shrinks the complexity in time of O(log n). For large number of operands, it is the good choice [2].

Digital multiplier plays an important role in micro controllers and digital signal processors (DSP) which has the MAC (Multiply and Accumulate) unit. As DSP structures seldom need multipliers of differ in size. A generic HDL code is useful to prove these structures. By using this method,

the designers can conceive different multipliers of different size by simply changing the operand size factor. The Baugh Wooley multiplier is signed multiplier which takes continuous bits with produce low delay. Gathering all these parameters, this method multiplier is used for continuous results with less complexity, interconnections [3]. A ripple carry adder is required in last stage of Baugh Wooley multiplier design.

1.2 Multipliers

In present scenario, multipliers are playing crucial part in digital signal processing and in many real time applications. As upgrading the technology, researchers involved to design the better multipliers which provide efficient improvements in high performance, near to zero power consumption, minimized area, and regularity of outline.

The method which has the operation as first add and then shift is the basic multiplication algorithm. To determine the work flow of the multiplier in parallel configuration, the half done products added to the basic parameters. To reduce the no of added half done products, Modified Booth algorithm is efficient algorithm. Mainly to improve the speed, reduce the sequential adding stages number Wallace Tree algorithm is used. To get more advantages in different parameters need to club the both Modified Booth and Wallace Tree algorithms for a single multiplier. As parallelism enhance then the how many shifts changes between the half done products and middle sums added. It improves in performance, complexity of silicon area due to irregular design, more power consumption due to interconnections or routing.

1.2.1 Serial Multipliers

In every circuit area, power, and delay are utmost important parameters and these all are must be in low. Similarly serial multiplier also used to tolerate the parameters in processors. In the design of serial multiplier, it requires single adder to sum the all partial products of m*n. As shown in figure.1. The multiplicand and multiplier inputs are arranged continuously. Here inputs can manage the both multiplicand and multiplier at different data depending on the length. In this figure, the data and reset can be initiated with two clocks. Since the first order delay for the circuit can be estimated though O(m, n) and is given by:

$$D = [(m+1)n+1]t_{fa} \tag{01}$$

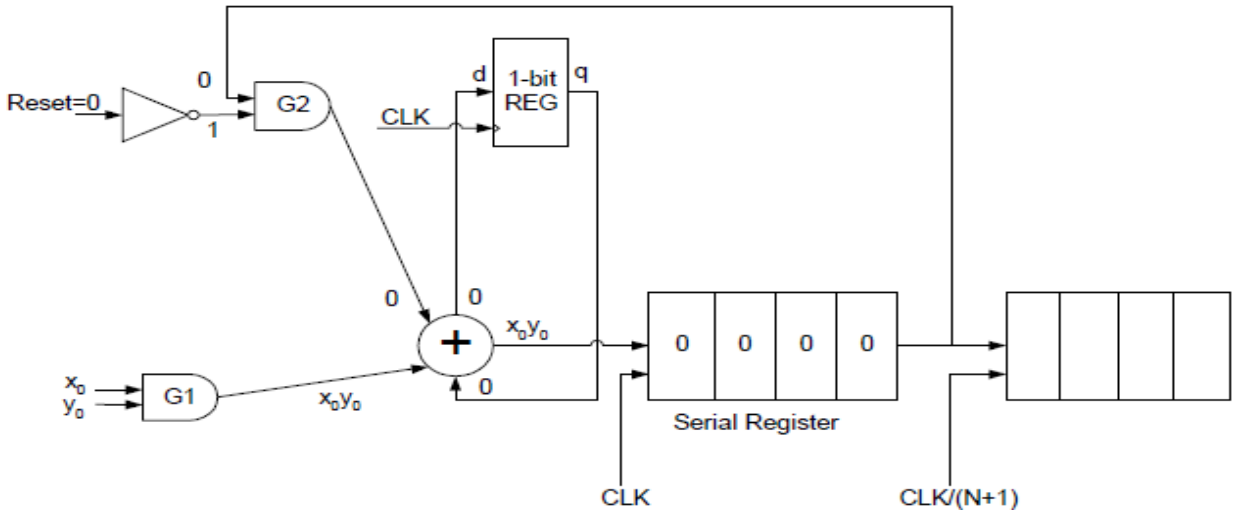

Fig.1.1. Design of Serial Multiplier

1.2.2 Serial/Parallel Multipliers

The essential approach for serial/Parallel multiplier circuit is represented below the figure.2. In this the multiplier recognizes the signed or unsigned 2's complement numbers and produce them. As in figure, the input y data is functioned in parallel and bit serial can be performed for multiplication. And x data is feed across the multiplier for serial operation. For each and every cycle N numbers of partial products are generated. For each successive cycle, each bit is added to the m*n partial products. The overall outcome accumulated after the n-m cycles, the needed area is n-1 for equal number of M-N. The advantage in hardware of this multiplier is compare to Baugh Wooley multiplier.

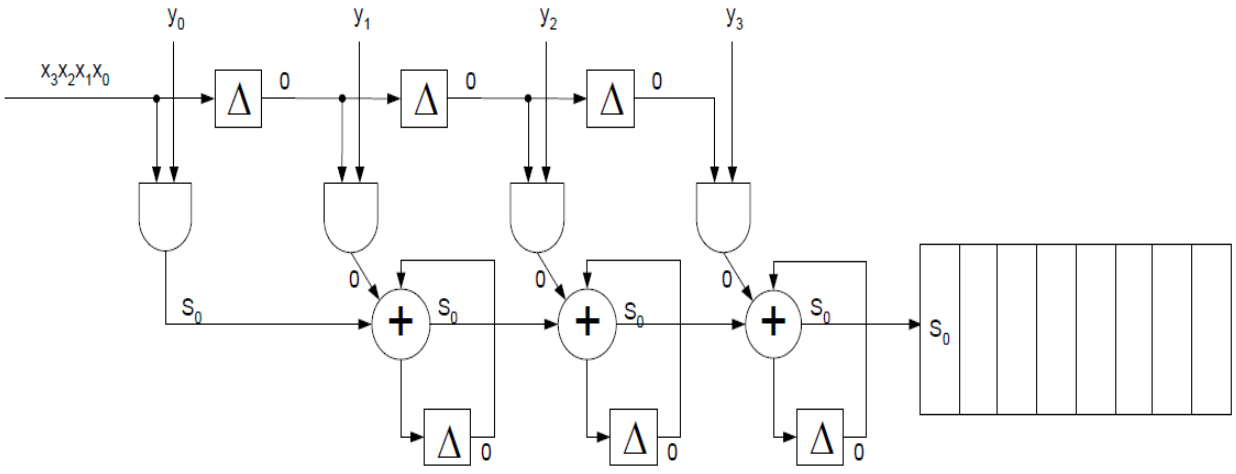

Fig.1.2. Design of Serial/Parallel Multiplier

1.2.3 Shift and Add Multipliers

The architecture represents the 32 bit Shift and Add multiplier for Multiplication of 32 bits. Depending on LSB Bit of multiplier, for every continuous clock, the bits of multiplier succeed to right and checked. If LSB bit is logic one then it acts upon shift operation. And its value is one then multiplicand is further added to accumulator after that succeeded to right for one bit. After the all 32 bits operation over then the multiplier bits are checked and product to accumulator. The size of accumulator is 2N (M-N), multiplier has N is initially in LSB. In asynchronous circuits, multipliers have more improvements.

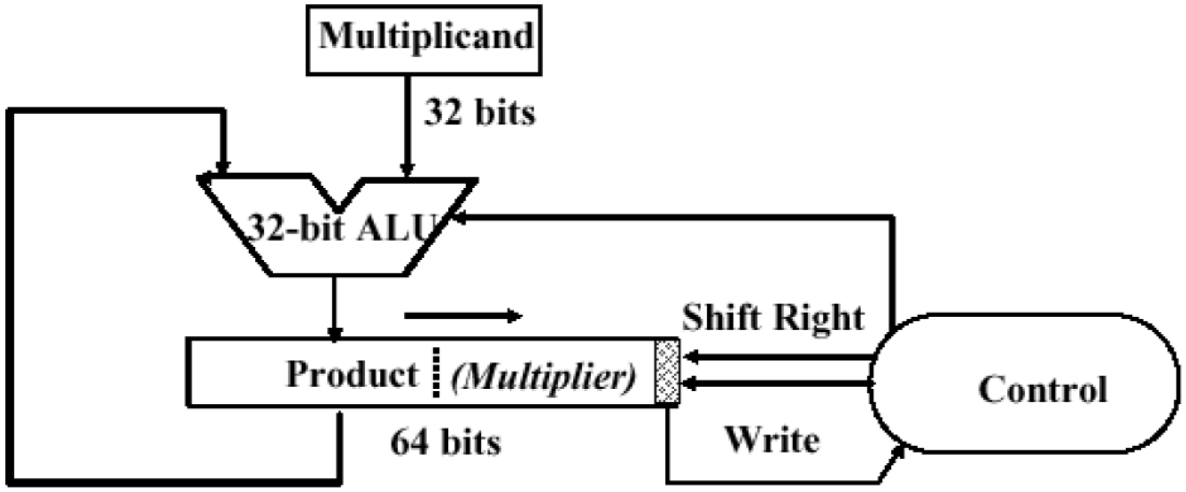

Fig.1.3. Design of Shift and Add multiplier

1.2.4 Array Multipliers

The eminent design of Array multiplier is a regular circuit structure. This Multiplier architecture is entirely base on Add and shift algorithm. Every single half done product is formed by the multiplicand and one of the multiplier bit's multiplication. Each and every half-done product is labeled as per their bits order and then after joined them. In this, addition can be accepted with simple carry and it can be done by using adder. For N bits length of multiplier need N-1 adders to multiplication process.

				A3	A2	A1	A0	Inputs
			x	B3	B2	B1	B0	
			C	B0 x A3	B0 x A2	B0 x A1	B0 x A0	
		+	B1 x A3	B1 x A2	B1 x A1	B1 x A0		
		C	sum	sum	sum	sum		
	+	B2 x A3	B2 x A2	B2 x A1	B2 x A0			Internal Signals
	C	sum	sum	sum	sum			
+	B3 x A3	B3 x A2	B3 x A1	B3 x A0				
C	sum	sum	sum	sum				
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Outputs

Fig.1.4. Basic Algorithm of Array multiplier

Up to now, there are different algorithms of array multipliers are available and hose main architectures are like Booth multiplier, Wallace-tree multiplier, Modified Booth multiplier and the Baugh-Wooley multiplier.

1.3 Baugh-Wooley Multipliers

The algorithm which is having array multiplication for two's complement bits is Baugh and Wooley. The focal point of this multiplier is the sign bits of all the multiplicand and multiplier is unsigned or positive. This algorithm is completely designed by using the conventional logic full adders. Here two's complement numbers multiplied and then finally we get the products as (p0 – p6). The multiplication proposes of Baugh- Wooley Multiplier approach is represented below.

TABLE 1.1. Baugh-Wooley multiplier for 4X4 bits

				a_3	a_2	a_1	a_0
			x	b_3	b_2	b_1	b_0
			1	$\overline{a_3b_0}$	a_2b_0	a_1b_0	a_0b_0
			$\overline{a_3b_1}$	a_2b_1	a_1b_1	a_0b_1	
		$\overline{a_3b_2}$	a_2b_2	a_1b_2	a_0b_2		
1	a_3b_3	$\overline{a_2b_3}$	$\overline{a_1b_3}$	$\overline{a_0b_3}$			
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

CHAPTER 2
REVIEW OF LITERATURE

2.1 International Papers

Rui Tang et al. 2005 [4] talks about how the wide digital circuits can be designed through QCA cells and predicts the QCA design style for circuits is depend upon the regular CMOS style of circuits design. The primary layout steps for QCA are composed of inserting the QCA to the available four clock zones and that to be suitable for these cells. Also circuit size is comparable to full adder there is requirement of at least four clocks which make that QCA circuit to operate properly. In QCA four clock zones are discussed:

1. Switch Phase
2. Hold Phase
3. Release Phase
4. Relax Phase

Depending on the clocking in these four zones each cell in a particular zone have same clock for that zone only. The signal which travels from one zone to any other zone successively shows a phase shift of 45 degrees. Also the delay of the complete circuit can be determined through the frequency of the clock. In a present QCA instrument there is a wire channel which is upto three cells whereas the MV takes upto a cell count of five. In this paper a design path for QCA circuits which depends on the regular design way for CMOS. The concerned design in this will enhance the speed and aid up into the design of wide digital circuits which is based on QCA.

Heumpil Cho et al. 2006 [5] discuss about electronic circuits depend upon the QCA technology. It has benefits such as high speed with a small dimension provide a good indication of the upcoming future gadgets which depend on this technology. The circuit designers utilize its simple as well as unique arrangement for deliberating a circuit at the structure level act as alternative for the CMOS level. In this paper author propose about the functional design of a RSA within QCA for comparisons. The layout can be made with different size of operand in the QCA designer. All the design should compare with the ripple carry adder as well as CLA adder on the trade-off such as area, complexity along with timing constraint. Instead large designs of

CSA provides a good solution for the trade-offs in between the complexity and the speed. The last designs display the functional along with stretchy design of a CSA. The parameters which supports the bistable simulation are the samples number = 102400, union tolerance is 0.001, radius of effect is 41nm, relativity permittivity is 12.9, clock high = 9.8E-22, clock low=3.8E-23, clock amplitude factor=2, layer separation=11.5nm, maximum iterations per sample=100.

Mehdi Askari et al. 2008 [6] also shows that an alternative to CMOS VLSI is found to be the Quantum-Dot Cellular Automata (QCA) and that is currently in investigation. It has benefits like sleek size, fast speed with lesser utilization factor are very effective from performance point of view. As in the formal computers in which data is being transmitted from location to location through electrical current, the QCA utilizes the method of split state for propagation of information. In this paper, the author proposed a design for examination of the circuit which is in chronological ring order in QCA. The objective is to allow the most use of any circuit for its compactness while considering its layout for the minimal use of the cells.
Every new QCA circuit require a clock not for synchronization and flow of information but in reality it outflow with the sufficient power to run and enable the design. In this working of clock can be improved through control of barriers which is in between the every adjacent quantum dots. After all the clock phases, the polarization of each QCA cell is getting demise upto when another switch phase actives due to the polarization of its neighbors.

Heumpil Cho et al. 2009 [8] showed that QCA is a new growing technology having the specification consisting of faster speed , lower power and the smaller size as compared to transistor based technology. The basic element of Quantum-dot cellular automata is the qubit cell. This work will enable the design trade-offs and are separated in QCA. In this paper author uses the QCA designer to implement a Carry Flow Adder (CFA) which is fast and proficient. To construct the wires, crossover and the gates, the construction block is a QCA cell. Recently, adder architectures which is based on regular designs were taken into account for execution and the simulation shows a attractive recital in terms of delay, areas as well as complexity. In this paper author also explores about serial multipliers and also a serial-parallel multiplier is simulate with varying size of operand.

Lee Ai Lim et al. 2012 [9] discuss that the aspect ratio of CMOS transistor keep reducing and finally it will target its limit of operation. Then the Quantum-dot cellular automata (QCA), is composed of that potential which will be used to assign to the digital circuit. Here, the author represents the basic phenomenon of the QCA cell theory along with some essential architectures of the QCA scheme. Therefore a substitute device needs to be invent, so that it improves the electronic devices expansion.

In any QCA design, the clocking is considered to be an important part in both the combinational as well as chronological circuit design. To allow the data bits to flow from one end to another end of the wire QCA uses the clocking method. As in electric transmission system there must be a sort of power loss when the electricity is need to be transferred from one portion to the other portion fo the wire and this sort of phenomenon also happen in the QCA single spread. So, in order to neglect this process of information loss , the signal needs to be get restored after every time duration. For any QCA design the energy which stores back the signal information occur from the clock and this clocking should apply to the QCA cells for the original power gain at every stage.

Kim A. Escobar et al. 2013 [10] projected that the Quantum-dot cellular automata (QCA) represents a very promising rising technology, which has been claimed to be faster and smaller than the most traditional CMOS technology. In the last years, significant advances have been made in QCA designs, since the opening of basic logic gates until the insertion of more complex circuits, like adders. However, new paradigms and challenge have emerged in this sense. The implementation of the basic blocks necessary to build corresponding prefix adders (PPAs) is existing in this work. These blocks have been evaluated and validated through the construction of a 4-bit PPA. The proposed adder discharge is compared to other QCA adders offered in the literature.

2.2 National Papers

Kunal Das et al. 2009 [7] planned that Quantum dot cellular automata (QCA) define the nano structure of a basic computer. It is used as another for designing high-speed computer over CMOS equipment. The basic logic in QCA is the logic state that does not measure with voltage

level; rather it measures the polarity of electrons in cell. The greater part Voter (MV) is first introduced to design the logic circuits, but only using MV, deceitful complex logic circuit became inefficient. Many proposal had been made for designing QCA logic gate. In this paper we focus on Novel nanostructure, reduced size and efficient design of "And-Or-Inverter" (AOI) and also present association with previously reported AOI gate. We design New AOI gate using a combination of Nand-Nor-Inverter (NNI) and MV. recreation result shows almost 54% reductions in size of AOI gate and improving gate delay due to less complication on compare to early report. We analyze QCA defect on proposed AOI gate and depict its permissible defect tolerance. We also depict NNI with its QCA nano constitution.

CHAPTER 3
PRESENT WORK

3.1 Performance Factor

The concept of multiplication came into existence some decades back and in correspond to that the multiplier also which perform this task of multiplication. Early research conclude that multiplication consist of periodic utilization of the ALU based full adder. Some new multiplier were interacted like array multiplier as the constraint of timing with the need of clock rate improvement. Since then only new ways are predicted for more complex multiplication [11] and the popularity achieved by modified-booth scheme which results in logarithmic depth tree reduction along with fast adder. As it has feature of demise the quantity of partial products to half when compared with half-done product terms that depends on AND gates. Because of this reduction circuitry size can be diminished which are nothing but a logarithmic depth reduction tree. Due to unordered growth, these kind of reduction trees was not so much popular as it is very hard to place them in the physical outlining of an multiplier. Only the reduction circuit causes the ease in execution along with improvement in multiplier presentation.

As the current leakage and for that loss of power is a important concern in the implementation strategy of the modified-booth, since it is provoked when there is requirement for quick multipliers. But with the concern of power it is not a good choice for implementation. Than in 1997 Callaway demonstrate that Wallace multiplier is a better choice as compared to modified-booth in terms of energy proficiency [11]. Even also power was the major concern, for high speed multipliers customized booth was still the core choice of implementation. Than the Baugh-wooley came into picture with better energy and power proficient as compared to above multipliers in a 130nm and 65nm technology. This kind of feature occurs due to only raise in delay parameter.

The signed multiplication in which bits of half-done products is simplified is achieved through Baugh-Wooley algorithm. It contain mainly of the following three steps:

1. The MSB of first N-1 half done product rows and similarly every bit of last half done product row except its MSB are flipped or upturned.
2. Single ‘1’ is need to be added at the N^{th} column.

3. The MSB of the ultimate bit is upturned

TABLE 3.1

Delay, Power, Energy and Area for 32-Bit Baugh-Wooley and Modified-Booth Multipliers in a 65-nm Process [11]

	Delay (ns)	Power(mW)	Energy(pJ)	Area(μm^2)
Baugh	2.59	23.4	60.6	48.1k
Booth	2.50	37.5	93.8	52.1k

TABLE 3.2

Delay, Power, Energy and Area for 32-Bit Baugh-Wooley and Modified-Booth Multipliers in a 130-nm Proces [11]

	Delay (ns)	Power(mW)	Energy(pJ)	Area(μm^2)
Baugh	3.63	7.81	28.4	88.8k
Booth	3.68	9.74	35.8	108.9k

3.2 Objective of the Study

Since last decade is a decade of production in the field of nano-electronics as many new gadgets for the study commune are being developed. As it consider the alternative field of research as compared to CMOS based traditional VLSI technology. For the digital purpose Quantum Dot Cellular Automata was one of rising concept in nanotechnology field. Since the interrelate is also based on the gadget which is utilize for logic in QCA. The majority gate also called as majority voter along with the inverter are the most used basic gates in QCA. For the proficiency in arithmetic circuits using QCA consist of designs of numerous type of adders as well as multipliers [8]. Serial-parallel multipliers also get affected through QCA based multiplier. Although short latency along with small area for signed multipliers are scarce but it targeting by QCA to achieve this features. Here, we tend to discuss the regular multiplier namely Baugh-Wooley multiplier for two's complement numbers and it ought to give an very efficient design with QCA tool for some new results. And any proficient full adder can work and allow the multiplier to be benefitted.

3.2.1 Quantum Logic in Baugh-Wooley

From the last decade, QCA was found to be very interesting in the digital system design and with low area and latency; past work is restricted for signed multipliers. Here we focus on the

efficient design of the Baugh-Wooley multiplier in QCA tool. The design should depend on some preponderance logic along with few new results. The proficiency of the design we make should confirm through the simulation result obtained in the QCADesigner tool.

Let us Suppose a pair of 2's complement number with an 8-bit number which are signed binary and they are abbreviated as 'm' and 'n' and they are given as $m^7m^6m^5m^4m^3m^2m^1m^0$ and $n^7n^6n^5n^4n^3n^2n^1n^0$ respectively be the 8-bit signed binary number. The architecture of Baugh-Wooley multiplier is shown in figure 3.1.

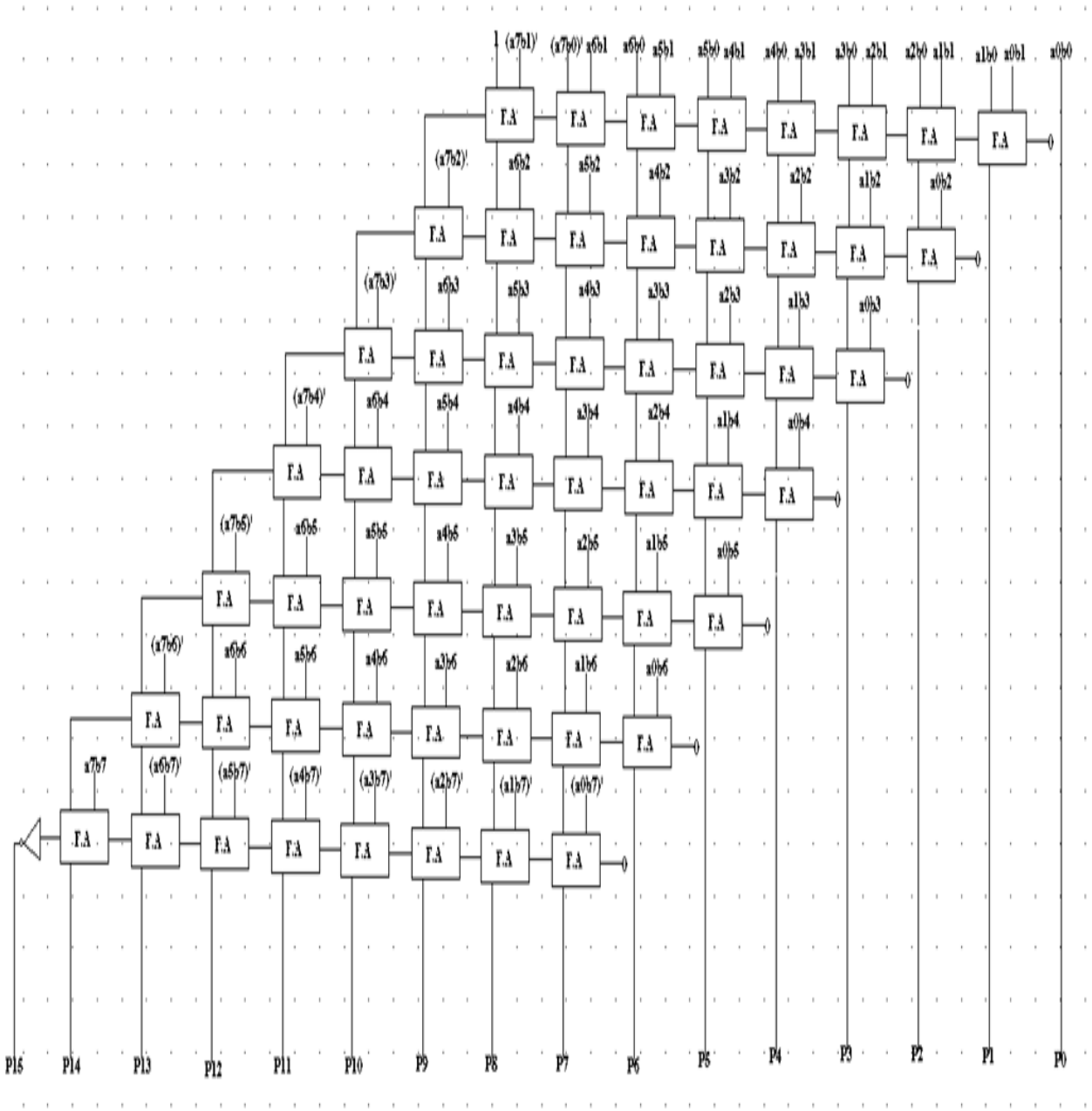

Fig. 3.1 Block diagram of 8-bit multiplier

3.3 Mathematical Analysis of 4-bit Multiplier

Let $m^3m^2m^1m^0$ and $n^3n^2n^1n^0$ be the two 4-bit signed as binary numbers in $2^{'}s$ complement form.

$$m = -m_3 2^3 + (m_2 2^2 + m_1 2^1 + m_0 2^0)$$

$$n = -n_3 2^3 + (n_2 2^2 + n_1 2^1 + n_0 2^0)$$

$$P = mn$$

$$= m_3 n_3 2^6 - m_3(n_2 2^2 + n_1 2^1 + n_0 2^0)\cdot 2^3 - n_3(m_2 2^2 + m_1 2^1 + m_0 2^0)2^3$$

$$+(m_2 2^2 + m_1 2^1 + m_0 2^0)(n_2 2^2 + n_1 2^1 + n_0 2^0)$$

Let $-(n_2 2^2 + n_1 2^1 + n_0 2^0) = -2^3 + n_2^{'} 2^2 + n_1^{'} 2^1 + n_0^{'} 2^0 + 2^0$

Then $P = mn$

$$= m_3 n_3 2^6 - m_3 2^6 + m_3(n_2^{'} 2^2 + n_1^{'} 2^1 + n_0^{'} 2^0)\cdot 2^3 + n_3 2^3$$

$$-n_3 2^6 + n_3(m_2^{'} 2^2 + m_1^{'} 2^1 + m_0^{'} 2^0)2^3 + n_3 2^3$$

$$+(m_2 2^2 + m_1 2^1 + m_0 2^0)(n_2 2^2 + n_1 2^1 + n_0 2^0)$$

Again

$$-m_3 2^6 = -2^7 + m_3^{'} 2^6 + 0^{'} 2^5 + 0^{'} 2^4 + 0^{'} 2^3 + 0^{'} 2^2 + 0^{'} 2^1 + 0^{'} 2^0 + 1$$

$$= -2^7 + m_3^{'} 2^6 + 2^5 + 2^4 + 2^3 + 2^2 + 2^1 + 2^0 + 1 = -2^6 + m_3^{'} 2^6$$

Also

$$-n_3 2^6 = -2^7 + n_3^{'} 2^6 + 2^5 + 2^4 + 2^3 + 2^2 + 2^1 + 2^0 + 1 = -2^6 + n_3^{'} 2^6$$

$$\Rightarrow -m_3 2^6 - n_3 2^6 = -2^6(1+1) + (m_3^{'} + n_3^{'})\cdot 2^6$$

$$\Rightarrow -m_3 2^6 - n_3 2^6 = -2^7 + (m_3^{'} + n_3^{'}) \cdot 2^6$$

$$P = mn = -2^7$$

$$+(m_3 n_3 + m_3^{'} + n_3^{'}) \cdot 2^6$$

$$+m_3(n_2^{'} 2^2 + n_1^{'} 2^1 + n_0^{'} 2^0) \cdot 2^3$$

$$+n_3(m_2^{'} 2^2 + m_1^{'} 2^1 + m_0^{'} 2^0) \cdot 2^3$$

$$+(m_3 + n_3) \cdot 2^3$$

$$+(m_2 2^2 + m_1 2^1 + m_0 2^0)(n_2 2^2 + n_1 2^1 + n_0 2^0)$$

$$P_0 = +2^0(m_0 n_0)$$

$$P_1 = +2^1(m_1 n_0 + m_0 n_1)$$

$$P_2 = +2^2(m_2 n_0 + m_1 n_1 + m_0 n_2)$$

$$P_3 = +2^3(m_2 n_1 + m_1 n_2 + m_3 + n_3 + m_3 n_0^{'} + m_0^{'} n_3)$$

$$P_4 = +2^4(m_2 n_2 + m_3 n_1^{'} + n_3 m_1^{'})$$

$$P_5 = +2^5(m_3 n_2^{'} + m_2^{'} n_3)$$

$$P_6 = +2^6(m_3 n_3 + m_3^{'} + n_3^{'})$$

$$P_7 = -2^7$$

3.4 Mathematical Analysis of 8-bit Multiplier

Let $m^7m^6m^5m^4m^3m^2m^1m^0$ and $n^7n^6n^5n^4n^3n^2n^1n^0$ be the two 8-bit signed as binary numbers in $2^{'}s$ complement form

$$m = -m_7 2^7 + (m_6 2^6 + m_5 2^5 + m_4 2^4 + m_3 2^3 + m_2 2^2 + m_1 2^1 + m_0 2^0)$$

$$n = -n_7 2^7 + (n_6 2^6 + n_5 2^5 + n_4 2^4 + n_3 2^3 + n_2 2^2 + n_1 2^1 + n_0 2^0)$$

$$P = mn$$

Solving the equation with the similar manner as in section 5.1, than we get the product terms as:

$$P = P^{15}P^{14}P^{13}P^{12}P^{11}P^{10}P^9P^8P^7P^6P^5P^4P^3P^2P^1P^0$$

Where each product term can be represent as:

$$P_0 = m_0n_0$$

$$P_1 = m_1n_0 + m_0n_1$$

$$P_2 = m_2n_0 + m_1n_1 + m_0n_2$$

$$P_3 = m_3n_0 + m_2n_1 + m_1n_2 + m_0n_3$$

$$P_4 = m_4n_0 + m_3n_1 + m_2n_2 + m_1n_3 + m_0n_4$$

$$P_5 = m_5n_0 + m_4n_1 + m_3n_2 + m_2n_3 + m_1n_4 + m_0n_5$$

$$P_6 = m_6n_0 + m_5n_1 + m_4n_2 + m_3n_3 + m_2n_4 + m_1n_5 + m_0n_6$$

$$P_7 = \overline{m_7n_0} + m_6n_1 + m_5n_2 + m_4n_3 + m_3n_4 + m_2n_5 + m_1n_6 + m_0n_7$$

$$P_8 = 1 + \overline{m_7n_1} + m_6n_2 + m_5n_3 + m_4n_4 + m_3n_5 + m_2n_6 + \overline{m_1n_7}$$

$$P_9 = \overline{m_7n_2} + m_6n_3 + m_5n_4 + m_4n_5 + m_3n_6 + \overline{m_2n_7}$$

$$P_{10} = \overline{m_7n_3} + m_6n_4 + m_5n_5 + m_4n_6 + \overline{m_3n_7}$$

$$P_{11} = \overline{m_7 n_4} + m_6 n_5 + m_5 n_6 + \overline{m_4 n_7}$$

$$P_{12} = \overline{m_7 n_5} + m_6 n_6 + \overline{m_5 n_7}$$

$$P_{13} = \overline{m_7 n_6} + \overline{m_6 n_7}$$

$$P_{14} = m_7 n_7$$

$$P_{15} = 1$$

3.5 Structure of QCA Cell

The diagram for the four-dot metal in QCA cell as shown in figure 3.2. In this four quantum dots arranged in the square shape. These dots are having a diameter which is very small called as metal Island and this dimension allows the energy for charging larger than k_bT and k_b represents the Boltzmann's constant [13]. The potential energy needed for the electrons to expel the electrostatic repulsion with respect to other electrons in the dot is considered as charging energy or we can say that it is an essential energy which is required to input an electron into a dot and these dots can able to trap individual charges only if the energy is found to be larger than thermal energy of k_bT [13].

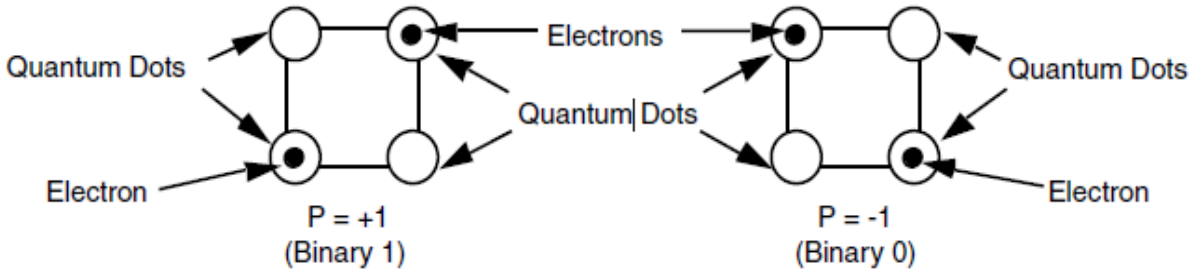

Fig.3.2. Polarization in QCA cell [13]

Through the means of tunnel of electrons as in quantum dots supports movement of electrons in and out of the cell. This path of tunneling is shown by lines connecting the various quantum dots as in figure 3.2. Due to Coulombic force there is an interaction electron are able to occupy the corner position in a QCA cell and produces two particular polarization levels. It makes the electrons to be far apart from each other in a drastically minimal position without exceeds its limit of the cell boundary. Here, the tunnel of an electron is fully control with the help of potential barriers which could be allow to raise and simultaneously lowering of border in

between QCA cells through plates act as capacitor on the dots plane [4] [14]. There also some other different polarized state in addition to these and they are non-classical as well as unpolarized state [13].

3.6 Clock Phases in QCA

In Figure 3.3. the four clocks in QCA are shown such as switch, hold, release and relax.

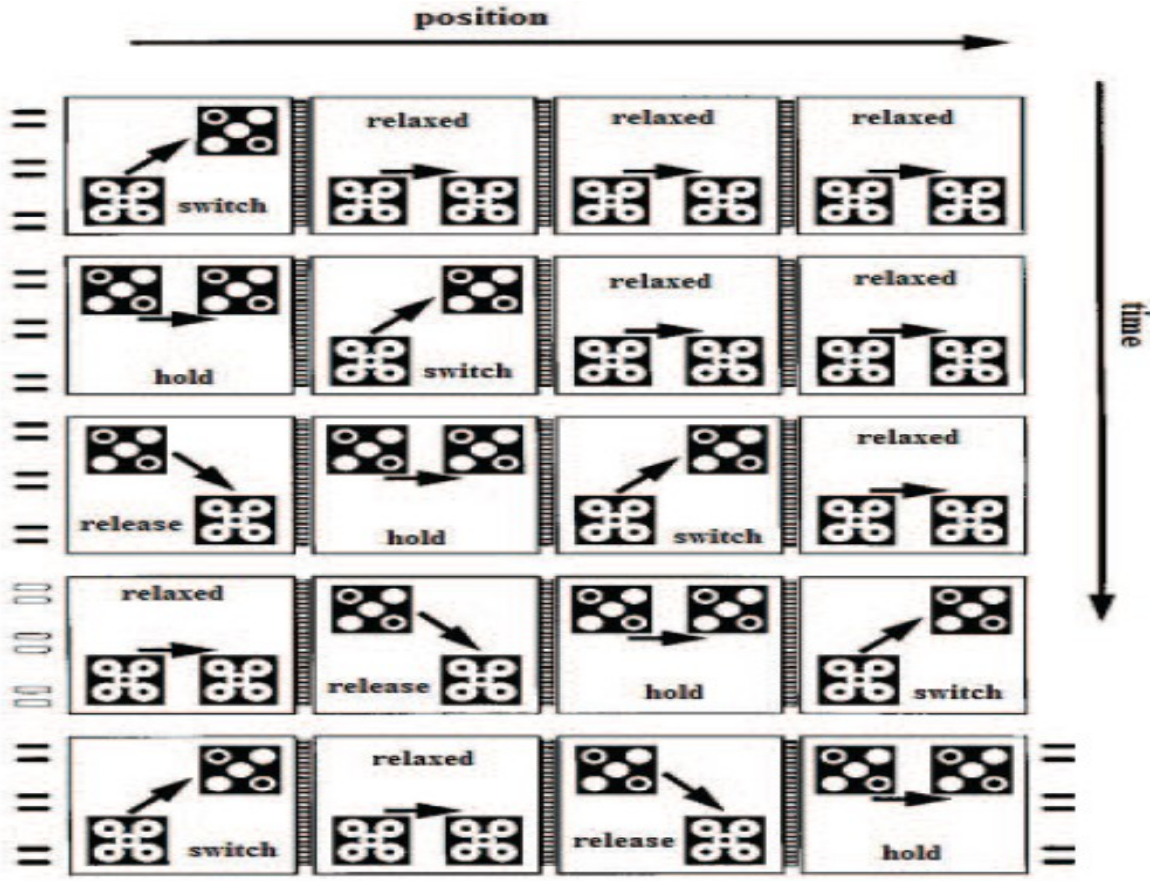

Fig.3.3 Four clock states of QCA [10]

1. Switch: When the clock is going from low to high logic levels or the barrier is rising, the cell becomes polarized with the polarization of its drivers [10].
2. Hold: When the clock is high or the barrier is raised, the cell retains its state [10].
3. Release: When the clock is going from high to low logic levels or the barrier is lowering, the cell is allowed to relax, losing its polarization [10].
4. Relax: When the clock is low or the barrier is low, the cell remains not polarized [10].

3.7 Experimental Work

3.7.1 AND Gate

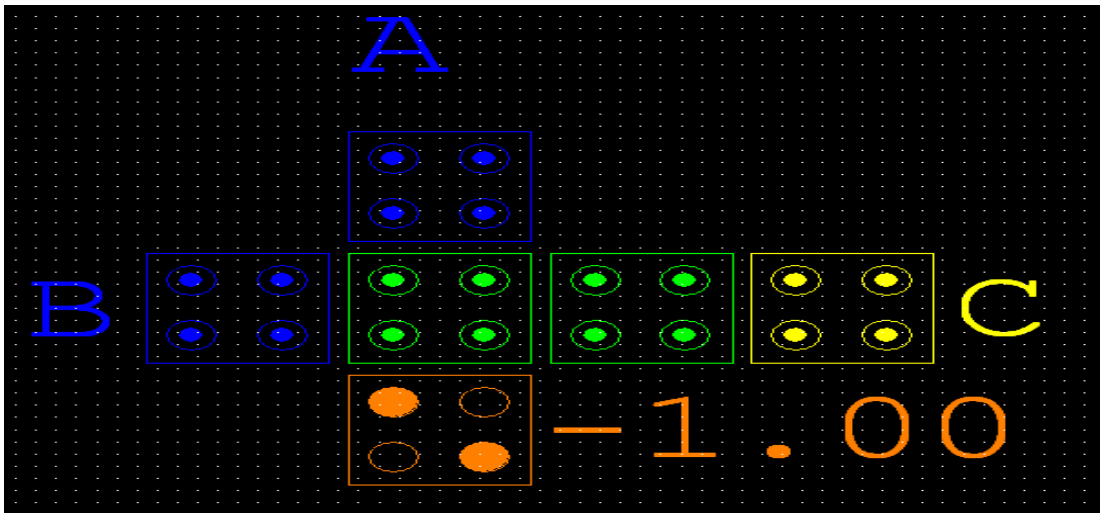

Fig.3.4. QCA Layout of AND gate

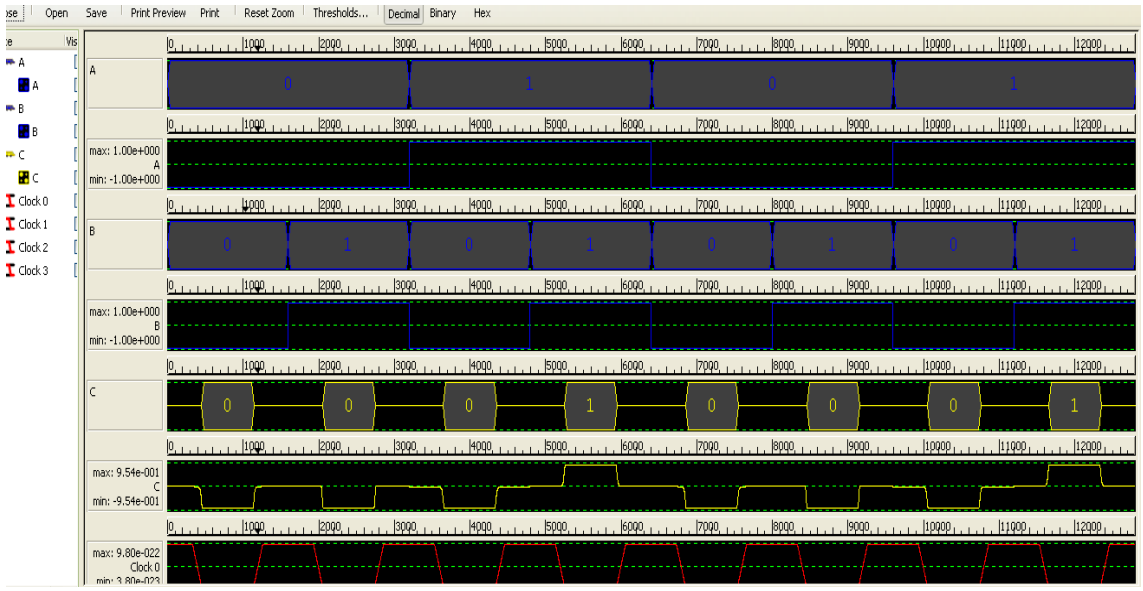

Fig.3.5. QCA output graph for AND gate

3.7.2 OR Gate

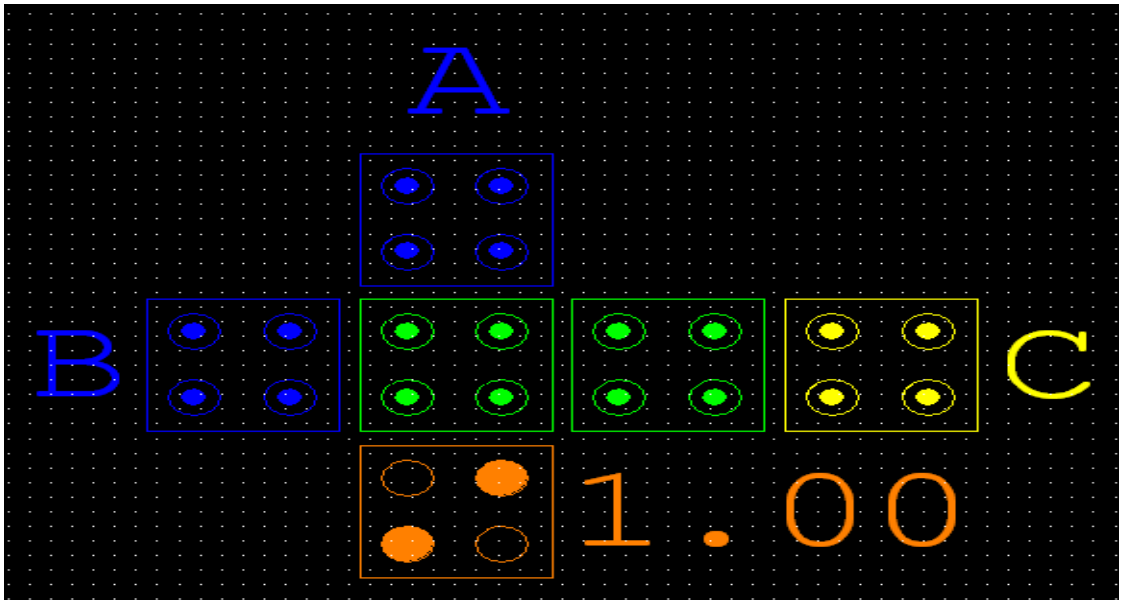

Fig.3.6 QCA Layout of OR gate

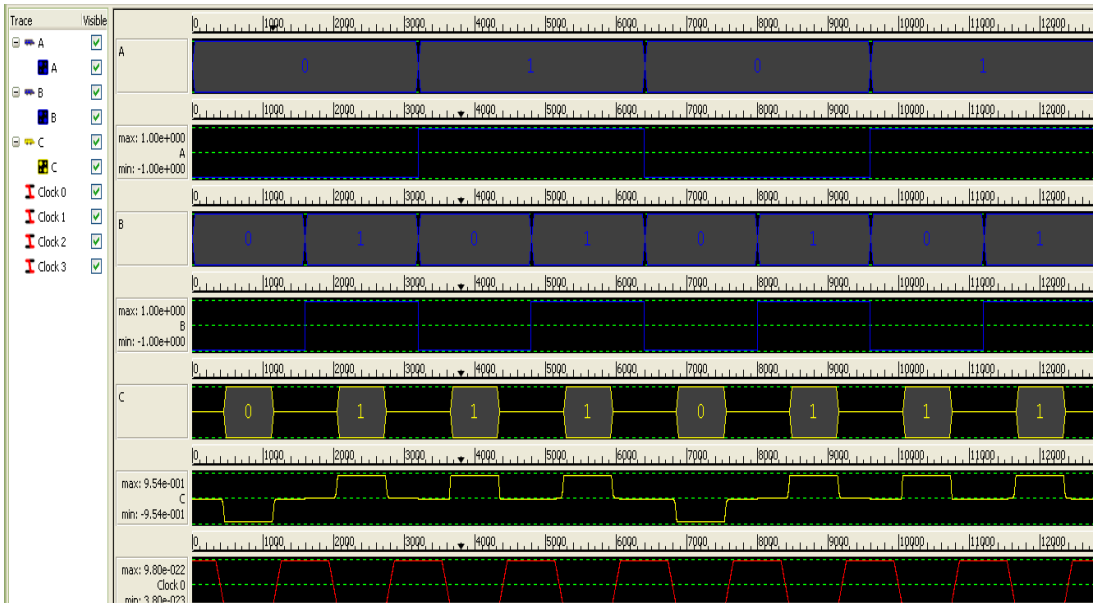

Fig.3.7 QCA output graph for OR gate

3.7.3 NAND Gate

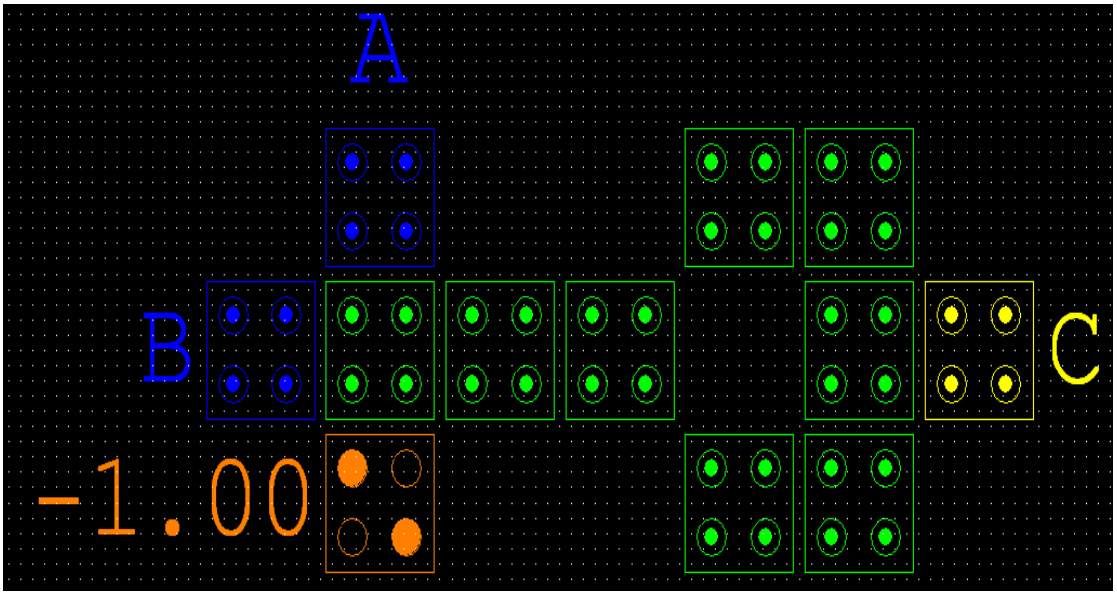

Fig.3.8 QCA Layout of NAND gate

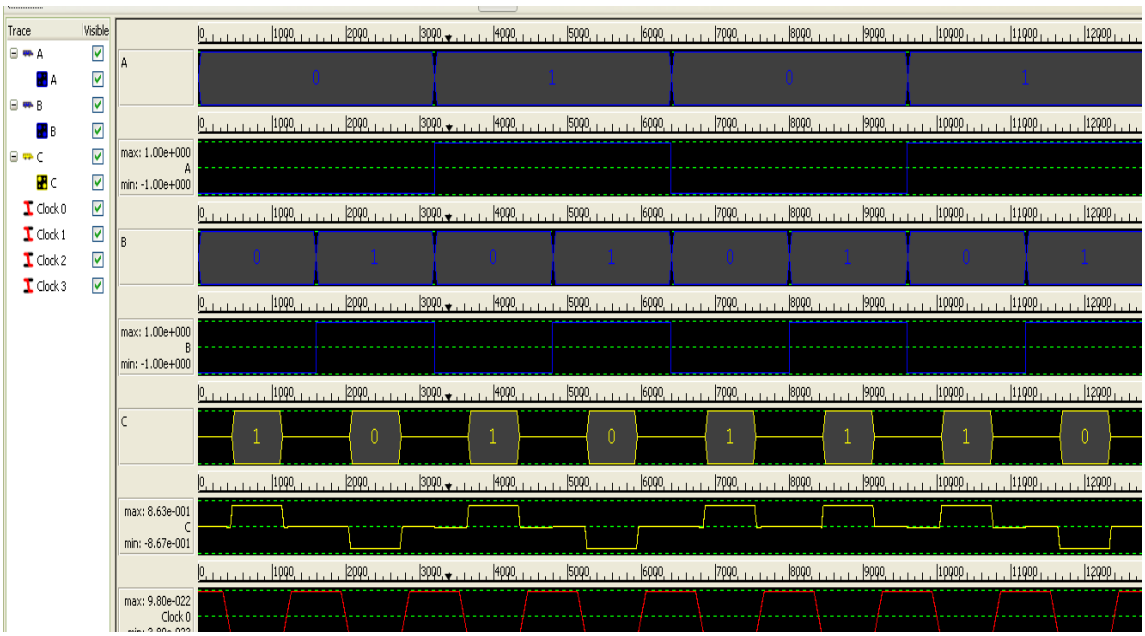

Fig.3.9 QCA output graph for NAND gate

3.7.4 NOR Gate

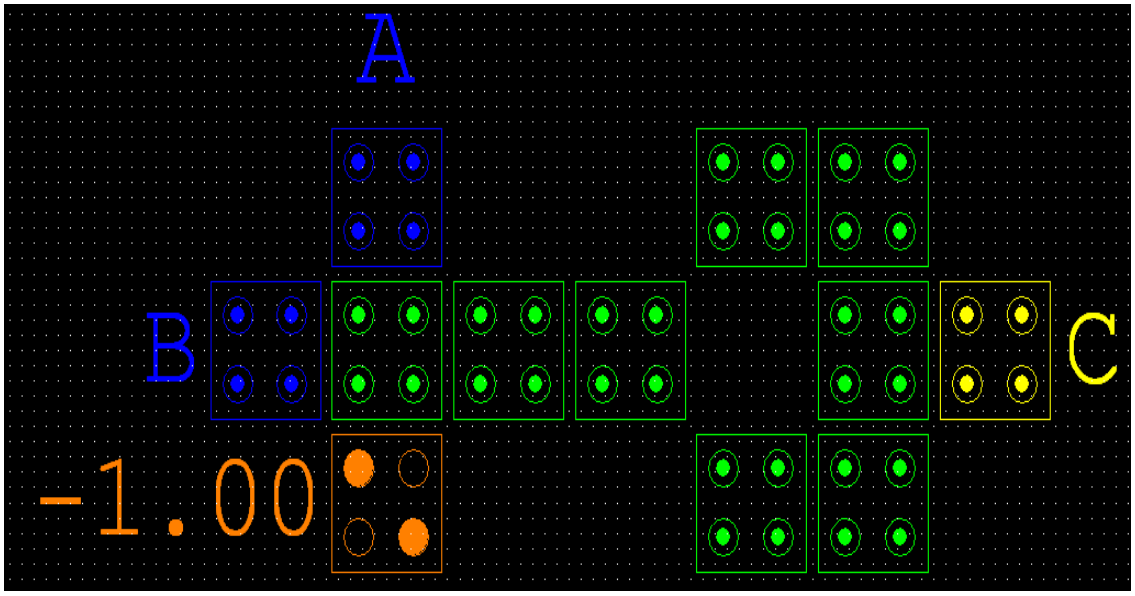

Fig.3.10 QCA Layout of NOR gate

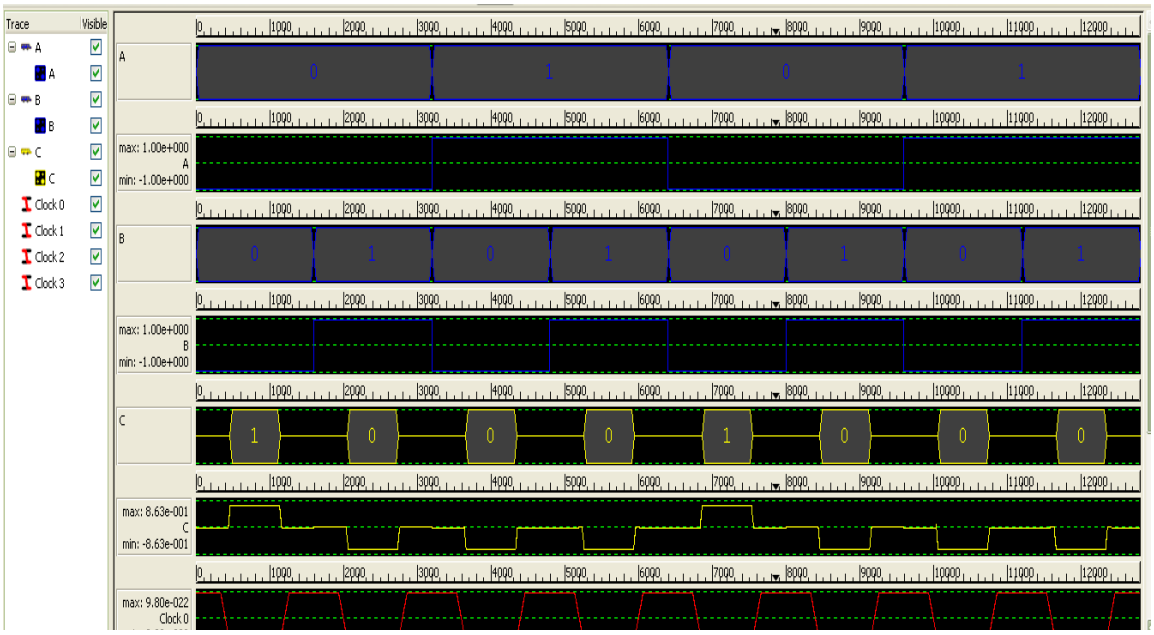

Fig.3.11 QCA output graph for NOR gate

3.7.5 XOR Gate

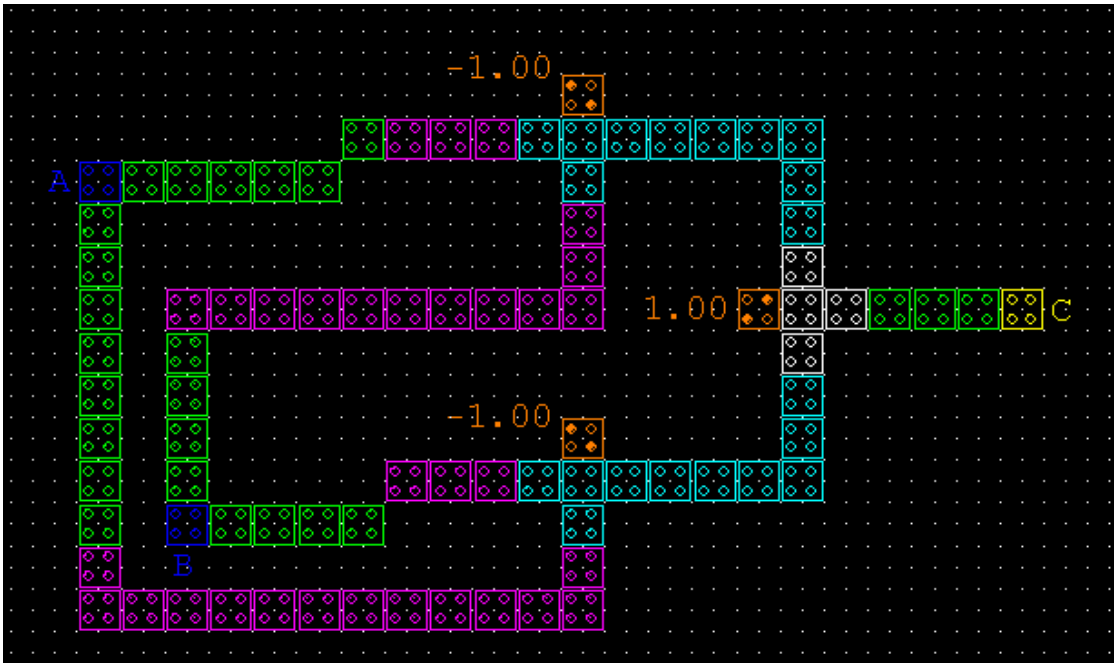

Fig.3.12 QCA Layout of XOR gate

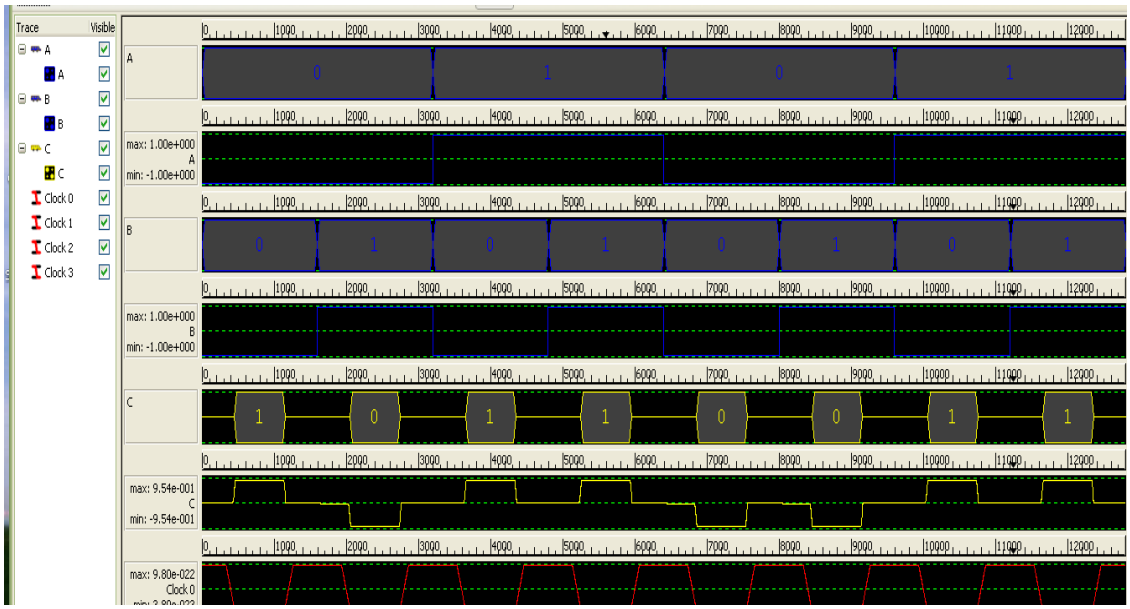

Fig.3.13 QCA output graph for XOR gate

3.7.6 XNOR Gate

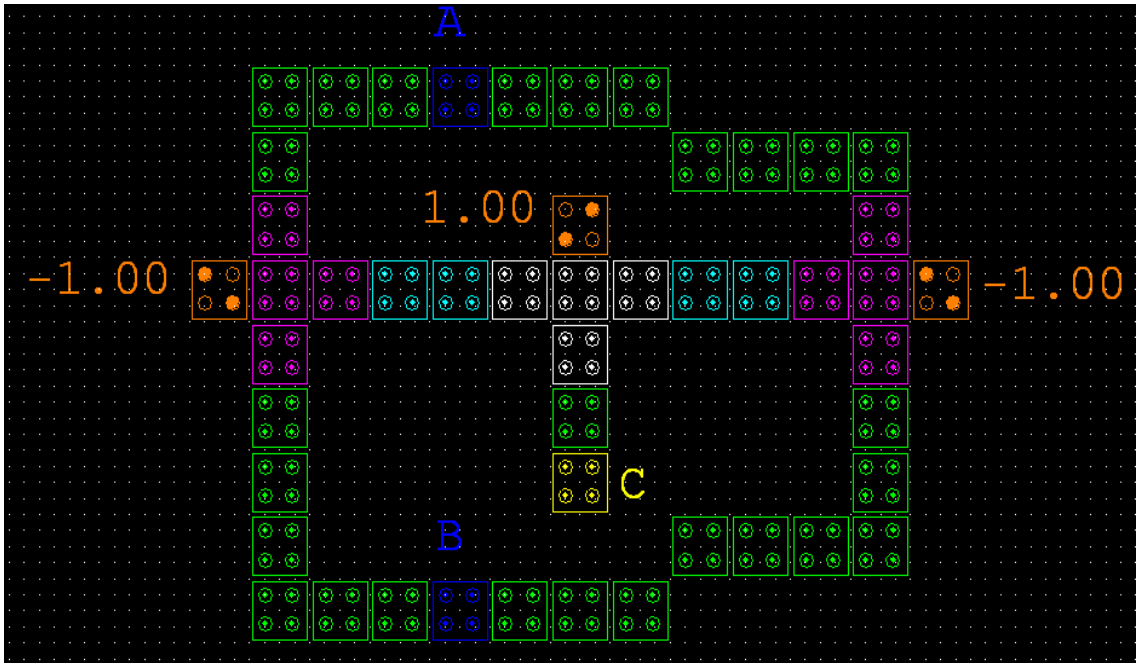

Fig.3.14 QCA Layout of XNOR gate

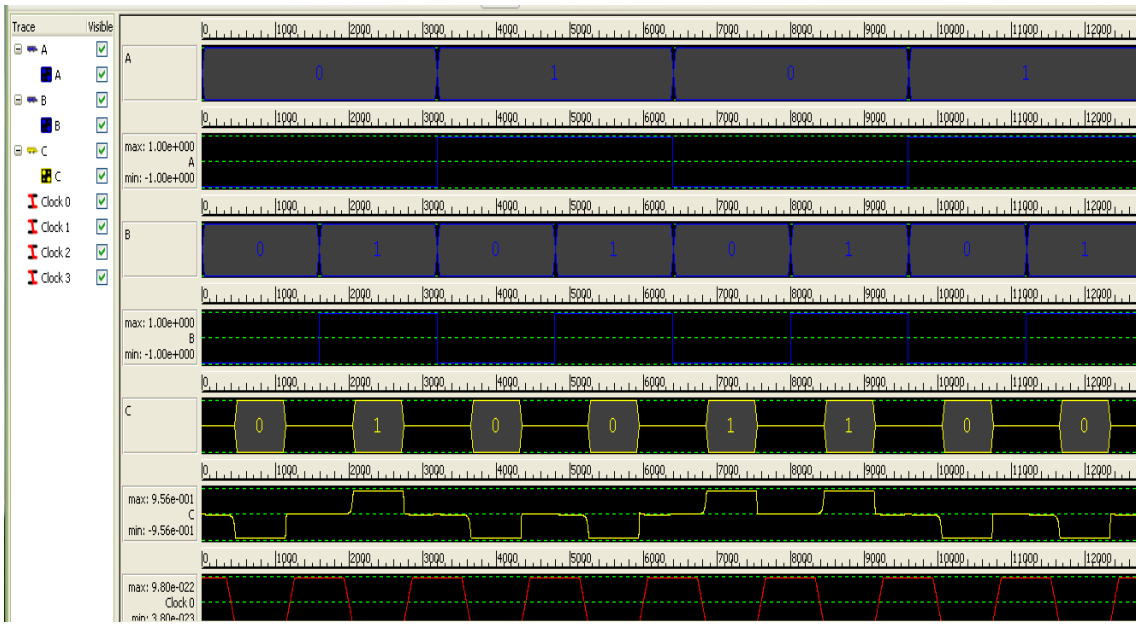

Fig.3.15 QCA output graph for XNOR gate

3.7.7 Half Adder

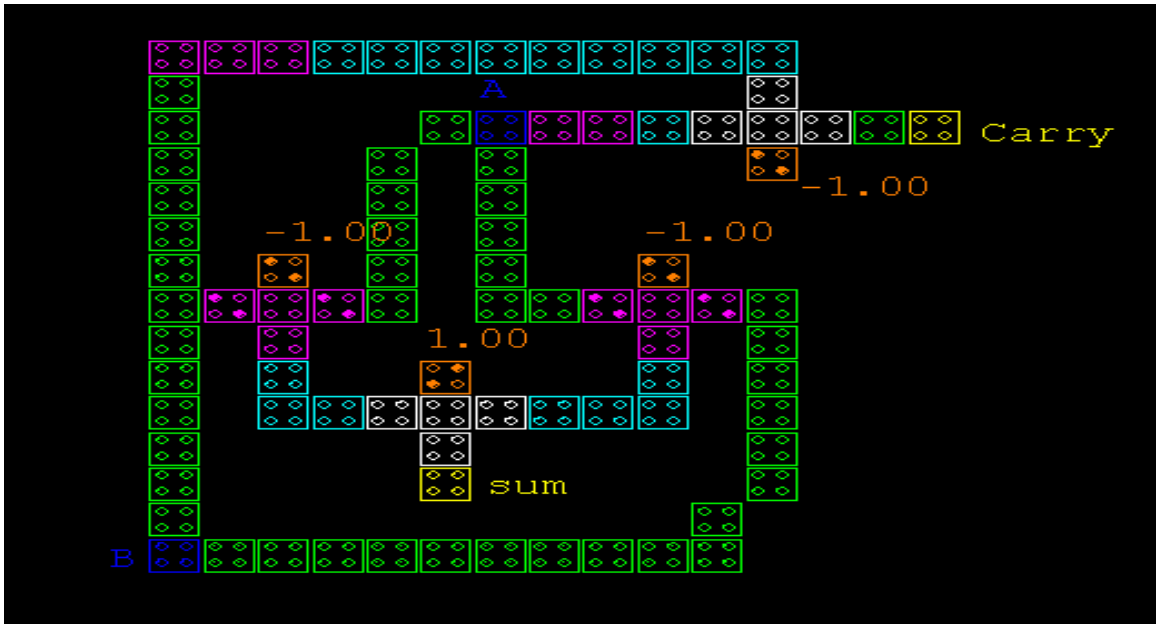

Fig.3.16 QCA Layout of Half Adder

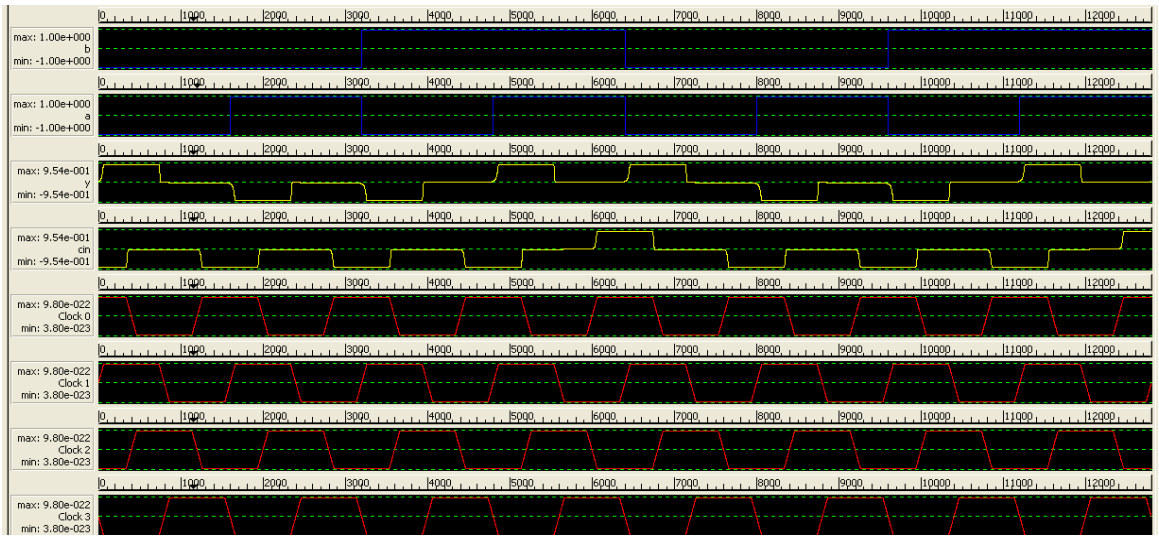

Fig.3.17 QCA output graph for Half Adder

3.7.8 Full Adder

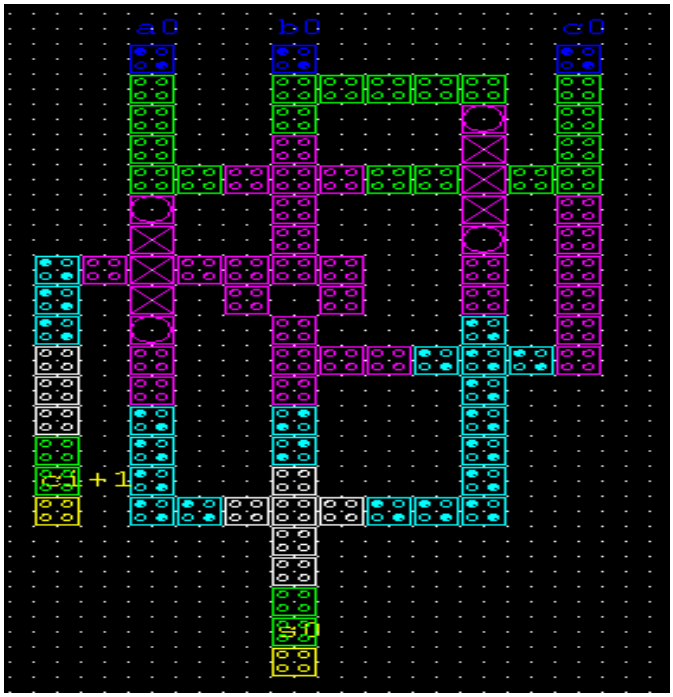

Fig.3.18 QCA Layout of FULL Adder

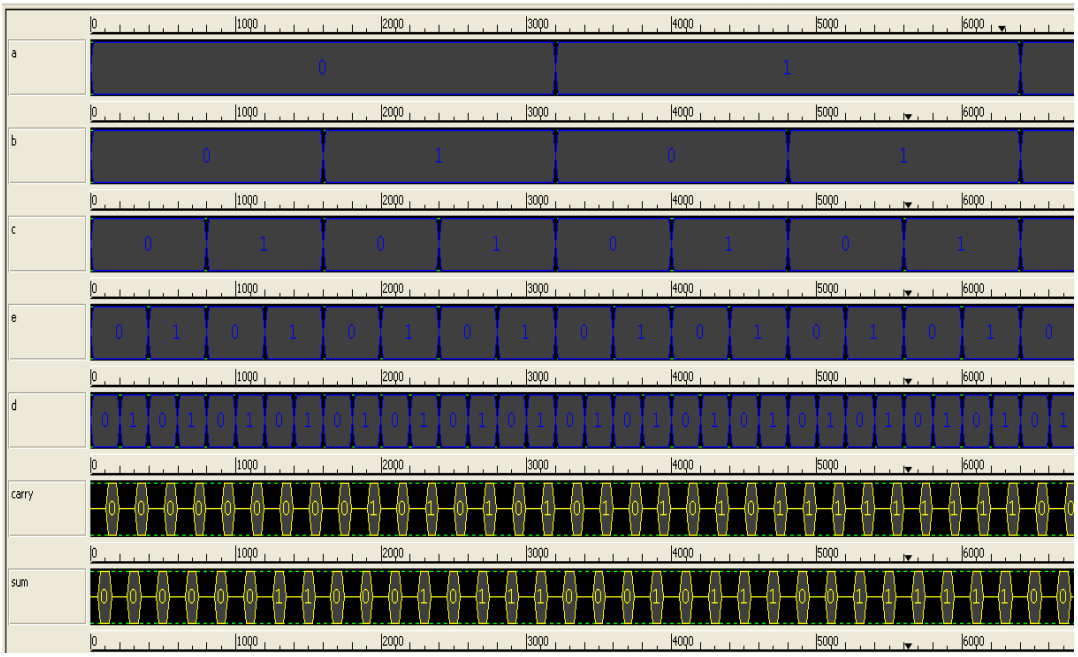

Fig.3.19 QCA output graph for FULL Adder

3.7.9 In-Depth Architecture of 4-Bit Multiplier

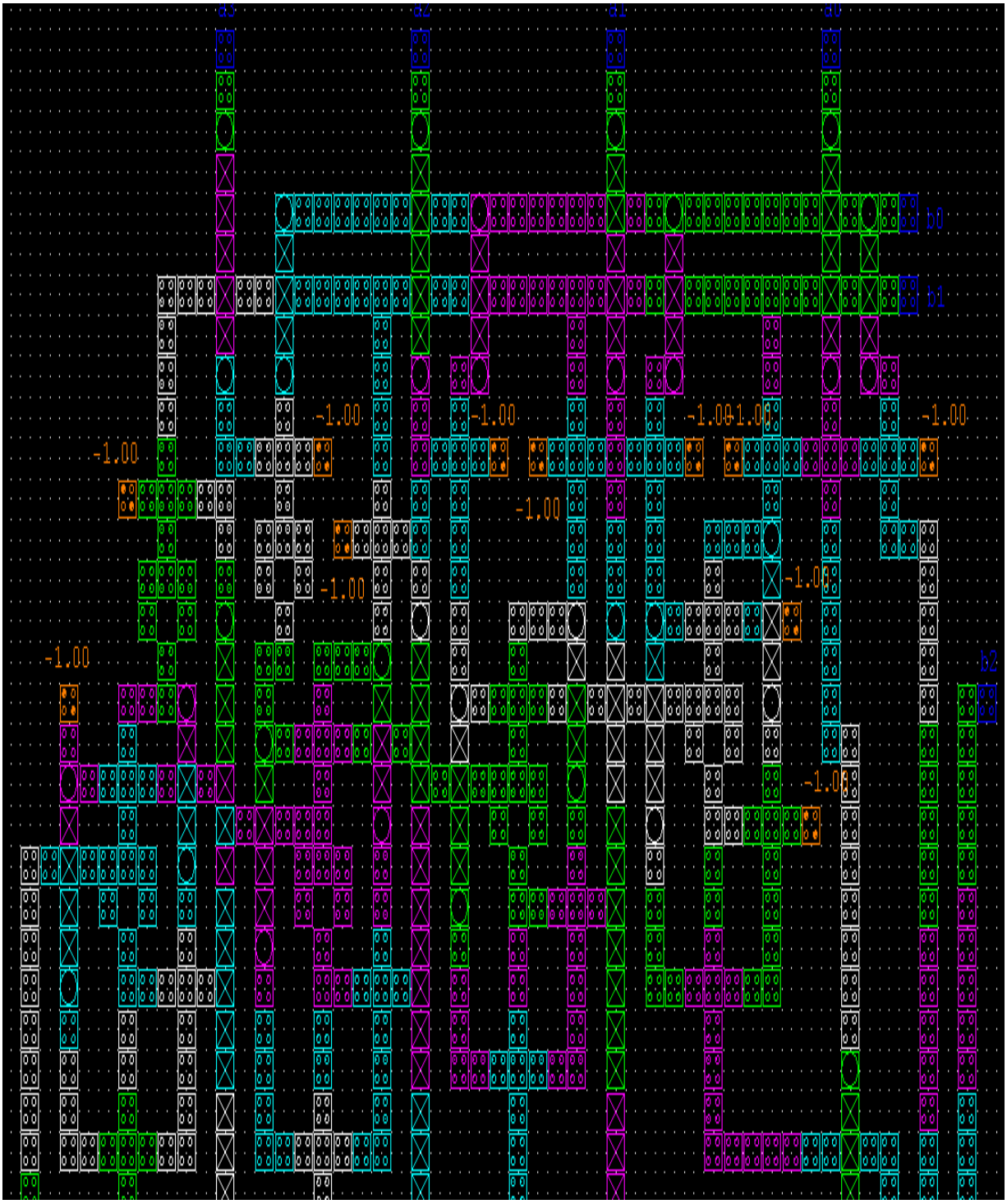

Fig.3.20 QCA Layout of Expanded layer of 4-bit architecture 1

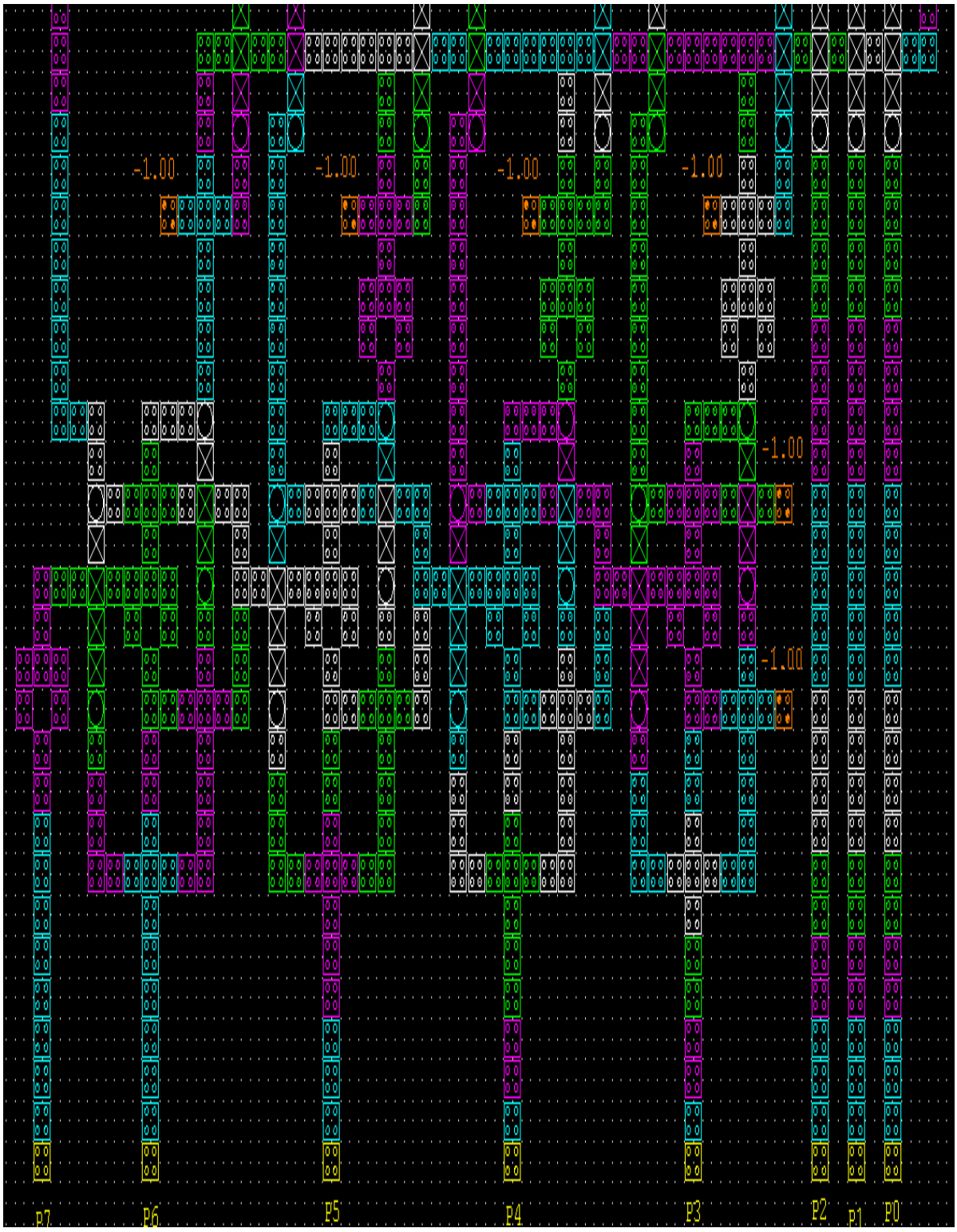

Fig.3.21 QCA Layout of Expanded layer of 4-bit architecture 2

3.7.10 QCA Architecture of 8-Bit Baugh-Wooley Multiplier

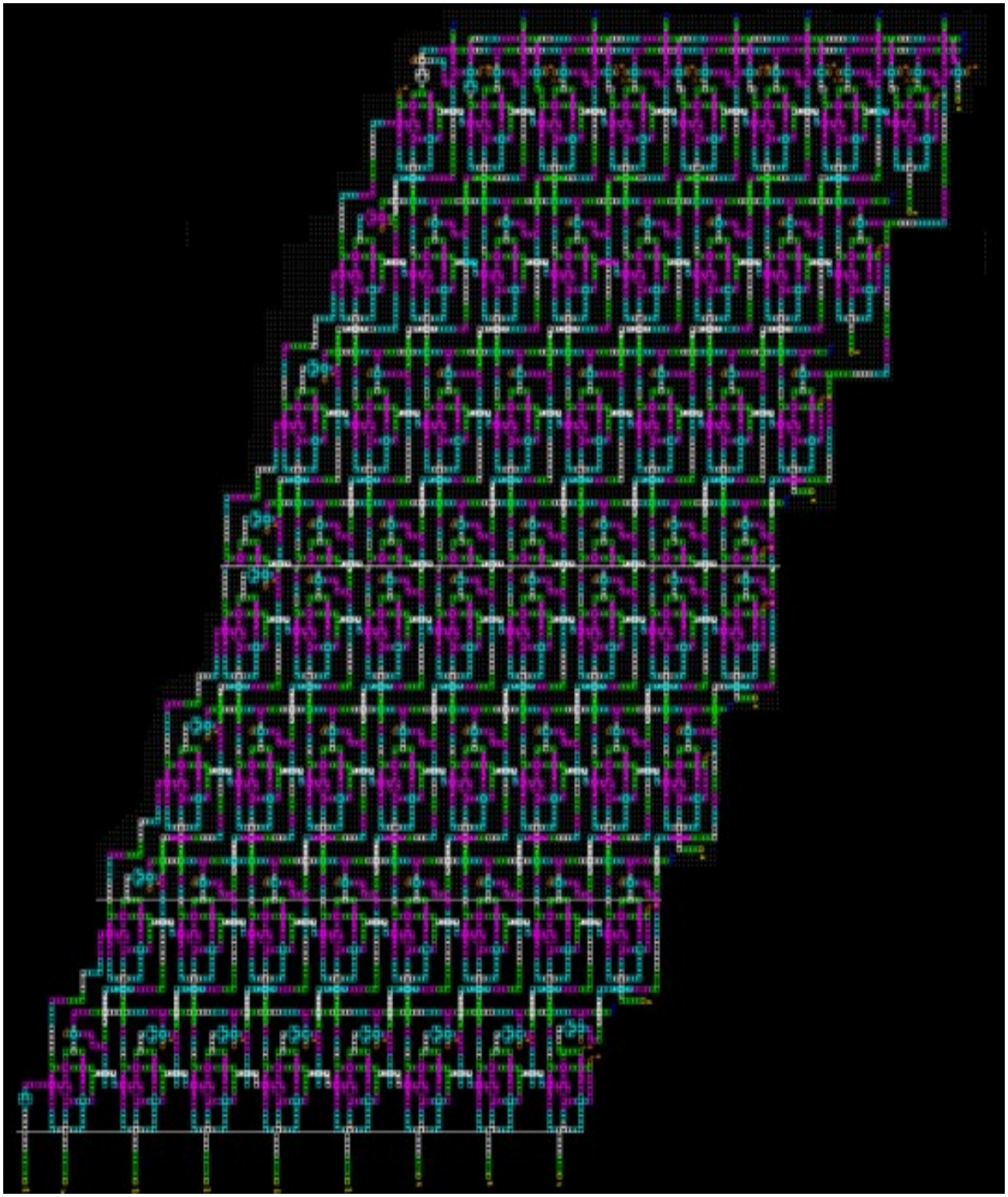

Fig.3.22 QCA Layout of 8-bit Baugh-Wooley Multiplier

3.7.11 Cadence Architecture of 8-Bit Baugh-Wooley Multiplier

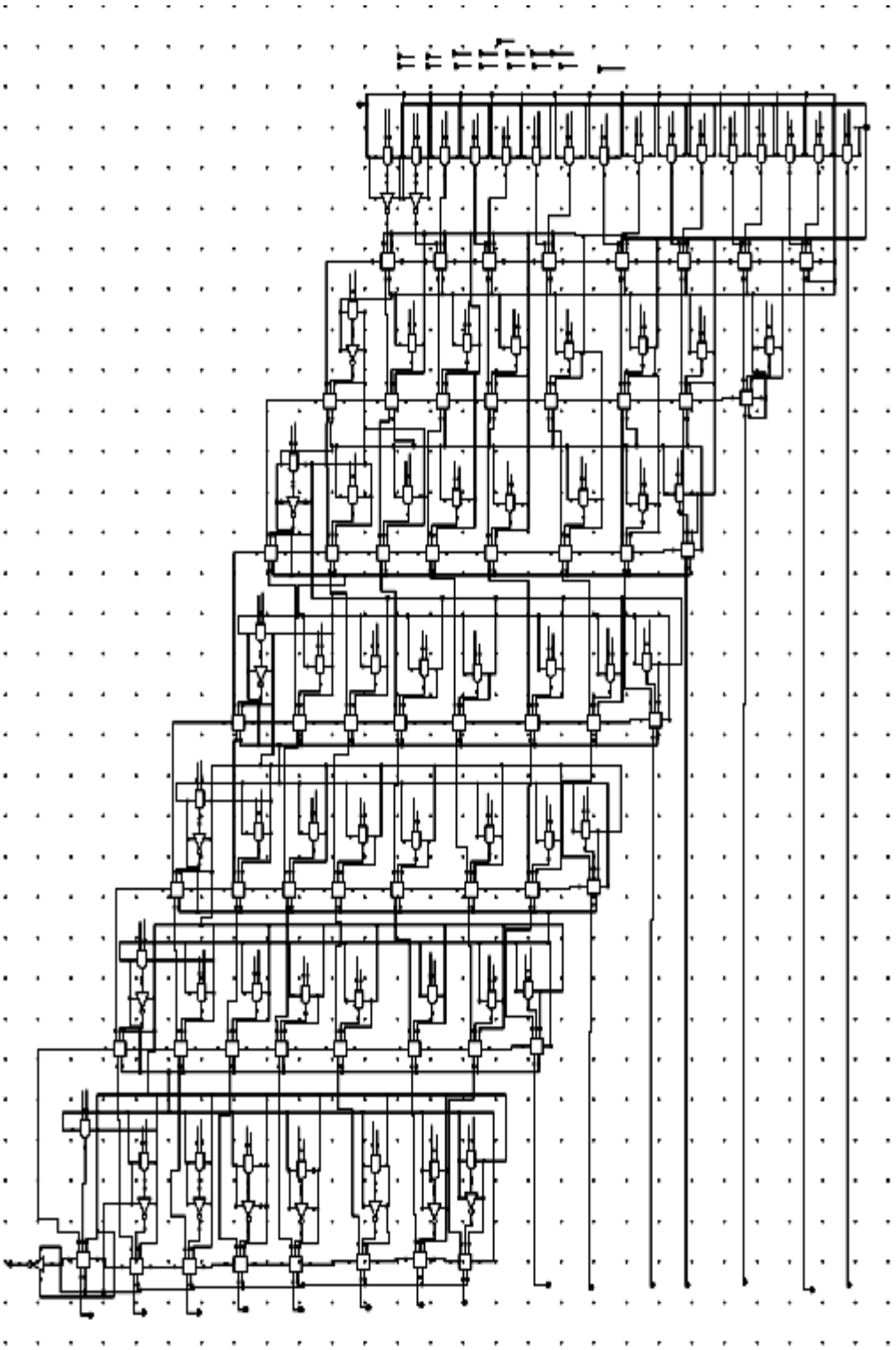

Fig.3.23 Cadence Layout of 8-bit Baugh-Wooley Multiplier

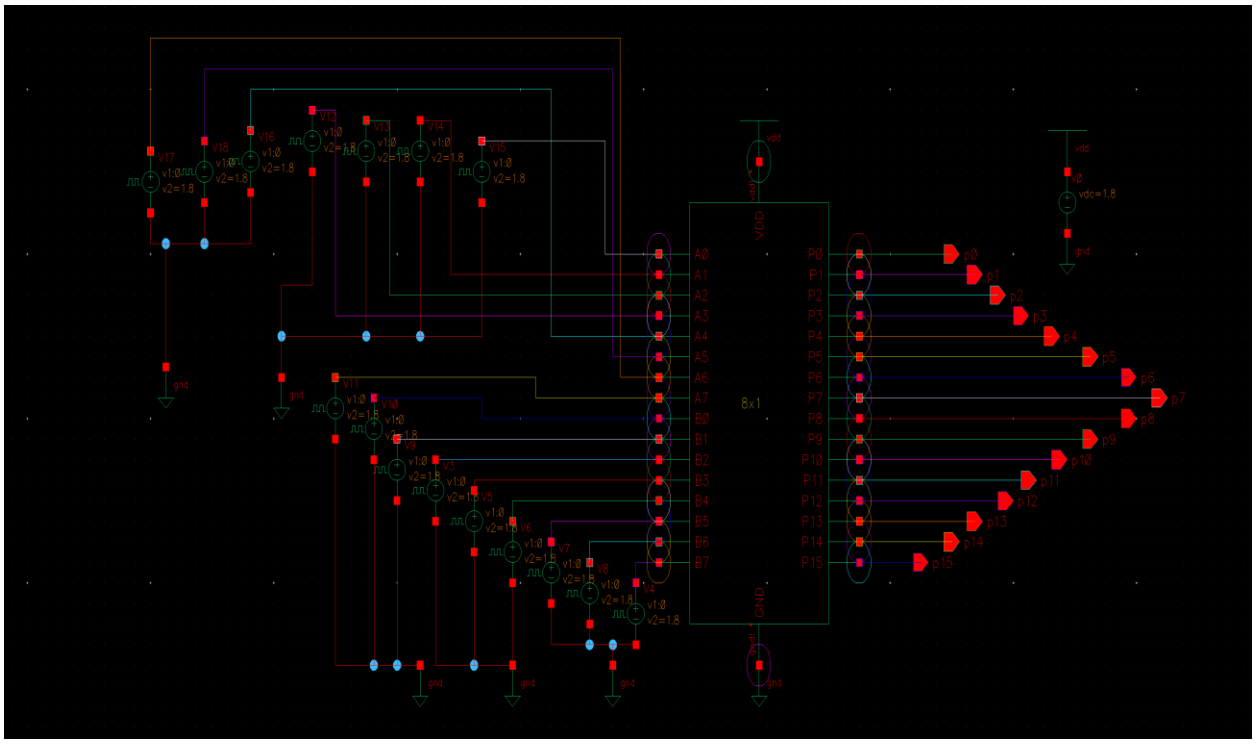

Fig.3.24 Cadence Symbol of 8-bit Baugh-Wooley Multiplier

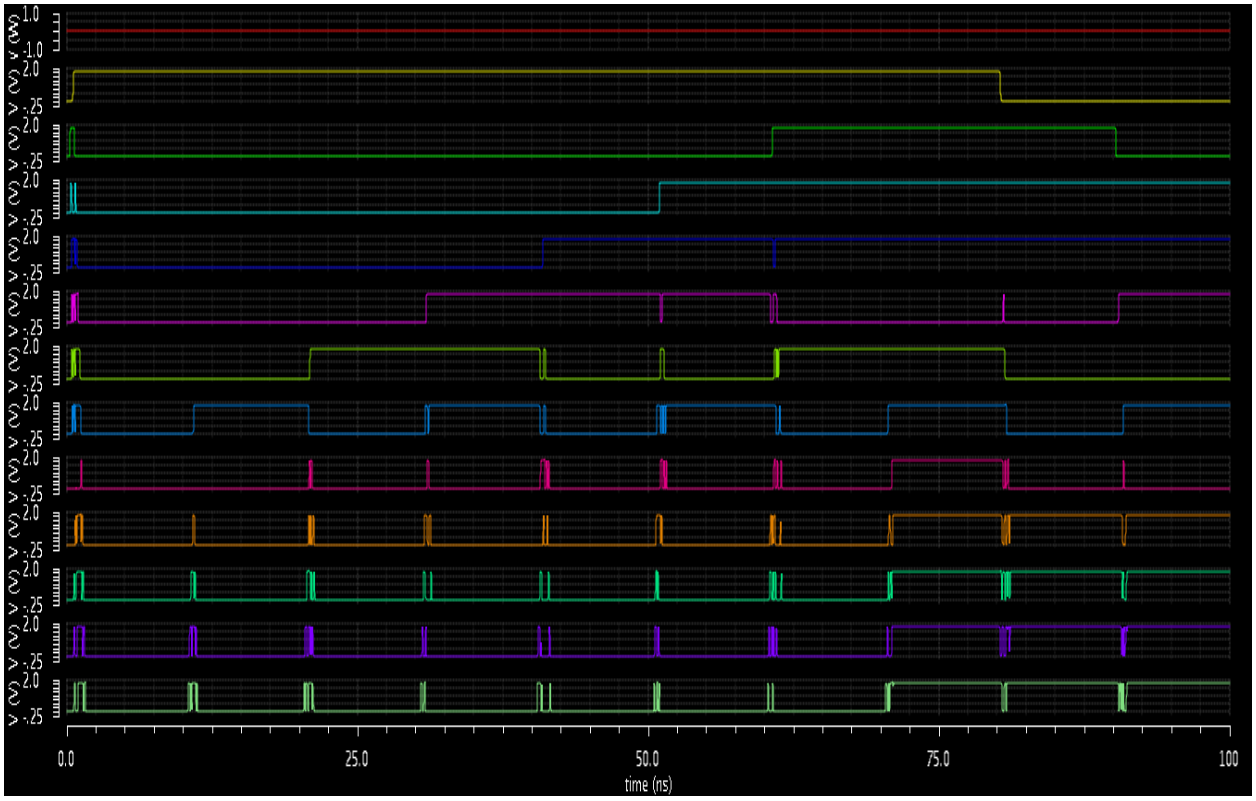

Fig.3.25 Cadence output graph of 8-bit Baugh-Wooley Multiplier

CHAPTER 4
RESULT AND DISCUSSION

4.1 QCA Result

4.1.1 4-Bit Baugh-Wooley Multiplier

For Simulation QCADesigner [12] is used. The dimension of cells assumes to height and weight was (18 x 18) nm respectively with a diameter for quantum dots to be 5nm. These cells are aligned over to a grid with center dot distance to be 20 nm. Coherence vector engine method used for design simulations. Comparisons shown for cell count, delay, area and the throughput of the multiplier

TABLE 4.1 QCA parameter for 4-bit Baugh-Wooley multiplier [12]

Multiplier Approach	Cell Count	Area (μm^2)	Latency (clocks0)	Throughput
Baugh-Wooley 4x4	1982	1.8	4.75	1

4.1.2 8-Bit Baugh-Wooley Multiplier

TABLE 4.2 QCA parameter for 8-bit Baugh-Wooley multiplier

Multiplier Approach	Cell Count	Area (μm^2)	Latency (clocks0)	Throughput
Baugh-Wooley 8x8	11399	18.35	14	1

4.2 Comparison

TABLE 4.3 Comparison for Baugh-Wooley multiplier for two technologies

	QCA	Cadence
Power	Depend on clock	Depend on Supply voltage
count	cell	Transistor
Area	Low (18.35um2)	High(>20um2)
Technology	Quantum	Nanotechnology
Latency	14	0
Performance	Fast	Comparable Slow
Tool	QCA Designer	Cadence Virtuoso

CHAPTER 5
CONCLUSION

5.1 Conclusion and Future Scope

Even after many years after its proposal, QCA has innumerous problems in all levels of the design flow, like the layout floor planning and some fault problems due to noise paths. This report presented the design of a complex 4- bit Baugh Wooley Multiplier using the Parallel Pipelined Adder's. The basic steps were the construction of discrete gates using the conversion from Boolean expressions to majority equations. Then, the PPA was assembled using the discrete circuits generated in the fourth step of procedure. Some decisions as which kind of crossover may be used have to be made. Another important design decision is which group propagation and group generation tree is the most appropriate to be adopted.

In this report, we have showed the design of the 8-bit Baugh-Wooley multiplier in QCA. The designs are based on some results in majority logic. The designs have been simulated and results show that the proposed design has low area as well as low delay.

The circuit area is divided into four sections and they are driven by four phase clock signals. In each zone, the clock signal has four states: high-to-low, low, low-to-high, and high. The cell begins computing during the high-to-low state and holds the value during the low state. The cell is released when the clock is in the low-to-high state and inactive during the high state.

This report also proposed a design methodology for QCA circuits simulate the full-adder based on qca cells. The Simulation Results from QCA 2.0.3 tool. The layout algorithm is adopted from the one used to balance the wave pipelined circuits. The proposed design methodology will speed up and facilitate the design of large QCA-based digital circuits much more. A design example proves the correctness and accuracy of this design methodology. The proposed design flow will be a sound reference and basis for the future QCA based NANO circuit design. As the development and understanding of QCA cell continues, the QCA model will become more accurate and the layout algorithm will be further optimized in area and delay aspects.

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APPENDIX

LIST OF ABBREVATIONS

A:

AOI: AND-Or-Inverter

B:

BW: Baugh-Wooley

C:

CSA: Complex Sum Adder

CMOS: Complementary Metal Oxide Semiconductor

D:

DSP: Digital Signal Processing

DCT: Discrete Cosine Transform

F:

FIR: Finite Impulse Response

FFT: Fast Fourier Transform

FH: Frequency Hopping

L:

LSB: Least Significant Bit

M:

MV: Majority Voter

MAC: Multiply and Accumulate

N:

NNI: NAND-NOR-Inverter

P:

PPA: Parallel Pipeline Adder

Q:

QCA: Quantum-dot Cellular Automata

V:

VLSI: Very Large Scale Integration