Design and Implementation of MOSFET based Folded Cascode Current Mirror

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Abstract **– A high performance MOSFET current mirror in a folded cascade configuration is design to achieve a high output resistance . The design has both n and p type MOSFET for current feedback between gate and source in order to achieve a constant drain current . In the discussed circuits we have found out the range of currents for which the circuit is showing amplification and mirroring effect. We need high output impedance so to drive more circuitry from it and the current mirror is the circuit that implements the principle that if a gate-source voltage of two uniforms MOS transistors is same then their channel current flowing would be equal. We have implemented the folded cascode current mirror where the range of current on which the circuit is mirroring the current ranges from 100mV to 700mV. The circuit is implemented on cadence virtuoso 180nm technology with 1.8V supply voltage.**

Keywords- Current mirror, Folded cascode current mirror, MOSFET current mirror.

I . INTRODUCTION

In various application like biomedical operates on very low voltage which needs a very high output impedance current mirror. The current mirror is the circuit that implements the principle that if a gate-source voltage of two uniforms MOS transistors is same then their channel current flowing would be equal. In the current mirror, we generate a current reference so to copy that current in various current sources in the system. Various advancement in the technology of CMOS design integrated most of the circuits in the same chip who all are working on very low supply voltage like radio frequency processor and various sensor like temperature and baseband signal processing circuit require very low voltage supply. Getting a very large impedance and wide output range and swing is the important parameter when working on the very low input voltage[1]. The current mirror is the circuit used where the operating voltage required to turn on the circuit is very low as in case of biomedical applications. In the current mirror, we need high output impedance so to drive more circuitry from it. If current (Id)= f(VGS), where function denotes the functionality of ID versus VGS, then VGS = f^{-1}(ID). Then if the transistor is biased through IREF then VGS = f^{-1}(IREF). Thus, voltage is put into the source-gate terminal then derived current as shown in fig. 1.

$Iout = ff^{-1}(IREF) = IREF$

$ID1 = \frac{1}{2} un\ cox(\frac{w}{l_1})(vgs - vth)^2(1 + \lambda vds1)$ *and*

$ID2 = \frac{1}{2} un\ cox(\frac{w}{l_2})(vgs - vth)^2(1 + \lambda vds2)$

So hence $\frac{ID2}{ID1} = \frac{\left(\frac{w}{l}\right)^2}{\left(\frac{w}{l}\right)^1}\frac{(1+\lambda vds2)}{(1+\lambda vds1)}$

So in order to minimize the consequence of channel length modulation cascade current source is used, the Vbias voltage Vb is so chosen that the voltage $V_y = V_X$ then the output current Iout tracks Iref with accuracy as shown in fig. 2 but this accuracy is obtained at the cost of voltage

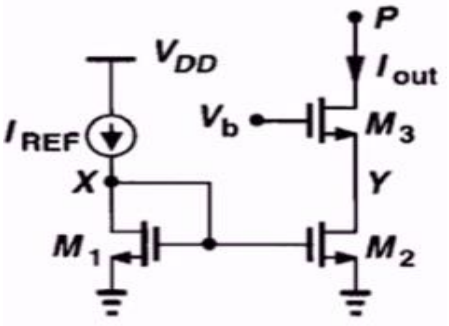

Fig.1 Current mirror

head room that is consumed by the M3 transistor. So now how to generate the Vb so that $V_y = V_X$ so from transistor M3 we have Vb - V_{gs3} = V_X or Vb = V_X+V_{gs3}. This shows that if gate–source voltage is adjoin to V_X , the necessitate value of Vb can be acquired by this .

If an additional diode connected load is added M0 in series of M1 which create the voltage of Vn = V_{gs0}+Vx . So proper dimension of M0 and M3 will make $V_{g3} = V_{g0}$. Now connecting Vn to the gate terminal of M3. We get $V_{gs0}+V_X = V_{gs3}+V_y$.

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Thus if the W/L aspect ratio of M3 by M1 is equal to W/L ratio of M2 by M1 then we can say that V_{gs3}= V_{gs0} and $V_X = V_y$. So if the current mirror is ideal than if the V_{ds} changes than I0 should not change as the output impedance of the ideal current mirror is infinite . we calculate output impedance by $\frac{\Delta Vo}{\Delta Io}$. So even though Vo is changing Io should not change according to the principle hence $\Delta Vo/0$ is infinite and hence the output resistance of current mirror comes out to be infinite[5]. So to have the output impedance increased we move on to next type of current mirror that is cascode current mirror.

So why we are using cascode current mirror because of extinguishing the result due to channel length modulation (CLM) and increase the yield impedance[2] as shown in the given fig. 2 and fig. 3 below.

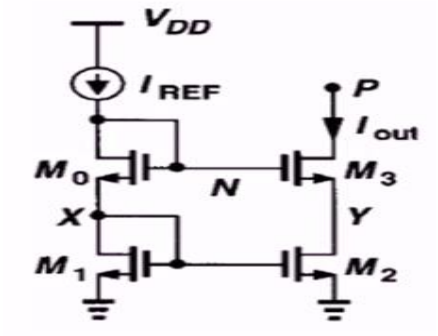

Fig.2 Cascade current mirror

At node N we give Vbias to both of the gate of M0 and M3 transistor to makeV_{gs0} equal to V_{gs3}.
So voltage at both the side is V_{gs0}+Vx = V_{gs3} +Vy
Now to make both of them equal proper dimension of the transistor is taken.

$$\frac{W}{L_3}*\frac{W}{L_0}=\frac{W}{L_2}*\frac{W}{L_1}$$

Which gives $V_{gs0} = V_{gs3}$

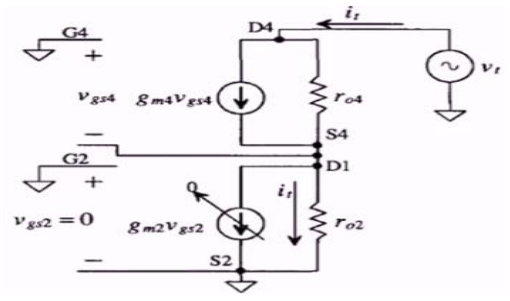

Fig.3 Small signal of cascode current mirror

And output impedance of the circuit is vt/it
So current

$$I_t = g_{m4} * V_{gs4} + \frac{V_t - (-V_{gs4})}{ro_4}$$

$$V_{gs4} = I_t * ro_2$$

So substituting the value of V_{gs4} in I_t ,we get

$$\frac{V_t}{I_t} = ro_4(1 + gm_4 * ro_2) + ro_2$$

$$R_0 = gm_4 * {r_o}^2$$

Where $r_0 = ro_2 = ro_4$

So small signal model of cascade is as shown . Here V_{gs2} is zero as voltage across M2 is zero as M1 is shorted as it acts like a DC voltage so that makes $g_{m2} * V_{gs2}$ equal to zero. So from the above equation we get to know that the total output resistance shown by the circuit is gm times the resistance, hence the output impedance of a modified cascode current mirror is very high with respect to simple current mirror whose resistance is R_{ds}[8].

II CIRCUIT DESCRIPTION

Figure 4 shows the cascode current mirror implemented in BJT with the folded cascode configuration . The diode-connected transistor was folded into two pair in the folded cascode current mirror. The design has dual pnp-npn current mirror for feedback from base and emmiter to have constant collector current .

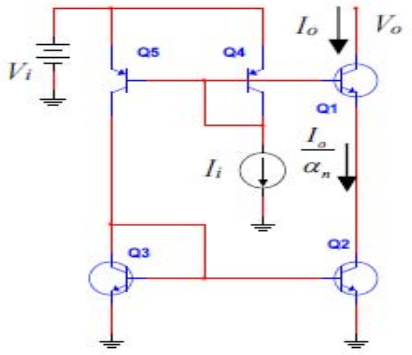

Fig.4 BJT cascode current mirror

The basic BJT current source consists of a reference transistor connected diode and a output transistor with circuit connections to the bases and emitters so the output collector current would be ideally, mirror of the current of the reference collector.

The result resistance of the basic current source is equal to the Early Effect resistor that is equal to Rout = r_0. The design has an output resistance of 71Mohm and impedance bandwidth product of 2.87 ohm – hz at 1mA output current and 1.6V input voltage[3][4]. This circuit can be implemented using MOSFET also

so the same circuit is been implemented using MOSFET as shown in the fig. 5.

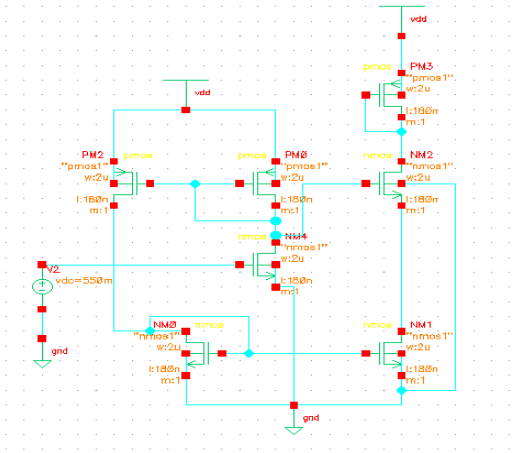

Fig.5 MOSFET folded current mirror.

III MATHEMATICAL MODELLING

In the circuit shown in fig. 6, PM3 MOSFET act as a driving load which act like a diode working in a saturation region always. The transistor NM0, PM0 also work as a simple diode connected, basically in comparison to simple cascode current mirror we are folding the NM MOSFET here into PM2 and PM0 . So a small signal model is needed to know the analysis where transistor NM0, PM0,PM3 will be simple act like a diode and easily replaced by simple resistance value in a small signal model. So basic small signal for the same is drawn for the transistor NM1,NM2,PM2 . NM2 transistor will act like a current source and will provide the reference current which is going to be mirrored to the NM2 drain terminal as shown in fig. 7.

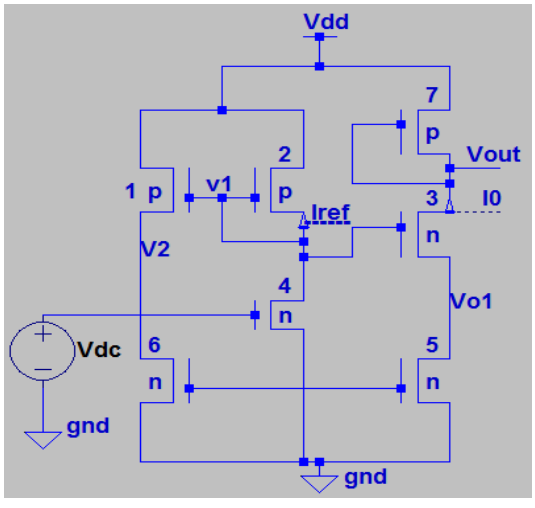

Fig.6 Proposed folded cascode current mirror

So basic idea for me to solve this is by coming from the output side to the input side so we have transistor no.5 and 3 at the output side of the circuit. Then considering the 5 transistor we have voltage across drain to source of 5 transitor is given by

$$V_{o1} = g_m * r_{o1} * V_{gs5} \qquad \text{eq-1}$$

And the current through the 3 transistor is given by

$$\frac{V_{out}-V_{o1}}{\frac{r_{o2}*R_{d1}}{r_{o2}+R_{d1}}} + g_m * V_{gs3} = 0 \qquad \text{eq-2}$$

Now from the circuit we get to know that the value of gate to source voltage for 3 transistor is

$$V_{gs3} = V_{g3} - V_{s3}$$

$$V_{gs3} = V_1 - V_{o1} \qquad \text{eq-3}$$

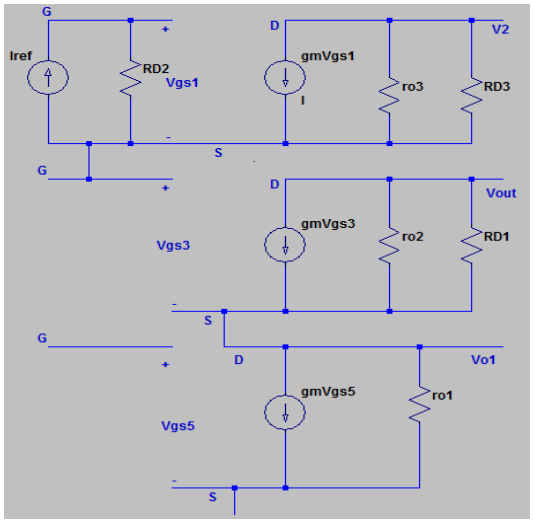

Fig.7 Small signal model of folded CM

Now we can substitute the value of Vgs3 in equation no,2 we will get the V_{out} value as

$$V_{out} = V_{o1}\left[1 + g_m\left(\frac{r_{o2}*R_{d1}}{r_{o2}+R_{d1}}\right)\right] - V_1\left[\frac{r_{o2}*R_{d1}}{r_{o2}+R_{d1}}\right] \qquad \text{eq-4}$$

Now considering the above small signal for transistor no.1 we get.
Current in the gate terminal is given by

$$I_1 = g_m * V_{gs1} + \frac{V_2}{\frac{r_{03}*R_{d3}}{r_{03}+R_{d3}}} \qquad \text{eq-5}$$

and current in the drain side is given by

$$I_2 = I_{ref} + \frac{V_{gs1}}{R_{d2}}$$

here $V_{gs1} = V_1$

$$\text{So } V_1 = R_{d2}(I_2 - I_{ref}) \qquad \text{eq-6}$$

then substituting the value of V1 to equation.

$$I_1 = g_m * V_1 + \frac{V_2}{\frac{r_{03}*R_{d3}}{r_{03}+R_{d3}}} \quad \text{eq-7}$$

Now substituting the value of V1 in equation no-7 and finding the value of g_m in respect to I_{ref} is given by.

$$g_m = \frac{I_1 + \frac{V_2}{\frac{r_{03} * R_{d3}}{r_{03} + R_{d3}}}}{R_{d2}(I_2 - I_{ref})}$$

Now this g_m is in terms of I_{ref} so now substitute this value of g_m into the eq-4 which is the output voltage.
So now the output voltage of the transistor in term of I_{ref} is given by.

$$V_{out} = V_{O1}\left[1 + \left[\frac{I_1 + V_2\left(\frac{r_{03}+R_{d3}}{r_{03}*R_{d3}}\right)}{R_{d2}(I_2 - I_{ref})}\right]\left(\frac{r_{o2}*R_{d1}}{r_{02}+R_{d1}}\right)\right]$$

$$- V_1\left[\frac{r_{o2}*R_{d1}}{r_{02}+R_{d1}}\right]$$

So we get to know that the output voltage is related on so many parameter , their can be another way of defining the circuit . The overall output voltage Vout in term of the reference voltage is defined.

IV RESULT AND DISCUSSION

The implemented circuit has been analysed in cadence virtuoso 180nm technology with a supply voltage of 1.8V . Different circuit is been analysed before implementing folded cascode mirror like current subtractor using current mirror where ranges varies from 0nA to 100µA [6] , a high advance cascode current mirror is analysed [7] from ranges .3 V to 1.8 V where NM2 is the drain terminal of input side and NM3 is the drain terminal of output mosfet as shown in the table 1. In the proposed circuit a range of value is tested to know the correct biasing voltage that is going to mirror the input current to the output current in the circuit. This MOSFET circuit implemented has the range from 100m – 800m voltage with the exact mirroring value at around 550mV as shown in the table 2. here NM4D represent the drain terminal of output transistor and NM2D represented the drain terminal of input side. In the proposed circuit of folded cascode current mirror for small voltages of around 0.4 V to 0.5 V the difference between the input and output side is minimum with a high output resistance of 163kohm at viasing voltage of 550mV with 1.8V power supply. The previously implemented folded cascode current mirror [3] implemented in BJT works well at around 1mA output current giving output resistance nearly equal to 71 MΩ.

Table.1. Cascode current mirror

Vbias Voltage	NM2/D/current input	NM3/D/current output
0.3 V	99.7042 µA	98.2305 µA
0.4 V	93.5833 µA	92.3942 µA
0.6 V	84.5302 µA	83.6872 µA
0.8 V	69.7290 µA	69.2167 µA
0.9 V	43.1119 µA	42.9191 µA
1.1 V	14.4909 µA	14.4705 µA
1.3 V	1.4230 µA	1.4285 µA
1.4 V	34.9627 nA	35.34 nA
1.6 V	341.881 pA	350.769 pA
1.8 V	4.2837 pA	7.7891 pA

Table.2.Folded cascode current mirror

Vbias Voltage	NM2/D/current input	NM4/D/current output
0.44 V	2.6231 µA	1.8673 µA
0.45 V	3.2818 µA	2.5102 µA
0.46 V	4.0772 µA	3.2153 µA
0.47 V	5.0339 µA	3.9643 µA
0.48 V	6.1763 µA	5.0229 µA
0.50 V	7.5297 µA	6.3138 µA
0.51 V	9.1196 µA	7.8759 µA
0.52 V	10.97 µA	9.7457 µA
0.53 V	13.103 µA	11.959 µA
0.55 V	15.534 µA	14.999 µA

V CONCLUSION AND FUTURE SCOPE

In this thesis work ,I learned that a current mirror can be used in various analog circuit where low

voltage application is needed as the devices now a days are much more portable so should work on low voltage to consume the battery consumption. A brief idea of how a current mirror is going to behave in different short of input biasing voltage is been discussed . All current mirrors have different short of range for which the current in the circuit is mirrored to another branch , from the study we get to know that the cascode current mirror is having good range of values mirrored with respect to other type of current mirror with having high output impedance it's resistance value is ∗ times the value shown by simple current mirror. The proposed circuit uses folded cascode current mirror and been used in a range from 100m to 600m voltage , with exact mirroring the current when Vbias provided to current source is equal to 550m V. It's output voltage equation is derived that shows the involvement of reference current into the output voltage. Further this design can be used to implement any bigger circuit like in current feedback amplifier and can be act as a current source.

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