A Novel Low Power Hybrid Flipflop using Sleepy Stack Inverter Pair

Helga Evangelene
Department of ECE.
Lovely Professional University
Jalandhar, India
mail2evangelene@gmail.com

Rajkumar Sarma
School of electronics, VLSI domain
Lovely Professional University
Jalandhar, India
rajkumar.sarma86@gmail.com

***Abstract*—This paper presents a low power hybrid flip flop using sleepy stack inverter pair for retaining the logic level till the end of evaluation and pre-charge phase of the flip flop. The sleepy stack inverter pairs are efficient in leakage power reduction and overall power dissipation as the technology scales down to 90nm and below. The performance of the proposed flip flop was compared with the conventional dual dynamic node pulsed hybrid flip flop (DDFF) which uses conventional static CMOS inverter pairs in cadence virtuoso 90nm tool. It shows 20% reduction in total power consumed with 89% reduction in leakage power at its output node. T flip flop, SR flip flop and JK flip flop were designed using this proposed D flip flop and its performance was compared with flip flops designed using DDFF. As the proposed flip flops have improved performance in terms of leakage power, total power and power delay product at high speed, it can be widely used in high performance applications.**

Keywords—Flip flops; leakage power; low power; leakage reduction

I. INTRODUCTION

Flip flops are widely used in synchronous sequential digital circuits. It can be designed by two ways namely dynamic logic style and static logic style. Dynamic style exhibits high speed and less area where as static design style exhibits low power. Here we consider a hybrid flip flop which possesses the advantage of dynamic and static design structure. The dynamic structure is present at the input side and static structure is present at the output side of the flip flop design.

An efficient flip flop will have high clock frequency to increase the speed of the system. Due to increase in speed of the systems, there is a huge challenge for researchers today to meet out the large power consumed by the system. The flip flops consume two types of power. They are 1) Dynamic power dissipation which is due to switching activity and short circuiting[1],[2]. The dynamic power dissipation is estimated by the well known formula given below:

$$P_d = f\,C\,V_{dd}^2 \quad (1)$$

where f is the clock frequency, C is load capacitance and V_{dd} is the supply voltage. 2) Static power dissipation is due to the leakage current and reverse bias PN junction [2]. The static power dissipation is estimated by the formula given below:

$$P_s = I_{leakage}\,V_{dd} \quad (2)$$

where $I_{leakage}$ is the leakage current and V_{dd} is the supply voltage. The leakage power is present at both runtime and off state. Even when the system is in off state the leakage current creates a scenario that the system is under operation. This leakage power is highly prevalent in deep sub micrometer (DSM) CMOS technology as the feature size gets reduced below 0.1micron. So the off state leakage power and runtime leakage power should be kept minimum. This paved way for the research in leakage reduction in flip flops. Leakage power reduction technique can be classified into two: 1. State destructive technique which does not retain exact logic state when the circuit is switched to other modes. 2. State saving technique which retains the exact logic state [3].

In our proposed approach, we reduce the leakage power and the overall total power at high speed by replacing the CMOS inverter pair by sleepy stack inverter pair [3]. This sleepy stack leakage reduction technique is a state saving technique. The purpose of inverter pair is to retain the logic value immediately after latching till the end of evaluation or pre-charge phase. So this inverter pair is at work throughout the operation of flip flop. This is the reason why we wanted to reduce leakage power in a specific part of the whole design though ultimately the overall power of the flip flop is also reduced.

The paper is organized as follows. Section II describes existing flip flop architecture. Section III describes the implementation of T flip flop, SR flip flop and JK flip flop using DDFF D flip flop. Section IV describes the proposed flip flop architecture. Section V represents Experimental setup and simulation results. Section VI concludes the paper.

II. EXISTING FLIP FLOPS

Hybrid flip flops are the high performance flip flops. Hybrid latch flip flop (HLFF)[4],[5], semi dynamic flip flop (SDFF)[6] and DDFF[7] are some of the hybrid flip flops. HLFF is the slowest among all hybrid flip flops but consumes low power. SDFF is the fastest hybrid flip flop with trade off in power. DDFF is the latest highly efficient hybrid flip flop. Fig.1 shows DDFF. It operates in two phases: 1) Evaluation Phase 2) Pre-charge phase.

A. Evaluation phase[7]

In this phase CLK=1. If the input D=1, then X1 node is discharged through the path N1,N2,N3. The logic value at X1

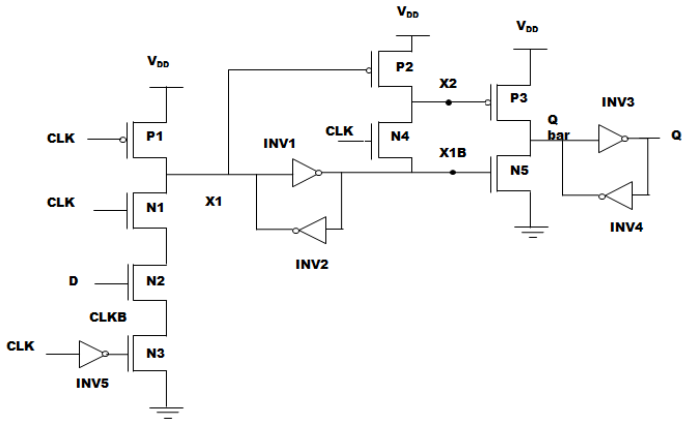

Fig. 1. Conventional DDFF

will be zero. This latching occurs only during 1-1 overlap of CLK and CLKB[7],[8],[9]. The logic value 0 is maintained at X1 by the inverter pair INV1 and INV2 till the evaluation phase gets over. The node X1B is high throughout the evaluation phase and Q bar discharges to 0. The output Q is maintained by the inverter pair INV3 and INV4 till next evaluation phase occurs. The node X2 is high when D is high throughout the evaluation phase. If the input D=0, then X1 node will be at logic 1 and X2 node will be in logic low. Q bar will be charged through P2. The node X2 remains low till the end of the evaluation phase.

B. Precharge phase[7].

In this phase CLK=0 and D can be either 1 or 0. It can also be called as holding mode. The X1 node remains high and X1B will be low. N1 stops the entry of next value of D until the end of pre-charge phase. So the previous output will be held till the next evaluation phase occurs.

This design has negative setup time and positive hold time. It has short transparency period which is due to 1-1 overlap of CLK and CLKB. This overlap eliminates race through problem. Here the inverter pair INV1,INV2 and INV3,INV4 were designed using normal static CMOS style. As these inverter pair is under operation throughout the two phases of the flip flop, it tends to undergo larger run time leakage current. This makes the design to consume unnecessary power when technology shrinks down to 90nm and below.

III. Implementation of T, SR and JK Flip Flops Using Conventional DDFF

The conventional DDFF is used to design dual dynamic node pulsed hybrid T, SR and JK flip flops which are shown in Fig 2, Fig 3, Fig 4. The T flip flop is designed using an XOR gate and conventional D flip flop. The characteristic equation of T flip flop is given as D=TQbar+TbarQ. The output of XOR gate is given as input to the N2 transistor of conventional D flip flop. The XOR gate is designed using PTL technique. The JK flip flop is designed using a multiplexer and and a D flip flop. The characteristic equation of D flip flop is given as D=JQbar+KbarQ. The output of the multiplexer is fed as input to the conventional D flip flop. The multiplexer is designed using NMOS transistor logic. Though it gives weak one as output, the DDFF has dual dynamic nodes which give strong one as output. The SR flip flop is designed using a SR block and a conventional D flip flop. The characteristic equation of SR flip flop is given as D=S+RbarQ which we term here as SR block. The SR block is designed using static CMOS technique. T flip flop has the maximum power dissipation compared to other flip flops because of toggling effect. SR flip flop has the least power dissipation. T flip flop is the fastest flip flop than other flip flops.

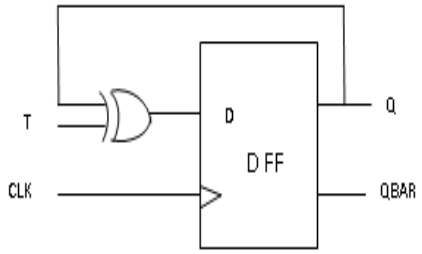

Fig. 2. T flip flop.

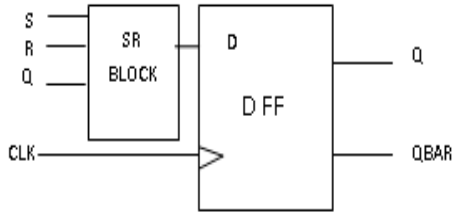

Fig. 3. SR flip flop.

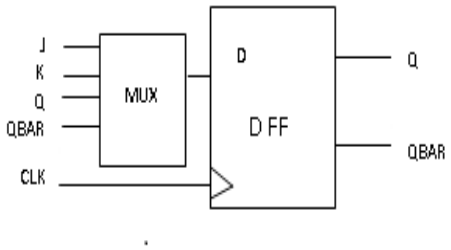

Fig. 4. JK flip flop.

IV. Proposed Flip Flop Architectures

In the proposed flip flop architecture the inverter pairs are designed using leakage power reduction technique known as sleepy stack technique. The static CMOS inverters in conventional DDFF is replaced by sleepy stack inverters because as feature size scales down below 0.1u, leakage power gets increased. When a static CMOS inverter is used in low feature size technology, the supply voltage gets reduced which in turn reduces the threshold voltage [10]. The transistor used were low threshold voltage one. So there is greater risk of leakage current in this case. Short channel length and change in gate length also pave way for higher leakage. This sleepy stack technique is the combination of sleep transistor technique and

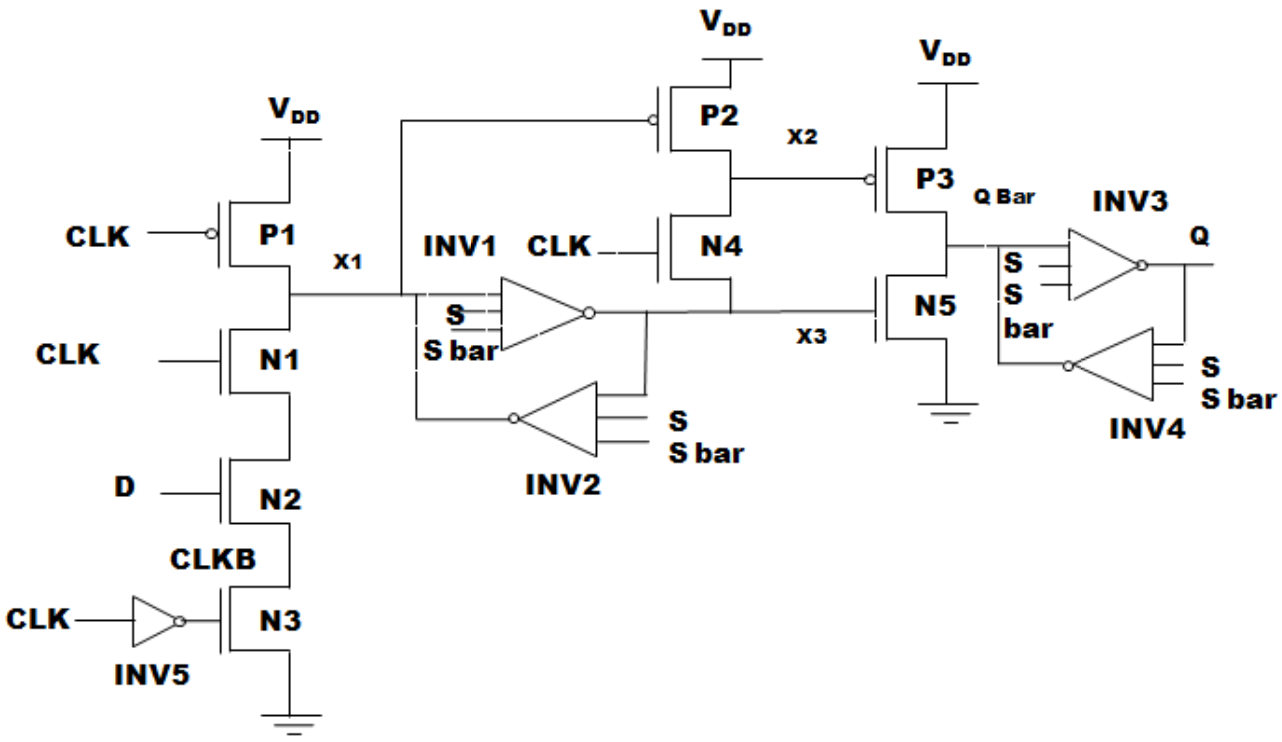

Fig. 5. Proposed D flip flop.

forced stack technique. It uses high threshold voltage transistors and stack effect to reduce the leakage power[3].

The sleepy stack inverter is shown in the Fig 6. P1,P2, N1,N2 are high threshold voltage transistors. P3 and N3 are low threshold voltage transistors. P2 and N2 are sleep transistors. It operates on two modes. 1) Active mode 2) Sleep mode.

A. Active mode

In active mode , S=0 and Sbar=1. The sleep transistors are switched ON throughout this mode. It has faster switching time. As sleep transistors are switched on throughout, it passes the logic values from source to drain and directly into the low V_{th} transistors regardless of the status of transistors which are parallel to sleep transistors[3].

B. Sleep mode

In sleep mode, S=1 and Sbar=0. The sleep transistors are switched OFF. Though they are switched OFF, the transistors parallel to sleep transistors helps in maintaining exact logic state of the design. Reduction in leakage power is achieved by two ways. Firstly high V_{th} transistors parallel to sleep transistors are used to block the leakage current. Secondly by stack effect created by P1, P3 and N1,N3 transistors. When two or more transistor which are stacked together are turned off simultaneously, there is greater reduction in leakage current. This effect is called as stack effect. Suppose when A=1, the stacked NMOS transistors N1, N3 are switched ON and stacked PMOS transistors P1,P3 are switched OFF. Thus the stacked PMOS do not allow any leakage current to pass through. Though there is large leakage power reduction, area is a trade off[3].

The proposed flip flop is shown in Fig 5. When this sleepy stack inverter pair is used in the flip flop, the overall leakage power reduction of the flip flop can be achieved by operating the flip flop in sleep mode.

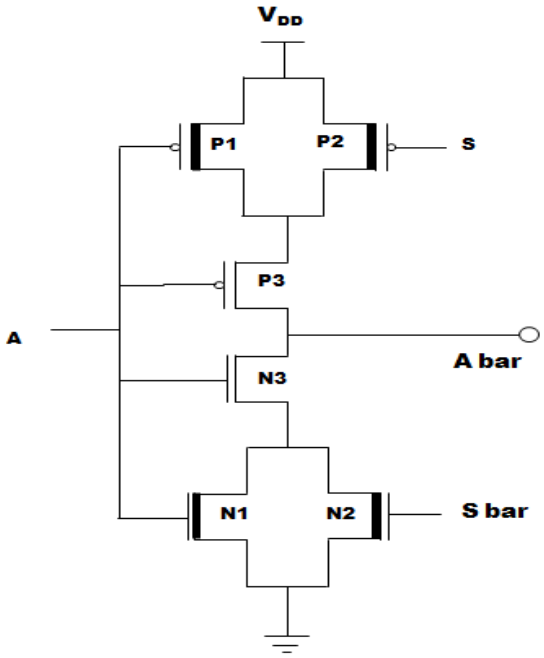

Fig. 6. Sleepy stack inverter

the flip flop in sleep mode. The total power is also reduced which can be obtained by running the flip flop in active mode. This proposed flip flop also operates as like DDFF in

evaluation and pre-charge phase. The latching of input takes place at evaluation phase and holding of the output takes place in pre-charge phase. The overlapping period (T_{ov}) of the flip flop is set as 61ps with supply voltage of 1.8V. Hold time of logic 0 (T_{hold0}) is observed to be 24ps. Hold time of logic 1 (T_{hold1}) is observed to be 35ps. The race around problem is overcome by the 1-1 overlap of CLK and CLKB.

This proposed D flip flop using sleepy stack inverter pair is used to design T,SR,JK flip flops which is shown in Fig.2, Fig.3 and Fig.4. It also exhibits the reduction in power compared to the conventional D,T,SR and JK flip flops.

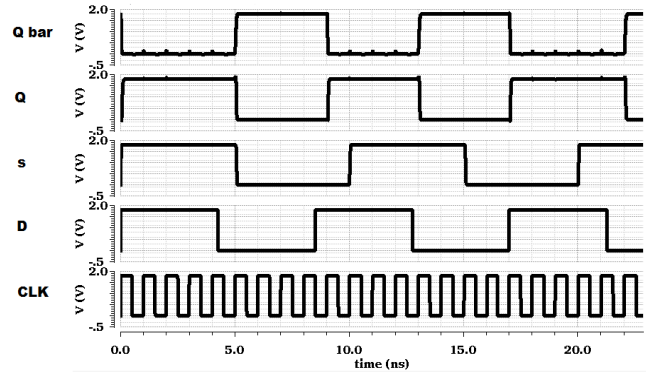

Fig. 7. Timing diagram of Proposed D flip flop.

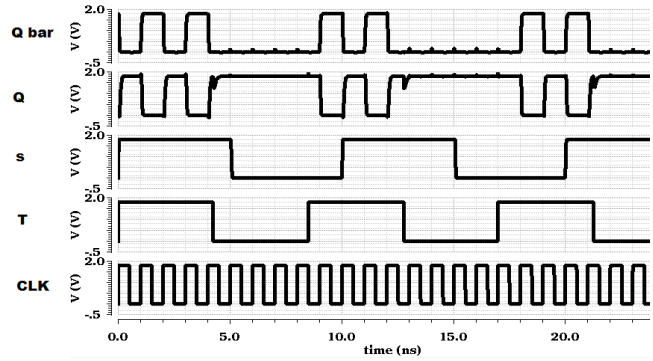

Fig. 8. Timing diagram of Proposed T flip flop.

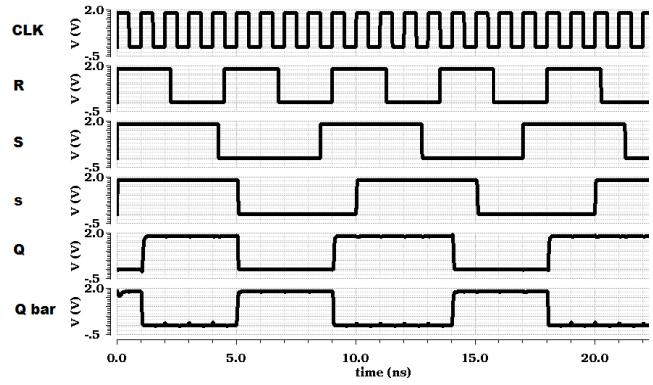

Fig. 9. Timing diagram of Proposed SR flip flop.

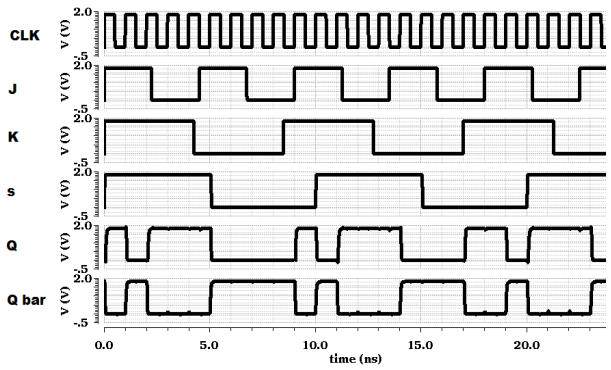

Fig. 10. Timing diagram of Proposed JK flip flop.

V. Experimental Setup and Simulation Results

The simulations were performed under 90nm technology in cadence-virtuoso tool. The supply voltage is given as 1.8V throughout for the entire simulation analysis. The leakage power and total power for static CMOS inverter and sleepy stack inverter were compared. It is observed that sleepy stack inverter has reduced leakage power to 99% and the total power is reduced to 13.8% as given in TABLE I.

The flip flop is operated at 1Ghz clock frequency. It has a negative set up time and positive hold time with respect to 1-1 overlap of CLK and CLKB. The power, delay and PDP are calculated at 25% data activity for the conventional D, T, SR, JK flip flops and proposed D, T, SR, JK flip flops which are given TABLE II, IV, V. The total power is reduced to 20%, 15%, 18%, 13.3% in proposed D, T, SR and JK flip flops. The leakage power is reduced to 89%, 85%, 88%, 90% in proposed D, T, SR and JK flip flops. The total power of T flip flop is observed to be highest. It is because of switching power dissipation. The delay is maintained in the proposed D flip flop as like conventional flip flop. The leakage power and total power is calculated for different data activities of conventional and proposed flip flop.

The total power of proposed flip flop is observed to be less for 25% and 0% data activities when compared with conventional flip flop. The power consumed at 100% data activity is same for both the conventional and proposed flip flops . The static leakage performance of flip flops for various input –output patterns were analyzed. When CLK=1, D=0, Q=0 the static leakage is minimum as given in TABLE VI. This concludes that the run-time leakage power and total power depends on the input vectors also.

TABLE I. Performance of Inverter

INVERTER	Leakage power (pW)	Total power(nW)
CMOS	4041.1	414
Sleepy stack	3.2508	356.8

TABLE II. PERFORMANCE OF D FLIP FLOP

Flip flops	Leakage power (nW)	Total power(µW)	Delay (ns)	PDP (fJ)
Conventional	52.596	63.25	4.6205	292.25
Proposed	5.7438	50.44	4.6175	232.91

TABLE III. TOTAL POWER DISSIPATED AT DIFFERENT DATA ACTIVITIES BY D FLIP FLOP

Flip flops	Total power (µW)			
	100%	*50%*	*25%*	*0%*
Conventional	76.96	73.2	63.17	14.35
Proposed	76.67	82.68	58.97	13.65

TABLE IV. PERFORMANCE OF CONVENTIONAL FLIP FLOPS

Conventional Flip flops	Leakage power (nW)	Total power(µW)	Delay (ns)	PDP (fJ)
D Flip flop	52.596	63.25	4.6205	292.25
T Flip flop	55.404	93.55	2.61	244.17
SR Flip flop	56.34	69.42	4.123	286.22
JK Flip flop	54.72	73.84	2.6175	193.28

TABLE V. PERFORMANCE OF PROPOSED FLIP FLOPS

Proposed Flip flops	Leakage power (nW)	Total power(µW)	Delay (ns)	PDP (fJ)
D Flip flop	5.7438	50.02	4.6175	230.97
T Flip flop	8.0514	78.9	2.6065	205.65
SR Flip flop	8.226	56.74	4.112	233.31
JK Flip flop	5.3082	63.96	2.6145	167.22

TABLE VI. LEAKAGE PERFORMANCE OF D FLIP FLOP AT VARIOUS INPUT-OUTPUT LEVELS

Flip flops	Leakage power (nW)			
	CLK=0 D=0 Q=0	*CLK=0 D=1 Q=1*	*CLK=1 D=0 Q=0*	*CLK=1 D=1 Q=1*
Conventional	53.316	53.316	923000	905400
Proposed	6.12	6.12	0.0225	8974

VI. CONCLUSION

In this paper, an improved power efficient flip flop using sleepy stack inverter pair was proposed. 99% reduction in leakage power was observed in sleepy stack inverter. The leakage power was reduced to 89%, 85%, 88%, 90% in proposed D, T, SR and JK flip flops. The total power is reduced to 20%, 15%, 18%, 13.3% in proposed D, T, SR and JK flip flops.

The best case data activity has been found out. The input-output vectors which gives reduced leakage is found out. As the leakage power depends on the input vectors, when the system is idle low leakage input vectors has to be fed as input to the system. The speed of the flip flop is maintained in the proposed flip flop as like in conventional one. The area is the only trade off.

REFERENCES

[1] H. Patrovi, R. Burd, U.Salim, F.Weber, L. DiGregorio, and D. Draper, "Flow throughnlatch and edge triggered flip flop hybrid elements," in *Proc.IEEE ISSCC Dig. Tech. Papers,* Feb.1997, pp.138-139.

[2] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 2003.

[3] J.C. Park and V. J. Mooney III, "Sleepy stack leakage reduction," IEEE Trans. VLSI Systems, vol. 14, no. 11, pp. 1250-1263, Nov. 2006.

[4] H. Patrovi, R. Burd, U.Salim, F.Weber, L. DiGregorio, and D. Draper, "Flow throughnlatch and edge triggered flip flop hybrid elements," in *Proc.IEEE ISSCC Dig. Tech. Papers,* Feb.1997, pp.138-139.

[5] N. Neodovic and V. G. Oklobdzija, "Hybrid latch flip-flop with improved power efficiency," in *Proc. Symp. Integr. Circuits Syst. Design, 2000, pp.211-215.*

[6] F.Klass, "Semi-dynamic and dynamic flip flops with embedded logic", in *Proc. Symp. VLSI Circuits Dig. Tech. Papers,* Honolulu, HI, Jun. 1998, pp. 108-109.

[7] Kalarikkal Absel, Lijo Manuel, and R.K. Kavitha, "Low Power dual dynamic node pulsed hybrid flip flop featuring efficient embedded logic," IEEE J. Very Large Scale Integration (VLSI) Systems, vol. 21,no. 9,pp. 1693-1704, Sep. 2013.

[8] O. Sarbishei and M. Maymandi-Nejad, "Power-delay efficient overlap-based charge-sharing free pseudo-dynamic D flip flops," in *Proc.IEEE Int. Symp. Circuits Syst.,* May 2007. Pp. 637-640.

[9] O. Sarbishei and M. Maymandi-Nejad, "A novel overlap-based logic cell: An efficient implementation of flip-flops with embedded logic," *IEEE Trans. Verynlarge Scale Integr. (VLSI) Syst.,* vol. 18, no. 2, pp. 222-231, Feb.2010.

[10] Y.-F. Tsai, D. Duarte, N. Vijayakrishnan, and M.J. Irwin, "Implications of technology scaling on leakage reduction techniques," in *Proc. Design Autom. Conf.,* Jun. 2003,pp. 187-190.