Quantum Gate Implementation of a Novel Reversible Half Adder and Subtractor Circuit

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Abstract— In this research work, the transistor level implementation and QCA implementation of TR reversible gate are performed and a comparison between both techniques on the ground of Area is executed. In the later section, a new-fangled design of the reversible adder and subtractor RSG gate is presented. This novel architecture can perform addition and subtraction operation simultaneously, which was never performed before using any of the existing reversible circuits. The proposed novel reversible gate, which uses 2X2 quantum gates and has a quantum cost of five, can be operated as Reversible Half Adder as well as Half Subtractor concurrently. The reversible gate proposed in this research will find numerous applicability in several DSP applications where half adder and half subtractor operates simultaneously.

Keywords— Reversible Computing; QCA; RSG; Quantum Computers; CNOT; C-V and C-V+ gates.

I. INTRODUCTION

Reversible rationale is developing as an ideal registering standard with applications in different fields, for example, optical processing, quantum figuring, quantum dot cellular automata, DNA processing and so on. Reversible circuits are data lossless circuits, in this one of a kind yield is produced for each input vector and the other way around. In a clear way, there ought to be balanced mapping among data sources and yields. Sources of info and Outputs ought to be bijective in nature. As per the literature, Landauer (in 1961) recommended that for any irreversible rationale calculation each lost bit information causes kTln2 joules of heat dissipation, where k is Boltzmann's constant and T is the absolute temperature at which calculation is carried out [2]. Further in 1973 Bennet hypothesized that energy dissipation will be null if the calculation is completed in a reversible way utilizing reversible gates [3]. One of the prime use of reversible rationale is in quantum figuring. A quantum PC works on single or multiple two-state quantum frameworks called as qubits. Each qubit is fit for speaking to 0 and 1 simultaneously. For a reversible circuit, a) garbage outputs b) delay and most importantly c) quantum cost act as most significant parameters [4][5]. The garbage yields are utilized as a part of reversible circuits with a specific end goal to keep up the principle of reversibility. Be that as it may, as a yield there is no noteworthiness of garbage yield. For any reversible gate to be used in quantum computing, it should be transformed into its quantum gate implementation, then only it can be utilized in quantum computers. Quantum Computers can possibly achieve certain computations altogether quicker than semiconductor-based PCs. This processing isn't obliged to two states however this encodes the information as quantum bits or qubits which exist in superposition. Qubits speak to ion, atom, photon or electron and their individual control gadgets that are coordinating to go about as PC memory and processor. Quantum Dot Cellular Automata (QCA) [12] was introduced in 1993. It was firstly verified in 1997[6]. The QCA is relied upon to accomplish high device density, low power consumption and very high-speed of operation. QCA is built as a 2-D cluster of quantum cells, in which each cell has an electrostatic communication with its neighboring cells. The basic circuits for QCA are majority gates, these gates work on the principle of majority input will win and become the output of circuit. In the literature many Majority gates are available these may be of three inputs, five inputs [14] and seven inputs [15] majority gate also. There are many reversible gates available in the literature like Feynman Gate, Toffoli Gate [7], Peres Gate [8] etc. We have synthesized and simulated TR gate [1] using two different simulation environments to verify the logic, this kind of work is itself a unique because this type of comparison regarding reversible gates are never done before in the literature. A new reversible gate is proposed in this paper which can serve as adder and subtractor simultaneously.

The paper is organized as follows: section II presents the basics of reversibility & quantum implementation of various reversible gates; Section III presents the delay calculations in reversible circuits; Section IV presents experimental results of TR gate in different simulation environment; Section V presents proposed RSG gate and its quantum gate implementation; Section VI presents proposed design for reversible full adder and subtractor; Section VII provides discussion and conclusions.

II. BASIC REVERSIBLE GATES

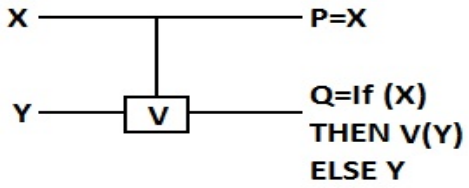
As per the studies [9], "the number of 1x1 and 2x2 reversible gates or quantum gates required in a design is referred to as quantum cost". The quantum cost of all 1 input vs 1 output and 2 inputs vs 2 outputs gates is taken as unity [9], [10], [11]. At the end of the day, the quantum cost of the reversible circuit is figured by checking the total quantities of NOT, CNOT, Controlled-V, and Controlled-V^+ gates required in a reversible circuit execution.

978-1-5386-6483-4/18/$31.00 ©2018 IEEE
DOI 10.1109/ICICS.2018.00027

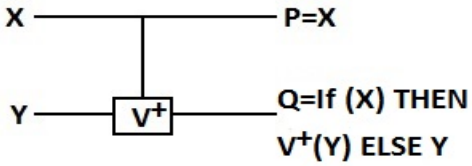
A. NOT Reversible Gate

A NOT reversible gate is a one input and one output (1 x 1) gate. It's quantum cost is unity.

(a) NOT Gate



(b) C-V/Controlled-V Gate



(c) C-V+/Controlled-V+ Gate

Fig. 1. The NOT, C-V and C-V+ Gates

B. C-V and C-V+ Reversible Gates

The basic properties of C-V and C-V^+ quantum gates are as follows:

$$V+V = NOT$$

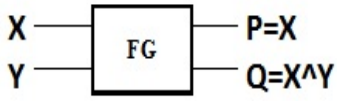
$$V+V^+=V^++V=identity$$

$$V^++V^+ = NOT$$

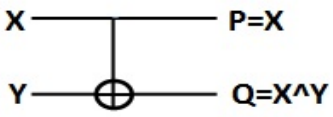
The above-mentioned properties demonstrate that when 2 V gates are in a series arrangement ("+") they act as a NOT gate. Furthermore, when 2 V^+ gates are in series arrangement they excessively act as a NOT gate. 1 V gate in series arrangement with another V+ gate (and the other way around) is an identity.

C. Feynman Gate (CNOT Gate)

It is a 2 inputs and 2 outputs reversible (2 x 2) gate having the mapping of (X,Y) to (P = X, Q = X xor Y). Where X and Y are data inputs and P and Q are outputs. It has a quantum cost of solidarity.



(a) Symbolic representation of CNOT Gate

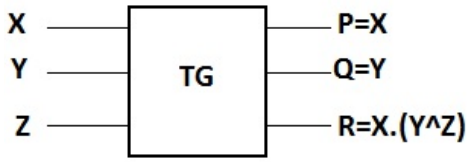


(b) CNOT Gate

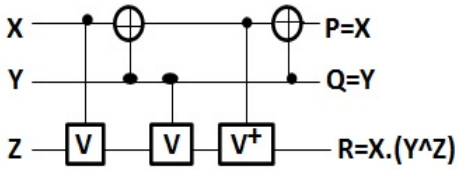
Fig. 2. CNOT gate and its symbolic representation

D. Toffoli gate

It is a 3 input & 3 output (3 x 3) reversible gate as shown in Fig. 3(a). It has the mapping of inputs X, Y and Z with the outputs P, Q and R as P = X, Q = Y and R = X & (Y xor Z). This gate consists of one V+ gates, two V gate and two CNOT gate. Therefore, the quantum cost of Toffoli gate is five as shown in Fig. 3(b) [7].



(a) Symbolic representation of Toffoli Gate

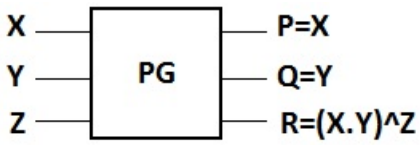


(b) Toffoli Gate

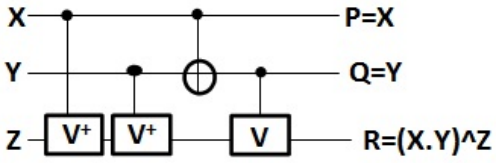
Fig. 3. Toffoli gate and its symbolic representation

E. Peres Gate

As per as the total number of inputs and outputs are concerned, Peres gate is same as Toffoli gate. Other than that, this reversible gate is having the mapping of inputs X, Y and Z with the outputs P, Q and R as P = X, Q = X xor Y and R = (X.Y xor Z) [8]. Fig 4(b) shows the Peres Gate and 4(a) shows the symbolic representation of Peres Gate. This gate consists of two V+ gates, one V gate and one CNOT gate. Therefore, the quantum cost of Peres gate is four.



(a) Symbolic representation of Peres Gate



(b) Peres Gate

Fig. 4. Peres gate and its symbolic representation

III. DELAY CALCULATION FOR REVERSIBLE CIRCUITS

Delay is another noteworthy parameter that demonstrates the effectiveness of the reversible circuit. As delay is constantly figured through critical path of the circuit subsequently, delay speaks to the lengthiest path of

the circuit. The delay of any reversible gate is figured through the quantity of quantum gates utilized as a part of a reversible circuit. Therefore, Feynman gate has 1 unit, Toffoli gate has 5 units and Peres gate has 4 units of delay.

IV. EXPERIMENTAL RESULTS

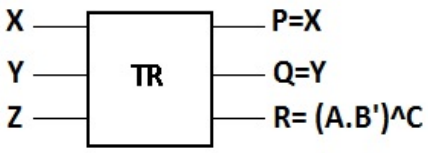


Fig. 5: TR Gate

In this research work, TR gate [1] is simulated in two different simulation environments. TR reversible gate is used as half subtractor. Fig. 5 shows the symbolic representation of TR gate and Table I shows truth table of TR gate. First result is opted using Cadence ASSURA 180nm, with no DRC error, the layout of TR gate is shown below in Fig. 6. Further same gate is designed in QCA Designer 2.0.3 [13] Layout Tool. The QCA layout is shown in Fig. 7.

TABLE I. TRUTH TABLE OF TR REVERSIBLE GATE

"X"	"Y"	"Z"	"P"	"Q"	"R"
F	F	F	F	F	F
F	F	T	F	F	T
F	T	F	F	T	F
F	T	T	F	T	T
T	F	F	T	T	T
T	F	T	T	T	F
T	T	F	T	F	F
T	T	T	T	F	T

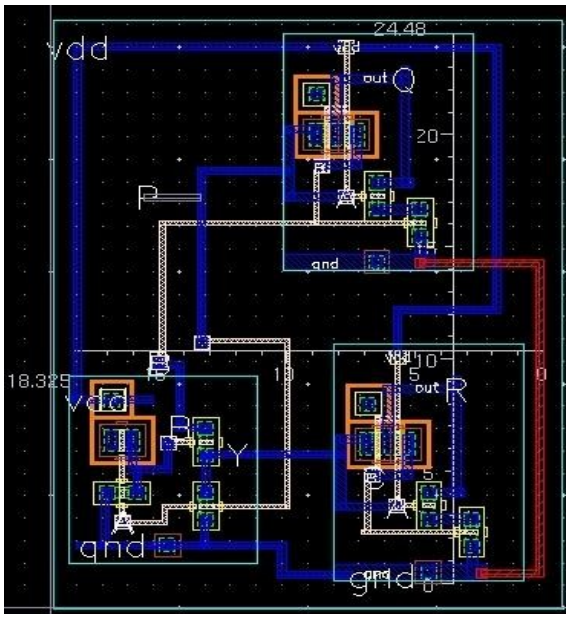


Fig. 6. Layout of TR Gate using cadence ASSURA

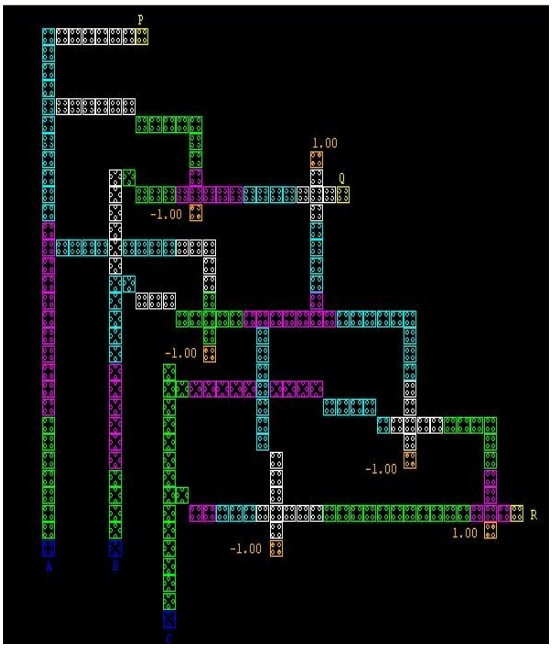


Fig. 7. QCA Layout of TR Gate

A comparative analysis between transistor technique and transistor less technique on the ground of area is shown in Table II below where as table III shows the area improvement in QCA.

TABLE II. COMPARISON OF AREA OF TR GATE

CMOS_180nm			QCA		
Length (μm)	Width (μm)	Area ($μm^2$)	Length (nm)	Width (nm)	Area ($μm^2$)
24.48	18.325	**448.6**	727.60	742.03	**0.54**

TABLE III. IMPROVEMENT OF AREA

CMOS_180nm	QCA	% Improvement in Area
448.6	0.54	9

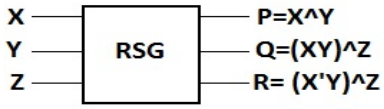
V. PROPOSED REVERSIBLE HALF ADDER AND SUBTRACTOR

In this paper a novel reversible RSG gate which can be served as reversible adder as well as subtractor simultaneously is proposed. As sum or difference of any two-bit digit is same, only the difference occurs in carry and borrow bit. Hence, we designed this gate using 3-inputs and 3-outputs taking reversibility into the consideration, which is the key factor of reversible gate. The proposed gate does not spoil any rule of reversibility. Table IV shows the truth table of RSG gate, Fig. 8(a) shows the RSG gate; 8(b) shows RSG gate as reversible half adder and subtractor; 8(c) shows its quantum implementation and 8(d) shows quantum implementation of reversible adder and subtractor. RSG gate has mapping

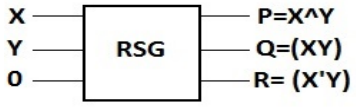
of (X, Y, Z) to (P= X xor Y, Q = (XY)xor Z, R= ($\overline{X}$ Y)xor Z.

TABLE IV. TRUTH TABLE OF RSG REVERSIBLE GATE

"X"	"Y"	"Z"	"P"	"Q"	"R"
F	F	F	F	F	F
F	F	T	F	T	T
F	T	F	T	F	T
F	T	T	T	T	F
T	F	F	T	F	F
T	F	T	T	T	T
T	T	F	F	T	F
T	T	T	F	F	T

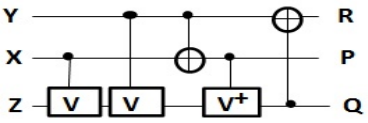


(a) Symbolic representation of RSG Gate



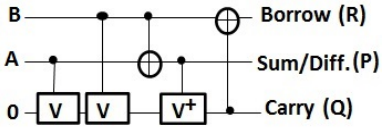
(b) RSG gate as reversible adder and subtractor

As we keep Z input as '0' P works as Sum/Diff, Q as Carry and R as Borrow.



(c) RSG Gate

We have modified the order of inputs and outputs as presented in the block diagram just to optimize its quantum cost, there will be no effect on the outputs and on its reversibility as well.



(d) RSG Gate as Adder and Subtractor

Fig. 8. RSG gate, RSG as Half adder and Subtractor and its quantum cost implementation

Let's take an example of any combination suppose A=1 and B=0, then first V gate will invert the bit at C that is 0 to 1 as its control pin is high, next V gate will pass this bit as it is because its control bit is low. Next V^+ gate will invert the incoming bit as its control pin is high, hence finally we will get P=1, Q =0 and R = 0 which is the required result.

This design is outperformed the TR gate as in terms of garbage output, it has quantum cost of 5 units, but this can be compensated in terms of both simultaneous arithmetic operations. Below Table V shows the comparison between TR[1] gate and RSG gate.

TABLE V. A COMPARISON OF TR AND RSG GATE

	QC	Delay	I/O Pins	Garbage Outputs
TR	4	4	3	1
RSG	5	5	3	0

VI. PROPOSED REVERSIBLE FULL ADDER CUM SUBTRACTOR

The proposed RSG gate can further be used to design reversible full adder cum subtractor. The design requires 3 RSG gates to design one complete unit of reversible full adder cum subtractor module. This module can be further used as to design ripple carry adder and subtractor. The proposed design is shown in Fig. 9 below. Here G1 and G2 are garbage outputs.

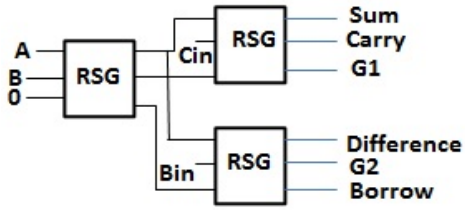


Fig. 9. Reversible Full Adder and Subtractor using RSG

VII. DISCUSSION AND CONCLUSION

In this research work, an efficient comparison between two different techniques is presented where QCA has outperformed the current existing technology of transistors. Now the era will come in which much more works will be done at atomic or molecular level. The comparison of area has proved that the QCA is the most promising and upcoming technology. The proposed RSG gate is very efficient in terms of garbage output. To optimize proposed reversible full adder and subtractor in terms of inputs and outputs counts and quantum cost can be the future scope for this research work.

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