Comparative Analysis of Carry Select Adder using 8T and 10T Full Adder Cells

Shivendra Pandey, *Member, IEEE*, Afshan Amin Khan and Rajkumar Sarma

***Abstract*—This paper present a comparison between the design of the 8T adder based Carry Select Adder (CSA) and 10T adder based CSA. Using both the designs of adders 4-bit CSA architecture has been developed and compared with the 28T adder 4-bit CSA. The 10T CSA design has reduced delay, power and area as compared with the 28T CSA with a slight tradeoff for area as compared to 8T CSA. The analysis shows that the 10T CSA is better than both 8T adder based CSA and 28T CSA. This work evaluates the performance of the 10T CSA design in terms of power, delay and area using 180nm CMOS process technology Cadence Virtuoso tool and Spectre simulator.**

***Index Terms*— Carry Select Adder (CSLA); Low power; Binary Excess -1 Converter (BEC), 10 Transistor adder.**

I. Introduction

IN recent years a large amount of the research effort has been given to improve the system architectures as a whole such as ALU, FIR Filters, FFT implementation etc., however the backbone of a digital system is a adder block. Thus improvement of the adder block will lead to the improvement of the system as a whole without any change in the architecture of the system. This works provides a detailed analysis of the already existing architecture of CSA [1] by making use of 28T [2], 8T [3], and 10T [4] adder. In the current VLSI industry optimization of both power and speed are of prime importance since the demand of the consumers is not only restricted to smaller size of the devices but also higher speeds with longer battery life. In order to achieve such a design specification high speed architectures are to be considered one such architecture is CSA than provides a good speed and lower power consumption with area trade off. The CSA is used in many computational systems to alleviate the problem of carry propagation delay by independent generating multiple carries and then select a carry to generate the sum. However, the CSA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by the multiplexers (MUX) [5].

This paper is organized as follows, in section II, we examine the existing CSA with BEC using 28T, in section III Implementation of CSA using 8T, in section IV Implementation of CSA using 10T, section V simulation and result analysis are discussed. The last section includes conclusion and references.

II. Existing CSA With BEC Using 28T Full Adder Cell

The Existing work gives the implementation of the CSLA using 28T [2] 1- bit full adder. For each full adder block in first level RCA block with Cin=0, and in second level Binary Excess Converter (BEC) is used instead of RCA with Cin=1 in regular CSA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. Hence reduces the area and power consumption of the regular CSLA to replace the n-bit RCA by an n+1-bit BEC. A structure and the function table of a 4-bit BEC are shown in Fig.1 and Table I respectively [6].

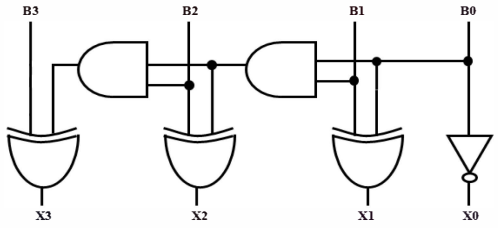

Fig.1 4-bit Binary Excess Converter

One of the biggest advantages of using this BEC logic is that when large amount of the bits are sent to CSA for addition BEC logic usage saves a very large amount of area as compared to RCA which is used in the conventional CSA. The equation (1) shows Boolean expression of 4-bit Binary Excess Converter [1].

$$\begin{aligned} X0 &= \overline{B0} \\ X1 &= B0 \oplus B1 \\ X2 &= B2 \oplus (B0 \,\&\, B1) \\ X3 &= B3 \oplus (B0 \,\&\, B1 \,\&\, B2) \end{aligned} \quad (1)$$

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TABLE I
FUNCTION TABLE OF THE 4-BIT BEC-1

B[3:0]	X[3:0]
0000	0001
0001	0010
0010	0011
⋮	⋮
1110	1111
1111	0000

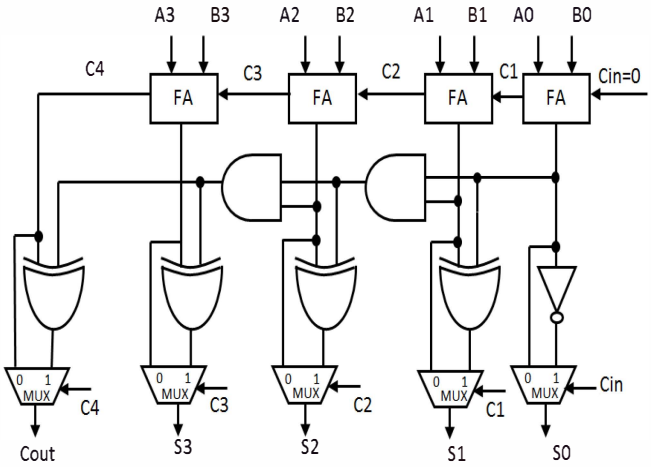


Fig.2 Architecture of Carry Select Adder with BEC

The architecture and basic function of the CSA is illustrated in Fig.2 by using the 4-bit BEC together with the MUX. One input of the 2:1 MUX gets output of RCA for Cin=0 and another input of the MUX is the BEC output. This produces the two possible partial results in parallel and the MUX is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large area reduction when the CSA with large number of bits are designed [6].The above Figure has one 4-bit RCA which has 3 Full adder (FA) and 1 FA for Cin=0. Instead of another 4-bit RCA with Cin=1 a 4-bit BEC is used which adds one to the output from 4-bit RCA [1].

III. CSA USING 8T FULL ADDER CELL

The basic cell used is 8T full adder [2], this cell comprises of three PMOS with a fixed gate negative voltage at volt terminal shown in Fig.3. The advantage of using negative fixed gate supply is that it keeps PM3 always slightly on so as to improve the output response of the XOR circuit. One of the big advantage of using 8T adder cell as basic cell is that area is reduced to a great deal but has a disadvantage of very much decreased driving capabilities. However the variation in W/L of the transistors can be done so as to improve the driving capabilities of the circuits, with a limit at the further optimization. Since if we further optimize the W/L ratios it

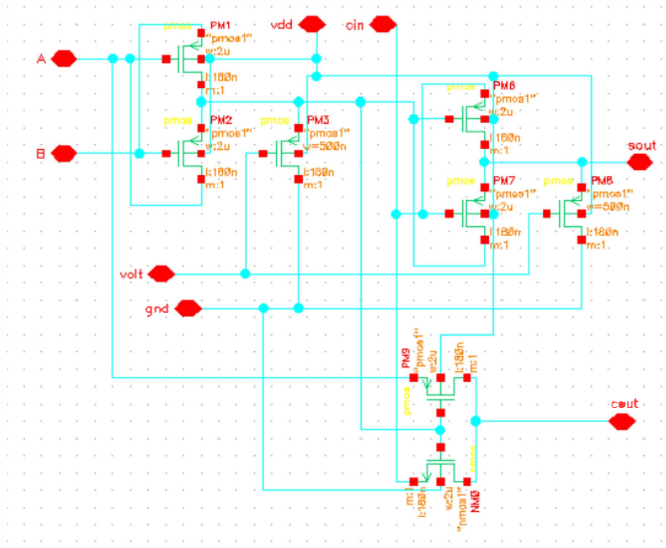


Fig.3 8T full adder cell

will lead to large amount of increase in the power as compared to the improvement of the output response.

The 4-bit CSA [1] designed using above 8T adder cell was implemented using the architecture shown in Fig.2. After the detailed analysis of the designed CSA it was observed that the output for the CSA is having serious threshold loss problems and both power and delay are very large. Thus may go beyond the practical usable range, since the 8T adder cell does not drive the cascaded structures.

IV. CSA USING 10T FULL ADDER CELL

The basic cell used in this CSA is a 10T full adder [3] shown in Fig.4. The full adder promises to be better in terms of the threshold loss problem as compared to the 8T full adder an also gives lower amount of the power consumption with an area trade off of two MOS devices. An improved version of 10T is used by varying the W/L ratio to a satisfactory level so as to achieve required driving capability.

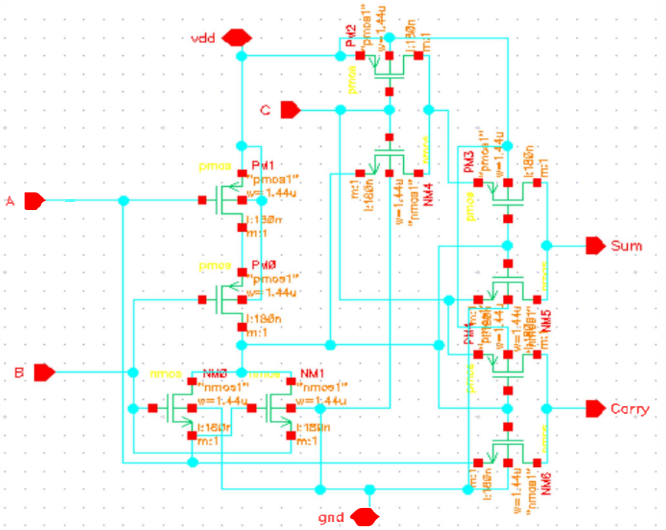


Fig.4 10T full adder cell

The 4-bit CSA [1] architecture shown in Fig. 2 is designed using the above 10T adder cell and the detailed analysis show that there is a very large improvement in the power consumption of CSA as well as compared to its 8T CSA variant. However here also some amount of degradation is seen but that can be acceptable for cascaded structures.

One of the reasons of this degradation is the use of 2T MUX at the last stage of the CSA. The use of this MUX adds to the already existing degradation of this CSA. The design of 2T MUX is given in Fig.5. This 2:1 MUX is used to select correct sum and carry output based on carry coming from previous stage [1]. It is implemented in Gate Diffusion Input (GDI) technique, and is bound to give some degradation.

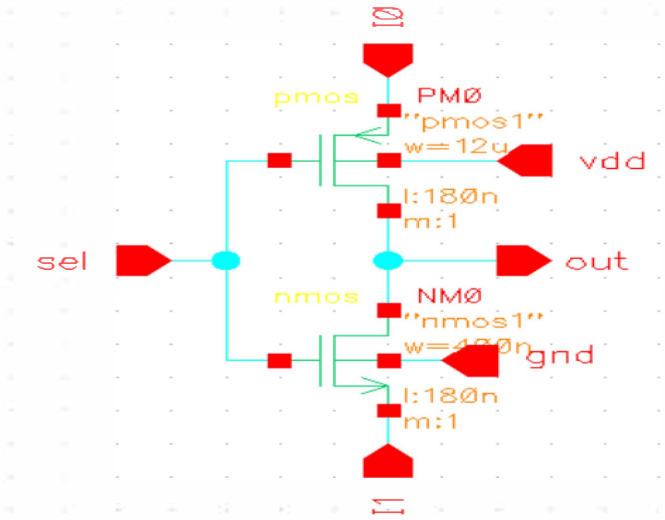


Fig.5 2T MUX cell

V. Simulation and Result Analysis

Table II illustrates power, delay and its power-delay product (PDP) of 28T, 8T and 10T CSA. Table shows that power and area of the 10T CSA are reduced as compared to 28T CSA more over the power and delay response is better in comparison to 8T as well. Hence the given design of the 10T CSA prove to be more reliable in terms of delay, power and PDP, hence becomes a preferred choice of the designer. The respective waveforms for output response of 28T CSA, 8T CSA and 10T CSA are shown in Fig.6, Fig.7 and Fig.8 respectively. And their average power waveforms and bar chart are shown in Fig.9, Fig.10, Fig.11 and Fig.12 respectively.

TABLE II
Comparative Analysis of Performance Parameters

Parameter	Existing CSA 28T	CSA 8T	CSA 10T
Power(µw)	96.6	363.8	86.85
Delay(ns)	9.23	22.08	3.08
PDP(fJ)	891.61	8032.7	104.02
No. of Transistors	184	104	112

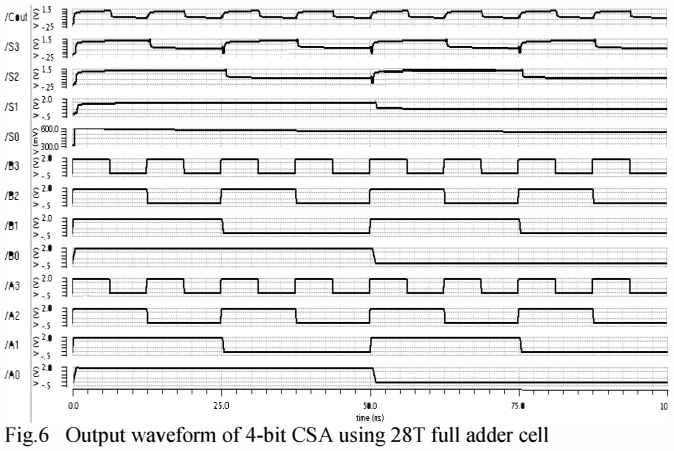


Fig.6 Output waveform of 4-bit CSA using 28T full adder cell

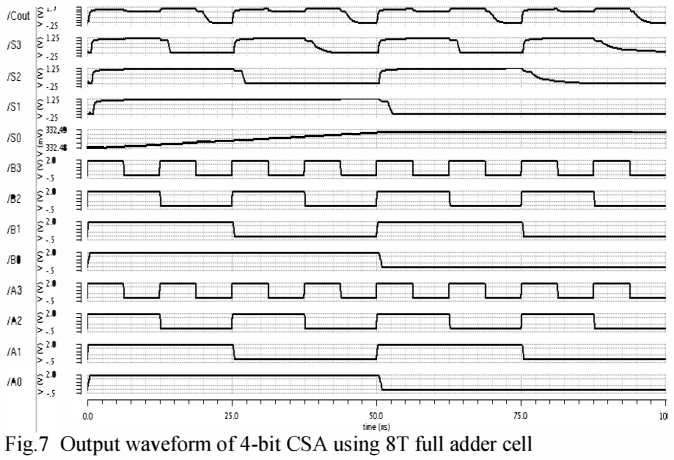


Fig.7 Output waveform of 4-bit CSA using 8T full adder cell

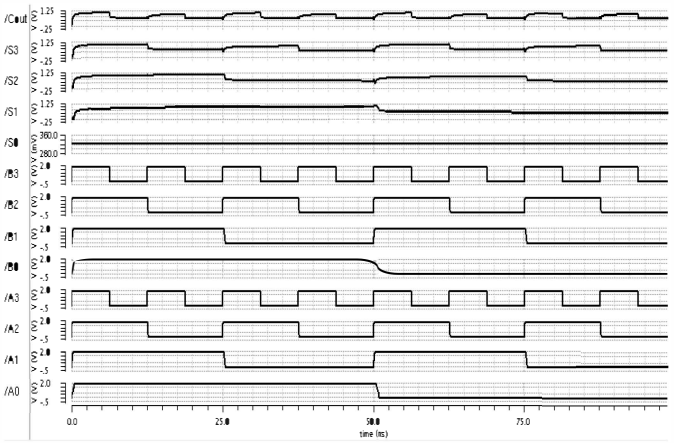


Fig.8 Output waveform of 4-bit CSA using 10T full adder cell

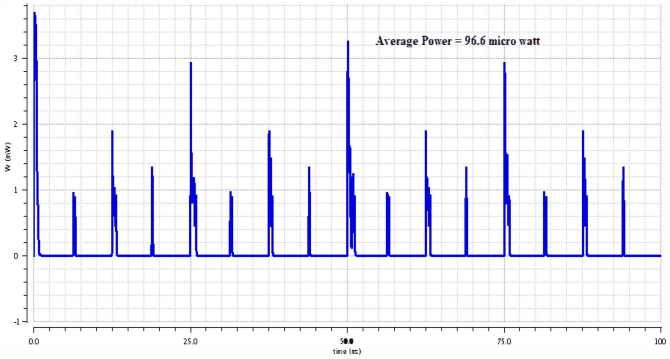


Fig.9 Average power of 4-bit CSA using 28T full adder cell

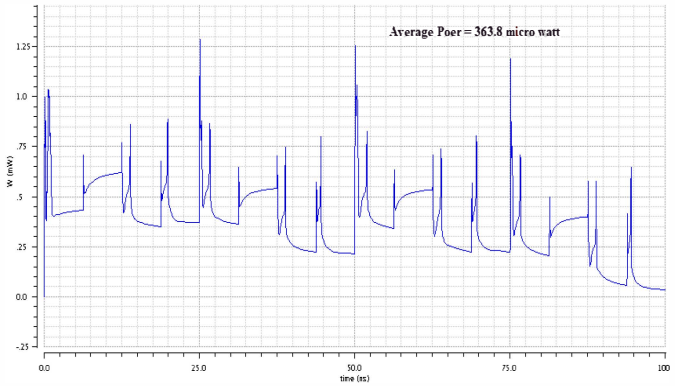


Fig.10 Average power of 4-bit CSA using 8T full adder cell

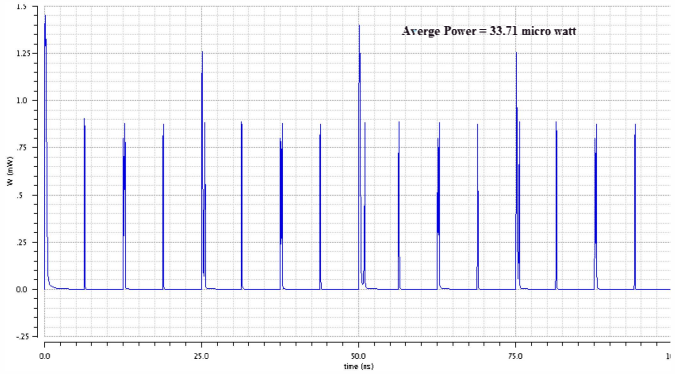
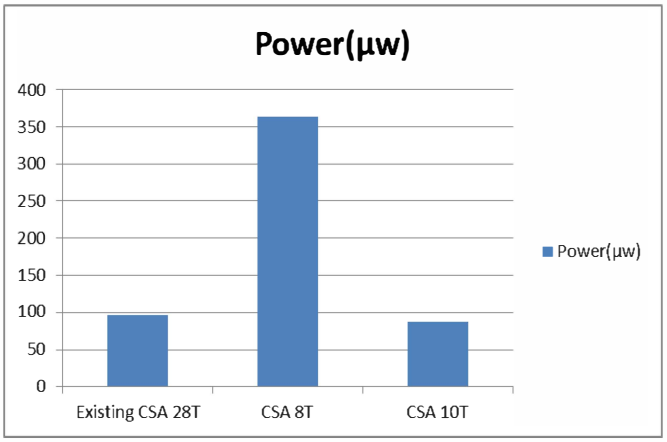
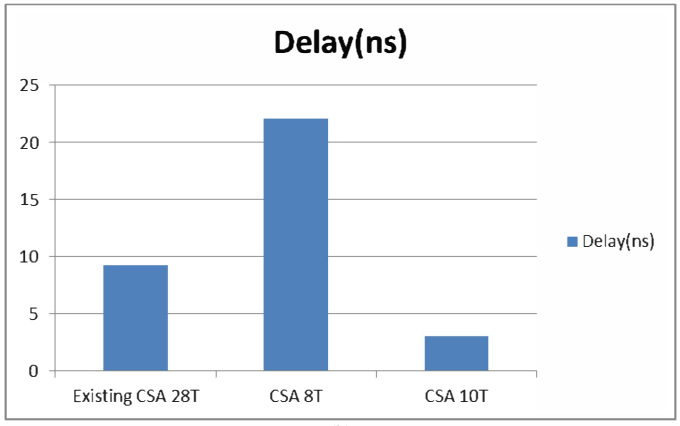


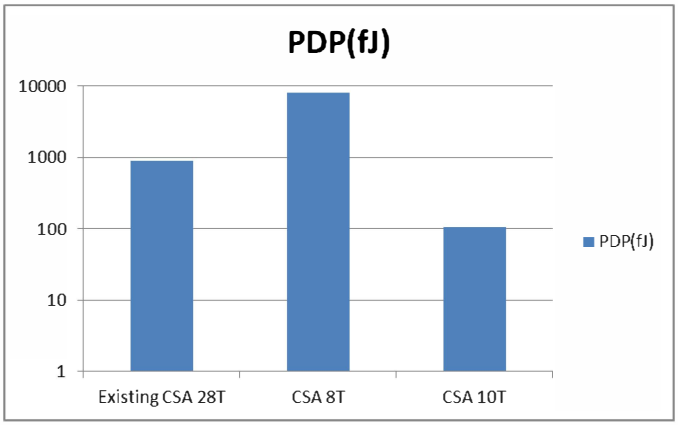
Fig.11 Average power of 4-bit CSA using 10T full adder cell



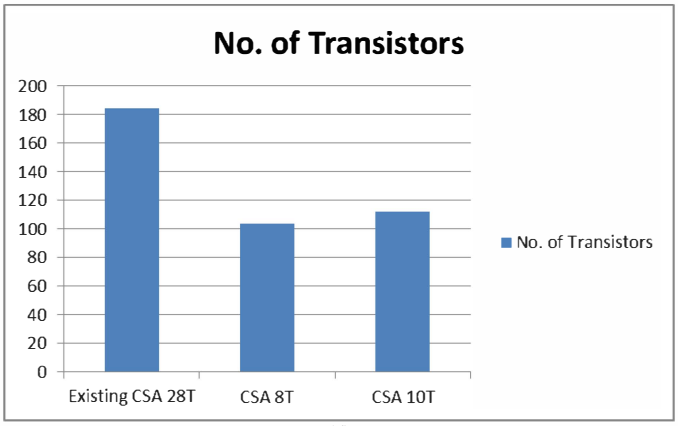
(a)



(b)



(c)



(d)

Fig.12 (a) Power(µw) (b) Delay(ns) (c) PDP(fJ) (d) No. of transistors

VI. CONCLUSION

In This paper, we have shown the design of carry select adder implementation using 10T full adder cell using BEC-1 approaches, therefore critical path has been optimized. The amount of power requirement for 10T CSA is reduced by 90.73% compared to 8T CSA and 65.10% compared to 28T CSA. The improvement in delay is 86.20% compared to 8T CSA and 66.56% compared to 28T CSA. However required no. of transistor is increased by 7.69% compared to 8T CSA and is reduced by 39.13% compared to 28T CSA. The compared result show that the 10T CSA has slightly larger area but the delay and power of the 10T CSA are significantly reduced. So we can say that 28T full adder cell is compatible for multiple stages in cascaded structure of any system, while 8T full adder cell is not compatible for multiple stages in cascaded structure and 10T full adder cell is compatible for multiple stages in cascaded structure but limited. Minimum no. of transistors count for full adder cell is 10T, which have driving capability of multiple stages in cascade. The future scope of this work can be taken to implement the higher order bit CSA by using 10T full adder cell.

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