Proceedings of the IASTED International Conference
Engineering and Applied Science (EAS 2012)
December 27 - 29, 2012 Colombo, Sri Lanka

DESIGN AND PERFORMANCE COMPARISON ANALYSIS OF HYBRID ADDERS

Rajkumar Sarma[#1] and Jyotirmoy Pathak[#2]
[#]School of Electronics Engineering, Lovely Professional University, Phagwara, Punjab- 144402, INDIA
[1]rajkumar.sarma86@gmail.com, [2]jyotirmoy4ever@gmail.com

ABSTRACT
Adder cell using Pass Transistor Logic (PTL) and Gate Diffusion Technique (GDI) is been described in this paper. GDI technique allows reducing power consumption, propagation delay and low PDP (power delay product) whereas Pass Transistor Logic (PTL) reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Performance comparison with various Hybrid Adder is been presented. In this paper, we propose a new PTL-GDI based cell designs, which is found to be much more power efficient in comparison with existing design technique. The significance of these designs is substantiated by the simulation results obtained from Cadence Virtuoso 180nm environment.

KEY WORDS
PTL, GDI, PDP, Low Power, Full Adder, VLSI.

1. INTRODUCTION

Full adders are fundamental units in various circuits, especially in circuits used for performing arithmetic operations such as compressors, comparators, parity checkers, and so on. Full adders are often in the critical paths of complex arithmetic circuits for multiplication and division. These in turn form the core of any system and thereby influence the overall performance of the entire system. Enhancing the performance of the full adder can significantly affect the system performance. Figure 1 shows the power consumption breakdown in a modern day high-performance microprocessor. The data path consumes roughly 30% of the total power of the system. Adders are an extensively used component in data paths and, therefore, careful design and analysis is required for these units to obtain optimum performance.

On the other hand, as discussed in [4], we can see from the Figure 1 that clock signals consumes 45% of the total power, which is very high in fact. As power dissipation has become one of the most important constraints in the design flow of modern processors, therefore, under this common scenario, it has become extremely important to consider the power consumption of any proposed module when there are non-transitioning input data or there is no clock signal activity.

The integrated circuit performances are restricted by how best the arithmetic operators are implemented in the cell library provided to the designer for the synthesis. As the complexity of arithmetic circuits grows with increasing processor bus width, energy consumption is becoming more important now than ever due to the increase in the number and density of transistors on chip and faster clock. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles. For example the goal to extend the battery life span of portable electronics is to reduce the energy expended per arithmetic operation, but low-power consumption need not necessarily implies low energy. To execute an arithmetic operation, a circuit can consume very low power by clocking at extremely low frequency but it may take a very long time to complete the operation.

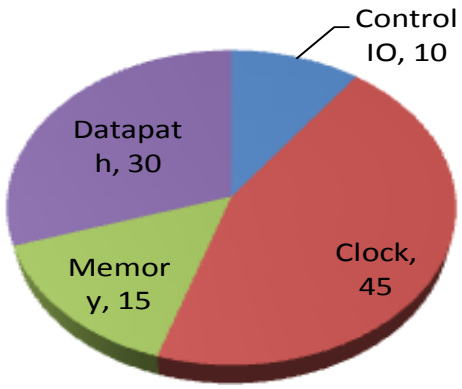

Figure 1. Power consumption by various units

In the next Section different traditional logic styles are discussed. In Section 3 & 4 different hybrid adders & Proposed Adder is been discussed. Finally a comparison of different adder with the proposed adder is been done in Section 6.

2. DIFFERENT LOGIC STYLES

Several logic styles have been used in the past to design full adder cells. Each design style has its own merits and demerits. Classical designs of full adders normally use only one logic style for the whole full-adder design. For

DOI: 10.2316/P.2012.785-123

example the static CMOS design. The main principle behind CMOS circuits that allows them to implement logic gates is the use of p-type and n-type metal–oxide–semiconductor field-effect transistors to create paths to the output from either the voltage source or ground. When a path to output is created from the voltage source, the circuit is said to be pulled up. The other circuit state occurs when a path to output is created from ground and the output pulled down to the ground potential.

Another very popular design is Pass Transistor Logic design. When an NMOS or PMOS is used alone as an imperfect switch, we sometimes call it a Pass Transistor. PTL reduces the numbers of transistors used to make different logic gates, by eliminating excess amount of transistor. Transistors are used here as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages (Vdd).

When both an NMOS and a PMOS transistor are connected in parallel to pass the signal, the circuit is referred to as a CMOS transmission gate. Transmission gate logic circuit is a kind of pass-transistor logic circuit. It is built by connecting a PMOS transistor and a NMOS transistor in parallel, which are controlled by complementary control signals.

Another conventional adder is the complementary pass-transistor logic (CPL). The complexity of CMOS Pass Gate logic can be reduced by dropping the PMOS transistor and using NMOS pass transistor. This technique is known an CPL. In this case, CMOS inverters must be used periodically to recover the full Vdd level since the NMOS pass transistor will provide a VOH of (Vdd-Vtn) in some cases. The CPL circuit requires complementary inputs and generates complementary outputs to pass on to the next CPL stage. It provides high-speed, full-swing operation and good driving capability due to the output static inverters. But due to the presence of a lot of internal nodes and static inverters, there is large power dissipation.

GDI method is based on the use of a simple cell as shown in Figure 2. At the first look the design is seems to be like an inverter, but the main difference is 1) GDI consist of three inputs- G (gate input to NMOS/PMOS), P (input to source of PMOS) and N (input to source of NMOS). (2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter. Figure 2 shows the basic GDI cell.

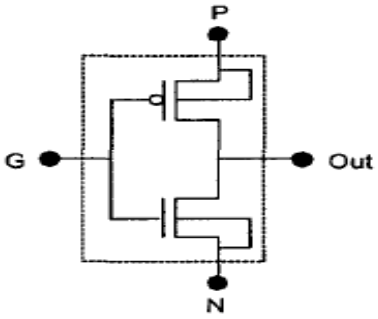

Figure 2. Basic GDI cell

Table 1 shows, as discussed in [9], how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6- 12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only 2 transistors per function) in GDI design method.

Table 1
Various Logic Functions of GDI Cell for Different Input Configurations, as in [9].

N	P	G	Out	Function
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

From the above discussion it is seen that different logic style has different merits and demerits. Moreover the main problem that is been faced by Hybrid adder circuits are power dissipation and time delay. Our main in this proposed design will be to reduce the delay with optimized power consumption and hence to reduce the Power Delay Product (PDP).

3. DIFFERENT HYBRID ADDERS

Several low-power and high-performance 1-bit hybrid Full Adder cells have been reported in the literature [1]. Here four different hybrid Full Adder Cells, which were reported to have better performance than others are reviewed and analyzed. The adders considered in this work were designed using traditional implementing methods, i.e. they use only transistors and no use input capacitors.

In Radhakrishnan Adder [5] a minimal transistor CMOS pass network XOR-XNOR cell that is fully compensated for threshold voltage drop in MOS transistors, is presented by the author. This new cell can reliably operate within certain bounds when the power supply voltage is reduced to certain level. It uses only six transistors for the combined XOR-XNOR cell and can operate reliably when the supply voltage is scaled down, as long as the voltage is not allowed to fall below double of threshold voltage. The total number of transistor used here for full adder operation is 14. The Design circuit is shown in Figure 3.

The Chang Adder [3] uses 26 transistors and it utilizes a modified low-power XOR/XNOR circuit. In this circuit worst case delay problems due to logic transitions are solved by adding more transistors; however, these additional transistors increase the power consumption of the full adder cell. Figure 6 shows Design circuit.

The Goel Adder [4] uses a XOR–XNOR circuit which can produce balanced full swing output. It has high-speed operation due to the cross-coupled PMOS Pull-up

transistors providing the intermediate signals quickly and a hybrid- MOS output stage with a static inverter at the output. The Design circuit is shown in Figure 4.

The Agarwal Adder [2] uses the Complementary Pass transistor Logic (CPL). This adder is mainly composed by NMOS transistors with pull–up PMOS transistors to obtain full swing output voltage. Due to positive feedback and use of NMOS transistors, the circuit is inherently fast. This adder has a balanced structure with respect to generation of SUM and CARRY signals. The Design circuit is shown in Figure 5.

4. PROPOSED PTL-GDI ADDER

In this design the SUM cell is designed using Pass Transistor Logic (PTL) and the CARRY cell is designed using Gate Diffusion Technique (GDI). The design is based on XOR-XOR based full adder style. The basic SUM as well as CARRY functionality is as follows:

H=A XOR B

SUM=H XOR Cin

CARRY=H'A + HCin

Firstly the H function is been generated using two PMOS and two NMOS transistors and then using Cin and H as input the SUM function is obtained. The SUM cell is designed using PTL technique as it is shown in Figure 7. The total number of transistor used is eight to obtain the SUM cell.

The CARRY cell is designed using GDI technique as shown in Figure 8. The GDI cell is similar to inverter cell. The only difference is instead of connecting the source of the PMOS to the VDD and source of NMOS to the GND, two different inputs are provided through the sources of PMOS and NMOS. For CARRY calculation again H is used as input to the Gate and A & Cin variables are connected to the Source of PMOS and NMOS respectively.

The overall circuit design, XOR cell symbol creation and output waveform are shown in Figure 9, 10 & 11 respectively.

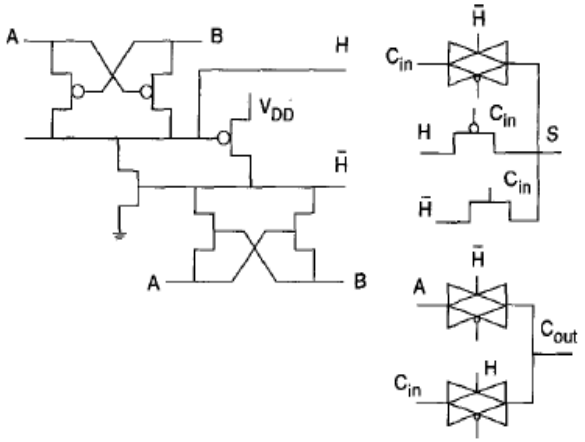

Figure 3. Radhakrishnan Adder [5]

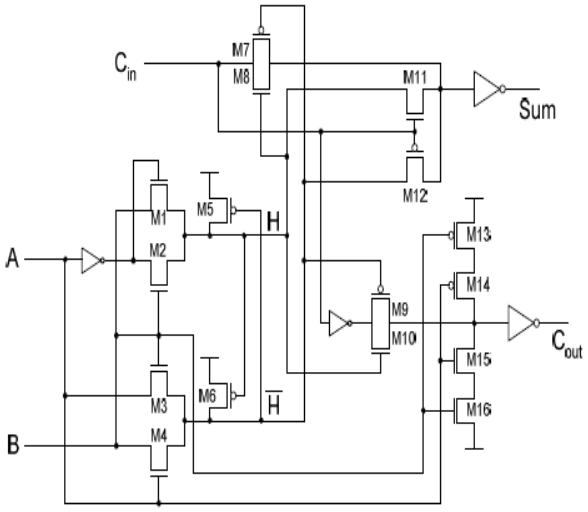

Figure 4. Goel Adder [4]

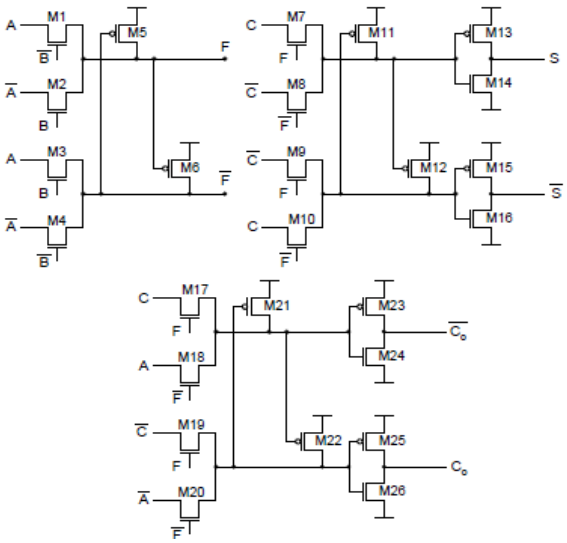

Figure 5. Agarwal Adder [2]

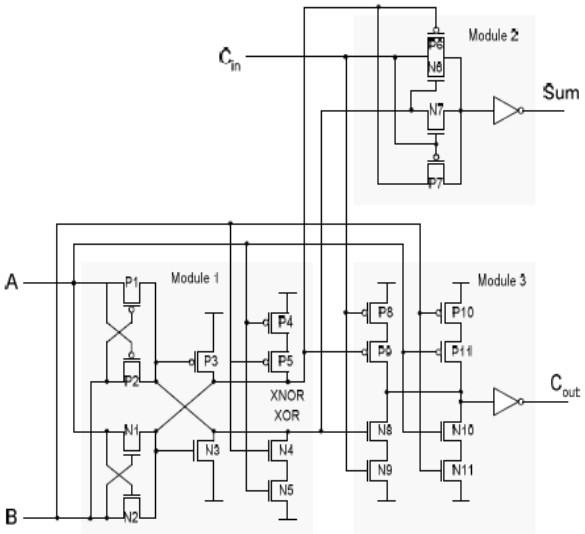

Figure 6. Chang adder [3]

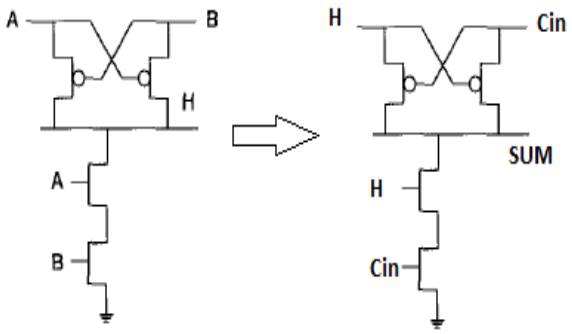

Figure 7. Proposed PTL-GDI structure for SUM cell

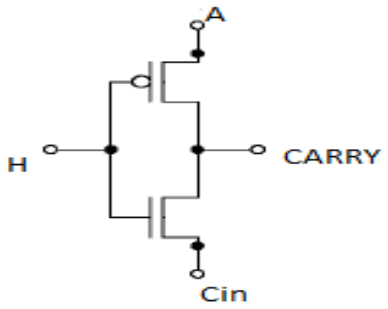

Figure 8. Proposed PTL-GDI structure for CARRY cell

5. SIMULATION ENVIRONMENT

All the adders are designed and simulated in Cadence Virtuoso 180nm technology. Their performances are measured in different supply voltages such as 3V, 1.8V and 0.8V at 100MHz. The delay was measured from 50% of the input voltage swing to 50% of the output voltage swing. Mainly three parameters are compared in this analysis; they are Delay, Power Consumption and Power Delay Product (PDP).

In order to have a fair comparison, all the simulated circuits are prototyped at optimum transistor sizing. The transistor sizes of all the simulated circuits have been included in the Figures. In the circuits, the numbers depict the width (W) of the transistors with the minimum feature size as 2µm.

6. SIMULATION RESULTS AND DISCUSSION

By optimizing the transistor sizes of the full adders considered, it is possible to reduce the delay of all adders without significantly increasing the power consumption, and transistor sizes can be set to achieve minimum PDP. All adders were designed with minimum transistor sizes initially and then simulated. To achieve minimum PDP, an iterative process of redesigning and transistor sizing after post-layout simulations was carried out.

Comparison of full adders designed to achieve minimum PDP is discussed below. In particular, three subsections refer to delay, power, and PDP respectively. In each subsection, effect of varying supply voltage is considered.

6.1 Number of Transistor Used

As it is a basic concept that if the number of transistor decreases the delay as well as power consumption decreases. So our main motive was to reduce the number of transistor in our proposed design.

Table 2
Number of Transistor Used by Different Adders

NUMBER OF TRANSISTORS			
Sl No	Adder	Nmos	Total
1	Radhakrishnan [5]	7	14
2	Agarwal [2]	19	32
3	Chang [3]	12	26
4	Goel [4]	11	22
5	Proposed Ptl-Gdi	5	10

6.2 Delay Comparison

As delay is the major issue to determine the characteristics of the design, our one main goal was to reduce the delay. The values of delay obtained for different Vdd values of 0.8V, 1.8V and 3V. To make the comparison easier, Table III shows the delay values at 3V, 1.8V & 0.8V.

Table 3
Delay comparison of different adders

DELAY(Pico second)				
SL NO	**ADDER**	**3V**	**1.8V**	**0.8V**
1	RADHAKRISHNAN [5]	19.03	25.02	103.1
2	AGARWAL [2]	59.13	79.74	448.3
3	CHANG [3]	28.99	46.99	974.5
4	GOEL [4]	55.68	92.4	746.6
5	PROPOSED PTL-GDI	17.13	23.29	93.69

As we can see from table II and table III that when the number of transistors decreases the delay also decreases. The delay is found to be very high in the case of Agarwal as well as Goel Adder. Worst performer is Agarwal Adder at 3V Vdd. But when the supply voltage decreases to 1.8V & 0.8V the worst performer is Goel Adder. Moreover in the case of Radhakrishnan Adder, Goel Adder & Chang Adder distorted outputs are generated at 0.8V Vdd (i.e. when the supply voltage decreases beyond

some threshold value these adders are found to produce unexpected output).

Now considering the proposed design i.e. Proposed PTL-GDI Design, the number of transistors used here is comparatively very less. On the other hand the delay is also very low at different supply voltages. Moreover the proposed design produces correct logic characteristics even when the supply voltage is reduced to 0.8V.

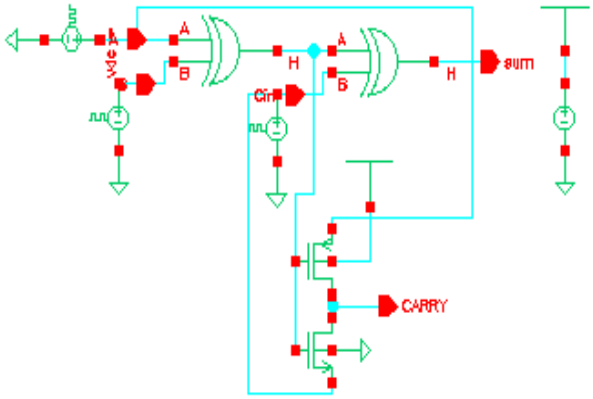

Figure 9. Proposed PTL-GDI cell circuit design

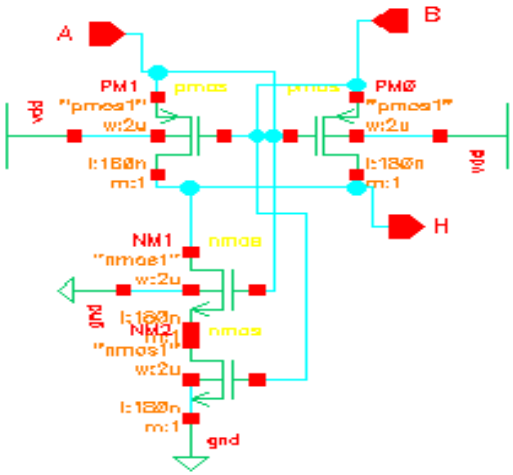

Figure 10. Proposed PTL-GDI XOR cell creation for SUM cell

6.3 Power Comparison

The average power dissipation is evaluated under different supply voltages. Table 4 tabulates the values at 3V, 1.8V & 0.8V. Among the conventional existing full adders, clearly CPL has the highest power dissipation. The CPL adder dissipates the most power because of its dual-rail structure and high number of internal nodes in its design. Therefore, the CPL topology should not be used if the primary target is low power dissipation.

In the comparison table as we can see, Goel Adder consumes a huge amount of power. Even though the numbers of transistor used for Agarwal Adder is maximum, its power consumption is found to be very less with respect to Goel Adder. The proposed PTL-GDI design consumes lesser power in comparison with Radhakrishnan Adder even though the numbers of transistors used is only four more in Radhakrishnan Adder.

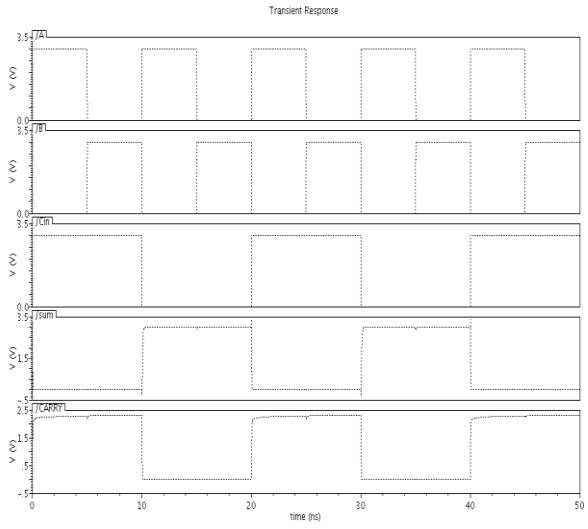

Figure 11. Proposed PTL-GDI cell output waveform. (The first three plots are for inputs i.e. A, B & Cin respectively and last two graphs are SUM & CARRY respectively).

Table 4
Power comparison of different adders

POWER CONSUMPTION(micro watt)				
SL NO	**ADDER**	**3V**	**1.8V**	**0.8V**
1	RADHAKRISHNAN [5]	12.28	4.044	312.4 pw
2	AGARWAL [2]	186.3	70.7	14.62
3	CHANG [3]	100.8	26.67	43.09 nw
4	GOEL [4]	876.5	228.7	12.13
5	PROPOSED PTL-GDI	2.779	1.097	225.3 pw

Table 5
PDP comparison of different adders

POWER DELAY PRODUCT(PDP)				
SL NO	**ADDER**	**3V**	**1.8V**	**0.8V**
1	RADHAKRISHNAN [5]	0.233 fj	0.101 fj	32.2 zj
2	AGARWAL [2]	11.016 fj	5.613 fj	6.554 fj
3	CHANG [3]	2.922 fj	1.253 fj	0.042 fj
4	GOEL [4]	48.803 fj	21.13 fj	9.056 fj
5	PROPOSED PTL-GDI	0.048 fj	0.026 fj	21.11 zj

The PDP is a quantitative measure of the efficiency of the tradeoff between power dissipation and speed, and is particularly important when low-power operation is needed. The values of PDP are evaluated under different supply voltages are tabulated in Table 5.

The PDP is measured in Femto joule (fj) and Zepto Joule (zj). The Goel Adder has the maximum PDP even though the numbers of transistor used in Goel Adder is lesser than Agarwal Adder. Though the Chang Adder is found to best in the literature (with respect to PDP), Proposed PTL-GDI design is having very less PDP in different supply voltages.

7. CONCLUSION

Hybrid design style gives more freedom to the designer to select different modules in a circuit depending upon the application. Using the adder categorization and hybrid design style, many full adders can be conceived. As an example, a novel full adder designed using PTL-GDI design style is presented in this paper that targets low PDP. The proposed hybrid full adder has better performance than most of the standard full-adder cells owing to the novels design modules proposed in this paper. It performs well with supply voltage scaling. We recommend the use of PTL-GDI design style for the design of high-performance circuits.

ACKNOWLEDGEMENT

The Authors acknowledge the support of the School of Electronics Engineering (SEE) of Lovely Professional University (LPU), phagwara.

REFERENCES

[1] Monico Linares Aranda, Ramon Báez, Oscar Gonzalez Diaz, "Hybrid Adders for High-Speed Arithmetic Circuits A Comparison". *7th International Conference on Electrical Engineering, Computing Science and Automatic Control*, Sep 2010.

[2] Sundeepkumar Agarwal, Pavankumar V K, Yokesh R., "Energy –Efficient, High Performance Circuits for Arithmetic Units". *21st International Conference on VLSI Design*, pp. 371-376, 2008.

[3] C.-H. Chang, J. Gu, and M. Zhang, "A review of 0.18nm full adder performances for tree structured arithmetic circuits," *IEEE Trans. Very Large Scale Integration Systems.*, vol. 13, no. 6, pp. 686–695, Jun. 2005

[4] Sumeer Goel, Ashok Kumar and Magdy A. Bayoumi, "Design of robust, energy efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," *IEEE Trans. Very Large Scale Integration. Systems*, vol. 14, no.12, pp.1309–1321, Dec. 2006.

[5] RADHAKRISHNAN, D., "Low-voltage low-power CMOS full adder," *IEEE Proc. Circuits Devices Syst.*, vol. 148, no. 1, pp. 19–24, Feb. 2001.

[6] RADHAKRISHNAN, D., WHITAKER, S.R., and MAKI, G.K. "Formal design procedures for pass transistor switching circuits", *IEEE J. Solid-State Circuits*, 1985, SC-20, pp. 53 1-536

[7] RADHAKRISHNAN, D. "Design of CMOS circuits" *IEEE Proc. Circuits Devices Syst.,* 1991, 138, (I),p p. 83-90

[8] PEDRON, C., and STAUFFER, A. "Analysis and synthesis of combinational Circuits", *IEEE Trans. Commit.-Aided Des. Integr. Circuits Syst*. 1988, 7, (7), pp. 775-786

[9] Morgenshteid, A., Fish, A., and Wagner, I., A. "Gate-Diffusion Input (GDI) - a novel power efficient method for digital circuits: a design methodology" *IEEE 2001*

[10] Nishad, A., K., Chandel, C., "Analysis of Low Power High Performance XOR Gate using GDI Technique", *IEEE Computer Society- International Conference on Computational Intelligence and Communication Systems,* 2011