A NOVEL LOW POWER AND HIGH SPEED MULTIPLY- ACCUMULATE (MAC) UNIT DESIGN FOR FIXED AND FLOATING-POINT ARITHMETIC NUMBERS

A Dissertation

Submitted

By

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To

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In partial fulfillment of the Requirement for the

Award of Degree of

MASTER OF TECHNOLOGY

IN

VLSI DESIGN

Under the guidance of

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(April 2015)

CERTIFICATE

This is to certify that N Jithendra Babu has completed objective formulation of his Dissertation report titled, "**A NOVEL LOW POWER AND HIGH SPEED MULTIPLIER-ACCUMULATOR (MAC) UNIT DESIGN FOR FIXED AND FLOATING-POINT ARITHMETIC NUMBERS**" under my guidance and supervision. To the best of my knowledge, the present work is the result of his original study and research. No part of the project has ever been submitted for any other degree at any University.

The project is fine for the submission and fulfillment of the conditions for the award of degree Master of Technology in VLSI Design.

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Date:

Objective of the Dissertation-II is satisfactory / unsatisfactory

Examiner I **Examiner II**

DECLARATION

I hereby declare that the Dissertation report entitled "**A NOVEL LOW POWER AND HIGH SPEED MULTIPLIER-ACCUMULATOR (MAC) UNIT DESIGN FOR FIXED AND FLOATING-POINT ARITHMETIC NUMBERS**", is an authentic record of my own work carried out as the requirements for the award of degree of Master of Technology in Vlsi Design at Lovely Professional University, Jalandhar under the guidance of Mr. Raj Kumar Sarma, Assistant Professor, Department of Electronics and Communication Engineering.

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It is certified that the above statement is correct to the best of my knowledge and belief.

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ACKNOWLEDGEMENT

This is a humble effort to express my sincere gratitude towards my mentor who has guided and helped me to explore the field of Low Power VLSI, which is the base of my dissertation undertaking.

Problem formulation is a major milestone for a student while working on Dissertation. As such this subject was a challenge for me and was an opportunity to prove my caliber. Being a beginner, I faced many problems, which would have frustrated me. I am highly grateful and obliged to my mentor.

It would not have been possible to see through the undertaken field of study without the guidance of **Mr. Rajkumar Sarma.** It was purely on the basis of his experience and knowledge that I am able to clear the theoretical and technical hurdles during the analyses and exploration of the selected field of study.

I would like to thank the **Mrs. Cherry Bhargava, HOD (Dept.of ECE), Mr.Bhupinder Varma, DOD (School of Electronics Engineering) and Project Approval Committee members** for their valuable comments and discussions and I would also like to thank **Lovely Professional University** for facilitating me to undertake this study.

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ABSTRACT

In this study, a Multiply-Accumulate (MAC) unit design has been proposed for fixed and floating point numbers. For the signal processing systems, the basic block for the processing of data is the MAC unit. The digital processing systems are mainly used for high speed signal processing where there is a need for multiplications, additions and some basic arithmetic operations. To perform such basic arithmetic operations the MAC unit is the basic block in the digital signal processing systems.

The MAC unit is designed using the various individual blocks and are synchronized for the overall design of MAC unit. At first, the MAC unit for the fixed point unsigned number architecture has been designed and the same design is used for implementing the fixed-point signed and floating-point number architecture. The individual blocks of the MAC unit are multiplier for multiplication process, register unit for storing of data, binary to BCD converter to convert the output of multiplier to be in the BCD format, BCD block to maintain the overall output of the MAC unit to be in the BCD format and finally an adder which is used to add the present input values with the previously accumulated value stored in the register unit.

The overall MAC units for the fixed-point unsigned, signed and floating-point numbers are designed in the cadence virtuoso 90nm technology. First the individual blocks are designed and the parameters like power, delay and power-delay product are analyzed using the cadence spectre tool and finally the overall MAC units for the unsigned, signed and floating point architectures are designed in cadence virtuoso 90nm technology and the parameters are analyzed by using the cadence spectre tool.

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LIST OF ABBREVATIONS

1. **MAC** – Multiplier- accumulator unit
2. **CMOS** – Complementary metal oxide semiconductor
3. **CLA** -- Carry look adder
4. **CSA** -- Carry save adder
5. **RCA** -- Ripple carry adder
6. **DSP** -- Digital signal processing
7. **DDFF** -- Dual Dynamic Hybrid Flip Flop
8. **PTL** -- Pass Transistor Logic
9. **GDI** -- Gate Diffusion Input

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CHAPTER 1

INTRODUCTION

The technology at the present generation is rapidly growing due to the development in the increase of portable electronics where there is a need for the limitation of power. Due to this, the design engineers are focusing mainly on the power consumption of an integrated circuit. Thus, there is a need for optimizing the power of an IC through various methods depending on the nature of the designer.

Now-a-days, the designers are involved in the design of high speed systems where there is a need for optimization. Digital signal processors are one of the high performing systems used in the processing elements. So, the work motivates to work on the performances of the high speed performing systems known as multiply-accumulate (MAC) unit which is a basic building block in many of the signal processing systems. In any of the digital processing systems the main function involves the multiplication and additions which are the main concerns that has an effect on the overall processing unit. Due to this the work focuses on the MAC unit where multiplication and addition are the major functions involving in it.

The function of MAC unit is to multiply the N-bit input values and then performs the addition with the previously accumulated value that is stored in the accumulator register. So, the proposed work investigates on the various building blocks that are the basic blocks in the design of the overall MAC unit. Thus, there is a need for optimizing the individual blocks that are to be efficient while designing MAC unit. The individual blocks are optimized to be low power and high speed and synchronized to implement the MAC unit. Since the proposed MAC unit based on the existing work from the literature review is meant to design for the unsigned number architecture which is capable of performing the operation of MAC unit for non-negative numbers. So, the work further moves to the implementation of MAC unit for fixed-point signed numbers. In the fixed point signed number architecture the proposed unit determines whether the value accumulated is positive or negative. Since, the fixed point number architecture deals with the small arithmetic operations there is a possibility of occurrence larger arithmetic operations in the digital processing systems. A new architecture has proposed known as floating-point MAC unit for floating number addition. In the floating point number system the real parts are indicated as mantissa and exponent of the system.

1.1. MAC UNIT:

The term MAC is represented as the multiply-accumulate (MAC) unit which is a high speed signal processing system in digital systems. The basic elements in the MAC unit are the multiplier, adder and the accumulator register.

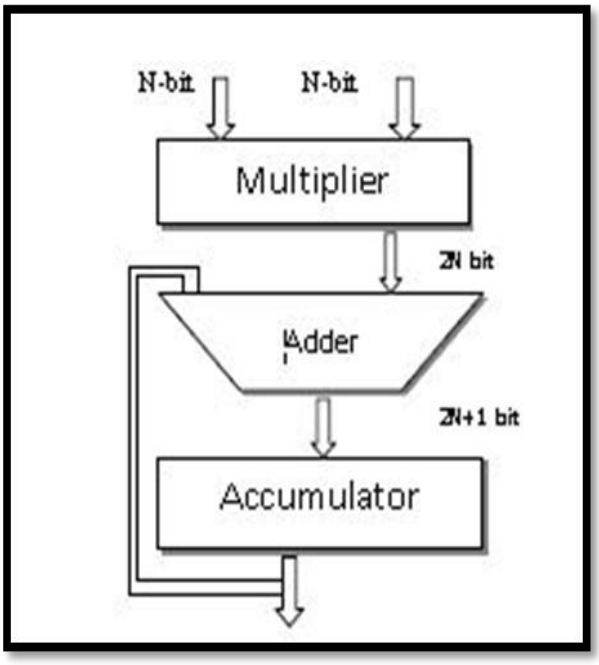


Fig.1. Basic MAC Unit

The function of MAC unit is to multiply the N-bit values that are fetched from the memory or some other location and adds the current output from the multiplier block with the previously accumulated values that are stored in the register. The mathematical representation of MAC unit is

$$F= \sum_{i=0}^{n-1} a_i b_i$$

1.1.1. MAC OPERATION:

The MAC is a basic block which performs high speed operations in the digital processing circuits where there is a need for the basic arithmetic operations. The conventional MAC unit is a part of DSP processor which performs the basic arithmetic operations such as multiplications and additions. In the design of MAC unit the designers need to have a look over the parameters like power and speed to make the proposed circuit to be efficient. The MAC unit consists of the basic blocks like multiplier, adder and register for storing the data. While designing the basic blocks we should think of optimizing the basic blocks to be efficient in terms of the power and speed of the system. The operation of MAC unit for the conventional unit is as follows:

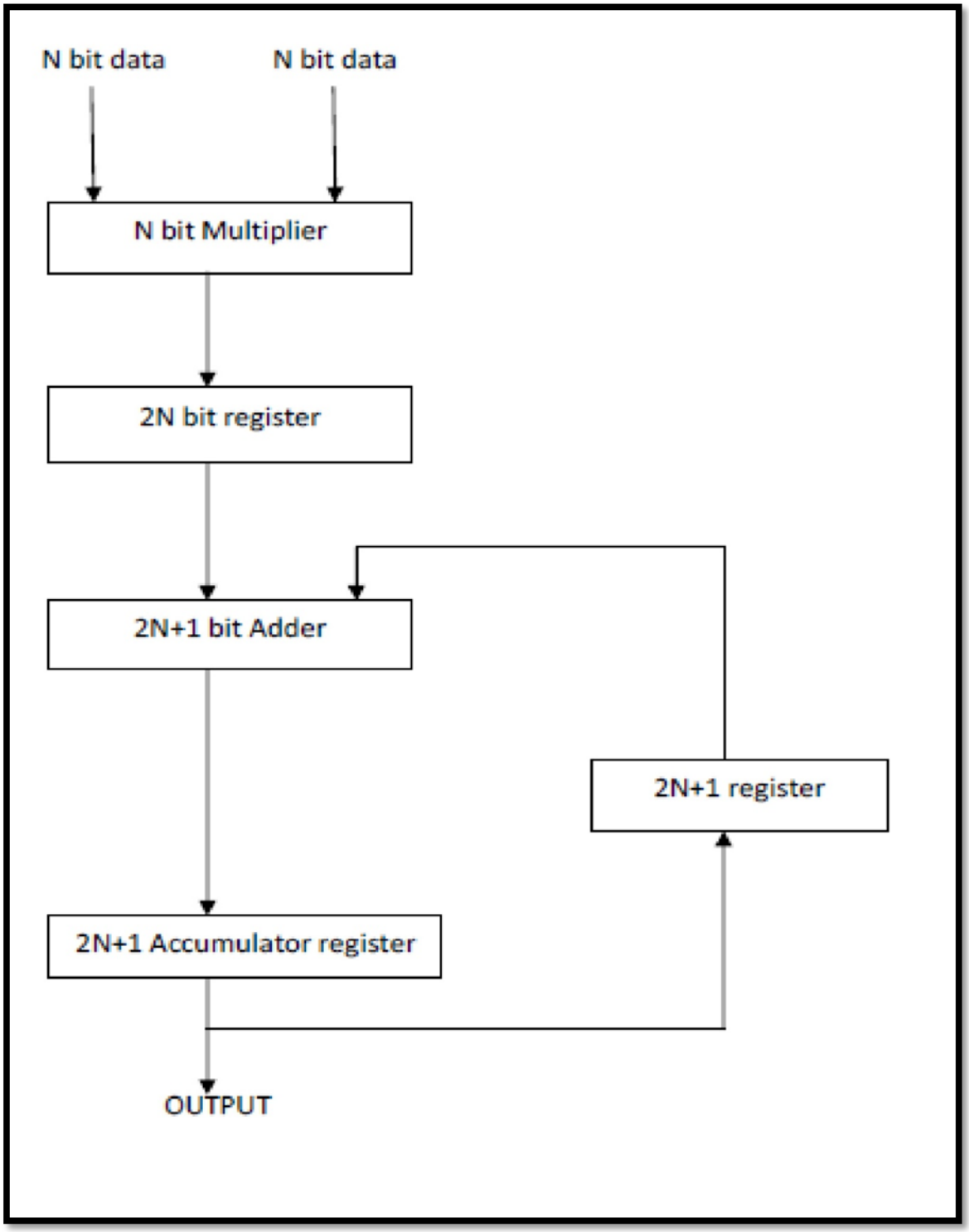


Fig.2. Existing MAC Unit

At the initial stage an N-bit inputs from the memory location are fetched and given as input to the multiplier. The multiplier multiplies the N-bit input values and passes the output to the register block as 2N bit outputs. The register block stores the multiplier output and passes the values to the next level after the certain clock generation. The adder circuit adds the multiplier output with the previously accumulated values that are stored

in the register which is termed as a feedback register to give the stored accumulated values. After the addition operation the accumulated values are passed to the register which is termed as accumulator register because it stores the accumulated values and passes to the feedback register for the next step operations as explained above.

1.1.2. MULTIPLIER:

The term multiplier indicates basically the multiplication of two set of values. In this study there is a need of multiplier circuit which is a basic and essential block for the processing of the MAC unit. Multipliers are the key role elements in the signal processing systems which performs the high speed operations.

Since the MAC unit is a high speed processor there is a need of designing the multiplier circuit to be of high speed. While designing a high speed circuit there is an impact on the power dissipation. Such that the designer needs to look over the power and speed of the combinational circuit for means of high processing systems. An efficient low power and high speed multiplier can be designed using the various algorithms. Some commonly used multiplier architectures for the design of multiplier is array multiplier, booth multiplier based on the booth's algorithm, wallace tree multiplier based on the wallace tree algorithm, radix-2 multiplier, Vedic multiplier etc.,

1.1.3. ACCUMULATOR REGISTER:

The word accumulator refers to the storing of accumulated data. It is the basic building block in the MAC unit for storing the accumulated values. The function of accumulator register is to store the values that have been added by the adder circuit with the previously accumulated values that has been stored in the register for next consecutive levels.

In this research study later on the following sections are discussed. The first section is about the introduction and evaluation of the MAC unit. The second section comprises of the scope of the study and the third is the objective of the study. The fourth section describes about the literature of review and the fifth section discusses about the design methodology. The sixth section discusses the present work and later results and discussions and finally conclusion and future scope.

1.2. CADENCE VIRTUOSO

Cadence is a hardware stimulator that permits the client to plan completely custom circuits and recreate them. Projects very much alike to cadence are broadly utilized as a

part of industry and exploration. Building crucial Cadence abilities will help you in your scholarly profession as an understudy, and your vocation as a specialist.

The cadence platform is a type of semi custom design software for the VLSI chip designing. The designer can design the circuits in the full custom design or semi custom design. The cadence simulators are the:

- Cadence NC launch
- Cadence Virtuoso
- RTL Complier (Encounter)
- Assura

The proposed work is designed in the cadence virtuoso environment. Under the cadence virtuoso environment there has the availability of different technological libraries:

- Gpdk 180nm
- Gpdk 90nm
- Gpdk 45nm

The research study is designed in the cadence virtuoso at 90nm technology library. The transistors in the library files are at level 11 where as the transistors in other simulators like TSMC, mentor graphics etc., and are at lower levels. The designer can design the circuits using the cadence virtuoso platform and can analyze the circuits using the cadence spectre tool.

The cadence spectre tool plays an important role in the analyzing of the circuit where the parameters of the circuit can be analyzed. The parameters like power, delay, SNR, pnoise, sample frequency and many more can be analyzed for a circuit using the cadence spectre tool. Using the cadence spectre tool the designer can perform the different analysis such as transistent, AC, DC and so on. The node voltages, transistor regions, transistor parameters, annotations, Dc voltages and many more can be synchronized using the cadence spectre tool.

CHAPTER 2

SCOPE OF THE STUDY

At the present generations the existence of low power designs are vast in designs. While designing a low power designs there should be consideration on the speed of IC. There are many types of high performing systems out of these, digital signal processors is one of the high performing systems where there is a limitation in the power. So, the research motivations tend to study on the high performing systems where MAC is a basic unit in such type of processing systems.

The scope of the research tends to design a low power and high speed MAC unit for the fixed and floating point numbers. From the review of literature, it indicates that the existing MAC units are implemented in digital designs through the digital design simulators.

The research study focus on the implementation of the proposed work by the analog method through EDA tools where the optimization of circuit can be done for the proposed system manually and can determine some parameters like power, delay and PDP.

CHAPTER 3
OBJECTIVE OF THE STUDY

In this research study the MAC unit for the fixed and floating point numbers are designed using the various individual blocks which are the basic functional blocks for the efficient performance of the overall MAC unit for the unsigned, signed and floating architectures.

Objectives:

- To individually determine and examine the basic blocks which are meant for designing the MAC unit.
- To implemented the individual blocks and finally the overall MAC unit for the unsigned, signed and floating architectures at cadence 90 nm technology library.
- To implement and analyze the novel designs of binary to BCD converter and BCD blocks those are the major functioning elements in this research study.
- To analyze the basic blocks of the design in terms of power, delay and power-delay product.
- To synchronize the individual blocks for the overall design of MAC unit for fixed and floating point architectures and optimizing the design to be efficient in terms of power, delay and power-delay product.

CHAPTER 4
REVIEW OF LITERATURE

This section contains the audit of writing about MAC unit. The concentrations on numerous diaries and gathering papers, articles identified with reference to the proposed work are discussed. This section presents vital thought and proposed hypothesis of the papers mulled over as indicated by the National and International gatherings.

ABOUT MAC:

(Avisek sen, *et al., 2013*[3]) This paper proposes the design of low power mac using the block enabling technique to optimize power dissipation. The mac is designed by 130 nm technology and it is operated at 200 MHz with 1.5v power supply. The total power consumption is reduced by the block enabling technique.

(Jagadesh.P *et al., 2013*[9]) An implementation of high performing 64 bit MAC is designed in their study. Multiplier is implemented by the Wallace tree multiplier and adder by carry save adder. The implementation is coded by verilog-HDL and synthesis by cadence RTL compiler using 0.18um technology. The MAC operates at 217 MHz and power is of 177.732 mw.

(Ashish B.kharate, *et al., 2013*[2]) Here a new MAC architecture is designed using the pipelining and clock gating techniques to reduce the power of MAC for use in digital fir filters. Each block is analyzed for its performance. Mac unit is designed and power is evaluated so that n-nit mac unit will be designed and the total power consumption will be found out. The mac designed in their work can use for filter realizations for high speed applications.

(Teffi Francis, *et al., 2013*[18]) This paper aims an optimization of power and delay of Braun multiplier by the bypassing technique and delay is reduced by the ripple carry adder in the last stage by full adders using the optimized adders. Double pass transistor logic (DPL), transmission gate (TG) and different logic adders are designed at 0.13um technology.

(Deepak s, *et al., 2012*[5]) A new multiplier design is proposed which reduces the partial products by 25% and this is used with different adders to implement multiplier and

accumulate unit. In this after comparing the parameters it is found that the proposed multiplier has the lowest propagation delay when compared with array and booth multipliers.

(Swaraj Raman M *et al., 2012*[15]) Their proposed work is on the reversible multiply and accumulate unit in a single clock cycle. They designed a Vedic mac using reversible logic and compared with other implementations in terms of number of garbage outputs, quantum cost and Depth.

(Shanthala s*, et al., 2009*[4]) The main aim of their study is to design a mac unit at 180 nm technology. For this various multipliers and full adders have been implemented. Static and dynamic adders are implemented. Spice code had written to test the functionality of mac and schematic design is done by the schematic composer through virtuoso. In terms of power, area the dissipation is of 50.26mw and 3*1.05 mm2. The latency is 6 clock cycles.

(A.Abdelgawad, *et al., 2007*[1]) They proposed an efficient area and high speed mac in the paper, first they examined about critical delays and also the hardware complexities of mac architectures. The architecture is designed using the binary trees used to construct a modified 4:2 compressor circuits. The speed of the critical path can be optimized by avoiding the modified compressor. The output stimulation results indicates that their system for 8-bit,16-bit,and 32-bit mac architecture optimizes area of 6.25%, 3.2% and 2.5% and speed by 14%, 16% and 19% respectively.

(Sriram R. Vangal*, et al., 2006* [16]) Their proposed work is on the design of a pipelined single precision FPMAC which represents a bit-level pipelined multiplier and accumulator unit with a single cycle accumulation loop throughout the system. The proposed techniques work at 3 GHz operation and achieved a reduction of 30% power reduction.

FOR ADDERS:

(Uma *et al., 2012*[19]) This paper presents the choice of selecting the adder topologies between the trades offs of delay, power consumption and area. The topologies in their work are ripple carry adder(RCA), carry look ahead adder(CLA), carry skip adder, carry save adder(CSA) and many more. The area, power and delay are analyzed at 0.12um six

metal layer cmos technology file using micro wind tool. The comparisons are done using the power, area and delay.

(Duvvuri Divya *et al., 2012*[6]) Their proposed work is on the design of reversible full adder circuits. These adder circuits are then implemented to design a 4-bit ripple carry adder and subtractor using the reversible logic and the power dissipation and delay has been calculated using the proposed design using the cadence RTL compiler.

(Shivshankar Mishra *et al., 2011*[17]) Their study is on the design of high performances devices such as 1-bit full adders using cmos. They have proposed two architectures of one bit full adders for an efficient performance in the design of digital circuits. They have compared the proposed circuits with the conventional adders and made the comparison of the power, delay and PDP.

(Madhusmita Mahapatro *et al., 2010*[13]) Their aim is of finding a counter part of all the irreversible basic logic gates and developing full custom layouts of the proposed design gates at 0.25um technology and by using those gates they have designed binary parallel adder and multiplier circuit of 4 bit using the reversible logic.

(Maii T. Emam *et al., 2010*[12]) In this they proposed Dual novel designs of adder and subtractor through reversible logic. The first design is based on the implementation of two's complement of Adder and Subtractor and second is novel reversible gate for the design of reversible adder/subtractor unit and it is applied to design a ripple adder or subtractor.

(Farshad Moradi *et al., 2009*[7]) In this they have proposed many full adder topologies for low power Dissipation. Their idea of designs is based upon Sense Energy Recovery Full adder (SERF) and the GDI (Gate Diffusion Input). These designs are used to reduce the usage of power. They have proposed different full adders and compared each other. The power consumption is reduced to 62% in SERF Design and 86% in GDI full adder design.

(Vahid Foroutan, *et al., 2008*[20]) Here a low power full adder is proposed based on the majority function. Here the XOR gates are eliminated where it is time consuming. The adder circuit is implemented in two level dynamic using zipper techniques. This proposed

design produces a considerable reduction of power dissipation in the overall circuit leads to the best power delay product.

FOR REGISTERS:

(Helga Evangelene *et al., 2014*[8]) In this paper a new novel hybrid low power Flip Flop is proposed using the Sleepy Stack inverter and this is compared with the Conventional Dual Dynamic Flip Flop (DDFF) in the cadence 90nm tool. This proposed flip Flop is then applied for designing the T, SR and JK Flip Flops and their performance is compared with conventional Flip Flops of DDFF.

(Kalarikkal Absel *et al., 2013*[11]) They proposed a new Hybrid Flip Flop and embedded Flip flop such that to eliminate the capacitance present in precharge Node. Their aim is to reduce the pipeline overhead. Their work is implemented in the 90nm UMC process and compared the designs with the other implementations in terms of area, speed and power dissipation.

(Jun Cheol Park *et al., 2006*[10]) They proposed a low power CMOS design known as sleepy stack. Their design can retain in a logic state during the sleep mode to achieve the low leakage power. The design is applied to generic circuits and the power leakage is reduced thus providing the designers a new choice of handling the leakage power problem.

CHAPTER 5
DESIGN METHADOLOGY

The objective of the study is to design a novel multiply-accumulate (MAC) unit for the representation of fixed and floating numbers. The architecture of the MAC unit for the fixed point numbers deals with the basic arithmetic operations that are for smaller operations. The floating point architecture deals with the larger arithmetic operations that are termed as mantissa and exponent where the mantissa bits are added and the exponent terms are directly added and are bypassed to the output level.

In the research study, three novel architectures have proposed for three different number representations. The MAC unit is a high performance device that is vastly used in the digital processing systems. So, while designing such a unit one should consider the parameters like power, delay and PDP of the basic blocks that are used in the design of the MAC unit.

The proposed designs are implemented in cadence virtuoso 90nm technology library. In this study a 4-bit MAC unit has been implemented such that it can extend upto 64-bit MAC for the future works. The design methodologies of the individual blocks are discussed below:

5.1. Wallace tree multiplier:

The research study starts with the analysis of the multiplier which is a basic block in the multiply-accumulate (MAC) unit. The MAC is a high speed device which is used in the digital processing systems where there is a need of multiplying the signals. So, the design and analysis of the multiplier should be of high speed and should dissipate less power. Generally, the high speed devices dissipate more power. To eliminate this there is a look over different architectures of the multiplier block to be efficient for the proposed design methodology and analyzed a multiplier architecture based on the Wallace tree algorithm. Since, the multiplier works on the principle Wallace tree algorithm and so it is known Wallace tree multiplier. In this work, a basic 4-bit multiplier has been designed and propagating the output of the multiplier block to the next levels.

The steps to be considered while designing a multiplier block will be:

- Product terms will be basically implemented by AND gates.
- For adding two product terms Half Adders will be used.
- For adding more than two product terms Ripple Carry Adder will be used.

- To calculate the final result Carry Look Ahead adder or Carry Select Adder will be used in order to increase the speed of operation.
- The internal of the Full adder cell has been implemented with 9T cell (PTL & GDI technique) & half adder with 6T cell using the pass transistor logic.

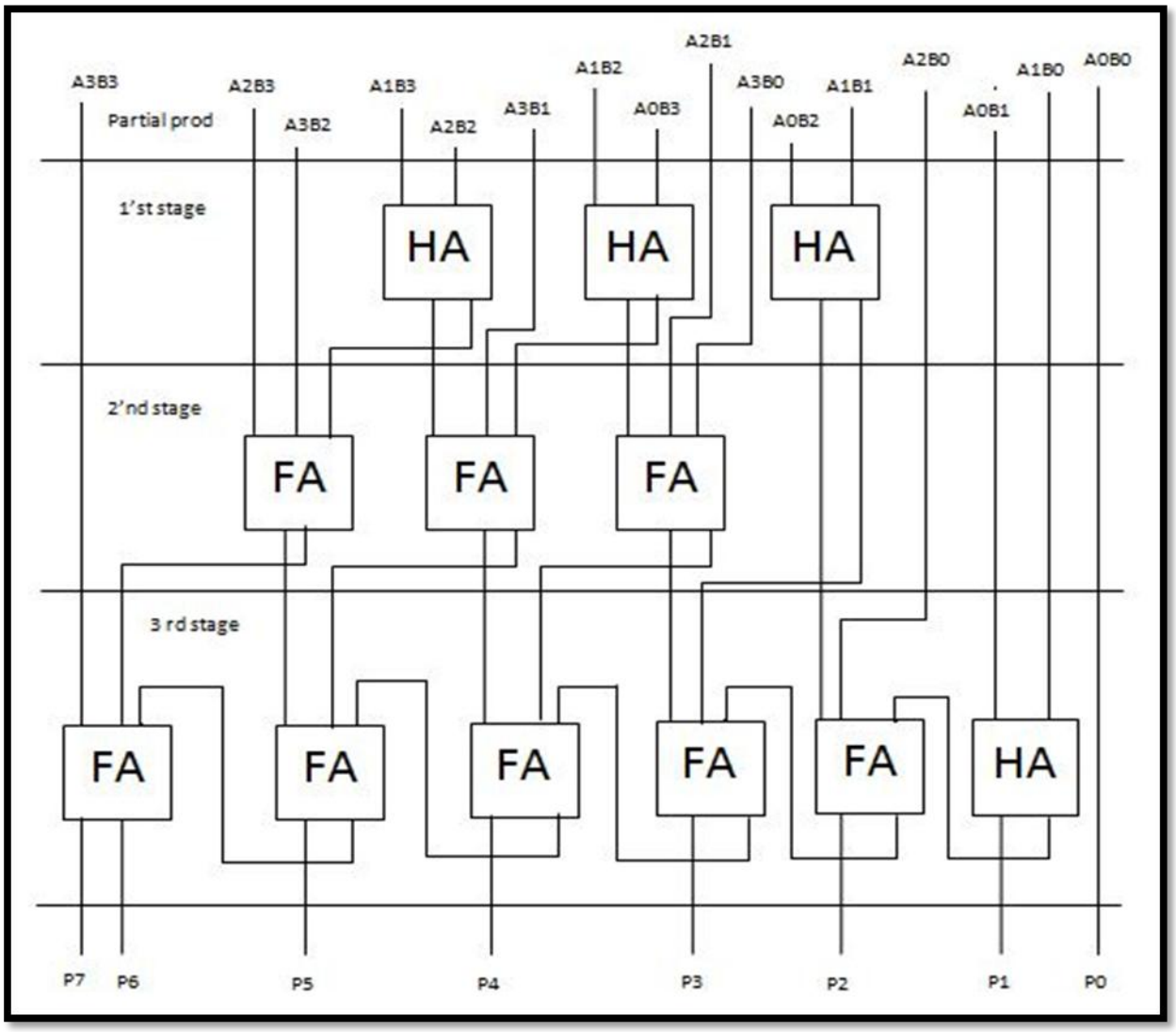


Fig.3. Wallace Tree Multiplier

- In the figure the terms 'A0B0' upto 'A3B3' represents the product terms that has been designed using a simple AND gates.
- At the first stage half adders are used to add the two product terms.
- At the second stage full adders are used to add the sum of the product terms.
- At the final stage an array of full adders in the form of ripple carry architecture are used to find the final product of the multiplier.

5.2. Adder:

The basic functional block in the design and in the individual blocks is the adder circuit. The adder circuit plays an important role in the design of the MAC unit. Since, the adder design is used in all the major individual blocks such as multiplier, binary to BCD and BCD block the design of adder circuit should be very much efficient regard of speed and power.

The adder circuit can be designed using the various architectures such as CMOS conventional architecture, adiabatic logic, quasi-domino adders, pass transistor logic, gate diffusion input logic, transmission gate logic, mux based adders, SERF adders etc,. The adder architecture is based on the combination of pass transistor logic, gate diffusion input logic and mux based design using in this design [17].

While there is a look into the architectures of the existing adders with the implemented adder there is a better efficiency regarding power and speed. Since adder circuits are used to perform the basic arithmetic operations such as the ‘add’, ‘multi’ and so on there is a need of analyzing the adder circuit to be a low power and high speed because it is used in the design of the individual blocks and the overall MAC unit. In this design to get the better signal propagation at the output levels there is a need of analyzing the adder circuit. The adder circuit is analyzed by the parametric analysis and modified the “W/L” ratios of the transistors to get the efficient signal at the output level.

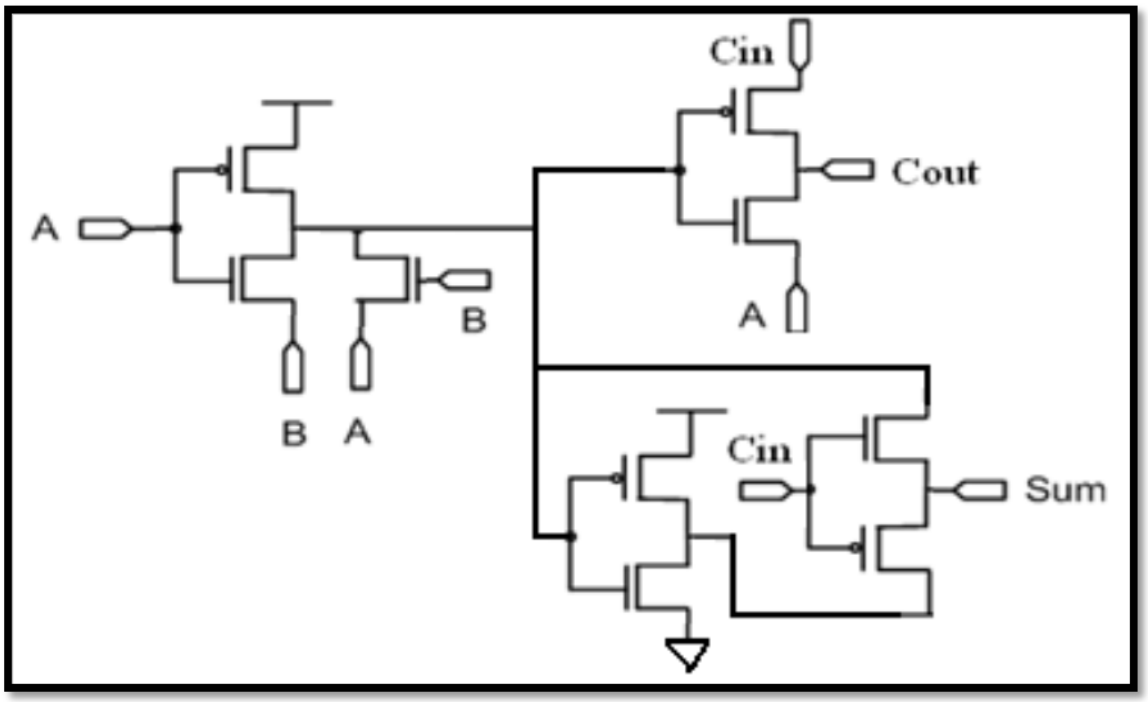


Fig.4. Proposed 9T Full adder Circuit

5.3. Binary to BCD converter:

In this study the binary to BCD plays a vital role in the analysis of the MAC unit. The need for the binary to BCD converter is due to the multiplier architecture. The multiplier block multiplies the N-bit input sets and produces the output in the binary format. Since, the proposed work deals with the BCD numbers. So, there is a need for the binary to BCD converter. The binary to BCD converter converts the multiplier output which is in the binary form to BCD format. The binary to BCD converter is designed using the basic logic gates such as AND, XNOR and 9T full adders with BCD blocks.

ALGORITHM:

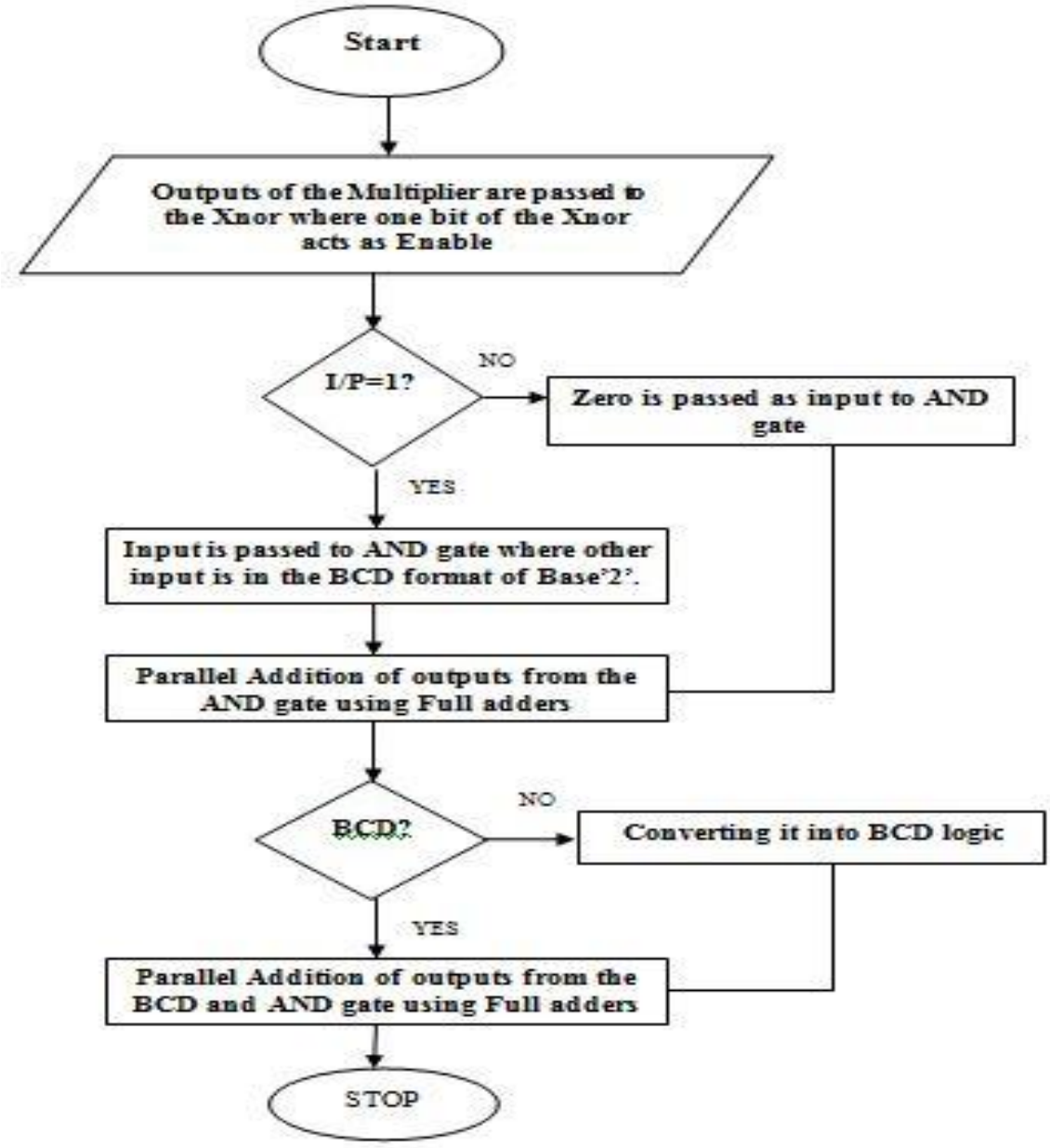


Fig.5. Flow Chart for Binary to BCD Conversion

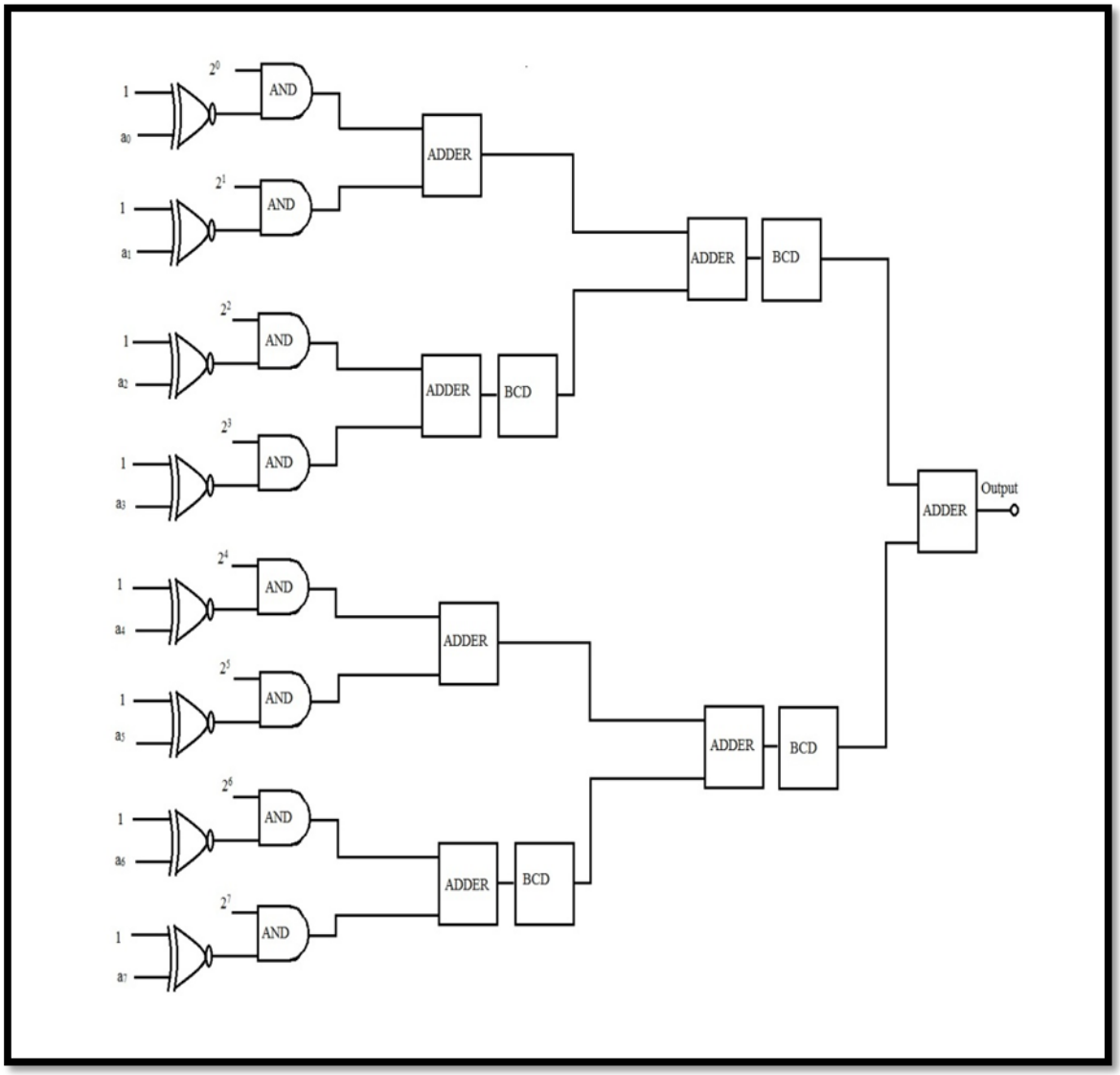


Fig.6. Binary to BCD converter

5.4. BCD Block:

In this study the design deals with the computations of the BCD logics. The proposed designs of MAC unit for unsigned, signed and floating numbers; deals with the binary coded decimal logic where larger operations can be easily computed. So there is a need for the BCD block in this design to maintain the overall proposed design to be in the BCD format. The BCD block is designed using three 12-bit 2:1 MUX, two 12-bit 4:1 MUX etc. The BCD block is used in two combinations in the proposed architecture as the first combination is used before the adder block which maintains the output of the first register block to be in BCD format and the second combination is used after the adder block which again helps in maintaining the overall output of the MAC unit to be in the Binary Coded Decimal format.

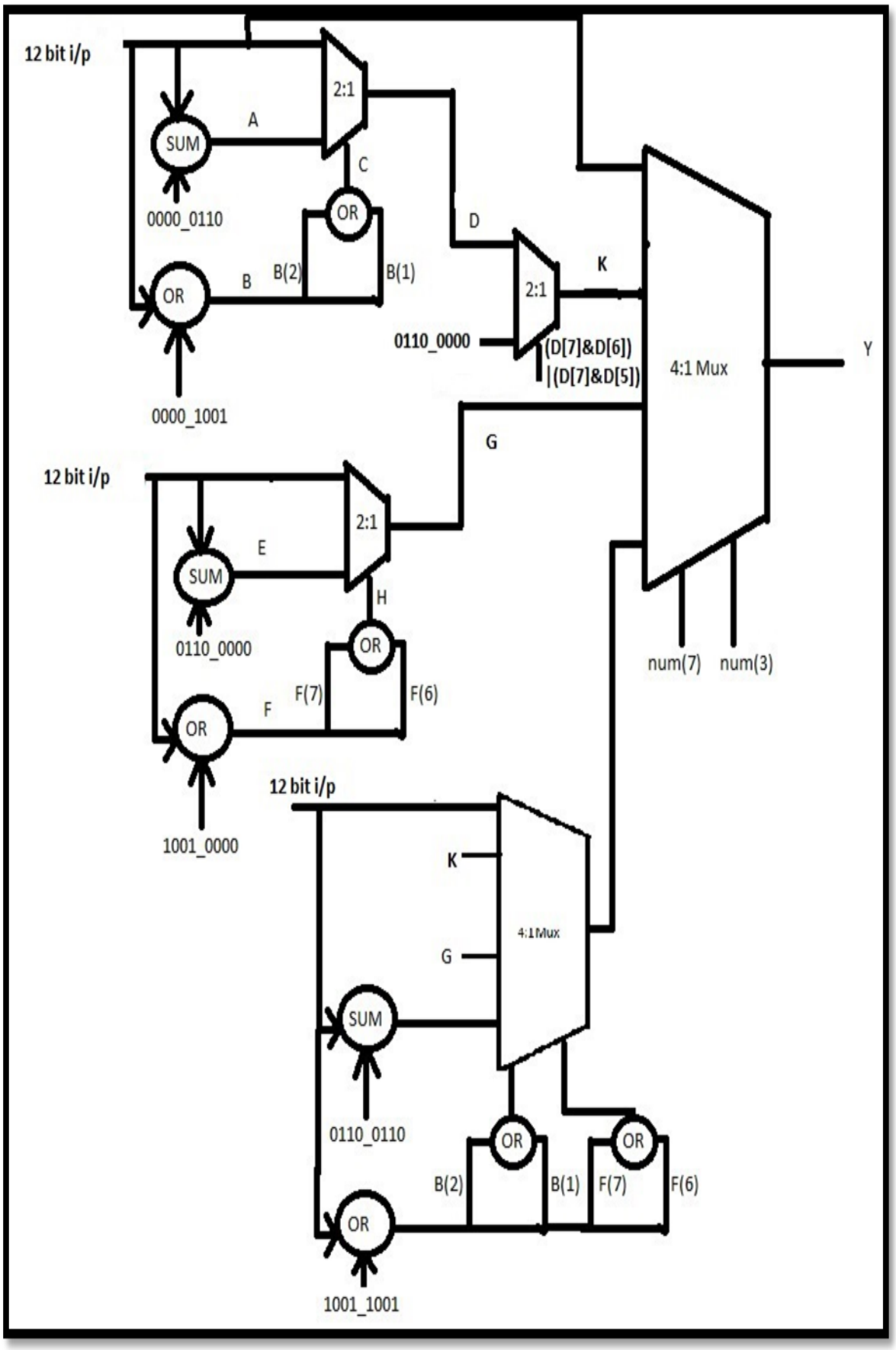


Fig.7. BCD Block

ALGORITHM:

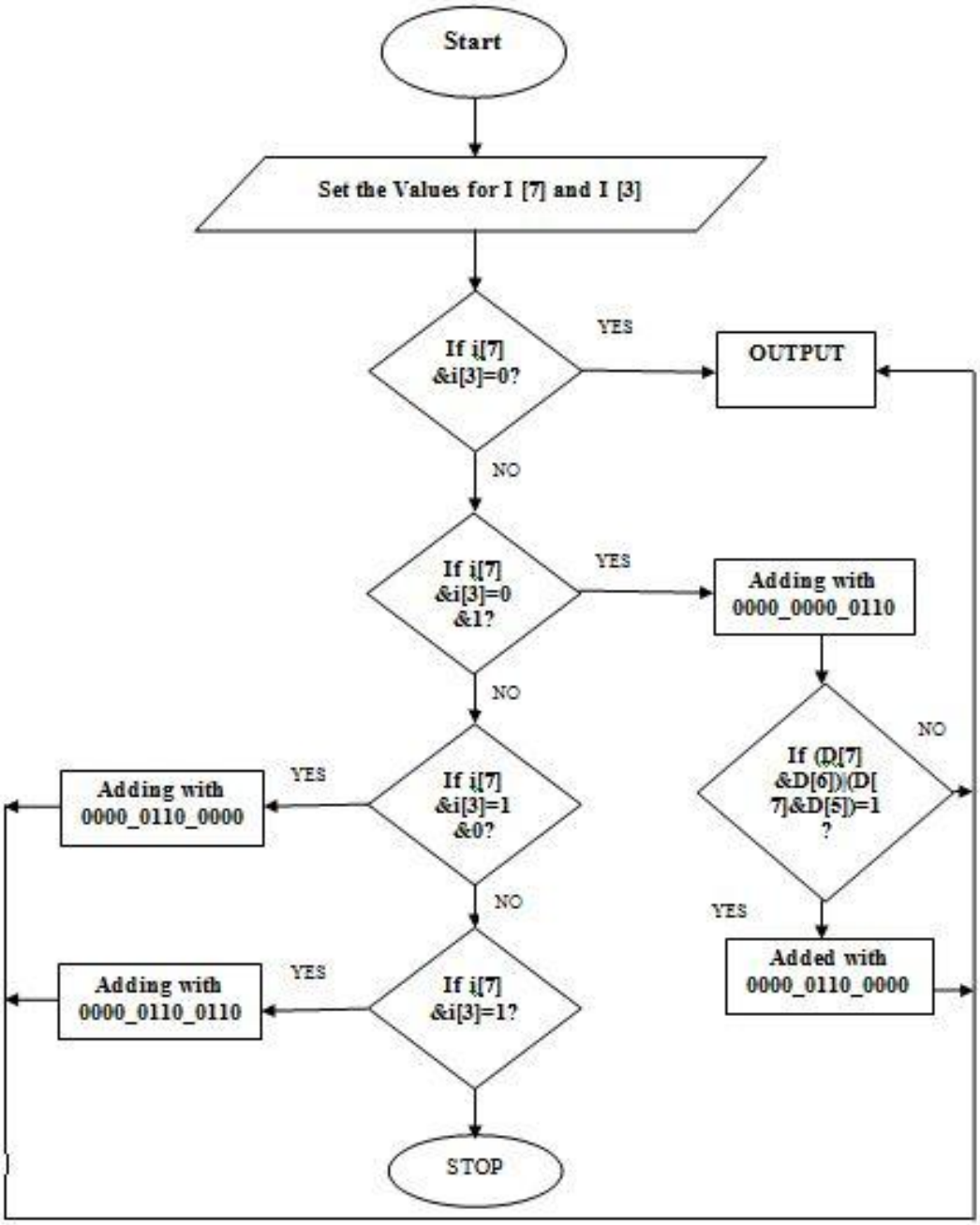


Fig.8. Flow Chart for BCD

5.5. Accumulator Register:

In this study the register unit plays an important role during the operation of the MAC unit. The word accumulator or register is termed as the storage of data that is needed to be computed. The proposed design deals with the large arithmetic operations where there exists a leakage effects during the operation of MAC unit. The proposed accumulator register is designed using the hybrid storage element known as the hybrid flip flop using the sleepy stack technique. In the proposed designs the register unit are cascaded to form

8-bit and 12-bit register units for the storage of 8 and 12-bit data in the storage element during the operation of MAC unit. The proposed register unit consists of a two major signals termed as "Rsel", "Wsel", and D-flip flop with clock gating designed using the sleepy stack technique which reduces the leakage effect during the sleep mode.

The operation of register unit for 1-bit data is as follows:

- At the initial stage the "Wsel" signal is asserted to high and the "Rsel" is asserted to low.
- During this phase depending upon the "clock" the "DATA" is written into the storage element.
- After the data is written into the storage element the "Wsel" is asserted to low and "Rsel" is asserted to be high.
- During this phase depending upon the clock signal the data is read out at the output of the register.
- The same operation is followed for the N-bit register unit.

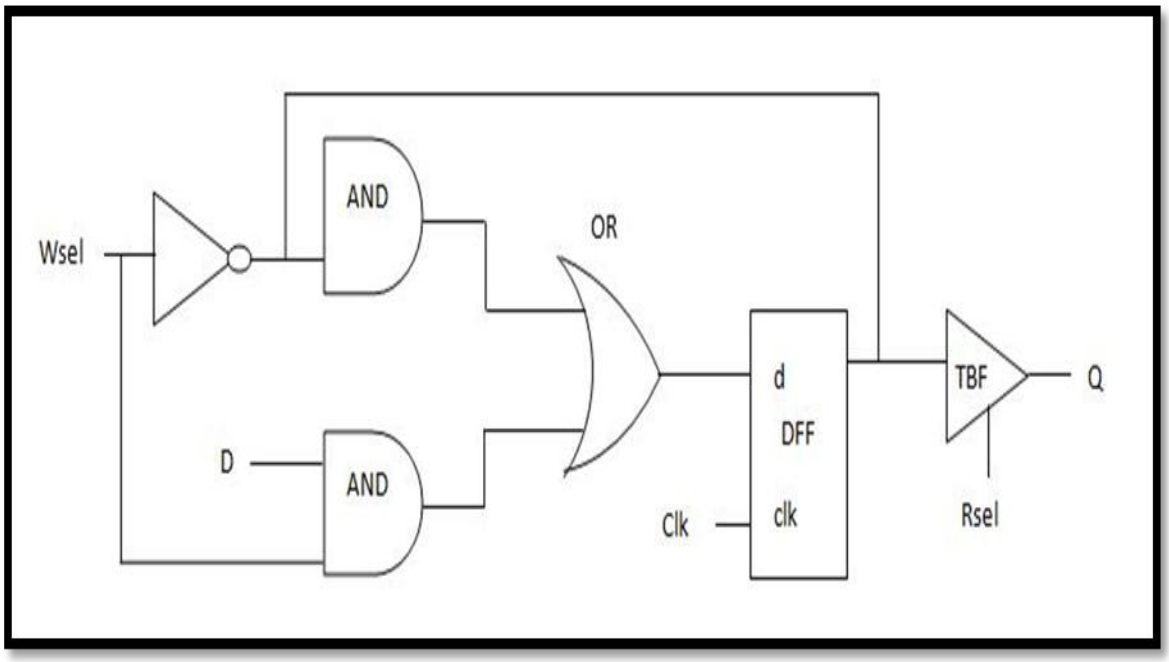


Fig.9. 1-Bit Register

5.5.1. Sleepy stack inverter:

The sleepy stack inverter is an important design in this research study which is used to reduce the leakage effects during the operation of MAC unit. The sleepy stack inverter is a combined version of two techniques known as sleep technique and stack technique. Hence the proposed inverter is termed as an ultra low power leakage cmos Sleepy Stack inverter.

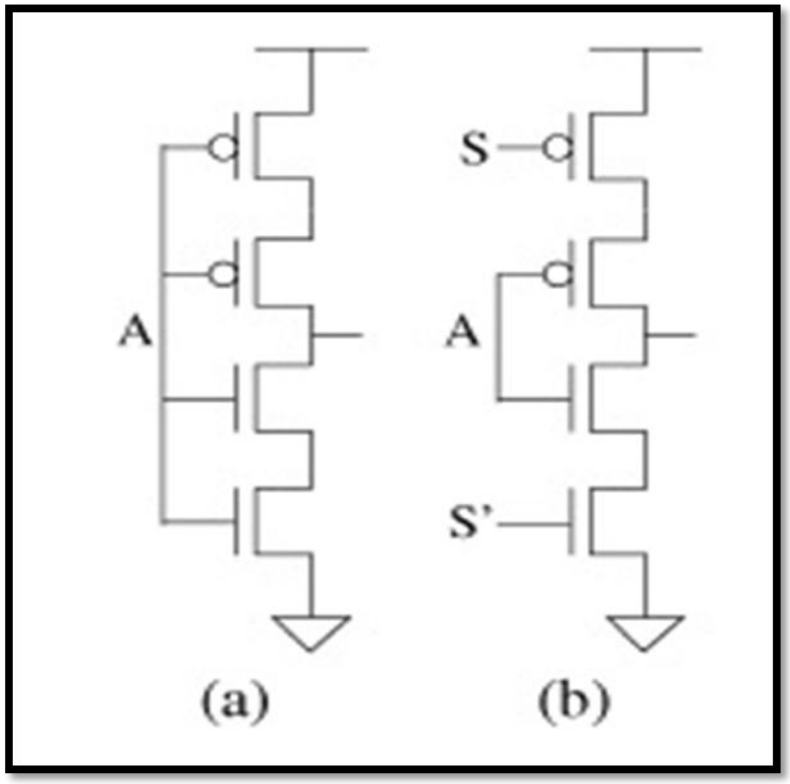


Fig.10. (a) forced stack technique (b) sleep transistor technique

The sleepy stack inverter operates in two modes of operation. They are:

1. **Active mode:**

   The architecture of sleepy stack inverter uses low V_{th} transistors and high V_{th} transistors. Due to this there is a control on the leakage effects. During this mode of operation the signals S and Sbar are turned on such that there exists a path between source to drain of the transistor. The high V_{th} transistor passes the VDD to the output through the low V_{th} transistor irrespective of the transistors parallel to the high V_{th} transistor. Due to this effect the inverter circuit enables high switching speed throughout the operation.

2. **Sleep mode:**

   During this mode the signals S and Sbar are turned OFF. The reduction of leakage in currents can be obtained by two ways.

   - First if the signals S and Sbar are killed off due to this there is an impact on the spillage current.
   - Suppose if the input signal is passed through "1" the transistors P1 and P3 are turned OFF and the transistors N3 and N1 are turned ON there exists a stack effect.

- Stack effect is nothing but when two are more transistors are turned OFF or ON simultaneously create an effect known as stack.
- Due to the stack effect there is a reduction in the leakage power due to the stack effect in the sleep mode.

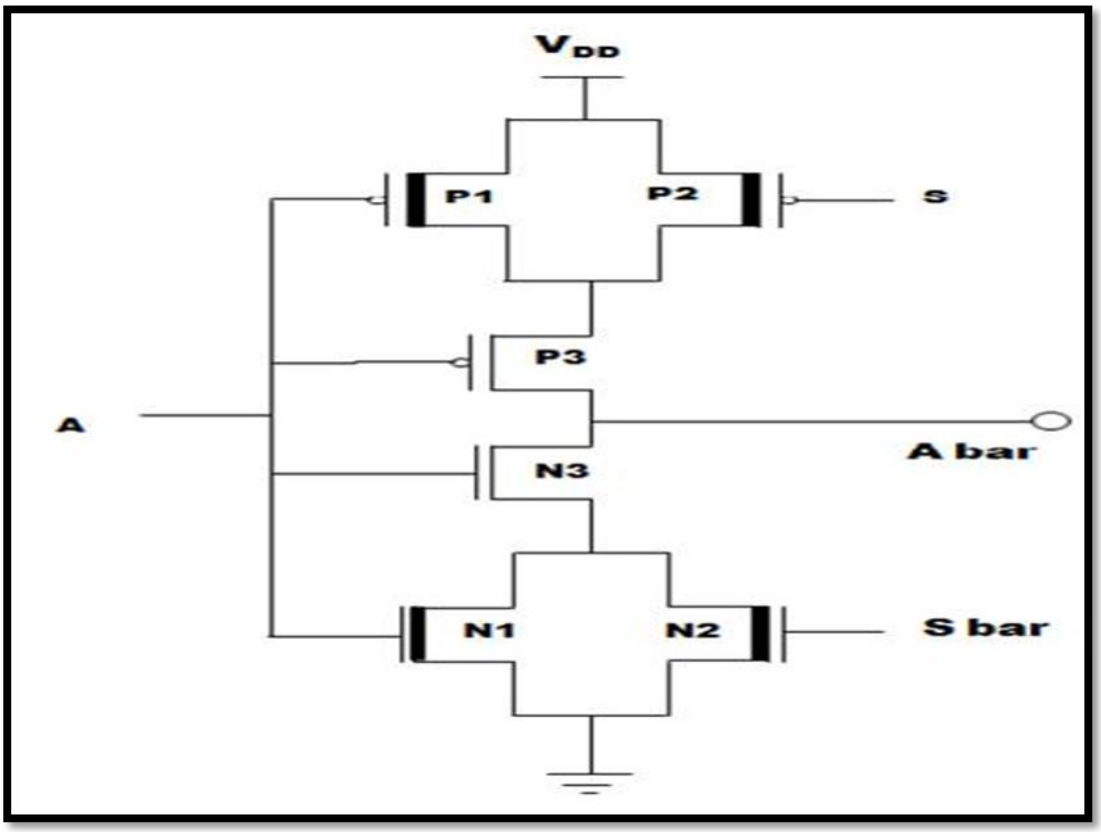


Fig.11. Sleepy Stack Inverter

5.5.2. D-Flip Flop:

The proposed D Flip-flop technique is based on a Hybrid Node Dual Dynamic Flip-Flop which removes the capacitance at precharge node follows a dynamic node structure which drives the output of the pull up, pull down transistors. The d-flip flop used here is designed using the sleepy stack technique which enhances high switching speed and less power dissipation and low leakage currents through the register unit. In the digital circuits the storing of data is done with the flip flops or latches. So, the design of d-flip flop has to be maintained at low power and high switching speed. The flip flop design used in the proposed architecture has two phases of operation. The design is based on a conventional dual dynamic flip flop which enhances the high switching speed throughout the circuit. The function of d flip flop is that it maintains the output which is followed by the input

whenever the clock pulse is high. So the flip flop designed here is a positive edge triggered hybrid node flip flop.

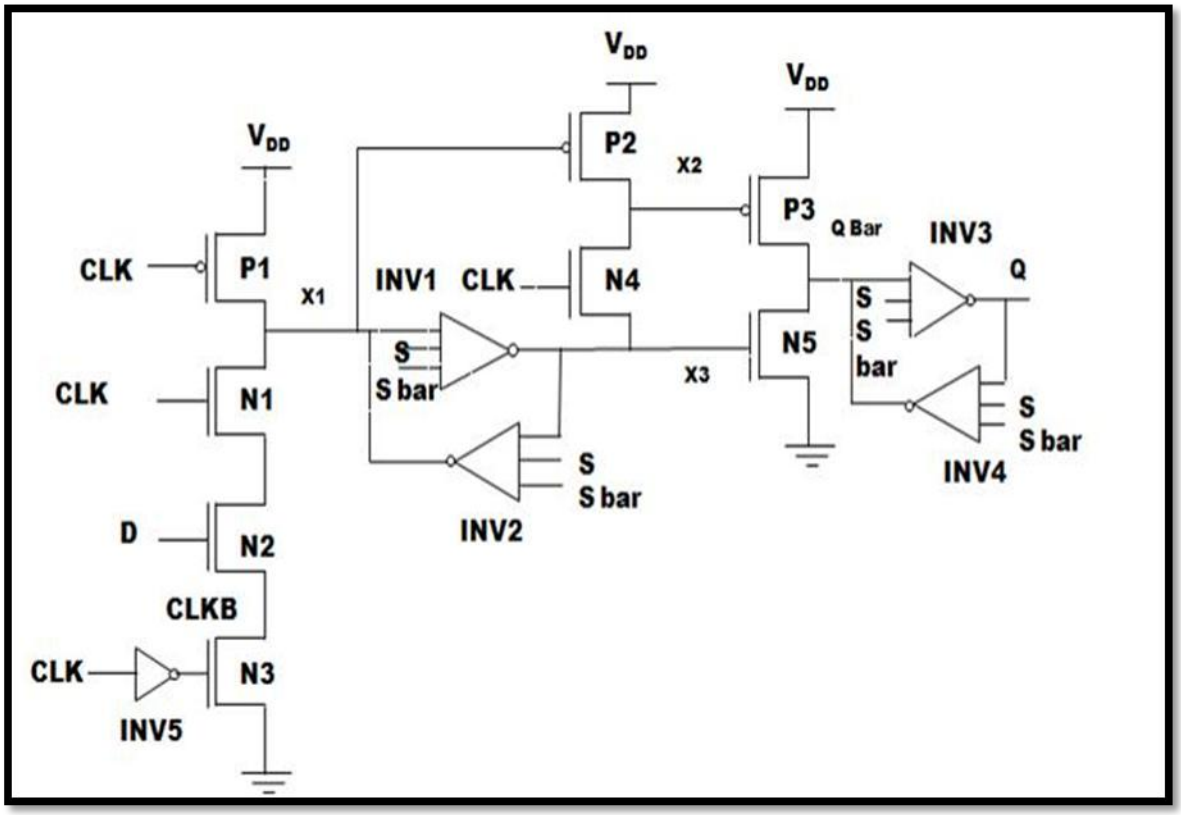


Fig.12. D-Flip Flop

The operation of the proposed flip flop is as follows:

1. **Evaluation Phase:**

   During this phase of operation the clock signal is asserted to be high and let the input be high. The node X1 exhibits logic zero and the node X2 maintains the logic high during the evaluation mode and the Q bar discharges to zero and the output Q is high till the precharge phase occurs. If the input is low then the node X1 exhibits logic one and node X2 exhibits logic low and the output at Q is zero.

2. **Precharge Phase:**

   During this mode of operation the clock signal is asserted low and the input can be '0' or '1'. The entire circuit maintains the previous logic state during this mode of operation until the next evaluation phase occurs. During this mode of operation there is a possibility of the leakage currents. To eliminate this sleepy stack inverter technique has been used in the design of hybrid flip flop which eliminates the leakage effects during the sleep mode.

5.6. Fixed-Point Unsigned Number Architecture:

In this study a new architecture for MAC unit depending upon the literature work has been proposed. The existing MAC unit function is that it multiplies the two values and then passes the multiplied value into the register. The register stores the multiplied value for the certain period of time and then passes the values to the adder circuit. The adder circuit sums the multiplied value with previously accumulated values that are stored in the feedback accumulator register.

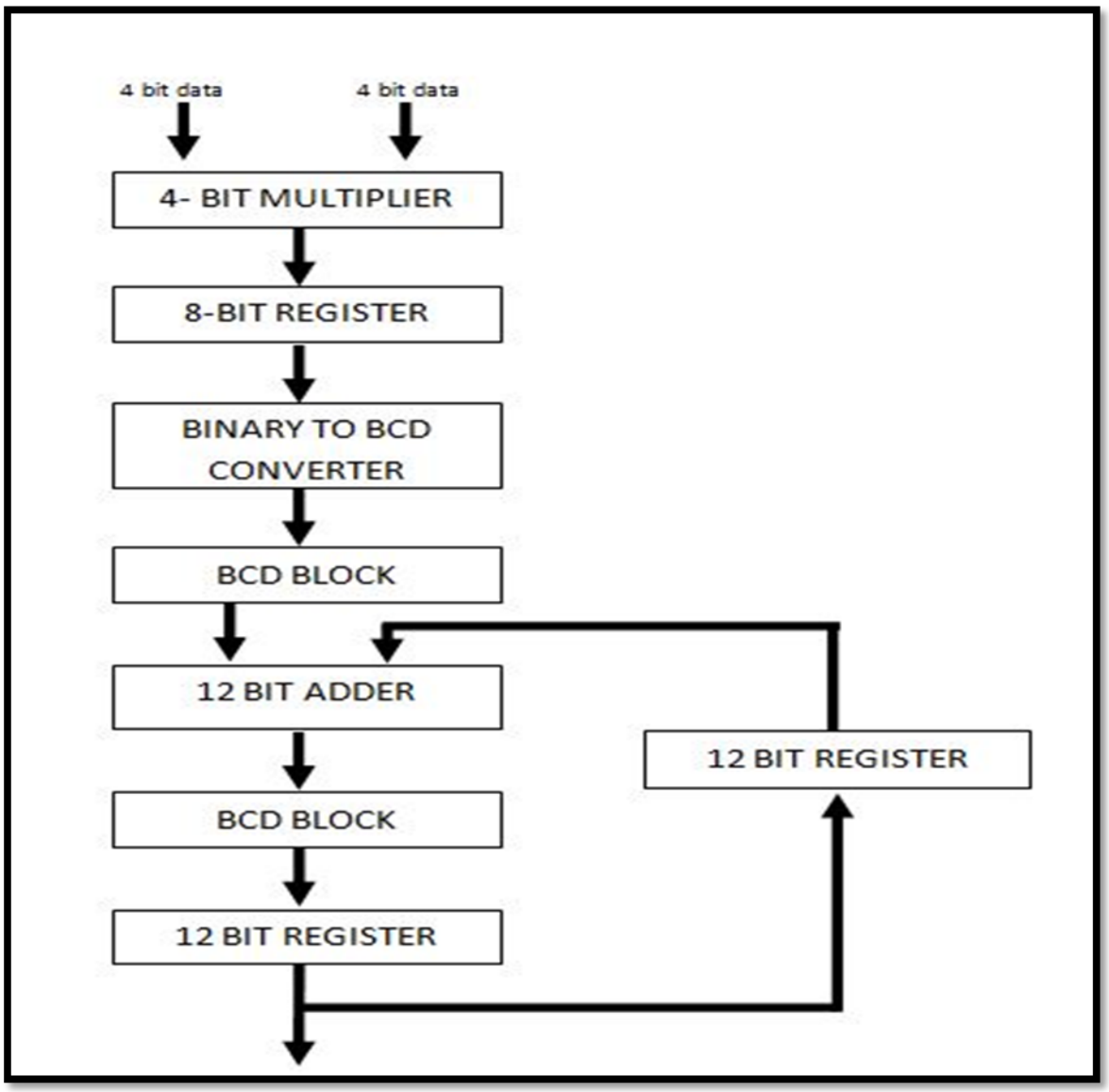


Fig.13. MAC Unit for Unsigned Number Architecture

The proposed MAC unit also works on the same function but with an additional synchronization of basic blocks that are necessary for the proposed design. The architecture for unsigned number system depends upon the existing MAC unit for the digital processing. The existing MAC unit design is for basic number system while the

proposed MAC designs are for BCD number systems. The basic individual blocks that are in the proposed design consists are Wallace tree multiplier, register unit, binary to BCD converter, BCD block to maintain the entire MAC unit to be in the BCD format, 12-bit adder of 9T transistors and a 12-bit accumulator register. The operation of the proposed design is that two sets of 4-bit input patterns are given to the multiplier unit where it gives an output of 8-bit. The 8-bit output from the multiplier block is stored in the 8-bit register unit when the "Wsel" signal is asserted high. After certain time period the "Wsel" signal is asserted to be low and "Rsel" signal is asserted high and the data is read to the binary to BCD depending upon the clock signal. The binary to BCD block converts the output of the multiplier values to the BCD format. The output from the binary to BCD is passed through the BCD block which maintains the values to be in the correct BCD format. The BCD values are given to 9T adder circuit which sums the current input values with the previously accumulated values that are stored in the feedback register. The output from the adder is again passed through the BCD block to maintain the output of the MAC unit to be in the BCD format.

5.7. Fixed-Point Signed Number Architecture:

The architecture for the fixed-point signed number is based on the proposed unsigned architecture. The operation of the signed architecture is similar to the unsigned architecture where the signed architecture deals with negative numbers. The input for the multiplier bit in this architecture is of 5-bit data where the higher bits of the two sets are Xored and the remaining input bits are multiplied using the multiplier block. The multiplier output will be of 8-bit and are stored in the register unit. The higher xored bit is directly by passed to the MUX block which determines that the input sets fetched are positive are negative.

The register unit stores the 8-bit data and passes it to the binary to BCD converter block and the same procedure is done as if in the unsigned architecture upto the BCD block. The function of signed architecture starts after the evaluation from the BCD block. The values from the BCD block are passed to the adder depends on the MUX block where the higher bits of the input patterns are xored and is used as a select line for the MUX block. Depending on the select line the MUX block determines whether the output from the BCD block will be positive or negative.

If the output of the BCD indicates a negative number depending upon the select line it is 10's complemented and passed through the MUX to the adder.

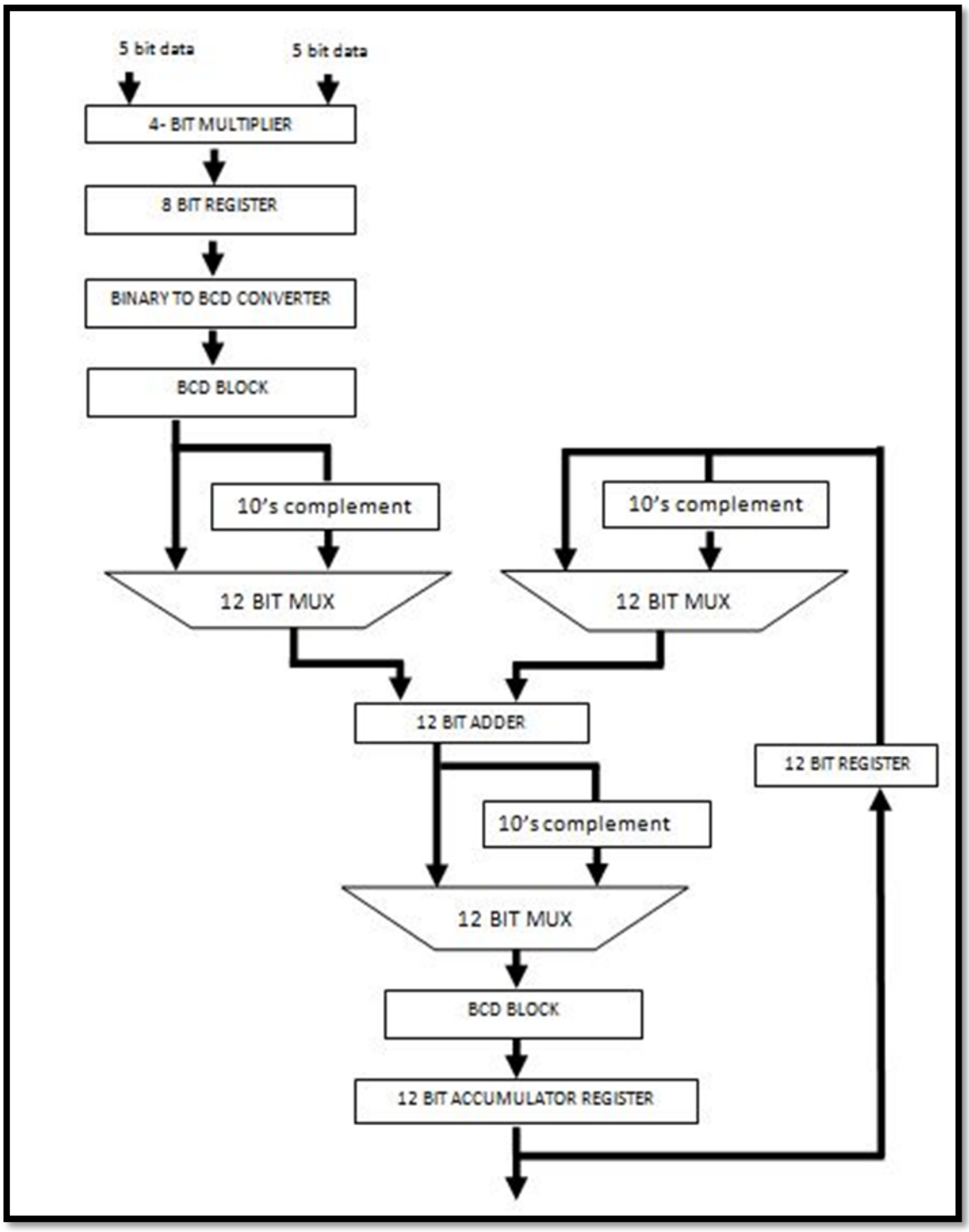


Fig.14. MAC Unit for Signed Number Architecture

There exist four possibilities of the number system during the analysis of the MAC unit for the signed number architecture.

- Both the numbers can be positive.
- First number can be positive and second number can be negative.
- First number can be negative and second number can be positive.
- Both the numbers can be a negative.

The fixed point signed architecture functions as follows. The output from the BCD block is verified through a MUX block whether it is a positive or negative and if it is a negative number the BCD output is 10's complemented and passed to the adder circuit to add with the previously accumulated value. Here again there is a possibility of negative number addition through the feedback register which stores the accumulated values. Hence the feedback accumulated value is 10's complemented depending upon the higher MSB bits. If the feedback value is a negative number it is 10's complemented and passed to the adder to add with the current input values that are the outputs from the BCD block. If the output of the BCD block is positive number and the accumulated value is negative then the accumulated value is 10's complemented and added with the BCD outputs. If both the combinations are negative then both the values are 10's complemented and added. After the addition of the current input with the previously accumulated value there is a chance of detection in the negative numbers. So, there is a need of 10's complementing the adder output depending upon the higher MSB bits if those indicate that the output of the adder is negative number.

5.8. Floating-Point Number Architecture:

The proposed MAC design for the floating point number is designed using the proposed MAC unit for fixed point signed numbers. Here in the fixed point architecture a simple MAC unit with an additional binary to BCD and BCD block is added to maintain the overall output of the MAC unit to be in the BCD format. As the same technique is used to design the floating point architecture with necessary modifications where there is a parallel analysis of the mantissa and the exponent term. The mantissa part is implemented by giving the mantissa bits as inputs to the multiplier block where there will be XOR of sign bits parallel to the multiplier and the output from the XOR will passed to the MUX that discharges the signal from the BCD block to find whether the output from the BCD block is signed or unsigned. The multiplier multiplies the mantissa bits and passes to the register block. There is a need for binary to BCD converter because the output from the multiplier will be in the binary format and it passes the output to the BCD block. The BCD block maintains the product term to be in the BCD format and passes the value to the MUX depending on the sign bit which acts as a select line. The feedback from the register is also passed through the MUX depending on the upper MSB of the feedback input and the outputs from the MUX blocks are passed to the adder to add. Once again

there is a need for the MUX which again generates an unsigned output and passes the

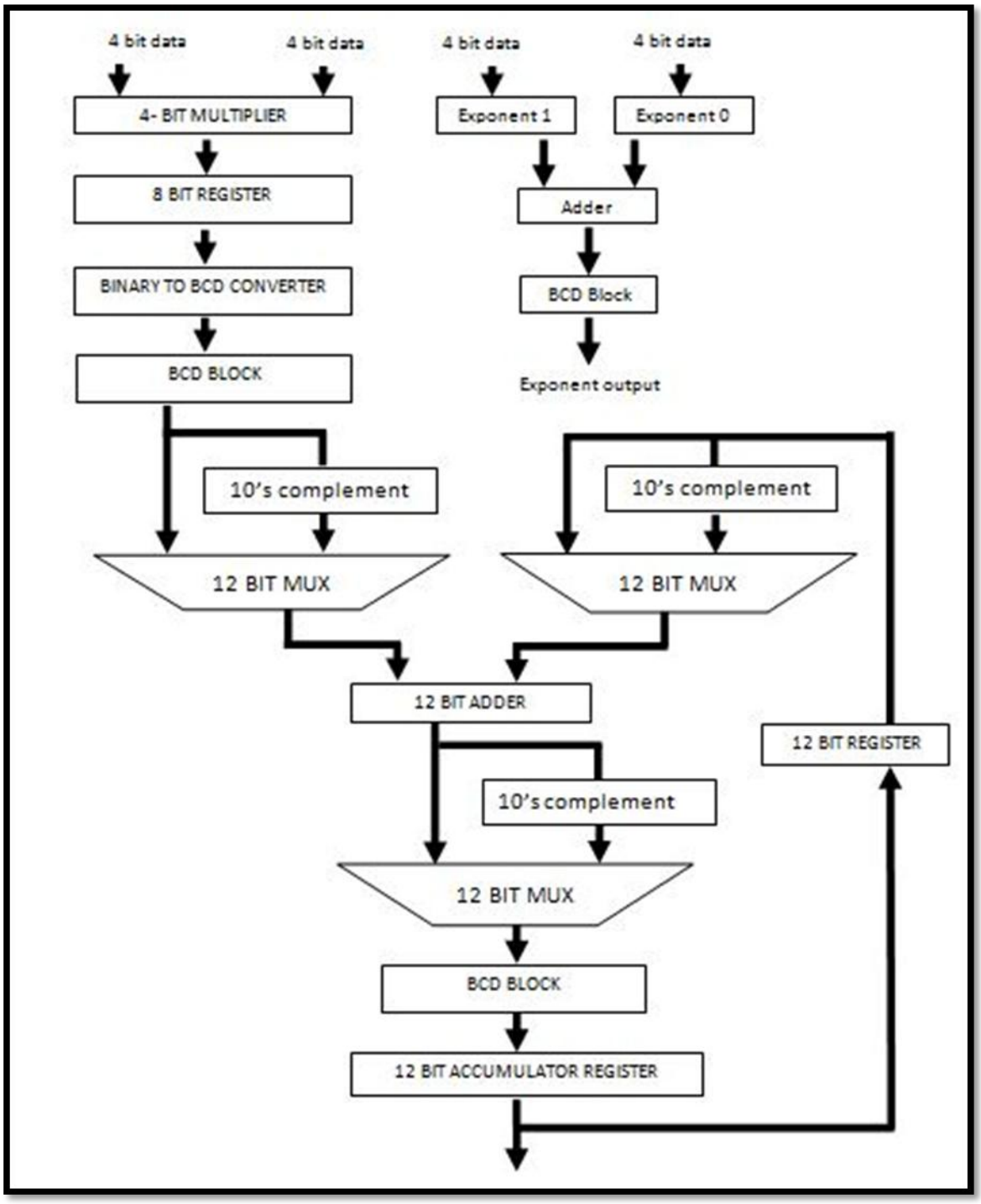


Fig.15. MAC Unit for Floating Point Number Architecture

value to the BCD block. Here again the BCD block maintains the overall output to be in the BCD format and the output is stored in the feedback register for the next addition and the output is read through the consecutive register at the last. The exponent terms are parallel added with the full adders and are bypassed through the BCD block if necessary and read at the output through bypassing.

CHAPTER 6

EXPERIMENTAL WORK

Sleepy Inverter Schematic:

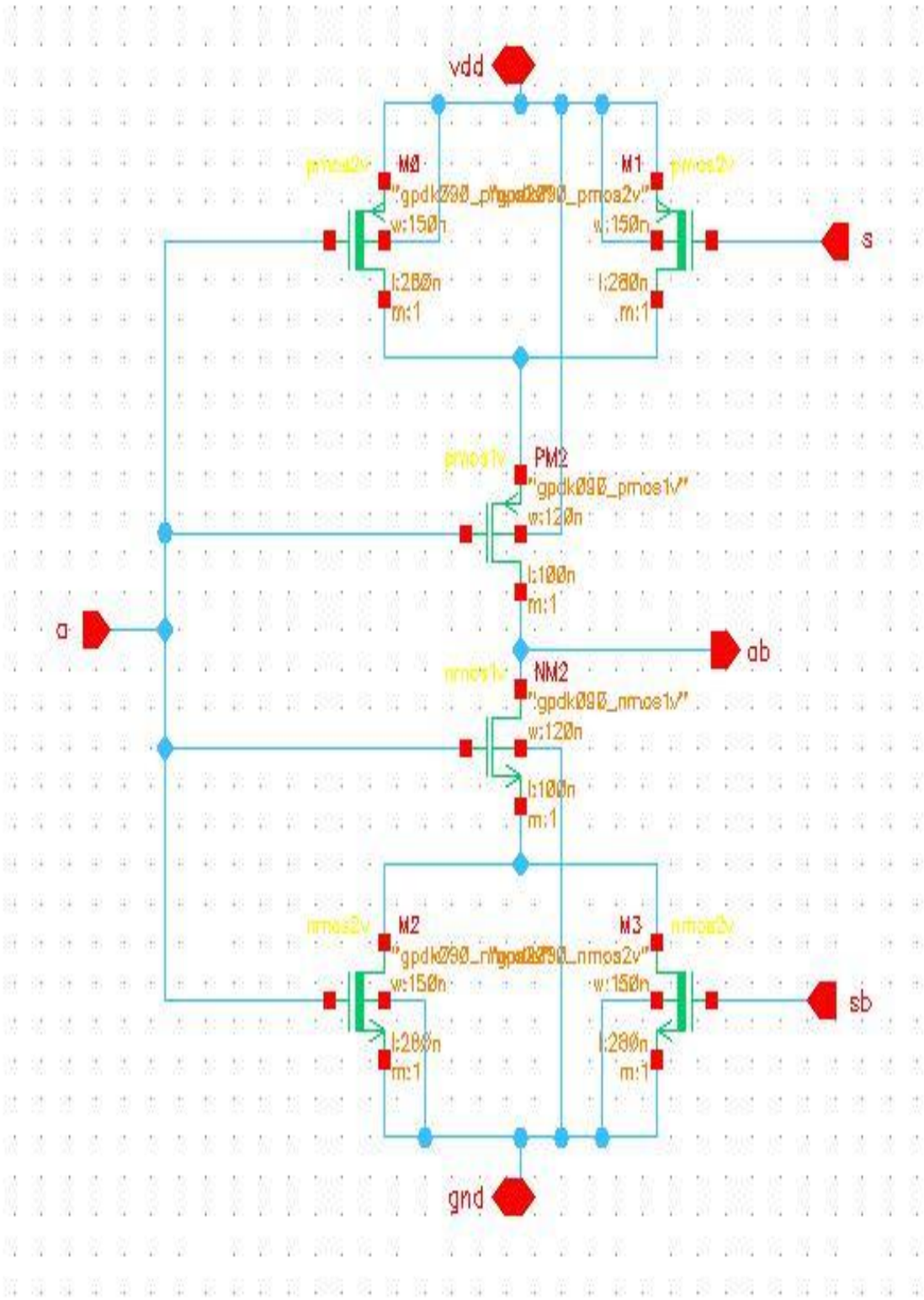


Fig. 16. Sleepy Inverter Schematic

D-Flip Flop Schematic:

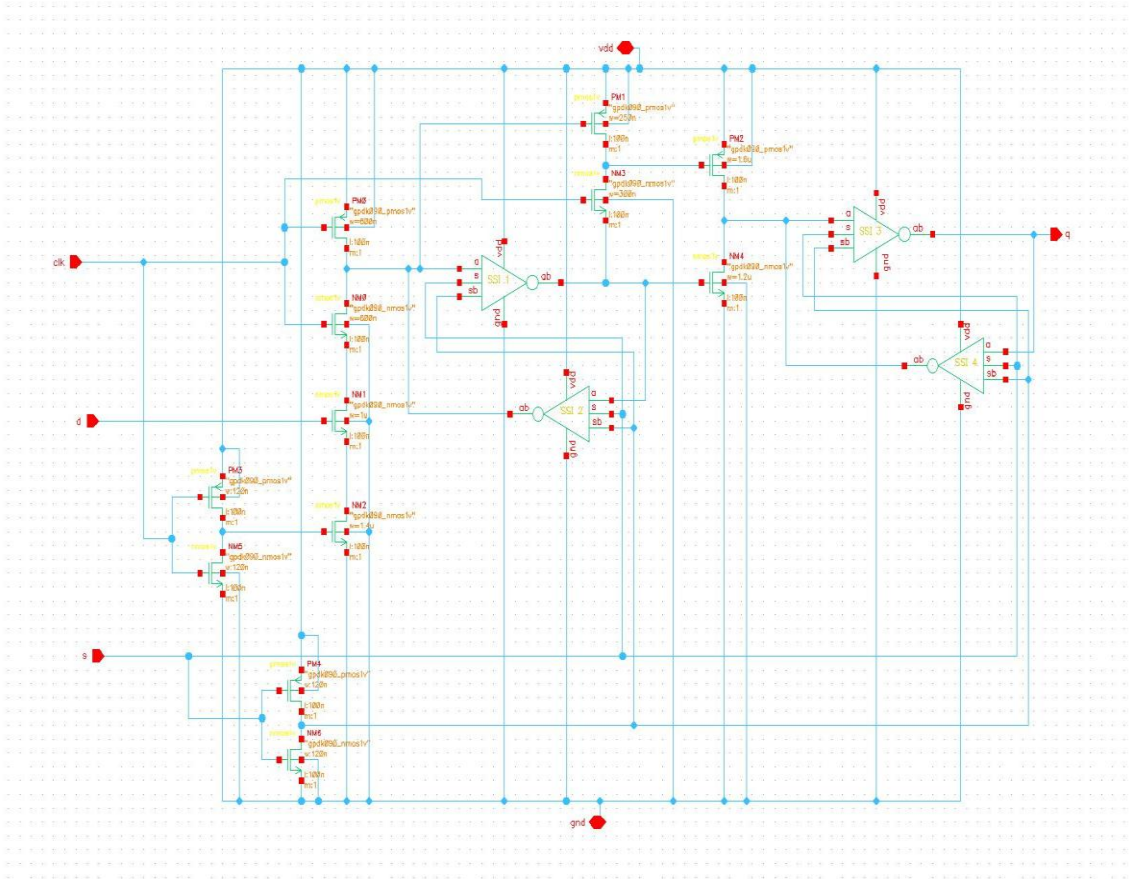


Fig.17. Proposed D-Flip Flop Schematic

1-Bit Register Schematic:

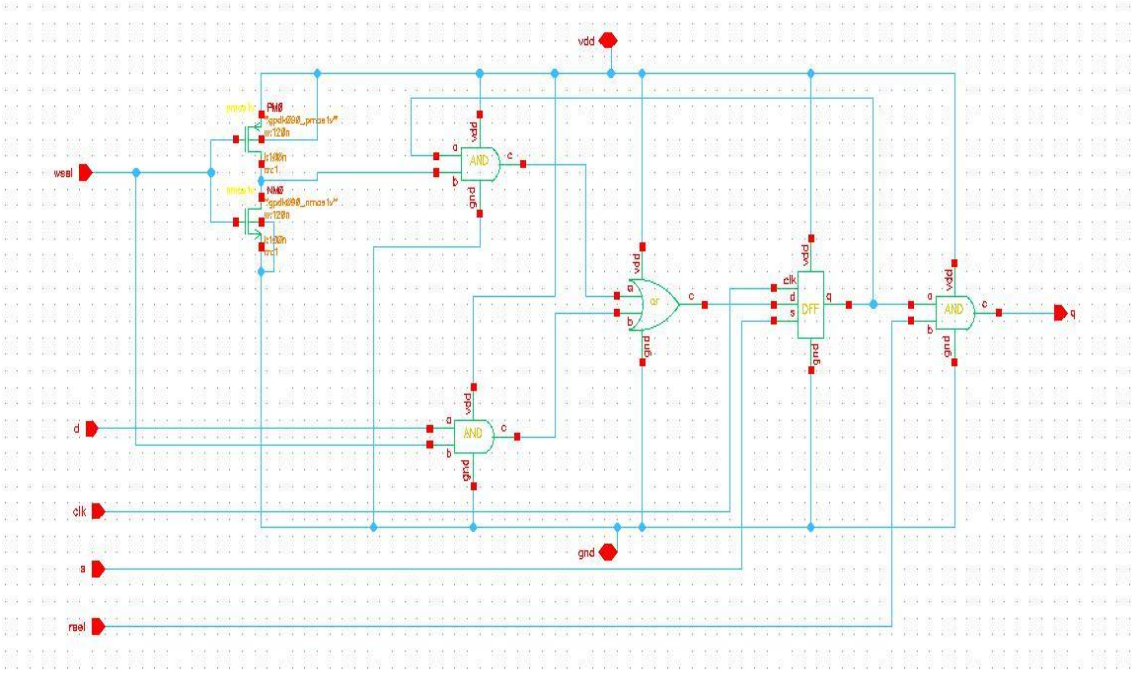


Fig.18. 1-Bit Register Schematic

8-Bit Register Schematic:

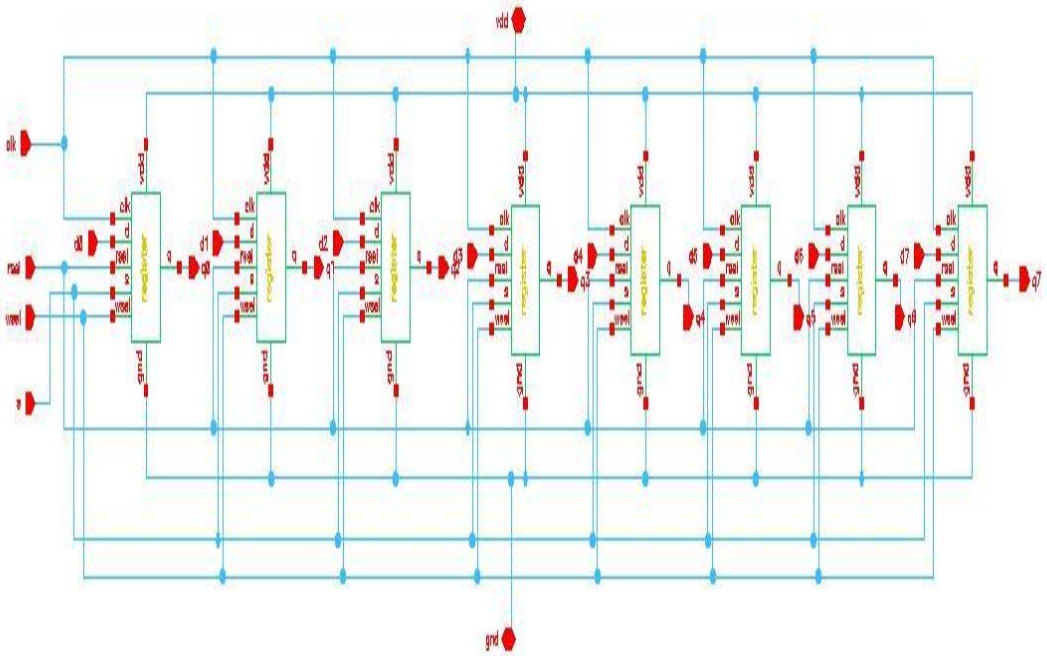


Fig.19. 8-Bit register Schematic

12-Bit Register Schematic:

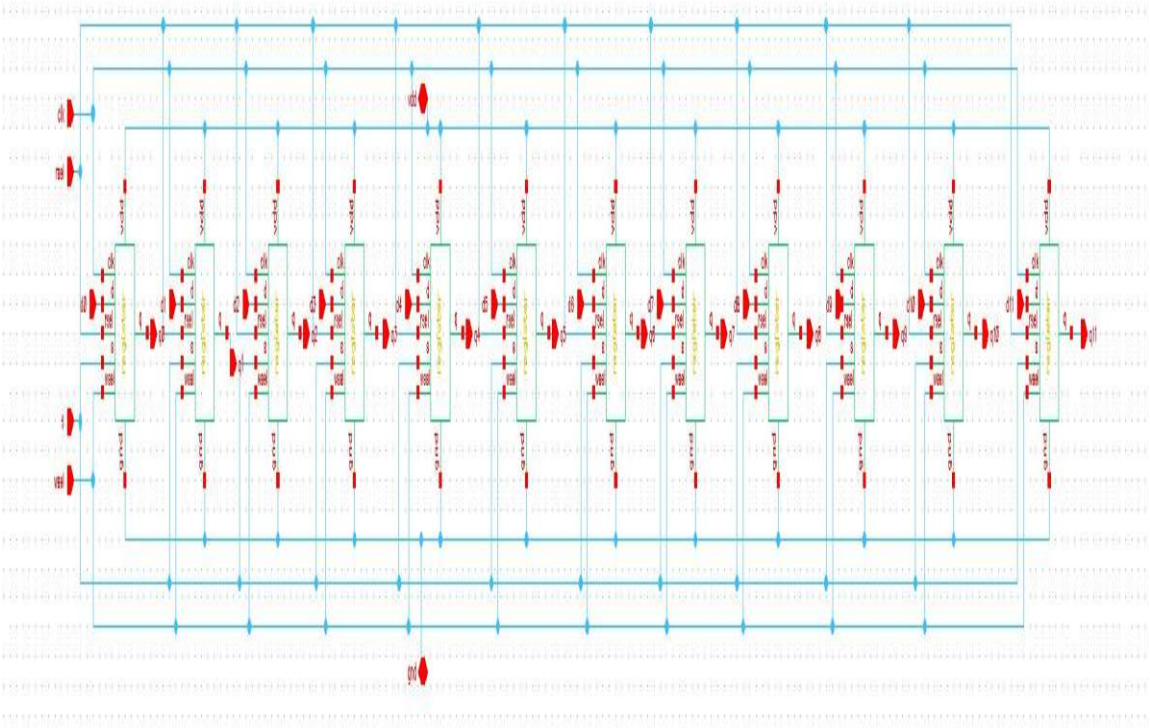


Fig.20. 12-Bit Register Schematic

1-Bit Adder Schematic:

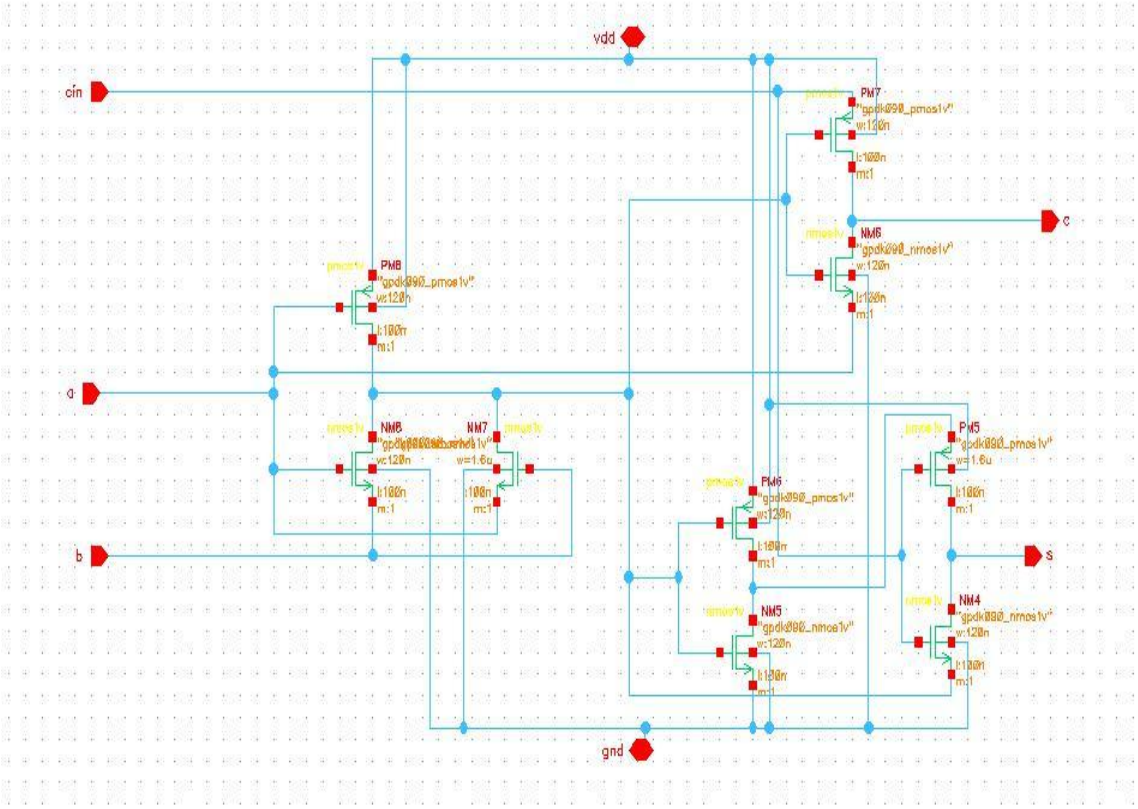


Fig.21. 1-Bit 9T Full Adder Schematic

12-Bit Adder Schematic:

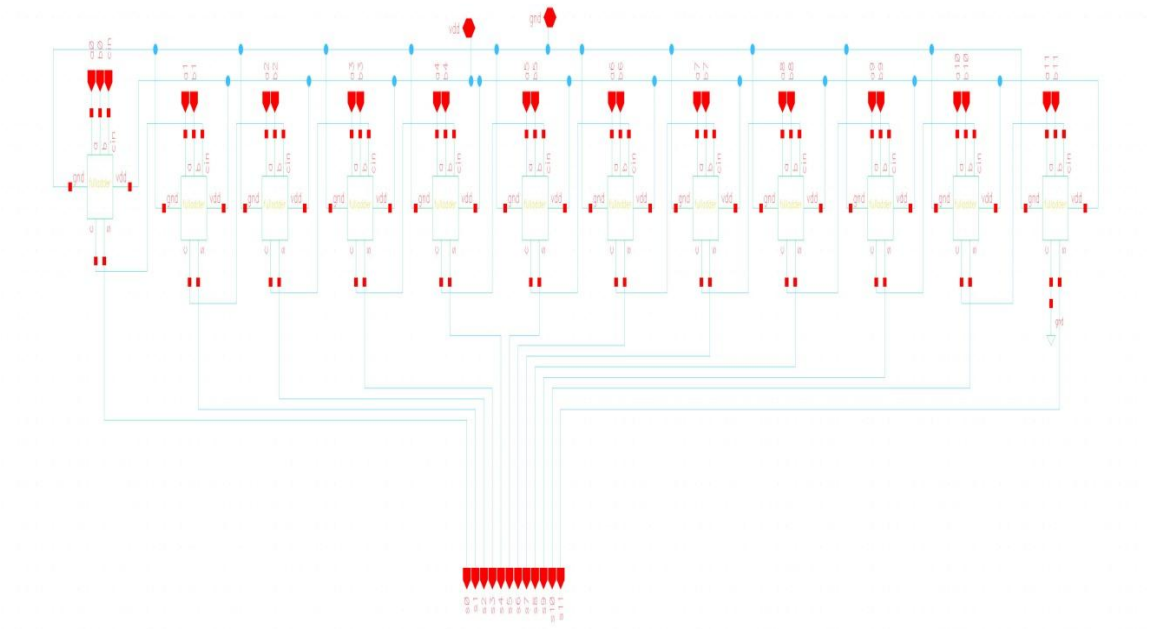


Fig.22. 12-Bit 9T Full Adder Schematic

4-Bit Multiplier Schematic:

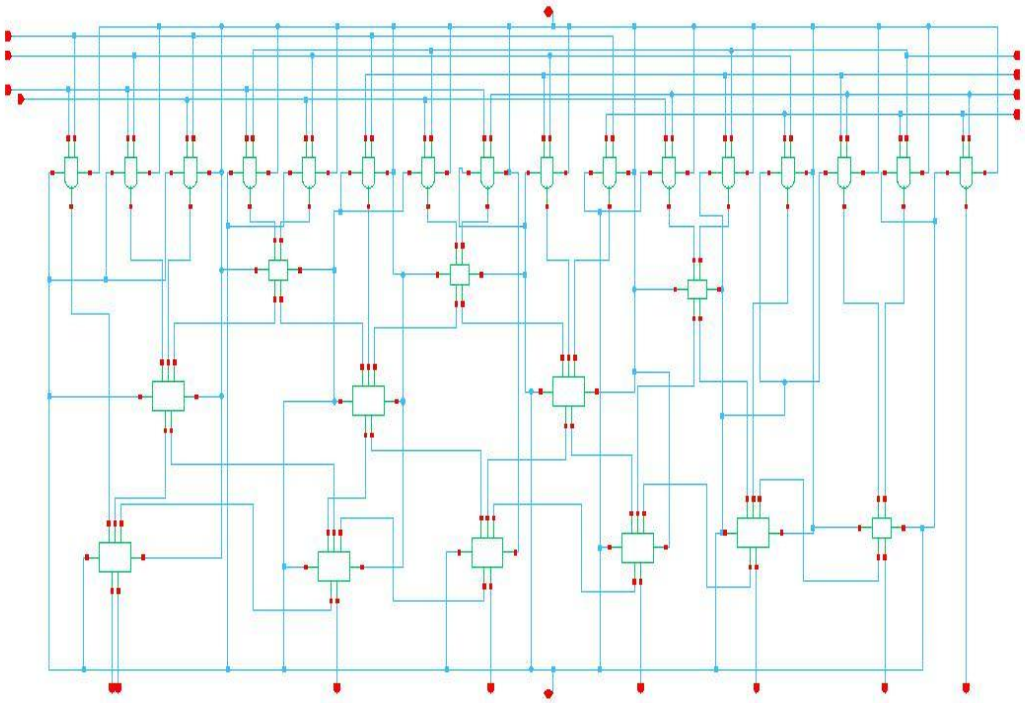


Fig.23. 4-Bit Multiplier Schematic

Binary to BCD Converter Schematic:

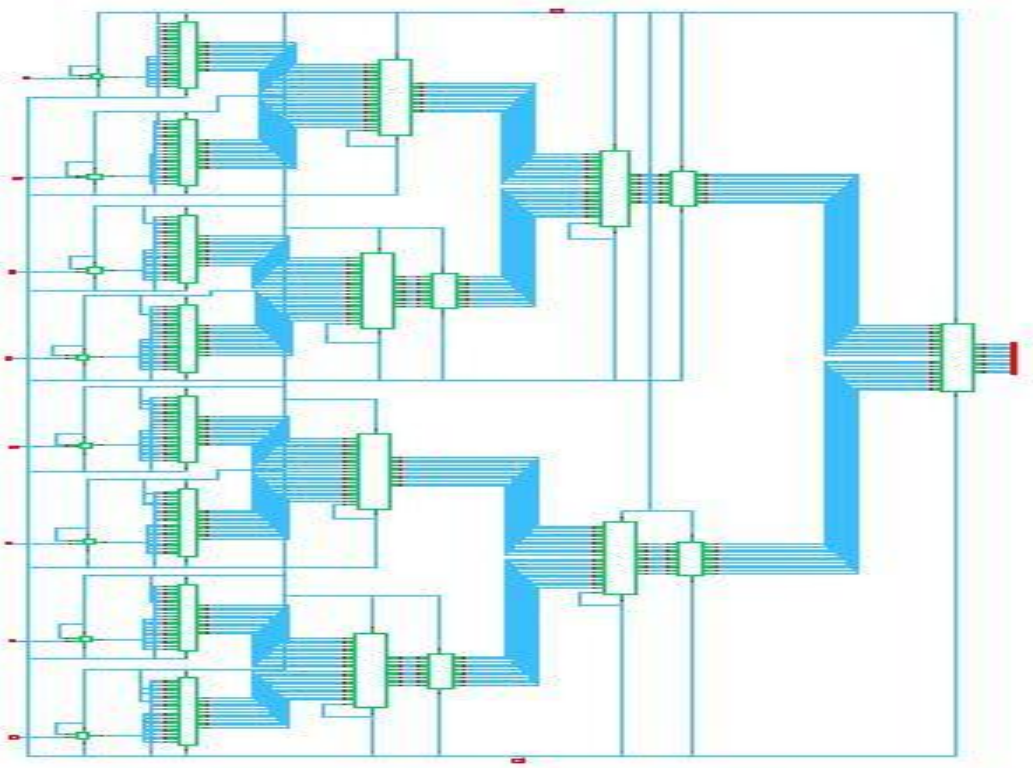


Fig.24. Binary to BCD Converter Schematic

BCD Block schematic:

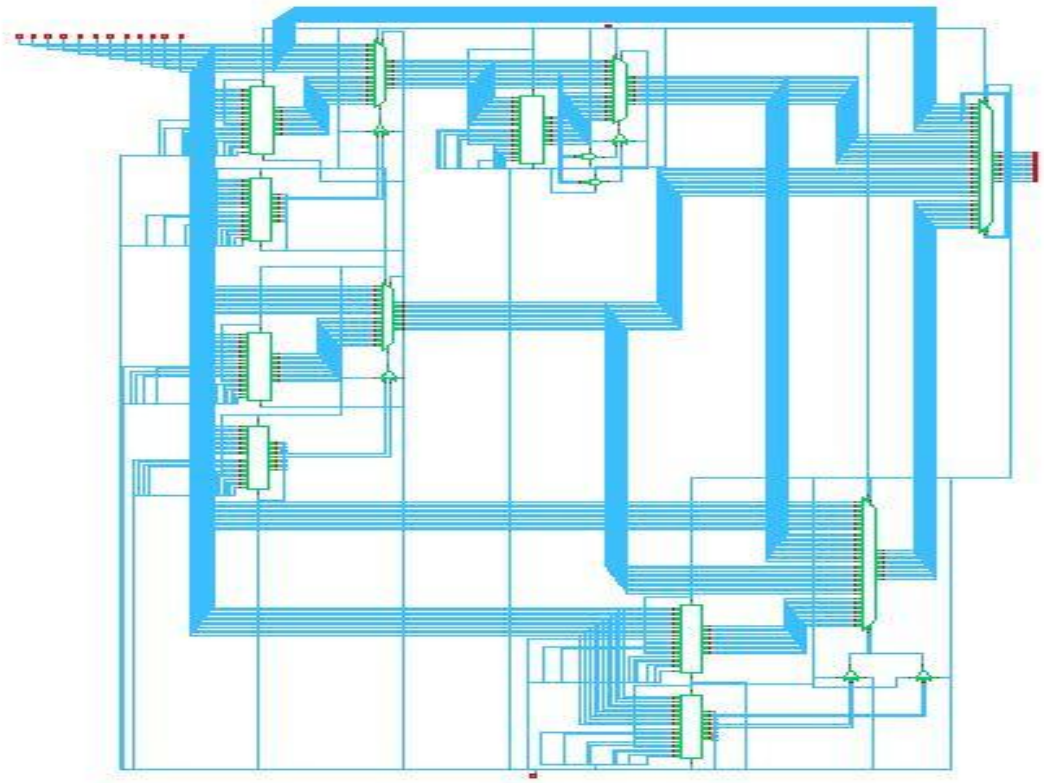


Fig.25. BCD Schematic

10's Compliment Schematic:

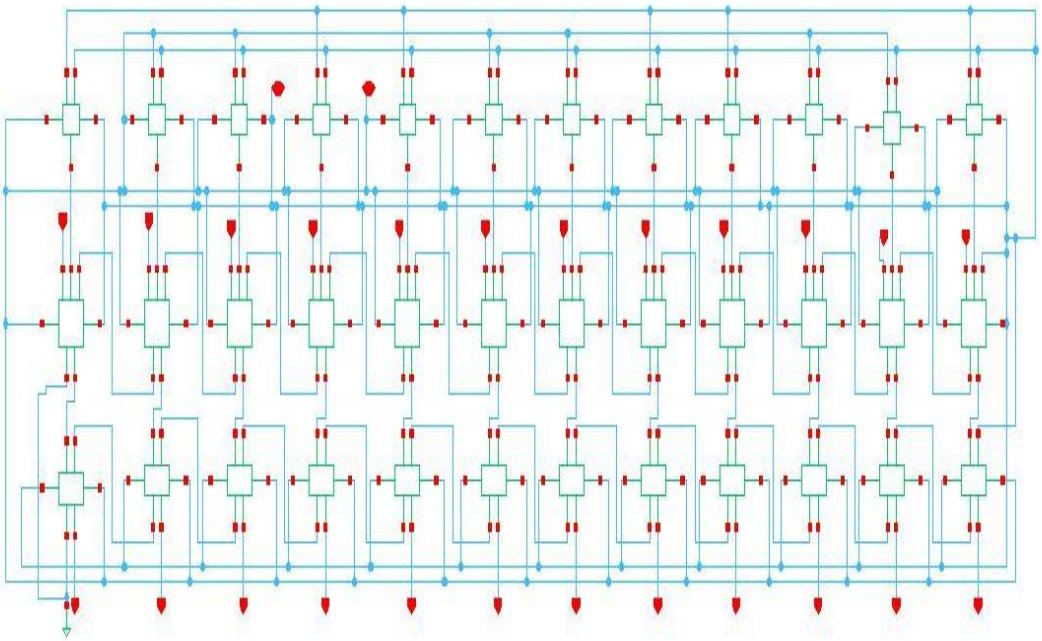


Fig.26. 10's Compliment Schematic

MAC for Unsigned Number Schematic:

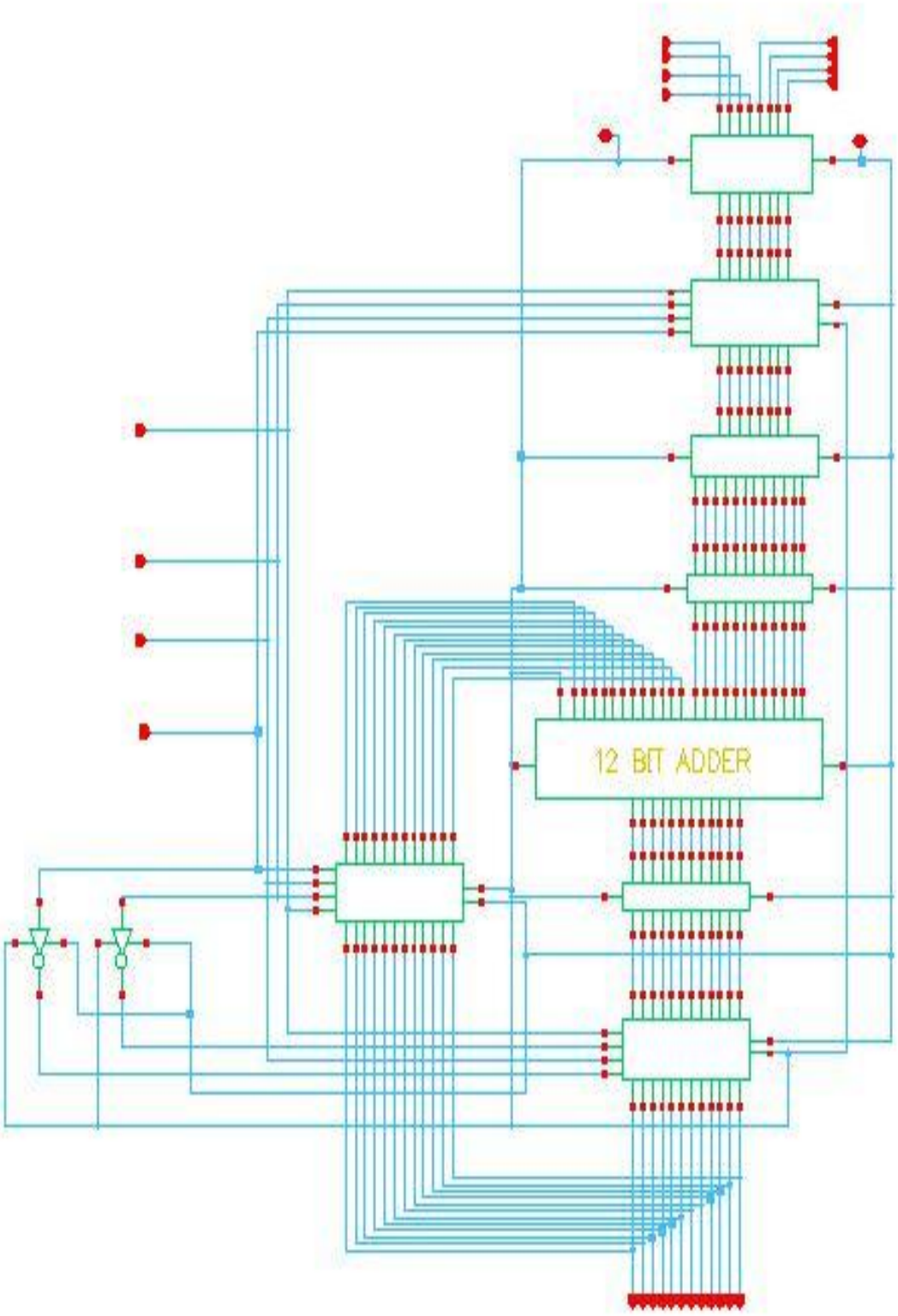


Fig.27. MAC Schematic for Unsigned Number

MAC for Signed Number Schematic:

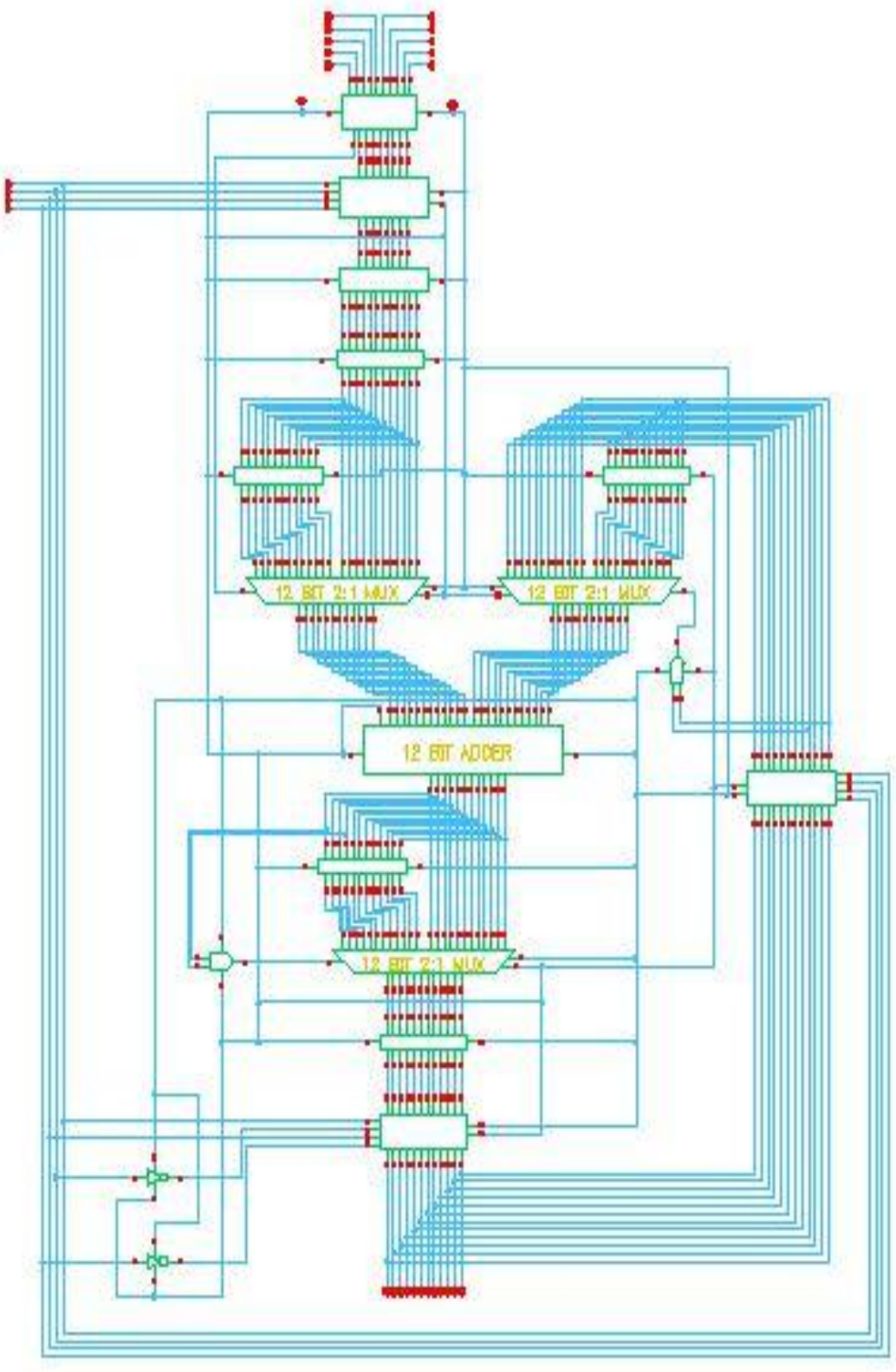


Fig.28. MAC Schematic for Signed Number

MAC for Floating Number Schematic:

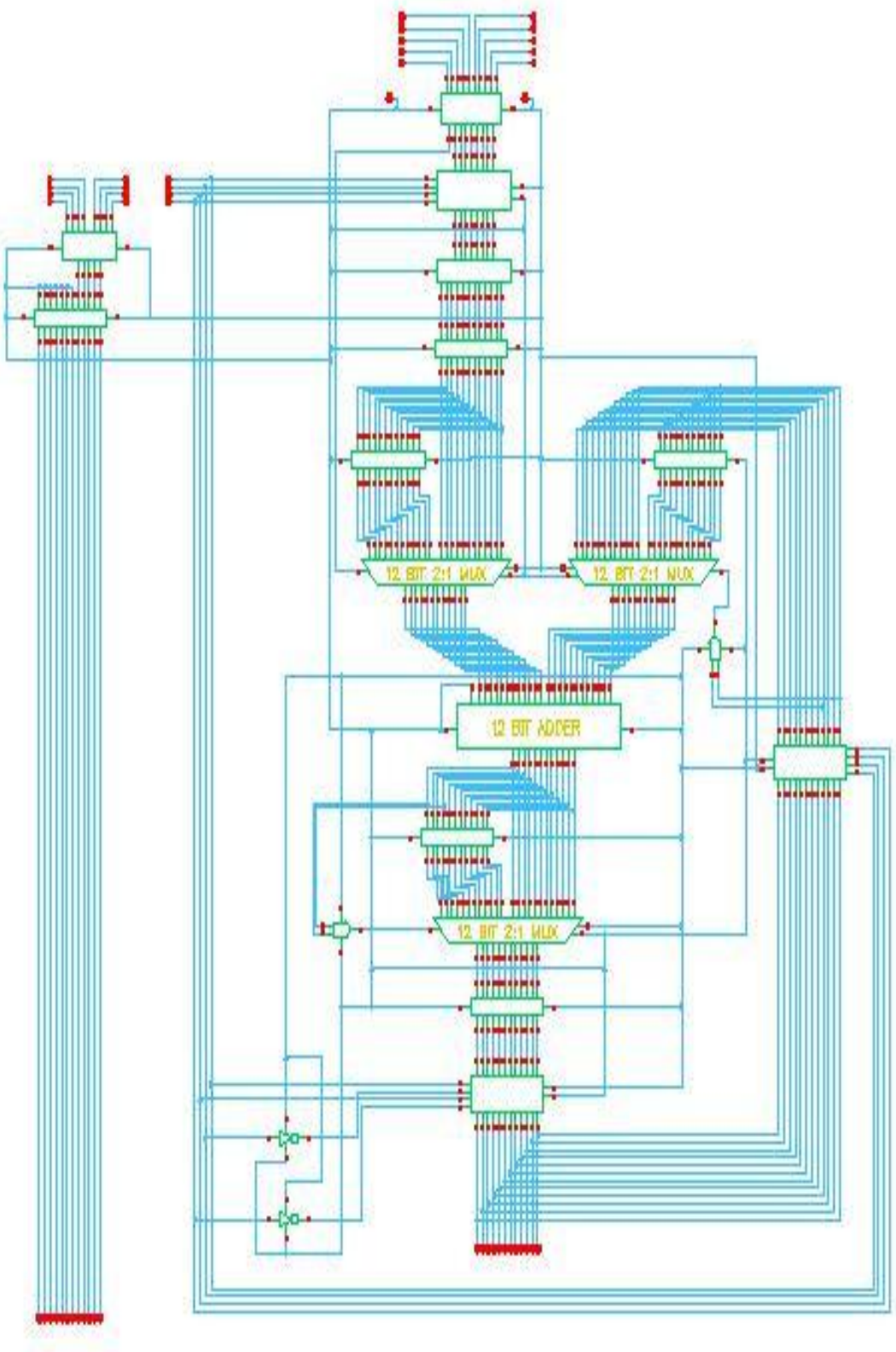


Fig.29. MAC Schematic for Floating-Point Architecture

CHAPTER 7

RESULTS AND ANALYSIS

Sleepy Inverter Output:

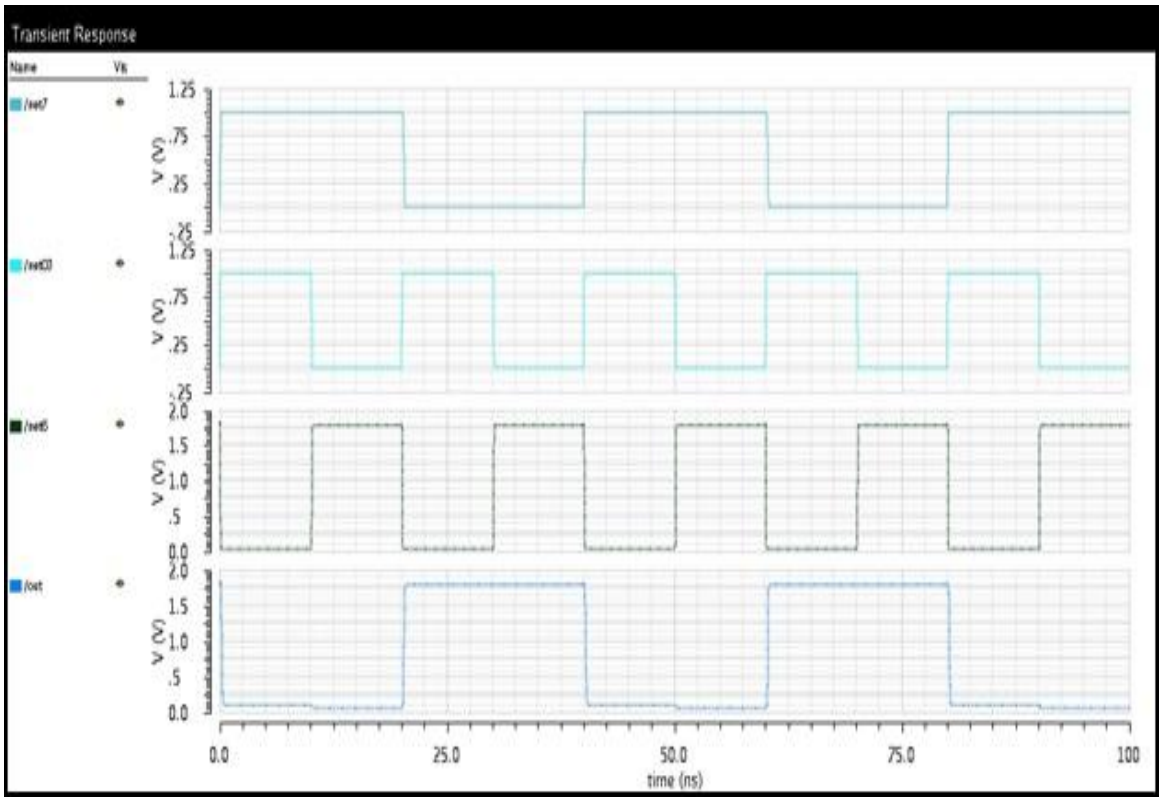


Fig.30. Sleepy Inverter Output

Sleepy Inverter Power:

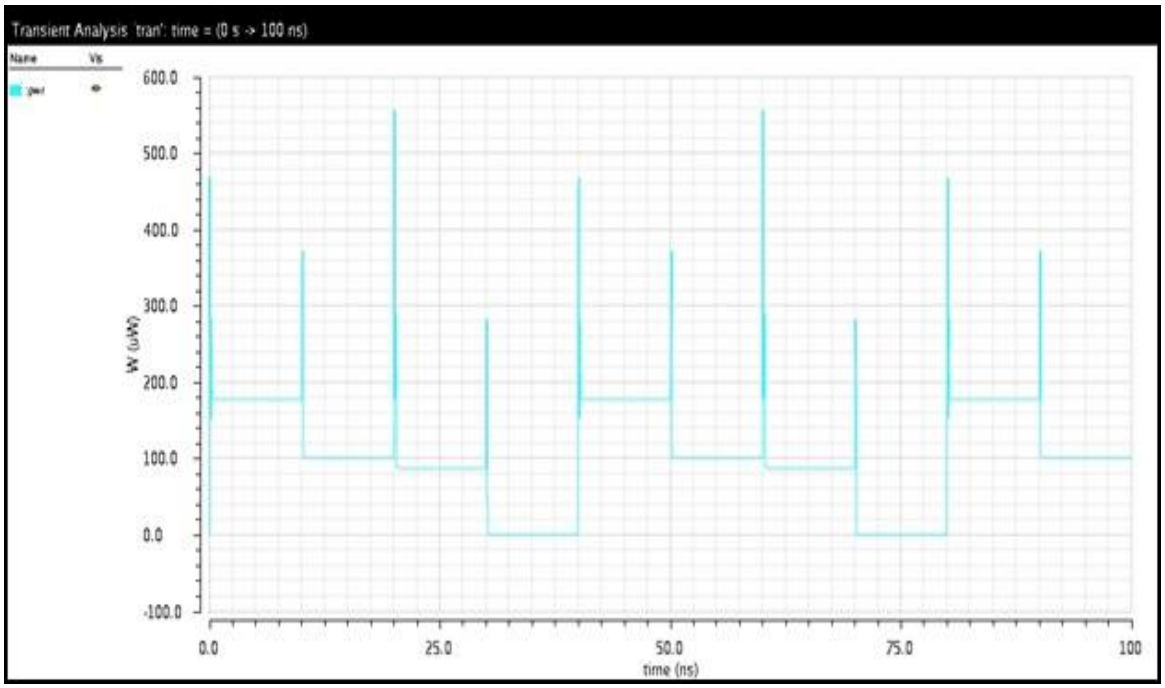


Fig.31. Sleepy Inverter Power

D-Flip Flop Output:

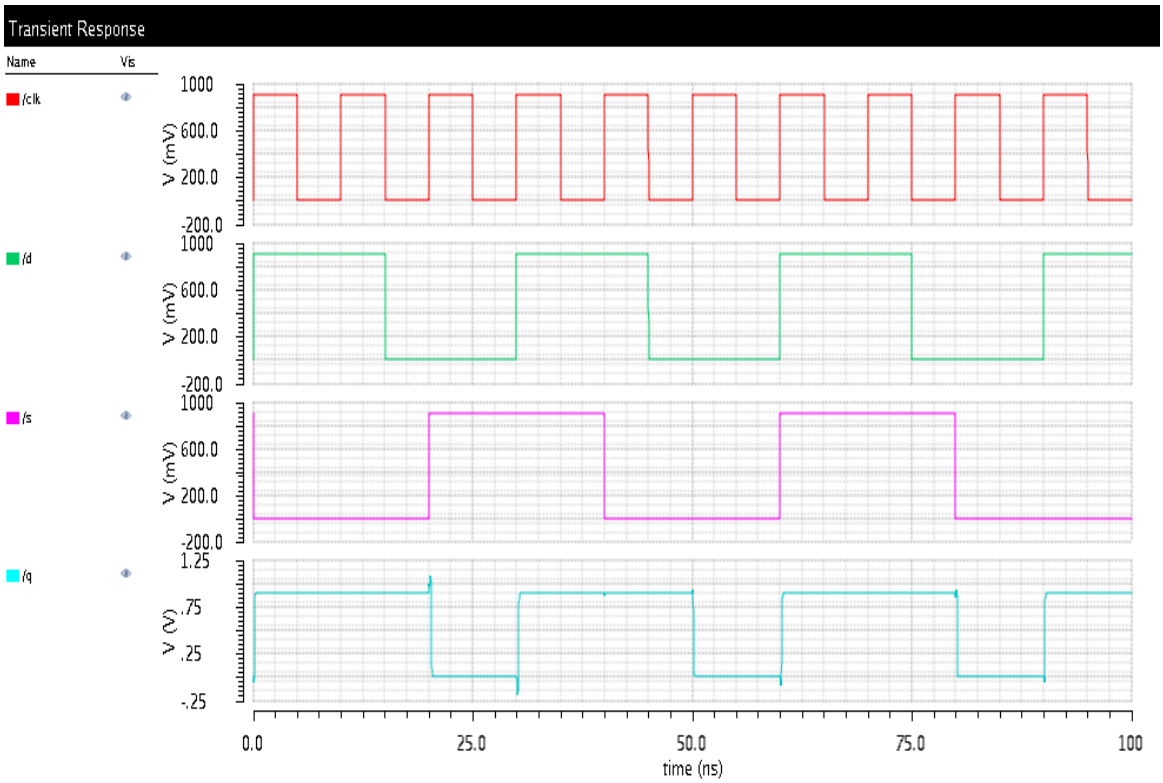


Fig.32. D-Flip Flop Output

D-Flip Flop Power:

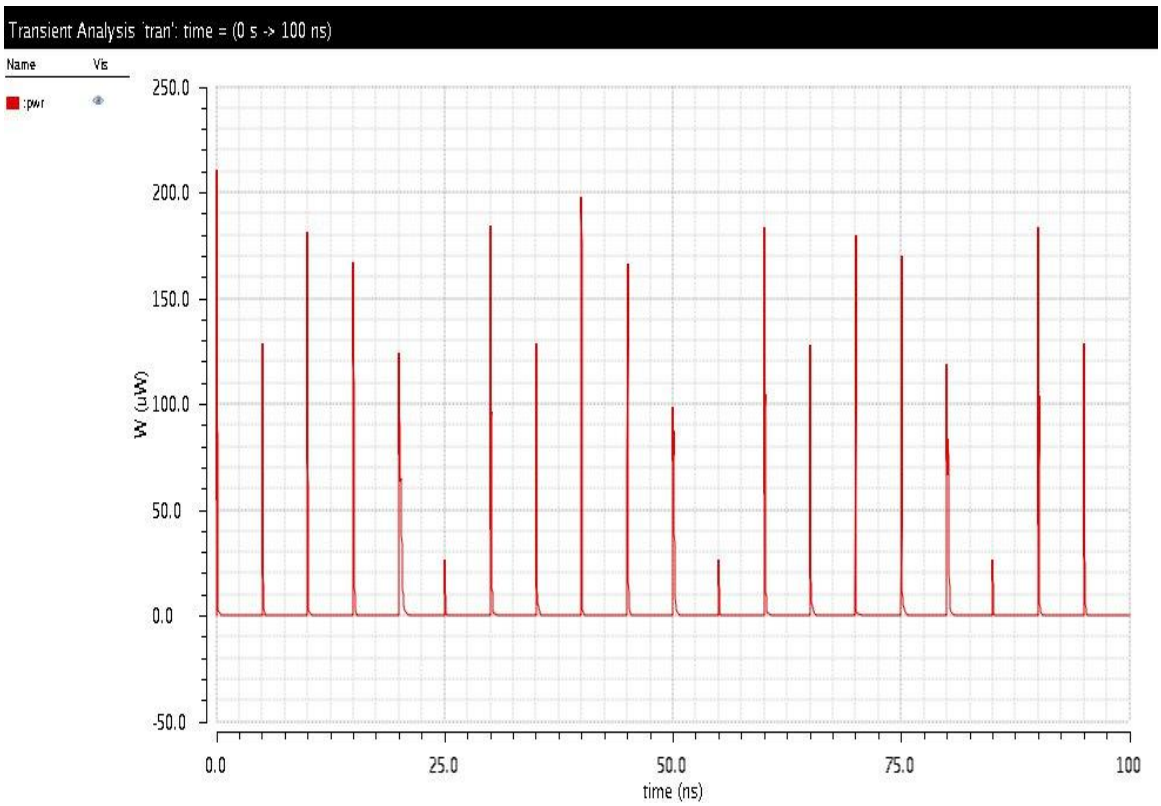


Fig.33. D-Flip Flop Power

1-Bit Register Output:

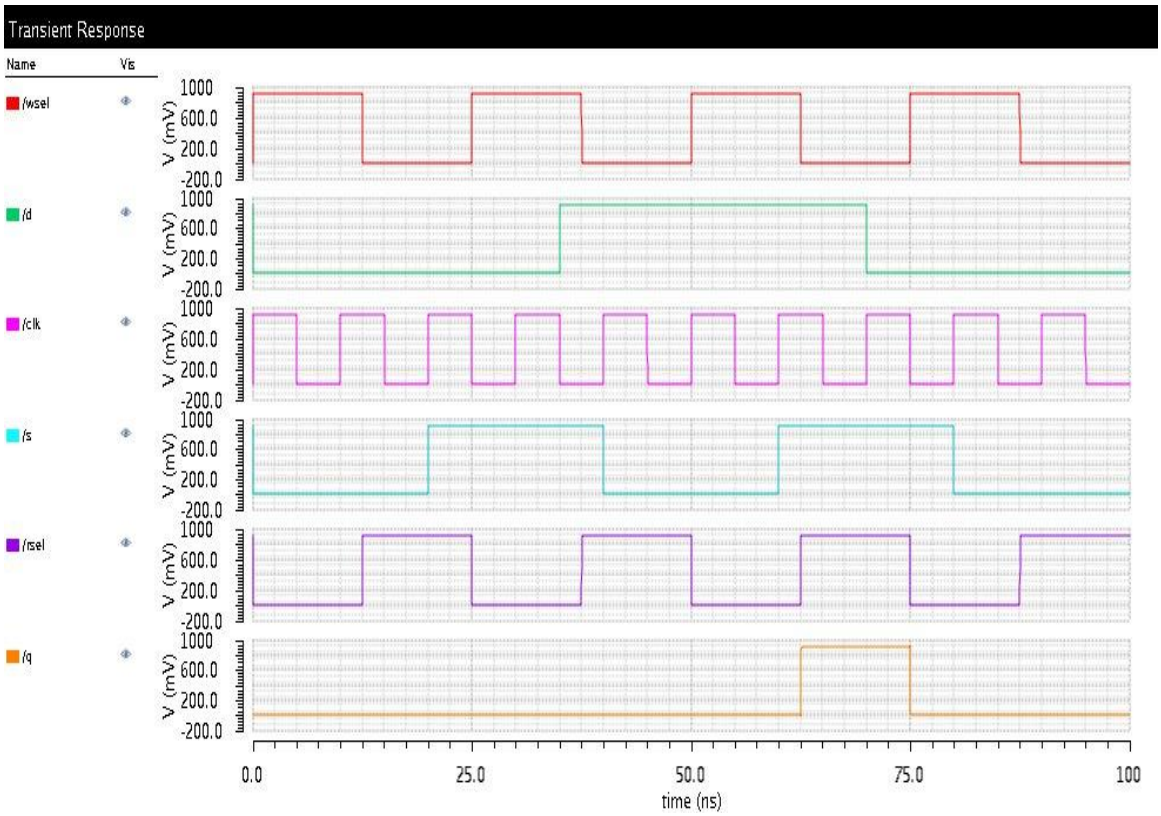


Fig.34. Register Output

1-Bit Register Power:

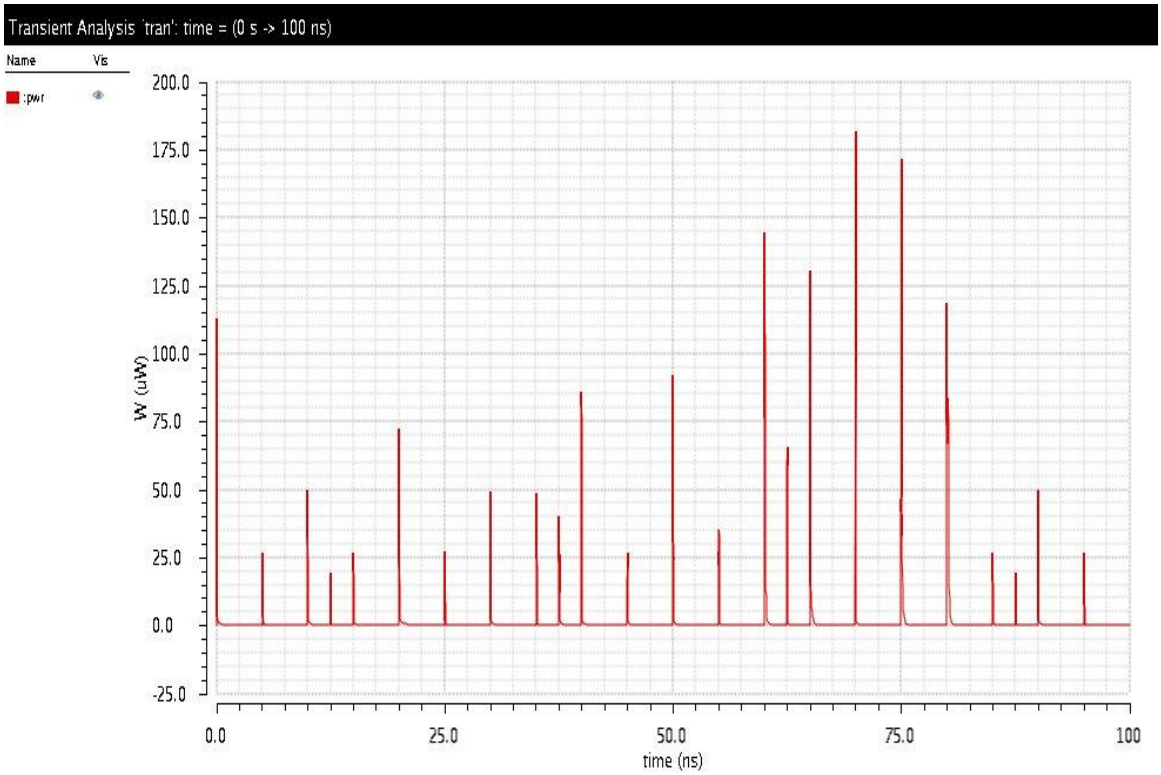


Fig.35. Register Power

1-Bit Adder output:

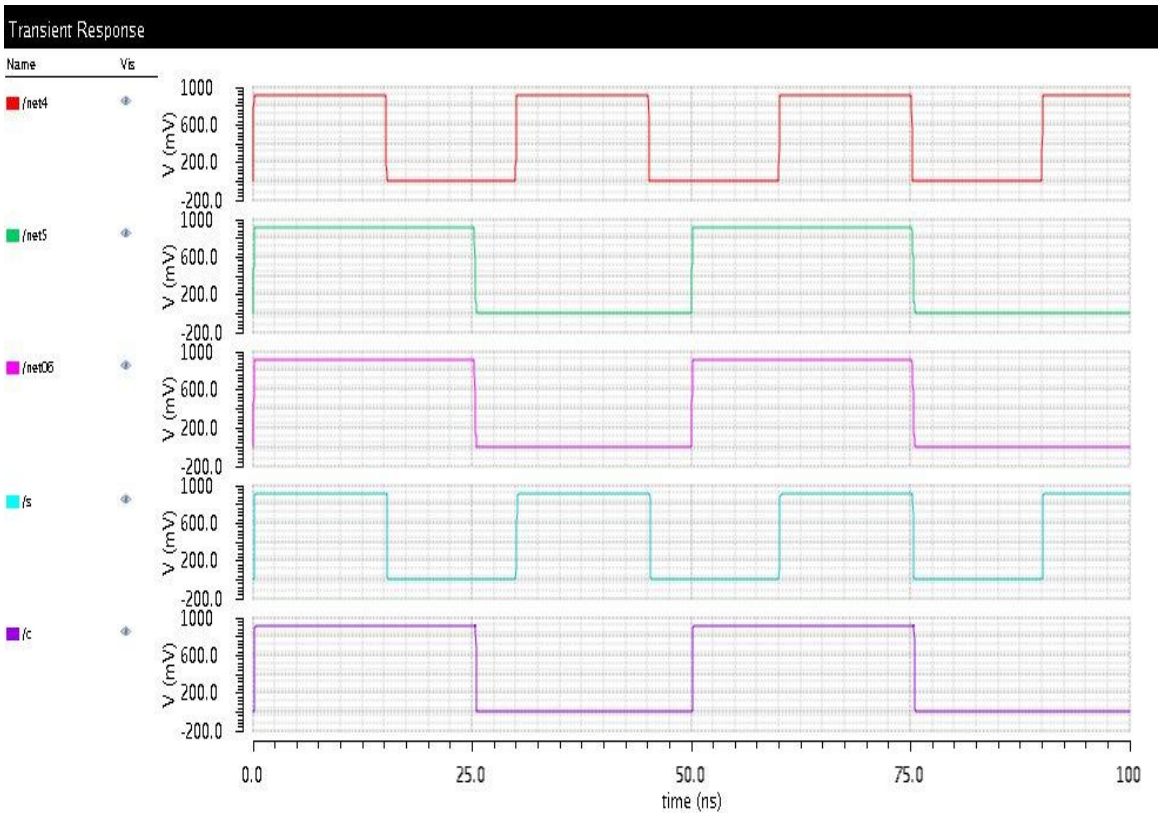


Fig.36. 1-Bit Adder Output

1-Bit Adder power:

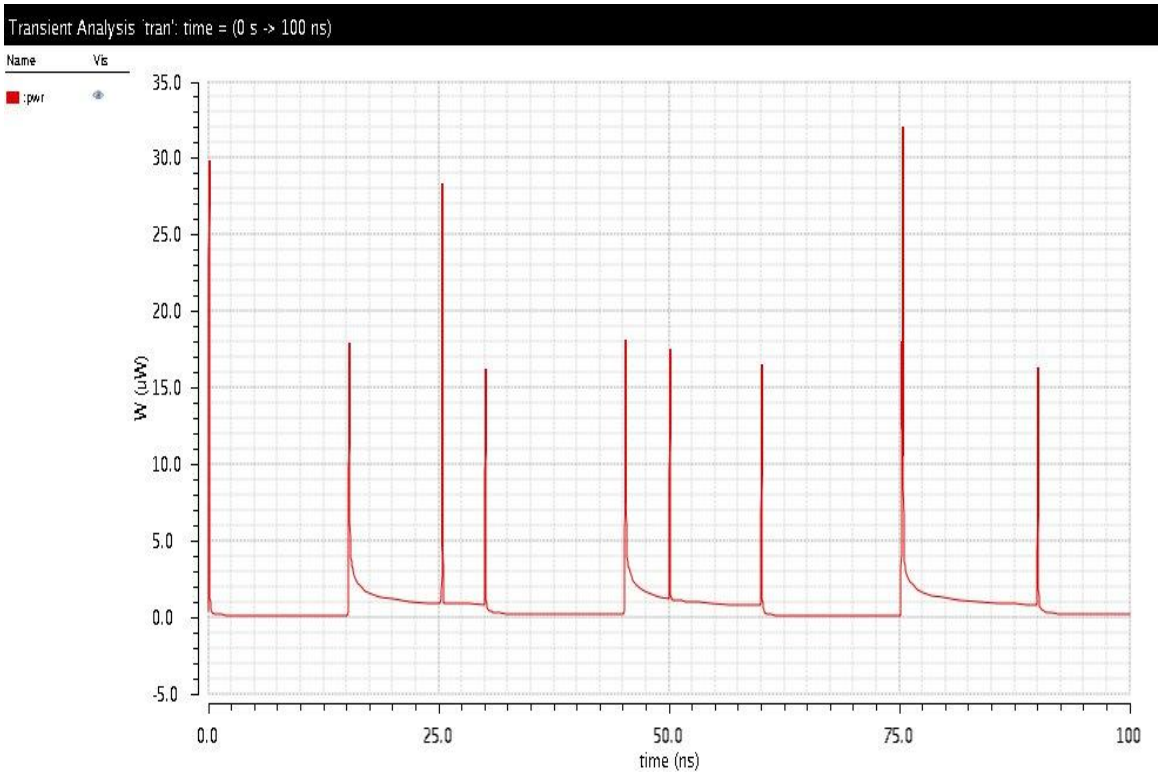


Fig.37.1-Bit Adder Power

4-Bit Multiplier Output:

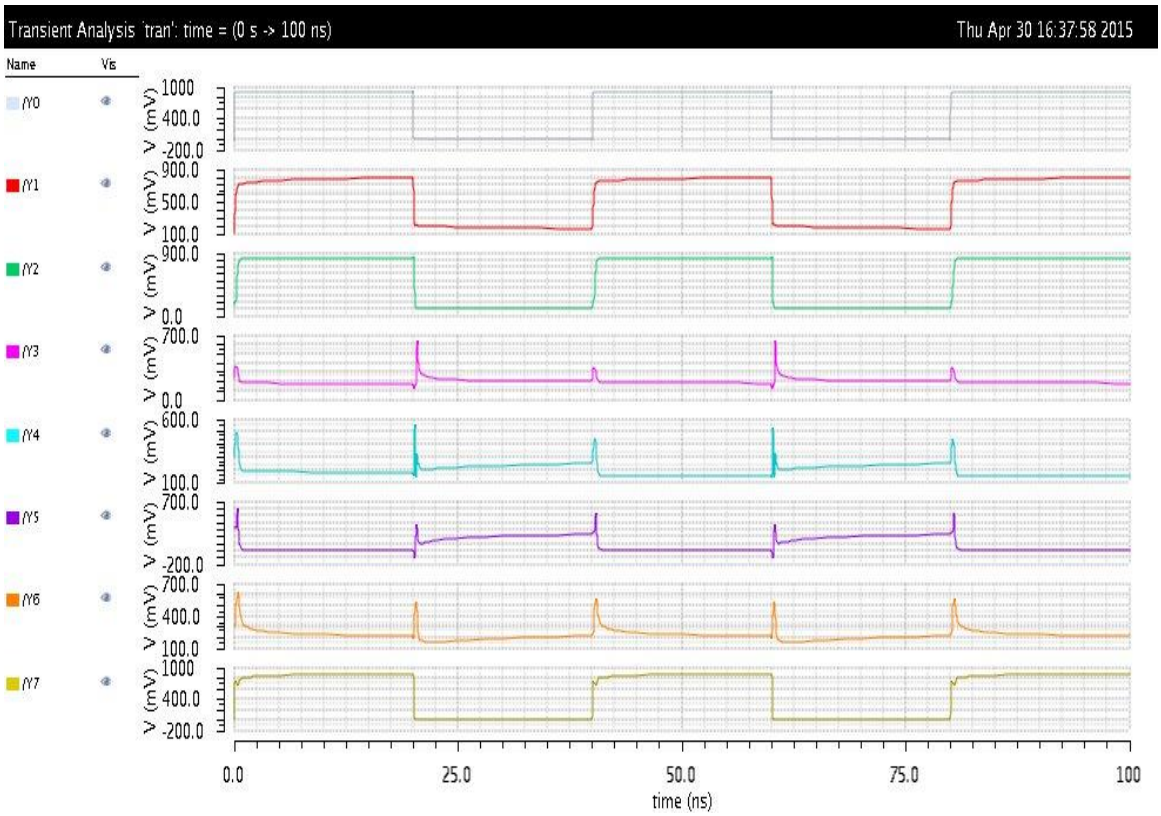


Fig.38. 4-Bit Multiplier Output

4-Bit Multiplier Power:

Fig.39. Multiplier Power

Binary to BCD Output:

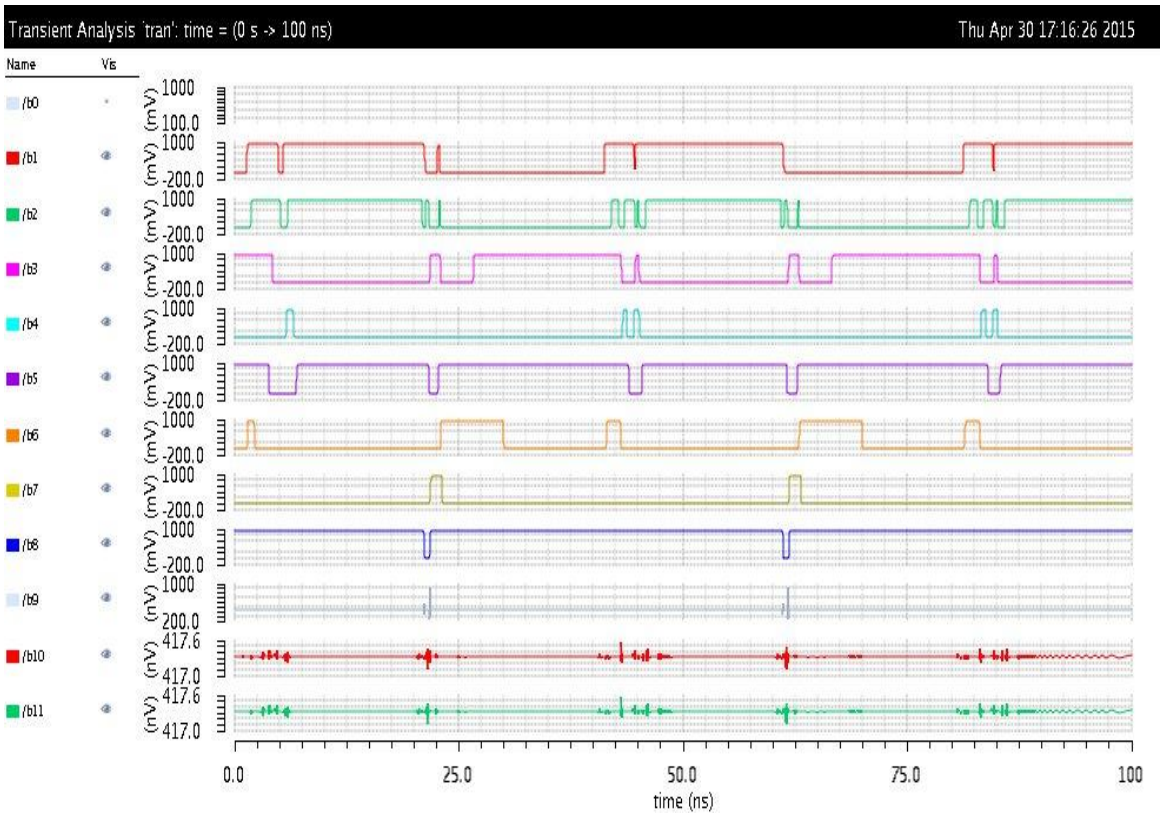


Fig.40. Binary to BCD Output

Binary to BCD Power:

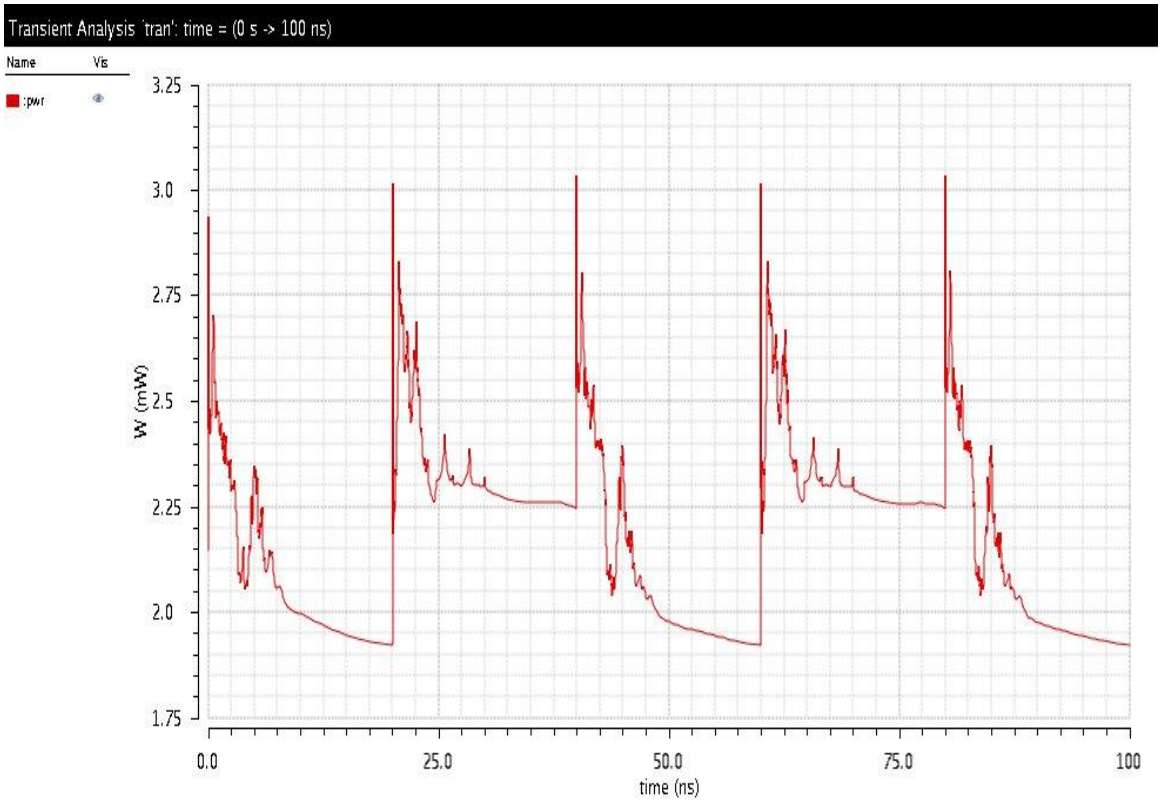


Fig.41. Binary to BCD Power

BCD Output:

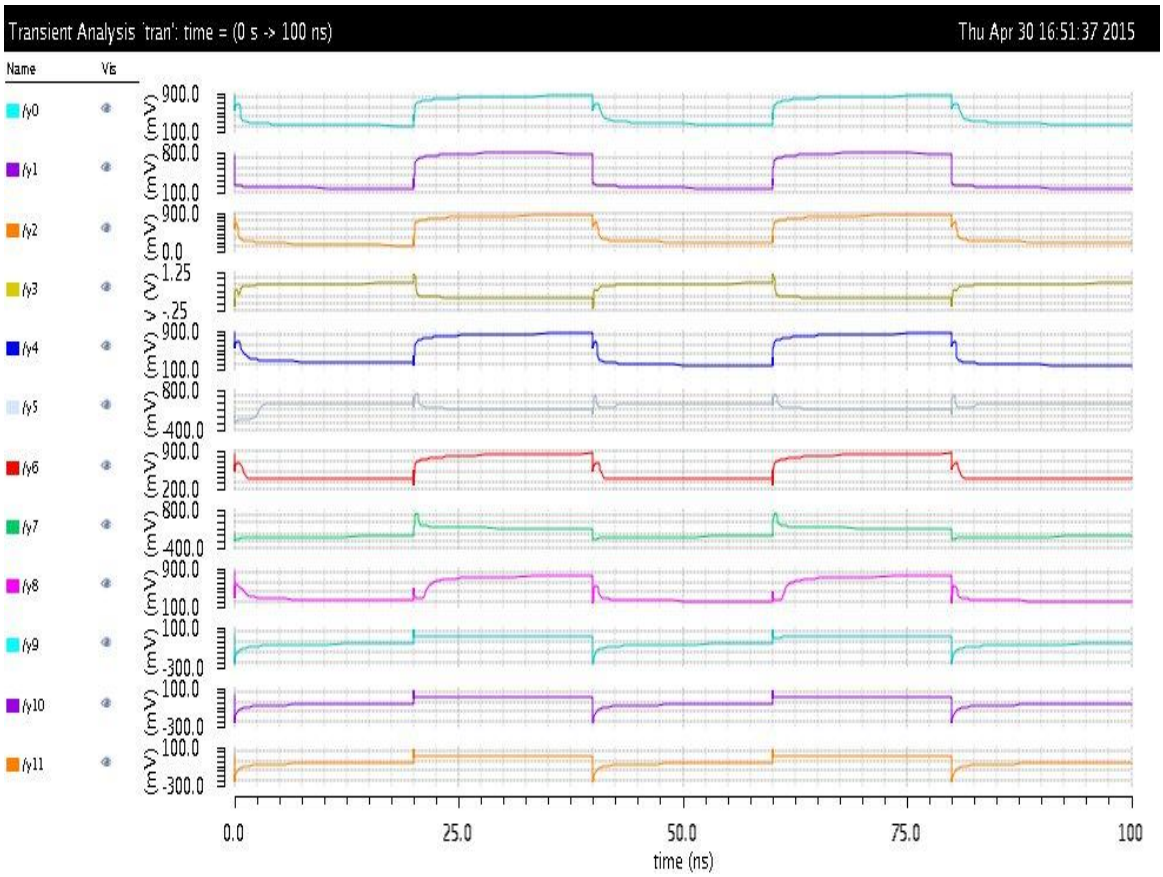


Fig.42. BCD Output

BCD Power:

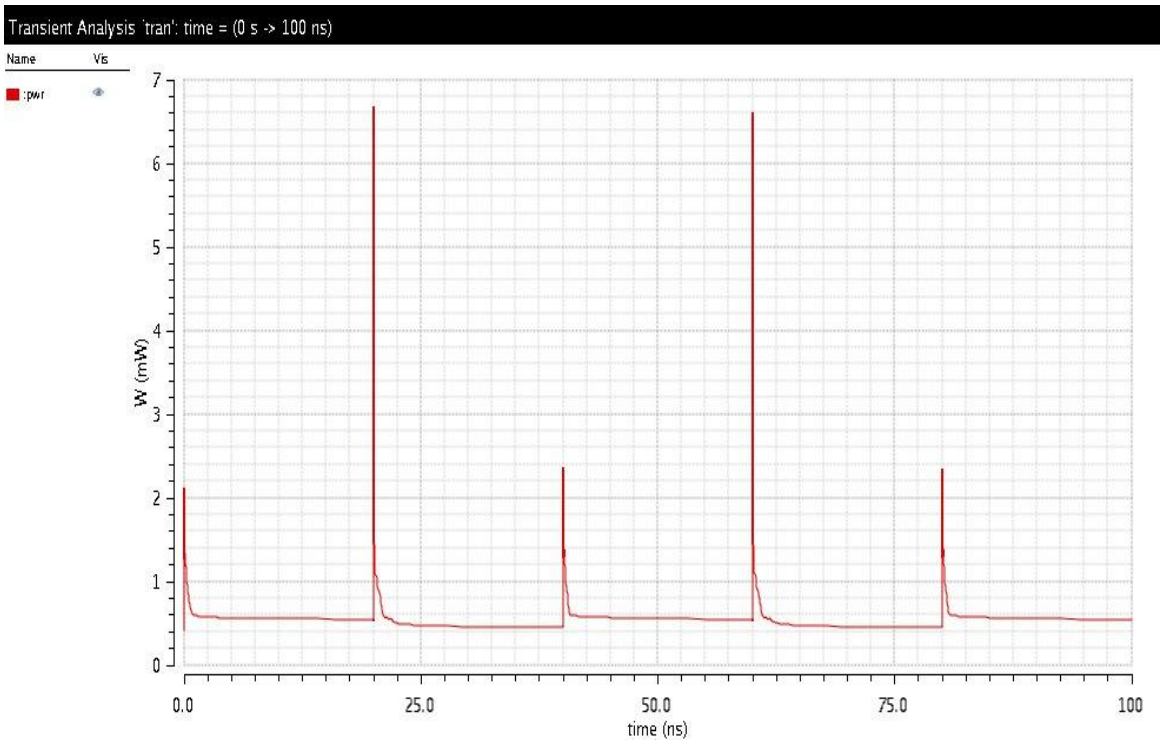


Fig.43. BCD Power

Unsigned MAC Output:

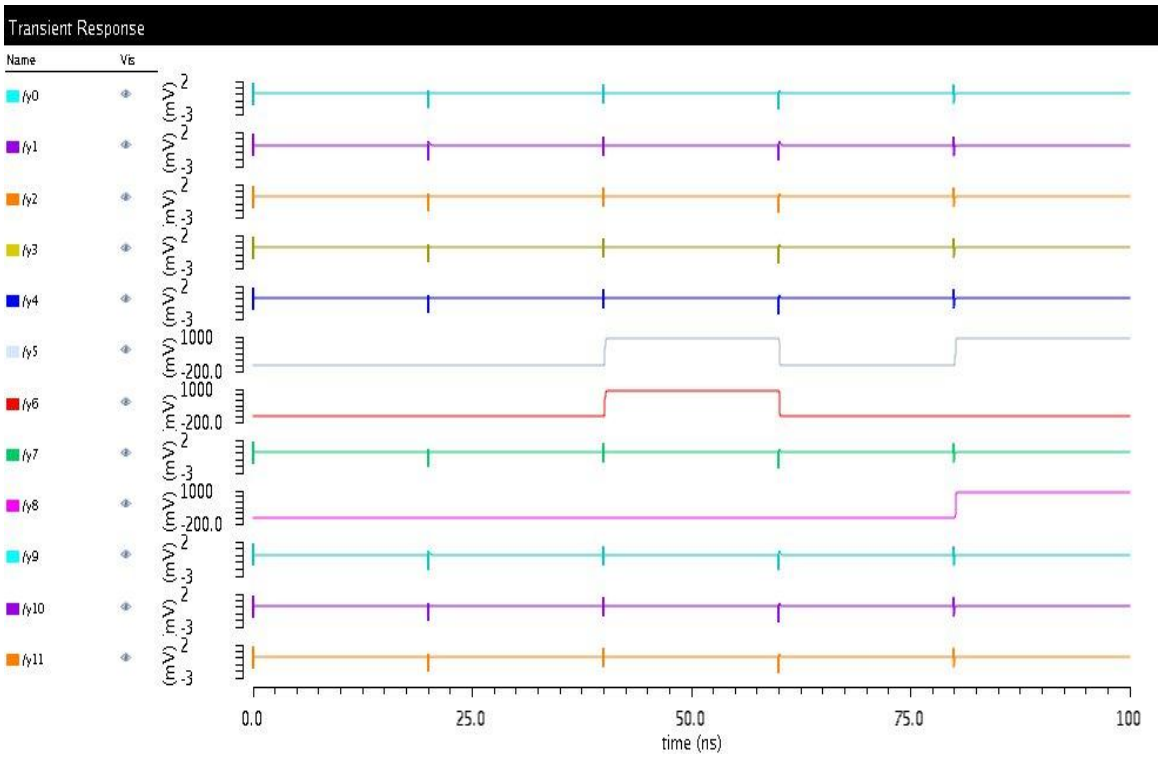


Fig.44. Unsigned MAC Output

Unsigned MAC Power:

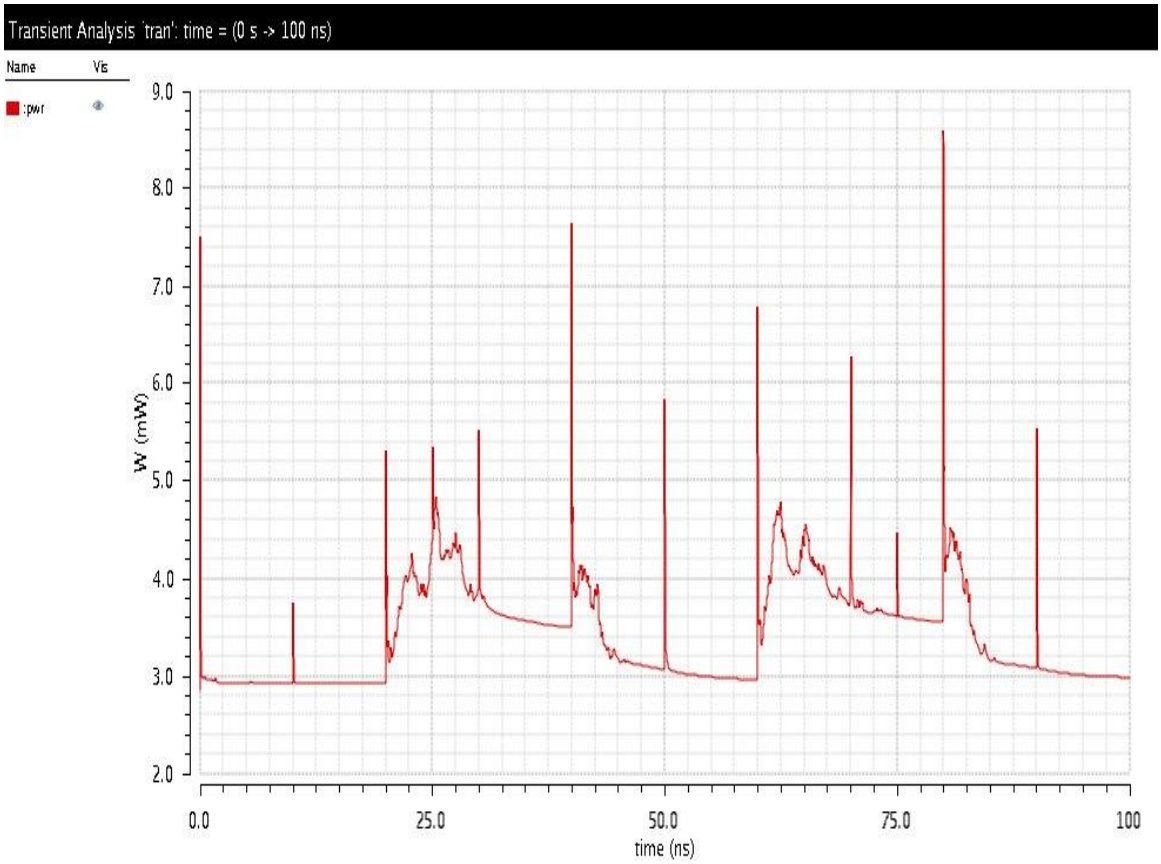


Fig.45. Unsigned MAC Power

Signed MAC Output:

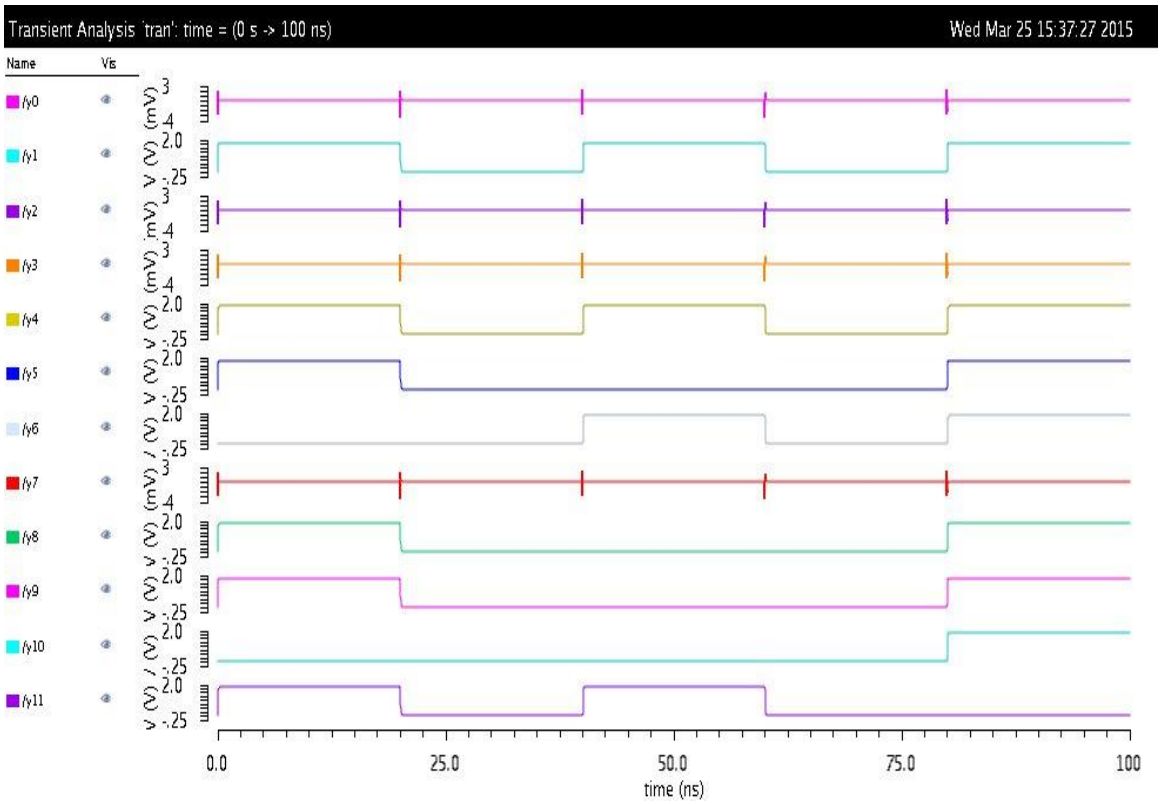


Fig.46. Signed MAC Output

Signed MAC Power:

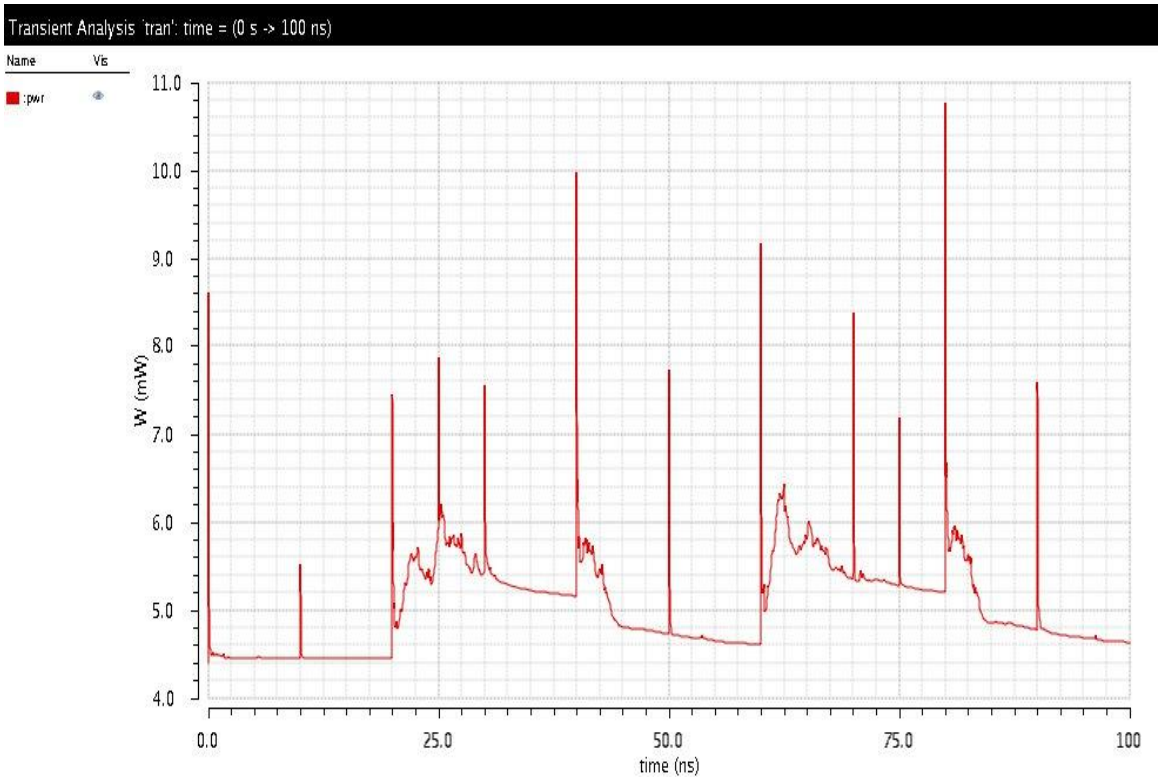


Fig.47. Signed MAC Power

Floating MAC power:

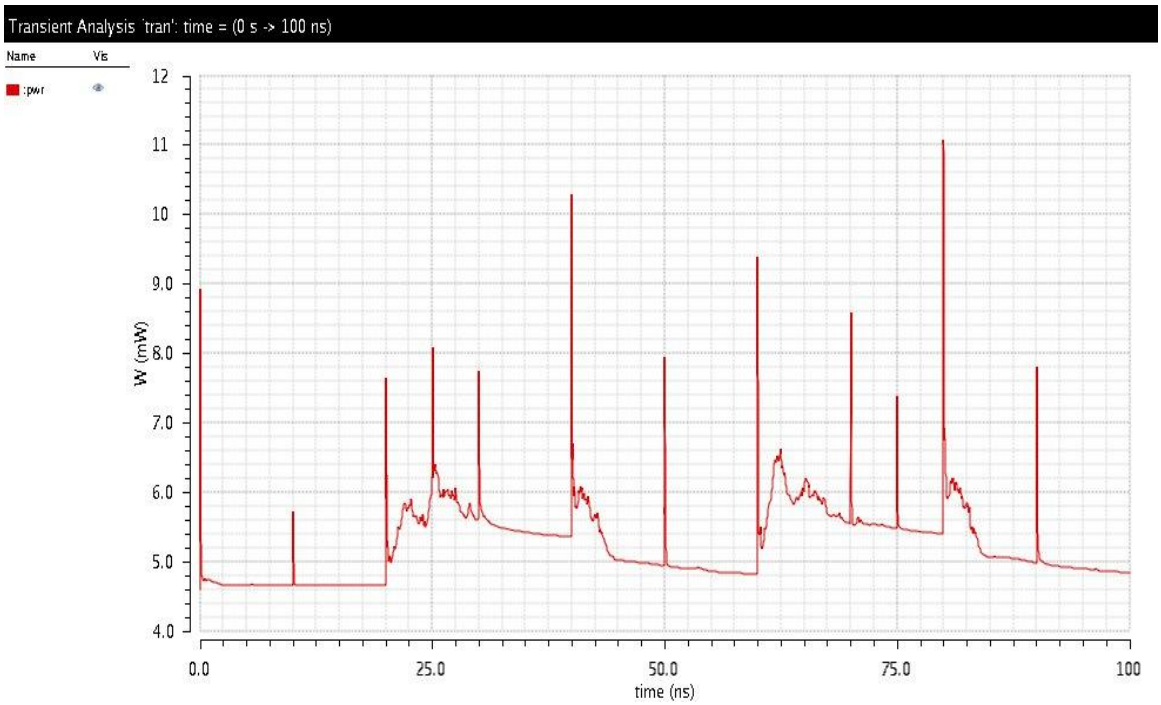


Fig.48. Floating MAC Power

Table 1: Power Analysis

BLOCK	0.9 V	1.2 V	1.8 V
4-Bit Multiplier	**28.58E-6**	**95.1E-6**	**410.6E-6**
8-Bit Register	**7.583E-6**	**16.13E-6**	**181.1E-6**
Binary to BCD	**1.76E-3**	**4.694E-3**	**17.17E-3**
BCD Block	**476.5E-6**	**1.206E-3**	**4.658E-3**
12-Bit Adder	**21.31E-6**	**53.03E-6**	**183.2E-6**
12-Bit Register	**7.11E-6**	**17.13E-6**	**143.6E-6**
Unsigned MAC	**2.661E-3**	**7.004E-3**	**27.42E-3**
Signed MAC	**5.507E-3**	**8.984E-3**	**51.52E-3**
Floating MAC	**5.234E-3**	**13.52E-3**	**53.98E-3**

Table 2: Delay Analysis:

BLOCK	0.9 V	1.2 V	1.8 V
4-Bit Multiplier	**20.90E-9**	**20.12E-9**	**20.13E-9**
8-Bit Register	**20.05E-9**	**20.05E-9**	**20.05E-9**
Binary to BCD	**5.888E-9**	**1.308E-9**	**2.671E-9**
BCD Block	**1.37E-9**	**869.8E-12**	**657.9E-12**
12-Bit Adder	**106.3E-12**	**75.73E-12**	**58.79E-12**
12-Bit Register	**20.06E-9**	**20.05E-9**	**20.05E-9**
Unsigned MAC	**40.1E-9**	**80.13E-9**	**80.1E-9**
Signed MAC	**207.1E-12**	**40.16E-9**	**40.11E-9**
Floating MAC	**40.28E-9**	**80.16E-9**	**80.11E-9**

Table 3: Power-delay Product Analysis:

BLOCK	**0.9 V**	**1.2 V**	**1.8 V**
4-Bit Multiplier	**574.17fs**	**1913fs**	**8265.3fs**
8-Bit Register	**152.03fs**	**323.4fs**	**3631fs**
Binary to BCD	**10.362fs**	**6.13452ps**	**45.86ps**
BCD Block	**652.80fs**	**1048.9fs**	**3064.4fs**
12-Bit Adder	**2265.25as**	**4015.9as**	**10770.3as**
12-Bit Register	**142.62fs**	**343.4fs**	**2879.18fs**
Unsigned MAC	**41.52ps**	**237.9ps**	**1064.5ps**

Signed MAC	**1140.4ps**	**571.87ps**	**2066.46ps**
Floating MAC	**210.82ps**	**1083.7ps**	**4324.33ps**

Table 4: Power Comparision

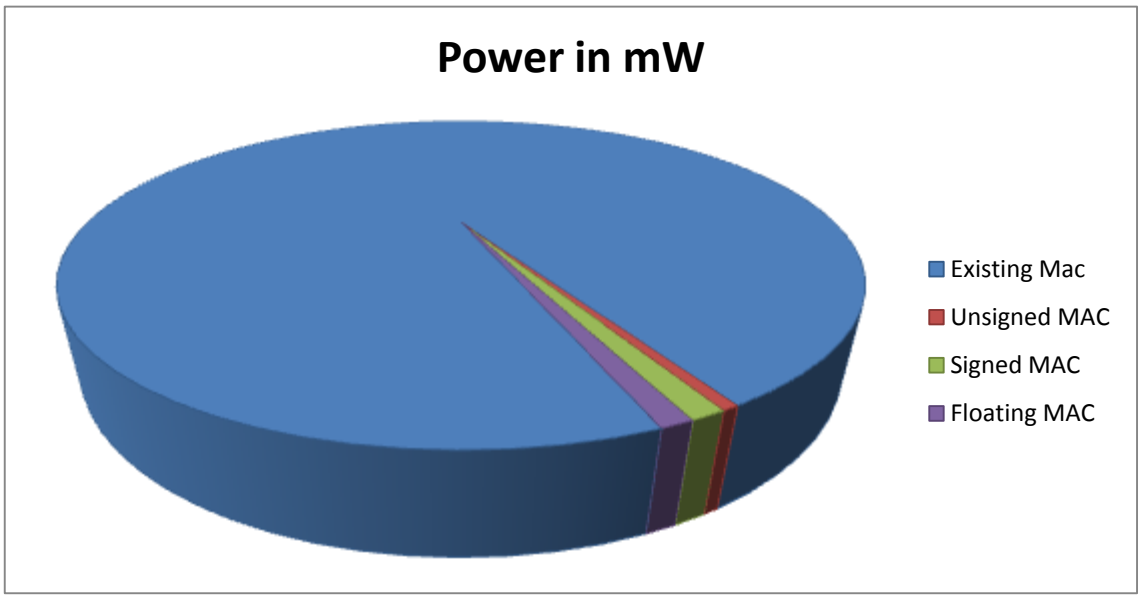
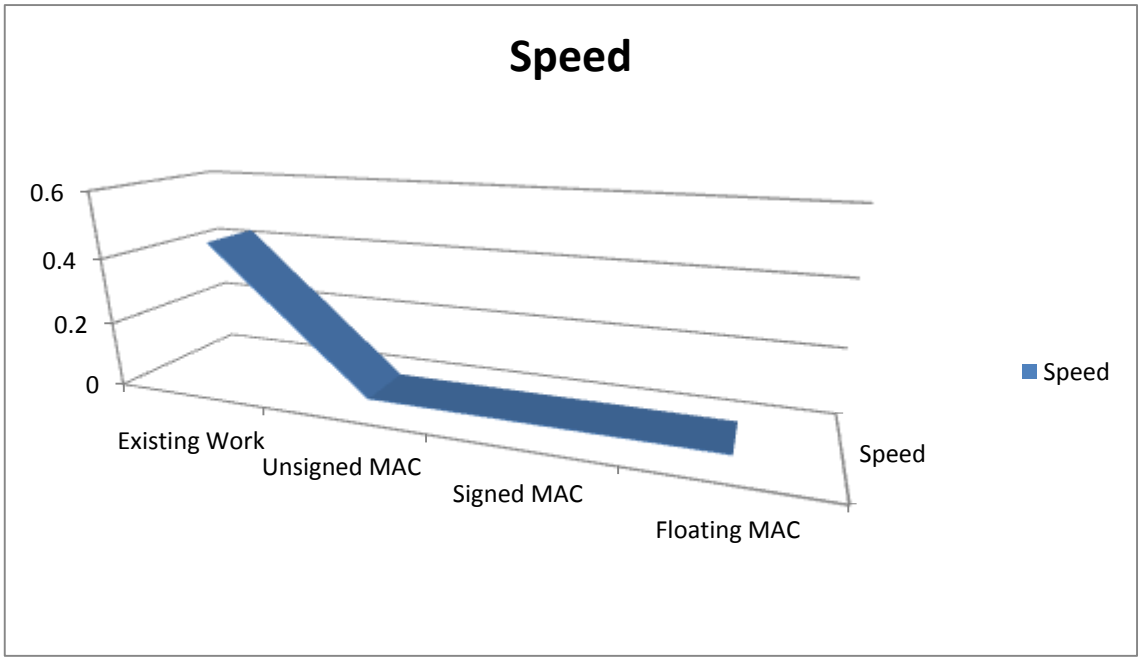


Table 5: Speed Comparision



CHAPTER 8

CONCLUSION AND FUTURE SCOPE

In this study, the novel architectures of the MAC unit for the fixed and floating-point numbers have been proposed. Since, the MAC unit is a high speed system used in the digital processing systems where there is a need for the basic arithmetic operations like addition and multiplication. The invidual blocks of the proposed MAC unit should also be efficient in terms of the parameters like power, speed and PDP. The basic blocks are implemented at the cadence virtuoso 90nm technology library. Due to the scaling of technology the individual blocks are analyzed and designed in order to meets the needs of the basic parameters. The synchronization of individual blocks to form the overall architecture of the MAC unit should be done effectively such that the performance of MAC unit should be efficient. The proposed 9T adder is analyzed through the parametric analysis to vary the "W/L" ratios of the transistors to make the operation of the addition to be efficient.

FUTURE SCOPE:

At present the work is mainly focused on the synchronization of the individual blocks to design an overall MAC unit and to achieve low power and high speed. The future scope can be of synchronizing the whole MAC unit to work in a single clock cycle where the basic operations like addition, multiplication and storing of data can be done at a single clock pulse. The make the layout's of the proposed architectures to determine the area.

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