2015 International Conference on Smart Technologies and Management for Computing, Communication, Controls, Energy and Materials (ICSTM), Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology, Chennai, T.N., India. 6 - 8 May 2015. pp.411-417.

A Novel Low Power and High Speed Multiply-Accumulate (MAC) Unit Design for Floating-Point Numbers

N. Jithendra Babu[1] and **Rajkumar Sarma**[2]

School of Electronics Engineering, Lovely Professional University, Punjab, India
Email: [1]Jithendra.lpu@gmail.com, [2]Rajkumar.sarma86@gmail.com

***Abstract*— At the present days, the low power designs are playing a vital role in every designs. Due to the existence of the battery designs in the integrated circuits the low power designs play a major role of operations in any circuit. In this paper our work is on a low power and high speed Multiply-accumulate unit that is the basic block in digital processing systems. Since, the basic blocks of MAC unit are multiplier, adder and accumulator. The design of these blocks should be efficient in terms of the power and speed. So our work is based on the BCD multiplication and addition and also to find the floating point numbers. Our implementation consists of multiplier, register, binary to BCD converter; Adder and BCD block which make the overall output of the MAC to be in the BCD format. First the individual blocks are designed and analyzed and the overall MAC is implemented in Cadence 0.9µm technology and power and delay analysis is done using the cadence spectre**

***Keywords*— Binary to BCD converter, Floating point, Wallace tree multiplier.**

I. INTRODUCTION

Due to the rapid development of systems in the very near generations, low power designs are the major considerations while designing the integrated circuits. In any of the digital or signal processing systems the main functions are multiplications and additions. MAC is the basic block which performs those operations and so it is considered as a basic unit in the processing units. The MAC unit consists of multiplier, adder and accumulator such that which is to be high speed and should consume less power. The performance of the MAC can be increased by optimizing the basic blocks that are used in the design of the overall MAC unit. Our proposed work depends on the high speed and low power dissipation which is also used to find the floating point numbers. Floating point numbers are nothing but the exponent terms of the input patterns. There are two types of arithmetic operations that play a major role in the addition of bits or in multiplication. They are floating and fixed point operations. Our proposed work is on the floating point MAC unit. Since, fixed point numbers for large arithmetic numbers is not efficient. So the invention of floating point was necessary where the real numbers are represented as floating point number with mantissa and exponent. It is represented as

$Y = M \times B^E$ where M is mantissa, B is base and E is exponent. The overall MAC is designed using the individual blocks and analyzed to be efficient with speed and low power dissipation. The function of the MAC unit is termed as

$$f = \sum_{i=0}^{N-1} a_i b_i$$

at the next levels the paper is divided into the following sections. Section II describes the MAC unit. Section III describes the individual blocks of the overall MAC unit. Section IV describes the proposed MAC unit for the floating point numbers. Section V describes the experimental work and section VI describes the results and analysis.

II. MAC UNIT

The digital signal processing elements mainly deals with the multiplications and additions. These arithmetic operations plays the important role in the processing of the signal processing systems, so it is the basic building block for any of the digital signal processing systems. So our proposed work is on the Multiply-Accumulate unit which is the basic block in any of the signal processing systems which multiplies the two values and adds the multiply output value with the previously accumulated value that is stored in the register. For this, MAC architecture is to be designed according to the functions of the different blocks to produce high speed throughout the system for an efficient processing. The basic building block of the MAC unit is represented in the fig.1 [1]. According to the figure an N-

input bits of two patterns are fetched from the storage location and given as input to the multiplier block which performs the multiplication and produces the 2N bit output as input to the resister block which stores the data and sends the data to next level as input to the to the adder. This adder performs the adding operation by adding the output from the register block with the previously accumulated value that is stored in the accumulator.

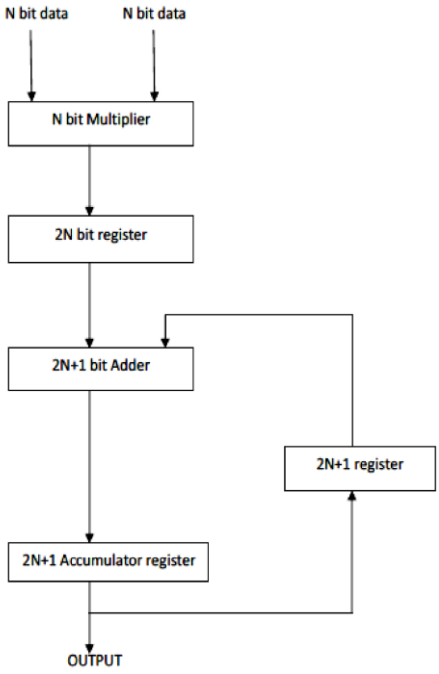

Fig. 1. Basic MAC Unit [1]

Thus, the output from the adder is given to the accumulator register and the overall output is taken from the output of the accumulator register which is stored in the feedback register for next consecutive steps. In the existing architecture the adder can be of different types such as ripple carry adder, carry look adder, carry select adder. In our proposed work our adder architecture for 12 bit is a simple ripple carry architecture which achieves high transition speed compare to other architectures. The architecture of the MAC unit consists of an N bit multiplier, 2N bit register, 2N bit adder and 2N+1 bit accumulator register of two sets one for storing the output value and the second is for reading the output value at the present state.

III. BASIC BLOCKS IN OUR DESIGN

A. Adder

As we know that adder is used basically for arithmetic operations in any of the digital circuits. In our proposed work adder is the basic concern because it is used in almost all of the individual blocks in the overall MAC unit. The basic arithmetic operations such as add, sub, multi and divide are implemented using adder as a basic building block [3]. Our proposed work is on low power designs due to this the design of a full-adder with low power dissipation and high speed is necessary. The adder circuit is the basic block in our research work that adds the current output value from the multiplier block with the previously accumulated value that is stored in the accumulator register. The adder we are using in our designs is of 9 transistors that provides better efficiency and low power dissipation throughout the MAC architecture by varying W/L values. The modification of the W/L values in the adder circuit is done because the proposed architecture is scaled down to design in 90 nm technology. This adder structure is used to design our multiplier block, binary to BCD converter and BCD block.

B. Wallace Tree Multiplier

Majority applications of the digital processing systems are multiplications. One needs to consider that while designing a multiplier; it should be of high speed and low power. Our proposed work is on low power such that the multiplier block should be efficient with the low power designs and the second aspect is speed. Due to this we have implemented the multiplier architecture which is known as Wallace tree multiplier [2] based on Wallace tree algorithm.

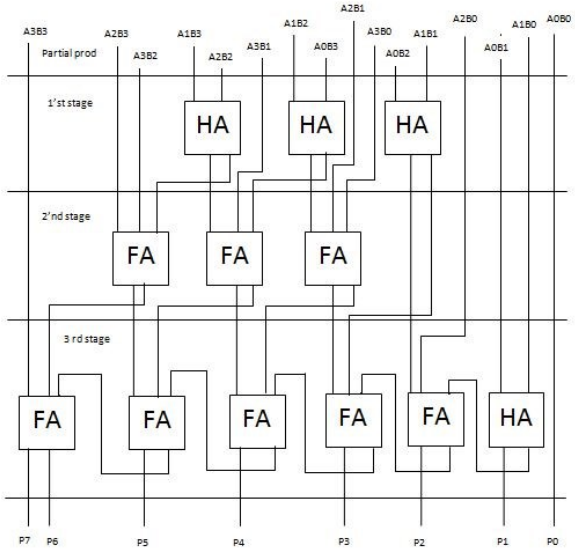

Fig. 2. Wallace Tree Multiplier

The block diagram is shown in Fig.2. The Wallace tree algorithm architecture for a 4-Bit is:

- At the first step, AND gates are used to multiply the partial products.

- At the second step, the partial products are added by using the half adder.
- At the last step, a simple ripple carry architecture using the full adders are used to produce final result by adding.

C. Binary to BCD

Since, the output from the multiplier block will be in the binary format. The proposed design is to convert the output of the multiplier block into the binary coded decimal format. The proposed design is designed using the basic logic gates AND, XNOR and the combinational block full adders. The output from the XNOR block passes through the AND gate which then passes the BCD value as an output whenever the output of XNOR is one and then the output from the AND gate is added by shifting the output values using the full adders.

D. BCD Block

The term BCD represents the binary coded decimal system. Our proposed work is on the BCD logic where we are multiplying the two values and then adding it with previously accumulated values. So, there is a need for the BCD circuit to maintain the overall MAC unit to be in the BCD format. Here we have proposed the BCD block which maintains the overall output of the MAC unit to be in the Binary Coded Decimal format. The BCD block is designed using three 2:1 MUX, two 4:1 MUX etc. The BCD block is proposed at two levels in our design and also in the binary to BCD converter. The block diagram of BCD logic is shown in Fig.3. The proposed design works according to the following combinations: If the input patterns i3 and i7 for BCD block are 0s then it is bypassed to the output of the BCD block directly. If the i3 bit is 1 and i7 bit is 0 then input is converted by adding 0110 to the LSB at the first stage and OR with 1001 to the input LSB bit and considering it as a select line and adding 0110 to MSB bit at the second stage from the output of MUX block and passed to the output depending on the select line (D[7] AND D[6]) OR (D[7] AND D[5]). If the i3 bit is 0 and i7 bit is 1 then input is converted by adding 0110 to the MSB bit and OR with 1001 to the input MSB bit and using it as select line to MUX block and passing the output. If the i3 and i7 bit is 1 then we are checking for all the combinations that are explained in the above steps by using a 4:1 MUX as first three inputs and last input will be by adding 01100110 to the input at the first stage and OR with 10011001 to the input and using it as a select line to pass the output.

E. Sleepy Stack Inverter

The sleepy stack is a combination of low Vth and high Vth transistors. The purpose of the sleepy stack inverter technique in our design is to eliminate the leakage currents during the operation of the MAC unit. This technique is a combination of two techniques forced stack technique and the other is sleep transistor technique [4].The block diagram is shown in Fig.4. This technique works in the following modes of operation:

1. *Active mode*— During this mode of operation the sleep transistors S and Sbar are turned on such that to make the transistor operation to be very fast.
2. *Sleep mode*— During this mode of operation the sleep transistors are turned off such that this arrangement makes the overall circuit to retain in the exact logic state and to eliminate the leakage effects.

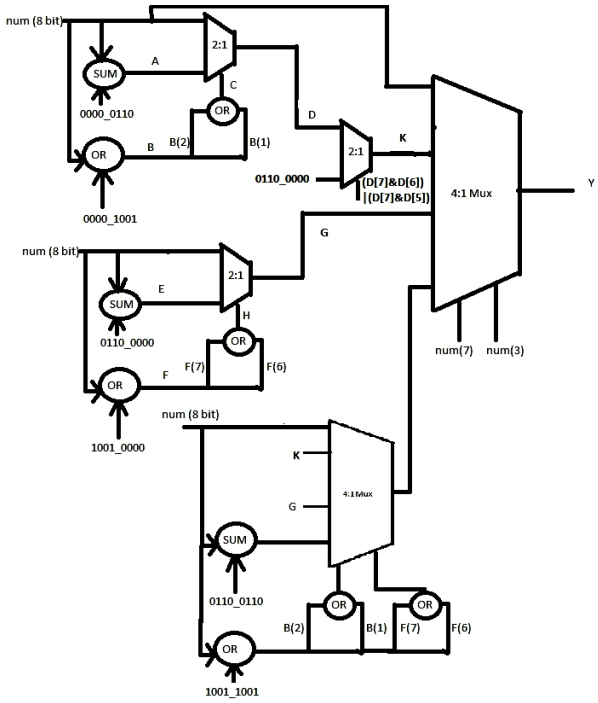

Fig. 3. Proposed BCD Block

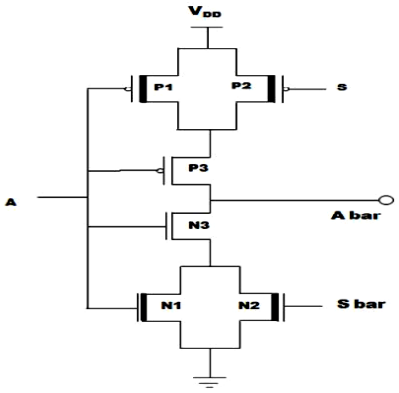

Fig. 4. Sleepy Stack Inverter

F. D-Flip Flop

In our proposed design the usage of d-flip flop is to store the output values that are used to add at the next consecutive level. The flip flop is of technique which has high switching

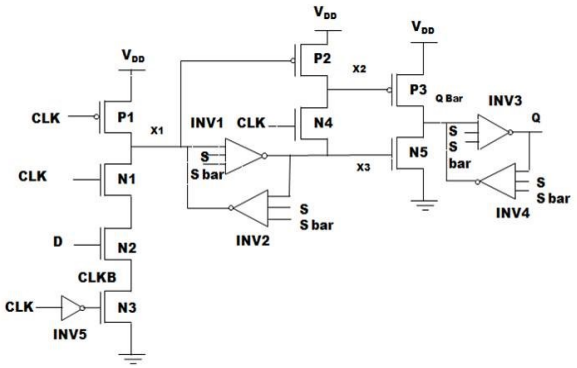

Fig. 5. D- Flip Flop

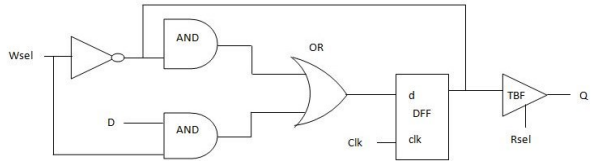

Fig. 6. 1- Bit Register

speed, less power dissipation and low leakage currents through the register unit [5]. Our design is implemented using a conventional dual dynamic flip flop which ensures that there is a high switching speed throughout the circuit [6]. The function of d flip flop is that the output follows the input whenever the clock pulse is active. By this it clearly makes that the flip flop designed here is a positive edge triggered hybrid node flip flop [5].The block diagram is shown in Fig.5.

G. Accumulator Register

In our proposed work the accumulator is used to store the output values from the multiplier block which is an 8-bit and the overall MAC unit which is of 12-bit used for the successive addition of the previous consecuted values with the adder circuit. The register block functions with the clock synchronization. The register will writes the data whenever Wsel is 1, if Rsel signal is 1, then the flip flop will read the value that is used as a input for next consecutive levels. The block diagram is shown in Fig.6.

IV. Proposed MAC Architecture for Floating Point Numbers

Our proposed MAC design for the floating point number is designed using the proposed MAC unit for fixed point numbers represented in Fig.7. Here in the fixed point architecture a simple MAC unit with an additional binary to BCD and BCD block is added to maintain the overall output of the MAC unit to be in the BCD format. As the same technique is used to design the floating point architecture with necessary modifications where there is a parallel analysis of the mantissa and the exponent term. The mantissa part is implemented by giving the mantissa bits as inputs to the multiplier block where there will be XOR of sign bits parallel to the multiplier and the output from the XOR will passed to the MUX that discharges the signal from the BCD block to find whether the output from the BCD block is signed or unsigned. The multiplier multiplies the mantissa bits and passes to the register block. There is a need for binary to BCD converter because the output from the multiplier will be in the binary format and it passes the output to the BCD block. The BCD block maintains the product term to be in the BCD format and passes the value to the MUX depending on the sign bit which acts as a select line. The feedback from the register is also passed through the MUX depending on the upper MSB of the feedback input and the outputs from the MUX blocks are passed to the adder to add. Once again there is a need for the MUX which again generates a unsigned output and passes the value to the BCD block. Here again the BCD block maintains the overall output to be in the BCD format and the output is stored in the feedback register for the next addition and the output is read through the consecutive register at the last. The exponent terms are parallel added with the full adders and are bypassed through the BCD

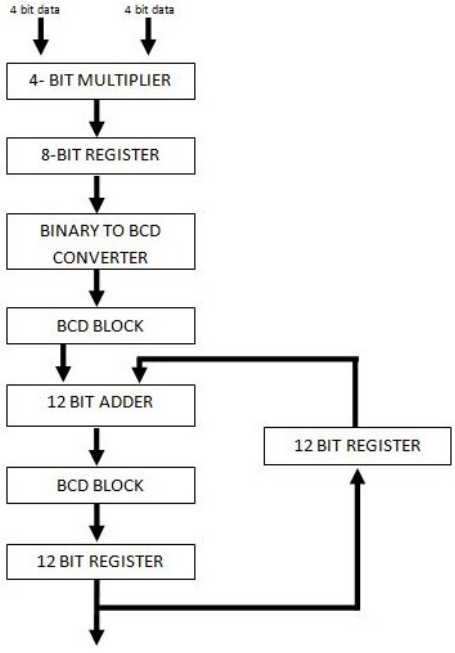

Fig. 7. Proposed MAC Architecture

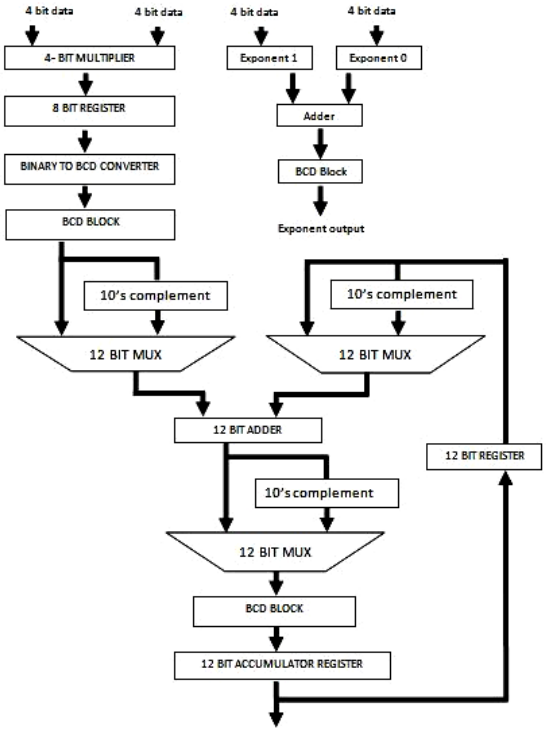

Fig. 8. Proposed Floating Point Architecture

block if necessary and read at the output through bypassing. The proposed MAC unit for Fixed and Floating point numbers is represented by Fig.7 and Fig.8 respectively.

V. EXPERIMENTAL WORK

The proposed MAC units for the fixed point and floating point are implemented successfully in the cadence virtuoso 90 nm technology. First the invidual blocks that are the key parts of the mac unit has been designed at the cadence virtuoso and the performance has been verified by considering the parameters power and delay. Finally the basic blocks are interconnected together to form the overall MAC unit both for the fixed point and floating point. During the implementation of the basic blocks there is a need for the analysis of the W/L values, because the technology is scaled down. The adder design which is the basic block in our work is designed by analyzing the widths of the transistors. The MUX blocks which are used in the design of BCD block is implemented by the pass transistor logic. Since, our proposed work is on the low power and high speed MAC the invidual block should also be high speed and low power. During the design of such type of circuits there will be large leakage currents this is removed using the sleep transistors. MAC unit is designed at the cadence virtuoso 90 nm technology and the following considerations are done. The overall time period of our proposed design is to be considered at 100ns and our input bits are considered to be varied from the 40ns to 20ns and the clock gating for the register unit is taken as a positive edge clock. The Wsel and Rsel of the register unit are inverting and varying with the time response of the input bits. The working of MAC unit is as follows the multiplier multiplies the two sets of 4-bit values with sign numbers and produces the output as an input to the register block during the time response of 20ns. In the register unit during the positive edge clock Wsel is to taken as 1 which writes the input data to my register block at 0 to 20ns. After the completion of writing the data into the register block Wsel is disabled and Rsel is enabled which reads the data at 21ns to 40ns and passes the output to the binary to BCD block. The binary to BCD block converts the multiplier output to the BCD format and passes it to the BCD block. The BCD block maintains the exact BCD logic and passes the value to the adder by means of a MUX. The BCD output is 10's complimented and passed to the adder circuit depending on the sign bit which acts as a select line. The adder circuit adds the current input with the previously accumulated value that is stored in the register and sends to the BCD block. Here again there is a possibility of the sign numbers through the feedback path. This is also rectified by using the 10's compliment logic and added with the current input value whether it is normal one or 10's complemented one. Here again the BCD block maintains the input to be in BCD value in the same time response and passes to the 12- bit accumulator register which reads the data from 41ns to 60ns which is the overall output of our fixed point Mac unit. The

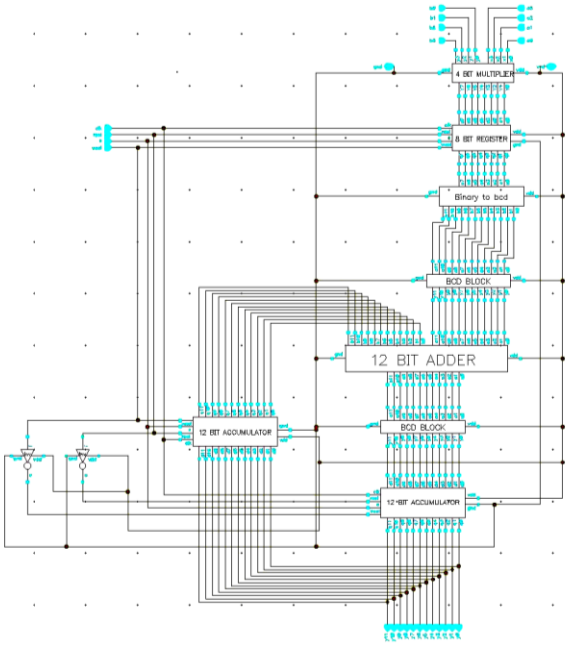

Fig. 9. Proposed MAC for Fixed Point Unsigned Number

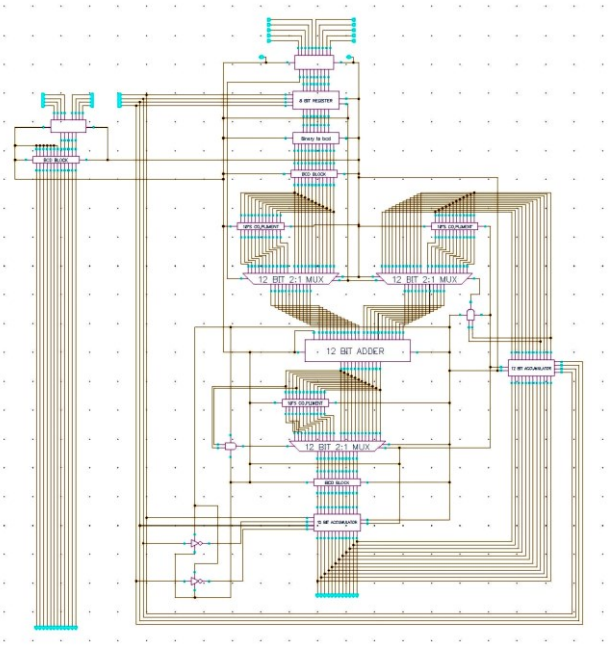

Fig. 10. Proposed MAC for Floating Point Number

performance analysis and the power, delay and power delay product are analyzed using the cadence spectre tool at the different supply voltages.

VI. Results and Analysis

The Mac unit for the fixed point and floating point numbers are designed at cadence virtuoso and the performance of the proposed architectures are analyzed using the cadence spectre tool and determined the power, delay and power delay product using the spectre stimulator of each individual block and the overall Mac unit. The Mac unit is stimulated at a supply voltage of 0.9V, 1.2V, 1.8V and power, delay are calculated at the three different supply voltages.

Table I. At 0.9 V

Block	*At 0.9 V*		
	Power	*Delay*	*PDP*
4-Bit Multiplier	28.58E-6	20.09E-9	574.17fs
8 Bit register	7.583E-6	20.05E-9	152.03fs
Binary to BCD	1.76E-3	5.888E-9	10.362fs
BCD	476.5E-6	1.37E-9	652.80fs
Adder	21.31E-3	6 106.3E-12	2265.25as
12 Bit register	7.11E-6	20.06E-9	142.62fs
Fixed MAC	3.408E-3	40.2E-9	136.68ps
Floating MAC	5.234E-3	40.28E-9	210.4ps

Table II. At 1.2 V

Block	*At 1.2 V*		
	Power	*Delay*	*PDP*
4-Bit Multiplier	95.1E-6	20.12E-9	1913fs
8 Bit register	16.13E-6	20.05E-9	323.4fs
Binary to BCD	4.694E-3	1.308E-9	6.13452ps
BCD	1.206E-3	869.8E-12	1048.9fs
Adder	53.03E-6	75.73E-12	4015.9as
12 Bit register	17.13E-6	20.05E-9	343.4fs
Fixed MAC	9.19E-3	80.13E-9	736.39ps
Floating MAC	13.52E-3	80.16E-9	1083.76ps

Table III. At 1.8 V

Block	*At 1.8 V*		
	Power	*Delay*	*PDP*
4-Bit Multiplier	410.6E-6	20.13E-9	8265.3fs
8 Bit register	181.1E-6	20.05E-9	3631fs
Binary to BCD	17.17E-3	2.671E-9	45.86ps
BCD	4.658E-3	657.9E-12	3064.4fs
Adder	183.2E-6	58.79E-12	10770.3as
12 Bit register	143.6E-6	20.05E-9	2879.18fs
Fixed MAC	13.29E-3	80.1E-9	1064.5ps
Floating MAC	53.98E-3	80.11E-9	4324.33ps

VII. Conclusion

The proposed MAC architectures for the fixed point signed and floating point numbers are designed at the cadence 90nm technology. Due to the scale down of the technology there is a need for the individual analysis of each block. The different blocks of mac were designed and analyzed to determine the power and delay. The power, delay and power-delay products are calculated using the cadence spectre for fixed point and floating point number architecture. As that the floating point architecture is meant for both the exponent and mantissa part which resembles the huge waveforms on the paper. So the output waveforms are unable to produce but the power, delay and PDP are analyzed using the output waveforms.

References

[1] Shanthala S, Kulkarni. S.Y.,"VLSI Design and Implementation of Low Power MAC Unit with Block Enabling Technique," European Journal of Scientific Research ISSN 1450-216X

[2] Shanthala S, Cyril Prasanna Raj, Dr.S.Y.Kulkarni, "Design and VLST Implementation of Pipelined Multiply Accumulate Unit," IEEE International Conference on Emerging Trends in Engineering and Technology, ICETET-09

[3] Shivshankar Mishra et al.," On the Design of High-Performance CMOS 1-Bit Full Adder Circuits," International Conference on VLSI, Communication & Instrumentation (ICVCI) 2011

[4] Jun Cheol Park and Vincent J. Mooney III, "Sleepy Stack Leakage Reduction," IEEE transactions on very large scale integration (vlsi) systems, vol. 14, no. 11, November 2006

[5] Helga Evangelene, "A Novel Low Power Hybrid Flipflop Using Sleepy Stack Inverter Pair," Science and Information Conference 2014 August 27-29, 2014 | London, UK

[6] Kalarikkal Absel, Lijo Manuel and Kavitha.R.K. "Low power Dual Dynamic Node Pulsed Hybrid Flipflop Featuring Efficient Embedded Logic," IEEE transactions on very large scale integration (vlsi) systems, vol. 21, no. 9, September 2013

[7] Abdelgawad.A, Madgy Bayoumi, "High Speed and Area Efficient MAC unit for Digital Signal Processing Applications," 1-4244-0921-7/07 $25.00 © 2007 IEEE.

[8] Ashish B.kharate, Prof P.R.Grumble, "VLSI Design and Implementation of Low Power Mac for Digital FIR filter," International Journal of Electronics Communication and Computer Engineering Volume 4, Issue (2) REACT-2013, ISSN 2249–071X.

[9] Avisek sen, Partha Mitra, Debarshi data, "Low Power Mac Unit for DSP processor," International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-1, Issue-6, January 2013.

[10] Abdelgawad.A, "Low Power Multiply Accumulate Unit (MAC) For Future Wireless Sensor Networks," 978-1-4673-4637-5/13/$31.00 ©2013 IEEE

[11] Deepak s, Binsu J Kailath, "Optimized MAC unit design," 978-1-4673-5696-1/12/$26.00 ©2012 IEEE

[12] Jagadesh.P, "Design of High Performance 64 bit MAC unit," 2013 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2013], 978-1-4673-4922-2/13/$31.00 ©20 13 IEEE

[13] Teffi Francis, Tera Joseph, Jobin K Antony, "Modified MAC Unit for Low Power High Speed DSP Application Using Multiplier with Bypassing Technique and Optimized Adders," IEEE – 31661s