

TI Designs: TIDA-010042

MPPT charge controller reference design for 12- and 24-V solar panels



TEXAS INSTRUMENTS

Description

This reference design is a Maximum Power Point Tracking (MPPT) solar charge controller for 12-V and 24-V solar panels. This compact reference design targets small- and medium-power solar charger solutions and is capable of operating with 15- to 60-V solar panel modules, 12- or 24-V batteries, and providing upwards of 20 A output current. The design uses a two-phase interleaved buck converter to step down the panel voltage to the battery voltage. The buck converter and its connected gate drivers are controlled by a microcontroller unit (MCU), which calculates the maximum power point using the perturb and observe method. The solar MPPT charge controller is created with real-world considerations, including reverse battery protection, software programmable alarms and indications, and surge and ESD protection.

Resources

TIDA-010042	Design Folder
CSD18540Q5B, CSD19531Q5A	Product Folder
MSP430F5132	Product Folder
TPD1E10B06	Product Folder
INA240	Product Folder
LM5009	Product Folder
OPT3001	Product Folder
TLV704	Product Folder



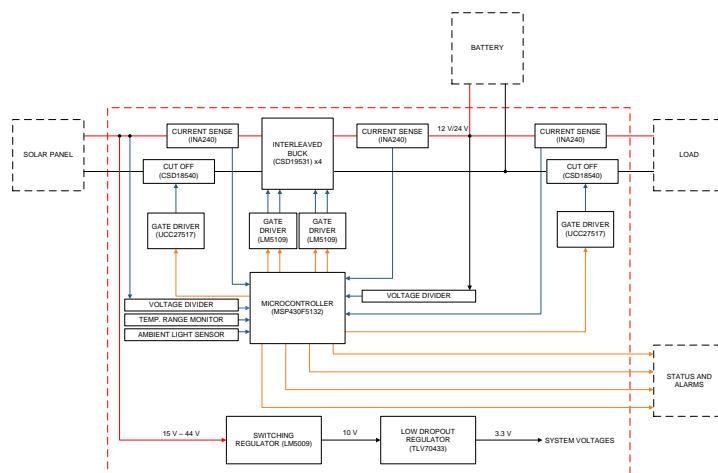
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Features

- 96% efficiency in 12-V systems and 97% efficiency in 24-V systems
- Wide input voltage range: 15 V to 60 V
- Flexible design supports 12- or 24-V battery voltages
- High rated output current: 20A
- Battery reverse polarity, over-charge and over-discharge protections
- System over-temperature and ambient light detection capabilities
- Small board form factor: 130 mm x 82 mm x 38 mm

Applications

- Solar Charge Controller
- Solar Power Optimizer





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1 System Description

This reference design is developed around the TI MSP430F5132 MCU and targeted for small and medium power solar charger solutions, capable of operating with 15- to 60-V solar panel modules and 12- or 24-V batteries with upwards of 20-A output current. However, the maximum current can be increased to 40 A by swapping for TO-220 package versions of the MOSFETs used in this design.

The design uses the perturb-and-observe algorithm for MPP tracking and has an operating efficiency of greater than 96%, including losses in the battery reverse polarity protection and panel reverse flow protection MOSFETs (CSD18540Q5B). The high efficiency is attributed to the low gate charge MOSFETs (CSD19531Q5A) and the interleaved buck topology in the design. Usage of small sized components is made possible by the high operating frequency (up to 200 kHz per stage) of the buck converter.

1.1 Key System Specifications

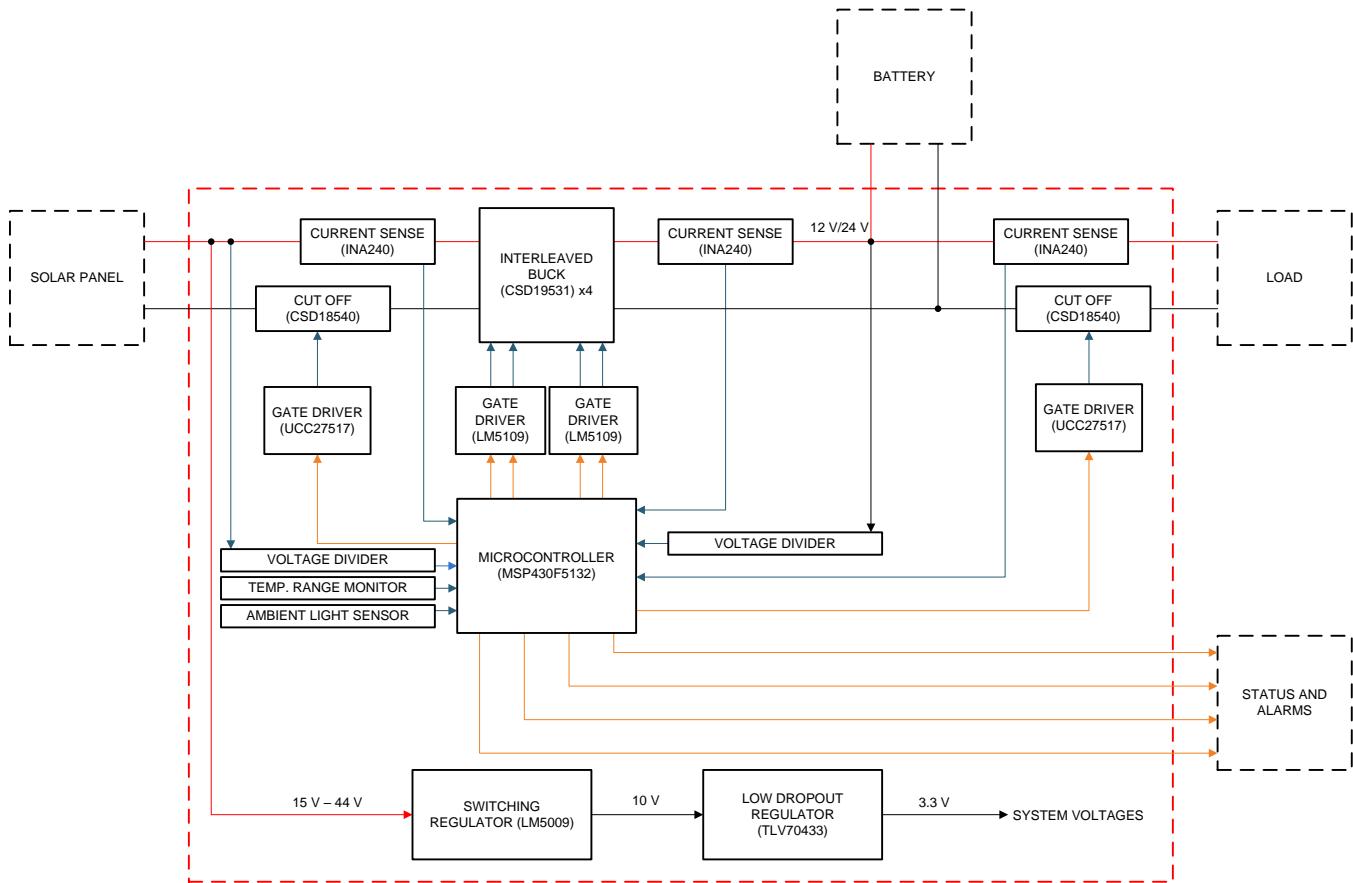
Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	UNIT
Input panel voltage range	15-60	V
Battery nominal voltage	12, 24	V
Rated maximum current	20	A
MPPT efficiency	>96	%
Interleaved buck operating frequency	180	kHz

2 System Overview

2.1 Block Diagram

Figure 1. TIDA-010042 Block Diagram



2.2 Design Considerations

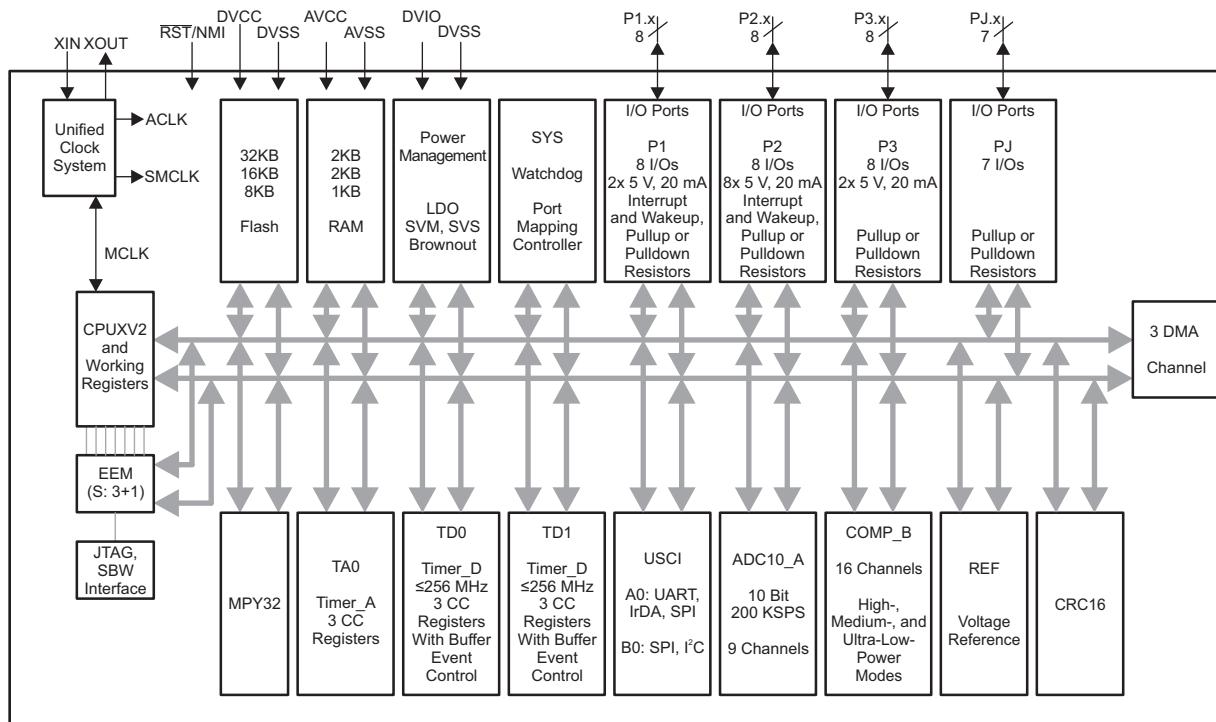
The TIDA-010042 board consists of a MCU (MSP430F5132) that gathers data from the panel and battery voltage lines and panel, battery, and load current sense amplifiers (INA240) and calculates and tracks the maximum power point of the solar panel. The MCUs then generate PWM signals that drive the gate drivers (LM5109B) of the interleaved buck converter, formed by CSD19531Q5A, 100-V N-Channel NexFET™ Power MOSFETs. The interleaved buck modulates the output battery charging current to maximize the power conversion efficiency and to prevent battery over-charge to increase the lifetime of the battery. A load enable gate (CSD18540Q5B) is also in place to protect from battery over-discharge, another means of extending the lifetime of the battery.

To power the system, a switching regulator (LM5009) is used to step down either the panel or battery voltage, whichever is greater, to 10 V for the gate drivers. From the 10 V, a low-dropout (LDO) regulator (TLV70433) is used to regulate a 3.3-V line for the rest of the components.

2.3 Highlighted Products

2.3.1 MSP430F5132

Figure 2. MSP430F5132 Block Diagram



The MSP430F5132 is a 25-MHz MCU with two 16-bit high resolution timers, 8KB flash, 1KB RAM, 10-bit ADC, and a 16-channel comparator.

- Low Supply-Voltage Range: 3.6 V Down to 1.8 V
- Ultra-Low Power Consumption
 - Active Mode (AM): 180- μ A/MHz
 - Standby Mode (LPM3 WDT Mode, 3 V): 1.1- μ A
 - Off Mode (LPM4 RAM Retention, 3 V): 0.9- μ A
 - Shutdown Mode (LPM4.5, 3 V): 0.25- μ A
- Wake up From Standby Mode in Less Than 5 μ s
- 16-Bit RISC Architecture, Extended Memory, 40-ns Instruction Cycle Time
- Flexible Power-Management System
 - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
 - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
 - FLL Control Loop for Frequency Stabilization
 - Low-Power Low-Frequency Internal Clock Source (VLO)
 - Low-Frequency Trimmed Internal Reference Source (REFO)
 - 32-kHz Crystals (XT1)
 - High-Frequency Crystals up to 25-MHz (XT1)
- Hardware Multiplier Supports 32-Bit Operations
- 3-Channel DMA
- Up to Twelve 5-V-Tolerant Digital Push-Pull I/Os With up to 20-mA Drive Strength

- 16-Bit Timer TD0 With Three Capture, Compare Registers and Support of High-Resolution Mode
- 16-Bit Timer TD1 With Three Capture, Compare Registers and Support of High-Resolution Mode
- 16-Bit Timer TA0 With Three Capture, Compare Registers
- Universal Serial Communication Interfaces (USCIs)
 - USCI_A0 Supports:
 - Enhanced UART Supports Automatic Baud-Rate Detection
 - IrDA Encoder and Decoder
 - Synchronous SPI
 - USCI_B0 Supports:
 - I2C
 - Synchronous SPI
- 10-Bit 200-ksps Analog-to-Digital Converter (ADC)
 - Internal Reference
 - Sample-and-Hold
 - Autoscan Feature
 - Up to 8-External Channels and 2-Internal Channels, Including Temperature Sensor
- Up to 16-Channel On-Chip Comparator Including an Ultra-Low-Power Mode
- Serial Onboard Programming, No External Programming Voltage Needed

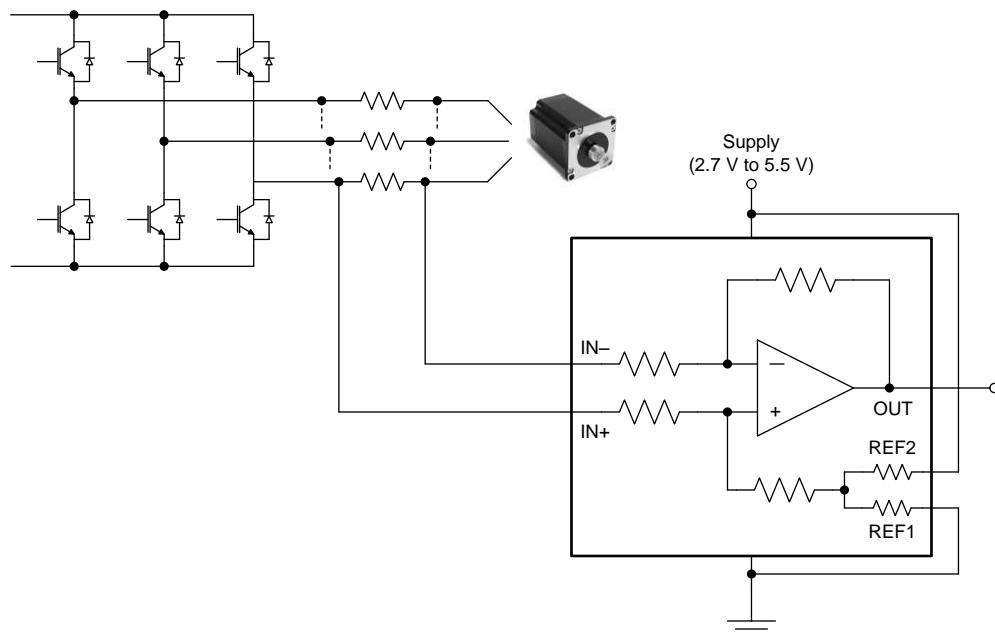
The voltage and current of the panel and battery lines are used to calculate and track the MPP and the MSP430F5132 enables quick data acquisition from the various analog signals using the internal analog-to-digital converter (ADC), set to read from the ADC channels once every 1.3 ms. Operating at 25 MHz allows for fast conversion and calculation to efficiently perform MPPT and adjust the interleaved buck converter output accordingly.

During battery charging mode, the MSP430F5132 generates pulse-width modulated (PWM) signals to the interleaved buck converter, where the duty cycle is proportional to the current output, or battery charging current, of the buck stage. The MCU is also responsible for managing the battery voltage by preventing over-charging of the battery, simply disabling the buck converter once a threshold voltage is reached, and protecting from over-discharging, disconnecting the load once a threshold load current is reached. By managing the battery, this reference design extends the life of the battery to utilize its maximum capabilities.

Status indicators and alarms, controlled by the MCU, are also included in the design to provide feedback to the user; however, they are left uninitialized.

2.3.2 INA240

Figure 3. INA240 Example Application



The INA240 is an 80 V, zero-drift current sense amplifier with enhanced PWM rejection.

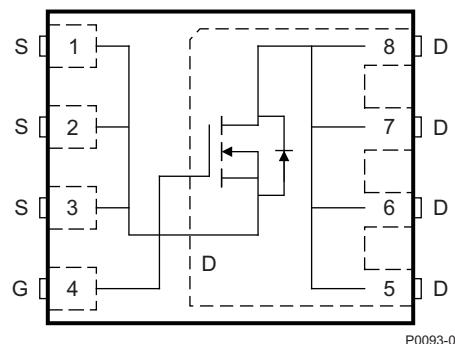
- Enhanced PWM Rejection
- Excellent CMRR:
 - 132-dB DC CMRR
 - 93-dB AC CMRR at 50 kHz
- Wide Common-Mode Range: -4 V to 80 V
- Accuracy:
 - Gain:
 - Gain Error: 0.20% (Maximum)
 - Gain Drift: 2.5 ppm/°C (Maximum)
 - Offset:
 - Offset Voltage: ±25- μ V (Maximum)
 - Offset Drift: 250 nV/°C (Maximum)
- Available Gains:
 - INA240A1: 20 V/V
 - INA240A2: 50 V/V
 - INA240A3: 100 V/V
 - INA240A4: 200 V/V
- Quiescent Current: 2.4 mA (Maximum)

The high common mode voltage (80 V) allows for support of up to 48-V battery systems without sacrificing accuracy and the negative common mode voltage (-4 V) allows the device to operate below ground to accommodate flyback.

The INA240 device is offered with 4 preset gain values of 20-, 50-, 100-, and 200 V/V with a maximum gain error of 0.20%. With support for a maximum system current of 20 A, the A2 (50-V/V gain) variation is used in this design to maximize current reading resolution and minimize power dissipation through the shunt resistor.

2.3.3 CSD19531Q5A

Figure 4. CSD19531Q5A Package Layout

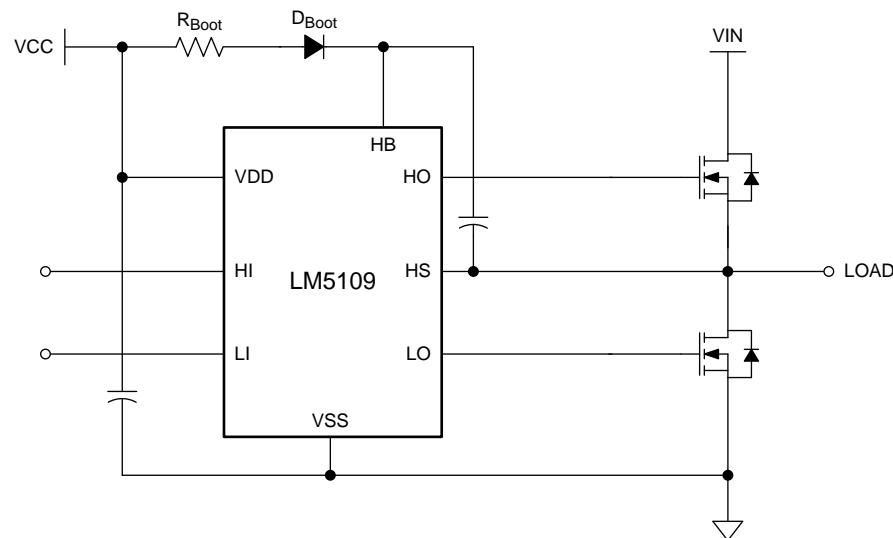


The CSD19531Q5A device is a 100-V, 5.3-mΩ NexFET Power MOSFET.

- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5 mm × 6 mm Plastic Package

2.3.4 LM5109B

Figure 5. LM5109 Example Circuit



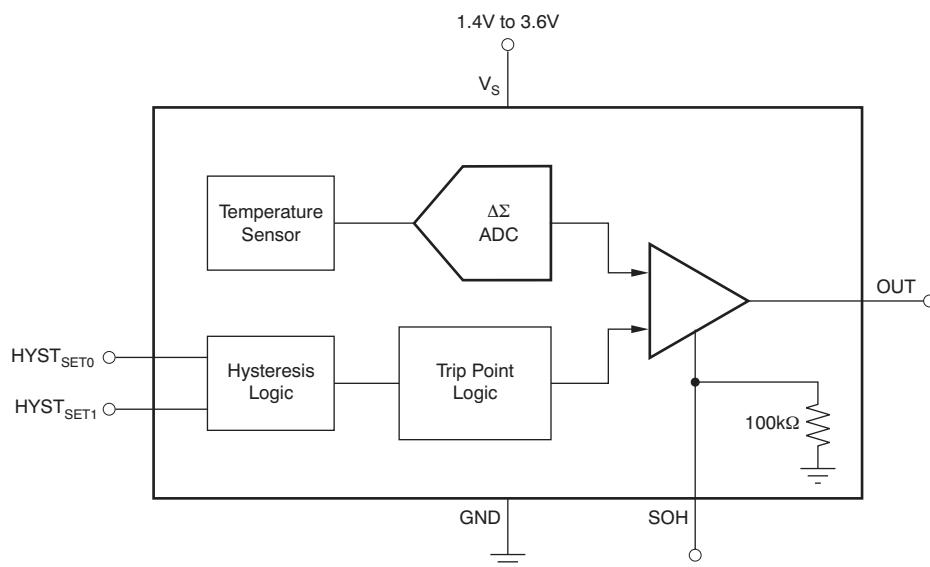
The LM5109B device is a 100-V, 1-A peak half bridge gate driver.

- Drives both a high side and low side N-Channel MOSFET
- 1-A peak output current (1.0-A sink, 1.0-A source)
- Independent TTL compatible inputs
- Bootstrap supply voltage to 118-V DC
- Fast propagation times (27 ns typical)
- Drives 1000-pF load with 15-ns rise and fall times

- Excellent propagation delay matching (2 ns typical)
- Supply rail undervoltage lockout
- Low power consumption
- Pin compatible with ISL6700

2.3.5 TMP303

Figure 6. TMP303 Block Diagram

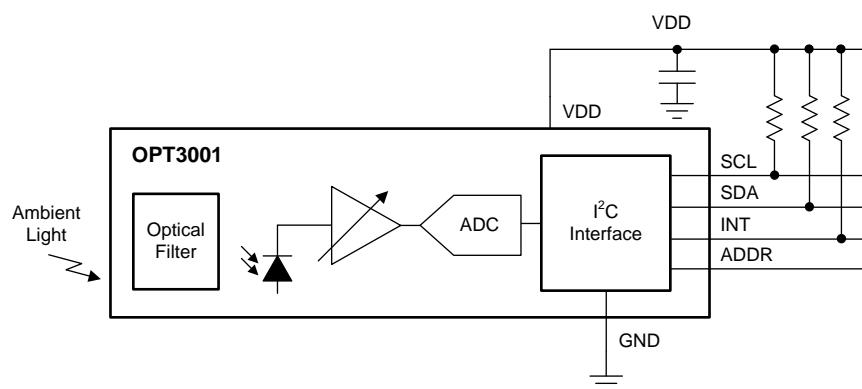


The TMP303 device is a factory-programmed temperature window comparator.

- Low Power: 5- μ A (Maximum)
- SOT-563 Package: 1.60 mm \times 1.60 mm \times 0.6 mm
- Trip Point Accuracy:
 - $\pm 0.2^{\circ}\text{C}$ (Typical) from -40°C to 125°C
- Push-Pull Output
- Selectable Hysteresis: 1-, 2-, 5-, 10°C
- Supply Voltage Range: 1.4 V to 3.6 V

2.3.6 OPT3001

Figure 7. OPT3001 Block Diagram



The OPT3001 is a digital ambient light sensor (ALS) with high-precision human-eye response.

- Precision Optical Filtering to Match Human Eye:
 - Rejects > 99% (typ) of IR
- Automatic Full-Scale Setting Feature Simplifies Software and Ensures Proper Configuration
- Measurements: 0.01-lux to 83-k lux
- 23-Bit Effective Dynamic Range With Automatic Gain Ranging
- 12 Binary-Weighted Full-Scale Range Settings: < 0.2% (typ) Matching Between Ranges
- Low Operating Current: 1.8- μ A (typ)
- Operating Temperature Range: -40°C to $+85^{\circ}\text{C}$
- Wide Power-Supply Range: 1.6 V to 3.6 V
- 5.5-V Tolerant I/O
- Flexible Interrupt System
- Small-Form Factor: 2.0 mm \times 2.0 mm \times 0.65 mm

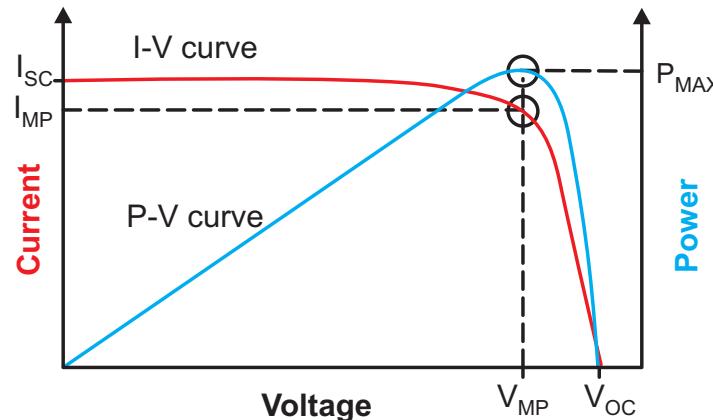
2.4 System Design Theory

2.4.1 MPPT Operation

The power output from a PV panel depends on a few parameters, such as the irradiation received by the panel voltage, panel temperature, and so forth. The power output also varies continuously throughout the day as the conditions affecting it change.

[Figure 8](#) shows the I-V curve and the P-V curve of a solar panel. The I-V curve represents the relationship between the panel output current and its output voltage. As the I-V curve in the figure shows, the panel current is at the maximum when its terminals are shorted and is at its lowest when the terminals are open and unloaded.

Figure 8. Solar Panel Characteristics I-V and P-V Curves



As [Figure 8](#) shows, obtain the maximum power output from the panel represented as P_{MAX} at a point when the product of the panel voltage and the panel current is at the maximum. This point is designated as the maximum power point (MPP).

The graphs in [Figure 9](#) and [Figure 10](#) show examples of how each of the various parameters affect the output power from the solar panel. The graphs also show the variation in the power output of a solar panel as a function of irradiance. Observe in these graphs how the power output from a solar panel increases with the increase in irradiance and decreases with a decrease in irradiance. Also note that the panel voltage at which the MPP occurs also shifts with the change in irradiance.

Figure 9. Solar Panel Output Power Variation Under Different Irradiation Conditions—Graph A

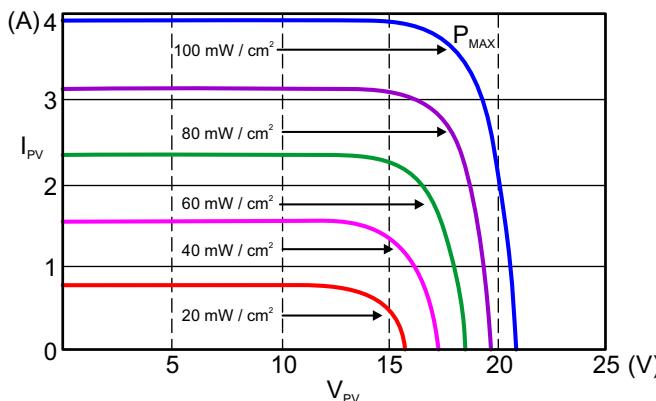


Figure 10. Solar Panel Output Power Variation Under Different Irradiation Conditions—Graph B

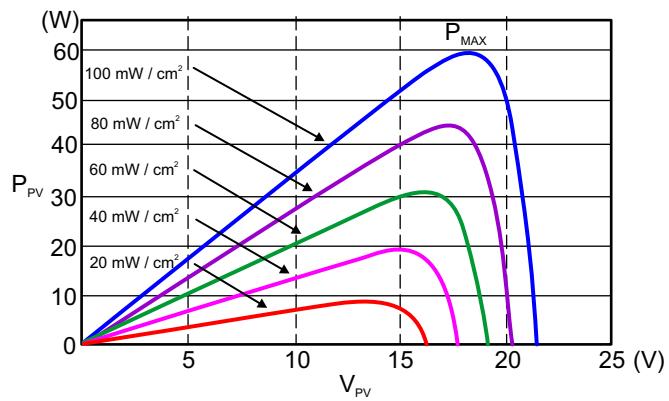
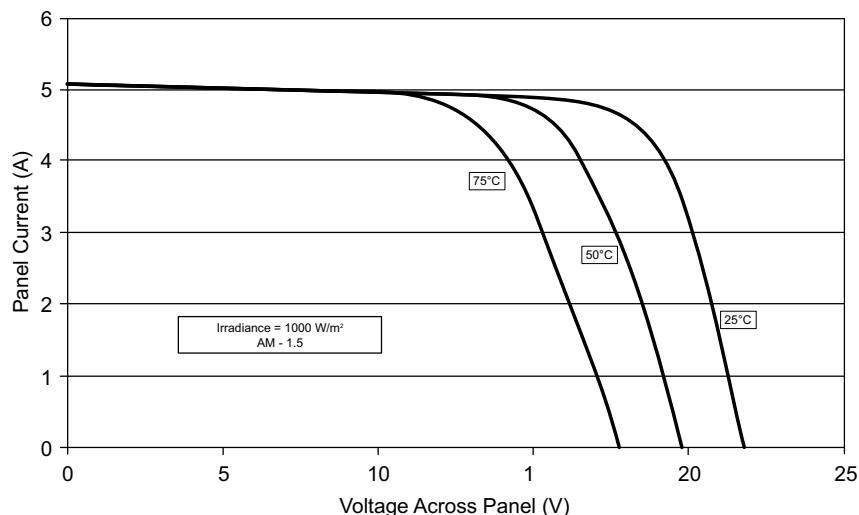


Figure 11 shows a typical graph representing the variation in the power output of a photovoltaic panel as a function of its temperature. Observe how the panel current (and thereby the panel power) decreases with an increase in temperature. The MPP voltage continues to shift substantially with the change in temperature.

Figure 11. Solar Panel I-V Curve Variation With Temperature Under Constant Irradiation Conditions



Draw the maximum power from a solar panel by operating the panel close to the MPP point; however, doing so poses two challenges:

1. Providing a way to connect a battery or load with a different operating voltage in comparison to the MPP of the panel
2. Identifying the MPP automatically, as it varies with the environmental conditions and is not a constant

Directly connecting a solar panel with a V_{MPP} close to 17 V to a 12-V lead acid battery forces the panel to operate at 12 V, which reduces the amount of power that can be drawn from the panel. From this situation, it can be surmised that a DC/DC converter is able to draw more power from the solar panel because this converter forces the solar panel to operate close to the V_{MPP} and transfer the power to a 12-V lead acid battery (impedance matching).

The preceding paragraph explains why the user implements a synchronous buck converter to charge the lead acid battery from the solar panel and address the first challenge.

The second challenge of automatically identifying the MPP of the panel is typically performed by employing MPPT algorithms in the system. The MPPT algorithm tries to operate the photovoltaic panel at the maximum power point and uses a switching power stage to supply the load with the power extracted from the panel.

Perturb and observe is one of the most popular MPPT algorithms used. The fundamental principle behind this algorithm is simple and easy to implement in a microcontroller based system. The process involves slightly increasing or decreasing (perturbing) the operating voltage of a panel. Perturbing the panel voltage is accomplished by changing the duty cycle of the converter. Assuming that the panel voltage has been slightly increased and that this leads to an increase in the panel power, then another perturbation in the same direction is performed. If the increase in the panel voltage decreases the panel power, then a perturbation in the negative direction is done to slightly lower the panel voltage.

By performing the perturbations and observing the power output, the system begins to operate close to the MPP of the panel with slight oscillations around the MPP. The size of the perturbations determines how close the system is operating to the MPP. Occasionally this algorithm can become stuck in the local maxima instead of the global maxima, but this problem can be solved with minor tweaks to the algorithm.

The P&O algorithm is easy to implement and effective, and was chosen for this design.

2.4.2 Interleaved Buck Converter

Table 2. Interleaved Buck Converter Design Criteria

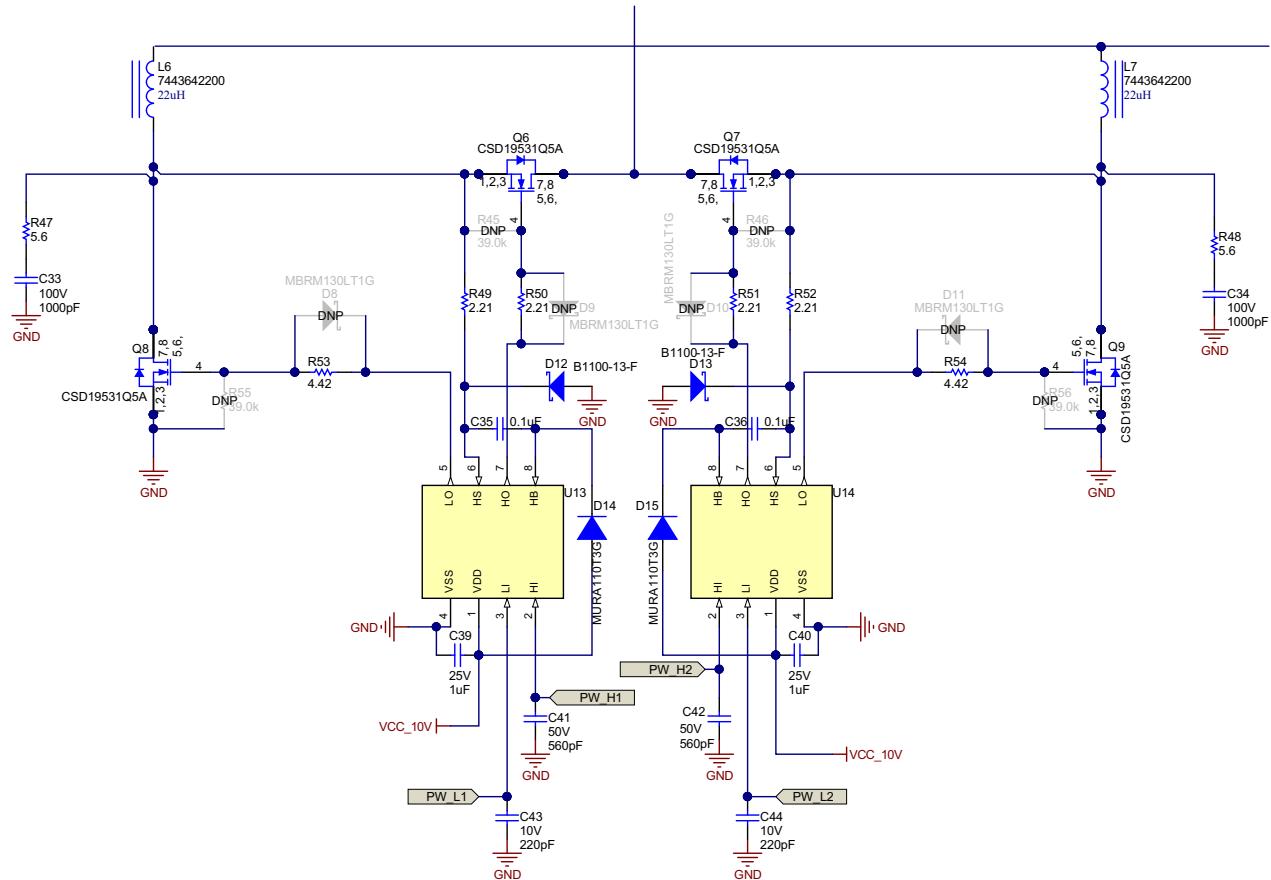
PARAMETER	SPECIFICATION
Max input voltage	60 V
Max Output voltage	24 V
Max current	20 A

This reference design implements a two-phase interleaved buck converter to decrease power dissipation and increase conversion efficiency. Interleaving also reduces ripple currents at the input and output of the buck converter (see [Benefits of a multiphase buck converter](#)), allowing for less filtering of signals.

With support for inputs of up to 60-V open-circuit voltage panels, the design must incorporate power MOSFETs with a maximum VDS of at least 60 V, while minimizing Qg and $R_{DS(on)}$ to reduce power loss and increase overall efficiency. The CSD19531Q5A is selected for this reference design for its high maximum VDS of 100 V and low Qg and $R_{DS(on)}$ of 37 nC and 5.3 mΩ, respectively, at a gate voltage of 10 V.

Each stage of the two-phase interleaved buck is designed using the standard synchronous buck topology as continuous conduction mode is desired to maintain a high efficiency while delivering the constant current required for battery charging.

Figure 12. Power Stage Schematic



2.4.3 Current Sense Amplifier

Table 3. Current Sense Amplifier Design Criteria

PARAMETER	SPECIFICATION
Max common-mode voltage	60 V
Maximum input current	20 A
Maximum output voltage	3.3 V

This reference design requires accurate measurement of the panel and battery currents to calculate and track the maximum power point. The design supports panels of up to 60 V for 24-V battery systems, so a maximum common-mode voltage of at least 60 V is required. The design also requires a negative common-mode voltage to ensure function during periods of flyback.

The INA240 is selected for this reference design. The best gain variation must be chosen, as higher gain amplifiers often have increased error and noise parameters, and paired with a shunt resistor that provides high resolution and low power dissipation. The following equations are used to calculate the resolution of the current sense amplifier and power dissipation of the shunt resistor for the parameters given in Table 3 and an example follows.

2.4.3.1 Shunt Resistor Selection

The minimum shunt resistor value for a 50-V/V gain amplifier is given by:

$$V_{\text{OUT}} = R_{\text{SHUNT}} \times (I_{\text{MAX}} \times \text{Gain}) = 3.3 \text{ V} = R_{\text{SHUNT}} \times (20 \text{ A} \times 50 \text{ V/V}) \quad (1)$$

So, $R_{SHUNT} \geq 3.3 \text{ m}\Omega$; since a lower power dissipation is a higher priority, an $R_{SHUNT} = 2 \text{ m}\Omega$ is selected for the design.

2.4.3.2 Current Measurement Resolution

The current resolution of the amplifier into a 10-bit ADC is given by:

$$I_{RES} = (V_{OUT} / (ADC MAX \times R_{SHUNT} \times Gain)) = (3.3 \text{ V} / (1023 \times 2 \text{ m}\Omega \times 50 \text{ V/V})) \quad (2)$$

$$\text{So, } I_{\text{RES}} = 32.25 \text{ mA per bit}$$

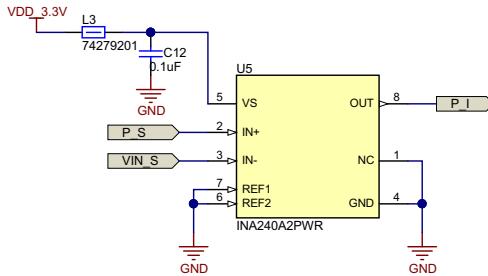
2.4.3.3 Shunt Resistor Power Dissipation

The maximum power dissipation is given by:

$$P_{DISS} = I_{MAX2} \times R_{SHUNT} = (20 \text{ A})^2 \times 2 \text{ m}\Omega \quad (3)$$

$$\text{So, } P_{\text{DISS}} = 0.8 \text{ W}$$

Figure 13. Shunt Amplifier Schematic



2.4.4 Switching Regulator

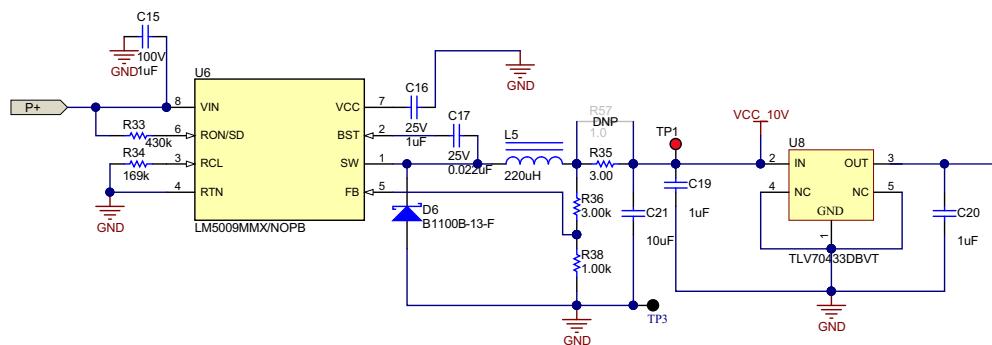
PARAMETER	SPECIFICATION
Input voltage range	10 V to 60 V
Output voltage	10 V
Load current	150 mA
Nominal switching frequency	185 kHz

This reference design requires 10 V for the gate drivers (the LM5109B and UCC27517 devices), subsequently stepped down to 3.3 V for the MSP430F5132 device and other components, to operate. To generate the 10-V line from the power lines (panel or battery voltages), a wide VIN buck, switching regulator is needed to support a maximum panel voltage of 60 V.

The LM5009 device is a wide VIN, on-time non-synchronous buck regulator that provides cost effective and highly efficient power conversion. See the *Application and Implementation* section of the [LM5009 Wide Input, 100-V, 150-mA, Step-Down Switching Regulator](#) as a starting point for this design; however, an input below 11.8 V was not supported during testing.

2.4.4.1 Changes to Example Application

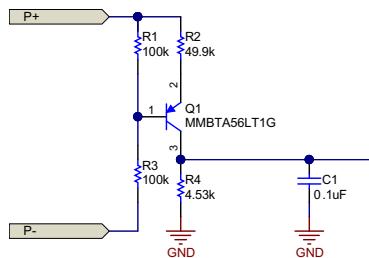
As previously mentioned, the original switching regulator design was not allowing system power-up at voltages below 11.8 V due to violation of the 300 ns minimum off-time. To increase the off-time, thereby decreasing the minimum VIN required to power the system and the switching frequency, R33 is increased from 237 k Ω to 430 k Ω . With this change, the minimum VIN is reduced to 11 V.

Figure 14. Power Supply Schematic


2.4.5 Panel Voltage Measurement

This reference design enables voltage sense of floating panels (disconnected via low-side panel enable). When disconnecting the panel from the system ground and using a simple voltage divider between the positive and negative connections of the panel, outputs of negative voltage are possible. To resolve this, the design uses a PNP bipolar junction transistor (BJT) to shift the signal such that the output is always positive and below 3.3 V with respect to ground.

With the base biased to half the panel voltage, so $VE > VB > VC$, the BJT (MMBTA56L) is kept in its forward active region and the circuit simply becomes an isolated voltage divider by converting the panel voltage into an equivalent current flowing through resistor R4. The voltage at the top node of R4 is then measured by the ADC of the MSP430F5132 MCU as an indirect, isolated measure of the panel voltage (see the [High Efficiency, Versatile Bidirectional Power Converter for Energy Storage and DC Home Solutions](#) design guide).

Figure 15. Voltage Measurement Schematic


3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 TIDA-010042

Figure 16 and [Figure 17](#) show the full design solution, with the bare PCB measuring at 130 mm × 82 mm.

Figure 16. TIDA-010042 Top View

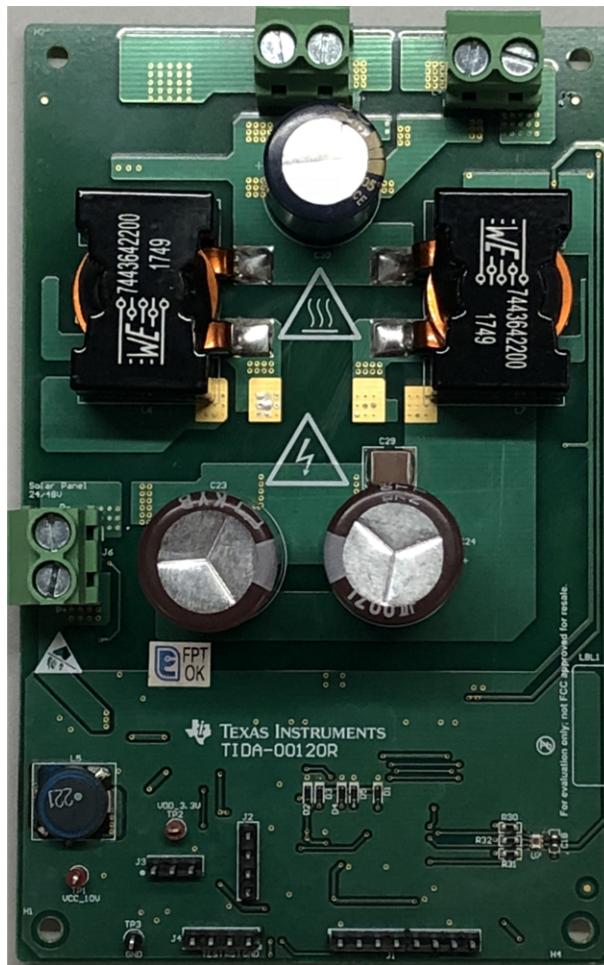
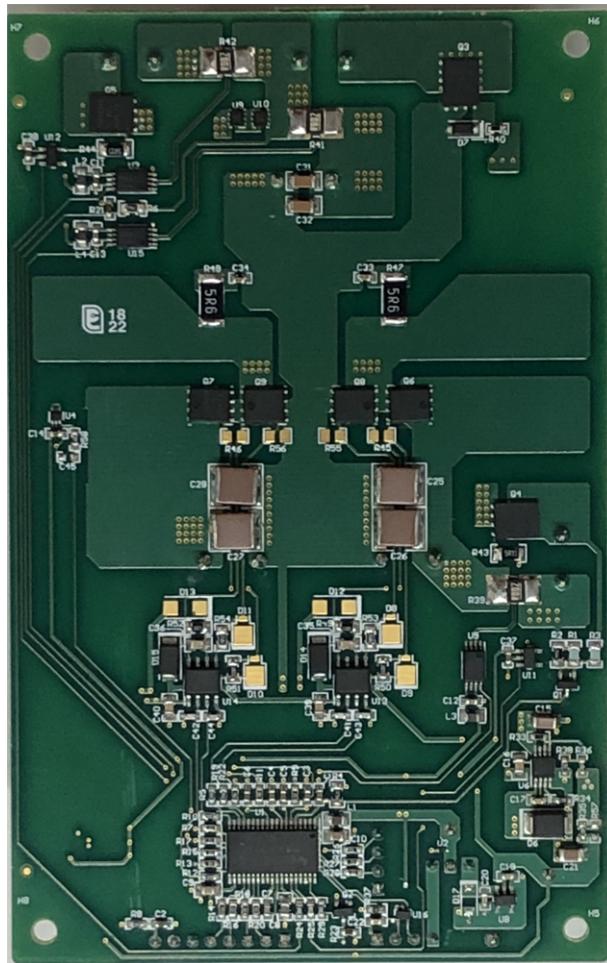


Figure 17. TIDA-010042 Bottom View



[Table 4](#) breaks out the various headers and their associated pin connections.

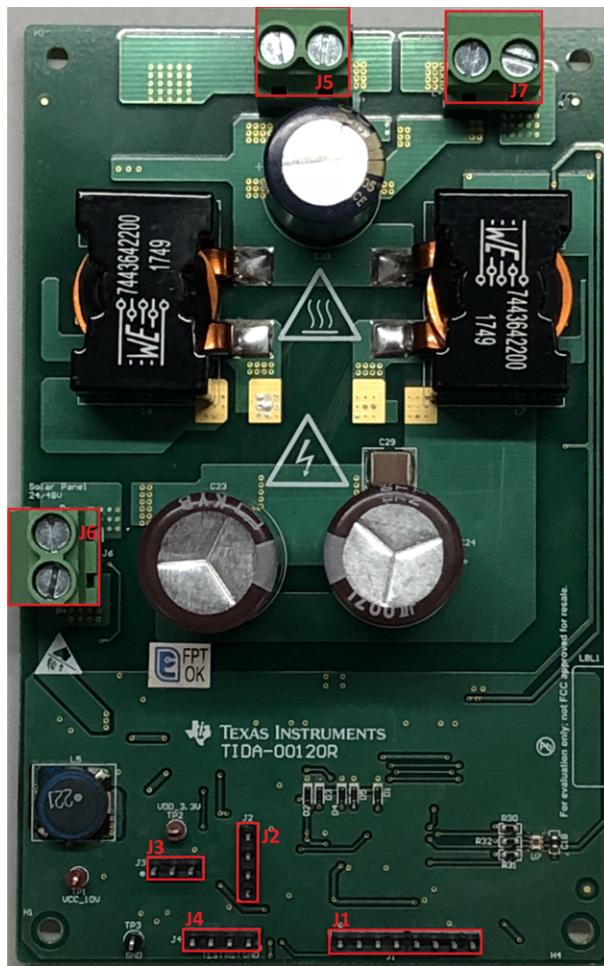
J1 is used for various status and alarm indicators and pins 4 and 5 are used for communication with the optional GUI provided with the TIDA-00120R software.

J2 can be configured to provide up to 3 battery status indicators.

J3 is used to provide the necessary 3.3 V for the microcontroller: pins 1 and 2 should be connected if power is provided by the battery and pins 2 and 3 should be connected if power is provided by the MSP-FET430UIF Programmer. If power is to be provided by the programmer, make sure the tool VCC is used. If system debugging is required with power provided by the battery, connect all 3 pins and make sure the target VCC is used.

J4 provides communication between the programmer and MSP430F5132.

J5, J6, and J7 are the battery, PV panel, and load connections, respectively.

Figure 18. TIDA-010042 Board Headers

Table 4. Headers Connections

DESIGNATOR	PIN NUMBER	SIGNAL
J1 – status and alarms	1	Ground
	2	MSP430F5132 Pin 26 (P2.7)
	3	MSP430F5132 Pin 25 (P2.6)
	4	MSP430F5132 Pin 24 (P2.5) -- also used for GUI RX
	5	MSP430F5132 Pin 23 (P2.4) -- also used for GUI TX
	6	NC
	7	Buzzer output
	8	10 V
J2 – battery status indicators	1	Ground
	2	MSP430F5132 Pin 3 (PJ.5)
	3	MSP430F5132 Pin 2 (PJ.4)
	4	MSP430F5132 Pin 14 (PJ.3)
J3 – 3.3-V power source	1	3.3-V LDO output
	2	Connect to 1 or 3 to provide 3.3 V to the system
	3	MSP-FET430UIF Programmer tool voltage

Table 4. Headers Connections (continued)

DESIGNATOR	PIN NUMBER	SIGNAL
J4 – programming header	1	MSP-FET430UIF Programmer voltage
	2	MSP-FET430UIF Test
	3	MSP-FET430UIF Reset
	4	MSP-FET430UIF Ground
J5 – battery connection	1	Positive battery (B+) terminal
	2	Negative battery (B-) terminal
J6 – PV panel connection	1	Negative panel (P-) terminal
	2	Positive panel (P+) terminal
J7 – load connection	1	Negative load (L-) terminal
	2	Positive load (L+) terminal

3.1.1.2 TDK-Lambda GEN100-33

The Genesys® 2U full-rack series of 3300-W DC programmable power supplies series gives the sufficient output power for testing the board, since it offers output voltages from 8 V(at 400 A) to 600 V (at 5.5 A).

https://www.us.tdk-lambda.com/hp/product_html/genesys2u3_3.htm

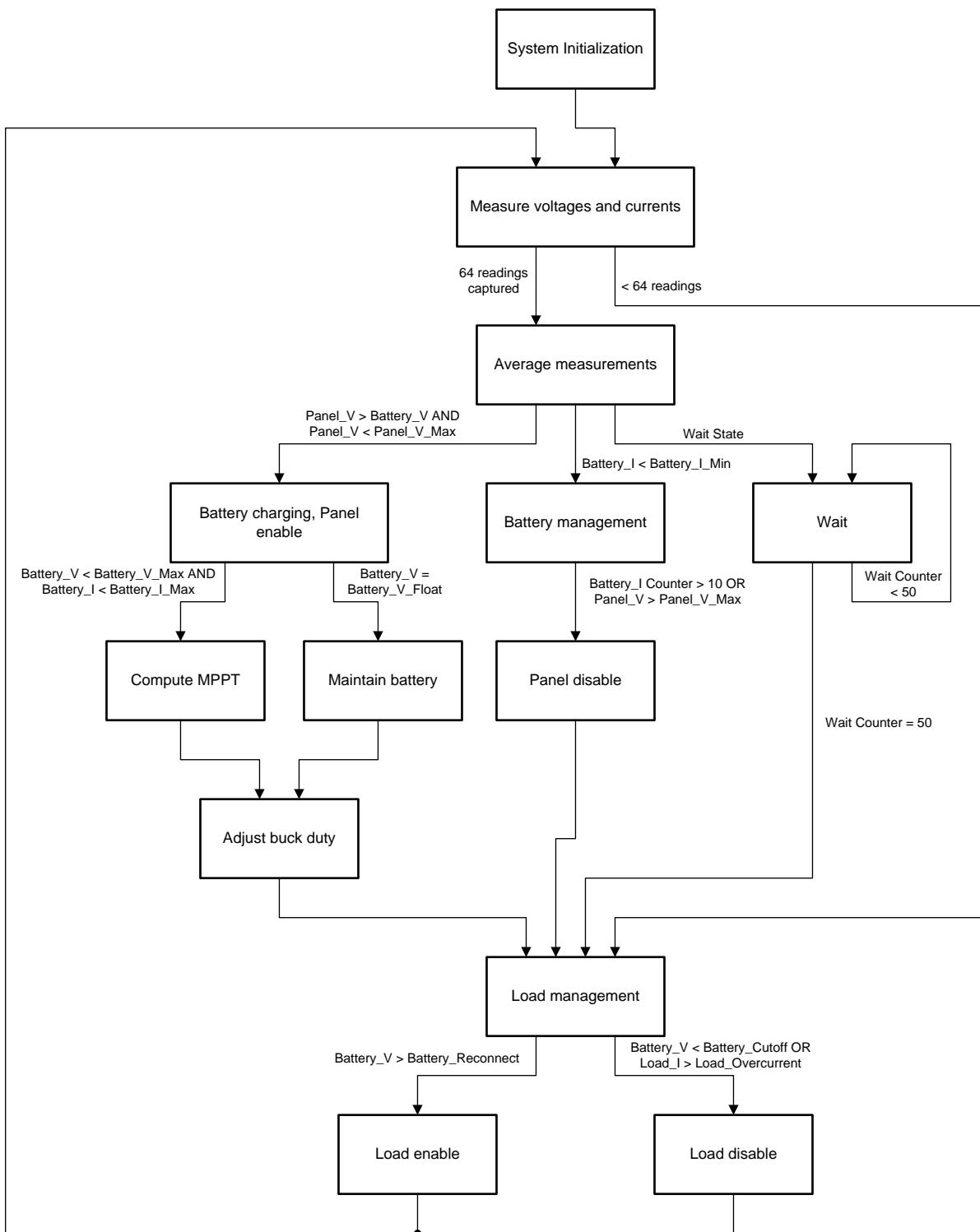
3.1.1.3 HP, Agilent 6060b

Agilent technologies 6060B series is used in the following measurements to draw power from the system. The single input electronic load is specified up to 300 W.

<https://www.keysight.com/en/pd-1000001519:epsg:pro-pn-6060B/300-watt-dc-electronic-load?&cc=US&lc=eng>

3.1.2 Software

Figure 19. TIDA-010042 Software Flow



After initializing peripherals like the ADC, the comparator or the timer, the value of the voltage and current measurements are read, as long as there are under 64 reading times. Otherwise, the software would jump to the Load management function.

Furthermore, the values get averaged and dependent on the input value the Battery Charging function, the Battery management function or a Wait State starts. The Battery Charging function enables the Panel, the Buck converter, calculates an MPP and sets the frequency for the Buck converter. The Battery management part disables the Panel, Buck Converter and continues with a waiting state. The Wait State lasts 5 seconds and is checking the input parameters.

To prevent from over discharging, the previous three functions are all followed by Load Management, which is able to control the load connection.

3.2 Testing and Results

3.2.1 Test Setup

Connect the DC voltage source, to the panel connection (J6). The input voltage should range from 15 V to 22 V for 12-V systems and from 30 V to 44 V for 24-V systems.

Connect the battery or electronic load to the battery connection (J5). This reference design supports 12- or 24-V batteries. If using an electronic load to simulate a battery, set the load to constant current mode (CC) and to the respective voltage system regulates its voltage itself.

3.2.2 Test Results

Figure 20. Efficiency Curve Over Output Current for the 12-V System

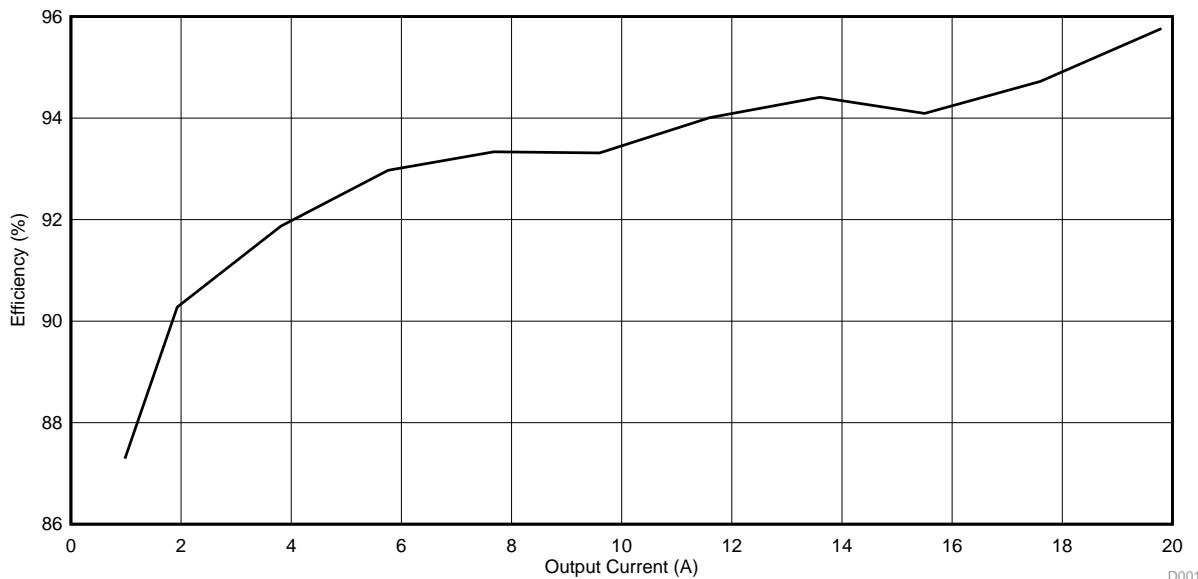


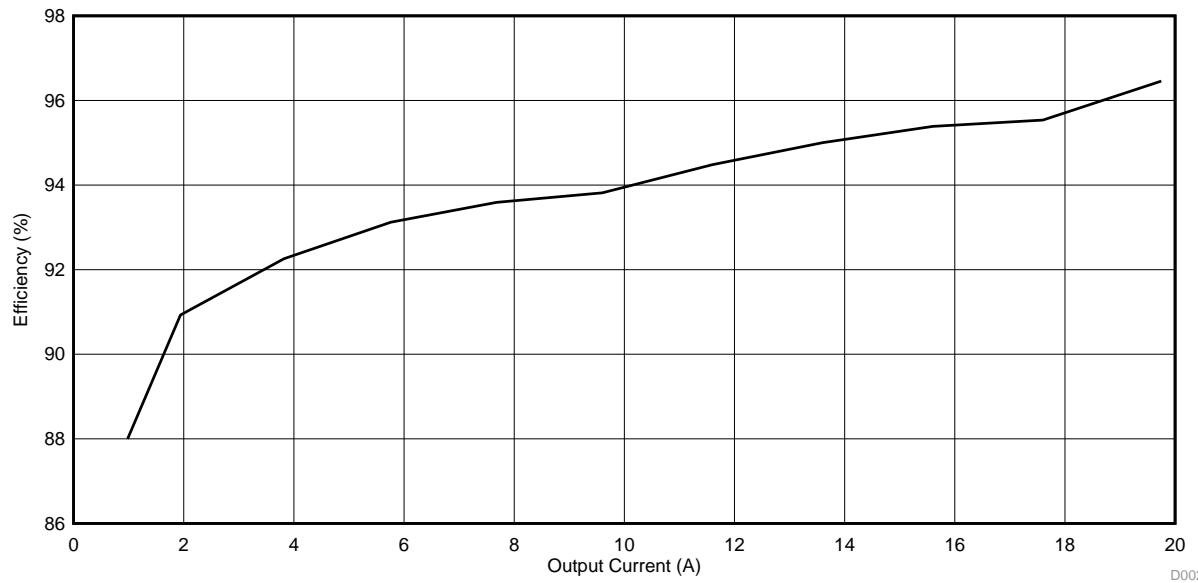
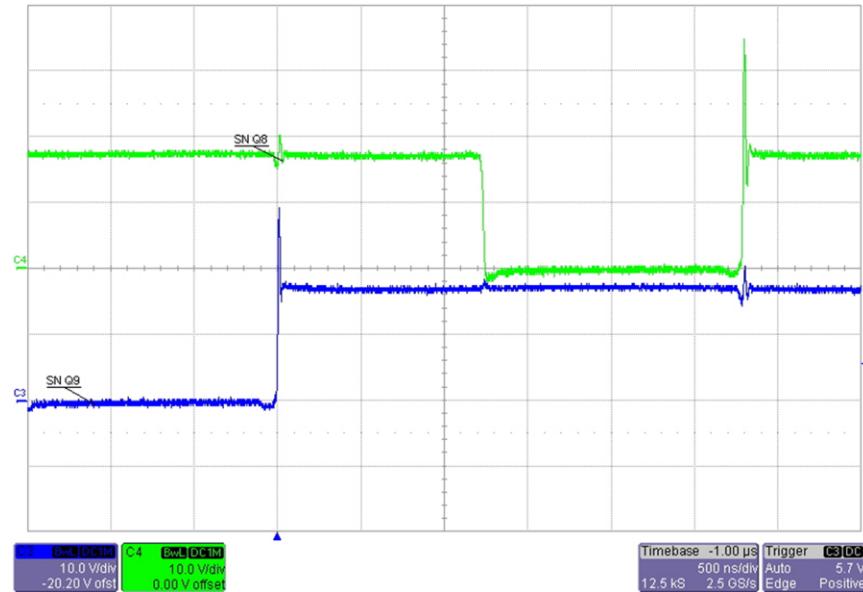
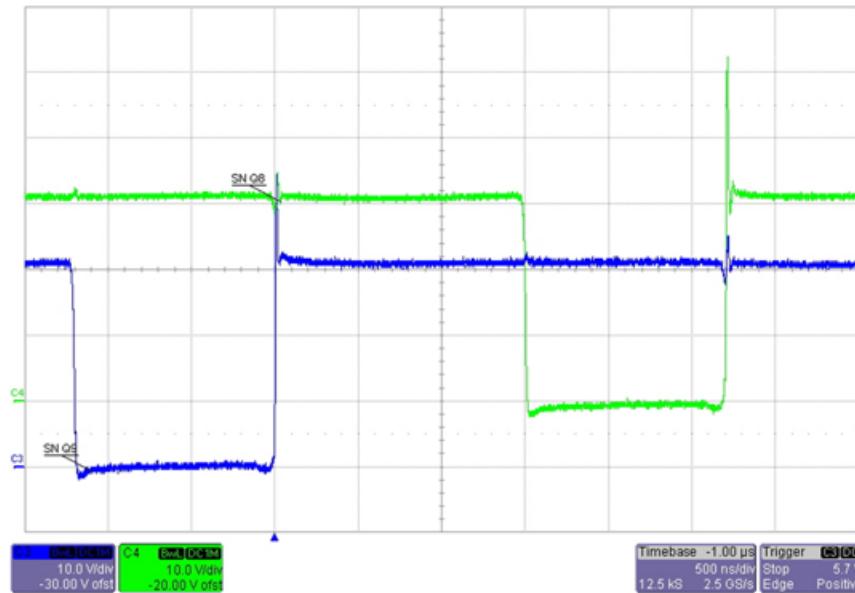
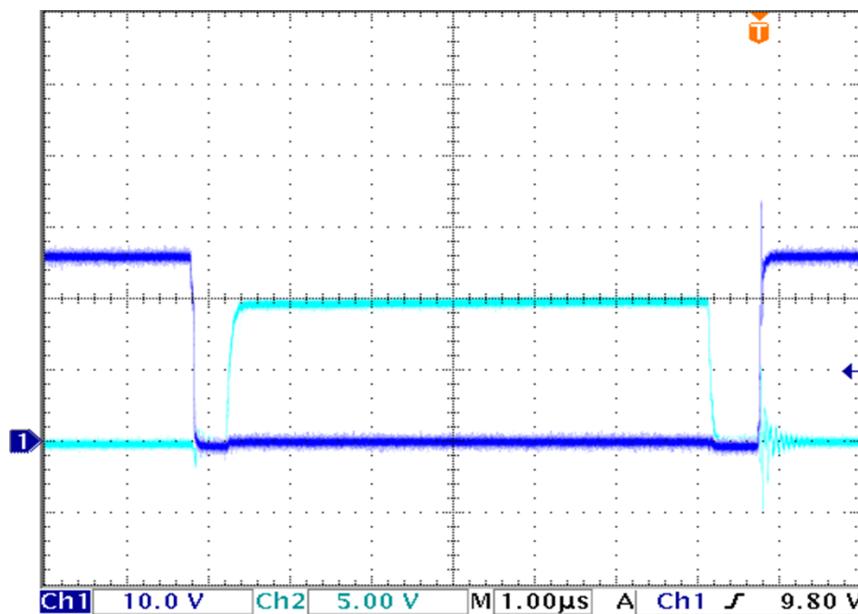
Figure 21. Efficiency Curve Over Output Current for the 24-V System

Figure 22. Switch Nodes at $V_{IN} = 17.5$ V; Gate Resistor: 10 Ω


Figure 23. Switch Nodes at V_{IN} 32 V; Gate Resistor: 10 Ω **Figure 24. Top and Bottom Gate Waveform Showing Dead-Time Implementation**

4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-010042](#).

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-010042](#).

4.3 PCB Layout Recommendations

4.3.1 Loop Inductances

When working with high frequency switching waveforms, loop inductances need to be minimized to keep ringing at a minimum. Loop inductances can arise due to component placement and routing. Place traces along the shortest distance between components and integrate bypass capacitors into the design to maintain signal integrity.

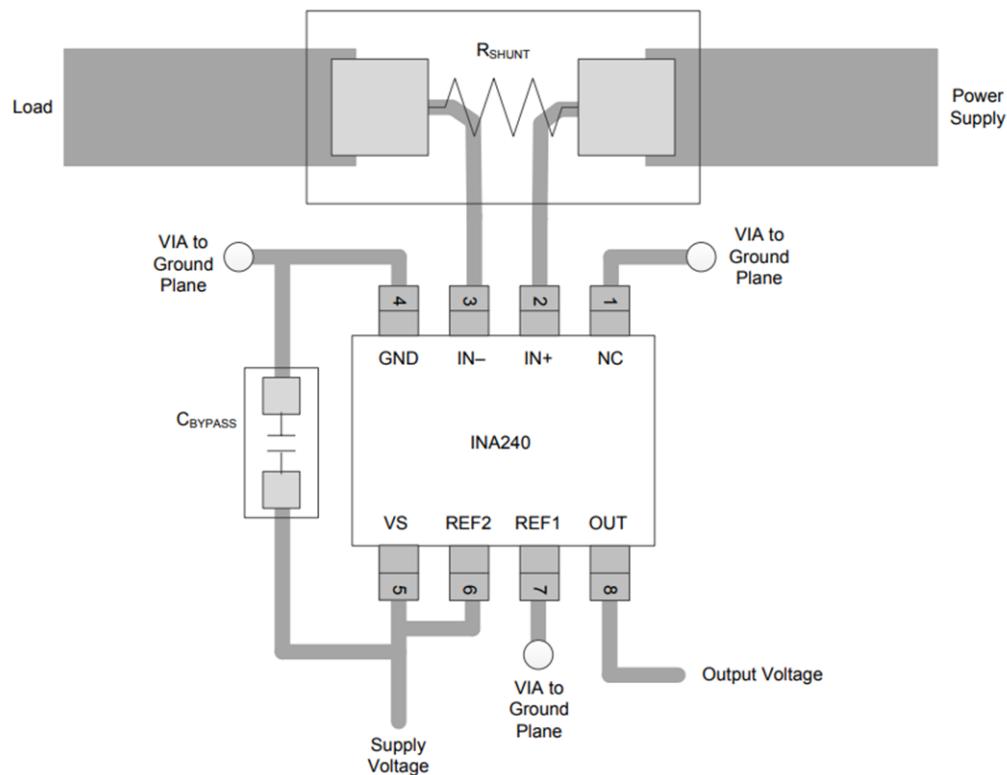
Trace length and placement need to be taken into consideration when routing. Short, straight traces produce the lowest impedance path for the signal and minimize the current loop area, thereby reducing loop inductances present.

Bypass capacitors filter and condition signals before use and should be placed as close to the respective component as possible. Any extraneous trace between the capacitor and component will mitigate the effectiveness of the bypass capacitor.

4.3.2 Current Sense Amplifiers

Poor routing of the current-sensing resistor can result in additional resistance between the input pins of the amplifier. Any additional high-current carrying impedance can cause significant measurement errors because the current resistor has a very-low-ohmic value. Use a Kelvin or 4-wire connection to connect to the device input pins. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins.

Figure 25. INA240 Recommended Layout



4.3.3 Trace Widths

Current capacity, or ampacity, of the trace and the allowable space between traces need to be taken into consideration when selecting traces widths for routing. For a given trace, there is a maximum current it can handle before failure. Injecting currents larger than rated leads to excess heat dissipation and can cause the trace to be destroyed.

This design can handle currents of up to 20 A. If designing for higher current systems, trace widths will need to be adjusted accordingly.

4.3.4 Layout Prints

To download the layer plots, see the design files at [TIDA-010042](#).

4.4 Altium Project

To download the Altium Designer® project files, see the design files at [TIDA-010042](#).

4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-010042](#).

4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-010042](#).

5 Software Files

To download the software files, see the design files at [TIDA-010042](#).

6 Related Documentation

1. Texas Instruments, *Benefits of a multiphase buck converter Technical Brief*
2. Texas Instruments, *High Efficiency, Versatile Bidirectional Power Converter for Energy Storage and DC Home Solutions*

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7 About the Author

VAIBHAVI SHANBHAG is a systems engineer at Texas Instruments, where she is responsible for developing reference design solutions for the Motor Drive segment within Industrial Systems. Vaibhavi received her bachelor of engineering in Electrical and Electronics engineering from BITS Pilani, K.K.Birla Goa campus.

DING-SHIN KUO is an applications engineer in the Grid Infrastructure Solutions team at Texas Instruments, with a focus in the renewable energy sector. Ding brings his experience in system design and testing to create an optimal system level design. Ding received his bachelor's and master's degrees in electrical engineering from the University of Florida.

Marion Loessl is a field application engineer, working in her trainee program for Grid Infrastructure System team at Texas Instruments in Dallas. Afterwards she will deploy to Germany to support customers with her technical and system based knowledge. Marion brings in her electrical engineering Bachelors degree from Ostbayrische Technische Hochschule Regensburg of Renewable Energy and Energy Efficiency.

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