RV INSTITUTE OF TECHNOLOGY AND MANAGEMNET

RV Institute of Technology and Management®

Laboratory Manual

Department of Electronics & Communication Engineering

ANALOG AND DIGITAL SYSTEM DESIGN LAB [BECL305]
SCHEME: 2022

SEMESTER –III

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PROGRAMME EDUCATION OBJECTIVES [PEOs]

PEO1: (Domain Knowledge) Graduates of Electronics & Communication Engineering will be able to utilize mathematics, science, engineering fundamentals, theoretical as well as laboratory based experiences to identify, formulate & solve engineering problems and succeed in advanced engineering or other fields.
PEO2: (Professional Employment) Graduates of Electronics & Communication Engineering will succeed in entry-level engineering positions in VLSI, Communication and Fabrication industries in regional, national, or global industries.
PEO3: (Engineering Citizenship) Graduates of Electronics & Communication Engineering will be prepared to communicate and work effectively on individual & team based engineering projects while practicing the ethics of their profession consistent with a sense of social responsibility.
PEO4: (Lifelong Learning) Graduates of Electronics & Communication Engineering will be equipped to recognize the importance of, and have the skills for, continuous learning to become experts in their domain and enhance their professional attributes

PROGRAMME OUTCOMES [POs]

PO1: Engineering Knowledge: Apply knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.
PO2: Problem Analysis: Identify, formulate, research literature and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and engineering sciences.
PO3: Design/ Development of Solutions: Design solutions for complex engineering problems and design system components or processes that meet specified needs with appropriate consideration for public health and safety, cultural, societal and environmental considerations.
PO4: Conduct investigations of complex problems using research-based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of information to provide valid conclusions.
PO5: Modern Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
PO6: The Engineer and Society: Apply reasoning informed by contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to professional engineering practice.
PO7: Environment and Sustainability: Understand the impact of professional engineering solutions in societal and environmental contexts and demonstrate knowledge of and need for sustainable development.
PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of engineering practice.
PO9: Individual and Team Work: Function effectively as an individual, and as a member or leader in diverse teams and in multi-disciplinary settings.
PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations and give and receive clear instructions.
PO11: Project Management and Finance: Demonstrate knowledge and understanding of engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12: Life-long Learning: Recognize the need for and have the preparation and ability to Engage in independent and life-long learning in the broadest context of technological changes

PROGRAMME SPECIFIC OBJECTIVES [PSOs]

PSO1: (Knowledge/ Skills) Explore emerging technologies in the field of Electronics & Communication Engineering using the knowledge and skills gained.
PSO2: (Application/Analysis/Problem solving) Apply techniques in different domains to create innovative products and services in the Communication, VLSI, DSP, and Networking.
PSO3: (Value/ Attribute) Work on various platforms as an individual/ team member to develop useful and safe Circuits, PCB, Power Management Systems and Automation for the society and nation.

ANALOG AND DIGITAL SYSTEM DESIGN LAB (BECL305)

SEMESTER - III

CONTENTS

Laboratory Safety Information

To work safely, it is important that you understand the prudent practices necessary to minimize the risks and what to do if there is an accident.

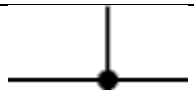
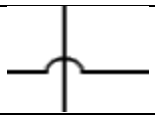
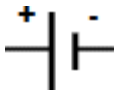
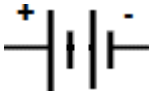
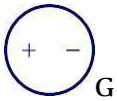
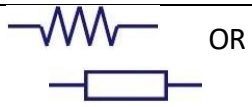
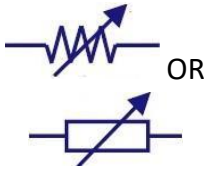
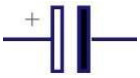
Electrical Shock

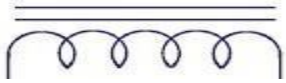
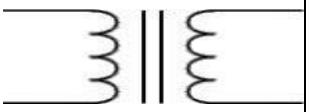
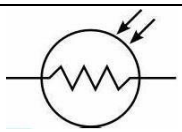
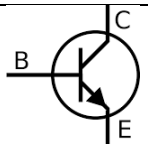
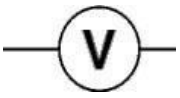
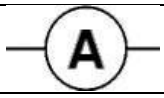
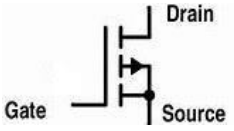
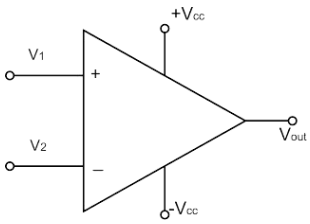
- Avoid contact with conductors in energized electrical circuits.
- Electrocution has been reported at de voltages as low as 42 volts. Just 100 mA of current passing through the chest is usually fatal.
- Muscle contractions can prevent the person from moving away while being electrocuted.
- Do not touch someone who is being shocked while still in contact with the electrical conductor or you may also be electrocuted.
- Make sure your hands are dry.
- The resistance of dry, unbroken skin is relatively high and thus reduces the risk of shock. Skin that is broken, wet or damp with sweat has a low resistance.
- When working with an energized circuit, work with only your right hand, keeping your left hand away from all conductive material. This reduces the likelihood of an accident that results in current passing through your heart.
- Be cautious of rings, watches, and necklaces. Skin beneath a ring or watch is damp, lowering the skin resistance.
- Shoes covering the feet are much safer than sandals.

Circuit Trouble Shooting Hints

- ✓ Be sure that the power is turned on.
- ✓ Be sure the ground connections are common.
- ✓ Be sure the circuit you built is identical to that in the diagram. (Do a node-by-node check)
- ✓ Be sure that the supply voltages are correct.
- ✓ Be sure you plug in cable to the right terminal in the multimeter to measure the voltage/resistance (upper terminal) or the current (lower terminal).
- ✓ Be sure that the equipment is set up correctly and you are measuring the correct parameter.
- ✓ Be sure the BJT's collector and emitter terminals are in correct orientation.
- ✓ If steps 1 through 5 are correct, then you probably have used a component with the wrong value or one that doesn't work.
- ✓ It is also possible that the equipment does not work (although this is not probable) or the bread-board you are using may have some unwanted paths between nodes.
- ✓ To find your problem you must trace through the voltages in your circuit *node by node* and compare the signal you have to the signal you expect to have.
- ✓ Finally, ask your lab assistant.

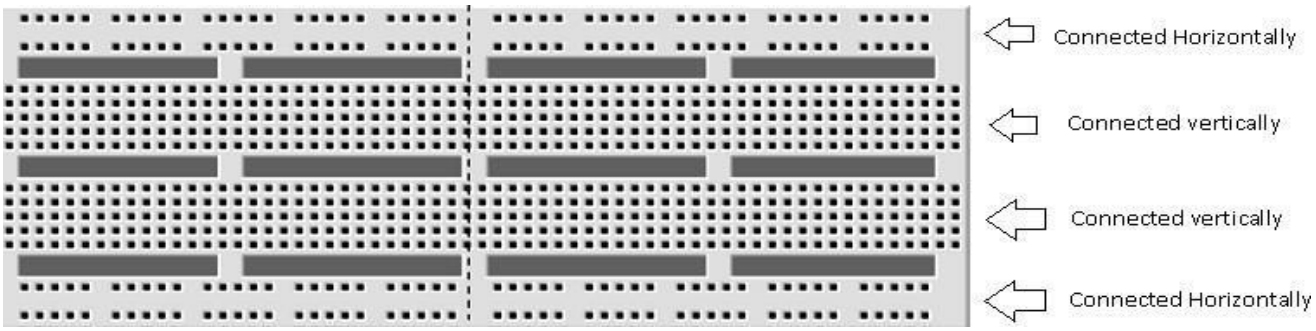
Component Symbol and Description

Component	Circuit Symbol	Function of Component
Wire		To pass current from one part of a circuit to another.
Wires joined		Wires connected at junctions should be staggered slightly to form two T-junctions, as shown.
Wires not joined		Wires crossing even though they are not connected.
Fuse		The Fuse reacts as safety element to protect circuit against large current and sudden urges of current.
Switch (SPST)		SPST = Single Pole, Single Throw. An on-off switch allows current to flow only when it is in the closed (on) position.
Cell		Cell Supplies electrical energy. The larger terminal is positive (+). A single cell is often called a battery, but strictly a battery is two or more cells joined together.
Battery		Supplies electrical energy. A battery is more than one cell. The larger terminal is positive (+).
AC Supply		This represents AC supply in the circuit.
DC Supply		This represents the DC power supply. It applies DC supply to the circuit.
Ground		It is equivalent to theoretical **0 V** and is used as zero potential reference. It is the potential of perfectly conducting earth.
Fixed Resistor		It is a device that opposes the flow of current in a circuit. These two symbols are used to represent fixed resistor.
Rheostat		It is a two terminal variable resistor. They are generally used to control the current in the circuit. Generally used in tuning circuits and power control applications like heaters, ovens etc
Capacitor		Capacitor stores the charge in the form of electrical energy. It can be used in both AC and DC circuits.
Electrolytic Capacitor		Almost all electrolytic capacitors are polarized and hence used in DC circuits. It can also be used as a filter, to block DC signals but pass AC signals.

Component	Circuit Symbol	Function of Component
Iron Core Inductor		A coil of wire which creates a magnetic field when current passes through it.
Transformer		Two coils of wire linked by an iron core. Transformers are used to step up (increase) and step down (decrease) AC voltages. Energy is transferred between the coils by the magnetic field in the core. There is no electrical connection between the coils.
Diode		A device which only allows current to flow in one direction.
LED		A transducer which converts electrical energy to light.
LDR		LDRs or photo-resistors are often used in circuits where it is necessary to detect the presence or the intensity level of light.
Zener Diode		A special diode which is used to maintain a fixed voltage across its terminals.
Transistor (NPN)		A transistor amplifies current. It can be used with other components to make an amplifier or switching circuit.
Voltmeter		A voltmeter is used to measure voltage. The proper name for voltage is 'potential difference', but most people prefer to say voltage!
Ammeter		An ammeter is used to measure current.
JFET N- Channel		N-channel JFET is made by n-type silicon bars which form two PN junctions at the side. Majority charge carriers here are electrons.
MOSFET P-Channel		The enhancement MOSFET structure has no channel formed during its construction. Voltage is applied to the gate, so as to develop a channel.
OPAMP		An **operational amplifier** (**op-amp**) is a DC-coupled high-gain electronic voltage **amplifier** with a differential input and, usually, a single-ended output.

Bread Board Connection Diagram

Internal Wire Connection



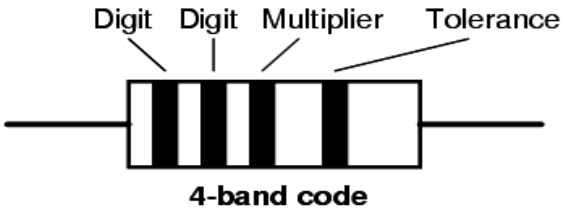
External Pin Connection

Standard Resistor Values and Color Coding

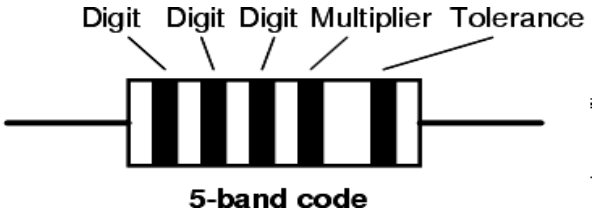
The standard resistor color code table:

Color	Digit 1	Digit 2	Digit 3*	Multiplier	Tolerance	Temp. Coef.	Fail Rate
Black	0	0	0	$\times 10^0$			
Brown	1	1	1	$\times 10^1$	±1% (F)	100 ppm/K	1%
Red	2	2	2	$\times 10^2$	±2% (G)	50 ppm/K	0.1%
Orange	3	3	3	$\times 10^3$		15 ppm/K	0.01%
Yellow	4	4	4	$\times 10^4$		25 ppm/K	0.001%
Green	5	5	5	$\times 10^5$	±0.5% (D)		
Blue	6	6	6	$\times 10^6$	±0.25% (C)		
Violet	7	7	7	$\times 10^7$	±0.1% (B)		
Gray	8	8	8	$\times 10^8$	±0.05% (A)		
White	9	9	9	$\times 10^9$			
Gold				$\times 0.1$	±5% (J)		
Silver				$\times 0.01$	±10% (K)		
None					±20% (M)		

** 3rd digit - only for 5-band resistors*



4-band code



5-band code

CIE MARKS SCHEME OF EVALUATION

Internal Examination (CIE) Marks: 50

Semester End Examination (SEE) Marks: 50

GENERAL PROCEDURE TO BE FOLLOWED BY THE STUDENT

Attendance	Minimum of 85% to be maintained. [Attendance at your regularly scheduled lab period is required. An unexpected absence will result in loss of credit for your lab. If for valid reason a student misses a lab, or makes a reasonable request in advance].
Punctuality	Late entry to the lab NOT permitted.
Dress Code	Should wear formal dress and shoe, No slippers.
Conduct	No eating or drinking is allowed. Unnecessary roaming around the lab to be avoided. Noise level is to be kept to the absolute minimum.
Safety	Students are to observe safety regulations at all times.
Equipment Usage	All mains and electrical equipment are to be switched off when not in use or when the lab session ends. Equipments need to handle smooth.
House Keeping	Students should keep their work station neat and clean.
Lab records	Record will be written individually. Please complete the cover Page and certificate page: Include your name, USN, Subject Code, subject Code, Semester, Academic year. Fill Inside pages with Experiment No., Date and Page No.
Hardware Laboratory Usage	Each laboratory station is equipped with a Power supply, CRO, Function generator, Digital Multi-meter, components and PCBs. Students work in groups of two, but maintain individual lab **Observation books** and submit individual **records**.

VTU SYLLABUS

ANALOG & DIGITAL SYSTEM DESIGN LABORATORY (BECL305)

CIE Marks 50	SEE Marks 50
Teaching Hours/Week (L:T: P: S)	0:0:2:0

Course objectives:

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the opamp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Study the static characteristics of SCR and test the RC triggering circuit.
- Design and test the combinational and sequential logic circuits for their functionalities.
- Use the suitable ICs based on the specifications and functions.

LABORATORY EXPERIMENTS

1. Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2. Design and set-up BJT/FET: i) Colpitts Oscillator, ii) Crystal Oscillator
3. Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator
4. Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4 bit binary input using toggle switches and (ii) by generating digital inputs using mod-16 counter.
5. Design and implement
   (a) Half Adder & Full Adder using basic gates and NAND gates,
   (b) Half subtractor & Full subtractor using NAND gates,
   (c) 4-variable function using IC74151(8:1MUX).
6. Realize
   (i) Binary to Gray code conversion & vice-versa (IC74139),
   (ii) BCD to Excess-3 code conversion and vice versa
7. (a) Realize using NAND Gates
   i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop
   (b) Realize the sift registers using IC7474/7495
   i) SISO ii) SIPO iii) PIPO iv) PISO v) Ring counter vi) Johnson counter
8. Realize
   (a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop
   (b) Mod-N Counter using IC7490 / 7476
   (c) Synchronous counter using IC74192

Demonstration Experiments

9. Design and Test the second order Active Filters and plot the frequency response,
    i) Low pass Filter
    ii) High pass Filter
10. Design and test the following using 555 timer
    i) Monostable Multivibrator
    ii) Astable Multivibrator
11. Design and Test a Regulated Power supply
12. Design and test an audio amplifier by connecting a microphone input and observe the output using a loud speaker.

- **Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

1. Design and analyze the BJT/FET amplifier and oscillator circuits.
2. Design and test op-amp circuits to realize the mathematical computations, DAC and precision rectifiers.
3. Design and test the combinational logic circuits for the given specifications.
4. Test the sequential logic circuits for the given functionality.

Demonstrate the basic electronic circuit experiments using SCR and 555 timer.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Suggested Learning Resources:

1. Fundamentals of Electronic Devices and Circuits Lab Manual, David A Bell, 5th Edition, 2009, Oxford University Press.
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition.

EXPERIMENT: 01:

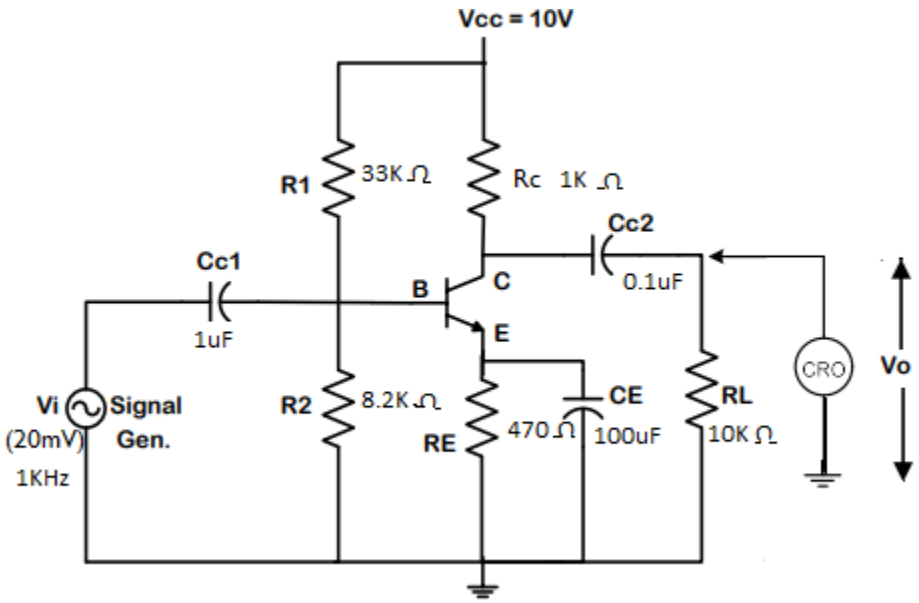
Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances

AIM: *To obtain the frequency response characteristics of a Current Series amplifier with and without feedback and Obtain the bandwidth.*

COMPONENTS REQUIRED :

Power supply 0-30V
CRO 20MHz 1No.
Signal generator 1-1MHz
Resistors 1kΩ, 4.7k, 8.2k, 2.2k, 33k,10K
Capacitors 10μF
Transistors SL100
Bread board CRO Probes

CIRCUIT DIAGRAM: BJT amplifier without feedback



DESIGN

Let V_{cc} = 12V ; I_C = 4mA ; V_E = 2V ; V_{CEQ} = 6V ; hfe (β_{DC}) = 100.

To find R_E :

Given V_E = 2V. Therefore, $R_E = V_E / I_E \approx V_E / I_C = 500\Omega$ **Let R_E = 470Ω** (standard)

To find R_C :

From the collector loop writing KVL we get

$V_{CC} = I_C R_C + V_{CE} + V_E$

$\therefore \quad R_C = (V_{CC} - V_{CE} - V_E) / I_C$

R_C = 1kΩ **R_C = 1kΩ** (standard)

To find R_1 and R_2 :

The base current $I_B = I_C / h_{fe}$ = 4mA / 100 = **0.04mA**

Let I_1 be current through R_1 and I_1 be 10 times of I_B

Writing the base loop KVL we get $V_B = V_E + V_{BE} = 2 + 0.7 = 2.7V$ **V_B = 2.7V**

Now, **$R1 = (V_{CC} - V_{B)} / I_1$**

R1 = (12 - 2.7)/0.4m = 23.25 kΩ **R1 = 33 kΩ** (standard)

Also **$R_2 = V_B / (I_1 - I_B)$**

R2 = 2.7/0.36m =7.5 kΩ **R2 = 8.2 kΩ** (standard)

Input impedance (Zin) :

In order to calculate the input impedance first calculate the value of **Zin** (base).

Zin (base) = $\beta r_e'$ where r_e' is the resistance of emitter diode.

$r_e \cong 25mV / I_C = 25mV / 4mA = 6.25\Omega$

Zin(base) = $\beta r_e' = 100 * 6.25 = 625\Omega$

The input impedance of an amplifier is the input impedance seen by the A.C. source driving the amplifier.

Therefore the biasing resistor R_1 and R_2 are included as follows $Z_{in} = (1+\beta r_e) \| R_1 \| R_2$ **Z_{in} = 558 kΩ**

Output impedance (Zo) :

The output impedance is given by $Zo = R_C \| R_L$

Let **R_L = 10 kΩ.** Therefore, **Zo = 909 Ω**

To find C_{C1} , C_{C2} and C_E :

Let **F_L = 100Hz** (Lower cut-off frequency)

Input coupling capacitor: $C_{C1} = 1 / (2*\pi*Z_{in}*F_L) = 1/(2*\pi*558*100) =$ **2.85 μF** **C_{C1} = 4.7 μF** (standard)

Output coupling capacitor: $C_{C2} = 1 / (2*\pi*(R_C + R_L)*F_{in}) = 1/(2*\pi*(1k + 10k)*100) = 0.144\mu F$

C_{C2} = **0.1μF** (standard)

Design of bypass capacitors: C_E

Emitter bypass capacitor $C_E = 1 / (2*\pi* r_e * F_L) = 1/(2*\pi* 6.25 * 100) = 254.6\mu F$ **C_E = 100μF** (standard)

PROCEDURE

1. *Rig up the circuit as per the given circuit diagram.*
2. *Switch on the D.C. power supply = 12V is given to the circuit.*
3. *Check the D.C. conditions without any input signal and record in table 1.*
4. *Select sine wave input and set the input signal amplitude to **20mV** frequency at **1kHz** constant, and observe the input / output waves on the CRO and adjust the input amplitude such that the output is undistorted waveform. Calculate mid-band gain using A_V = Vo(p-p) / Vin(p-p).*
5. *Keeping the input amplitude constant, vary the frequency from 100Hz to 2MHz and note down the corresponding output voltage (p-p) in the table 2.*
6. *Calculate gain in dB and plot the frequency response curve and find the bandwidth.*

[NOTE: The circuit with feedback = without bypass capacitor (C_E)
The circuit without feedback = with bypass capacitor]

OBSERVATIONS: Table 1 : **D.C. Conditions :**

Parameter	V_{RC}	V_{CE}	V_E	V_{BE}	V_B
Theoretical	4	6	2	0.7	2.7
Practical					

[NOTE: Use the tabular column separately for with and without feedback circuit]

Table 2: Frequency response with feedback **Vin (P-P) = 20mV**

Frequency Hz	Vo(p-p)	A_V = Vo(p-p) / Vin(p-p)	A_V (dB) = 20*log A_V	Frequency Hz	Vo(p-p)	A_V = Vo(p-p) / Vin(p-p)	A_V (dB) = 20*log A_V
100				50K			
200				100K			
300				300K			
500				500K			
700				600K			
1K				700K			
3K				800K			
5K				900K			
10K				1M			
20K				2M			

Measurement of Input Impedance

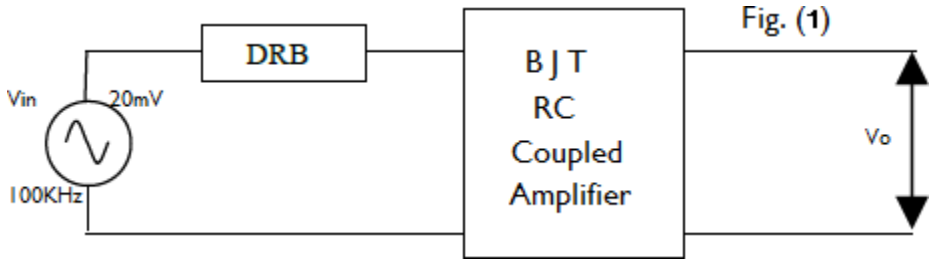
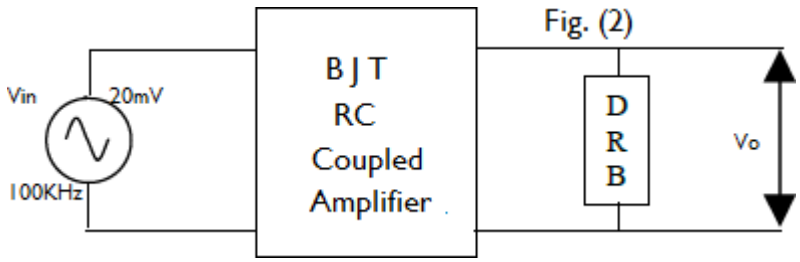


Fig. (1)

PROCEDURE

1) Connect the circuit of Fig(1).
2) Set the following: i) DRB to zero. ii) Input (Vin) sine wave amplitude of 20mV. iii) Input sine wave frequency to any mid band frequency (say,100 KHz).
3) Measure Vo(p-p).
4) Increase DRB till V_O = Vo(p-p)/2. The corresponding DRB value gives the input impedance Zi.

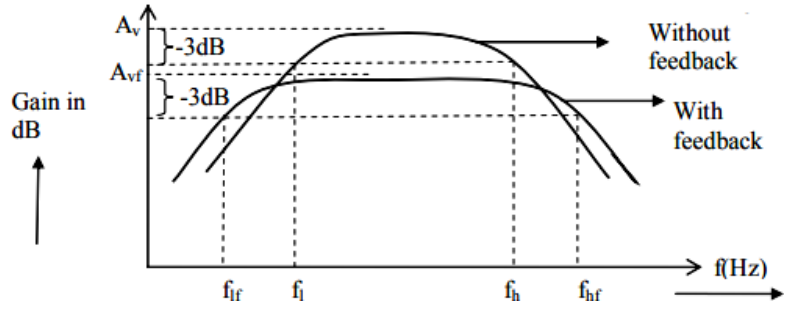
Measurement of Output Impedance



PROCEDURE

1) Connect as in Fig(2).
2) Set the following: i) DRB to maximum value ii) Input (Vin) sine wave amplitude to 20mV. iii) Input sine wave frequency to any mid band frequency (say, 100 KHz)
3) Measure Vo(p-p).
4) Decrease DRB till Vo = Vo(p-p)/2. The corresponding DRB value gives the output impedance Zo.

MODEL GRAPH :



Bandwidth= fl-fh

Results:

With C_E (Without feedback):	**Without C_E: (With feedback):**
Av (Mid-band) =.	Av (Mid-band) = ...
Bandwidth = ... Hz	Bandwidth = ... Hz
Input impedance =.....Ω	Input impedance =.....Ω
Output impedance =.....Ω	Output impedance =.....Ω

The RC-coupled amplifier was designed and rigged up and the parameters were found.

PRECAUTIONS: 1. Connections must be made with proper polarity.
2. Avoid loose and wrong connections.

EXPERIMENT: 02

Design and set-up of Colpitt's, Crystal Oscillator and RC Phase shift Oscillator using BJT

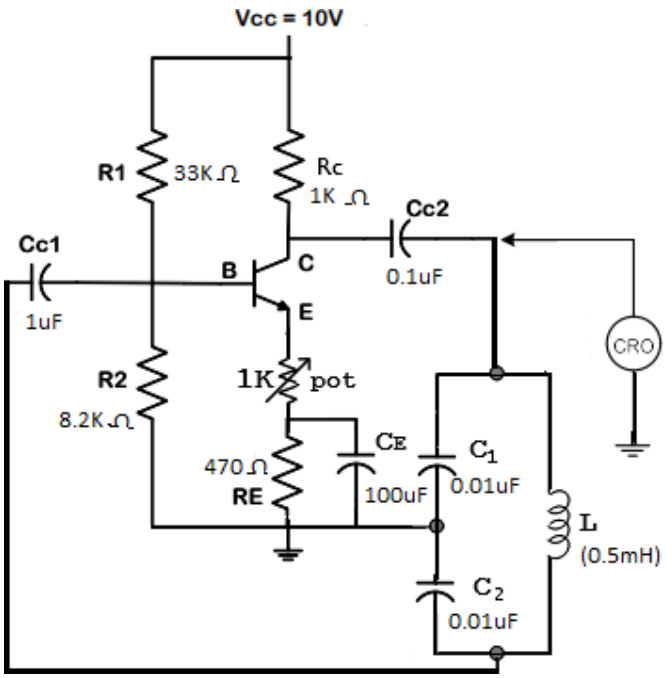
COLPITT'S OSCILLATOR

Aim: *Design and set-up the Colpitt's oscillator to determine the frequency of oscillation f_o=100KHz Using BJT*

Components and equipments required:

Transistor SL 100,
Resistors 470Ω, 1KΩ 10KΩ and 33 KΩ;
Capacitors 0.1μf - 3nos,
Discrete inductances 100 μH – 2 nos,
Capacitor 470 pF – 2nos, Power supply, CRO,
Connecting wires

CIRCUIT DIAGRAM: Colpitt's Oscillator



DESIGN:

Let V_{cc} = 12V ; I_C = 4mA ; V_E = 2V ; V_{CEQ} = 6V ; hfe (β_{DC}) = 100.

To find R_E :

Given V_E = 2V. Therefore, $R_E = V_E / I_E \approx V_E / I_C = 500\Omega$ **Let R_E = 470Ω** (standard)

To find R_C :

From the collector loop writing KVL we get

$V_{CC} = I_C R_C + V_{CE} + V_E$

$\therefore \quad R_C = (V_{CC} - V_{CE} - V_E) / I_C$

R_C = 1kΩ **R_C = 1kΩ** (standard)

To find R_1 and R_2 :

The base current $I_B = I_C / h_{fe}$ = 4mA / 100 = **0.04mA**

Let I_1 be current through R_1 and I_1 be 10 times of I_B

Writing the base loop KVL we get $V_B = V_E + V_{BE} = 2 + 0.7 = 2.7V$ **V_B = 2.7V**

Now, **$R1 = (V_{CC} - V_B) / I_1$**

R1 = (12 - 2.7)/0.4m = 23.25 kΩ **R1 = 33 kΩ** (standard)

Also **$R_2 = V_B / (I_1 - I_B)$**

R2 = 2.7/0.36m =7.5 kΩ **R2 = 8.2 kΩ** (standard)

To find C_{C1} , C_{C2} and C_E :

Let **F_L = 100Hz** (Lower cut-off frequency)

Input coupling capacitor: $C_{C1} = 1 / (2*\pi*Z_{in}*F_L) = 1/(2*\pi*558*100) =$**2.85 μF** **$C_{C1}$ = 4.7 μF** (standard)

Output coupling capacitor: $C_{C2} = 1 / (2*\pi*(R_C + R_L)*F_{in}) = 1/(2*\pi*(1k + 10k)*100) =$ 0.144**μF**

C_{C2} = **0.1μF** (standard)

Design of bypass capacitors: C_E

Emitter bypass capacitor $C_E = 1 / (2*\pi* r_e * F_L) = 1/(2*\pi* 6.25 * 100)$=254.6μF

C_E =100μF (standard)

Tank circuit design

Frequency of oscillation for Colpitt's oscillator is

$$f_0 = \frac{1}{2\pi\sqrt{L \times Ceq}} \qquad \text{where } Ceq = \frac{C_1 C_2}{C_1 + C_2}$$

let $C_1 = C_2 = 0.01\mu F$. $\therefore Ceq = \dfrac{(0.01)(0.01)10^{-12}}{(0.02)10^{-6}}$

$$\boxed{Ceq = 0.005\,\mu F}$$

We have f_0 =100kHz, Then $L = \dfrac{1}{4\pi^2 f_0^2 Ceq}$

$$L = \frac{1}{4\,\pi^2(10000)(10^3)^2 * 0.005 * 10^{-6}} = 5.06 \times 10^{-4}\,H \quad \boxed{L = 0.506mH}$$

PROCEDURE

1. Switch on the Power Supply and check the D.C conditions.

2. Check for the sinusoidal waveform at output. If the output is distorted adjust 1KΩ Potentiometer to get perfect SINE wave.

3. Measure the period (T) of oscillation and calculate the frequency (f_o) of oscillation.

4. Compare the measured frequency with re-computed theoretical value for the component values connected.

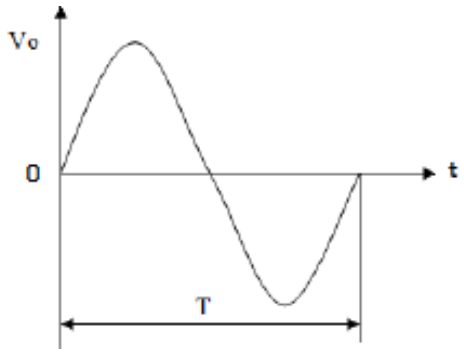
Observation:

Parameter	V_{RC}	V_{CE}	V_E	$I_{CQ} = V_{RC} / R_C$	V_{BE}	V_B
Theoretical	4.8V	6 V	1.2V	4.5 mA	0.6 V	1.8 V
Practical						

TABULATION

Sl.No.	Inductance (L) Henry	CAPACITANCE μF			Theoretical $f_0 = \frac{1}{2\pi\sqrt{L \times Ceq}}$	T sec	f_o=1/T Hz	Amplitude Volts
		C1	C2	C_{eq}				
1								
2								
3								

Model Graph:



Result: Performance of the Colpitt's oscillators is tested.

Theoretical frequency F_0 = 100KHz.

Practical frequency $F_0 = \frac{1}{T}$ = _____kHz

Aim: *Design and set-up the crystal oscillator and determine the frequency of oscillation.*

Components and equipments required:

Transistor SL 100,
Crystal – 2MHz,
Resistors 470Ω, 1KΩ 10KΩ and 33 KΩ;
Capacitors 0.1μf - 2nos,
Power supply, CRO, Connecting wires

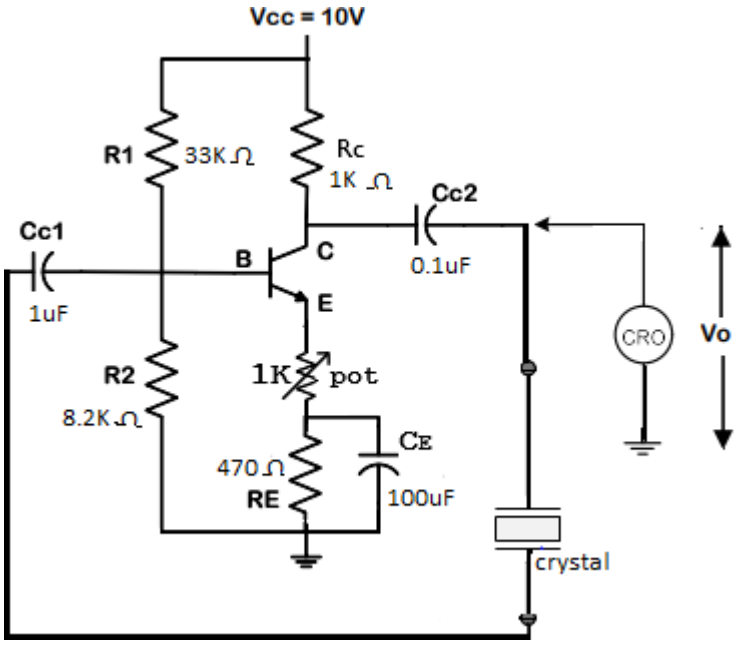
Theory: Crystal oscillators are used in order to get stable sinusoidal signals despite of variations in temperature, humidity, transistor and circuit parameters. A piezo electric crystal is used in this oscillator as resonant tank circuit. Crystal works under the principal of piezo-electric effect. i.e., when an AC signal applied across the crystal, it vibrates at the frequency of the applied voltage. Conversely if the crystal is forced to vibrate it will generate an AC signal. Commonly used crystals are Quartz, Rochelle salt etc.

(Design of amplifier using BJT is same as Colpitt's oscillator excluding feedback circuit)

PROCEDURE

1. Switch on the Power Supply and check the D.C conditions.
2. Check for the sinusoidal waveform at output. If the output is distorted adjust 1KΩ Potentiometer to get perfect SINE wave.
3. Measure the period (T) of oscillation and calculate the frequency (f_o) of oscillation.
4. Compare the measured frequency with re-computed theoretical value for the component values connected.

CIRCUIT DIAGRAM : Crystal Oscillator



Observation:

Parameter	V_{RC}	V_{CE}	V_E	$I_{CQ} = V_{RC} / R_C$	V_{BE}	V_B
Theoretical	4.8V	6 V	1.2V	4.5 mA	0.6 V	1.8 V
Practical						

Result: Performance of the Crystal oscillators is tested.

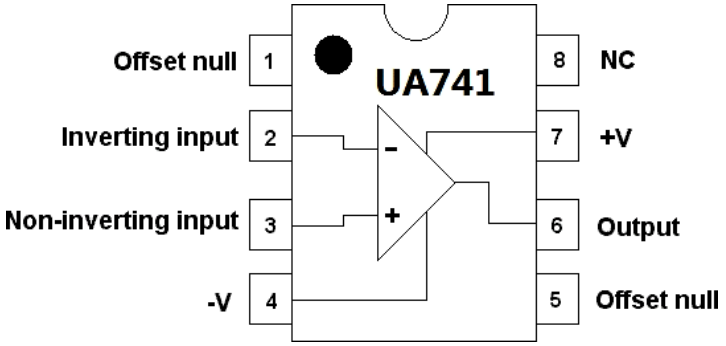
Theoretical frequency F_0 = 2 MHz.

Practical frequency $F_0 = \frac{1}{T}$ = _____kHz

EXPERIMENT: 03:

Design Adder, Integrator, Differentiator and comparator circuits using Op-Amp

PIN DIGRAM of OPAMP:



Aim:

i) Design an adder circuit using opamp and verify
ii) Design a differentiator circuit using opamp and verify
iii) Design an integrator circuit using opamp and verify
iv) Design an comparator circuit using opamp and verify

Components Rquired:

1. IC 741
2. Resistors as per design
3. Function generator
4. Regulated power supply
5. IC bread board trainer
6. CRO / Patch cards / CRO probes

THEORY:

ADDER: Op-amp can be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or an adder. Summing amplifier can be classified as inverting & non- inverting summer depending on the input applied to inverting & non-inverting terminals respectively. Circuit Diagram shows an inverting summing amplifier with 2 inputs. Here the output will be amplified version of the sum of the two input voltages with 180^0 phase reversal.

Differentiator: It is an opamp circuit which performs the mathematical operation of differentiation. That is the output waveform is the derivative or differentia l of the input voltage. That is $Vo = - R_fC\ d(V_{in})/dt$. The differentiator circuit is constructed from basic inverting amplifier by replacing the input resistance Ri with capacitor C. This circuit also works as high pass filter.

Integrator: It is a closed loop op-amp circuit which performs the mathematical operation of integration. That is the output waveform is the integral of the input voltage and is given by $Vo = (-1/RfC) \int V_{in}dt$. The integrator circuit is constructed from basic inverting amplifier by replacing the feedback resistance Rf with capacitor C. This circuit also works as low pass filter.

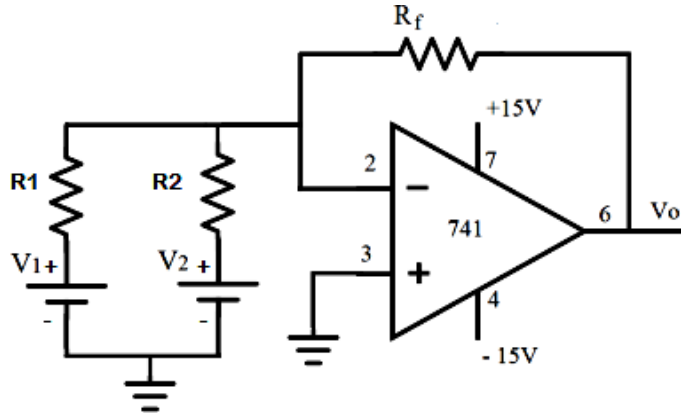
Comparator: A voltage comparator is a two-input circuit that compares the voltage at one input to the voltage at the other input. Usually one input is a reference voltage and the other input a time varying signal. If the time varying input is below or above the reference voltage, then the comparator provides a low or high output accordingly (usually the plus or minus power supply voltages, since the op-amp is used in the open loop configuration, a small difference (−) makes the output to saturate).

Design an adder circuit using opamp and verify

Design: $V_o = -R_F \left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right]$ if $R_1 = R_2 = R_F = R$

$V_o = -(V_1+V_2)$ ≡ output voltage is proportional to the algebraic sum of the input voltages, V_1, V_2

CIRCUIT DIGRAM: ADDER



PROCEDURE

Summing/Adder Amplifier:

1. Connections are made as per the circuit diagram.
2. Input DC voltages V1 and V2 are given and the corresponding output voltage Vo is measured from Multi-meter or CRO.
3. Output varies as Vo = - (V1 + V2), since $R_F = R$.

TABULATION

Sl.No	R1 Ω	R2 Ω	R_F Ω	V1 volts	V2 volts	$V_o = -R_F \left[\frac{V_1}{R_1} + \frac{V_2}{R_2}\right]$ volts	Vo (practical) volts
1	1K	1K	1K	1	2		
2	1K	3.3K	2.2K	1	2		

Differentiator

$\mathbf{V_{out} = -R_f C \{dV_{in} / dt\}}$

The output V_{out} is R_f C times the differentiation of the input voltage.
The product $\mathbf{R_f C}$ is called as the RC time constant

Integrator

$$V_{out} = -\frac{1}{CR_{in}} \int V_{in}\, dt$$

The output V_{out} is CR_{in} times the integration of the input voltage V_{in}.
The product $\mathbf{CR_{in}}$ is called as the RC time constant

Design:

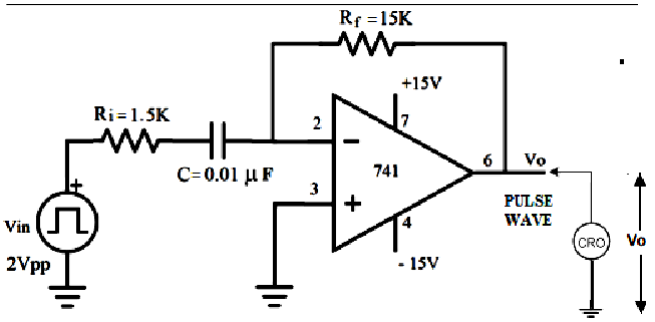
Given f = 1 KHz, sothat, T = 1/f = 1ms
Design equation is $T = 2\pi R_f C$
Let C = 0.01μF
Then, R_f = 15KΩ
Let Ri = Rf/10 = 1.5KΩ

Design:

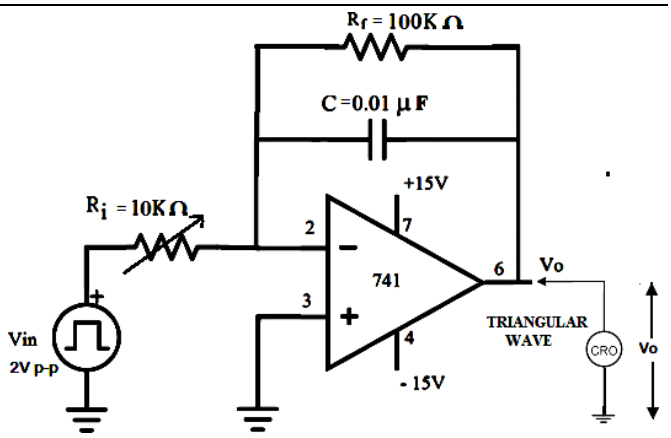
Given f =1 KHz So T = 1/f = 1ms
Design equation is $T = 2\pi RiC$
Let C = 0.01μF
Then Ri = 10KΩ Take $R_f = 10Ri$ = 100KΩ

EX: Given V_p = 1 V and f = 1K Hz,
input voltage is Vi = V_p sin ωt
We know ω = 2πf
Hence Vo = - R_f C (dVi /dt) = - 0.94 cosωt

CIRCIUT DIAGRAM



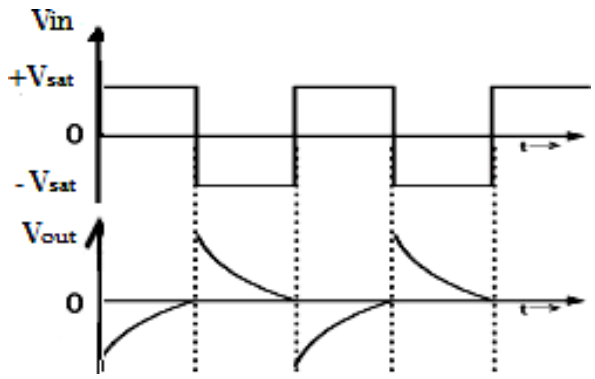
CIRCIUT DIAGRAM



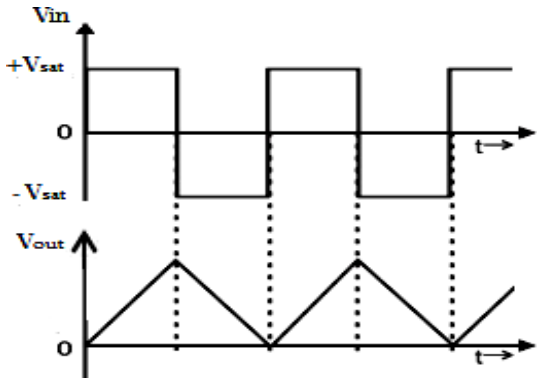
Tabulation

Type of circuit ↓	Input Square wave		Output Wave	
	Amplitude	Time period	Amplitude	Time period
Differentiator				
Integrator				

Expected Waveforms (Differentiator)



(Integrator)



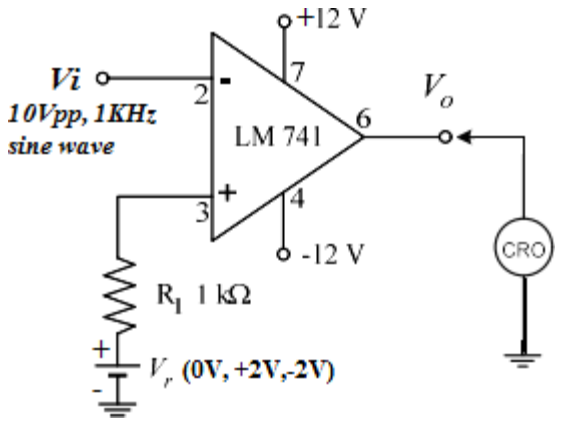
PROCEDURE

Differentiator/ Integrator:

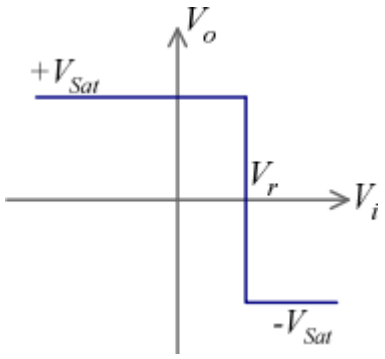
1. Connections are made as per the circuit diagram.
2. A square wave/ triangle wave of 4V (p-p) and frequency of 1KHZ from function generator is applied to the inverting terminal (2) as input.
3. Using both channels of CRO, observe and record the corresponding amplitude and time period for input/output for the frequencies of 500 Hz and 1kHz.
4. With the above data plot the output graphs with time on X-axis and voltage on Y-axis. Compare this with the Equations given above.

COMPARATOR

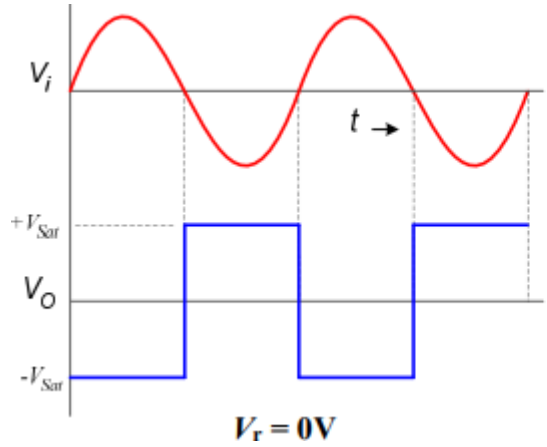
Circuit diagram



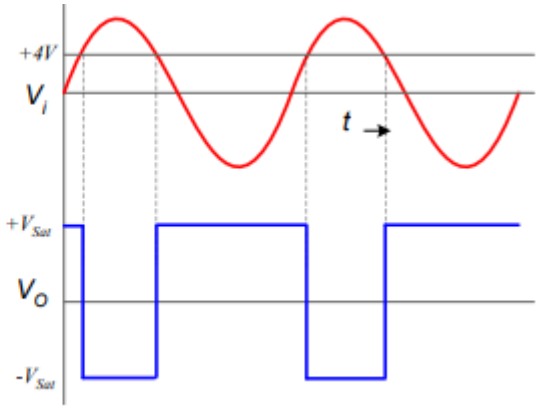
Transfer characteristics



Expected Waveforms



$V_r = 0V$



$V_r = +4V$

PROCEDURE

1. Set up the circuit as shown in the diagram.
2. Set the input voltage 10 V peak to peak, 1 kHz in function generator, and apply this as input signal to the circuit. Observe the output waveform in CRO.
3. Obtain the response for different V_r (say, V_r = 0V,±2V). Also, obtain the transfer characteristics.

RESULT: Theoretical and practical output values for adder and input/output waveforms/values of integrator, differentiator and comparator are observed using opamp.

Viva questions	4. Define slew rate.
1. What are the ideal characteristics of an OP-AMP?	5. What are the applications of differentiator?
2. Define OP-AMP.	6. What are the applications of integrator?
3. What do you mean by CMRR?	7. What is a difference between inverting and non-inverting amplifier?

EXPERIMENT: 04

4-Bit R-2R Digital to Analog Converter

(i) Using 4 bit binary input from toggle switches

Aim : *To design 4 bit R-2R ladder DAC using Op-Amp for an output & reference voltage of 5 V.*

Apparatus :

1.	IC	µA741
2.	Resistors	As per design
3.	Multimeter	-
4.	Base board + connecting wires	-

Theory:

What is DAC? Digital to analog converter (DAC) is used to get analog voltage corresponding to an input digital data. Data in binary digital form can be converted to corresponding analog form by using a R-2R ladder (binary weighted resistor) network and a summing amplifier. It is more common and practical. Below is the circuit and output simulated waveform of R-2R ladder network DAC. This circuit also uses an op amp (741) summing amplifier circuit.

The resolution of the converter will be equal to the value of the least significant bit (LSB) which is given as:

$$Resolution = V_{LSB} = -\frac{V_{ref}}{2^n}$$

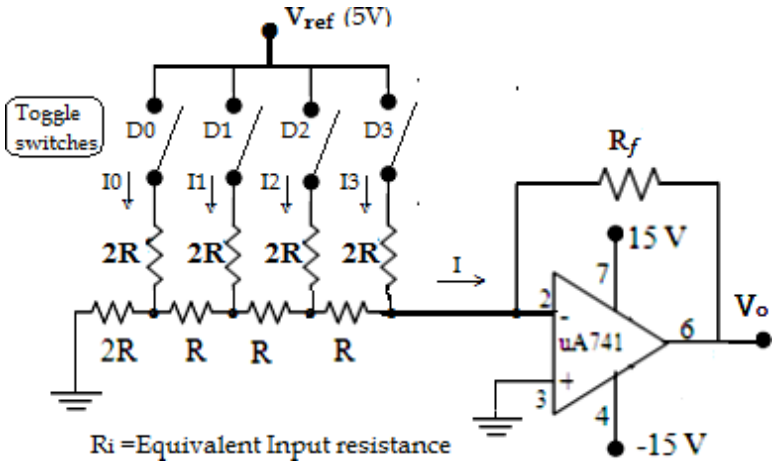
$$\text{For } 4-\text{bit DAC}, \quad V_{ref} = 5\text{V}, \quad \text{n} = 4, \quad Resolution = V_{LSB} = -\frac{5}{16} = -0.3125V$$

Then the smallest step change of the analogue output voltage, V_{OUT} for a 1-bit LSB change of the digital input of this 4-bit R-2R digital-to-analogue converter example is: 0.3125 volts. That is the output voltage changes in steps or increments of 0.3125 volts and not as a straight linear value.

DESIGN

To design a 4 bit R-2R DAC for an output voltage, V_o = 5V, let R_i = input equivalent resistance of the ladder network, R_F = feedback resistance.

From the circuit diagram, $\mathbf{I_{out} = I_0+I_1+I_2+I_3}$ (using KCL), then finding each current terms from Ohm's law


Vref (5V)
Toggle switches
D0
D1
D2
D3
I0
I1
I2
I3
2R
2R
2R
2R
2R
R
R
R
I
Rf
15 V
7
2
6
Vo
uA741
3
4
-15 V
Ri =Equivalent Input resistance

$$I_{out} = \left(\frac{V_{ref}}{2R}\right)D_3 + \left(\frac{V_{ref}}{2R}\right)D_2 + \left(\frac{V_{ref}}{2R}\right)D_1 + \left(\frac{V_{ref}}{2R}\right)D_0$$

$$I_{out} = \left(\frac{V_{ref}}{R}\right)\left[\frac{D_3}{2} + \frac{D_2}{4} + \frac{D_1}{8} + \frac{D_0}{16}\right]$$

$R = R_i =$ input equivalent resistance $\qquad I_{out} = -\left(\frac{V_{out}}{R_F}\right) \quad or \quad V_{out} = I_{out} \cdot R_F$

Therefore, above equation becomes, $\frac{V_{out}}{R_F} = -\frac{V_{ref}}{16R_i}[8D_3 + 4D_2 + 2D_1 + D_0]$

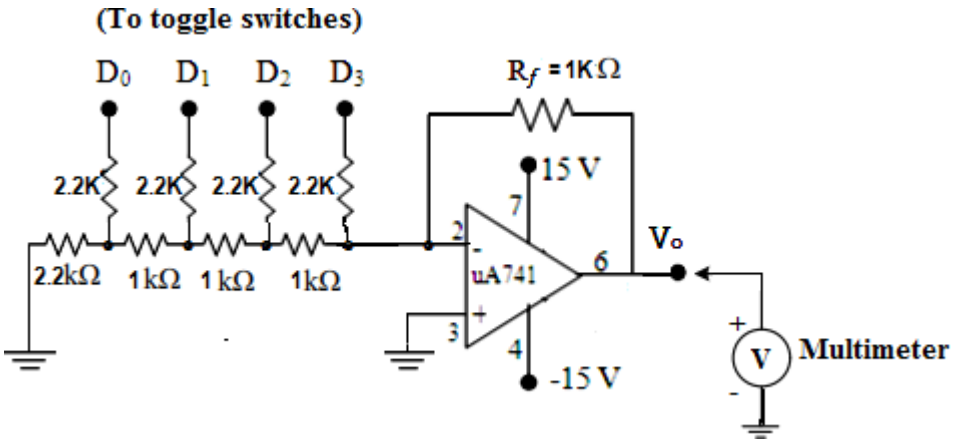
If $R_i = R_F = 1K\Omega$

$$V_{out} = -\frac{V_{ref}}{16}[8D_3 + 4D_2 + 2D_1 + D_0]$$

For example, $(1010)_2 = (10)_{10}$ is applied from toggle switches then,

D3 = 1 (MSB), D2 = 0, D1 = 1, D0 = 0 (LSB) and V_{ref} =5V, **V_{out} = -3.125V**

CIRCUIT DIAGRAM



PROCEDURE

1. Connections are made as shown in the circuit diagram.
2. Digital input data is given at D3, D2, D1, D0 and corresponding analog output voltage V0 is measured using millimeter.
3. *Compare practical and theoretical values of analog output voltage corresponding to binary input combination and find the error value.*
3. Tabulate the readings & plot the graph between V_o on y-axis V_{in} on X-axis.

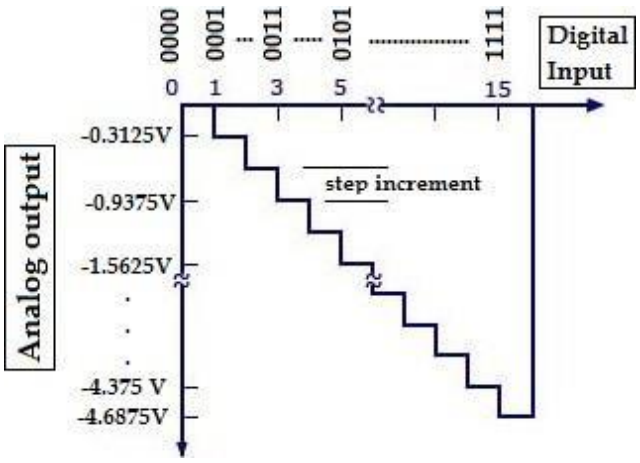
NOTE :

1. D0, D1, D2 & D3 are binary inputs (digital) applied from toggle switches.
2. V_o is the analog output.
3. Binary inputs Do, D1, D2 & D3 can take either the value '0' or '1' (Logic 0 → 0 Logic 1 → +5V).
4. Binary input Di (i = 0 to 3) can be made '0' by connecting the i/p to ground. It can be made '1' by connecting to +5 V.

TABULATION

Decimal Value	Binary inputs (switches)				Analog $V_{(Practical)}$ volts (X)	Analog $V_{(Theoretical)}$volts (Y)	Error X-Y
	D3	D2	D1	D0			
0	0	0	0	0			
1	0	0	0	1			
2	0	0	1	0			
3	0	0	1	1			
4	0	1	0	0			
5	0	1	0	1			
6	0	1	1	0			
7	0	1	1	1			
8	1	0	0	0			
9	1	0	0	1			
10	1	0	1	0			
11	1	0	1	1			
12	1	1	0	0			
13	1	1	0	1			
14	1	1	1	0			
15	1	1	1	1			

Ideal 4-bit R-2R DAC Transfer Characteristics



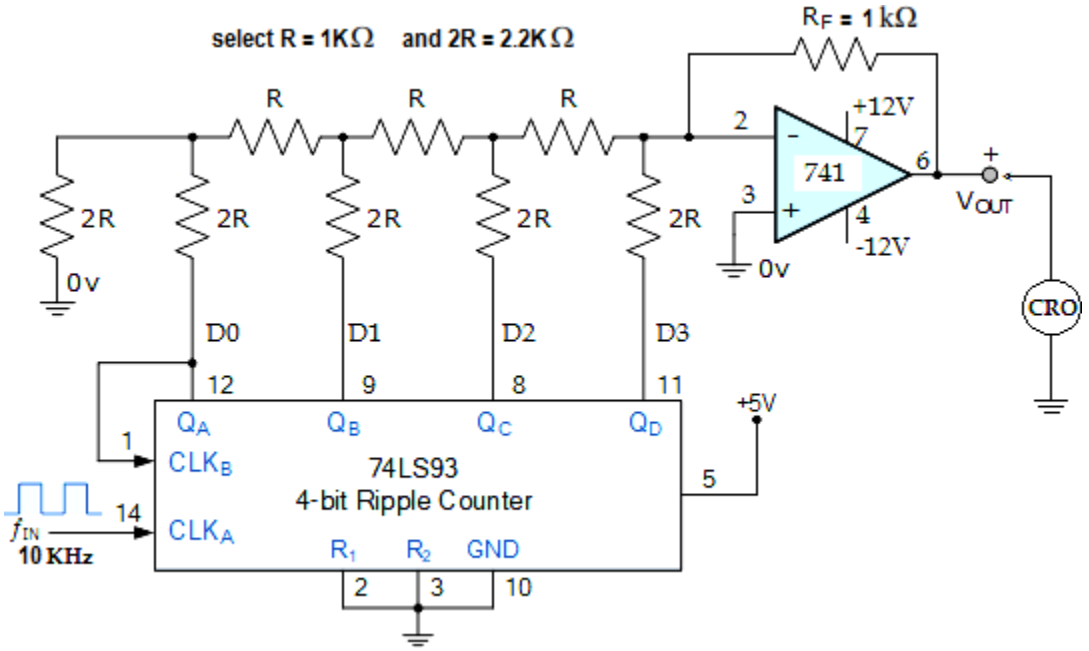
(ii) by generating digital inputs using mod-16 counter

Components Required:

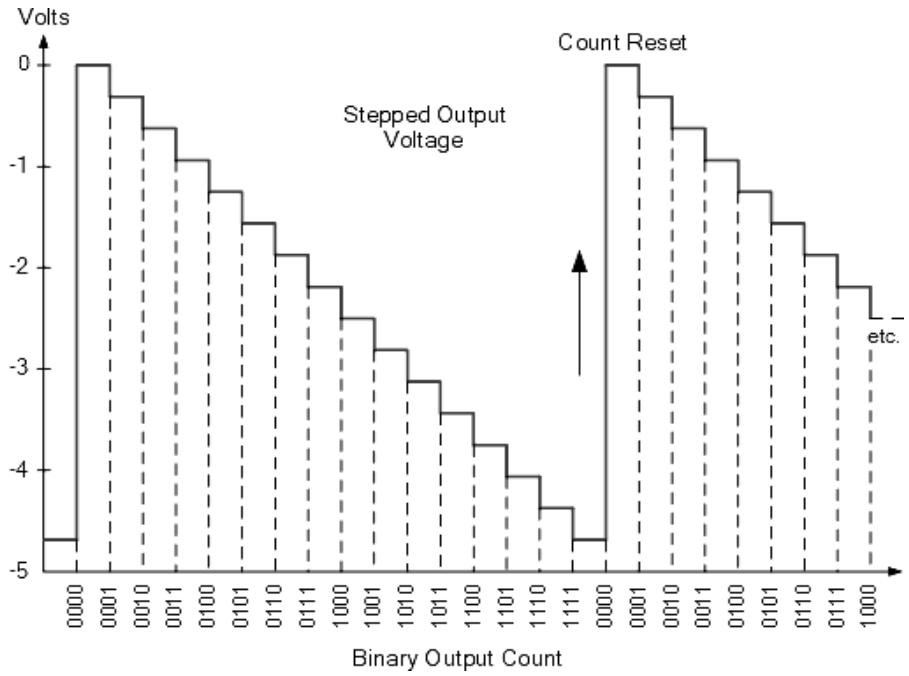
1. Resistors (1KΩx4, 2KΩx5)
2. 741 Op Amp
3. 7493 Counter IC

In this circuit the **IC 7493** is a counter simply it provides digital binary inputs (0000 to 1111) to OPAMP inputs $D_3D_2D_1D_0$ and observe & note down the display on CRO screen.

CIRCUIT DIAGRAM



Model Graph



RESULT: 4 bit R-2R DAC is verified using toggle switches and counter IC 7493.

EXPERIMENT NO 5
ADDERS/SUBTRACTORS/MULTIPLEXER

AIM: Design and implement

(a) Half Adder & Full Adder using basic gates and NAND gates
(b) Half subtractor & Full subtractor using NAND gates
(c) 4-variable function using IC74151(8:1MUX).

5(a) Half Adder & Full Adder using basic gates and NAND gates

COMPONENTS REQUIRED:

Sl.No.	Components	Quantity
1	IC 7400	3
2	IC 7408	1
3	IC 7486	1
4	IC 7432	1
5	Patch Chords	20 - 30
6	IC Trainer Kit	1

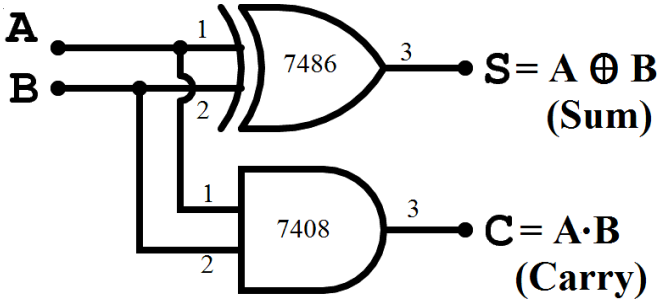
THEORY:

Half-Adder: A combinational logic circuit that performs the addition of two data bits, A and B, is called a half-adder. Addition will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, C. The Boolean functions describing the half-adder are:

$S = A \oplus B$ $C = A\,B$

Full-Adder: The half-adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds two data bits, A and B, and a carry-in bit, Cin, is called a full-adder. The Boolean functions describing the full-adder are:
$S = (x \oplus y) \oplus Cin$ $C = xy + Cin\,(x \oplus y)$

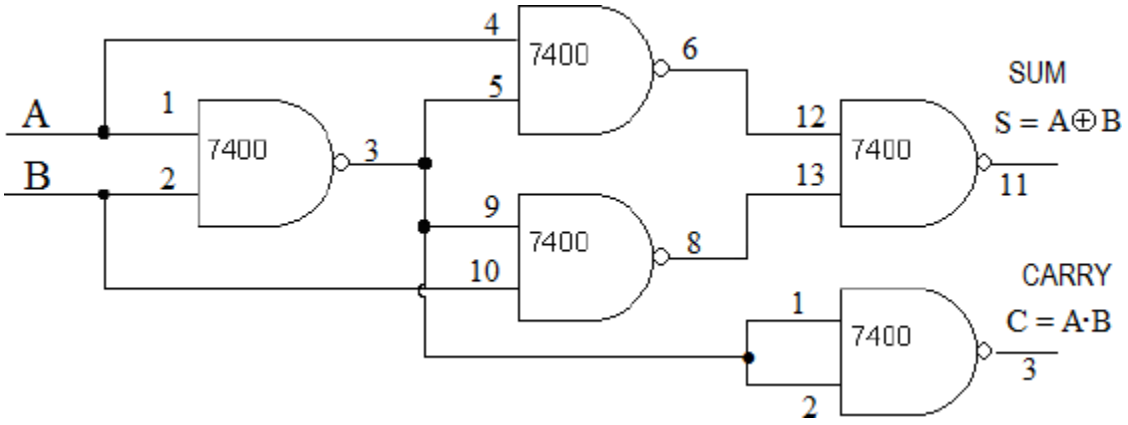
HALF ADDER USING BASIC GATES



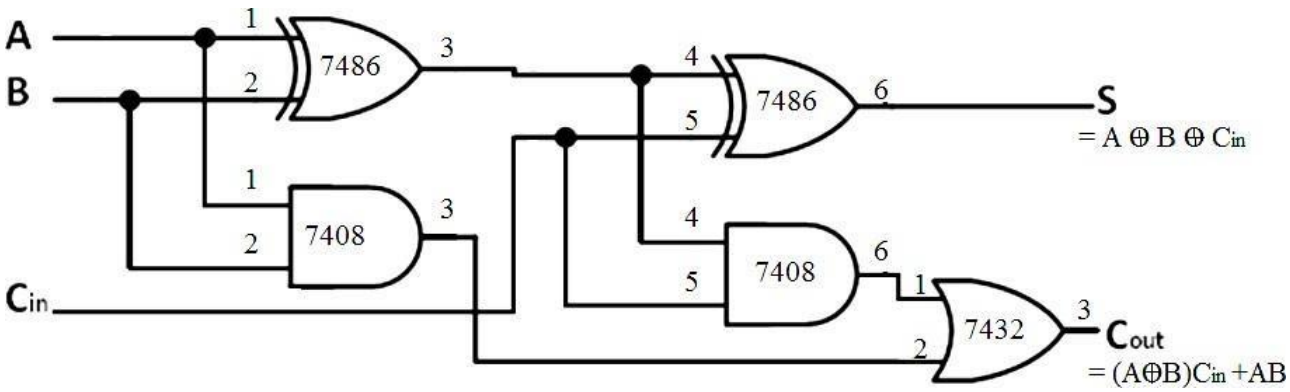
TRUTH TABLE

Inputs		Outputs	
A	B	Sum(S)	Carry©
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

HALF ADDER USING NAND GATES ONLY



FULL ADDER CIRCUIT USING BASIC GATES



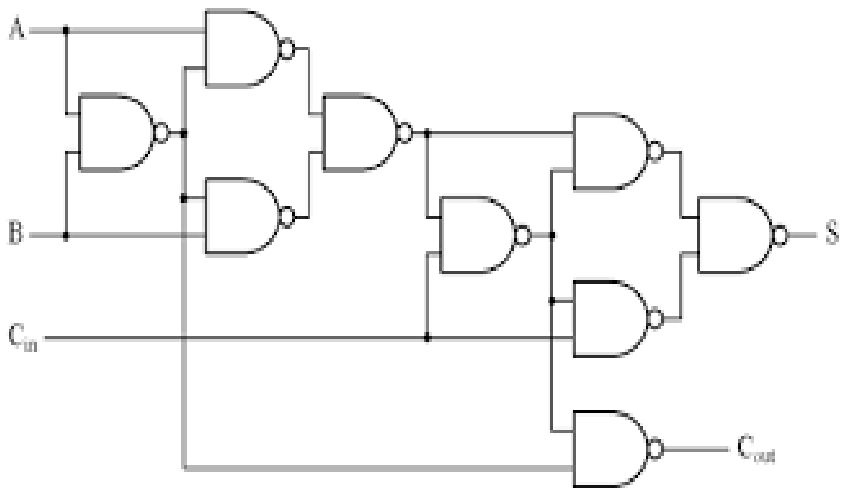
TRUTH TABLE

Inputs			Outputs	
A	**B**	**C_{in}**	**Sum (S)**	**Carry (C_{out})**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\text{Sum} = A \oplus B \oplus C_{in}$$

$$\text{Carry} = (A \oplus B)C_{in} + AB$$

FULL ADDER CIRCUIT USING NAND GATES ONLY



PROCEDURE

1. Verify the all gates according to respective truth tables.

2. Make the connections as per the circuit diagram.

3. Switch on VCC and apply various combinations of input according to the truth table.

4. Note down the output readings for half and full adder sum and the carry bit for different combinations of inputs.

RESULT: *Half adder, Full adder using basic/NAND gates are verified.*

5(b) Half subtractor & Full subtractor using NAND gates

Half Subtractor: Subtracting a single-bit binary value B from another A (i.e. A –B) produces a difference bit D and a borrow out bit B-out. This operation is called half subtraction and the circuit to realize it is called a half subtractor. The Boolean functions describing the half Subtractor are:

$$D = A \oplus B \qquad Br = A' B$$

Full Subtractor: Subtracting two single-bit binary values, B, Cin from a single-bit value A produces a difference bit D and a borrow out Br bit. This is called full subtraction. The Boolean functions describing the full-subtracter are:

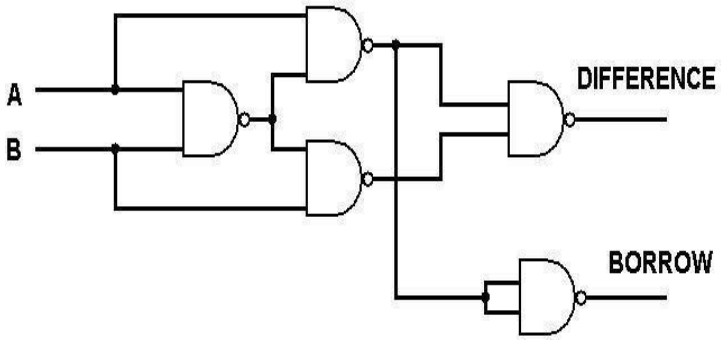
$$D = (A \oplus B) \oplus Cin$$

$$Br = A'B + A' (Cin) + B (Cin)$$

COMPONENTS REQUIRED:

Sl.No.	Components	Quantity
1	IC 7400	3
2	Patch Chords	20 - 30
3	IC Trainer Kit	1

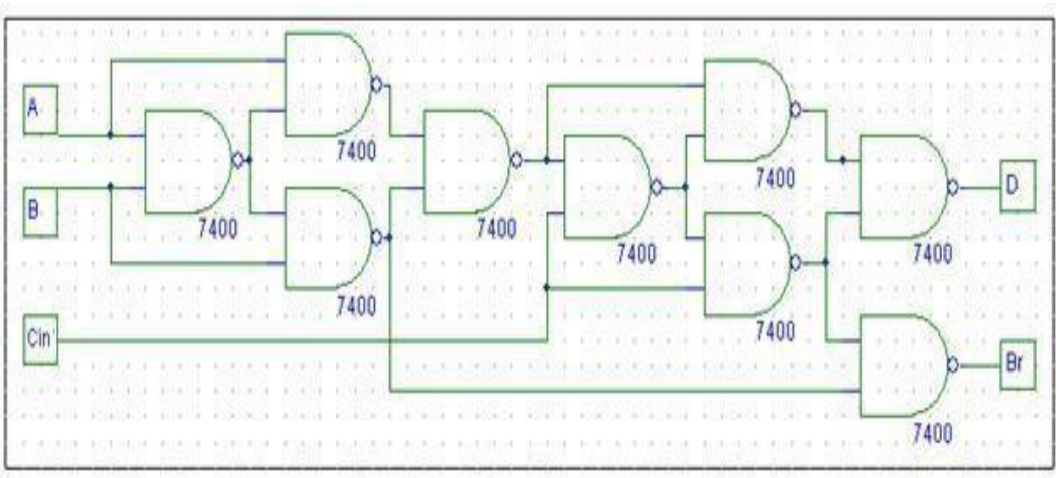
HALF SUBTRACTOR USING NAND GATES ONLY



TRUTH TABLE

Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

FULL SUBTRACTOR USING NAND ONLY



TRUTH TABLE

A	B	Bin	D	Br
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

PROCEDURE

5. Verify the all gates according to respective truth tables.

6. Make the connections as per the circuit diagram.

7. Switch on VCC and apply various combinations of input according to the truth table.

8. Note down the output readings for half and full adder sum and the carry bit for different combinations of inputs.

RESULT: *Half subtractor and Full subtractor using NAND gates are verified.*

4 VARIABLE FUNCTION USING IC 74151

5(c) 4-variable function using IC74151(8:1MUX).

AIM: *To Realize the 4 variable function using IC 74151 (8:1 Multiplexer).*

COMPONENTS REQUIRED:

Sl.No.	Components	Quantity
1	IC 74151	1
2	IC 7404	1
3	Patch Chords	20 - 30
4	IC Trainer Kit	1

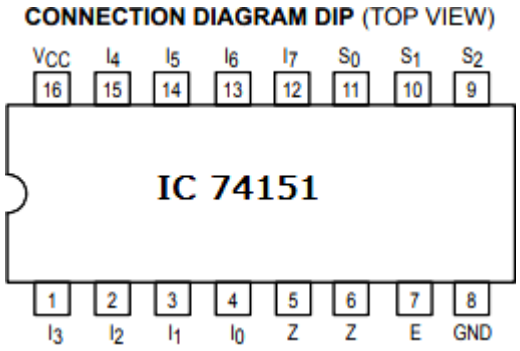
THEORY

The TTL/MSI SN54/74LS151 is a high speed 8:1 digital multiplexer. It provides, in one DIP package, the ability to select one bit of data from 8 data inputs. The LS151 can be used as a universal function generator to generate any logic function of 4 variables.

Basic multiplexer has several data inputs and a single output line. The selection of a particular input line is controlled by a set of selection line. There are 2^n input lines & n is the number of selection line whose bit combinations determines which input is selected.

Example: S2 S1 S0 = 010 code which corresponds to D2 input data line. Now apply D2 =0/1, this data 0/1 is transmitted to Y.

The given function is in terms of min-terms and is to be implemented using a 8:1 MUX. An 8:1 MUX has three select lines, whereas the given function is a 4 variable function. Hence, a logic is needed to give combination of A as inputs while only B, C and D as select line inputs. The method for the same is described below.



Design Example: To implement the following function: F(A,B,C,D) = Σ (0,1,3,4,8,9,15).

Step-1: Using K-map Boolean terms are determined for the variable A as shown below.

	D0	D1	D2	D3	D4	D5	D6	D7
Ā	(0)	(1)	2	(3)	(4)	5	6	7
A	(8)	(9)	10	11	12	13	14	(15)
	1	1	0	Ā	Ā	0	0	A

Step-2: Construct digital circuit for the given 4 variable function F(A,B,C,D) = Σ (0,1,3,4,8,9,15), such that a logic is needed to give combination of A as inputs (1, 1, 0, Ā, Ā, 0, 0, A) while only B, C and D as select line inputs.

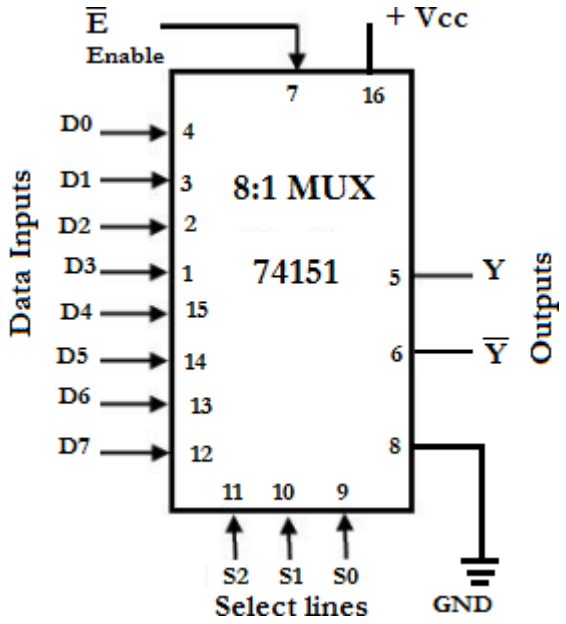


Fig.(a) Basic pin Description of IC 74151

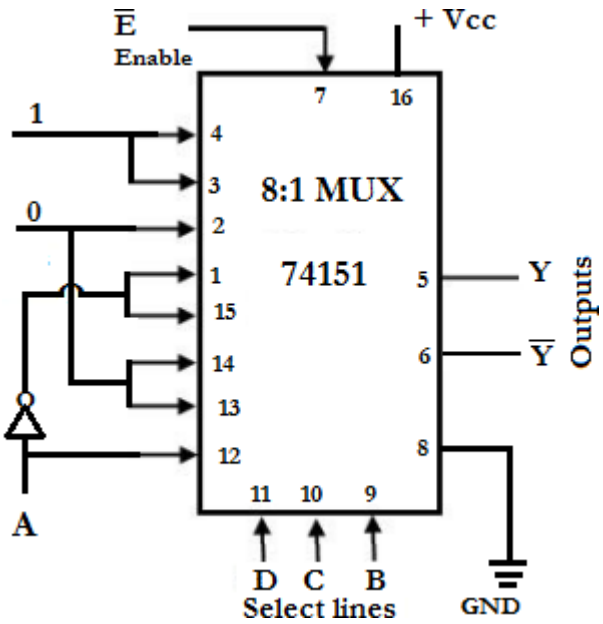


Fig. (b) IC74151 designed for F(A,B,C,D) = Σ (0,1,3,4,8,9,15)

Step-3: Connect the circuit as shown in the fig. (b) and verify the following truth table.

A	B	C	D	Enable	Decimal	Y = F(A,B,C,D)
0	0	0	0	0	**0**	1
0	0	0	1	0	**1**	1
0	0	1	0	0	2	0
0	0	1	1	0	**3**	1
0	1	0	0	0	**4**	1
0	1	0	1	0	5	0
0	1	1	0	0	6	0
0	1	1	1	0	7	0
1	0	0	0	0	**8**	1
1	0	0	1	0	**9**	1
1	0	1	0	0	10	0
1	0	1	1	0	11	0
1	1	0	0	0	12	0
1	1	0	1	0	13	0
1	1	1	0	0	14	0
1	1	1	1	0	**15**	**1**

Result: *4 variable function $F(A,B,C,D) = \Sigma(0,1,3,4,8,9,15)$ using IC 74151 (8:1 Multiplexer) is realized.*

EXPERIMENT: 06
Binary to Gray code conversion & vice versa (IC 74139)

Aim: *To realize binary to gray code conversion and vice versa using IC74139 (2-4 Decoder).*

COMPONENTS REQUIRED:

Sl.No.	Components	Quantity
1	IC 74139	1
2	IC 7404	1
3	IC 7420	1
4	Patch Chords	20 - 30
5	IC Trainer Kit	1

THEORY:

The logical circuit which converts binary code to equivalent gray code is known as binary to gray code converter. The gray code is a non-weighted code. The successive gray code differs in one bit position only that means it is a unit distance code. It is also referred as cyclic code. It is not suitable for arithmetic operations. It is the most popular of the unit distance codes. It is also a reflective code. An n-bit Gray code can be obtained by reflecting an n-1 bit code about an axis after 2^n-1 rows, and putting the MSB of 0 above the axis and the MSB of 1 below the axis.

Binary to gray code conversion

Following steps are required in this conversion:

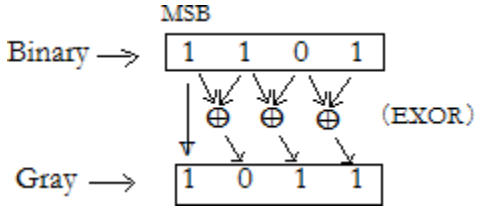
(1) The MSB of the gray code is equal to MSB of binary number.

(2) Second bit of the gray code will be exclusive-or of the first and second bit of the given binary number.

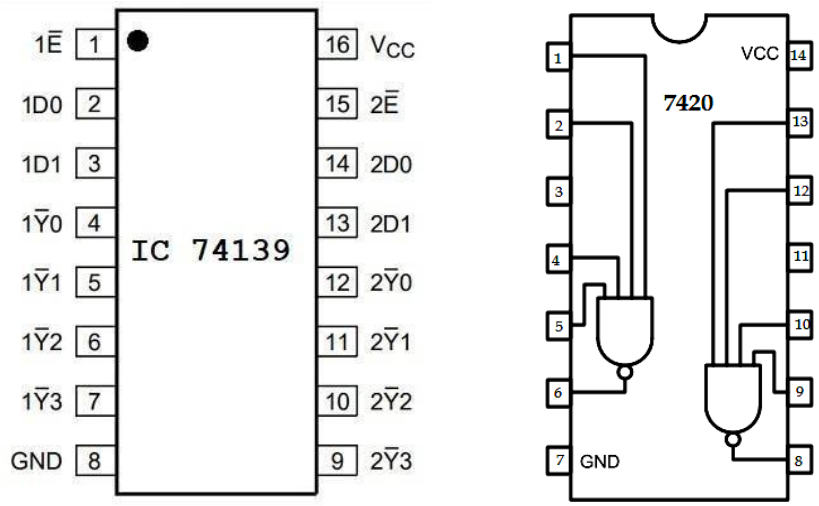
(3) The third bit of gray code will be equal to the exclusive -or of the second and third bit of the given binary number.

Thus the Binary to gray code conversion goes on.

One example given below can make your idea clear on this type of conversion.



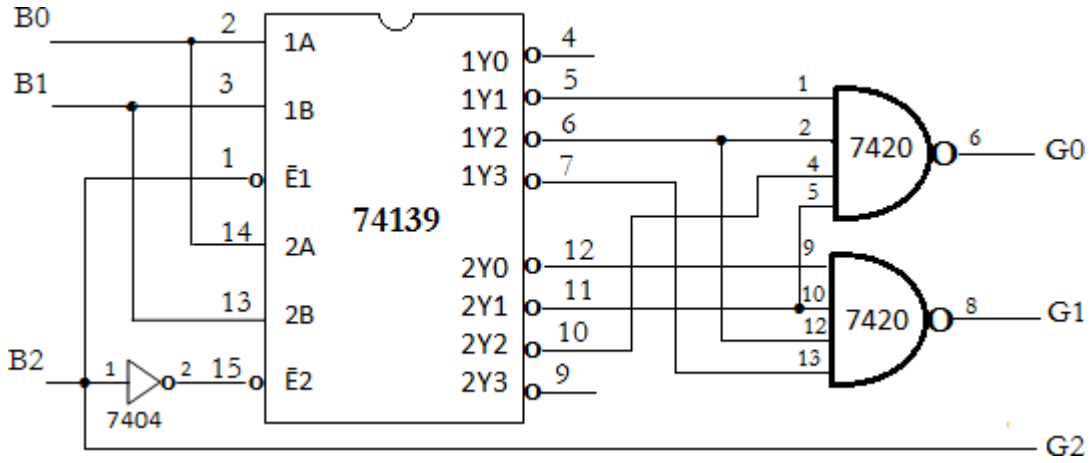
PIN DIAGRAMS



Truth Table: Binary to Gray conversion

Decimal	Binary (Input) B2 B1 B0	Gray (Output) G2 G1 G0	Conversion operation	Min-terms
0	0 0 0	0 0 0	G2 = B2 G1 = B1 ⊕ B2 G0 = B1 ⊕B0	$G_0 = \Sigma (1,2,5,6)$
1	0 0 1	0 0 1		
2	0 1 0	0 1 1		
3	0 1 1	0 1 0		$G_1 = \Sigma (2,3,4,5)$
4	1 0 0	1 1 0		
5	1 0 1	1 1 1		
6	1 1 0	1 0 1		$G_2 = \Sigma (4,5,6,7)$
7	1 1 1	1 0 0		

CIRCUIT DIAGRAM

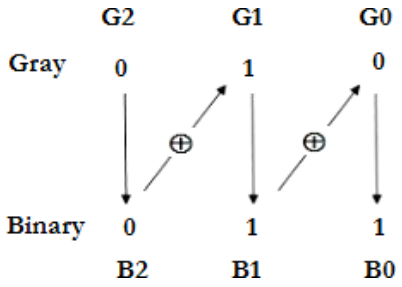


Gray code to binary conversion

Following steps are required in this conversion:

1) The MSB of the binary number will be equal to the MSB of the given gray code.
2) Start with MSB of Binary number and EXOR it to the second bit of gray number to get next bit of binary.
3) This step is continued for all the bits to do Gray code to binary conversion.

One example given below can make your idea clear on this type of conversion

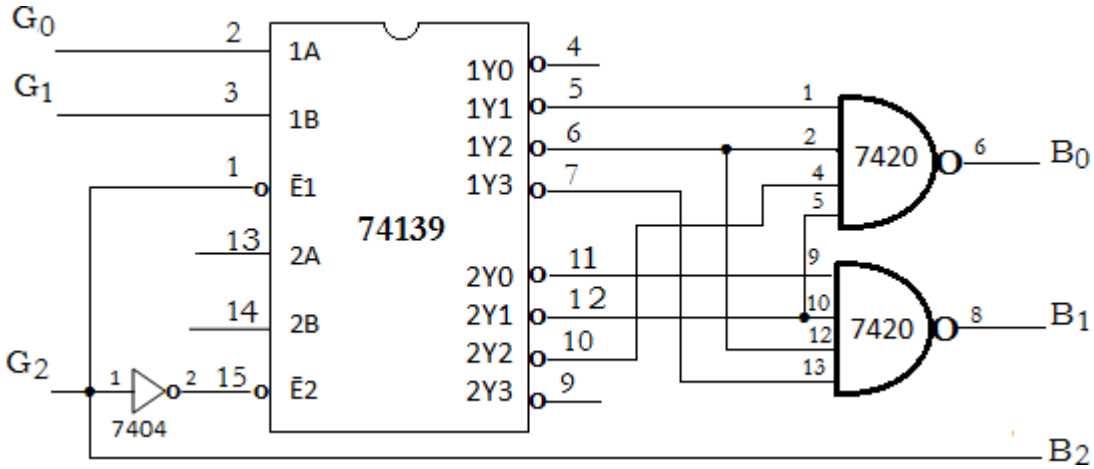


$$B_2 = G_2$$
$$B_1 = G_2 \oplus G_1$$
$$B_0 = G_2 \oplus G_1 \oplus G_0$$
$$(\oplus \Rightarrow Ex - Or\ Operation)$$

Truth Table: Binary to Gray conversion

Decimal	Gray (Input) G2 G1 G0	Binary (Output) B2 B1 B0	Conversion operation	Min-terms
0	0 0 0	0 0 0	$B_2 = G_2$ $B_1 = G_2 \oplus G_1$ $B_0 = G_2 \oplus G_1 \oplus G_0$	$B_0 = \Sigma (1,2,4,7)$
1	0 0 1	0 0 1		
2	0 1 1	0 1 0		
3	0 1 0	0 1 1		$B_1 = \Sigma (2,3,4,5)$
4	1 1 0	1 0 0		
5	1 1 1	1 0 1		
6	1 0 1	1 1 0		$B_2 = \Sigma (4,5,6,7)$
7	1 0 0	1 1 1		

CIRCUIT DIAGRAM



PROCEDURE

1) *Check all the components for their working.*
2) *Insert the appropriate IC into the IC base.*
3) *Make connections as shown in the circuit diagram.*
4) *Verify the Truth Table and observe the outputs.*

BCD TO EXCESS-3 CODE CONVERSION AND VICE VERSA

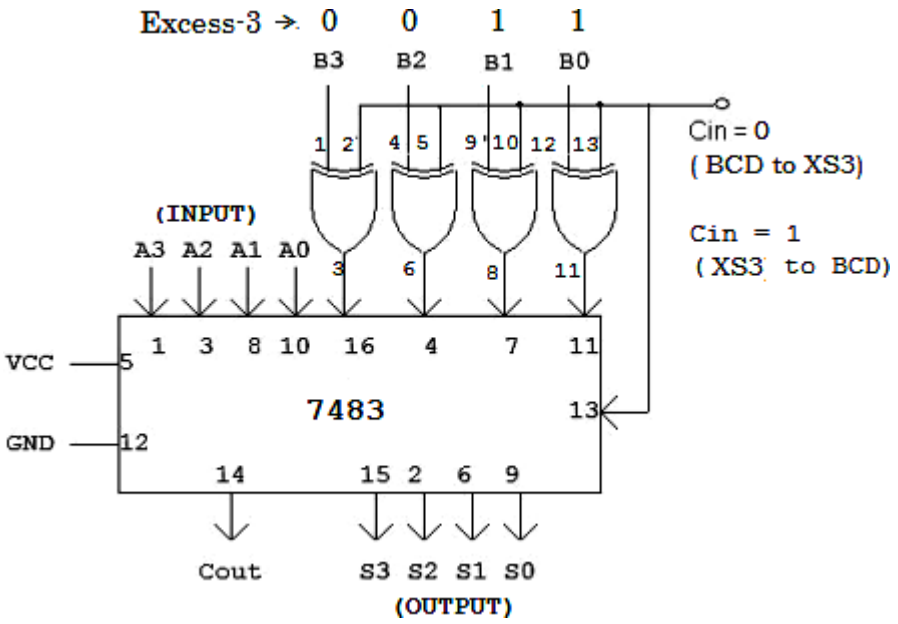
AIM: *To realize BCD to Excess-3 code conversion and vise versa using IC 7483*

COMPONENTS REQUIRED:

Sl.No.	Components	Quantity
1	IC 7486	1
2	IC 7483	1
3	Patch Chords	20
4	IC Trainer Kit	1

THEORY

Code converter is a combinational circuit that translates the input code word into a new corresponding word. In this code each decimal digit is represented by a 4 -bit binary number. BCD is a way to express each of the decimal digits with a binary code. In the BCD, with four bits we can represent sixteen numbers



(0000 to 1111). But in BCD code only first ten of these are used (0000 to 1001). The remaining six code combinations i.e. 1010 to 1111 are invalid in BCD.

To Construct a BCD-to-excess-3-code converter with a 4-bit adder feed BCD code to the 4- bit adder as the first operand and then feed constant 3 (0011) as the second operand. The output is the corresponding excess-3 code. To make it work as a excess-3 to BCD converter, we feed excess-3 code as the first operand and then feed 2's complement of 3 as the second operand. The output is the BCD code.

Excess-3 Code - It is non-weighted code used to express decimal numbers. The Excess -3 code words are derived from the 8421 BCD code words adding $(0011)_2$ or $(3)_{10}$ to each code word in 8421.

CIRCUIT DIAGRAM: BCD to EXCESS -3 / EXCESS -3 to BCD Conversion

NOTE: Neglect C_{out} in the circuit

TRUTH TABLES

BCD to EXCESS-3 code

BCD (input)				BCD code word	Excess -3 (output)			
B3	B2	B1	B0		E3	E2	E1	E0
0	0	0	0	0	0	0	1	1
0	0	0	1	1	0	1	0	0
0	0	1	0	2	0	1	0	1
0	0	1	1	3	0	1	1	0
0	1	0	0	4	0	1	1	1
0	1	0	1	5	1	0	0	0
0	1	1	0	6	1	0	0	1
0	1	1	1	7	1	0	1	0
1	0	0	0	8	1	0	1	1
1	0	0	1	9	1	1	0	0

EXCESS-3 to BCD code

Excess -3 (input)				BCD code word	BCD code (output)			
E3	E2	E1	E0		B3	B2	B1	B0
0	0	1	1	0	0	0	0	0
0	1	0	0	1	0	0	0	1
0	1	0	1	2	0	0	1	0
0	1	1	0	3	0	0	1	1
0	1	1	1	4	0	1	0	0
1	0	0	0	5	0	1	0	1
1	0	0	1	6	0	1	1	0
1	0	1	0	7	0	1	1	1
1	0	1	1	8	1	0	0	0
1	1	0	0	9	1	0	0	1

PROCEDURE

1) *Check all the components for their working.*
2) *Insert the appropriate IC into the IC base.*
3) *Make connections as shown in the circuit diagram.*
4) *Verify the Truth Table and observe the outputs.*

RESULT: *BCD to Excess-3 code conversion and vise versa using IC 7483 are realized.*

EXPERIMENT: 7
Realize Master Slave JK Flipflop, D-Flipflop & T-Flipflop Using NAND Gates

AIM: *To realize Master Slave JK flip-flop, D-flip-flop & T-flip-flop using NAND gates*

COMPONENTS REQUIRED:

Sl.No.	Components	Quantity
1	IC 7400	3
2	IC 7410	1
3	Patch Chords	20
4	IC Trainer Kit	1

THEORY

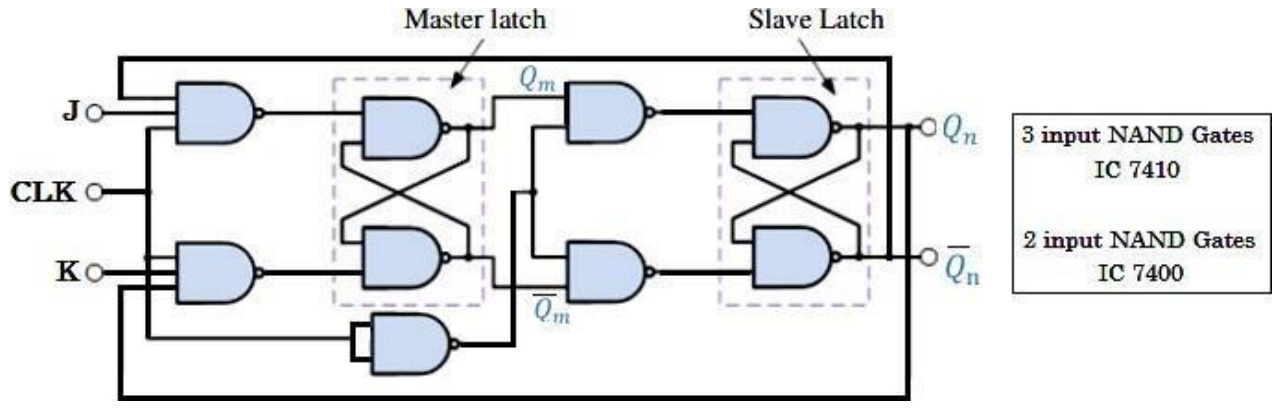
Flip-Flops are binary cells capable of storing one bit of information. A Flip Flop has two outputs, one for the normal value and one for complement value of the bit stored in it.

JK FLIP-FLOP is basically an SR flip flop with feedback which enables only one of its two input terminals, either SET or RESET to be active at any one time under normal switching thereby eliminating the invalid condition of SR flip flop. However, if J = K = 1 and clock input is applied the circuit will "toggle" as its outputs switch and change state complementing each other. This timing problem called "race". The *master-slave flip- flop* eliminates all the timing problems by using two SR flip-flops connected together in a series configuration. One flip-flop acts as the "Master" circuit, which triggers on the leading edge of the clock pulse while the other acts as the "Slave" circuit, which triggers on the falling edge of the clock pulse. This results in the two sections, the master section and the slave section being enabled during opposite half-cycles of the clock signal.

D FLIP-FLOP: It has only one data input (D) and clock input (CP). The outputs are labeled Q and Q'. The data (0 or 1) at the input 0 is delayed one clock pulse from getting to output Q. SD and CD are active low input (Negative edge trigger) to set and reset the Flip-Flop i.e. these inputs will be effective when logic 0 is applied. A D Flip-flop is a bi-stable circuit whose 0 input is transferred to the output after a clock pulse is received.

T FLIP-FLOP This T Flip-Flop is obtained from a JK type if both inputs are tied together. The designation T shows ability of Flip-Flop to toggle. Regardless of the present state of the Flip-Flop, it assumes the complement state when the clock pulse occurs while input T is logic1. When T=0, both AND gates are disabled and hence there is no change in the previous output. When T=1, (J=K=1) output toggles.

CIRCUIT DIAGRAM FOR MASTER SLAVE JK FF



FUNCTION TABLE

CP	J	K	Q_m	$\bar{Q}_m$	Q_n	$\bar{Q}_n$
0→1	0	0	Hold		Hold	
1→0	0	0	Hold		Hold	
0→1	0	1	0	1	Hold	
1→0	0	1	Hold		0	1
0→1	1	0	1	0	Hold	
1→0	1	0	Hold		1	0
0→1	1	1	Toggle		Hold	
1→0	1	1	Hold		Toggle	

T FLIP-FLOP:

The T flip-flop is a single input version of the JK flip-flop. The T flip-flop is obtained from the JK type if both inputs are tied together.

CIRCUIT DIAGRAM: Same as Master-Slave JK flip-flop with J = K = 1

Till CLK = 0, the output is in hold state (three input AND gate principle).

When CLK = 1, for T=0, previous output is memorized by the circuit.

When T = 1 along with the clock pulse, the output toggles from the previous value as given in the characteristic table below.

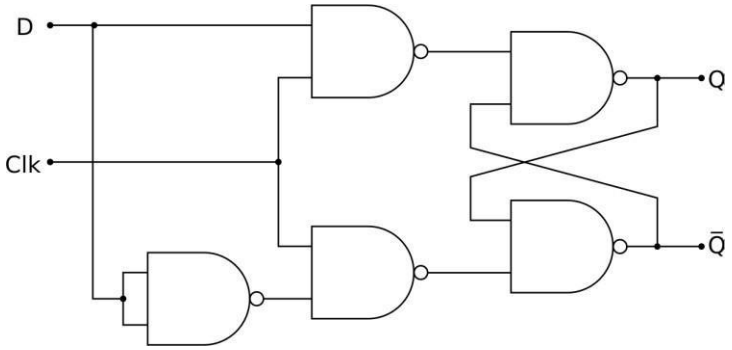
Truth Table

Clock	T	Output Q	Output $\bar{Q}$
0 →1	0	Q	$\bar{Q}$
0 →1	1	$\bar{Q}$	Q
1 →0	X	Q	$\bar{Q}$

D FLIP-FLOP

D flip-flop is a controlled Bi-stable latch where the clock signal is the control signal. when **D = 1 and CLOCK = HIGH,** Output : Q = 1, $\bar{Q}$ = 0. Working is correct.

CIRCUIT DIAGRAM



Truth Table

Clock	D	Output Q	Output $\bar{Q}$
0 →1	0	0	1
0 →1	1	1	0
1 →0	X	Q	$\bar{Q}$

PROCEDURE

1) *Turn on power to the circuit.*
2) *For each input combination, note the logic state of the normal (Q) and complementary ($\bar{Q}$) outputs as indicated by the LEDs (ON = 1; OFF = 0), and record the results in a table.*
3) *Compare your results with the truth tables.*

RESULT: *Master Slave JK flip-flop, D-flip-flop & T-flip-flop using NAND gates are verified.*

SHIFT REGISTERS

AIM: *To realize different types of shift registers Serial In Serial Out [SISO], Serial In Parallel Out [SIPO], Parallel In Parallel Out [PIPO] and Parallel In Serial Out [PISO] using IC 7495 and to verify function table.*

COMPONENTS REQUIRED:

Sl.No.	Components	Quantity
1	IC 7495	1
2	IC 7404	1
3	Patch Chords	20
4	IC Trainer Kit	1

THEORY

The binary information (data) in a register can be moved within or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers. They are very important in applications involving the storage and transfer of data in a digital system.

Types of shift registers:

Serial In Serial Out [SISO]:

In this type of register, the output of one flip-flop is connected to the input of the next flip-flop. Output of the register is obtained from the last flip-flop. Depending on the direction of the input given shifting takes place in this. Bit by bit loading and shifting takes place with every clock pulse.

Serial In Parallel Out [SIPO]:

This is similar to SISO except that the output is taken from each flip-flop. Thereby the shifted value is shown at once.

Parallel In Parallel Out [PIPO]:

Upon giving clock pulse, data is loaded in parallel in all flip-flops. Output is taken from each of the flip-flop.

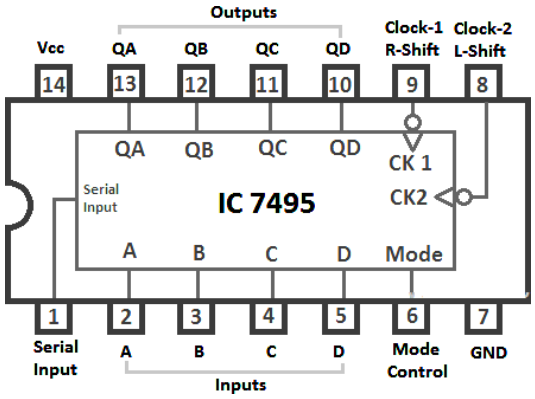
Parallel In Serial Out [PISO]:

Here we use a control input Load/ (Shift) such that if Load/ (Shift) = 1, data is loaded in all flip-flops in parallel and when the Load/ (Shift) = 0, data is shifted with every clock pulse. Output is obtained from the last flip-flop.

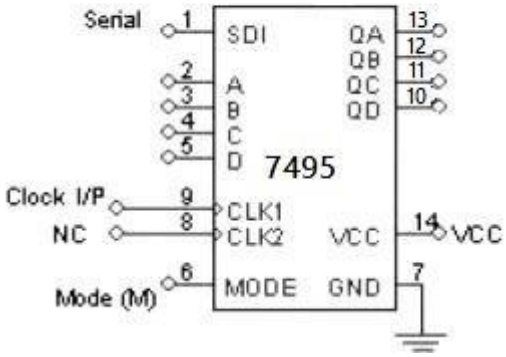
3 Modes of Operation of IC 7495: Parallel, Shift right and Shift Left

Parallel	Serial
Mode control = 1	Mode control = 0
Clock 2	Clock-1

Pin Diagram of IC 7495



SIPO (Right Shift)



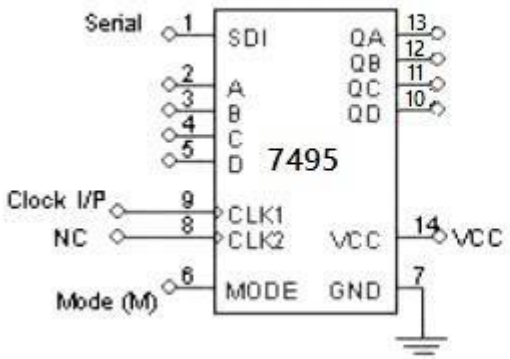
SIPO Function Table

Clock	Serial i/p	QA	QB	QC	QD
1	0	0	X	X	X
2	1	1	0	X	X
3	1	1	1	0	X
4	1	1	1	1	0

PROCEDURE

1. *Connections are made as per circuit diagram.*
2. *Apply the data at serial i/p (pin-1)*
3. *Apply one clock pulse at clock 1 (Right Shift) observe this data at QA.*
4. *Apply the next data at serial i/p.*
5. *Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new data applied will appear at QA.*
6. *Repeat steps 2 and 3 till all the 4 bits data are entered one by one into the shift register.*

SISO (Right Shift)



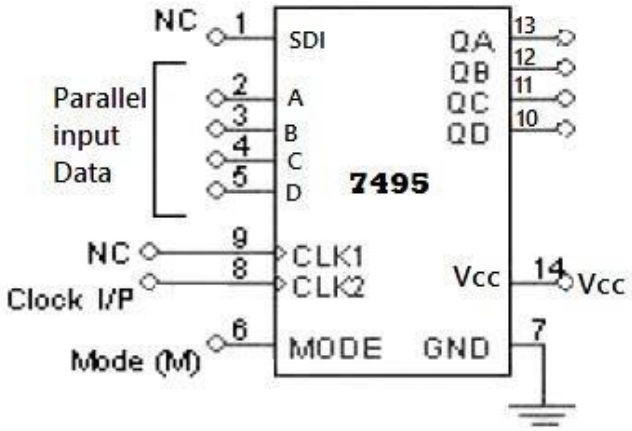
SISO Function Table

Clock	Serial i/p	QA	QB	QC	QD
1	do=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=do
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2
7	X	X	X	X	1=d3

PROCEDURE

1. Connections are made as per circuit diagram.
2. Load the shift register with 4 bits of data one by one serially.
3. At the end of 4th clock pulse the first data 'd0' appears at QD.
4. Apply 5th clock pulse; the second data 'd1' appears at QD.
5. Apply 6th clock pulse; the third data appears at QD.
6. Application of next clock pulse will enable the 4th data 'd3' to appear at QD.
Thus the data applied serially at the input comes out serially at QD.

PISO:-



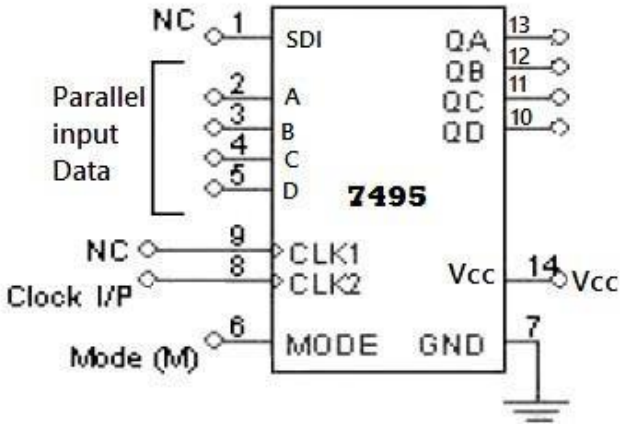
PISO Function Table

Mode	Clock	Parallel i/p				Parallel o/p			
		A	B	C	D	QA	QB	QC	QD
1	1	1	0	1	1	1	0	1	1
0	2	X	X	X	X	X	1	0	1
0	3	X	X	X	X	X	X	1	0
0	4	X	X	X	X	X	X	X	1

PROCEDURE

1. Connections are made as per circuit diagram.
2. Apply the desired 4-bit data at A, B, C and D.
3. Keeping the mode control =1 apply one clock pulse. The data applied at A, B, C and D will appear at QA, QB, QC and QD respectively.
4. Now mode control = 0. Apply clock pulses one by one and observe the data coming out serially at QD.

PIPO:-



PIPO Function Table

Clock	Parallel i/p				Parallel o/p			
	A	B	C	D	QA	QB	QC	QD
1	1	0	1	1	1	0	1	1

PROCEDURE

1. Connections are made as per circuit diagram.
2. Apply the 4 bit data at A, B, C and D.
3. Apply one clock pulse at Clock 2 (Note: Mode control =1).
4. The 4 bit data at A, B, C and D appears at QA, QB, QC and QD respectively.

RESULT*: shift registers using IC 7495 for SIPO/SISO, PISO/PIPO are verified.*

RING COUNTER

AIM: *To realize Ring counter and Johnson counter using IC 7495*

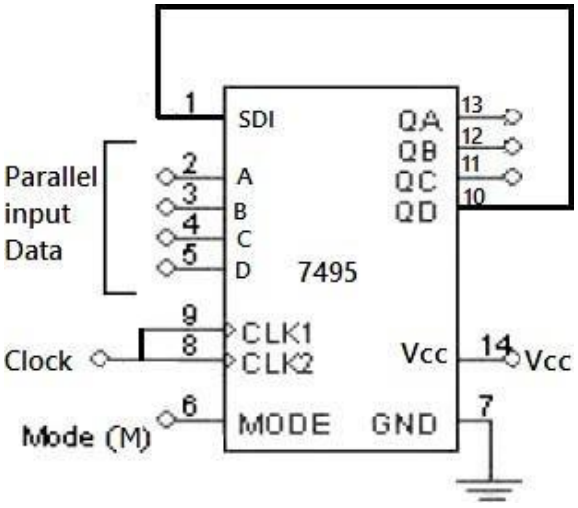
COMPONENTS REQUIRED:

Sl.No.	Components	Quantity
1	IC 7495	1
2	IC 7404	1
3	Patch Chords	20
4	IC Trainer Kit	1

THEORY

A ring counter is a circular shift register which is initiated such that only one of its flip-flops is the state one while others are in their zero states. A ring counter is a Shift Register with the output of the last one connected to the input of the first, that is, in a ring. Typically, a pattern consisting of a single bit is circulated so the state repeats every n clock cycles if n flip-flops are used. It can be used as a cycle counter of n states.

RING COUNTER:



Function Table

Mode	Clock	QA	QB	QC	QD
1	1	1	0	0	0
0	2	0	1	0	0
0	3	0	0	1	0
0	4	0	0	0	1
0	5	1	0	0	0
0	6	repeats			

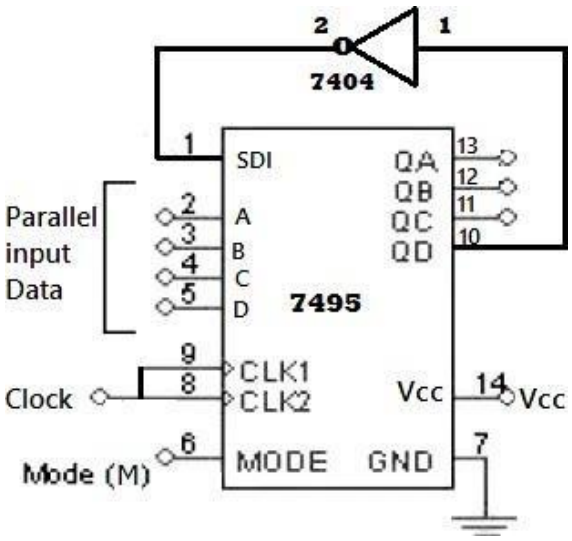
JOHNSON COUNTER

THEORY:

A Johnson counter (or switch tail ring counter, twisted-ring counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage. The register cycles through a

sequence of bit-patterns, whose length is equal to twice the length of the shift register, continuing indefinitely. These counters find specialist applications, including those similar to the decade counter, digital-to-analog conversion, etc. They can be implemented easily using D- or JK-type flip-flops.

JOHNSON COUNTER:



Function Table

Mode	Clock	QA	QB	QC	QD
1	1	1	0	0	0
0	2	1	1	0	0
0	3	1	1	1	0
0	4	1	1	1	1
0	5	0	1	1	1
0	6	0	0	1	1
0	7	0	0	0	1
0	8	0	0	0	0
0	9	1	0	0	0
0	10	repeats			

PROCEDURE:

1. Make the connections as shown in the respective circuit diagram.
2. Initial condition is set by setting up the circuit as shown in the figure.
3. Apply clock and observe the output after each clock pulse, record the observations and verify that they match the expected outputs from the truth table.
4. Verify the operation of ring counter/Johnson counter circuit as per the function tables

RESULT: *Ring counter and Johnson counter using IC 7495 are verified*

EXPERIMENT: 8

REALIZE: i) Design MOD-N synchronous up counter & down counter using IC 7476 (JK FF) ii) MOD-N counter using IC 7490/7476 iii) Synchronous counter using IC 74192

MOD-N synchronous up counter & down counter using IC 7476 (JK FF)

AIM: *i) Design and study (MOD-7) 3 bit synchronous counter (Up counter & Down counter) using JKflip flops.*

COMPONENTS REQUIRED:

Sl.No.	Components	Quantity
1	IC IC 74LS76A	1
2	IC 7408	1
3	Patch Chords	20
4	IC Trainer Kit	1

THEORY

Counters : counters are logical device or registers capable of counting the no. of states or no. of clock pulses arriving at its clock input where clock is a timing parameter arriving at regular intervals of time, so counters can be also used to measure time & frequencies. They are made up of flip flops. Where the pulse are counted to be made of it goes up step by step & the o/p of counter in the flip flop is decoded to read the count to its starting step after counting n pulse incase of module counters.

Counter are of two types:

1) Asynchronous counter 2) Synchronous counter.

Asynchronous counter commonly called ripple counter, the first flip-flop is clocked by the external clock pulse & then each successive flip-flop is clocked by the Q or Q' output of the previous flip-flop. Therefore in an asynchronous counter the flip-flop's are not clocked simultaneously.

When counter is clocked such that each flip flop in the counter is triggered external clock at the same time, the counter is called as *synchronous counter*. Ex:- Ring counter & Johnson counter

Types of synchronous counter:

1) Up counter 2) Down counter.

Decision for number of flip-flops

Example : If we are designing mod N counter and m number of flip-flops are required then m can be found out by this equation.

$N <= 2^m$

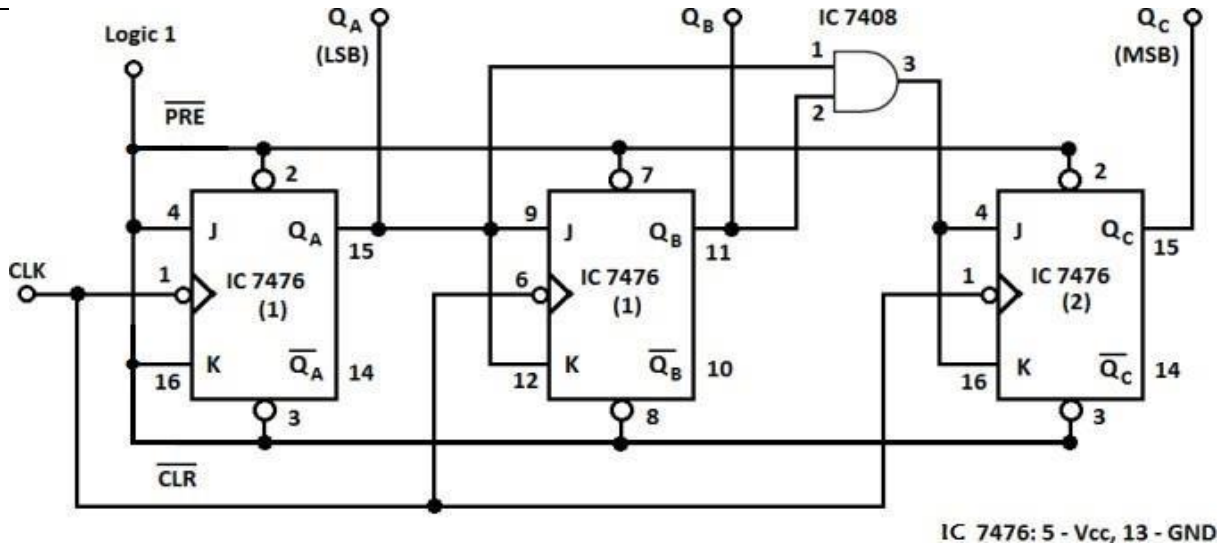
Here we are designing Mod-7 counter Therefore, N= 7 and number of Flip flops or bits (m) required is, **for m =3,** 7<=8, which is TRUE.

3 bit Synchronous up counter:

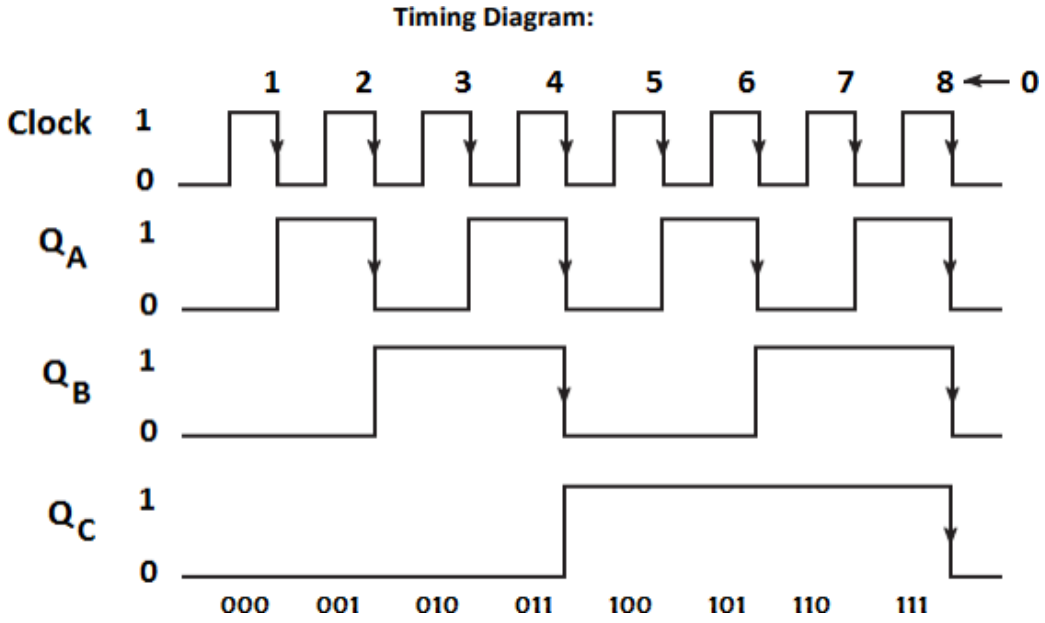
The up counter counts from 0 to7 (000 - 111) for this MS JK flip flop IC 74LS76 is used, 2 MS J-K flip flops are available. It is observed that the AND gate inputs are fed by the non-complement outputs of FF_A and FF_B. The clock pulse is given at pin 1 & 6 of the 1st IC & pin 1 of 2nd IC, respectively to apply clock to all flip flop at a time.

3 bit Synchronous down counter:

This is used to count from 7 to 0 (111-000) for this also 2 IC's of 74LS76 are required & hence we use 3 MS JK flip flops. It is observed that the AND gate inputs are fed by the complement outputs of FF_A and FF_B. The clock pulse is given at pin 1 & 6 of the 1st IC & pin 1 of 2nd IC, respectively to apply clock to all flip flop at a time.



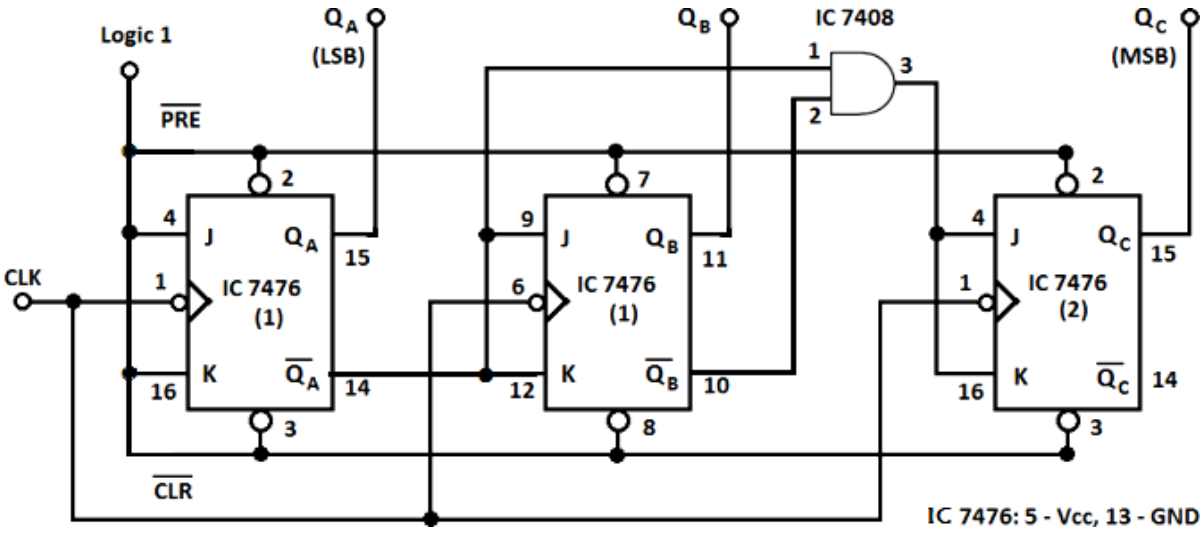
UP COUNTER CIRCUIT DIAGRAM



PROCEDURE

1. Connect the circuit as shown in the diagram.
2. Connect PRE input to the logic 1 (+5V).
3. Connect CLR input to the logic 0 (0V) or ground to reset counter.
4. Connect CLR input to the logic 1.
5. Apply the clock pulse to CLK input.
6. Observe the output and verify the observation table.

DOWN COUNTER CIRCUIT DIAGRAM



Observation Table:

Up Counter

Clock Input	Output		
Count	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Down Counter

Clock Input	Output		
Count	Q_C	Q_B	Q_A
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

ii) MOD – N COUNTER USING IC 7490

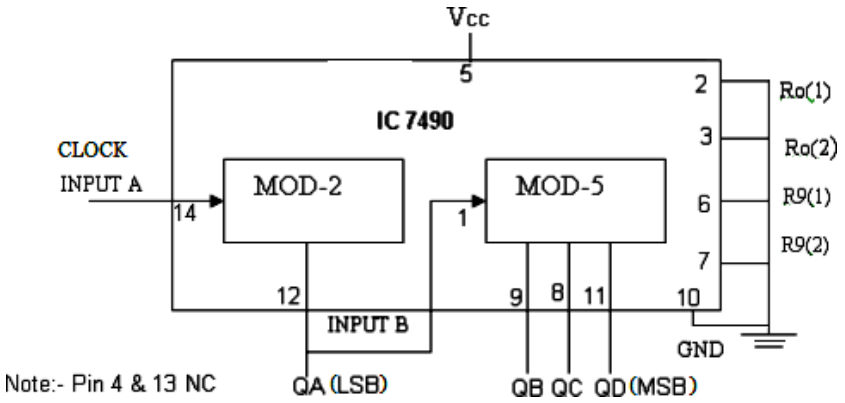
AIM: *ii) Realization of (MOD-10) counter using IC7490*

THEORY

If N=10, it is said to be a decade counter (MOD-10 counter). Its operation is as follows:

1. The output of MOD-2 is externally connected to the input B which is the clock input of the internal MOD-5 counter.
2. Hence QA toggles on every falling edge of clock input whereas the output QD,QC,QB of the MOD-5 counter will increment from 000 to 100 on low going change of QA output.
3. Due to cascading of MOD-2 and MOD-5 counter, the overall configuration becomes a MOD-10.
4. The reset inputs Ro(1), Ro(2) and preset inputs R9(1), R9(2) are connected to ground so as to make it inactive.

Mod-10 Counter Circuit



OBSERVATION TABLE

CLK	Count	O/p of MOD-5			O/p of MOD-2
		QD	QC	QB	QA
0	0	0	0	0	0
1	1	0	0	0	1
2	2	0	0	1	0
3	3	0	0	1	1
4	4	0	1	0	0
5	5	0	1	0	1
6	6	0	1	1	0
7	7	0	1	1	1
8	8	1	0	0	0
9	9	1	0	0	1

iii) SYNCHRONOUS COUNTER USING IC 74192

AIM: *iii) Realization of synchronous counter using IC74192*

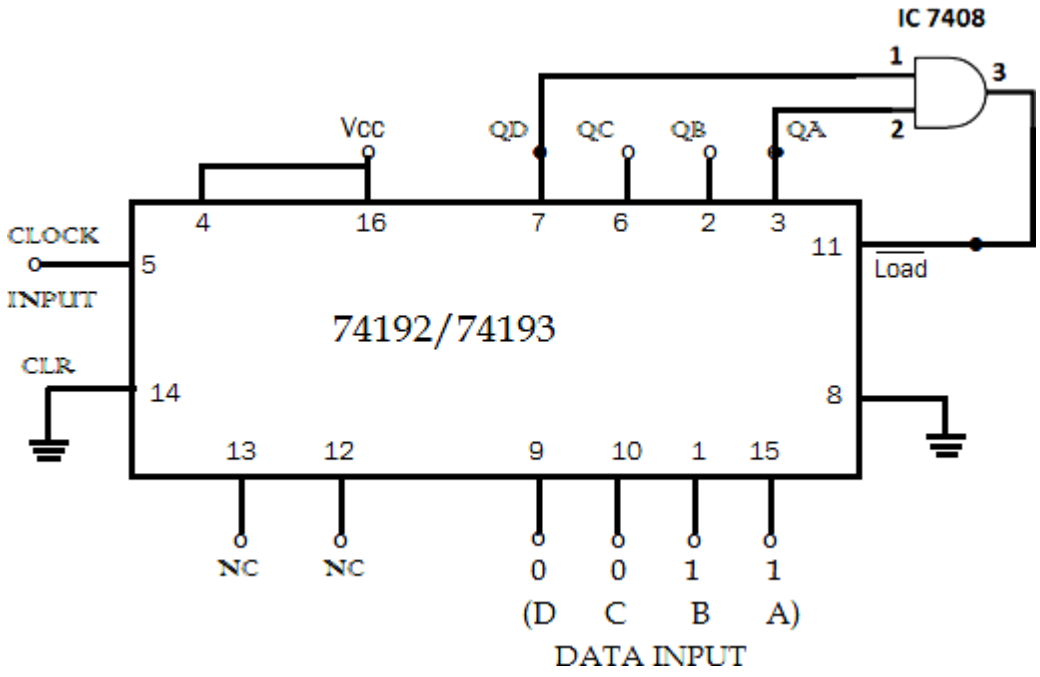
THEORY:

A 74192 IC is a pre-settable synchronous 4-bit Up/Down decimal counter, capable of reset to zero, preloading with a specified value, as well as generating carry and borrow signals that allow one to construct multi-digit counters. The result of the synchronization is that all the individual output bits of each FF changing state at exactly the same time in response to the common clock signal with no ripple effect and therefore, no propagation delay.

PROCEDURE

1. *Check all the components for their working.*
2. *Make connections as shown in the circuit diagram.*
3. *Clock pulses are applied one by one at the clock input and output is observed at QA, QB, QC & QD*
4. *Verify the Truth Table from the outputs.*

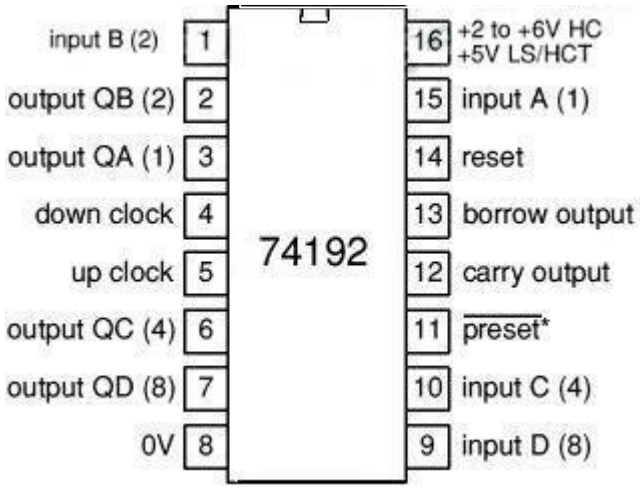
CIRCUIT DIAGRAM: COUNT UP FROM 3 TO 8



OBSERVATION TABLE

Clk	QD	QC	QB	QA
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	0	0	1	1

PIN DIAGRAM



RESULT: *The functioning of MOD-7using JK FF, MOD-10 using IC 7490 & Synchronous counter using IC74192 are verified.*

DEMONSTRATION EXPERIMENTS
EXPERIMENT: 9

AIM: *To design & conduct an experiment on II order*

i. *Low pass Butterworth filter to study the frequency response & to verify the roll off factor.*
ii. *High pass Butterworth filter to study the frequency response and to verify the roll off factor.*

Low Pass Filter

COMPONENTS REQUIRED:

Resistors as per design
IC µ741
Capacitor 0.01µF (3)
Connecting wires

THEORY

A second-order low-pass filter is an electronic circuit that attenuates (reduces) highfrequency I n audio and signal processing applications to remove noise and unwanted highfrequency components. The cutoff frequency is the frequency at which the filter begins to attenuate the signal, and the quality factor determines the sharpness of the cutoff.

The circuit diagram of a second-order low pass filter usually includes two capacitors and two resistors. One common implementation is the Sallen-Key topology, which is composed of an op-amp and four passive components. Overall, a second-order low pass filter can be used in various applications such as audio processing, signal conditioning, and control systems.

DESIGN

Specifications: Gain (Av) =1.586
Cutoff frequency fH=1k Hz

Assume R1 =10KΩ
Av =1+ Rf/R1,
Av –1 =Rf/R1
0.586*R1 =Rf
4Rf = 5.86k Ω.
Choose Rf = 5.6kΩ.

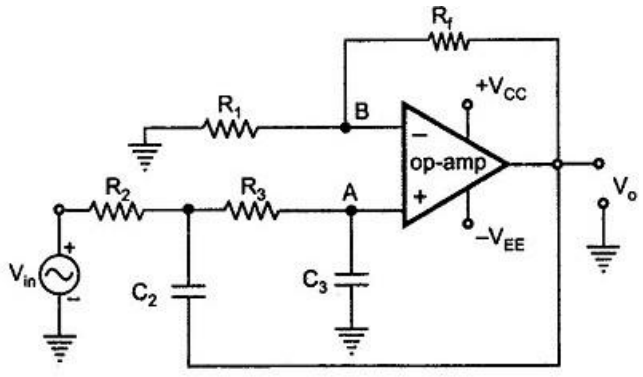
For II order LPF

$ii)The cutoff\ \ frequency\ f_H = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$

$=1/2\pi RC\ for\ R_2=R_3=R\ \&\ C_2=C_3=C$

Assume C = 0.01µF
R = 1/2*πfHC
R = 15kΩ

CIRCUIT DIAGRAM



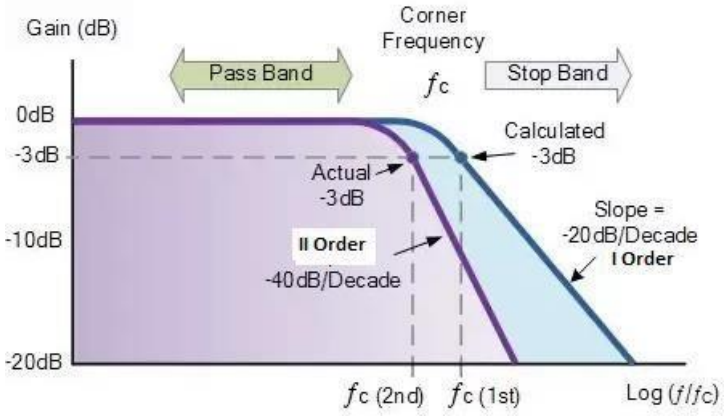
Second order low pass butterworth filter

Tabular Column :

Vi = _____V

f in Hz	Vo in Volt	Av = Vo / Vi	Gain in dB = 20 Log Av

Expected Graph:



High Pass Filter

COMPONENTS REQUIRED:

Resistors as per design
IC µ741
Capacitor 0.01µF (2)
Connecting wires

THEORY

A second-order high-pass filter is an electronic circuit that passes signals with a frequency higher than a certain cutoff frequency and attenuates signals with frequencies lower than the cutoff frequency. It offers a steeper roll-off than a first-order filter, making it useful for applications where precise control over the cutoff frequency is crucial. In manual configurations, adjustments to the filter's performance involve manipulating the values of capacitors, inductors, or additional resistors. This manual tuning capability provides flexibility for customizing the filter's response to suit specific requirements in electronic circuits, such as audio systems or communications equipment.

The circuit diagram of a second-order high pass filter usually includes two capacitors and two resistors. One common implementation is the Sallen-Key topology, which is composed of an op-amp and four passive components. Overall, a second-order low pass filter can be used in various applications such as audio processing, signal conditioning, and control systems.

DESIGN

Specifications: Gain (Av) =1.586
Cutoff frequency fH=10k Hz
Assume R1 =10KΩ
Av =1+ Rf/R1,
Av –1 =Rf/R1
0.586*R1 =Rf
Choose Rf = 17.064kΩ.

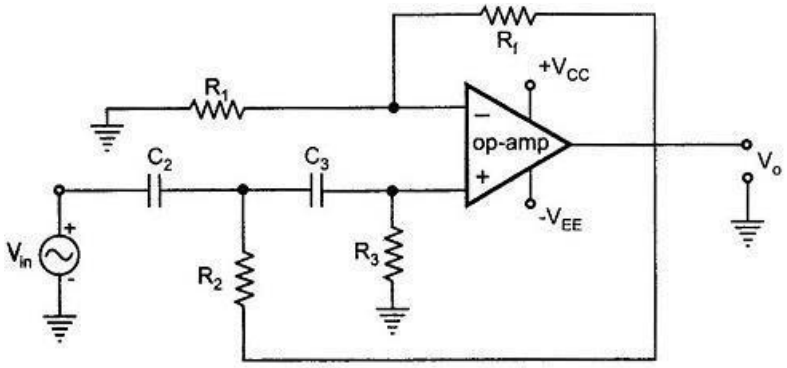
For II order LPF

$ii)The cutoff\ \ frequency\ f_L = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$

$=1/2\pi RC\ for\ R2=R3=R\ \&\ C2=C3=C$

Assume C = 0.1μF
R = 1/2*πfHC
R = 318Ω

CIRCUIT DIAGRAM



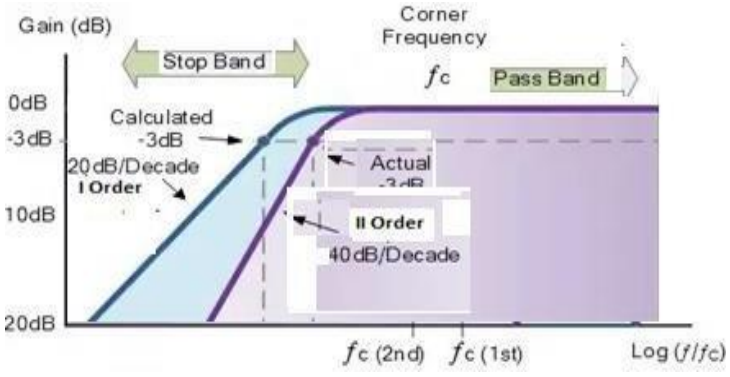
Second order high pass Butterworth filter

Tabular Column :

Vi = _____V

f in Hz	Vo in Volt	Av = Vo / Vi	Gain in dB = 20 Log Av

Expected Graph:



RESULT: *The functioning of the circuit and its behavior is verified.*

EXPERIMENT: 10

Design Monostable and Astable Multivibrator Using 555 Timer

MONOSTABLE MULTIVIBRATOR

AIM: *To construct and study the operation of a monostable multivibrator using 555IC timer.*

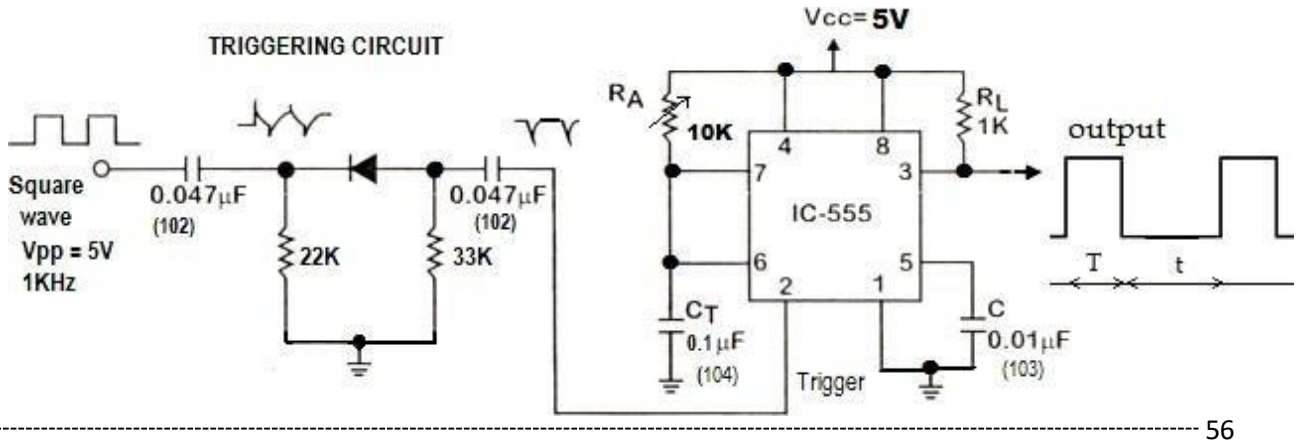
APPARATUS:

1. 555 IC timer
2. Capacitors (0.1μF, 0.01μF)
3. Resistors 1KΩ

THEORY

Monostable multivibrator is also known as triangular wave generator. It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. Timer IC 555 is also used as one shot or monostable operation. Since there are many real life application where many applications needs to operate for only specific time interval for such application one shot or monostable operation is suitable. When negative going pulse is applied to pin 2 which leads to output pin 3 goes to high. The negative edge of the trigger pulse causes the internal comparator 2 trigger the flip flops leads to output high at pin 3. The voltage across capacitor rises to 2VCC/3 through supply and resistor R1. When the voltage across capacitor reaches to 2VCC/3 the internal comparator 1 triggers the flip flop from and which send the output from high to low. Figure shows the waveforms associated with the operation of the IC 555 as a monostable. The output waveform shows that the wide range from microsecond to many seconds can be possible with appropriate values of R and C. This flexibility of time period makes IC 555 versatile for many real life applications. The time period is given by $T_p = 1.1\ RC$.

DESIGN: **Waveforms**



Output pulse width (T) = Delay time is given by

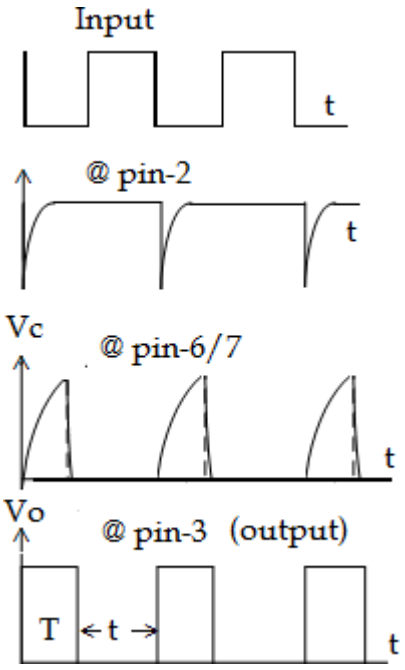
T = 1.1 R C .....*(1)*

Let T = 1ms ; C = 0.1μF

$$R = \frac{T}{1.1C} = \frac{1x10^{-3}}{1.1x0.1x10^{-6}} = 9.09K\Omega$$

R = 10KΩ (std)

Apply input square-wave signal from the signal generator of f = 1KHz (T = 1ms) and V_{pp} =5V



MONOSTABLE MULTIVIBRATOR CIRCUIT DIAGRAM

1. Connections are made as per the circuit diagram.
2. Setup negative triggering using triggering circuit & it is applied at the terminal 2 of IC 555.
3. Observe the output waveforms and measure the output voltage (V_O) and voltage across capacitor (Vc). Calculate the theoretical values of above measured parameters.
4. Theoretically the time period (T) is calculated by $T=1.1R_1C_1$ where $R_1 = 10K\Omega$ $C_1=0.1\mu F$.
5. Practical and theoretical charging and discharging timers are measured.
6. Plot the wave forms as per the scale.

TABULATION

PROCEDURE

Parameter	Theoretical	Practical
T (ms)	1 m sec	
t (ms)	6 m sec	

RESULT: Monostable multivibrator using timer IC 555 is designed, setup and the waveforms are obtained.

ASTABLE MULTIVIBRATOR

AIM: *To construct and study the operation of Astable multivibrator using 555 timer*

APPARATUS:

1. IC 555 Timer
2. Resistors as per design
3. Capacitors (0.1µF, 0.01µF)
4. CRO

THEORY: The capacitor charges through resistors R_A and R_B the voltages across capacitor rises to $2V_{CC}/3$. This voltage acts as a threshold voltage at pin 6 which is input to internal comparator which finally trigger the internal flip flop so that output pin 3 goes low. Also flip flop drives the internal discharge transistor to ON allowing capacitor to get discharge from R_B this lead to decrease in capacitor voltage to $V_{CC}/3$ and the flip flop get trigger and discharge transistors gets off and output set to high. This leads to charging of capacitor through R_A and R_B to V_{CC}. A diode D1 is connected between the discharge and threshold terminals (as also across R_B). Thus the capacitor now charges only through R_A (since R_B is shorted by diode conduction during charging) and discharges through R_B. Another optional diode D_2 is also connected in series with R_B in reverse direction for better shorting of R_B.

Design:

The time for charging C from 1/3 to 2/3 Vcc = ON Time = 0.693 (RA + RB) C

The time for discharging C from 2/3 to 1/3 Vcc = OFF Time = 0.693 RB C

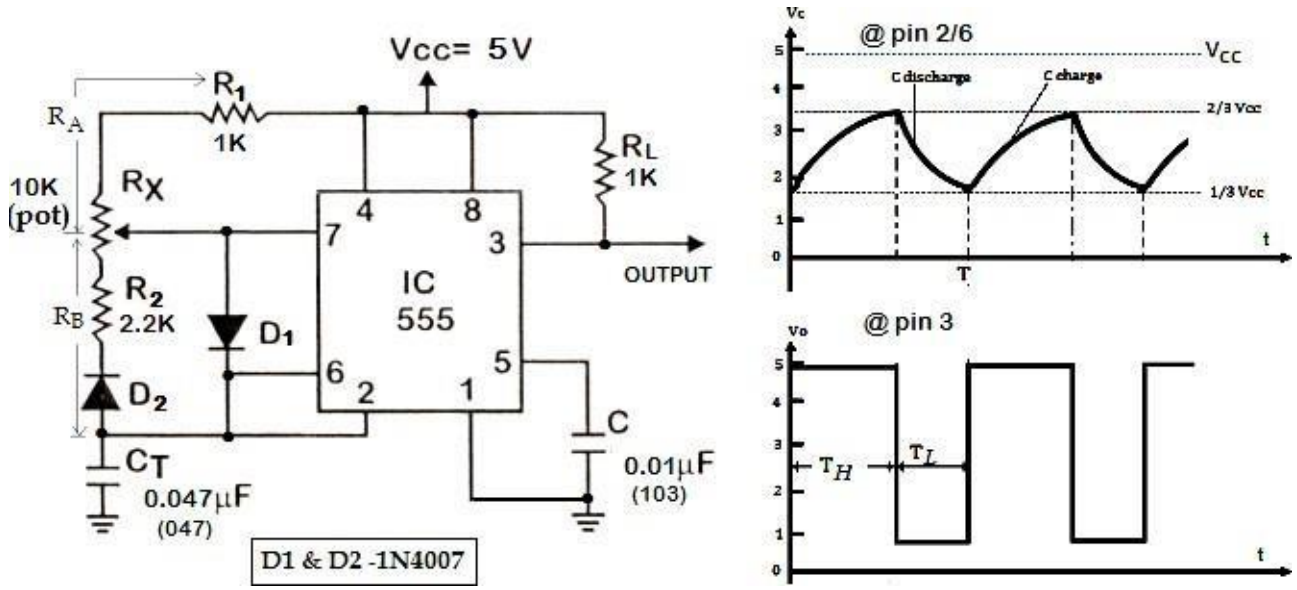
$f_{osc} = 1/ T_{osc} = 1.44/(R_A + R_B)C$

Duty Cycle = $R_A/ (R_A + R_B)$

Min. Duty Cycle = $R_1/(R_1 + RX + R_2)$ Max. Duty Cycle = $(R_1 + RX)/(R_1 + RX + R_2)$

To vary the duty cycle from about 0 to 100%, a potentiometer, RX, is used. Thus a variable duty cycle is achieved.

ASTABLE MULTIVIBRATOR CIRCUIT DIGRAM and WAVEFORMS



PROCEDURE

1. Connections are made as per the circuit diagram.

2. Set the DC power supply to provide V_{CC}=5V .

3. Connect output pin (3) of 555 to channel 1 of CRO and pin (2/6) to channel 2 of CRO.

4. Observe the output waveforms and measure the output voltage (V_O) and voltage across capacitor (Vc). Calculate the theoretical values of above measured parameters.

5. Plot the output voltage waveforms for output voltage and voltage across capacitor.

*Frequency, f= 1.45/ (R_A+2R_B)C and % of Duty cycle = (TH/ (TH+TL))*100*

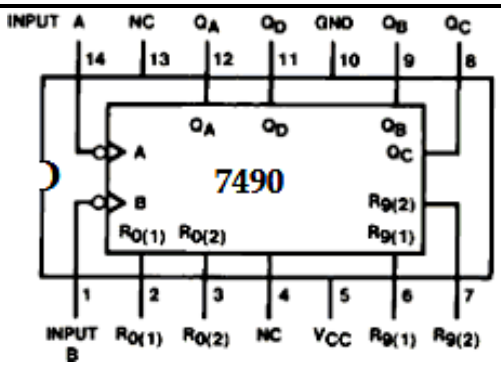
6. Practically TL and TH are measured and theoretical values are verified with practical values.

TABULATION

T_H (ms)		T_L (ms)		T (ms)		F (Hz)		Duty Cycle
Theoretical	Practical	Theoretical	Practical	Theoretical	Practical	Theoretical	Practical	
								60%
								50%
								40%

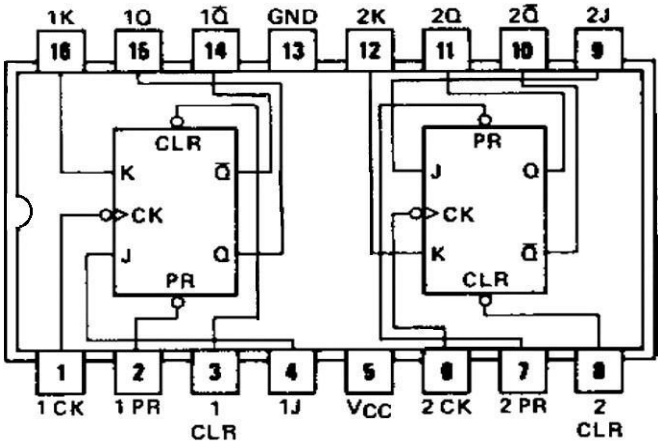
RESULT: Astable multivibrator using timer IC 555 is designed, setup and the waveforms are obtained.

IC 7490



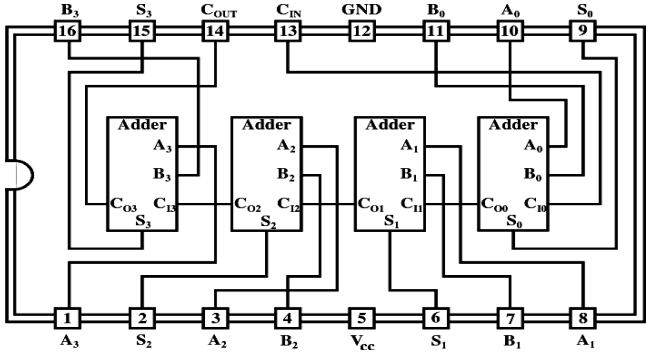
It is an asynchronous (decade) mod-10 counter. It consists of 4 flip flops that are internally connected so as to provide mod 2 & mod 5 counter functions. It can count the binary numbers from 0000 to 1001. After 1001 it gets reset and again starts counting.

IC 7476



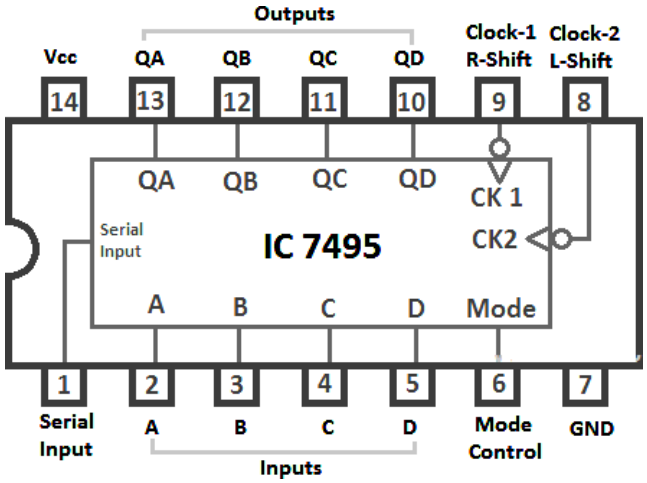
Master—slave JK Flip Flop, has two JK flip flops inside it and each can be used individually based on application. **74LS76** is a negative edge-triggered J-K flip-flop. It has a preset and clear function which allows the IC to bypass the clock and inputs and give the different outputs.

IC 7483



It is a digital adder IC that can add two 4 bit binary numbers. IC 7483 consists of four individual full adder circuits which are internally connected. It has also input and output carry circuit.

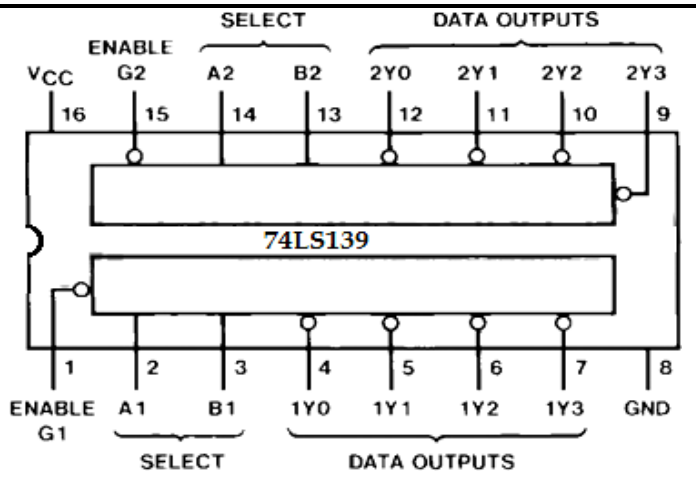
IC 7495



It is a 4-Bit shift register with serial and parallel synchronous operating modes. The *serial shift right* and *parallel load* are activated by separate clock inputs which are selected by a *mode control* input. The data is transferred from the serial or parallel inputs to the Q outputs synchronous with logic 1→0 transition of clock input.

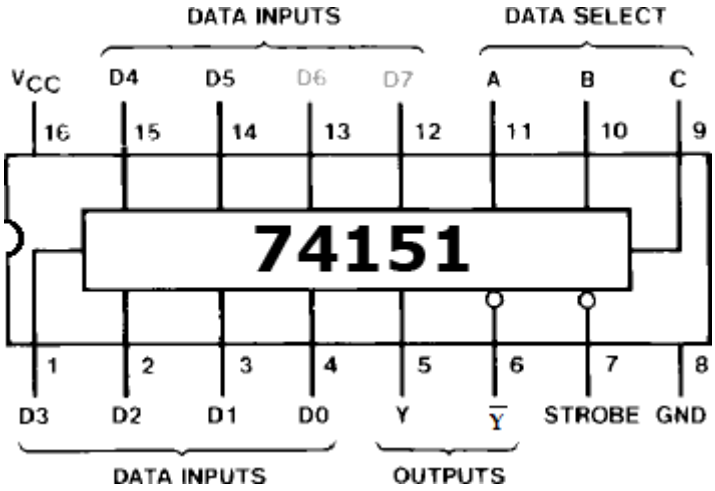
IC 74139

Dual 2-to-4 line separate Decoder / Demultiplexer in DIP-16 Package. The active-low enable input can be used as a data line in demultiplexing applications. Decoder can be used as Code a converter.



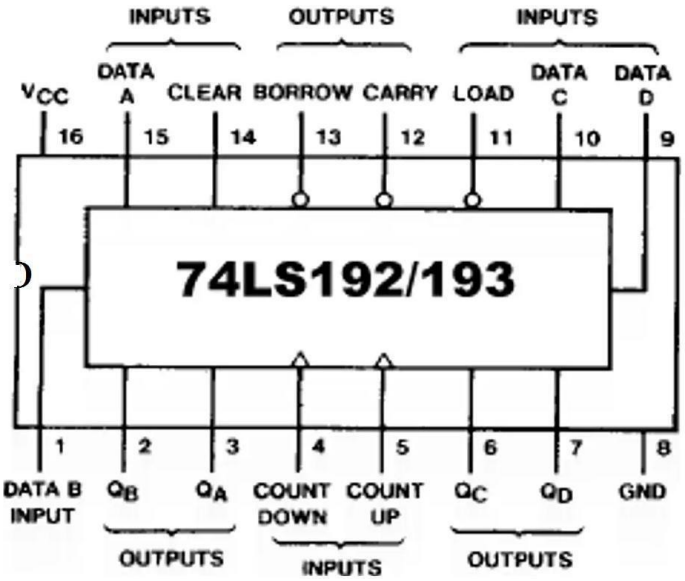
IC 74151

It is an 8: 1 multiplexer which provides two complementary outputs Y & Ȳ. The LS151 can be used as a universal function generator to generate any logic function of four variables.



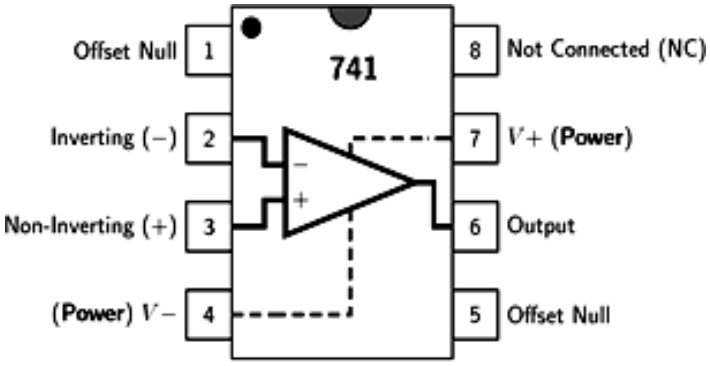
IC 74192

The SN54/74LS192 is an UP/DOWN BCD Decade (8421) Counter and the. SN54/74LS193 is an UP/DOWN MODULO-16 Binary Counter. These chips also have parallel data input leads that can be used to preset the counter. Two clock inputs are available; one for an UP count and the other for a DOWN count.



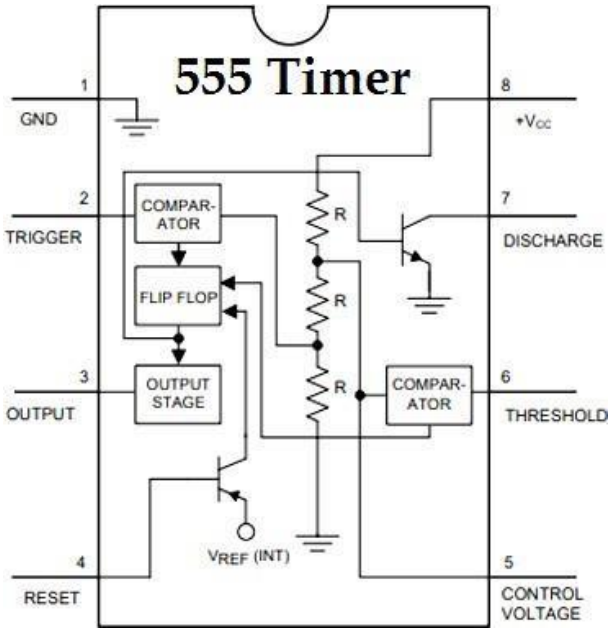
IC µA 741 (OPAMP)

The 741 Operational Amplifier IC is a monolithic integrated circuit, comprising of a general purpose Operational Amplifier. It was first manufactured by Fairchild semiconductors in the year 1963. The number 741 indicates that this operational amplifier IC has 7 functional pins, 4 pins capable of taking input and 1 output pin.

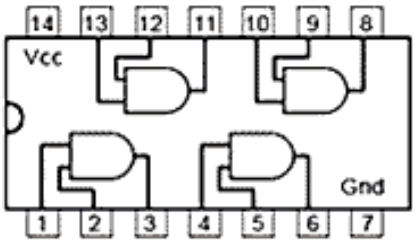


IC 555 TIMER

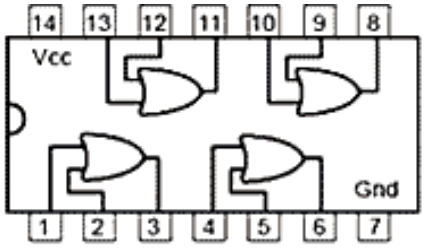
It is an integrated circuit used in a variety of timer, delay, pulse generation, and oscillator applications. The 555 Timer IC got its name from the three 5KΩ resistors that are used in its voltage divider network. It is first introduced in early 1970.



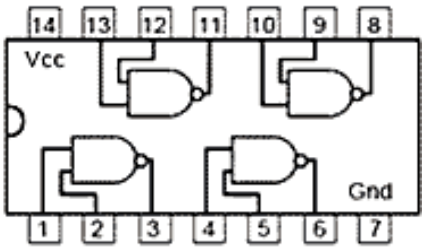
PIN CONFIGURATION OF DIGITAL ICs



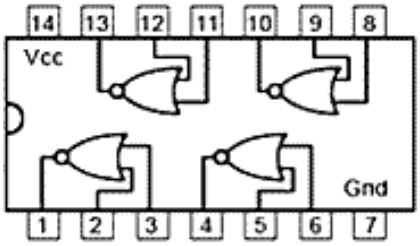
7408 Quad 2 input AND Gates



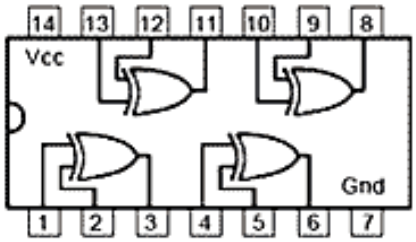
7432 Quad 2 input OR Gates



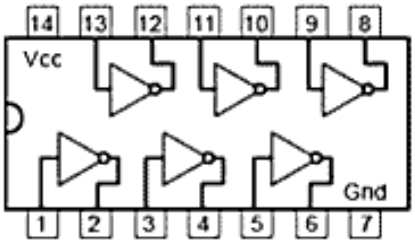
7400 Quad 2 input NAND Gates



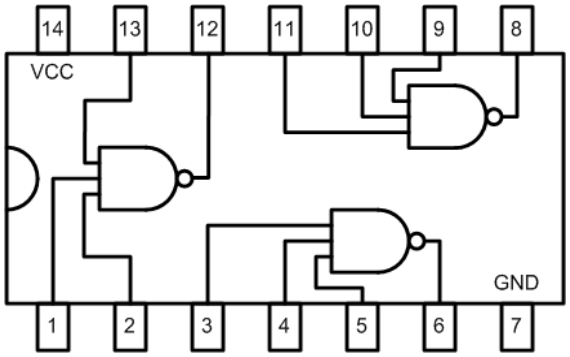
7402 Quad 2 input NOR Gates



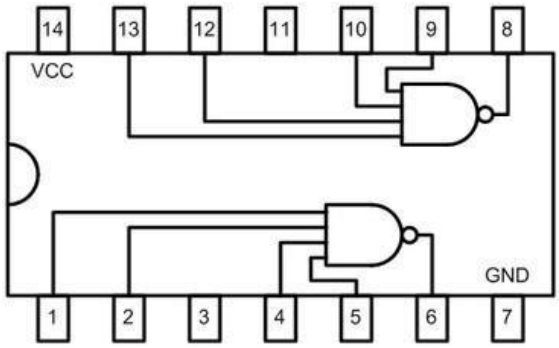
7486 Quad 2 input XOR Gates



7404 Hex NOT Gates XNOR Gates



7410 Triple 3 Input NAND



7420 Dual 4 Input NAND