System Development Plan

for the

The Balance Project

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DOCUMENT CHANGE HISTORY

The following table is a simple list of released revisions sent for review. Records of reviews and the review artifacts are saved with reviewer information in the The Balance Projectartifact repository.

Change Record

Date	Version	Author(s)	Change Reference
13 Sep 2025	P1	Vinay Agarwal	Preliminary DRAFT version

Draft P1 Preliminary version of this document.

1. Baseline Document draft 1

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CHAPTER 1

Scope

This document provides the System Development Plan (**SDP**) for the Balance System. The system will be referred to as the Balance System.

1.1 Identification

The Balance System described in this document shall be known as Balance System version 1.

1.2 System Overview

The Balance System is a game that users an play a game.

Figure 1 shows the high-level architecture for the Balance System system. This diagram

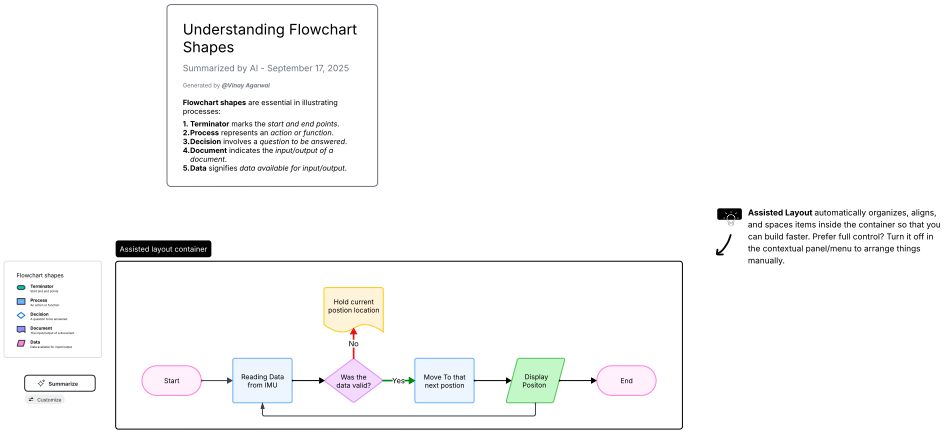

Figure 1: System Overview

shows the major external interfaces that provide the capabilities of Balance System.

This system would be a game where the user would have to balance a ball on a LCD screen that is builtin on the STM32 board. The objective of the game is to balance the ball on the screen based on the way the board was tilted. Balance System would keep track of the current position of the ball and where the next updated move is. This helps keep track

of the system of where the ball is until a movement has occurred. Balance System shall process at a maximum 180 Hz. This would give the user enough time to process the current angle of the ball and be able to present on the LCD-TFT screen.

1.3 Document Overview

This document contains an overview of how the software for the Balance System will be created and distributed to the hardware. It include system purpose, software development plan, and development procedure.

CHAPTER 2

References

This section provides a list of referenced items for this document.

2.1 Acronyms and Abbreviations

This section defines acronyms and abbreviations used in this and related documents.

Table 1: Acronym Definitions

Acronym	Definition
YSM	Yourdon Structured Method
LTDC	Layered Transmission Display Controller
STM	STMicroelectronics
MEMS	Micro-Electro-Mechanical Systems
End of acronym definition table	

2.2 Glossary and Definitions

This section defines glossary terms used in this and related documents.

Table 2: Glossary Terms and Definitions

Glossary Term	Definition
STM32F429I	Micro-controller board has all component fit onto one board.
Customer	The professor that is view the grading all assignments.
End of glossary terms table	

2.3 Referenced Documents

This section lists the referenced documents for this document. The references are categorized into two categories:

External Documents not directly associated with this project.

Project Documents that are directly associated with this project.

2.3.1 External Documents

2.3.2 Project Specific Documents

CHAPTER 3

Required Work Overview

The scope of the work is to write software to an STM32F429I-Disc. The application would be a full stack development. This system shall require user input and display report.

3.1 Program Status

The project started because of the board the was purchased for another class. That class ask to create a system that requires input and outputs between an MCU. It is easier to just use that project as a guideline to project plan for this class.

3.2 SDLC Situation

This section is **...TBD...**.

3.3 Requirement Plans

The current plan is to write requirement once the deployment system is solidify. The requirements will be written in a different in file. This file will be a csv that organizes what need to be done for the system.

3.4 Documentation Plans

This section is **...TBD...**.

The following documents are listed here just to test reference generation. A "real" **SDP** would reference these as applicable for the project.

- **ref˙˙KNEAD˙OCD˙ExProj**, **ref˙˙KNEAD˙OCD˙ExProj** [**ref˙˙KNEAD˙OCD˙ExProj**] is the **OCD**, which outlines the project overall so, generally, it is created first.
- **ref˙˙KNEAD˙SDP˙ExProj**, **ref˙˙KNEAD˙SDP˙ExProj** [**ref˙˙KNEAD˙SDP˙ExProj**] is this document.
- **ref˙˙KNEAD˙SPS˙ExProj**, **ref˙˙KNEAD˙SPS˙ExProj** [**ref˙˙KNEAD˙SPS˙ExProj**] is the **SPS**, which should come from the customer or end user, but often is generated by the developer with customer approval.
- **ref˙˙KNEAD˙SSS˙ExProj**, **ref˙˙KNEAD˙SSS˙ExProj** [**ref˙˙KNEAD˙SSS˙ExProj**] is the **SSS** that is the developer's design specification to meet the **SPS** requirements.

- **ref˙˙KNEAD˙SUM˙ExProj**, **ref˙˙KNEAD˙SUM˙ExProj** [**ref˙˙KNEAD˙SUM˙ExProj**] is the **SUM** that acts somewhat like part of the **SSS** since it illustrates the **UI** design part of the **SSS**, but in a separate artifact that also can be used as a standalone users' manual.

- **ref˙˙KNEAD˙HRS˙ExProj**, **ref˙˙KNEAD˙HRS˙ExProj** [**ref˙˙KNEAD˙HRS˙ExProj**] is a **HRS**, which often is not used for smaller projects but can have multiple instances for large projects to more fully detail hardware design.

- **ref˙˙KNEAD˙SRS˙ExProj**, **ref˙˙KNEAD˙SRS˙ExProj** [**ref˙˙KNEAD˙SRS˙ExProj**] is a **SRS**, which often is not used for smaller projects but can have multiple instances for large projects to more fully detail software or firmware design.

- **ref˙˙KNEAD˙IRS˙ExProj**, **ref˙˙KNEAD˙IRS˙ExProj** [**ref˙˙KNEAD˙IRS˙ExProj**] is the **IRS**, which often is not use but may be needed, even if **HRS** or **SRS** artifacts are not, to fully document detailed interfaces such as Application Programming Interfaces (**APIs**) or other detailed mechanical or electrical interfaces.

- **ref˙˙KNEAD˙SSDD˙ExProj**, **ref˙˙KNEAD˙SSDD˙ExProj** [**ref˙˙KNEAD˙SSDD˙ExProj**] is the **SSDD** that provides a road map to the design and other design details needed to understand the hardware and software design.

- **ref˙˙KNEAD˙STP˙ExProj**, **ref˙˙KNEAD˙STP˙ExProj** [**ref˙˙KNEAD˙STP˙ExProj**] is the **STP** that highlights the planning for system testing.

- **ref˙˙KNEAD˙STS˙ExProj**, **ref˙˙KNEAD˙STS˙ExProj** [**ref˙˙KNEAD˙STS˙ExProj**] is the **STS**, which is sometimes called a test procedure. There could be multiple of these based on the overall project size.

- **ref˙˙KNEAD˙STR˙ExProj**, **ref˙˙KNEAD˙STR˙ExProj** [**ref˙˙KNEAD˙STR˙ExProj**] is an **STR** that documents the results of a given test. Multiple instances are expected based on the test plan. And, there could be multiple versions of a given test plan to document repeated occurrences of a given test specification/procedure.

- **ref˙˙KNEAD˙SVD˙ExProj**, **ref˙˙KNEAD˙SVD˙ExProj** [**ref˙˙KNEAD˙SVD˙ExProj**] is an **SVD** that documents a given release of a system. Multiple versions of these "release notes" are expected, with one **SVD** issued for each system release cycle.

3.5 Schedule and Resource Constraints

This section is **...TBD...**.

3.6 Other Constraints

This section is **...TBD...**.

CHAPTER 4

System Development Plans

This chapter is **...TBD...**.

4.1 Hardware Development Plans

The System will not need additional hardware for completion of work. If additional features are needed then this section shall be updated.

4.2 Firmware Development Plans

This System would require new updates to the firmware. Most firmware update is caused because of different packages that would update the middleware on the system. To keep the system up to date. Every release would have a tag to which firmware released.

4.3 Software Development Plans

The design shall be written as a uml format. Then would have a top down design.

4.4 Integration Plans

Currently, the plan is the update to the system through STLink. The STLink should be used to used to flash the system and debug the system.

4.5 Testing Plans

To keep a CICD pipeline structure, there shall be an automated process to build and test my code. As code get developed and processed every merge into a codebase.

4.6 Other Development Activities

This section is **...TBD...**.

CHAPTER 5

System Transition Plans

This chapter is **...TBD...**.

5.1 Configuration Management Plans

This section is **...TBD...**.

5.2 Release Plans

This section is **...TBD...**.

5.3 User Support Plans

This section is **...TBD...**.

5.4 Other Transition Plans

This section is **...TBD...**.

CHAPTER 6

Management and Control Activities

The full codebase will be Version Source Controlled(VSC).

6.1 Technical Review Events

The development system does not have technical review events.

6.2 Skills and Resources Needed

Users shall have documentation and demonstrations on how the system would work. This would be displayed on the LCD screen.

6.3 Scheduled Development and Monitoring

This would be maintained by the professor's schedule.

6.4 Other Management and Control Activities

This section is **...TBD...**.

APPENDIX

Other Info

ALL-Appendix :: This section shall contain any general information that aids in understanding this artifact (e.g., background information, rationale, etc.)

This section provides other information, as necessary, to document the system development plan.

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