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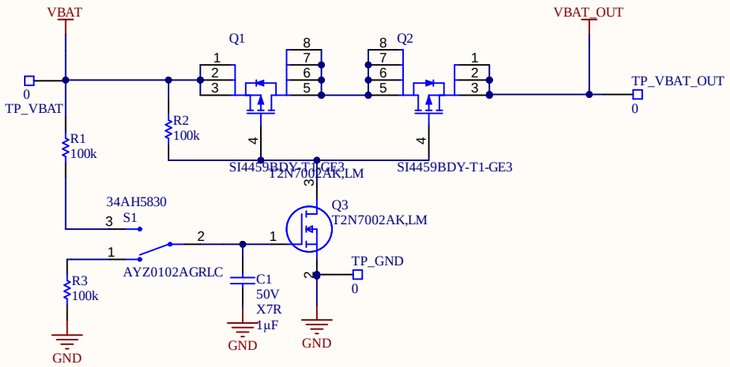
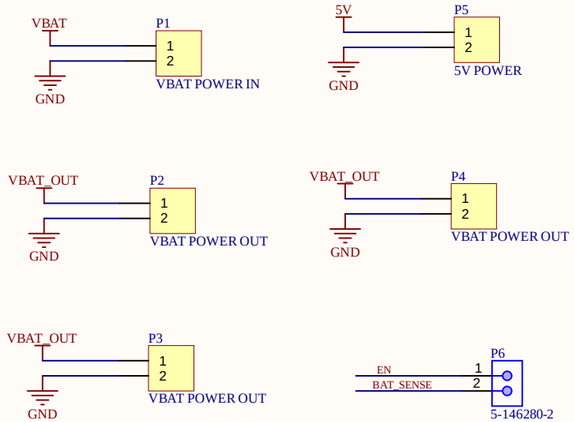
REVISION	DESCRIPTION	DATE	APPROVED

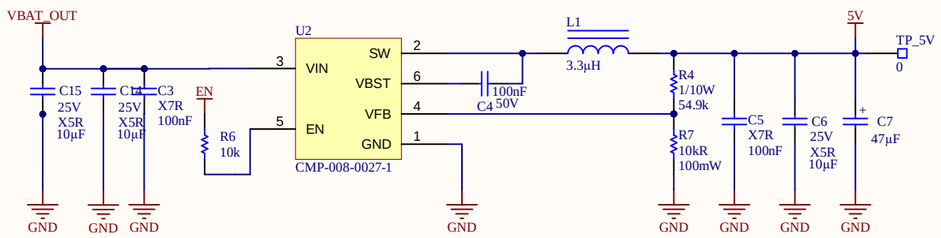
High Side Switch with Soft Start and Reverse Polarity Protection



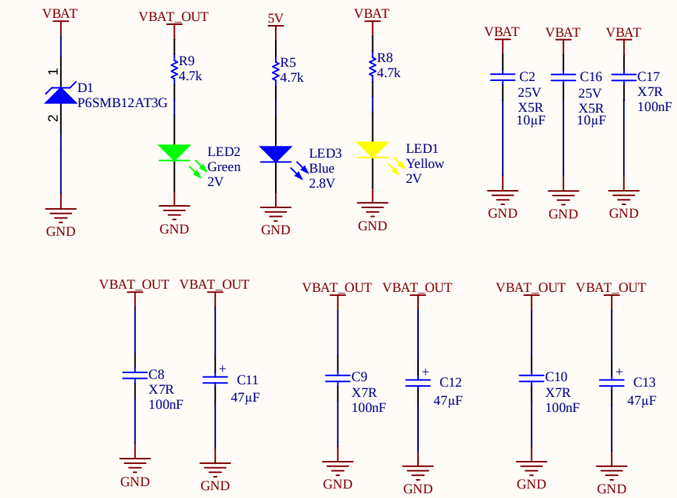
Connectors



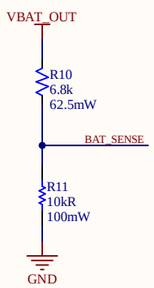
5V Buck Converter



Capacitors, Indicators and TVS Diodes



Battery Sense



APPROVALS	DATE
ENG: *	--/--/--
DSN: *	--/--/--
CHK: *	--/--/--
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG: 1	

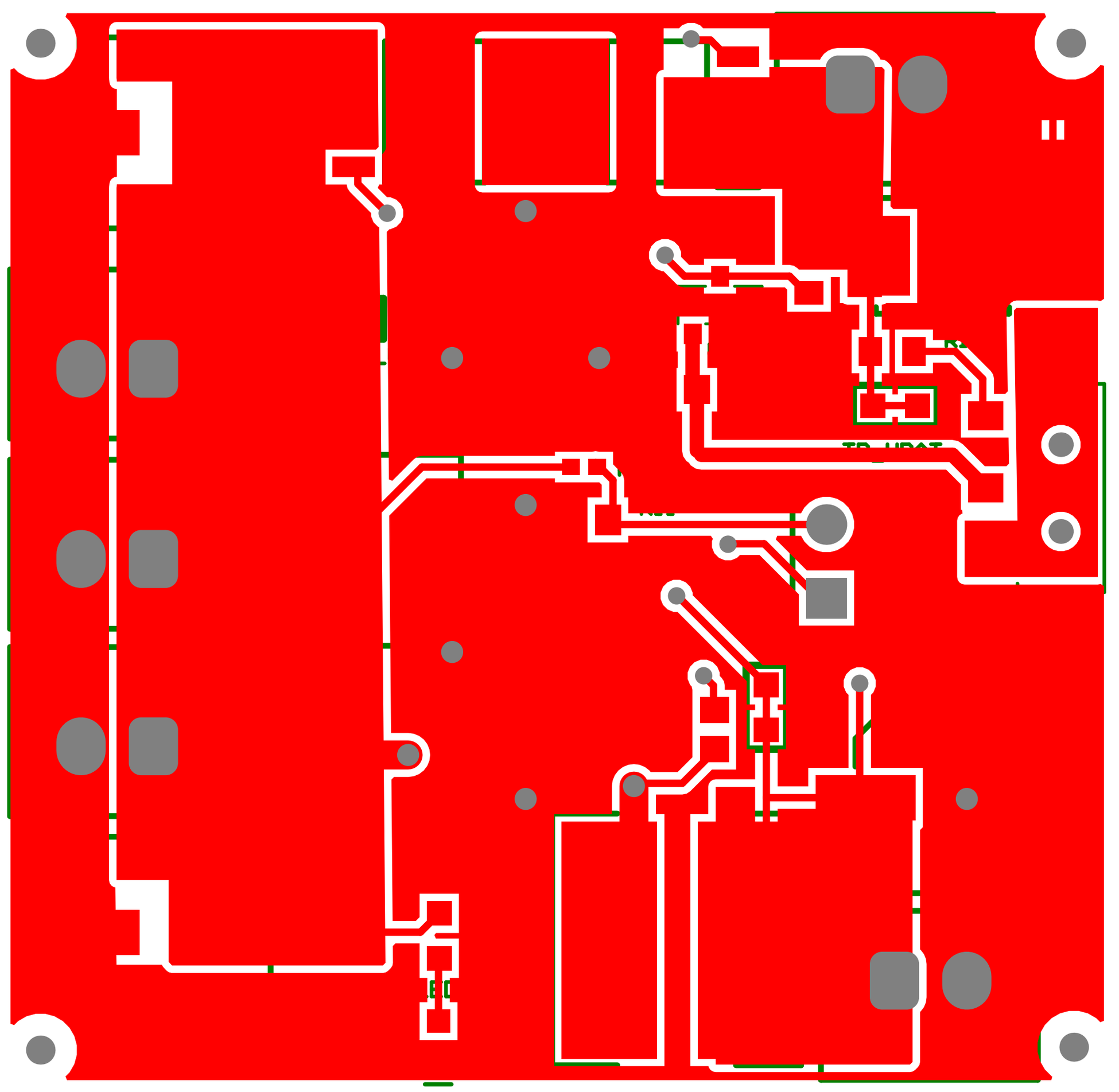
PROJECT: *

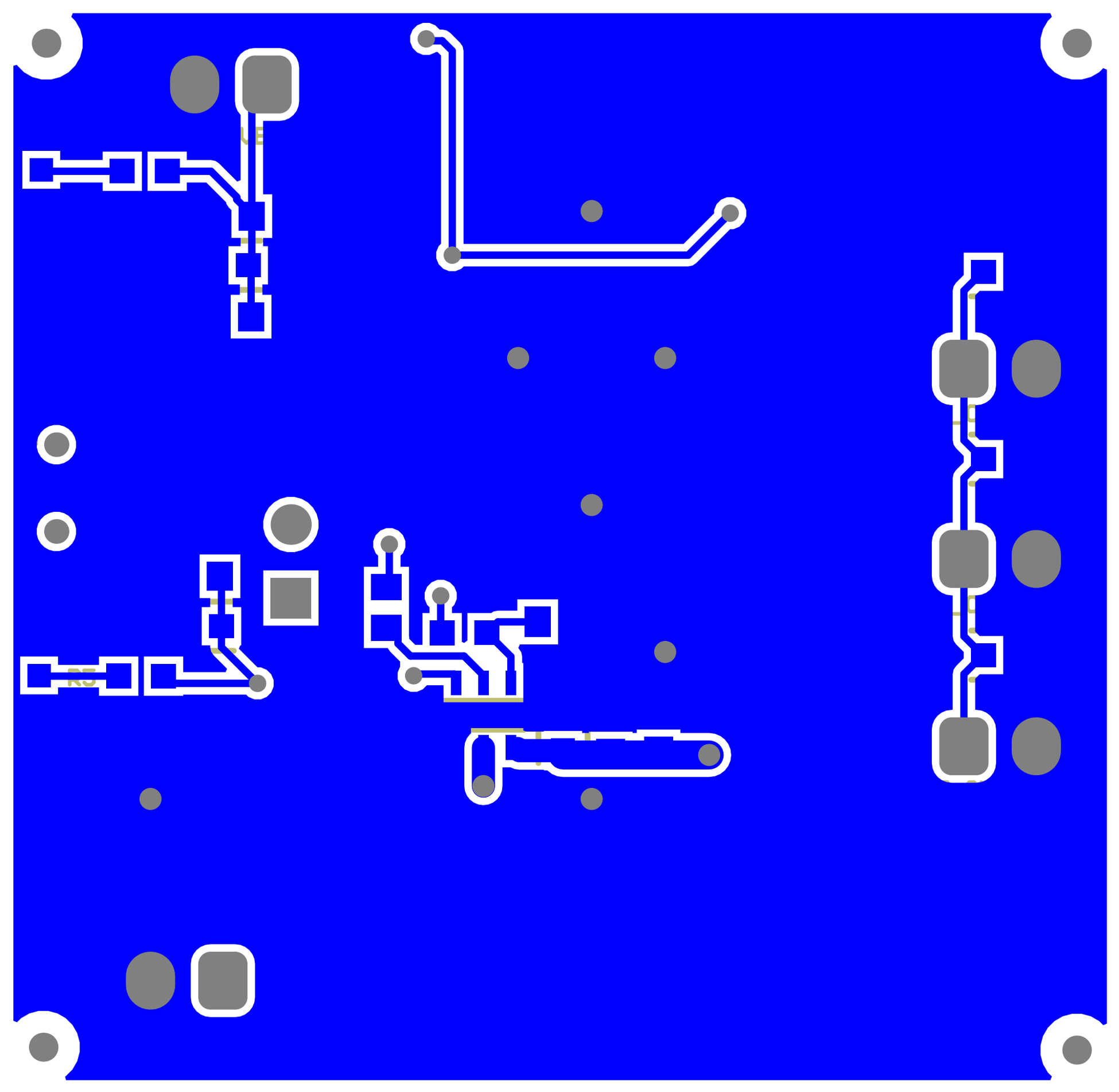
PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM:

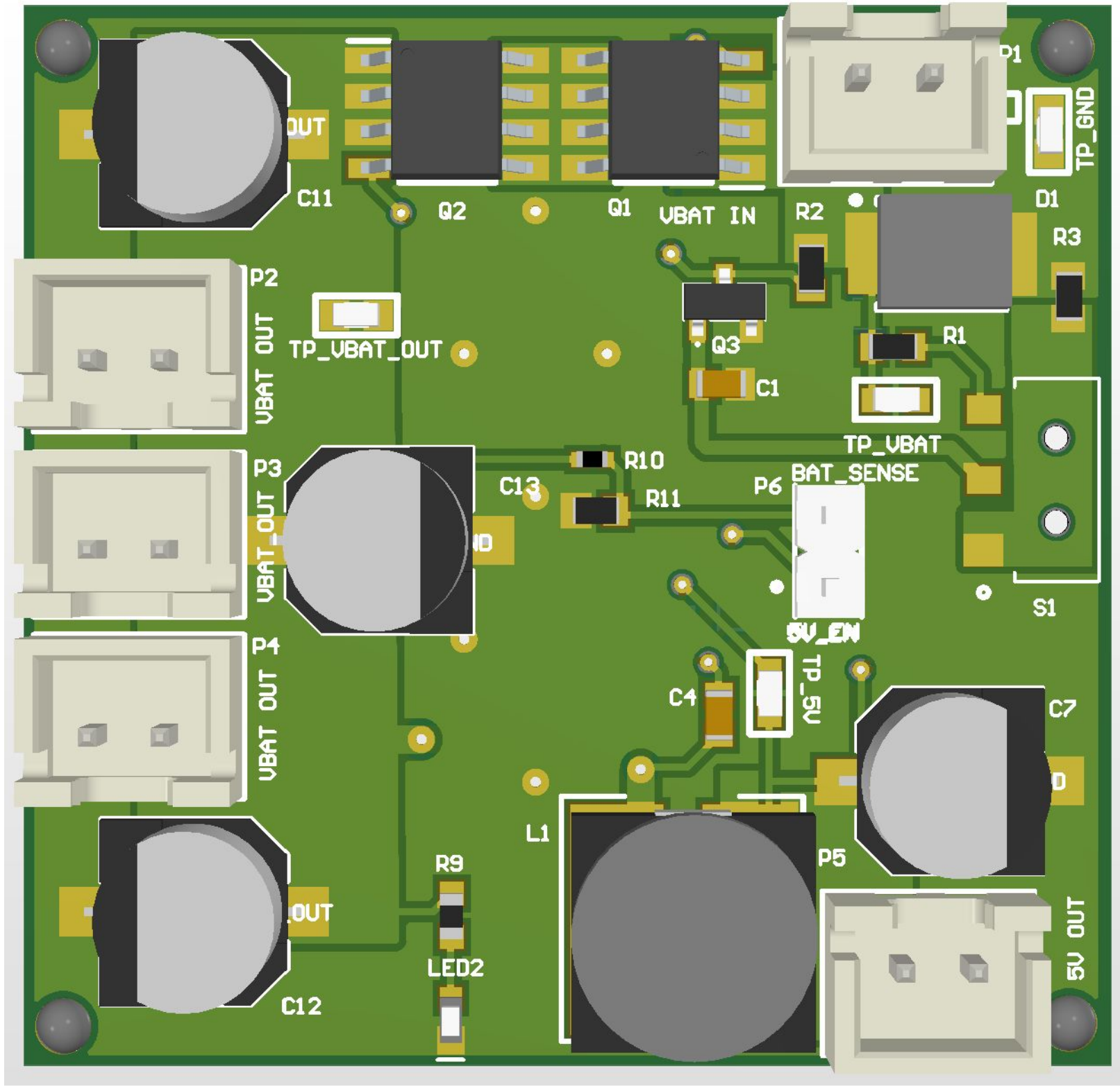
TITLE: Power Distribution Board

SIZE	CAGE CODE	DWG NO.	REV
B			

SCALE: | FILE NAME: Sheet1.SchDoc | SHEET 1 OF 1






P1
TP_GND
D1
R3
R2
VBAT IN
Q2
Q1
C11
OUT
P2
VBAT OUT
TP_VBAT_OUT
Q3
C1
R1
TP_VBAT
P3
VBAT_OUT
C13
R10
R11
P6
BAT_SENSE
S1
5V_EN
P4
VBAT OUT
C4
TP_5V
C7
L1
P5
R9
LED2
C12
5V OUT

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad Q3-3(24.875mm,28.15mm) on Top Layer And Track (25.375mm,27.8mm)(26.325mm,27.8mm) on Top Overlay [Top Overlay] to [Top Solder]
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_5V-1(26.475mm,12.475mm) on Top Layer And Track (25.775mm,11.8mm)(25.775mm,14.7mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad TP_5V-1(26.475mm,12.475mm) on Top Layer And Track (25.775mm,11.8mm)(27.175mm,11.8mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_5V-1(26.475mm,12.475mm) on Top Layer And Track (27.175mm,11.8mm)(27.175mm,14.7mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_5V-1(26.475mm,14.025mm) on Top Layer And Track (25.775mm,11.8mm)(25.775mm,14.7mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad TP_5V-1(26.475mm,14.025mm) on Top Layer And Track (25.775mm,14.7mm)(27.175mm,14.7mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_5V-1(26.475mm,14.025mm) on Top Layer And Track (27.175mm,11.8mm)(27.175mm,14.7mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_GND-1(36.375mm,32.425mm) on Top Layer And Track (35.675mm,31.75mm)(35.675mm,34.65mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad TP_GND-1(36.375mm,32.425mm) on Top Layer And Track (35.675mm,31.75mm)(37.075mm,31.75mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_GND-1(36.375mm,32.425mm) on Top Layer And Track (37.075mm,31.75mm)(37.075mm,34.65mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_GND-1(36.375mm,33.975mm) on Top Layer And Track (35.675mm,31.75mm)(35.675mm,34.65mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad TP_GND-1(36.375mm,33.975mm) on Top Layer And Track (35.675mm,34.65mm)(37.075mm,34.65mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_GND-1(36.375mm,33.975mm) on Top Layer And Track (37.075mm,31.75mm)(37.075mm,34.65mm) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad TP_VBAT_OUT-1(11.025mm,26.675mm) on Top Layer And Track (10.35mm,25.975mm)(10.35mm,27.375mm) on Top Overlay [Top Overlay]
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_VBAT_OUT-1(11.025mm,26.675mm) on Top Layer And Track (10.35mm,25.975mm)(13.25mm,25.975mm) on Top Overlay [Top Overlay]
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_VBAT_OUT-1(11.025mm,26.675mm) on Top Layer And Track (10.35mm,27.375mm)(13.25mm,27.375mm) on Top Overlay [Top Overlay]
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_VBAT_OUT-1(12.575mm,26.675mm) on Top Layer And Track (10.35mm,25.975mm)(13.25mm,25.975mm) on Top Overlay [Top Overlay]
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_VBAT_OUT-1(12.575mm,26.675mm) on Top Layer And Track (10.35mm,27.375mm)(13.25mm,27.375mm) on Top Overlay [Top Overlay]
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad TP_VBAT_OUT-1(12.575mm,26.675mm) on Top Layer And Track (13.25mm,25.975mm)(13.25mm,27.375mm) on Top Overlay [Top Overlay]
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad TP_VBAT-1(30.15mm,23.675mm) on Top Layer And Track (29.475mm,22.975mm)(29.475mm,24.375mm) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_VBAT-1(30.15mm,23.675mm) on Top Layer And Track (29.475mm,22.975mm)(32.375mm,22.975mm) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_VBAT-1(30.15mm,23.675mm) on Top Layer And Track (29.475mm,24.375mm)(32.375mm,24.375mm) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_VBAT-1(31.7mm,23.675mm) on Top Layer And Track (29.475mm,22.975mm)(32.375mm,22.975mm) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad TP_VBAT-1(31.7mm,23.675mm) on Top Layer And Track (29.475mm,24.375mm)(32.375mm,24.375mm) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad TP_VBAT-1(31.7mm,23.675mm) on Top Layer And Track (32.375mm,22.975mm)(32.375mm,24.375mm) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U2-1(22.85mm,11.85mm) on Bottom Layer And Track (20.5mm,12.475mm)(23.3mm,12.475mm) on Bottom Overlay [Bottom Overlay] to [Bottom
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad U2-1(22.85mm,11.85mm) on Bottom Layer And Track (23.3mm,12.475mm)(23.3mm,13.475mm) on Bottom Overlay [Bottom Overlay] to
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U2-2(21.9mm,11.85mm) on Bottom Layer And Track (20.5mm,12.475mm)(23.3mm,12.475mm) on Bottom Overlay [Bottom Overlay] to [Bottom
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad U2-3(20.95mm,11.85mm) on Bottom Layer And Track (20.5mm,12.475mm)(20.5mm,13.475mm) on Bottom Overlay [Bottom Overlay] to
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U2-3(20.95mm,11.85mm) on Bottom Layer And Track (20.5mm,12.475mm)(23.3mm,12.475mm) on Bottom Overlay [Bottom Overlay] to [Bottom
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad U2-4(20.95mm,14.1mm) on Bottom Layer And Track (20.5mm,12.475mm)(20.5mm,13.475mm) on Bottom Overlay [Bottom Overlay] to [Bottom
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U2-4(20.95mm,14.1mm) on Bottom Layer And Track (20.5mm,13.475mm)(23.3mm,13.475mm) on Bottom Overlay [Bottom Overlay] to [Bottom
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U2-5(21.9mm,14.1mm) on Bottom Layer And Track (20.5mm,13.475mm)(23.3mm,13.475mm) on Bottom Overlay [Bottom Overlay] to [Bottom
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U2-6(22.85mm,14.1mm) on Bottom Layer And Track (20.5mm,13.475mm)(23.3mm,13.475mm) on Bottom Overlay [Bottom Overlay] to [Bottom
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad U2-6(22.85mm,14.1mm) on Bottom Layer And Track (23.3mm,12.475mm)(23.3mm,13.475mm) on Bottom Overlay [Bottom Overlay] to [Bottom

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "5V_EN" (27.15mm,15.108mm) on Top Overlay And Text "5V_EN" (27.239mm,15.199mm) on Top Overlay Silk Text to Silk Clearance [0mm]
Silk To Silk Clearance Constraint: (0.223mm < 0.254mm) Between Text "5V_EN" (27.15mm,15.108mm) on Top Overlay And Track (25.775mm,14.7mm)(27.175mm,14.7mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.223mm < 0.254mm) Between Text "5V_EN" (27.15mm,15.108mm) on Top Overlay And Track (27.175mm,11.8mm)(27.175mm,14.7mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.189mm < 0.254mm) Between Text "5V_EN" (27.15mm,15.108mm) on Top Overlay And Track (27.38mm,15.96mm)(27.38mm,20.63mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.099mm < 0.254mm) Between Text "5V_EN" (27.239mm,15.199mm) on Top Overlay And Track (27.38mm,15.96mm)(27.38mm,20.63mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.138mm < 0.254mm) Between Text "5V_EN" (27.239mm,15.199mm) on Top Overlay And Track (29.72mm,15.96mm)(29.72mm,20.63mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.041mm < 0.254mm) Between Text "BAT_SENSE" (27.35mm,20.833mm) on Top Overlay And Track (27.38mm,15.96mm)(27.38mm,20.63mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.074mm < 0.254mm) Between Text "BAT_SENSE" (27.35mm,20.833mm) on Top Overlay And Track (29.72mm,15.96mm)(29.72mm,20.63mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.146mm < 0.254mm) Between Text "C7" (36.458mm,12.45mm) on Top Overlay And Track (36.15mm,11.2mm)(36.15mm,13.425mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "LED3" (37.691mm,16.55mm) on Bottom Overlay And Track (36.783mm,16.534mm)(37.693mm,16.534mm) on Bottom Overlay Silk Text to Silk
Silk To Silk Clearance Constraint: (0.176mm < 0.254mm) Between Text "P1" (34.667mm,35.725mm) on Top Overlay And Track (34.328mm,31.346mm)(34.328mm,37.188mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.149mm < 0.254mm) Between Text "P2" (8.133mm,27.775mm) on Top Overlay And Track (0.347mm,28.379mm)(7.84mm,28.379mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.131mm < 0.254mm) Between Text "P2" (8.133mm,27.775mm) on Top Overlay And Track (7.84mm,22.537mm)(7.84mm,28.379mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Text "P4" (8.208mm,14.675mm) on Top Overlay And Track (0.347mm,15.329mm)(7.84mm,15.329mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.206mm < 0.254mm) Between Text "P4" (8.208mm,14.675mm) on Top Overlay And Track (7.84mm,9.487mm)(7.84mm,15.329mm) on Top Overlay Silk Text to Silk Clearance [0.206mm]
Silk To Silk Clearance Constraint: (0.17mm < 0.254mm) Between Text "TP_GND" (37.908mm,31.884mm) on Top Overlay And Track (35.675mm,31.75mm)(37.075mm,31.75mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.144mm < 0.254mm) Between Text "TP_GND" (37.908mm,31.884mm) on Top Overlay And Track (35.675mm,34.65mm)(37.075mm,34.65mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.144mm < 0.254mm) Between Text "TP_GND" (37.908mm,31.884mm) on Top Overlay And Track (37.075mm,31.75mm)(37.075mm,34.65mm) on Top Overlay Silk Text to Silk Clearance
Silk To Silk Clearance Constraint: (0.105mm < 0.254mm) Between Text "TP_VBAT_OUT" (9.459mm,25.217mm) on Top Overlay And Track (10.35mm,25.975mm)(10.35mm,27.375mm) on Top Overlay Silk Text to Silk
Silk To Silk Clearance Constraint: (0.069mm < 0.254mm) Between Text "TP_VBAT_OUT" (9.459mm,25.217mm) on Top Overlay And Track (10.35mm,25.975mm)(13.25mm,25.975mm) on Top Overlay Silk Text to Silk
Silk To Silk Clearance Constraint: (0.199mm < 0.254mm) Between Text "TP_VBAT_OUT" (9.459mm,25.217mm) on Top Overlay And Track (13.25mm,25.975mm)(13.25mm,27.375mm) on Top Overlay Silk Text to Silk