University of Central Florida

Department of Computer Science

CDA 5106: Spring 2020

Machine Problem 1: Cache Design, Memory Hierarchy Design

by

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Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

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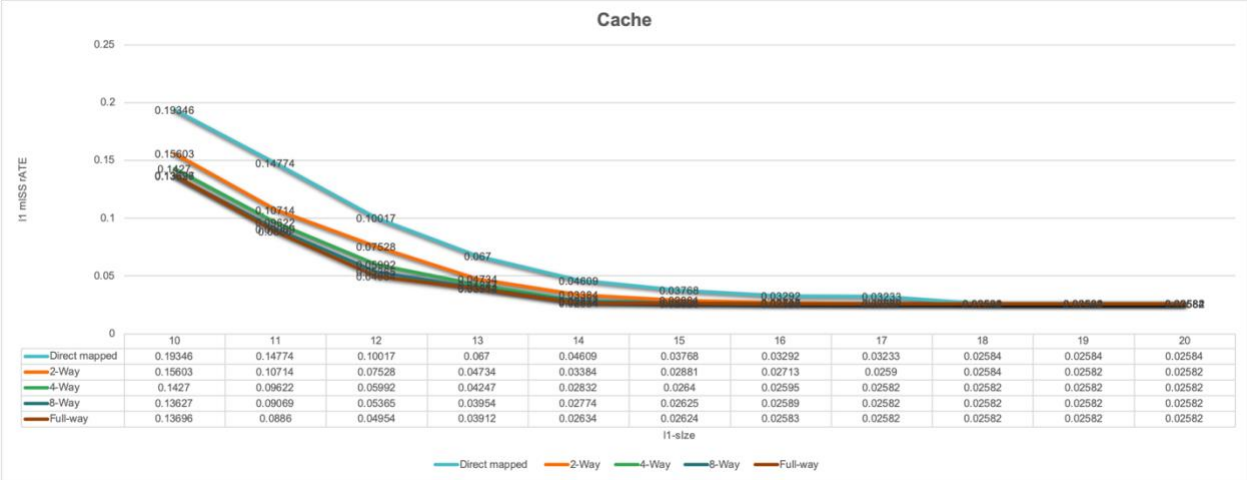
(sign by typing your name)

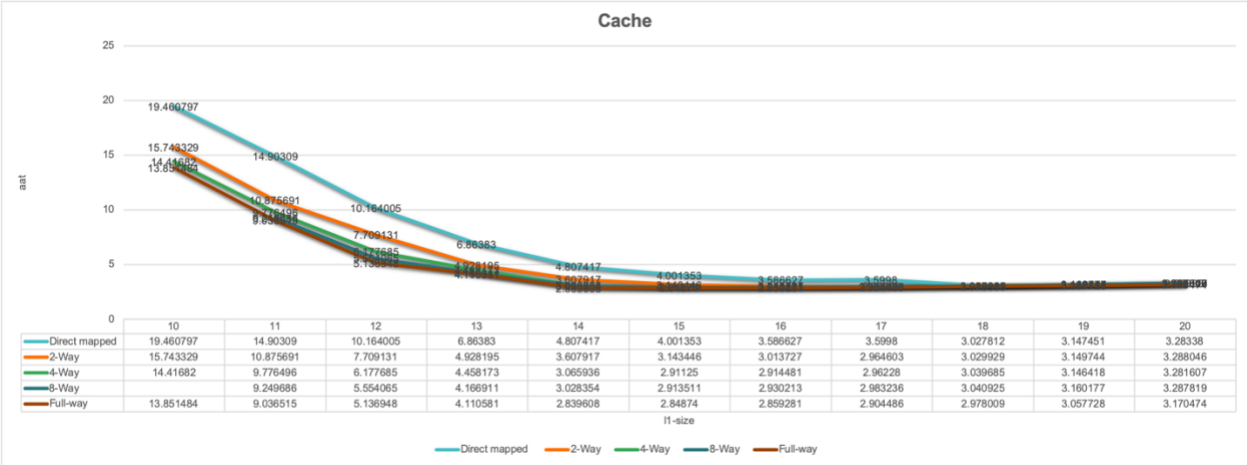
1.L1 cache exploration : SIZE and ASSOC on miss rate.



	10	11	12	13	14	15	16	17	18	19	20
Direct mapped	0.19346	0.14774	0.10017	0.067	0.04609	0.03768	0.03292	0.03233	0.02584	0.02584	0.02584
2-Way	0.15603	0.10714	0.07528	0.04734	0.03384	0.02881	0.02713	0.0259	0.02584	0.02582	0.02582
4-Way	0.1427	0.09622	0.05992	0.04247	0.02832	0.0264	0.02595	0.02582	0.02582	0.02582	0.02582
8-Way	0.13627	0.09069	0.05365	0.03954	0.02774	0.02625	0.02589	0.02582	0.02582	0.02582	0.02582
Full-way	0.13696	0.0886	0.04954	0.03912	0.02634	0.02624	0.02583	0.02582	0.02582	0.02582	0.02582

1. As we can see, as the cache size increases for each associativity , the miss rate reduces exponentially until a point and then remains constant.
2. For, cache having fixed size as the associativity increases the miss rate reduces significantly initially but stabilizes afterwards.

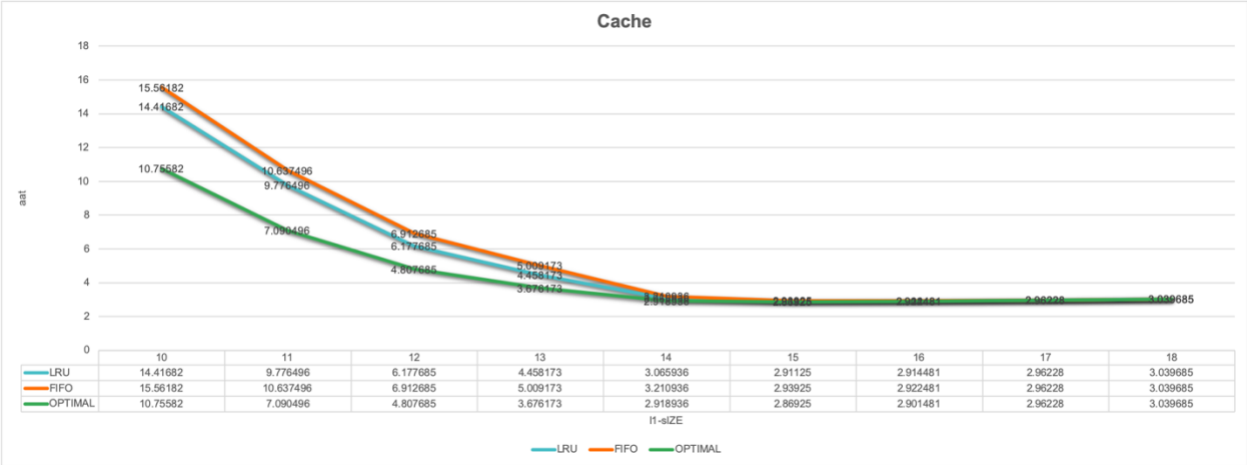
2.L1 cache exploration : SIZE and ASSOC on AAT



	10	11	12	13	14	15	16	17	18	19	20
Direct mapped	19.460797	14.90309	10.164005	6.86383	4.807417	4.001353	3.586627	3.5998	3.027812	3.147451	3.28338
2-Way	15.743329	10.875691	7.709131	4.928195	3.607917	3.143446	3.013727	2.964603	3.029929	3.149744	3.288046
4-Way	14.41682	9.776496	6.177685	4.458173	3.065936	2.91125	2.914481	2.96228	3.039685	3.146418	3.281607
8-Way		9.249686	5.554065	4.166911	3.028354	2.913511	2.930213	2.983236	3.040925	3.160177	3.287819
Full-way	13.851484	9.036515	5.136948	4.110581	2.839608	2.84874	2.859281	2.904486	2.978009	3.057728	3.170474

1. The cache configuration of only L1 Cache and Block size = 32 gives lowest AAT.
2. Associativity is Fully Associative and AAT is 2.839608.

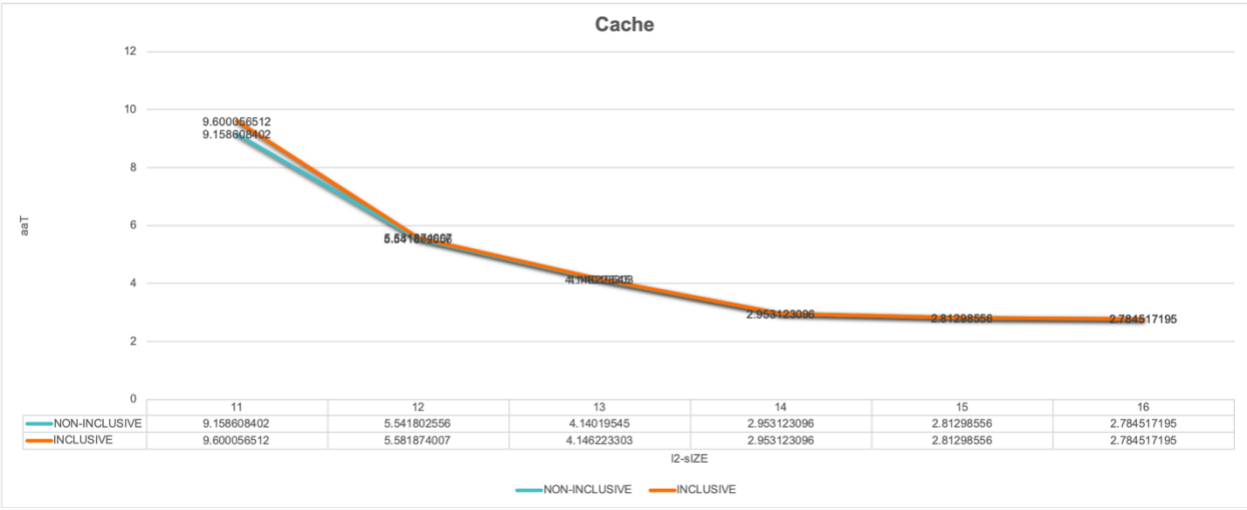
3.Replacement policy study



	10	11	12	13	14	15	16	17	18
LRU	14.41682	9.776496	6.177685	4.458173	3.065936	2.91125	2.914481	2.96228	3.039685
FIFO	15.56182	10.637496	6.912685	5.009173	3.210936	2.93925	2.922481	2.96228	3.039685
OPTIMAL	10.75582	7.090496	4.807685	3.676173	2.918936	2.86925	2.901481	2.96228	3.039685

1. AAT is lowest for the Optimal replacement policy. The gap decreases afterwards for large size caches.
2. LRU replacement policy is the second best after Optimal.

4.Inclusion property study



	11	12	13	14	15	16
NON-INCLUSIVE	9.158608402	5.541802556	4.14019545	2.953123096	2.81298556	2.784517195
INCLUSIVE	9.600056512	5.581874007	4.146223303	2.953123096	2.81298556	2.784517195

1. AAT is higher for inclusive property than non-inclusive property. But as the cache size increases, the gap between them decreases.
2. Inclusive property works better with systems having multiple cache and cores. Non-inclusive is good for cache with small size.