VLSI PRACTICE

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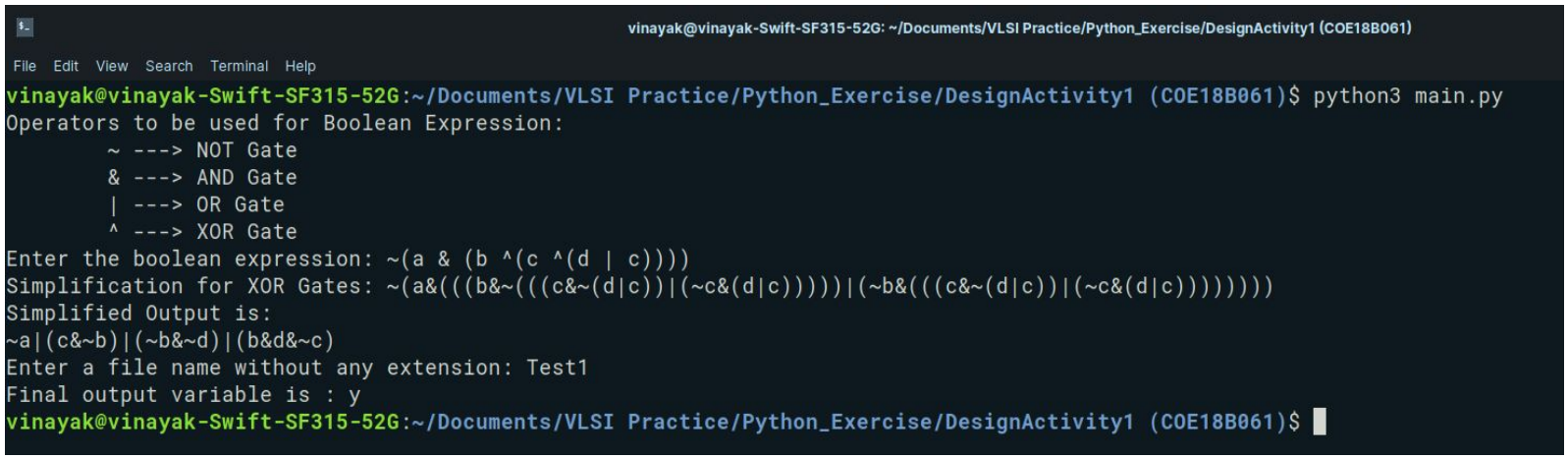
Design Activity 1 ***Date: 30th September 2020***

Expression to IRSIM File Generator

Output 1:



Irsim File: Test1.sim

```
p a vdd na 2 4
n a na gnd 2 4
p b vdd nb 2 4
n b nb gnd 2 4
p d vdd nd 2 4
n d nd gnd 2 4
p c vdd nc 2 4
n c nc gnd 2 4
p c vdd n1 2 4
p nb vdd n1 2 4
n c n1 n0 2 4
n nb n0 gnd 2 4
```

```
p n1 vdd n2 2 4
n n1 gnd n2 2 4

p nb vdd n4 2 4
p nd vdd n4 2 4
n nb n4 n3 2 4
n nd n3 gnd 2 4

p n4 vdd n5 2 4
n n4 gnd n5 2 4

p b vdd n7 2 4
p d vdd n7 2 4
n b n7 n6 2 4
n d n6 gnd 2 4

p n7 vdd n8 2 4
n n7 gnd n8 2 4

p n8 vdd n10 2 4
p nc vdd n10 2 4
n n8 n10 n9 2 4
n nc n9 gnd 2 4

p n10 vdd n11 2 4
n n10 gnd n11 2 4

p na vdd n12 2 4
p n2 n12 n13 2 4
n na n13 gnd 2 4
n n2 n13 gnd 2 4

p n13 vdd n14 2 4
n n13 gnd n14 2 4

p n14 vdd n15 2 4
p n5 n15 n16 2 4
n n14 n16 gnd 2 4
n n5 n16 gnd 2 4

p n16 vdd n17 2 4
n n16 gnd n17 2 4
```

p n17 vdd n18 2 4
p n11 n18 n19 2 4
n n17 n19 gnd 2 4
n n11 n19 gnd 2 4

p n19 vdd y 2 4
n n19 gnd y 2 4

Output 2:

Irsim File: Test2.sim

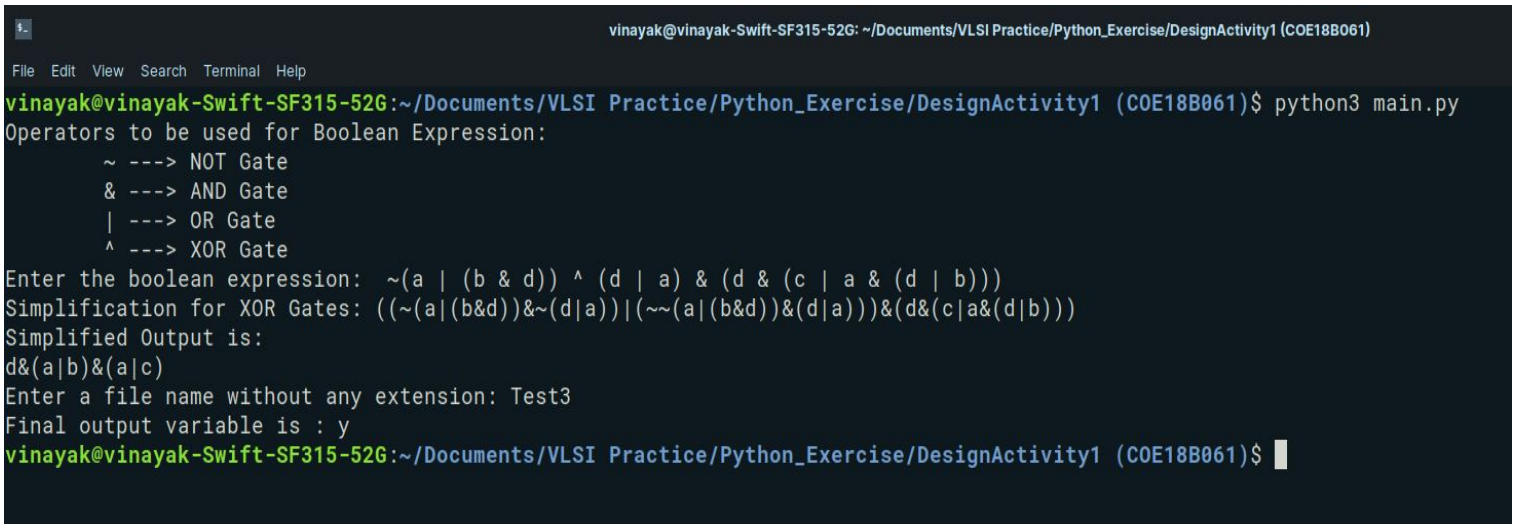
p a vdd na 2 4
n a na gnd 2 4
p b vdd n0 2 4
p d n0 n1 2 4
n b n1 gnd 2 4
n d n1 gnd 2 4

p n1 vdd n2 2 4
n n1 gnd n2 2 4

p n2 vdd n3 2 4
p na n3 n4 2 4
n n2 n4 gnd 2 4
n na n4 gnd 2 4

p n4 vdd y 2 4
n n4 gnd y 2 4

Output 3:



Irsim File: Test3.sim

p a vdd n0 2 4
p b n0 n1 2 4
n a n1 gnd 2 4
n b n1 gnd 2 4

p n1 vdd n2 2 4
n n1 gnd n2 2 4

p a vdd n3 2 4
p c n3 n4 2 4
n a n4 gnd 2 4
n c n4 gnd 2 4

p n4 vdd n5 2 4
n n4 gnd n5 2 4

p d vdd n7 2 4
p n2 vdd n7 2 4
n d n7 n6 2 4

n n2 n6 gnd 2 4

p n7 vdd n8 2 4
n n7 gnd n8 2 4

p n8 vdd n10 2 4
p n5 vdd n10 2 4
n n8 n10 n9 2 4
n n5 n9 gnd 2 4

p n10 vdd y 2 4
n n10 gnd y 2 4