



AVR Peripherals

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Logistics

- Google code: Hope everyone has commit privileges
- Introductory lab session
 - How was it?
 - Program in either arduino or C - C is preferable since generally people say that arduino gets limited when doing complex stuff
- First assignment due date postponed to January 26 (demo on January 27)
 - Take ownership for purchasing stuff for the class in rotation: Check with me for common stuff for the class - We will reimburse such expenses
 - Rest of the deadlines remain
 - Be ready to explain your code - even the downloaded code
 - Put the log message as final submitted code for your final submission
- Quiz next time in the class for 20-30 minutes



Revision

■ Explain the following:

- Boot loader
- AVR fuses
- What are some fuse register parameters?

■ Clocks:

- What are the different clocks distributed in AVR?
- What are the different sources of clocks in AVR?

■ Sleep modes:

- What are different sleep modes?
- What is the function of Power Reduction Register (PRR)?

■ Interrupts:

- How is priority of interrupts decided?
- What are multiple sources of external interrupts?



Timer/Counter0

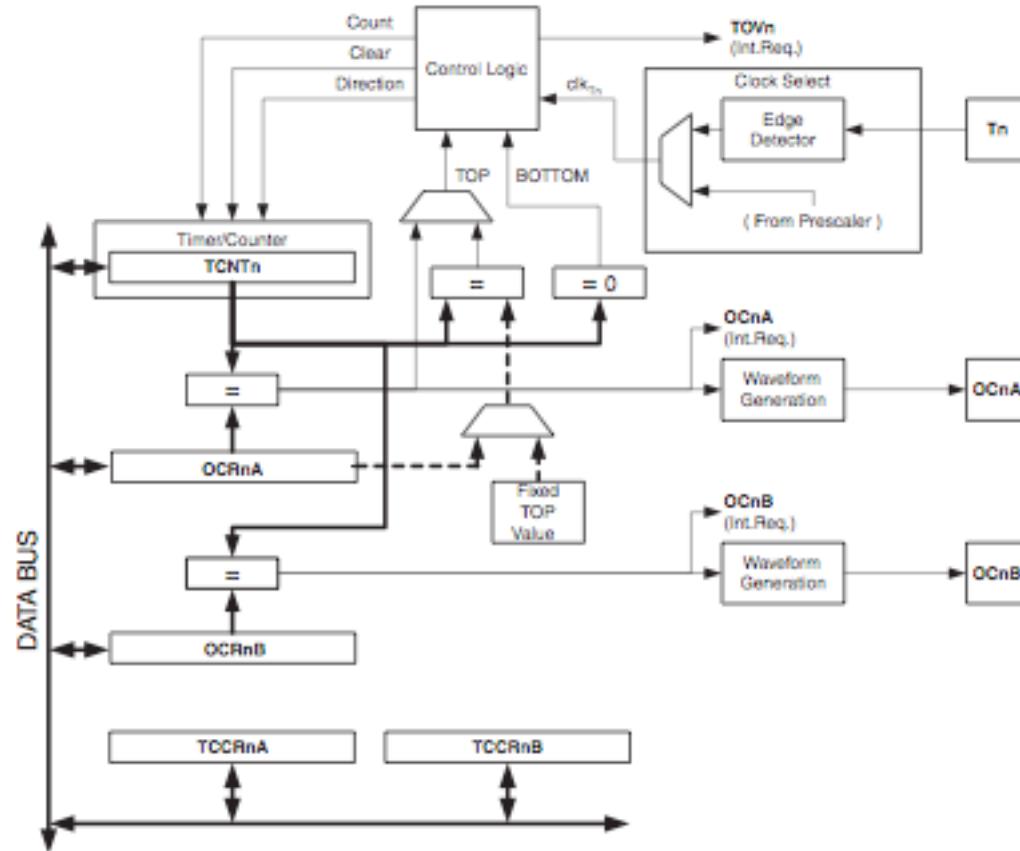
- General purpose 8 bit timer/counter module
- Two independent output compare units
- Support for PWM
- Some definitions:

BOTTOM	The counter reaches the BOTTOM when it becomes 0x00.
MAX	The counter reaches its MAXimum when it becomes 0xFF (decimal 255).
TOP	The counter reaches the TOP when it becomes equal to the highest value in the count sequence. The TOP value can be assigned to be the fixed value 0xFF (MAX) or the value stored in the OCR0A Register. The assignment is dependent on the mode of operation.

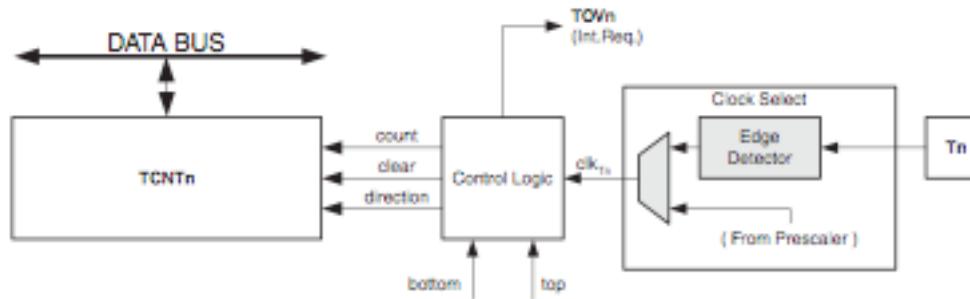
- Clock source: Internal/External (T0 Pin)
 - Controlled by Clock Select (CS02:0) bits located in Timer Counter Control Register (TCCR0B)
 - Double buffered Output Compare Registers (OCR0A, OCR0B) are compared with timer/counter values at all times



Timer/Counter0: Block Diagram



Counter Unit



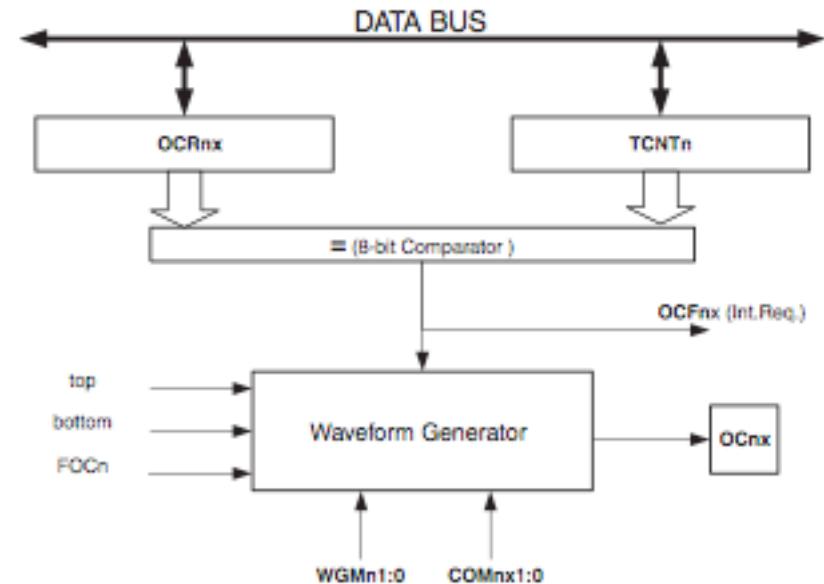
- Main part of 8-bit Timer/Counter is the programmable counter unit
- Signal description:

count	Increment or decrement TCNT0 by 1.
direction	Select between increment and decrement.
clear	Clear TCNT0 (set all bits to zero).
clk_{Tn}	Timer/Counter clock, referred to as clk_{T0} in the following.
top	Signalize that TCNT0 has reached maximum value.
bottom	Signalize that TCNT0 has reached minimum value (zero).

- Depending on mode of operation, counter is cleared, incremented or decremented at each timer clock

Output Compare Unit

- Continuously compare TCNT0 with Output Compare Registers (OCR0A, OCR0B)
- A match will set the Output Compare Flag (OCF0A) at the next timer clock cycle
- If the corresponding interrupt is enabled, OCF generates an Output Compare Interrupt
 - OCF is automatically cleared when the interrupt is executed
 - Waveform Generator uses the match signal to generate an output according to output modes set by WGM02:0 bits and Compare Output Mode (COM01:0)
 - Match output of comparator can be forced by writing a one to Force Output Compare (FOC0) bit



Modes of Operation: Normal

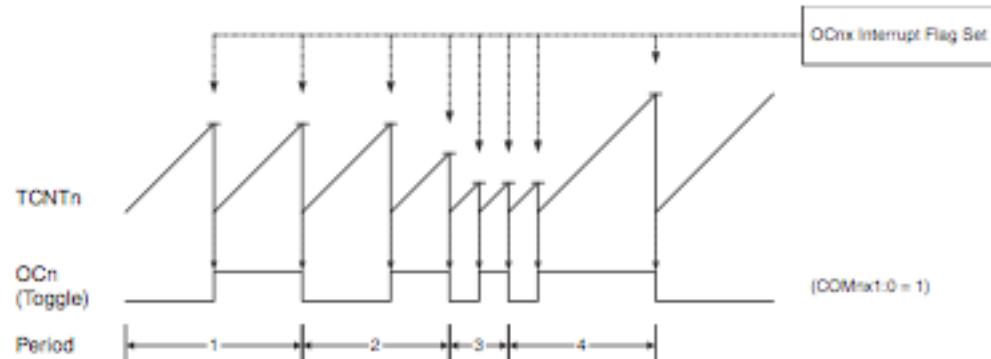
- Modes of operation defined by combination of Waveform Generation Mode (WGM02:0) and Compare Output Mode (COM01:0)
- Normal Mode: WGM0 = 0
 - Counting direction is up
 - No counter clear performed: Counter overruns when it passes its maximum value; Timer/Counter Overflow Flag (TOV0) will be set in the same cycle as TCNT0 becomes 0
 - Output Compare Unit can be used to generate interrupt at some given time



Modes of Operation: CTC

■ Clear Timer on Capture Match (CTC) Mode: WGM0 = 2;

- Counter is cleared to zero when TCNT0 value matches OCR0A value
- OCR0A defines the top value and hence also its resolution
- An interrupt can be generated each time the counter reaches the TOP value using OCF0A Flag

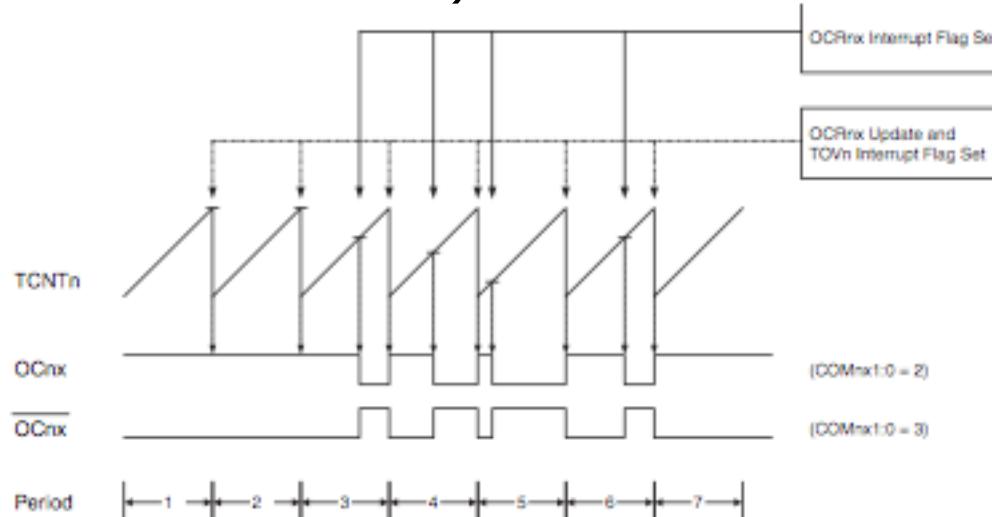


- For generating a waveform, OC0A can be set to toggle on each compare match using COM0A = 1

- Waveform generated will have a maximum value frequency of $f_{OC0} = f_{CLK_I/O}/2$ when OCR0A is set to 0; Generalizing:
$$f_{OCn} = f_{CLK_I/O}/(2 * n * (1 + OCR_n))$$
 [n - prescaler factor]

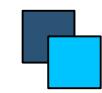
Modes of Operation: Fast PWM

- Fast Pulse Width Modulation Mode: WGM0 = 3 or 7;
 - Counter counts from BOTTOM to TOP (defined as 0xFF when WGM0 is 3 and OCR0A when WGM is 7)

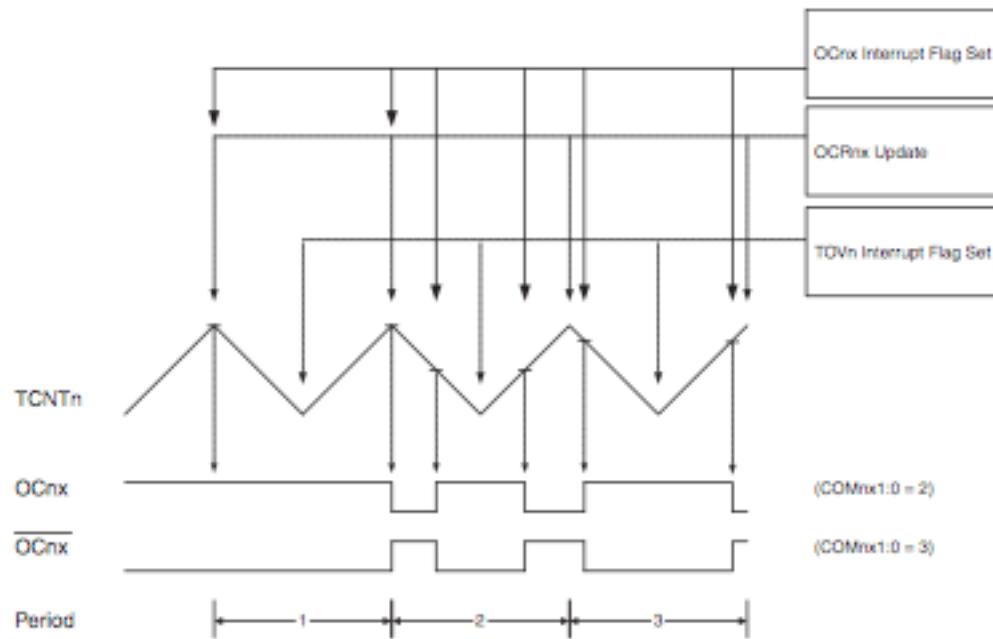


- Non-inverting compare output mode (COM0 = 2), OC0 is cleared on compare match and set at ZERO
- Inverting compare output mode (COM0 = 3), OC0 is set on compare match and cleared at ZERO
- OCR0A = BOTTOM: Narrow spike for each MAX+1 timer clock cycle
- OCR0A = MAX: Constantly high/low output

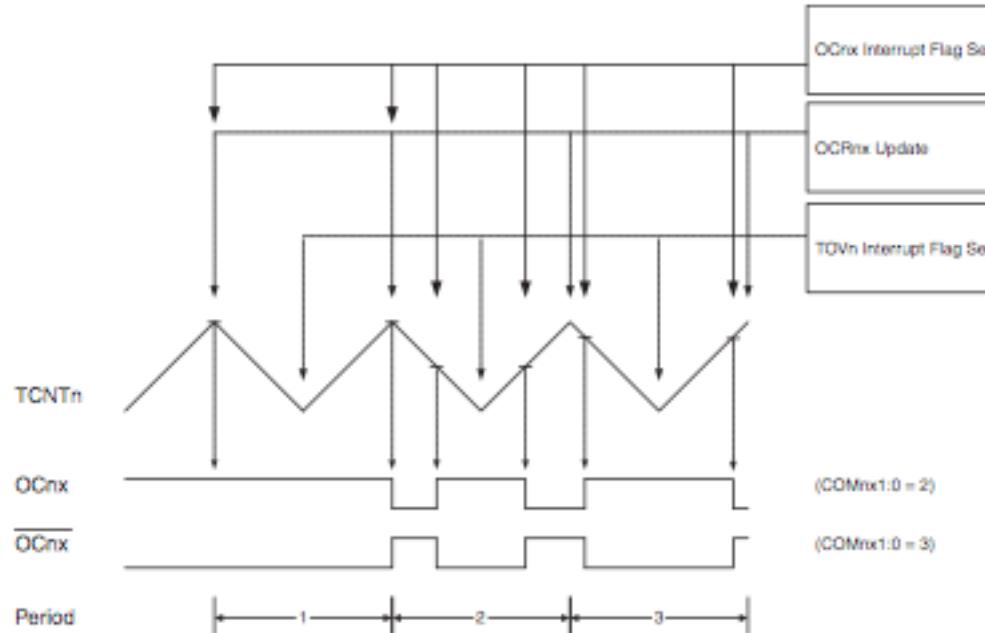
Modes of Operation: Phase Correct PWM



- Phase Correct Pulse Width Modulation Mode: WGM0 = 1 or 5;
 - Counter counts from BOTTOM to TOP and then from TOP to BOTTOM
 - TOP defined as 0xFF when WGM0 = 1 and OCR0A when WGM0 = 5

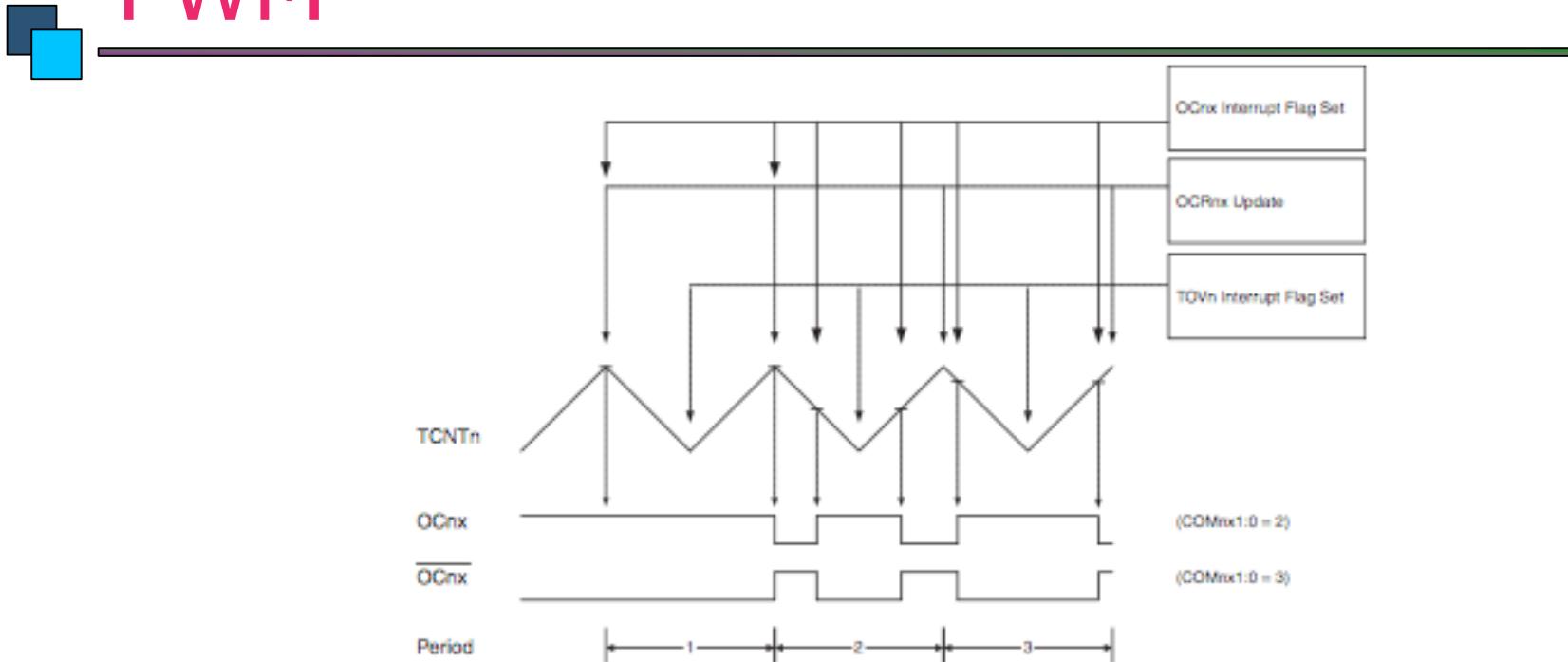


Modes of Operation: Phase Correct PWM



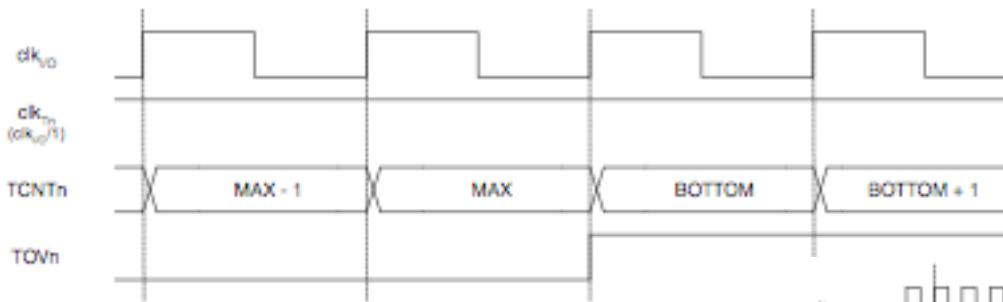
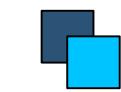
- Non-inverting compare output mode ($\text{COM}0 = 2$), $\text{OC}0$ is cleared on compare match while upcounting and set on compare match while downcounting
- Inverting compare output mode ($\text{COM}0 = 3$), $\text{OC}0$ is set on compare match while upcounting and cleared on compare match while downcounting

Modes of Operation: Phase Correct PWM



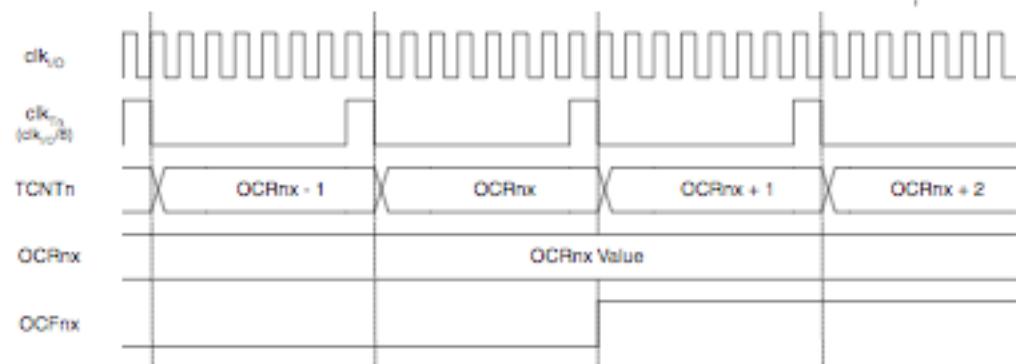
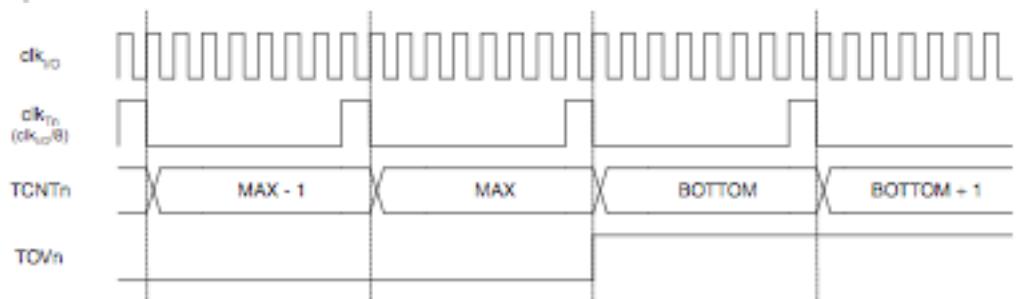
- Extreme values are special cases: BOTTOM - Continuously low; MAX - Continuously high
- Two cases when there is transition without a match as well (to ensure symmetry around BOTTOM):
 - OCR0 changes its value from MAX (as above)
 - Timer starts counting from a value higher than one in OCR0

Timer/Counter - Timing Diagrams



No Prescaling

With Prescaler $f_{\text{clk_I/O}}/8$



Setting of OCF0



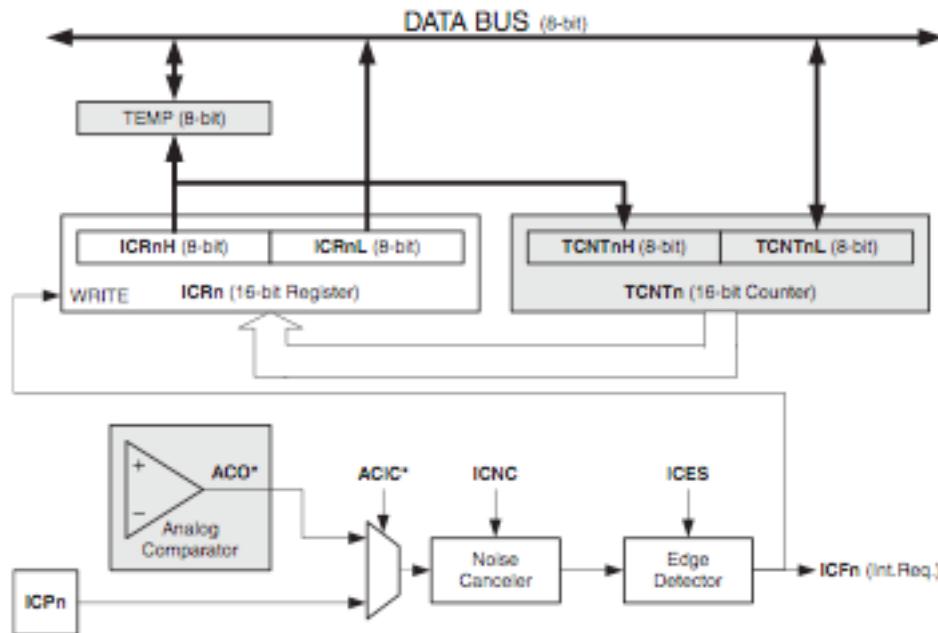
■ Timer/Counter1

- General purpose 16 bit timer/counter module
- Two independent output compare units
- Support for PWM
- Mostly similar to Timer/Counter0
- Additionally, one input capture unit
 - Capture Timer/Counter value at a given external event
- Single temporary register shared for all 16-bit accesses
 - For 16-bit write, high byte must be written before the low byte
 - For 16-bit read, low byte must be read before the high byte



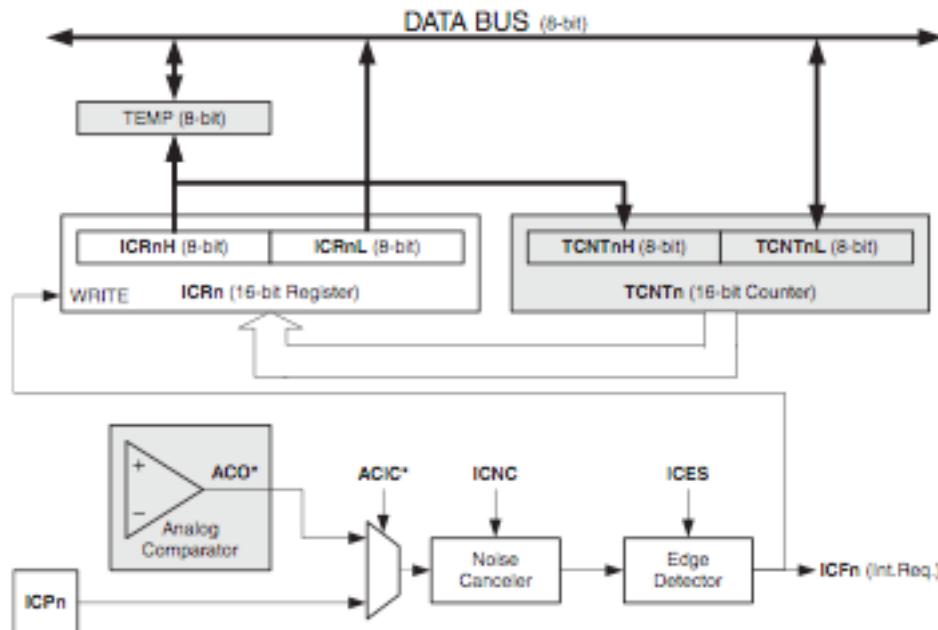
Input Capture Unit

- Capture external events and give them a time stamp indicating time of occurrence
- External signal can be applied via ICP1 pin or via analog-comparator unit by setting Analog Comparator Input Capture (ACIC) bit
- Time stamps can be used to calculate frequency, duty cycle, and other features of signal or for creating the logs



Input Capture Unit

- When a capture is triggered, 16-bit value of counter is written to Input Capture Register (ICR1), Input Capture Flag (ICF1) is set
- Noise canceller improves noise immunity using a simple digital filtering scheme
- If the processor has not read ICR1 value before the next event occurs, the value in the register will be overwritten

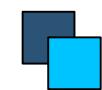


■ Timer/Counter2

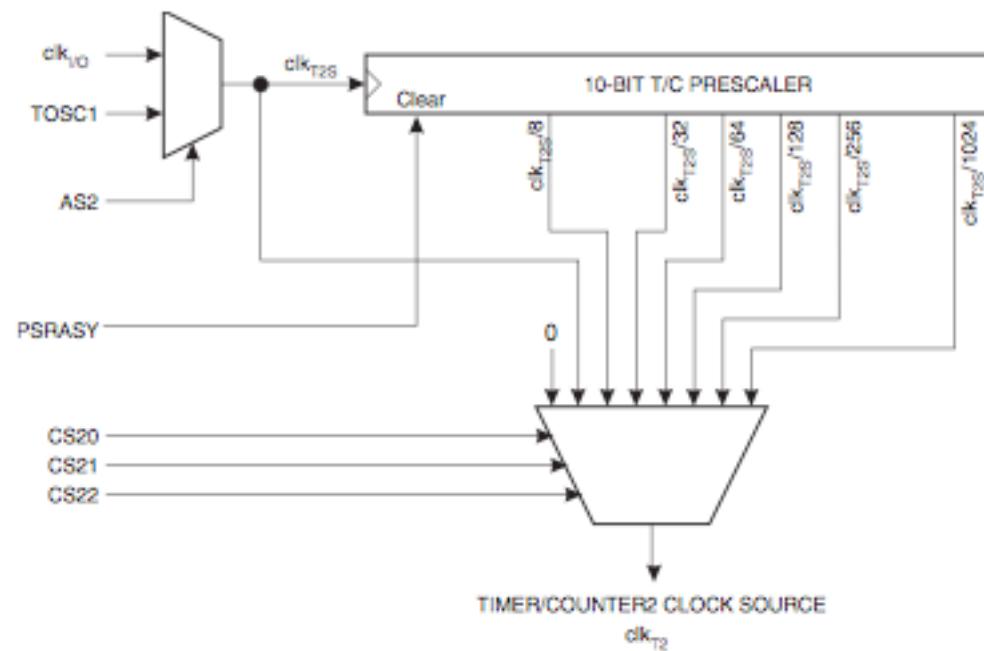
- General purpose 8 bit timer/counter module
- Can be clocked internally via the prescaler or asynchronously clocked from TOSC1/2 pins
 - Asynchronous operation is controlled by Asynchronous Status Register (ASSR)
- Rest same as Timer/Counter0



Timer/Counter2: Asynchronous Operation

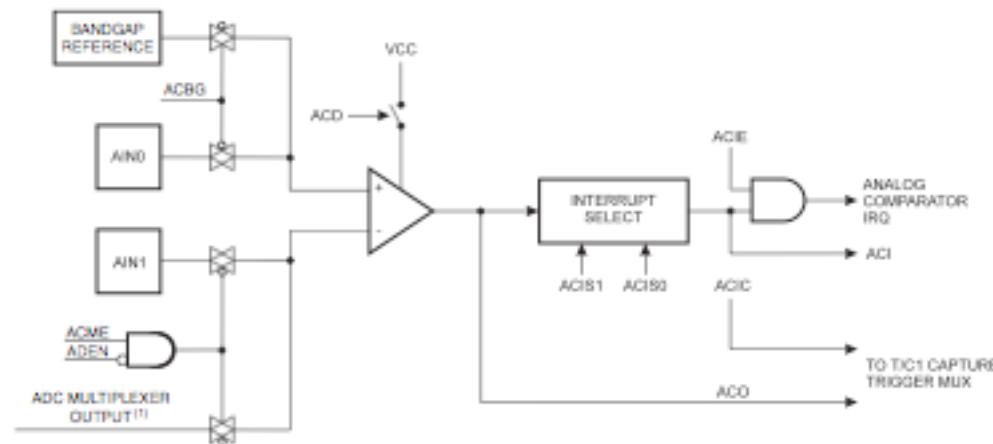


- CPU main clock frequency must be more than 4 times the Oscillator frequency
- Can work with predictable prescaler:



Analog Comparator

- Compares the input values on positive pin AIN0 and negative pin AIN1
- When voltage on AIN0 is greater than that on AIN1, Analog Comparator Output (ACO) is set
- Output can be set to trigger Timer/Counter1 Input Capture function or can also trigger interrupt specific to analog comparator
 - Interrupt triggering can be enabled on output rise, fall or toggle



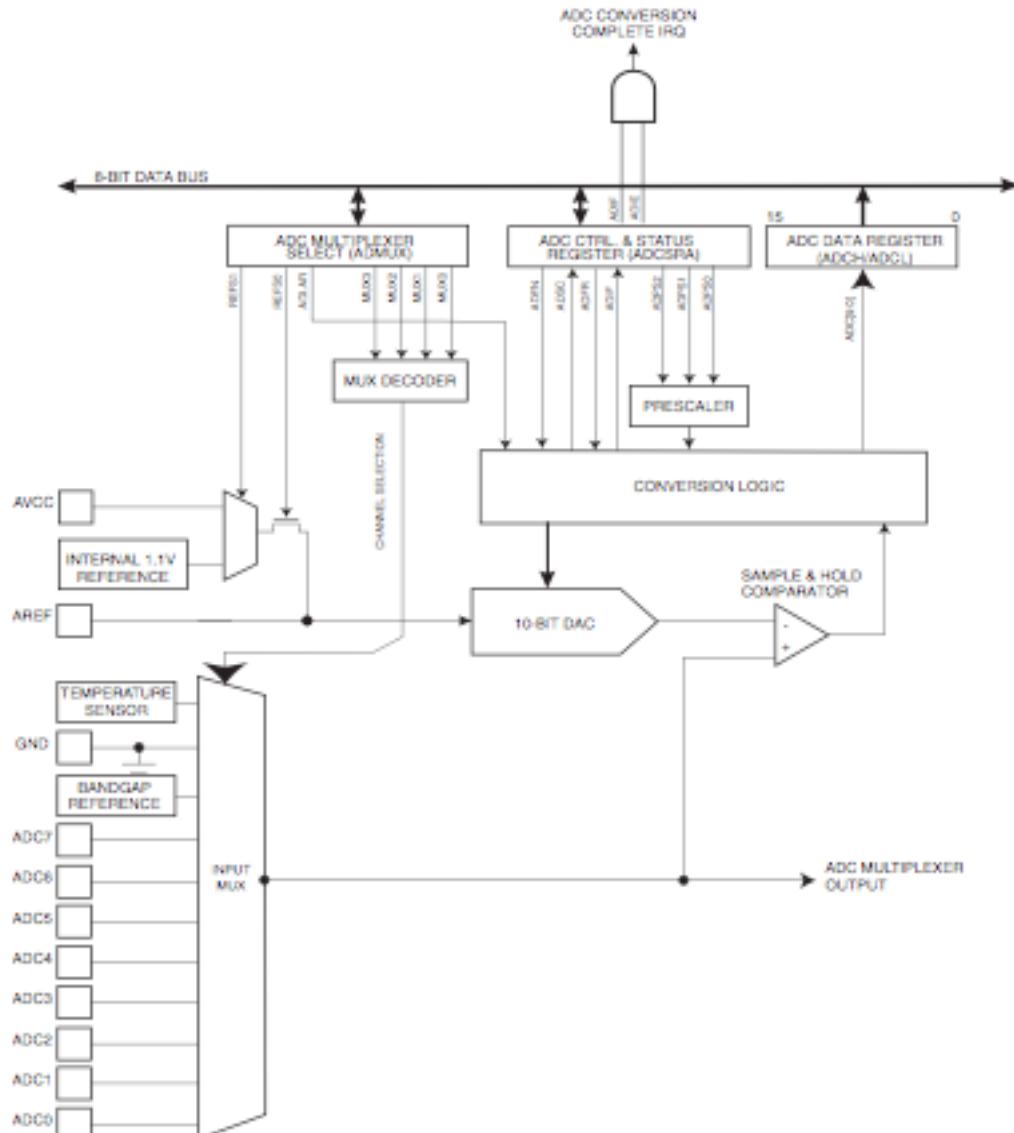
Analog to Digital Converter (ADC)

- 10-bit resolution
- Connected to 8-channel Analog multiplexer allowing eight single ended (0 V reference) voltage inputs constructed from pins of Port A
- Contains sample and hold circuit ensuring that input voltage to ADC is held constant during conversion
- Minimum value represents GND and maximum value approximately the reference voltage
- 13-260 uS conversion time
- Interrupt on ADC conversion complete
- Sleep mode noise canceller
- Up to 76.9 kSPS (up to 15 kSPS at maximum resolution)

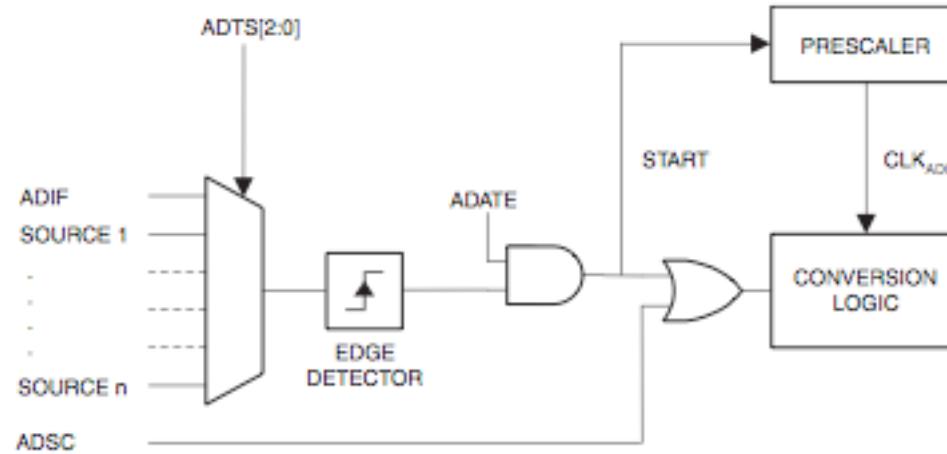


ADC: Block Diagram

- Analog input channel selected by MUX bits in ADMUX
- Enabled by ADC Enable Bit (ADEN) in ADCSRA
- 10-bit result presented to ADC Data Registers ADCH/ADCL
- ADC has its own interrupt that can be triggered when a conversion completes

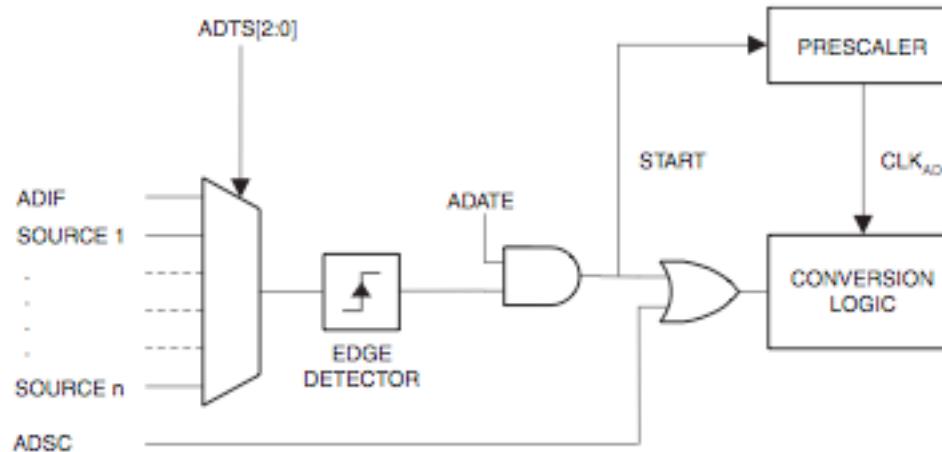


ADC: Starting a Conversion



- Single conversion is started by disabling the Power Reduction ADC (PRADC) and enabling the ADC Start Conversion (ADCSC) bit
 - ADCSC is cleared by hardware when the conversion is complete
- Auto triggering can be enabled by various sources
 - Setting ADC Auto trigger enable bit (ADATE) in ADCSRA
 - Trigger source selected by ADTS bits in ADCSRB
 - When a positive edge occurs on selected trigger signal, ADC prescaler is reset and a conversion is started: Provides a method of starting at fixed intervals

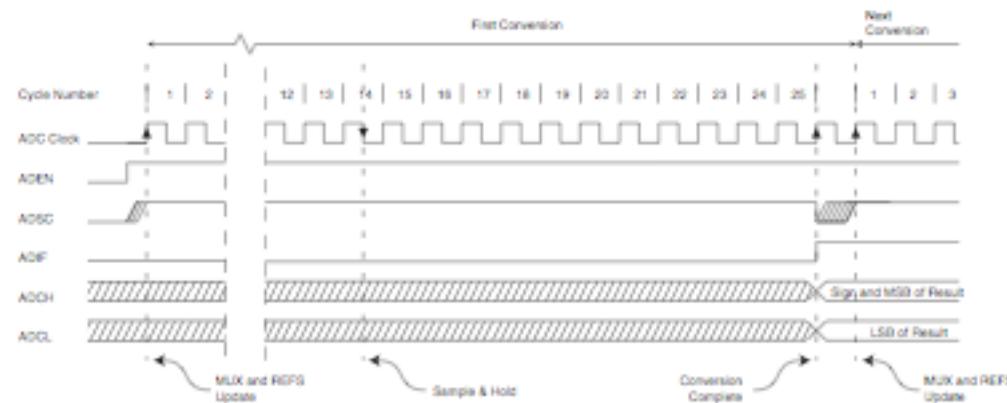
ADC: Auto Triggering



- If another positive edge occurs on trigger signal during conversion, it will be ignored
- If a trigger signal is set when the conversion is complete, a new conversion will not be started
- Using the ADC interrupt flag as a trigger source makes the ADC start a new conversion as soon as the ongoing conversion has finished

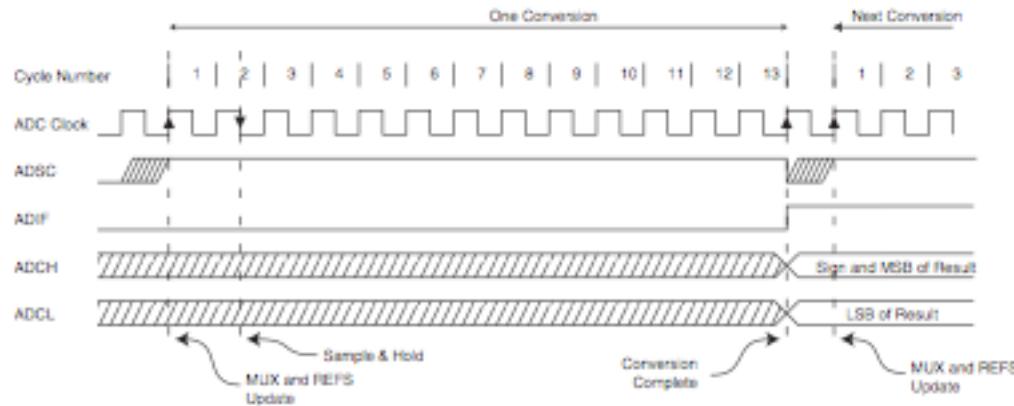
ADC: Conversion Timing

- Successive approximation circuitry requires a clock frequency between 50 KHz and 200 KHz
- ADC modules contains a prescaler that generates an acceptable ADC clock from any CPU frequency higher than 100 KHz
- A normal conversion takes 13 ADC clock cycles
- First conversion after turning on takes 25 ADC clock cycles due to extra time required for initializing analog circuitry (in sample and hold)



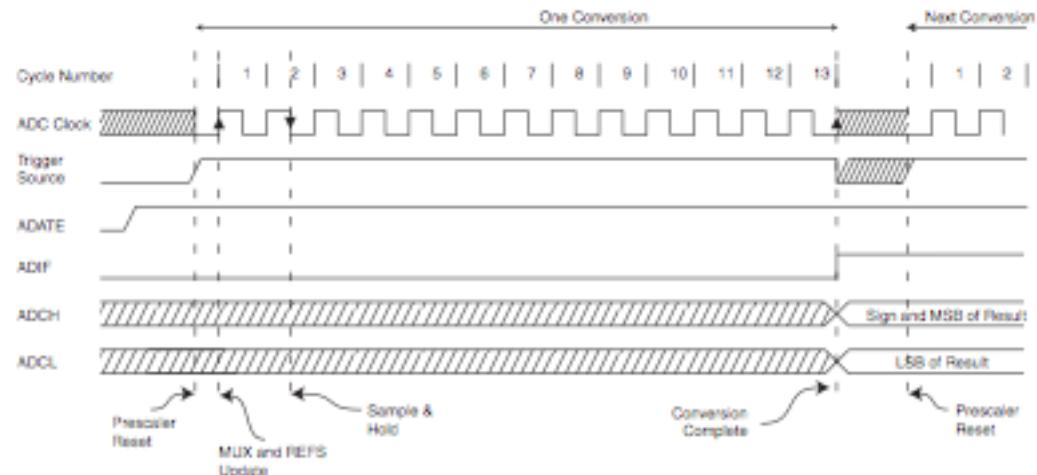
First Conversion

ADC: Conversion Timing

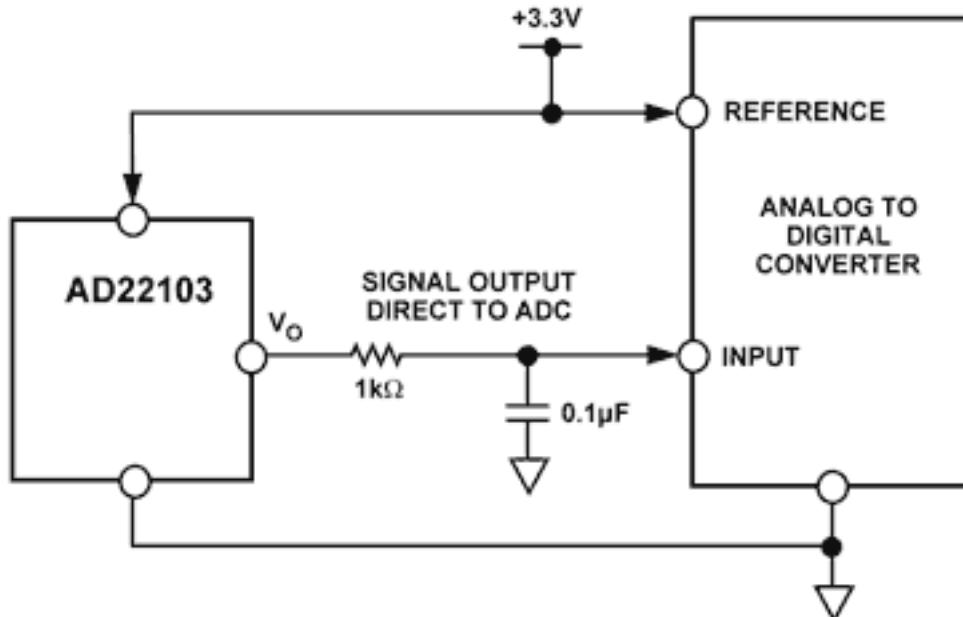


Single Conversion

Auto-trigger Conversion

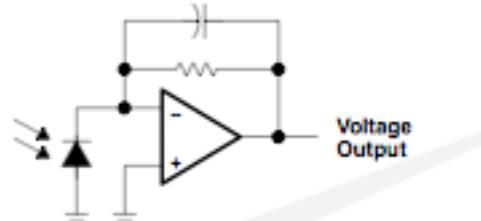


Using External Sensors - Temperature



- AD22103 temperature sensor by Analog Devices
 - Temperature coefficient of 28 mV/°C
 - Output proportional to $T \cdot V_S$
 - Temperature span: 0 - 100 °C
 - Price - \$1.65
 - Transfer function: $V_{OUT} = (V_S/3.3) \times [0.25 + 0.028 \times T_A]$

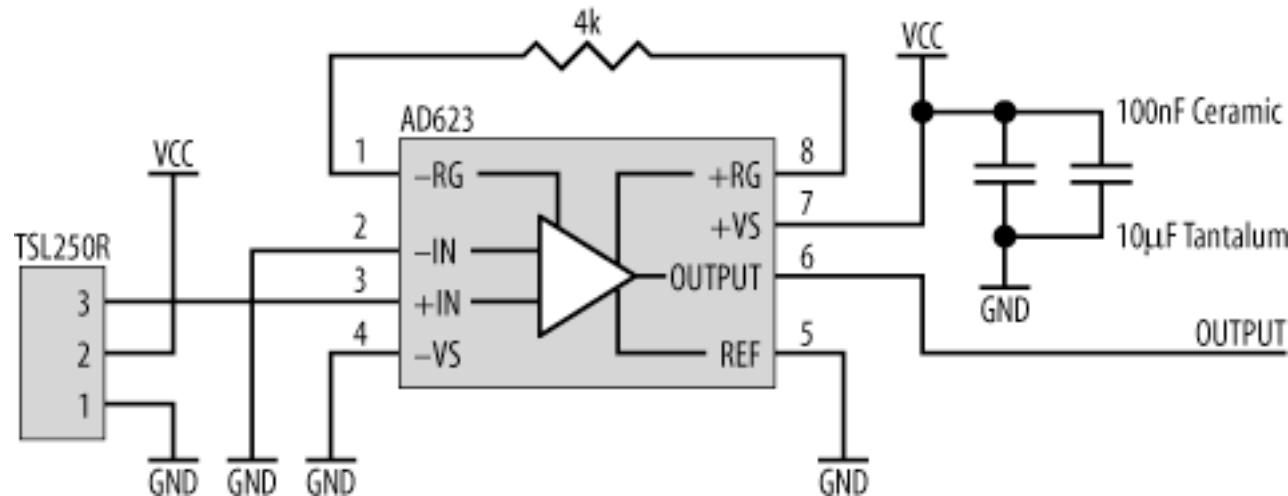
Using External Sensors - Light



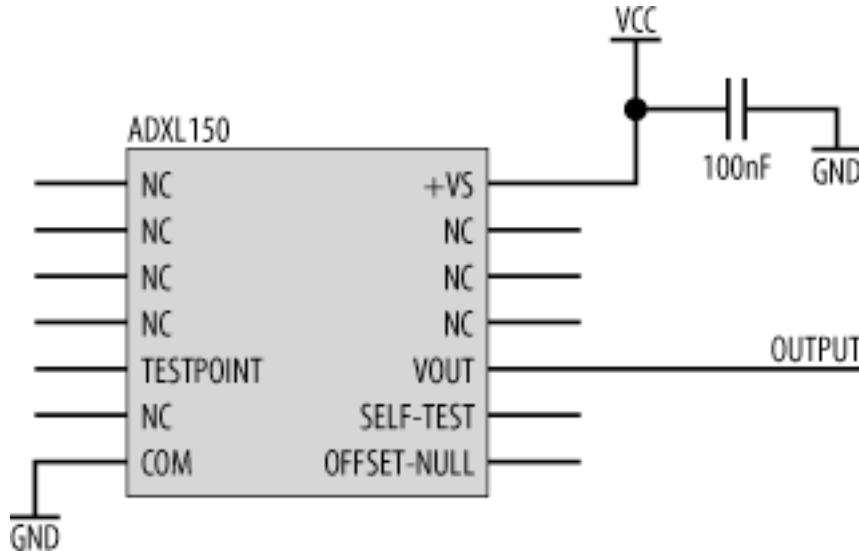
- TSL250R light sensor by TAOS (Texas Advanced Optical Solutions, spinoff of TI)
 - Consists of photodiode and an integrated amplifier
 - Converts light intensity to a voltage
 - Typical responsivity: $137 \text{ mV}/(\mu\text{W}/\text{cm}^2)$ at wavelength of 635 nm
 - Typical current consumption: 1 mA
 - Maximum output voltage for a supply of 5V ~ 4V
 - Loose resolution if we connect directly to 5V ADC
 - What is the solution?

Amplifying the light sensor

- AD623: General purpose Op Amp by Analog Devices
- Requires only a single external resistor to set the gain using:
$$R_G = 100 / (\text{Gain} - 1) \text{ kOhms}$$
- In this case Gain = 1.25 $\rightarrow R_G = 4 \text{ kOhms}$



Using External Sensors - Accelerometer



- ADXL150 single-axis accelerometer by Analog Devices
 - Use for measuring gentle vibrations to violent physical shocks such as car-crash
 - On-chip signal conditioning and amplification
 - Output proportional to both the acceleration and supply voltage:
$$V_{OUT} = V_S/2 - (\text{sensitivity} * V_S/5 * \text{acceleration})$$
 - Typical value of sensitivity = 38.0

QUESTIONS?

