

AVR Microcontrollers - II

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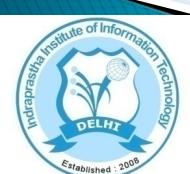
January 19, 2011

Partly adopted from ES Programming, DAIICT Slides by Prabhat Ranjan



Logistics

- Blogs: Start participating. Put in interesting stuff, queries etc.
- Students registered for the course
 - Ensure you are in the mailing list - you will be responsible for not doing anything communicated on the mailing list
 - Anyone who has not formally registered in the course - Prateek Gaur?
- Introductory lab session on Thursday from 1-2:30 pm
 - Read the Vendor Document on the course website before the lab session to speed up the learning
- First assignment due January 23
 - Submit your assignments through google code -
<https://code.google.com/p/cse537-2011/>
 - Create a sub-directory with your email address e.g. aman08005



Revision

- Microcontroller Memory
 - Flash Program Memory
 - Application Boot loader section
 - Data SRAM
 - EEPROM
- ATMEGA328p - 3 ports for GPIOs
 - 3 Registers in I/O space for each port - DDRx, PORTx, PINx
- Reset Sources
 - Power-on Reset
 - Watchdog Reset
 - External Reset
 - Brown-out Reset
 - MCUSR for status information on Reset

32 Registers
64 I/O Registers
160 Ext I/O Reg.
0x0100
Internal SRAM (512/1024/1024/2048 x 8)

0x0000 - 0x001F
0x0020 - 0x005F
0x0060 - 0x00FF
0x02FF/0x04FF/0x4FF/0x08FF





Boot loader

- Code in the bootloader section of the flash to auto-download hex program into the main flash section (0x0000 onwards)
- Boot loader behaves as though you have in-circuit programmer between your PC and ATMEGA328p board
- Upon hardware reset
 - PC jumps to start of boot loader section
 - Boot loader waits for 2 seconds for the PC to establish communication
 - If no “sync” characters received in 2 seconds, it jumps to 0x0000 to start executing the main program
- Consumes 2 KB of the flash memory - Rest 30 KB left for the program memory
- To keep the board always in boot loader mode, jumper Pin 12 to Reset pin



AVR Fuses

- Similar to a config file, fuses are used to configure important system parameters at the time of programming
 - E.g. specifying the clock source and speed
- Fuses are not erased when AVR memory is erased
 - It is not required to reprogram the fuses every time AVR is programmed
 - It can cause problems if incorrect settings are selected
- If you want to change some of the fuse bits
 - Read the current fuse configuration to get the configuration of the remaining bits
 - Combine it with new settings to get the byte information for the fuse bits
 - Configure the byte information in fuse bytes while programming the chip
- Do not change fuses when operating from boot loader
- Fuse values are latched when the device enters the programming mode and changes will have no effect until the part leaves the programming mode



ATMEGA328p Fuses

High Fuse Byte	Bit No	Description	Default Value
RSTDISBL ⁽¹⁾	7	External Reset Disable	1 (unprogrammed)
DWEN	6	debugWIRE Enable	1 (unprogrammed)
SPIEN ⁽²⁾	5	Enable Serial Program and Data Downloading	0 (programmed, SPI programming enabled)
WDTON ⁽³⁾	4	Watchdog Timer Always On	1 (unprogrammed)
EESAVE	3	EEPROM memory is preserved through the Chip Erase	1 (unprogrammed), EEPROM not reserved
BOOTSZ1	2	Select Boot Size (see Table 26-7 on page 291, Table 26-10 on page 292 and Table 26-13 on page 293 for details)	0 (programmed) ⁽⁴⁾
BOOTSZ0	1	Select Boot Size (see Table 26-7 on page 291, Table 26-10 on page 292 and Table 26-13 on page 293 for details)	0 (programmed) ⁽⁴⁾
BOOTRST	0	Select Reset Vector	1 (unprogrammed)

Low Fuse Byte	Bit No	Description	Default Value
CKDIV8 ⁽⁴⁾	7	Divide clock by 8	0 (programmed)
CKOUT ⁽³⁾	6	Clock output	1 (unprogrammed)
SUT1	5	Select start-up time	1 (unprogrammed) ⁽¹⁾
SUT0	4	Select start-up time	0 (programmed) ⁽¹⁾
CKSEL3	3	Select Clock source	0 (programmed) ⁽²⁾
CKSEL2	2	Select Clock source	0 (programmed) ⁽²⁾
CKSEL1	1	Select Clock source	1 (unprogrammed) ⁽²⁾
CKSEL0	0	Select Clock source	0 (programmed) ⁽²⁾



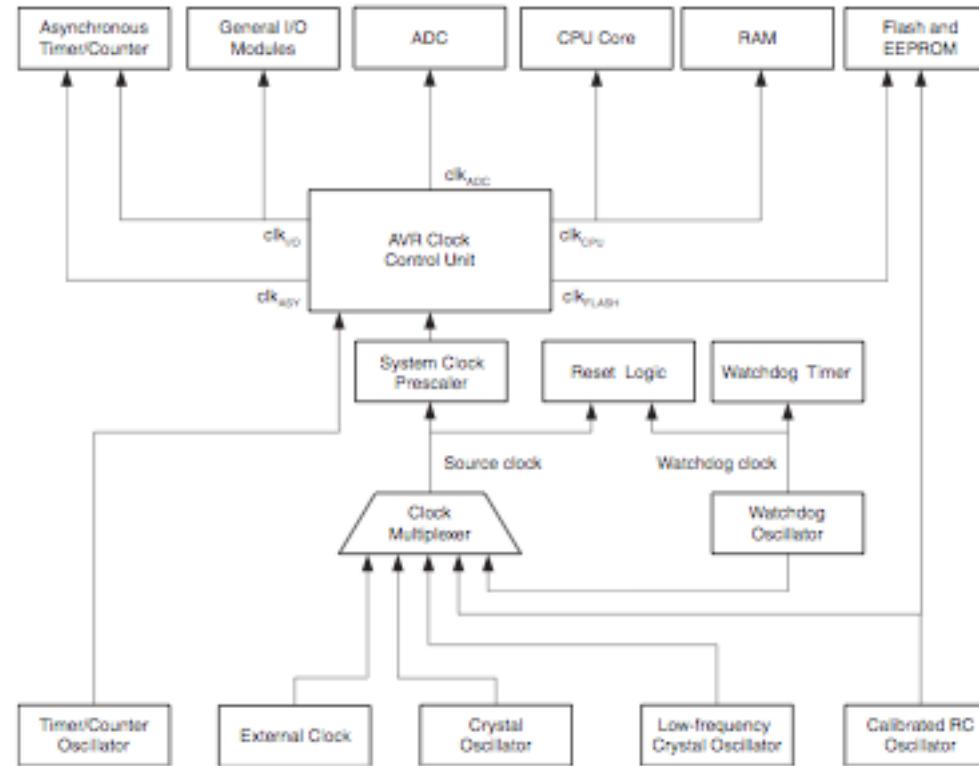
ATMEGA328p Fuses

Extended Fuse Byte	Bit No	Description	Default Value
-	7	-	1
-	6	-	1
-	5	-	1
-	4	-	1
-	3	-	1
BODLEVEL2 ⁽¹⁾	2	Brown-out Detector trigger level	1 (unprogrammed)
BODLEVEL1 ⁽¹⁾	1	Brown-out Detector trigger level	1 (unprogrammed)
BODLEVEL0 ⁽¹⁾	0	Brown-out Detector trigger level	1 (unprogrammed)

- Partially different set of fuse bits for ATMEGA32u4 - See Datasheet (Section on “Memory Programming” for details)



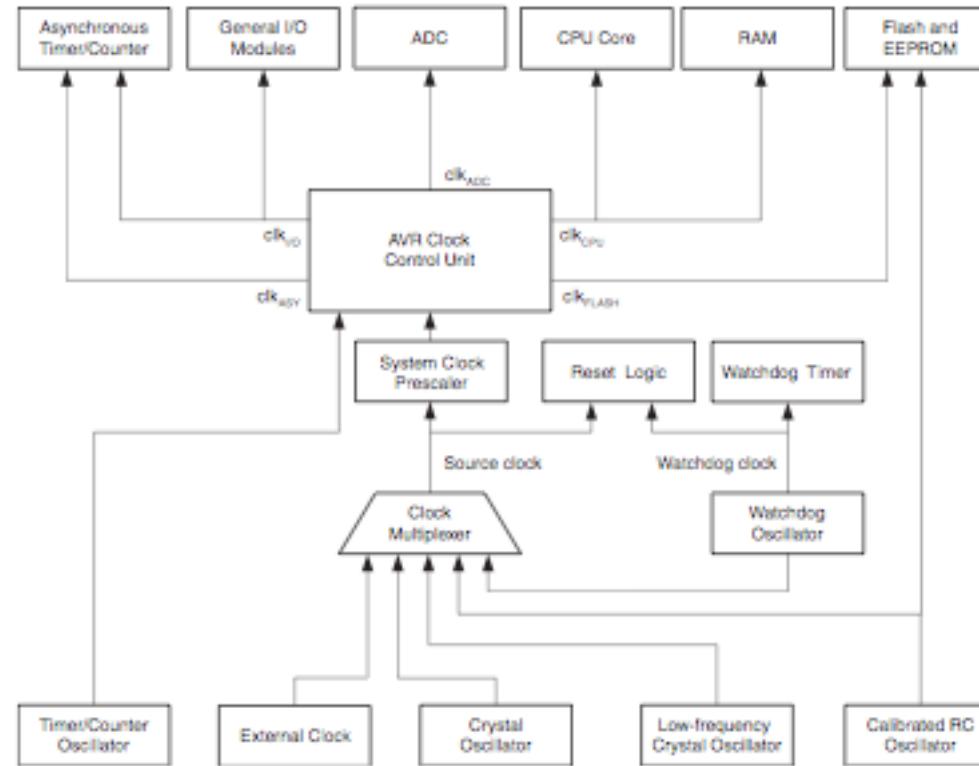
Clock Systems - clk_{CPU}



■ CPU clock - clk_{CPU}

- Routed to parts of system concerned with AVR core
- E.g. General Purpose Register File, Status Register, Data Memory Holding Stack Pointer

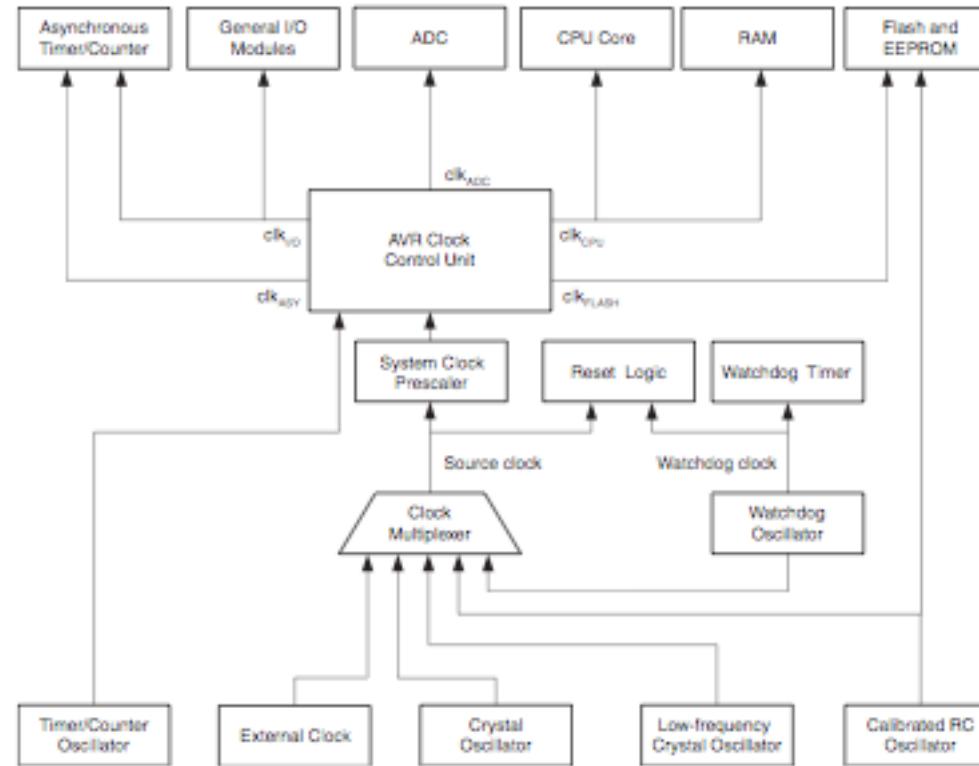
Clock Systems - $\text{clk}_{\text{FLASH}}$



■ Flash clock - $\text{clk}_{\text{FLASH}}$

- Controls the operation of flash interface
- Usually active simultaneously with clk_{CPU}

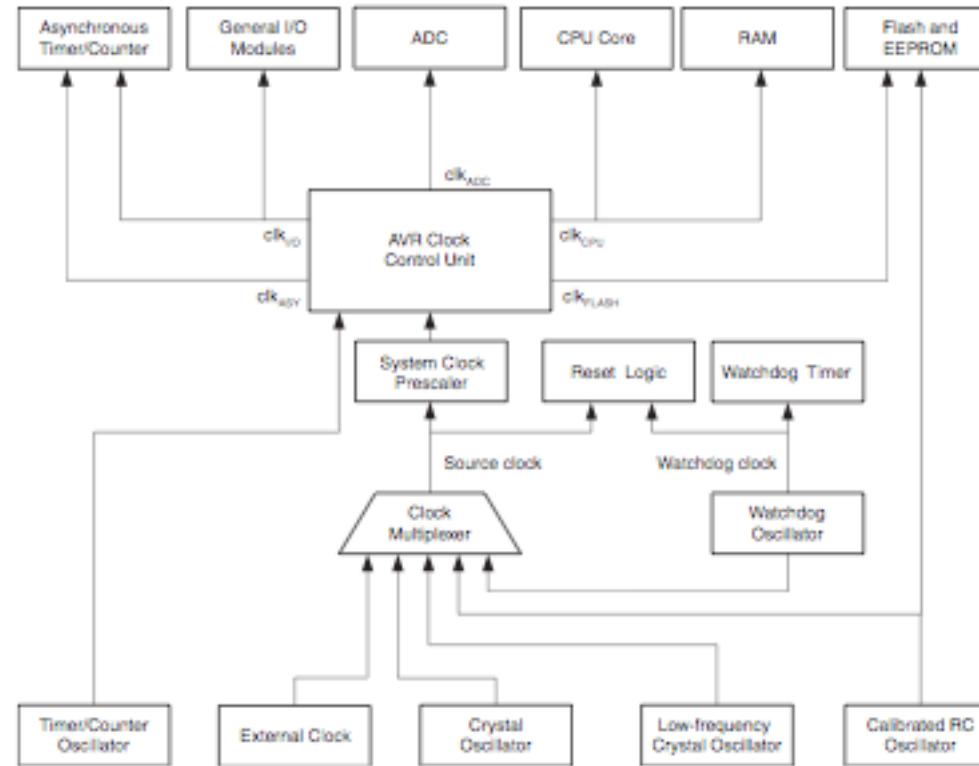
Clock Systems - clk_{ASY}



■ Asynchronous Timer clock - clk_{ASY}

- Allows asynchronous Timer/Counter to be directly controlled
- Usually active simultaneously with clk_{CPU}

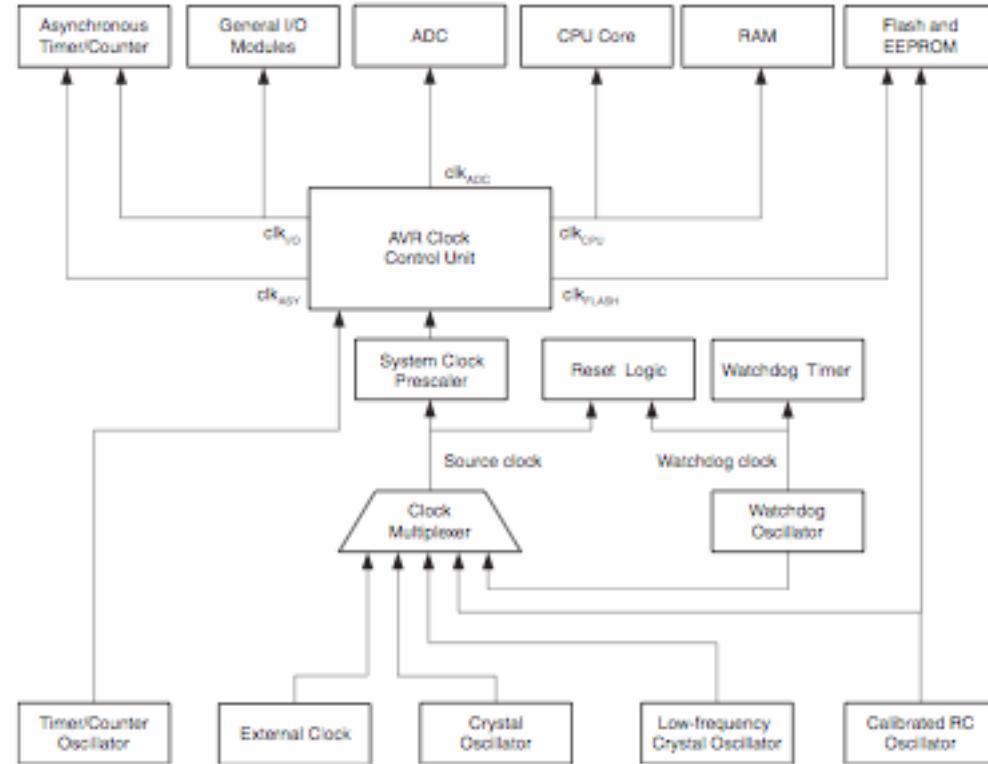
Clock Systems - clk_{ADC}



■ ADC clock - clk_{ADC}

- Dedicated clock for ADC such that CPU and I/O clocks can be halted to reduce the noise from the digital circuitry - Helps in more accurate ADC conversion

Clock Systems - $\text{clk}_{\text{I/O}}$



I/O clock - $\text{clk}_{\text{I/O}}$

- Used by majority of I/O modules e.g. Timer/Counters, SPI, USART
- Also used by external interrupt module

Clock Sources - ATMEGA328p

Device Clocking Option	CKSEL3...0
Low Power Crystal Oscillator	1111 - 1000
Full Swing Crystal Oscillator	0111 - 0110
Low Frequency Crystal Oscillator	0101 - 0100
Internal 128 kHz RC Oscillator	0011
Calibrated Internal RC Oscillator	0010
External Clock	0000
Reserved	0001

■ Multiple clock sources

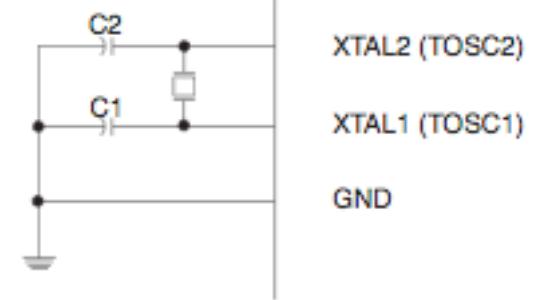
- Selectable by Flash Fuse Bits

- Default clock source - Internal RC Oscillator at 8 MHz (CLKSEL = "0010" and CLKDIV8 programmed (0), resulting in 1 MHz system clock



ATMEGA328p - On-chip Oscillator

- Quartz crystal or ceramic resonator used to generate clock using on-chip oscillator
- Low power crystal oscillator can operate in three different modes, each optimized for a specific frequency range
 - Not capable of driving other clock inputs
 - Susceptible to noisy environments



- Full swing crystal oscillator
 - Useful for driving other clock inputs and in noisy environments
 - Higher power consumption

Frequency Range (MHz)	Recommended Range for Capacitors C1 and C2 (pF)	CKSEL3...1 ⁽¹⁾
0.4 - 0.9	-	100 ⁽²⁾
0.9 - 3.0	12 - 22	101
3.0 - 8.0	12 - 22	110
8.0 - 16.0	12 - 22	111

Frequency Range ⁽¹⁾ (MHz)	Recommended Range for Capacitors C1 and C2 (pF)	CKSEL3...1
0.4 - 20	12 - 22	011

- Low frequency crystal oscillator
 - Optimized for use with 32.768 KHz watch crystal

ATMEGA328p - Internal RC Oscillator



- By default, calibrated internal RC Oscillator provides 8 MHz clock
- If selected, it will operate with no external components

Frequency Range ⁽²⁾ (MHz)	CKSEL3...0
7.3 - 8.1	0010 ⁽¹⁾

- Another low power internal oscillator operating at 128 KHz
- Very low power clock source not designed for high accuracy

Nominal Frequency ⁽¹⁾	CKSEL3...0
128 kHz	0011

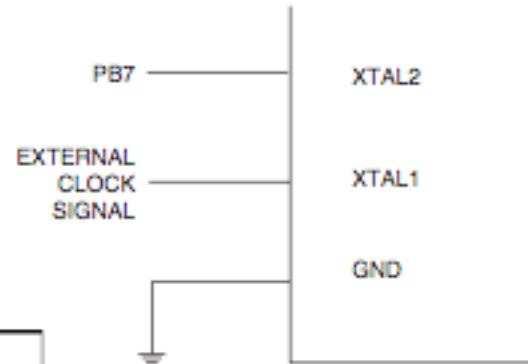


ATMEGA328p - External Clock



- Drive XTAL1 pin with external clock source
- Select appropriate clock fuse bits configuration

Frequency	CKSEL3...0
0 - 20 MHz	0000



- The device can also output the system clock on CLKO pin
 - To enable, CLKOUT fuse bit has to be programmed
- If the system clock prescaler is used, it is the divided clock that is outputted

ATMEGA328p - Related I/O Registers



OSCCAL (Oscillator Calibration Register)

- Used to trim the calibrated internal RC Oscillator

Bit (0x66)	7	6	5	4	3	2	1	0	OSCCAL
Initial Value	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	
ReadWrite	R/W								
Device Specific Calibration Value									

	Frequency	V _{cc}	Temperature	Calibration Accuracy
Factory Calibration	8.0 MHz	3V	25°C	±10%
User Calibration	7.3 - 8.1 MHz	1.8V - 5.5V	-40°C - 85°C	±1%

CLKPR (Clock Prescale Register)

- Define the division factor between the clock source and internal system clock

Bit (0x61)	7	6	5	4	3	2	1	0	CLKPR
Initial Value	CLKPCE	-	-	-	CLKPS3	CLKPS2	CLKPS1	CLKPS0	
ReadWrite	R/W	R	R	R	R/W	R/W	R/W	R/W	
See Bit Description									



Power Management and Sleep Modes

- Sleep modes enable application to shut down unused modules in MCU, thereby saving power
- Six sleep modes - Idle, ADC Noise Reduction, Power down, Power save, Standby, Extended Standby
- Sleep Mode Control Register (SMCR) contains control bits for power management

Bit	7	6	5	4	3	2	1	0	SMCR
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- To enter any of the mode, SE bit in SMCR must be written to logic 1 and SLEEP instruction must be executed

SM2	SM1	SM0	Sleep Mode
0	0	0	Idle
0	0	1	ADC Noise Reduction
0	1	0	Power-down
0	1	1	Power-save
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Standby ⁽¹⁾
1	1	1	Extended Standby ⁽¹⁾



Sleep Modes - IDLE

Sleep Mode	Active Clock Domains					Oscillators		Wake-up Sources								Software BOD Disable
	clk _{CPU}	clk _{FLASH}	clk _{IO}	clk _{ADC}	clk _{KEY}	Main Clock Source Enabled	Timer Oscillator Enabled	INT1, INT0 and Pin Change	TWI Address Match	Timer2	SPM/EEPROM Ready	ADC	WDT	Other IO		
Idle			X	X	X	X	X ⁽²⁾	X	X	X	X	X	X	X		
ADC Noise Reduction				X	X	X	X ⁽²⁾	X ⁽³⁾	X	X ⁽²⁾	X	X	X			
Power-down								X ⁽³⁾	X					X	X	
Power-save					X		X ⁽²⁾	X ⁽³⁾	X	X				X	X	
Standby ⁽¹⁾						X		X ⁽³⁾	X					X	X	
Extended Standby					X ⁽²⁾	X	X ⁽²⁾	X ⁽³⁾	X	X			X		X	

- Notes:
- Only recommended with external crystal or resonator selected as clock source.
 - If Timer/Counter2 is running in asynchronous mode.
 - For INT1 and INT0, only level interrupt.

- IDLE Mode (SM2..0 = 000) - Stops the CPU but allows IO interfaces and ADCs to run
- Enables MCU to wake up from external triggered interrupt as well as some internal ones



Sleep Modes - ADC NRM

Sleep Mode	Active Clock Domains					Oscillators		Wake-up Sources								Software BOD Disable
	clk _{CPU}	clk _{FLASH}	clk _{IO}	clk _{ADC}	clk _{KEY}	Main Clock Source Enabled	Timer Oscillator Enabled	INT1, INT0 and Pin Change	TWI Address Match	Timer2	SPM/EEPROM Ready	ADC	WDT	Other IO		
Idle			X	X	X	X	X ⁽²⁾	X	X	X	X	X	X	X		
ADC Noise Reduction				X	X	X	X ⁽²⁾	X ⁽³⁾	X	X ⁽²⁾	X	X	X			
Power-down								X ⁽³⁾	X				X	X		
Power-save					X		X ⁽²⁾	X ⁽³⁾	X	X			X	X		
Standby ⁽¹⁾						X		X ⁽³⁾	X				X	X		
Extended Standby					X ⁽²⁾	X	X ⁽²⁾	X ⁽³⁾	X	X			X	X		

- Notes:
- Only recommended with external crystal or resonator selected as clock source.
 - If Timer/Counter2 is running in asynchronous mode.
 - For INT1 and INT0, only level interrupt.

- ADC Noise Reduction Mode (SM2..0 = 001) - Stops the CPU and most IOs as well but allows ADCs to run
- Improves the noise environment for the ADC, enabling higher resolution measurements



Sleep Modes - Power-down Mode

Sleep Mode	Active Clock Domains					Oscillators		Wake-up Sources								Software BOD Disable
	clk _{CPU}	clk _{RASH}	clk _{I/O}	clk _{ADC}	clk _{KEY}	Main Clock Source Enabled	Timer Oscillator Enabled	INT1, INT0 and Pin Change	TWI Address Match	Timer2	SPM/EEPROM Ready	ADC	WDT	Other IO		
Idle			X	X	X	X	X ⁽²⁾	X	X	X	X	X	X	X		
ADC Noise Reduction				X	X	X	X ⁽²⁾	X ⁽³⁾	X	X ⁽²⁾	X	X	X			
Power-down								X ⁽³⁾	X					X	X	
Power-save					X		X ⁽²⁾	X ⁽³⁾	X	X				X	X	
Standby ⁽¹⁾						X		X ⁽³⁾	X					X	X	
Extended Standby					X ⁽²⁾	X	X ⁽²⁾	X ⁽³⁾	X	X			X		X	

Notes:

- Only recommended with external crystal or resonator selected as clock source.
- If Timer/Counter2 is running in asynchronous mode.
- For INT1 and INT0, only level interrupt.

- Power-down Mode (SM2..0 = 010) - External Oscillator is stopped
- Halts all generated clocks, allowing operations of asynchronous modules only
- If level triggered interrupt is used for wake up, the changed level must be held for some time



Sleep Modes - Power-save Mode

Sleep Mode	Active Clock Domains					Oscillators		Wake-up Sources							
	clk _{CPU}	clk _{FLASH}	clk _{I/O}	clk _{ADC}	clk _{ASY}	Main Clock Source Enabled	Timer Oscillator Enabled	INT1, INT0 and Pin Change	TWI Address Match	Timer2	SPM/EEPROM Ready	ADC	WDT	Other IO	Software BOD Disable
Idle			X	X	X	X	X ⁽²⁾	X	X	X	X	X	X	X	
ADC Noise Reduction				X	X	X	X ⁽²⁾	X ⁽³⁾	X	X ⁽²⁾	X	X	X		
Power-down								X ⁽³⁾	X					X	X
Power-save					X		X ⁽²⁾	X ⁽³⁾	X	X				X	X
Standby ⁽¹⁾						X		X ⁽³⁾	X					X	X
Extended Standby					X ⁽²⁾	X	X ⁽²⁾	X ⁽³⁾	X	X			X		X

- Notes:
- Only recommended with external crystal or resonator selected as clock source.
 - If Timer/Counter2 is running in asynchronous mode.
 - For INT1 and INT0, only level interrupt.

- Power-save Mode (SM2..0 = 011) - Similar to Power-down mode
 - If Timer/Counter2 is enabled, it will keep running during sleep
- Timer2 Asynchronous operation is not present in ATMEGA32u4 making this mode same as Power-down mode
 - Still present due to compatibility reasons



Sleep Modes - Standby Mode

Sleep Mode	Active Clock Domains					Oscillators		Wake-up Sources								Software BOD Disable
	clk _{CPU}	clk _{FLASH}	clk _{I/O}	clk _{ADC}	clk _{KEY}	Main Clock Source Enabled	Timer Oscillator Enabled	INT1, INT0 and Pin Change	TWI Address Match	Timer2	SPM/EEPROM Ready	ADC	WDT	Other I/O		
Idle			X	X	X	X	X ⁽²⁾	X	X	X	X	X	X	X		
ADC Noise Reduction				X	X	X	X ⁽²⁾	X ⁽³⁾	X	X ⁽²⁾	X	X	X			
Power-down								X ⁽³⁾	X					X	X	
Power-save					X		X ⁽²⁾	X ⁽³⁾	X	X				X	X	
Standby ⁽¹⁾						X		X ⁽³⁾	X					X	X	
Extended Standby					X ⁽²⁾	X	X ⁽²⁾	X ⁽³⁾	X	X			X		X	

- Notes:
- Only recommended with external crystal or resonator selected as clock source.
 - If Timer/Counter2 is running in asynchronous mode.
 - For INT1 and INT0, only level interrupt.

- Standby Mode (SM2..0 = 110) - Similar to Power-down mode
 - Exception - Oscillator is kept running
- From Standby Mode, the device wakes up in 6 clock cycles



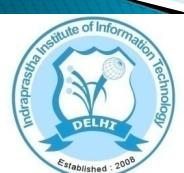
Sleep Modes - Extended Standby Mode

Sleep Mode	Active Clock Domains					Oscillators		Wake-up Sources							
	clk _{CPU}	clk _{FLASH}	clk _{IO}	clk _{ADC}	clk _{KEY}	Main Clock Source Enabled	Timer Oscillator Enabled	INT1, INT0 and Pin Change	TWI Address Match	Timer2	SPM/EEPROM Ready	ADC	WDT	Other IO	Software BOD Disable
Idle			X	X	X	X	X ⁽²⁾	X	X	X	X	X	X	X	
ADC Noise Reduction				X	X	X	X ⁽²⁾	X ⁽³⁾	X	X ⁽²⁾	X	X	X		
Power-down								X ⁽³⁾	X				X		X
Power-save					X		X ⁽²⁾	X ⁽³⁾	X	X			X		X
Standby ⁽¹⁾						X		X ⁽³⁾	X				X		X
Extended Standby					X ⁽²⁾	X	X ⁽²⁾	X ⁽³⁾	X	X			X		X

Notes:

- Only recommended with external crystal or resonator selected as clock source.
- If Timer/Counter2 is running in asynchronous mode.
- For INT1 and INT0, only level interrupt.

- Extended Standby Mode (SM2..0 = 111) - Similar to Power-save mode
 - Exception - Oscillator is kept running
- From Extended Standby Mode, the device wakes up in 6 clock cycles



Power Reduction Register

- Power Reduction Register (PRR) provides a method to stop the clock to individual peripherals to reduce power consumption
 - Current state of peripheral is frozen and I/O registers can not be read or written
 - Resources in use when clock is stopped will remain occupied
 - Peripheral should be disabled before stopping the clock
 - Waking up a module (by clearing the bit in PRR) puts the module in same state as before shutdown
- Can be used in idle/active mode to significantly reduce the overall power consumption

Bit	7	6	5	4	3	2	1	0	PRR	ATMEGA328P
(0x64)	PRTWI	PRTIM2	PRTIM0	-	PRTIM1	PRSPI	PRUSART0	PRADC		
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W		
Initial Value	0	0	0	0	0	0	0	0		

ATMEGA32u4

Bit	7	6	5	4	3	2	1	0	PRR0	PRR1
	PRTWI	PRTIM2	PRTIM0	-	PRTIM1	PRSPI	-	PRADC		
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R	R/W		
Initial Value	0	0	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0	PRR1	
	PRUSB	-	-	PRTIM4	PRTIM3	-	-	PRUSART1		
Read/Write	R/W	R	R	R	R/W	R	R	R/W		
Initial Value	0	0	0	0	0	0	0	0		



Minimizing Power Consumption

- Some of the functions if enabled, remain so in all/most sleep modes. These should be explicitly disabled before entering any sleep mode
 - Analog to Digital Converter
 - Analog Comparator - When entering Idle/ADCNR mode, Analog Comparator should be disabled, if not used
 - Brown-out Detector
 - Internal Voltage Reference
 - Watchdog Timer
 - On-chip debug system
- Port pins: When entering a sleep mode, all port pins should be configured to consume minimum power
 - In sleep modes where $\text{clk}_{\text{I/O}}$ and clk_{ADC} are stopped, input buffers will be disabled ensuring no power consumed by input logic
 - Input buffer enabled when input logic is needed for detecting wake-up conditions



ATMEGA328p - Interrupts

- All interrupts are assigned individual enable bits, together with a global interrupt enable bit which should be written logic one together to enable the interrupt
- Address in the program memory space for interrupt vectors determines the priority level of the interrupt
 - Lower the address, higher is the priority
- Primarily two types of interrupts:
 - Triggered by an event that sets the interrupt flag
 - Trigger as long as interrupt condition is present
- Interrupt execution response is four clock cycles
 - After four clock cycles program vector address for the actual interrupt handling routine is executed
 - The vector is normally a jump to interrupt routine which takes three clock cycles
 - A return from interrupt handling routine takes four clock cycles



ATMEGA328p - Interrupt Vectors

VectorNo.	Program Address ⁽¹⁾	Source	Interrupt Definition
1	0x0000 ⁽¹⁾	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog System Reset
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	INT1	External Interrupt Request 1
4	0x0006	PCINT0	Pin Change Interrupt Request 0
5	0x0008	PCINT1	Pin Change Interrupt Request 1
6	0x000A	PCINT2	Pin Change Interrupt Request 2
7	0x000C	WDT	Watchdog Time-out Interrupt
8	0x000E	TIMER2 COMPA	Timer/Counter2 Compare Match A
9	0x0010	TIMER2 COMPB	Timer/Counter2 Compare Match B
10	0x0012	TIMER2 OVF	Timer/Counter2 Overflow
11	0x0014	TIMER1 CAPT	Timer/Counter1 Capture Event
12	0x0016	TIMER1 COMPA	Timer/Counter1 Compare Match A
13	0x0018	TIMER1 COMPB	Timer/Counter1 Compare Match B
14	0x001A	TIMER1 OVF	Timer/Counter1 Overflow
15	0x001C	TIMER0 COMPA	Timer/Counter0 Compare Match A
16	0x001E	TIMER0 COMPB	Timer/Counter0 Compare Match B
17	0x0020	TIMER0 OVF	Timer/Counter0 Overflow
18	0x0022	SPI, STC	SPI Serial Transfer Complete
19	0x0024	USART, RX	USART Rx Complete
20	0x0026	USART, UDRE	USART, Data Register Empty
21	0x0028	USART, TX	USART, Tx Complete
22	0x002A	ADC	ADC Conversion Complete
23	0x002C	EE READY	EEPROM Ready
24	0x002E	ANALOG COMP	Analog Comparator
25	0x0030	TWI	2-wire Serial Interface
26	0x0032	SPM READY	Store Program Memory Ready



ATMEGA328p - Interrupt Vectors

BOOTRST	IVSEL	Reset Address	Interrupt Vectors Start Address
1	0	0x000	0x002
1	1	0x000	Boot Reset Address + 0x0002
0	0	Boot Reset Address	0x002
0	1	Boot Reset Address	Boot Reset Address + 0x0002

■ Reset and Interrupt Vector placement

Bit	7	6	5	4	3	2	1	0	MCUCR
0x35 (0x55)	-	BODS ^[1]	BODSE ^[1]	PUD	-	-	IVSEL	IVCE	
Read/Write	R	R/W	R/W	R/W	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

■ MCU Control Register

■ Interrupt Vector Select (IVSEL)

- 0 implies IVs are placed at the start of Flash memory
- 1 implies Ivs are places at the start of Boot Loader Section

■ Interrupt Vector Change Enable (IVCE)

- Must be written to logic 1 to enable change of IVSEL bit



ATMEGA328p - External Interrupts

- Triggered by INT0 and INT1 pins or any of the PCINT23..0 pins
- PCINTs internally combined
 - PCI2 will trigger if any enabled PCINT[23:16] toggles
 - PCI1 will trigger if any enabled PCINT[14:8] toggles
 - PCI0 will trigger if any enabled PCINT[7:0] toggles
- PCMSK2, PCMSK1, PCMSK0 Registers control which pins contribute to the pin change interrupt
- PCINT23..0 are detected asynchronously

Bit (0x68)	7	6	5	4	3	2	1	0	PCICR
Read/Write	-	-	-	-	-	PCIE2	PCIE1	PCIE0	
Initial Value	0	0	0	0	0	R/W	R/W	R/W	

Bit 0x1B (0x3B)	7	6	5	4	3	2	1	0	PCIFR
Read/Write	-	-	-	-	-	-	PCIF2	PCIF1	PCIF0
Initial Value	0	0	0	0	0	R	R	R/W	R/W
	0	0	0	0	0	R	R	R/W	R/W

Bit (0x6D)	7	6	5	4	3	2	1	0	PCMSK2
Read/Write	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	
Initial Value	R/W								
	0	0	0	0	0	0	0	0	

Bit (0x6C)	7	6	5	4	3	2	1	0	PCMSK1
Read/Write	-	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	
Initial Value	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

Bit (0x6B)	7	6	5	4	3	2	1	0	PCMSK0
Read/Write	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	
Initial Value	R/W								
	0	0	0	0	0	0	0	0	



ATMEGA328p - External Interrupts

- INT0 or INT1 interrupts can be triggered by rising or falling edge or a low level
- Recognition of rising or falling edge requires presence of an I/O clock

Bit	7	6	5	4	3	2	1	0	
(0x69)	-	-	-	-	ISC11	ISC10	ISC01	ISC00	EICRA
ReadWrite	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Any logical change on INT1 generates an interrupt request.
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

Bit	7	6	5	4	3	2	1	0	
0x1D (0x3D)	-	-	-	-	-	-	INT1	INT0	EIMSK
ReadWrite	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Bit	7	6	5	4	3	2	1	0	
0x1C (0x3C)	-	-	-	-	-	-	-	-	EIFR
ReadWrite	R	R	R	R	R	R	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	



QUESTIONS?

