

AVR Microcontrollers

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Partly adopted from ES Programming, DAIICT Slides by Prabhat Ranjan



Logistics

- Orders for microcontroller kits
 - Already placed - They will arrive Tomorrow
 - Placed a few extra orders as well
- CSE537 Mailing list - Please add yourself
- Invitation to contribute on the blog sent
 - Anyone who has not yet received it?
- Introductory lab session on Thursday from 12-2 pm (Hardware Lab)
- Submit your assignments through google code -
<https://code.google.com/p/cse537-2011/>
 - Create a sub-directory with your email address e.g. aman08005
- Shifting the Wednesday class to Thursday 2:30 - 4 pm





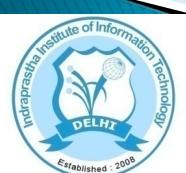
Miscellaneous

■ Revision

- Key issues in embedded systems: Size, energy and performance
 - Critical components: Processing speed, storage capacity, communication bandwidth, timing
- Microcontroller architecture: Core, Memory, Peripherals
 - Come in various flavors - 8/16/32 bit, memory sizes, communication interfaces, peripherals

■ Choice of platforms for assignments and projects:

- Atmel ATMEGA328P (you purchase)
- Atmel ATMEGA32u4 (1/you purchase)
- TelosB (4)
- mBed (Willing to purchase 1-2)
- uLeap (1)





Microcontroller Memory

■ Primarily three types of memory:

- Program Flash Memory: Used for storing the program
- Data Memory of SRAM: Used for temporary storage of data values
- EEPROM Memory: Used for permanent storage of data values or initial parameters for the microcontroller

■ ATMEGA328P

- 32 KB Flash
- 2 KB SRAM
- 1 KB EEPROM

■ ATMEGA32u4

- 32 KB Flash
- 2.5 KB SRAM
- 1 KB EEPROM



AVR Architecture

■ Harvard Architecture

- Separate bus and memory for program and data

■ Program memory - In-system programmable flash

- 32 KB in our case
- Divided into boot program section and application program section

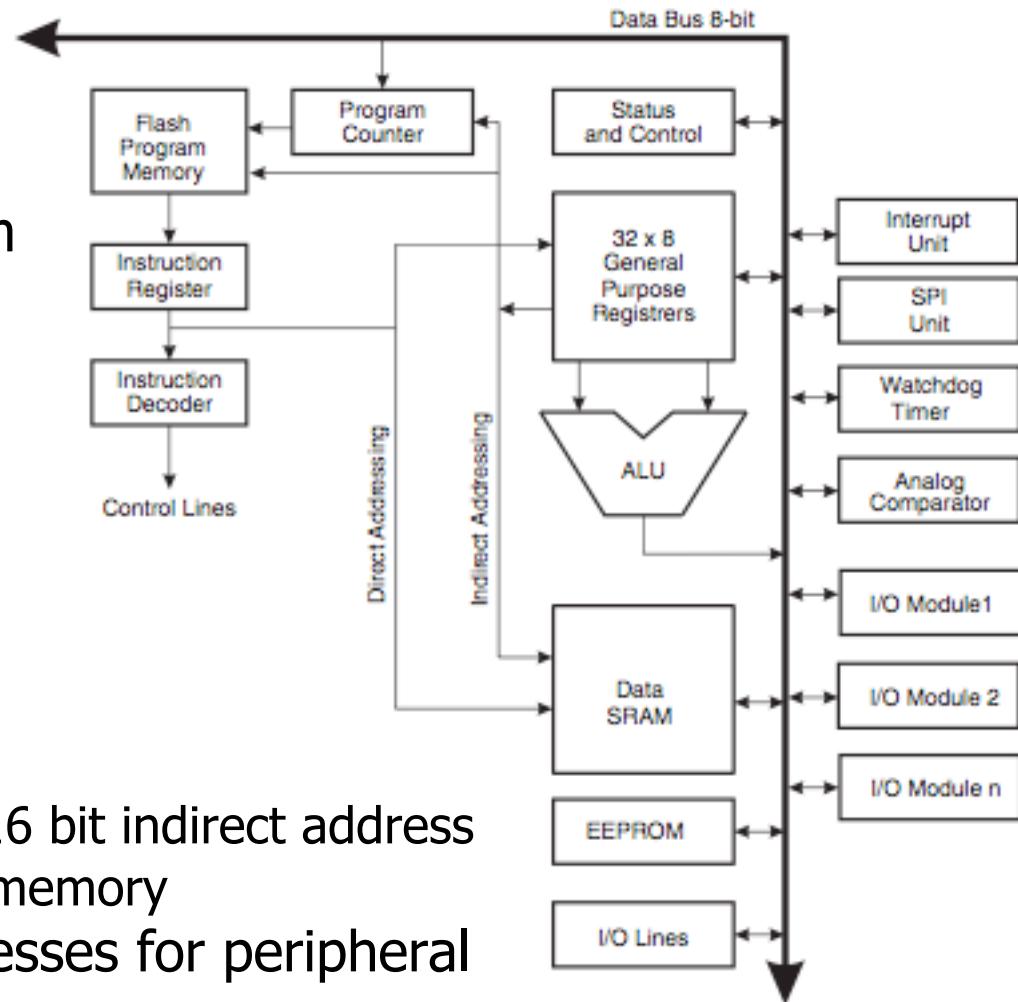
■ Data SRAM

- 2/2.5 KB (328P/32u4)

■ 32x8bit working registers

- 6 of them can be used for 16 bit indirect address pointers (X-, Y-, Z-) for data memory

■ I/O memory space - 64 addresses for peripheral functions



General Purpose Working Registers

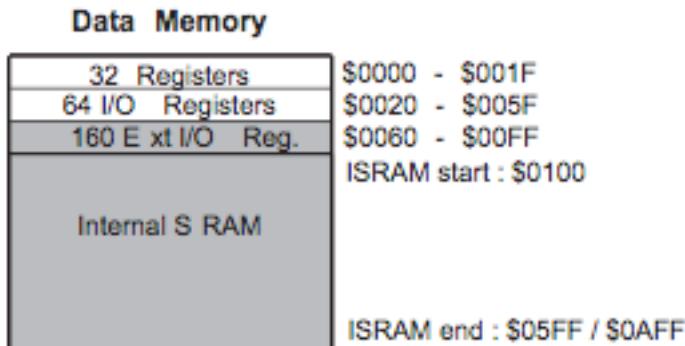
- Each register is also assigned a data memory address mapping them directly to the first 32 locations of user Data space
- R26 to R31 act as 16 bit address pointers for indirect addressing of user space
- 64 I/O memory space can be accessed directly or Data space locations following register files i.e. from 0x20 - 0x5F
- Extended I/O space from 0x60 - 0xFF in SRAM

7	0	Addr.	
R0		0x00	
R1		0x01	
R2		0x02	
...			
R13		0x0D	
R14		0x0E	
R15		0x0F	
R16		0x10	X-register Low Byte
R17		0x11	
...			
R26		0x1A	X-register High Byte
R27		0x1B	
R28		0x1C	Y-register Low Byte
R29		0x1D	Y-register High Byte
R30		0x1E	Z-register Low Byte
R31		0x1F	Z-register High Byte

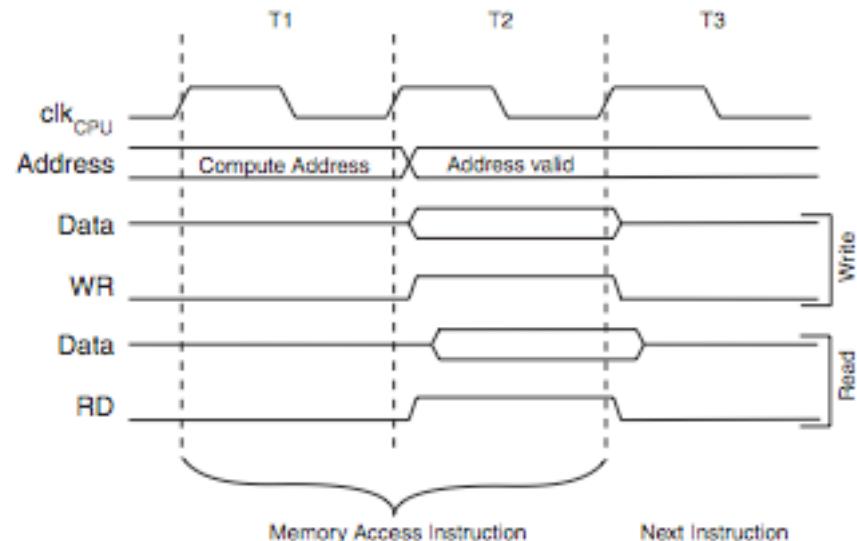
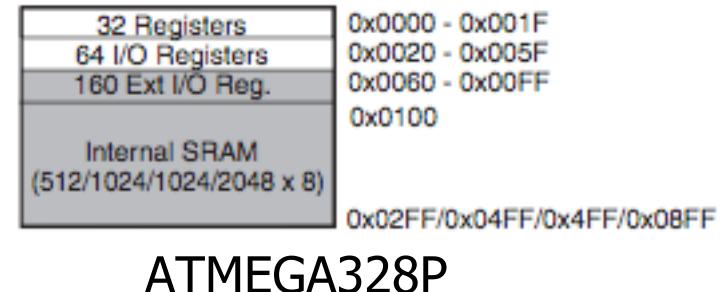


SRAM Data Memory

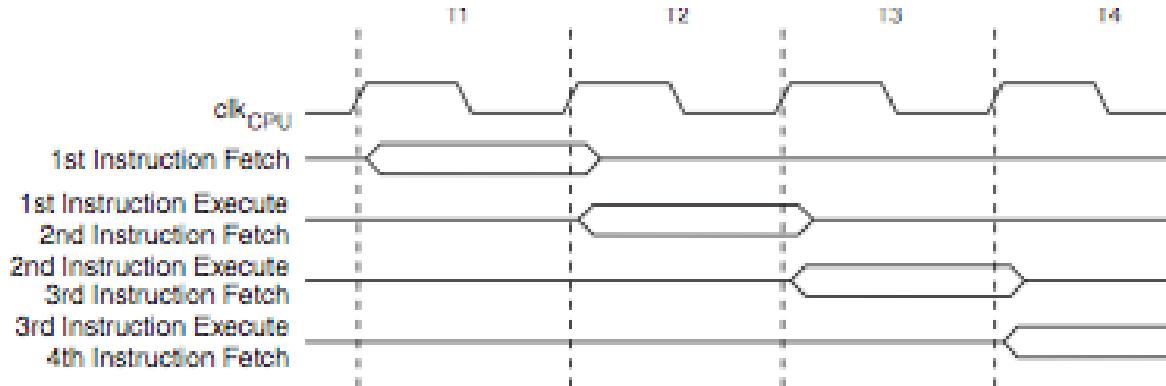
- First 32 locations for register file
- Next 64 for standard I/O Memory
- Next 160 for extended I/O Memory
- Next locations for internal data SRAM
 - 2560 (2.5 KB) for ATMEGAu4
 - 2048 (2 KB) for ATMEGA328P
- Direct addressing reaches the entire data space
- Access time - 2 CPU clock cycles



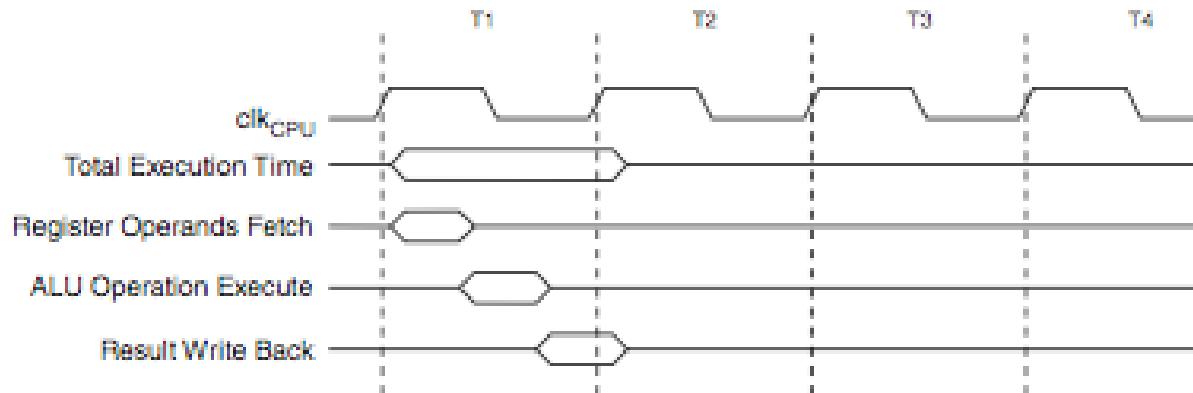
ATMEGA32u4



Instruction Execution Timing



Parallel Instruction Fetches and Instruction Executions

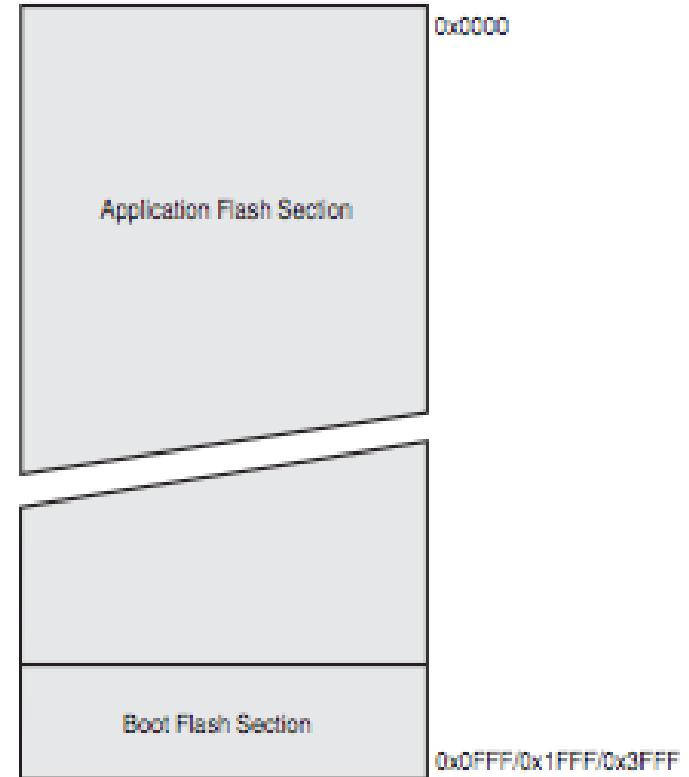


Single Cycle ALU Operation



Flash Program Memory

- In-system reprogrammable
- Organized as 16k x 16
 - All instructions are 16/32 bits wide
- For software security, divided into Boot Flash Section and Application Flash Section
 - Boot Flash Section is for Boot Loader Program for programming the Application Flash Section using on-board UART
- Endurance of at least 10,000 write/erase cycles
- What should be the size of program counter?
- If no boot loader is needed, entire flash is available for application code



EEPROM Data Memory

- 1 KB of data EEPROM memory
- Organizes as a separate data space in which single byte can be written/read
- Endurance of at least 100,000 write/erase cycles
- EEPROM access registers are accessible in I/O space
- EEPROM read - CPU is halted for 4 clock cycles before next instruction is executed
- EEPROM write - CPU is halted for 2 clock cycles

Bit	15	14	13	12	11	10	9	8	EEARH
	-	-	-	-	EEAR11	EEAR10	EEAR9	EEAR8	EEARL
	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	EEARL
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	X	X	X	X	
	X	X	X	X	X	X	X	X	

EEPROM Address Register

Bit	7	6	5	4	3	2	1	0	MSB	LSB	EEDR
Read/Write	R/W										
Initial Value	0	0	0	0	0	0	0	0	0	0	

EEPROM Data Register



Pinout - ATMEGA328P

■ 3 Ports

- PORTB, PORTC,
PORTD

- Each of the port pins
can be used for simple I/O

- Most serve the dual
purpose for a peripheral
function

- 3 I/O memory address locations allocated for each port
 - Data Register - PORTx (R/W)
 - Data Direction Register - DDRx (R/W)
 - Port Input Pins - PINx (Read Only)

(PCINT14/RESET) PC6	1	28	□ PC5 (ADC5/SCL/PCINT13)
(PCINT16/RXD) PD0	2	27	□ PC4 (ADC4/SDA/PCINT12)
(PCINT17/TXD) PD1	3	26	□ PC3 (ADC3/PCINT11)
(PCINT18/INT0) PD2	4	25	□ PC2 (ADC2/PCINT10)
(PCINT19/OC2B/INT1) PD3	5	24	□ PC1 (ADC1/PCINT9)
(PCINT20/XCK/T0) PD4	6	23	□ PC0 (ADC0/PCINT8)
VCC	7	22	□ GND
GND	8	21	□ AREF
(PCINT6/XTAL1/TOSC1) PB6	9	20	□ AVCC
(PCINT7/XTAL2/TOSC2) PB7	10	19	□ PB5 (SCK/PCINT5)
(PCINT21/OC0B/T1) PD5	11	18	□ PB4 (MISO/PCINT4)
(PCINT22/OC0A/AIN0) PD6	12	17	□ PB3 (MOSI/OC2A/PCINT3)
(PCINT23/AIN1) PD7	13	16	□ PB2 (SS/OC1B/PCINT2)
(PCINT0/CLKO/ICP1) PB0	14	15	□ PB1 (OC1A/PCINT1)



Configuring the Pin

- DDxn bit in DDRx Register selects the direction of this pin
 - DDxn as logic 1 implies Pxn is configured as output pin
 - DDxn as logic 0 implies Pxn is configured as input pin
 - E.g. DDRD=0xF0
 - Port D : Pin 0-3 - Input
 - Pin 4-7 - Output
- PORTx Register functions differently depending on whether the pin is set to input/output
 - Simpler case is when the pin is configured as output
 - PORTx Register controls the value at physical IO pin
 - DDRC = 0xFF //Set all Port C pins to output
 - PORTC = 0xF0 //Set first 4 pins of Port C low and next 4 pins high



Configuring the Pin

- When a pin is set to input, PINx register contains the value applied to the pin
 - foo = PIND //Store the value of PORTD pins in foo

- Alternate functions of Port B

Port Pin	Alternate Functions
PB7	XTAL2 (Chip Clock Oscillator pin 2) TOSC2 (Timer Oscillator pin 2) PCINT7 (Pin Change Interrupt 7)
PB6	XTAL1 (Chip Clock Oscillator pin 1 or External clock input) TOSC1 (Timer Oscillator pin 1) PCINT6 (Pin Change Interrupt 6)
PB5	SCK (SPI Bus Master clock Input) PCINT5 (Pin Change Interrupt 5)
PB4	MISO (SPI Bus Master Input/Slave Output) PCINT4 (Pin Change Interrupt 4)
PB3	MOSI (SPI Bus Master Output/Slave Input) OC2A (Timer/Counter2 Output Compare Match A Output) PCINT3 (Pin Change Interrupt 3)
PB2	SS (SPI Bus Master Slave select) OC1B (Timer/Counter1 Output Compare Match B Output) PCINT2 (Pin Change Interrupt 2)
PB1	OC1A (Timer/Counter1 Output Compare Match A Output) PCINT1 (Pin Change Interrupt 1)
PB0	ICP1 (Timer/Counter1 Input Capture Input) CLKO (Divided System Clock Output) PCINT0 (Pin Change Interrupt 0)



Pinout - ATMEGA32u4

■ 5 Ports

- PORTB, PORTC, PORTD, PORTE, PORTF

■ Partial bits exposed for some ports:

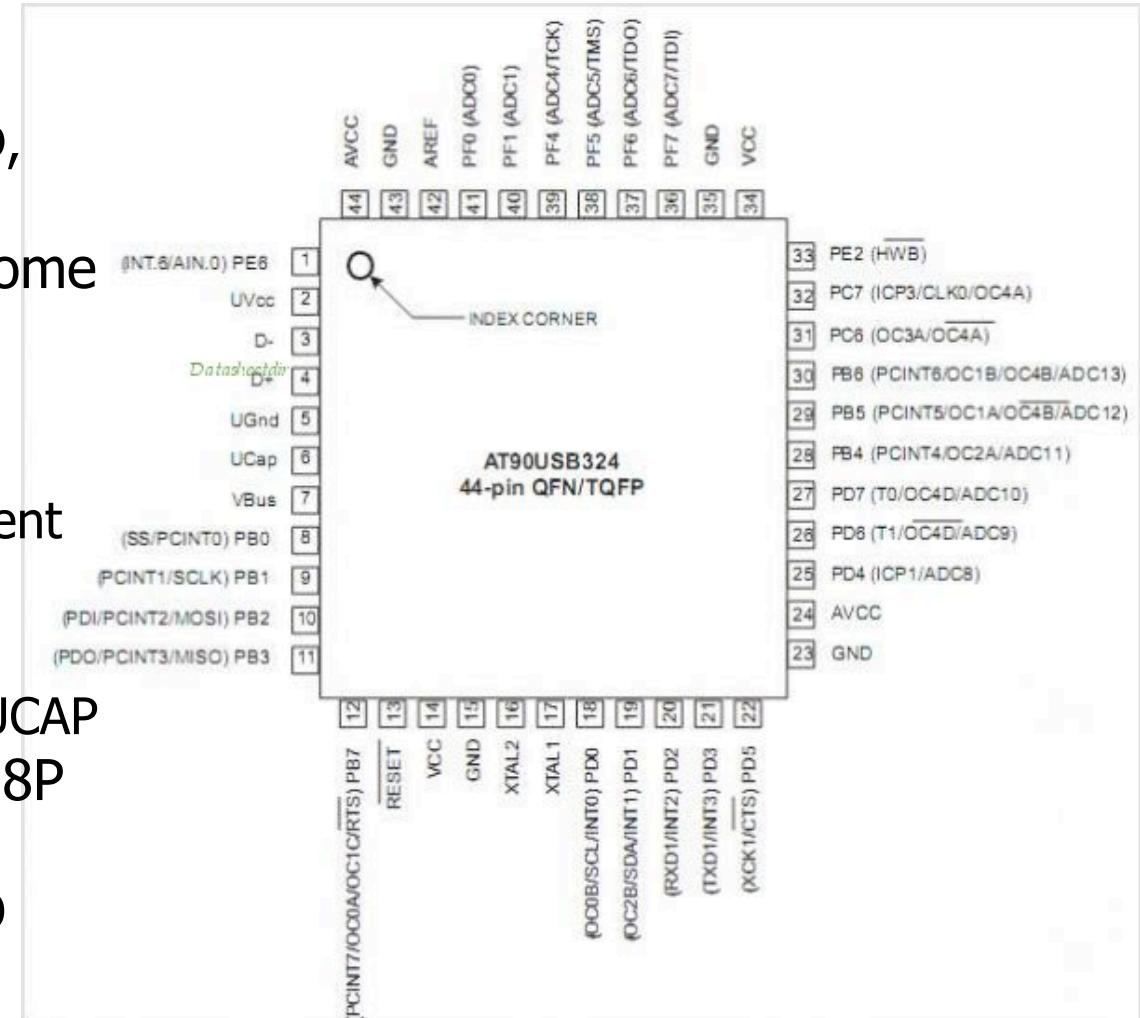
- PORTC: Bit 6 and 7
- PORTE: Bit 2 and 6
- PORTF: Bit 2 and 3 absent

■ Integrated USB OTG Interface

- D+, D-, UGND, UVCC, UCAP

■ Similarities to ATMEGA328P

- GPIO functionality
- Similar Registers for I/O configuration

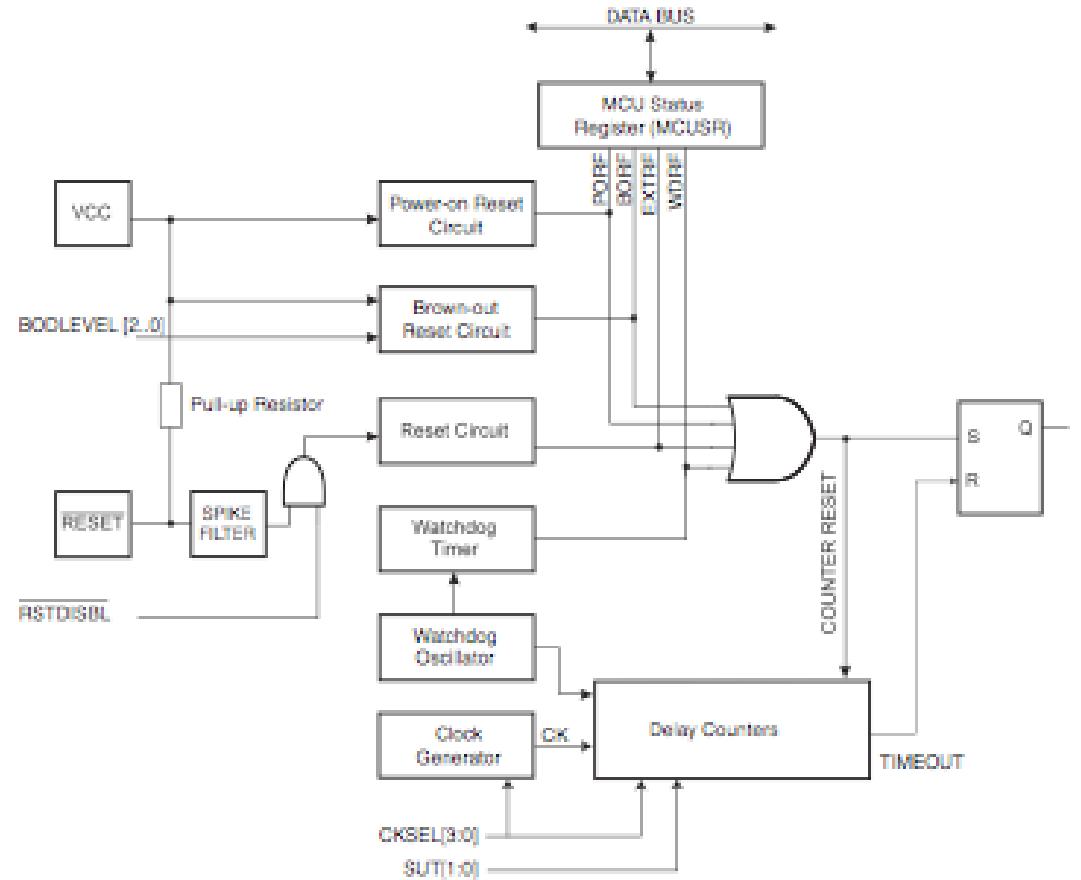


■ System Control and Reset

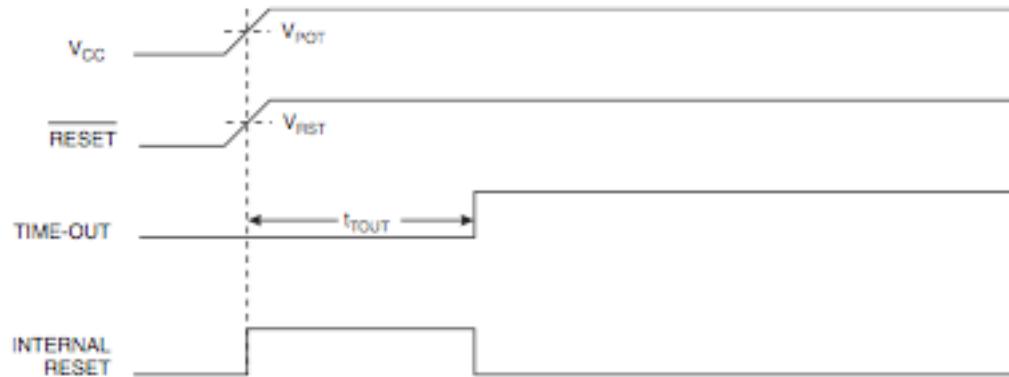
- I/O ports of AVR are immediately set to their initial state when a reset source gets active and the program starts execution from the Reset Vector
- After all Reset sources have gone inactive, a delay counter is invoked, stretching the internal reset
 - Allows power to reach a stable value before normal operation begins
 - Time out period defined by user
- Reset Sources
 - Power on Reset: MCU Reset when supply voltage is below the power on reset threshold (V_{POT})
 - External Reset: Low level present on RESET pin for longer than minimum pulse length
 - Watchdog System Reset: On expiry of watchdog timer, when enabled
 - Brown-out Reset: When supply voltage is less than Brown-out reset threshold (V_{BOT}) and Brown-out Detector enabled



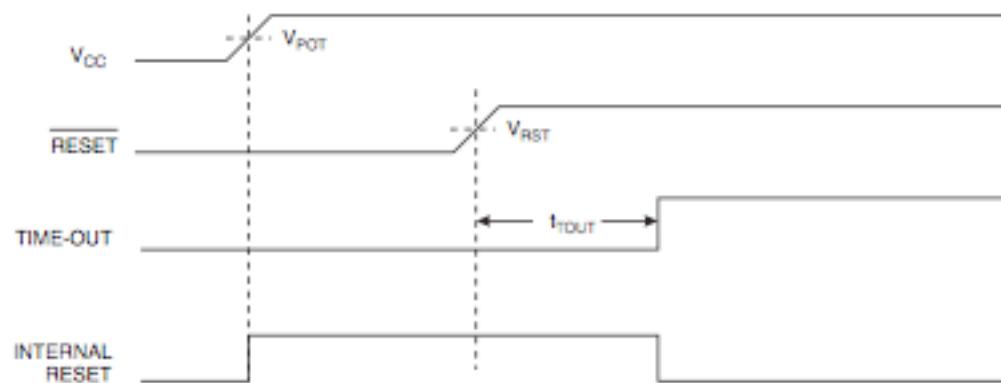
Reset Logic



Power-on Reset

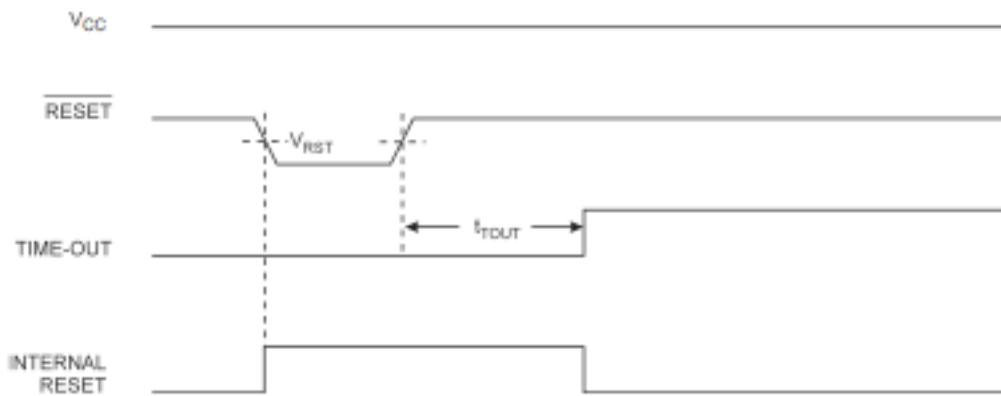


■ MCU Start-up, RESET tied to V_{CC}



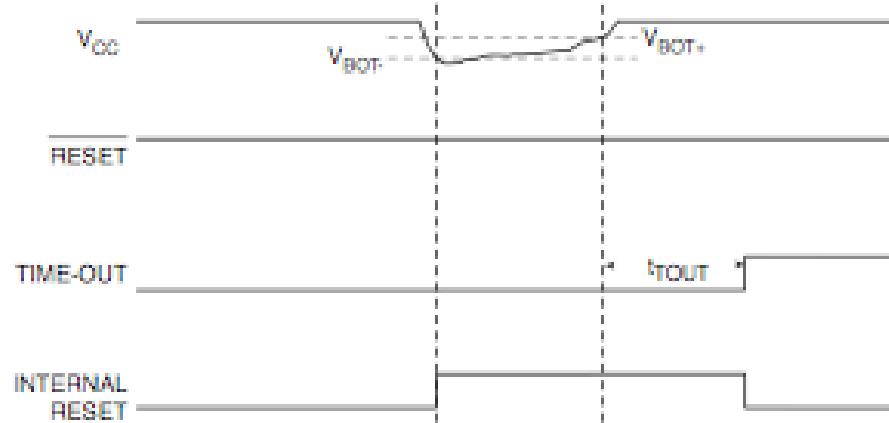
■ MCU Start-up, RESET extended externally

External Reset



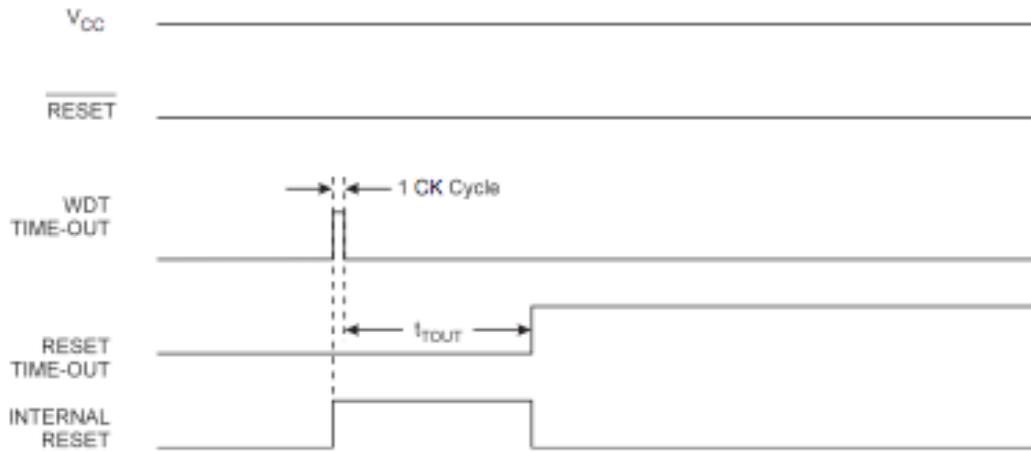
- Generated by low level on RESET pin
- Only pulses longer than minimum pulse width will generate a reset
- After signal reaches V_{RST} on positive edge, delay counter starts MCU after Time-out period t_{OUT}

Brown-out Reset



- Monitors supply voltage by comparing it with fixed trigger level
 - Trigger level has hysteresis to ensure spike free detection
- Brown-out Reset activated when BOD is enabled and $V_{CC} < V_{BOT-}$
- Once $V_{CC} > V_{BOT+}$, delay counter starts MCU after time out period (t_{OUT}) has expired

Watchdog Reset



- When Watchdog times out, it generates a short reset pulse of 1 clock cycle width
- Delay counter starts MCU after time out period (t_{TOUT}) has expired post the falling edge of the reset pulse
- Counts cycles off a separate on-chip 128 KHz oscillator
- In normal operation mode, it is required that the system uses the WDR - Watchdog Timer Reset - instruction to restart the counter before the time-out value is reached

MCU Status Register

Bit	7	6	5	4	3	2	1	0	MCUSR
0x34 (0x54)	-	-	-	-	WDRF	BORF	EXTRF	PORF	
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0					See Bit Description

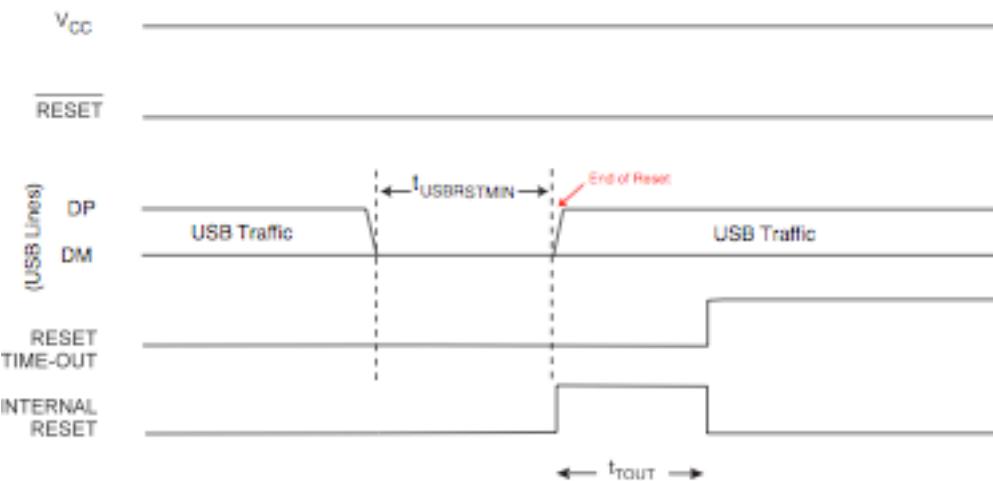
- MCU Status Register provides information about which reset source caused an MCU reset
- If a source caused reset, corresponding bit will be set in MCUSR
 - Bit 7:4 - Reserved (Read as 0)
 - Bit 3 - WDRF (Watchdog System Reset Flag)
 - Bit 2 - BORF (Brown-out Reset Flag)
 - Bit 1 - EXTRF (External Reset Flag)
 - Bit 0 - PORF (Power-on Reset Flag)
- Bit 1-3 are reset by Power-on Reset or by writing a logic 0 to the flag
- User should read and then reset the MCUSR as early as possible in the program to identify the source of reset at a later stage



ATMEGA32u4: Additional Resets

■ ATMEGA32u4 has 2 additional resets

- JTAG AVR Reset - MCU is reset as long as there is logic 1 in Reset register
- USB End of Reset - MCU is reset (excluding the USB controller that remains enabled and attached) on detection of USB End of Reset condition on the bus
 - May be used to enhance system reliability

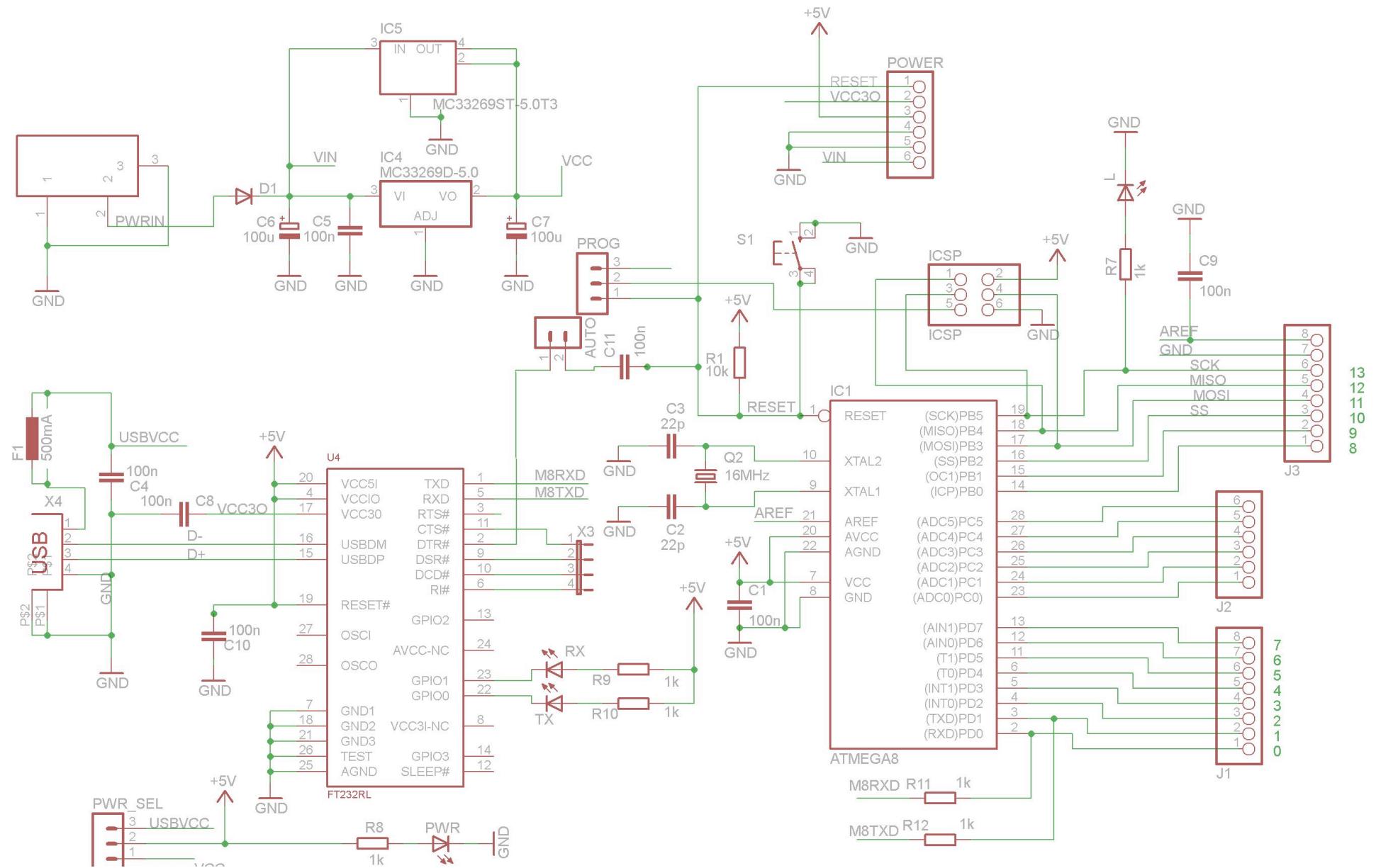


USB Reset During Operation

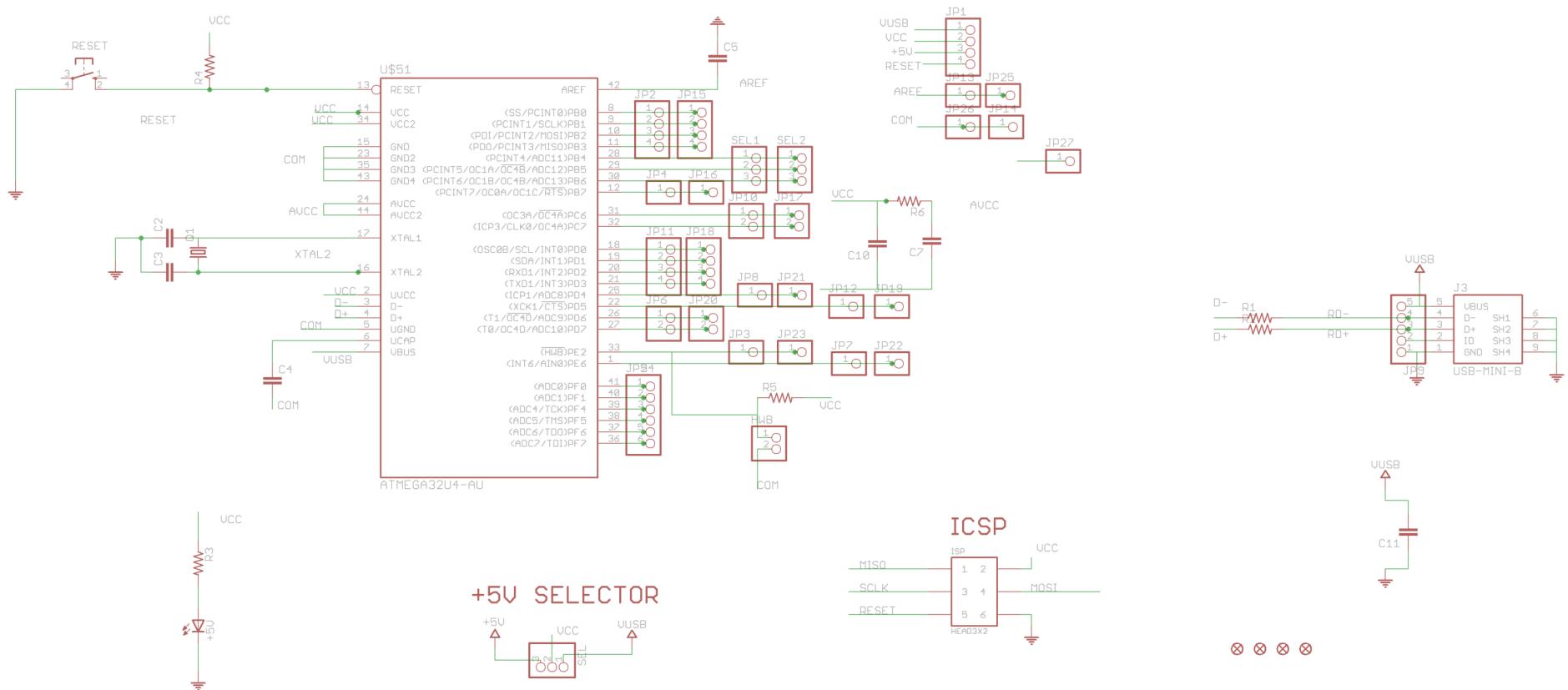
Bit	7	6	5	4	3	2	1	0	MCUSR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0						See Bit Description

Modified MCUSR

ATMEGA328p Board



ATMEGA32u4 Board



To Conclude

- Most useful resources on AVR:
 - Datasheet for ATMEGA328P -
http://www.atmel.com/dyn/resources/prod_documents/doc8271.pdf
 - Datasheet for ATMEGA32u4 -
http://www.atmel.com/dyn/resources/prod_documents/doc7766.pdf
- Next Class
 - Clock options in AVR
 - Interrupt handling
 - Programming the AVR



QUESTIONS?

