EE/CE 6301: Advanced Digital Logic

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Dept. of EE
Univ. of Texas at Dallas

Session 01

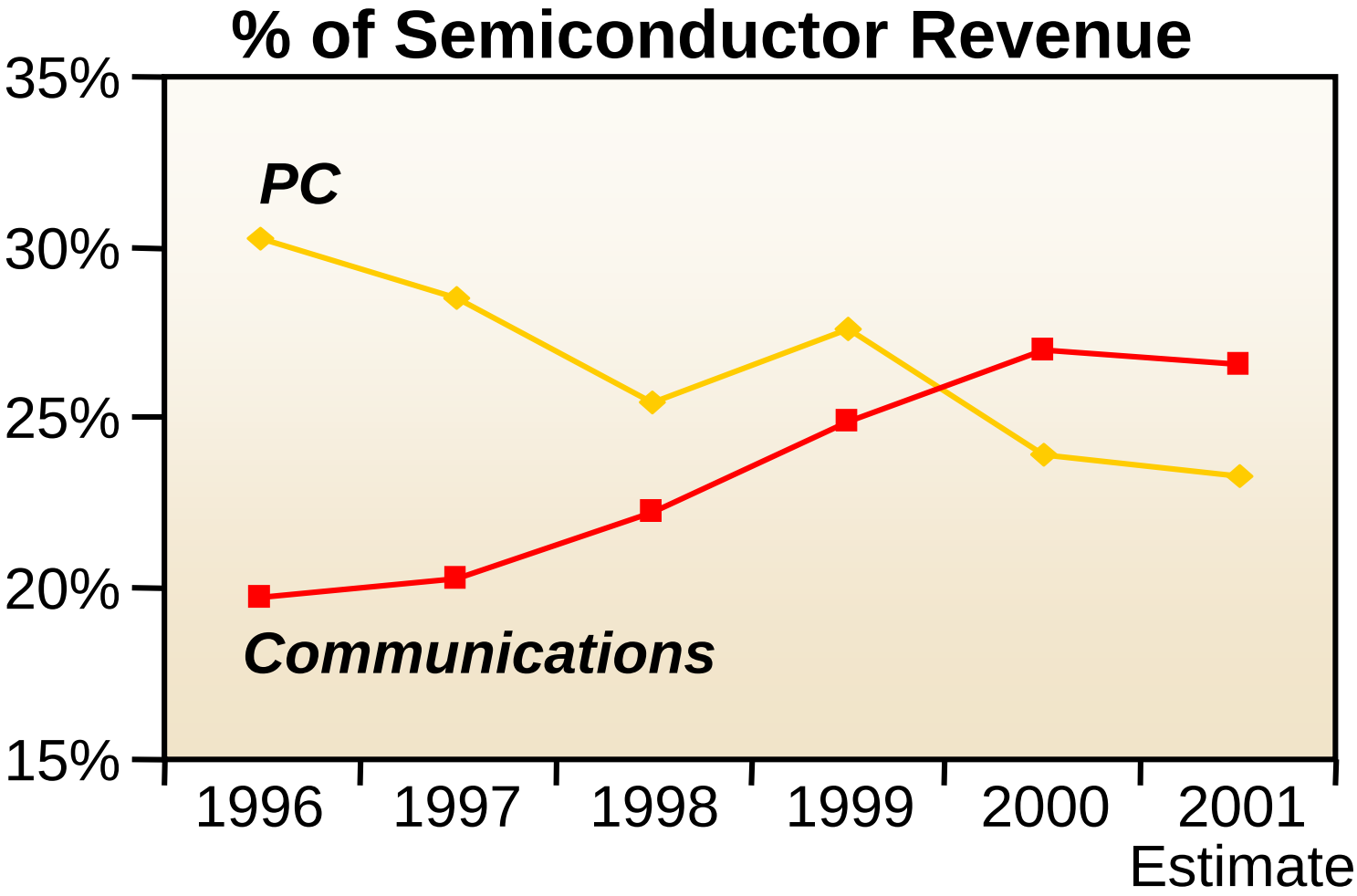
Introduction

Credits

- *This presentation was adapted from work of Mehrdad Nourani of the University of Texas at Dallas.*

Motivational Discussion

PC Market vs. Communication Market



For the first time in 2000, semiconductor revenues in communication exceeded revenues in PC sector.

Source: Dataquest

Personal Products



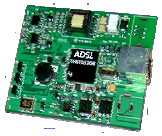
PDA

2G/2.5G Cellular

3D Cellular Phones


Video Phone

IP Phone

Cable Modem

DSL Modem

Bluetooth Products

Home Networking





Digital Still Camera

Digital Camcorder

PDA Camera

Network Still Camera





DAB Radio

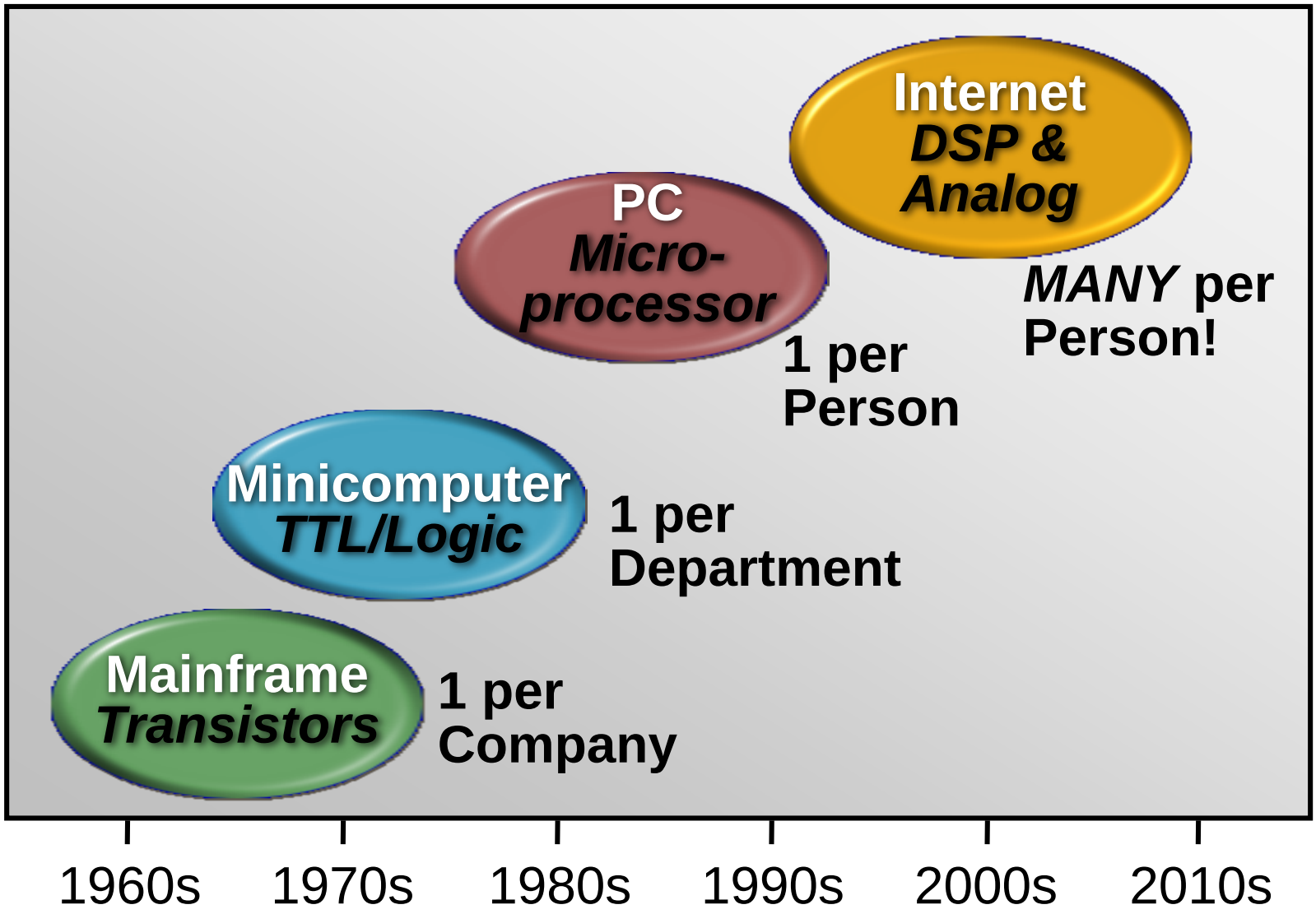
Digital TV

Internet Audio Player

Digital Video Recorder/Server

iSTB

Technology in the Internet Age



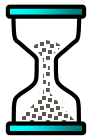
Source: UTD Seminar by Gene Frantz

PC-Age vs. Internet Age

PC Age

Computer Focus

- Non-Real Time
- Stationary
- Digital I/O
- µP and Memory



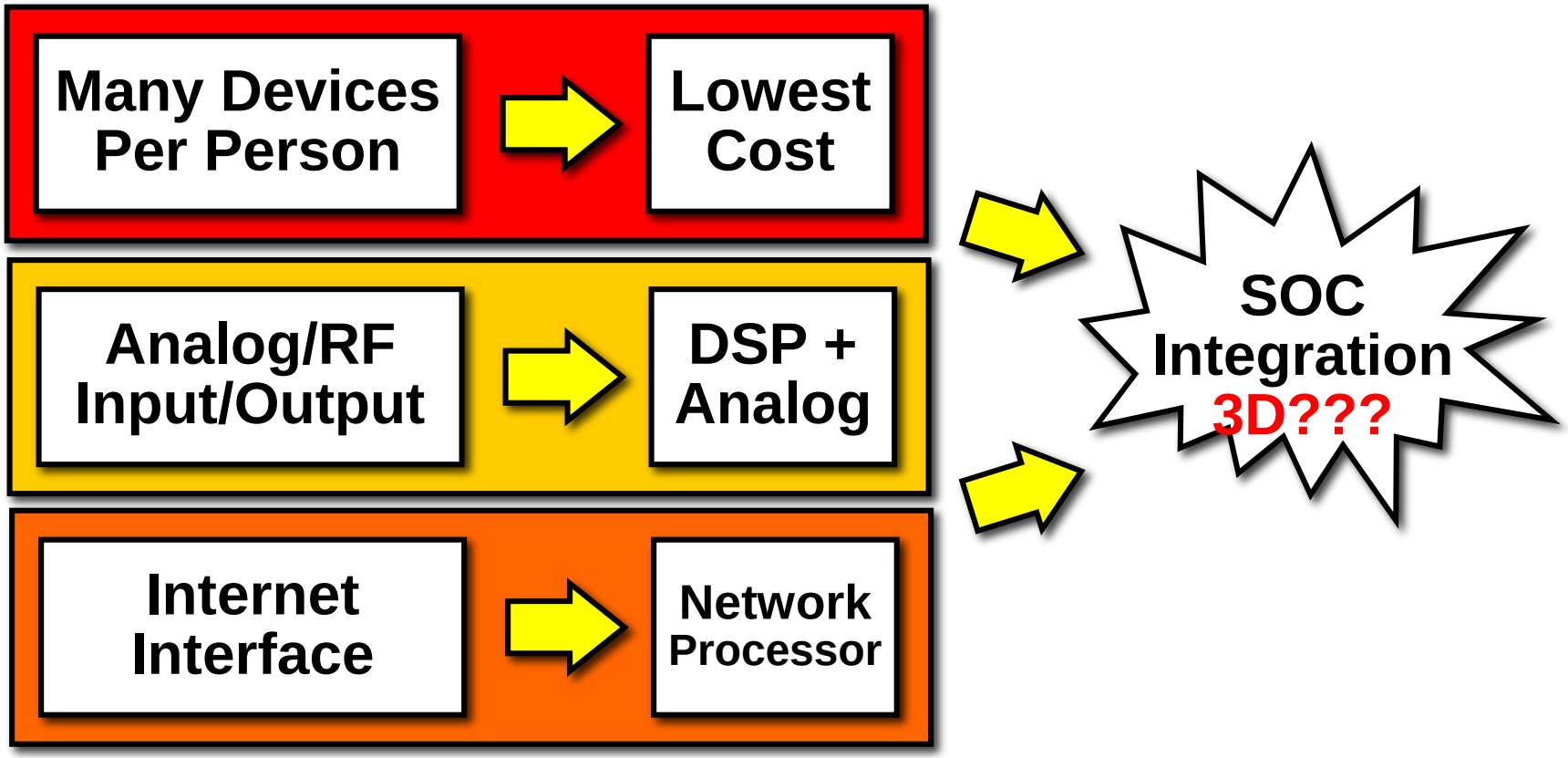
Internet Age

Communication Focus

- Real Time
- Mobile
- Analog I/O
- DSP and Analog

Source: UTD Seminar by Gene Frantz

System-on-Chip Integration + 3D

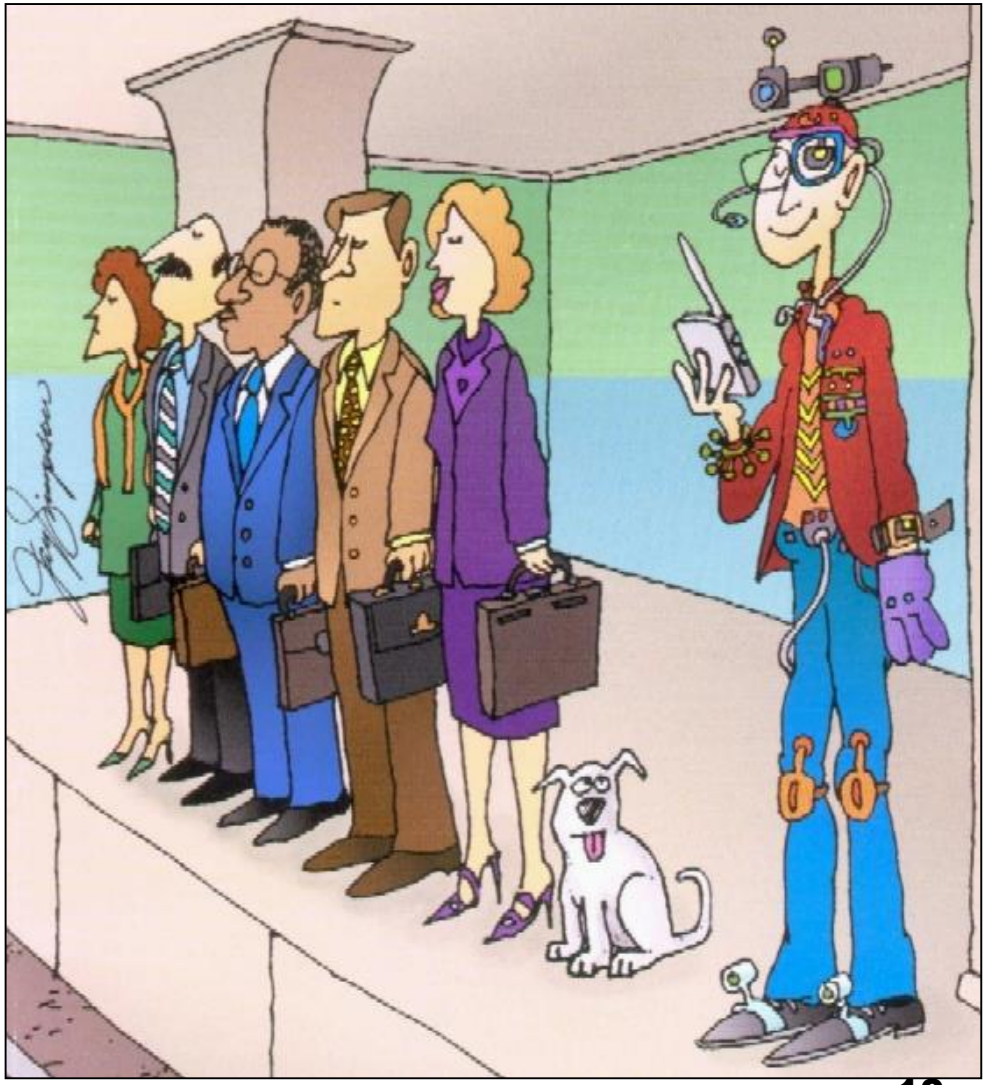


SOC integration means more than integration of multiple IP digital cores. It means integration of functions that are implemented today in different technologies.

Source: UTD Seminar by Gene Frantz

Continued Aggregation

Wireless LAN
Digital Audio
Digital Video
Instant Messaging
Navigation
Camera
Games
E-Commerce
Mobile Devices



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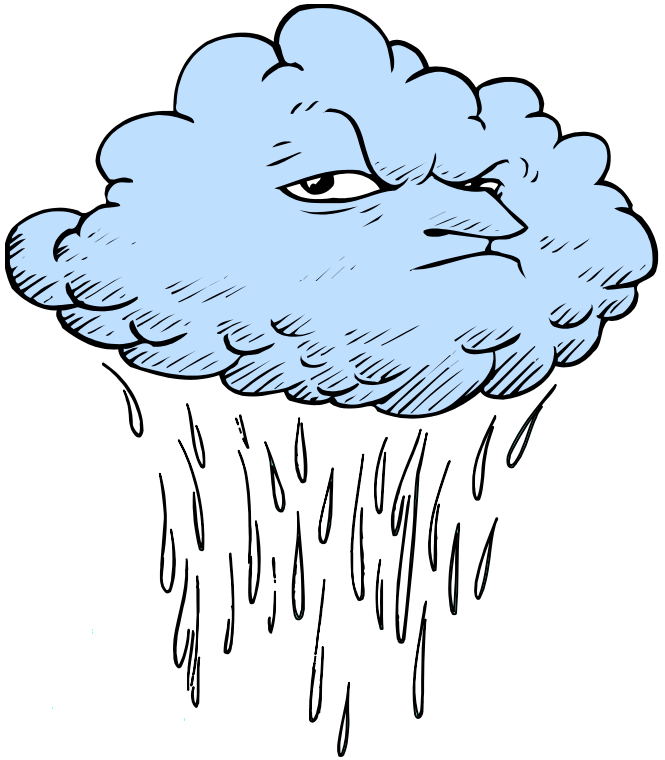
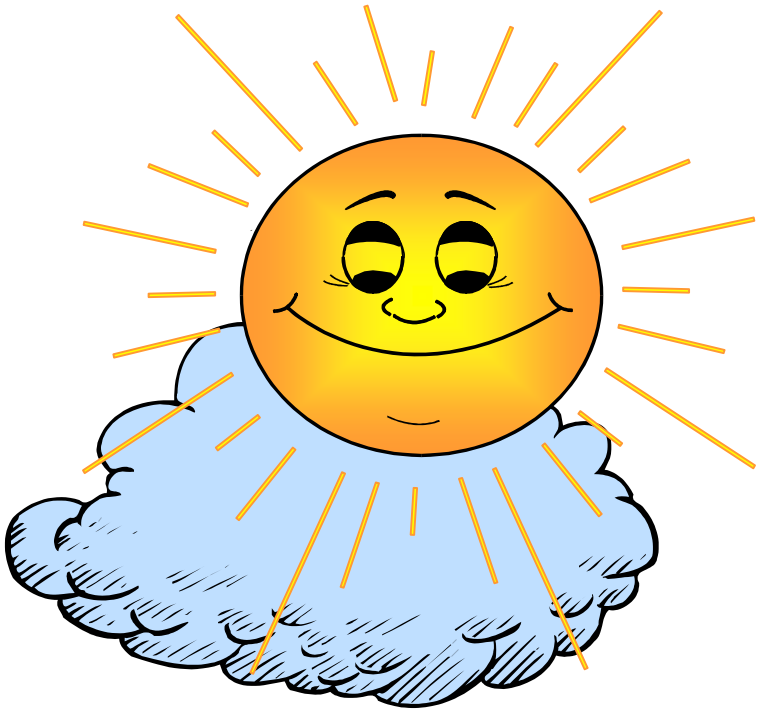
Technology in the Internet Age



Moore's Law is predicted to stagnate toward the end of the decade …

Source: UTD Seminar by Gene Frantz

Technology in the Internet Age



Moore's Law is predicted to stagnate toward the end of the decade …

… but SOC Integration has the potential to continue IC cost reduction and to perpetuate growth of Personal Internet Products.

Source: UTD Seminar by Gene Frantz

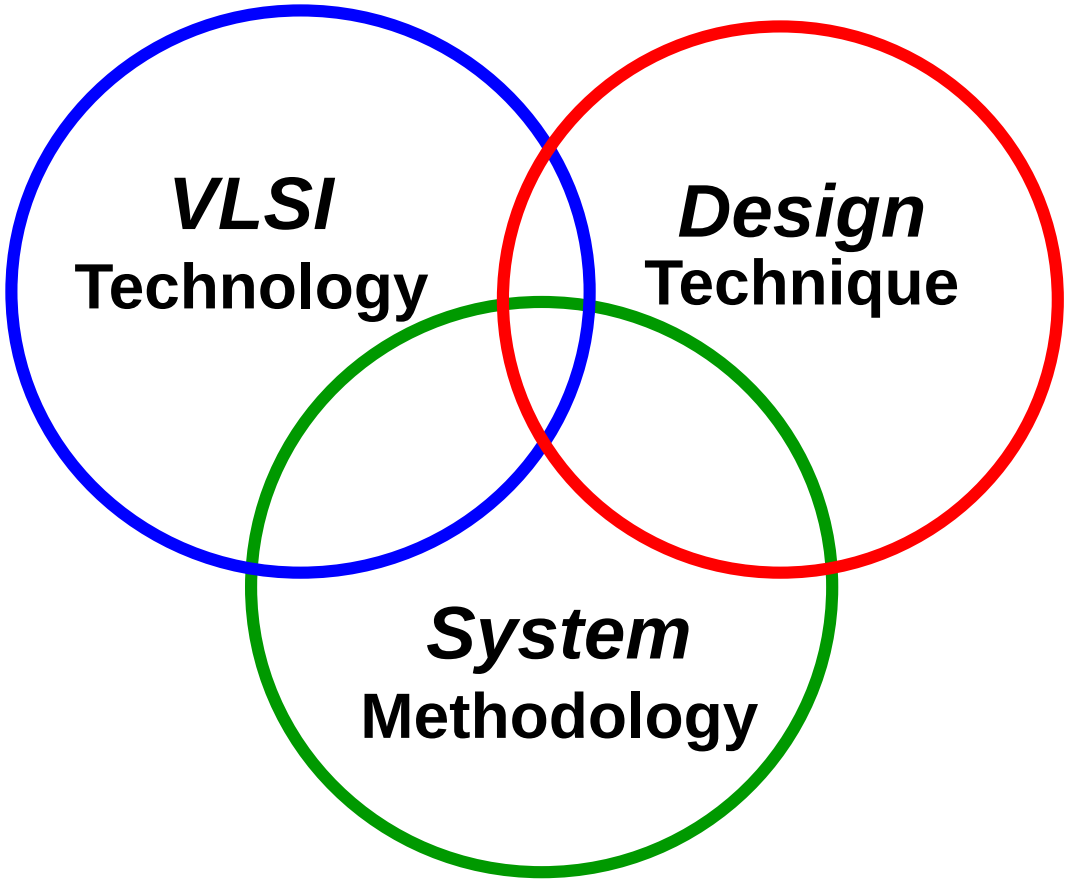
Amazing Growth

- 1971: Intel 4004
  - —2300 Transistors, 750KHz, 60000 Operations/sec
  - —$200
- 2000: DEC Alpha
  - —15.2 Million Transistors, 700MHz,2 Billion Operations/sec
  - —$300
- Gordon Moore (Intel founder):

"If the car industry had been progressing at the rate the semiconductor industry has, today a Rolls-Royce would cost three dollars, could get half-a-million miles per gallon of gas, and would be cheaper to throw away than to pay for parking."

What is Our Course About?

- We need to have a good understanding of three concepts:



SoC: System on a Chip

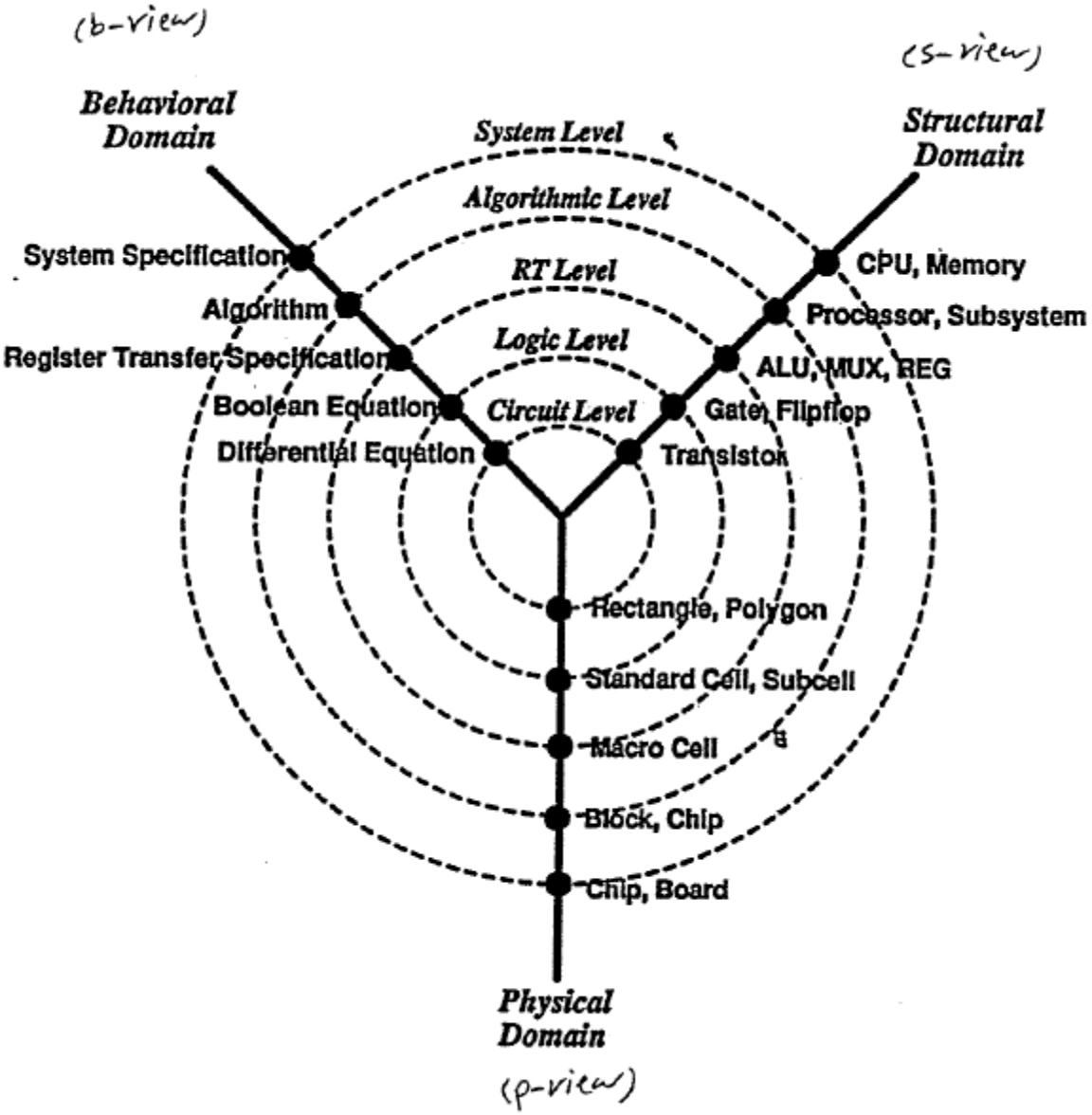
- The 2005 prediction: SoC's will be > 500M gates
- How do you create million gate ASICs with same amount of resources? While ...
  - —Decrease development time
  - —Increase functionality and performance
  - —Keep small design teams

- Important Issues
  - —Design Methodology (Design flow)
  - —Tools that support the Methodology
  - —IP reuse (Intellectual Property)

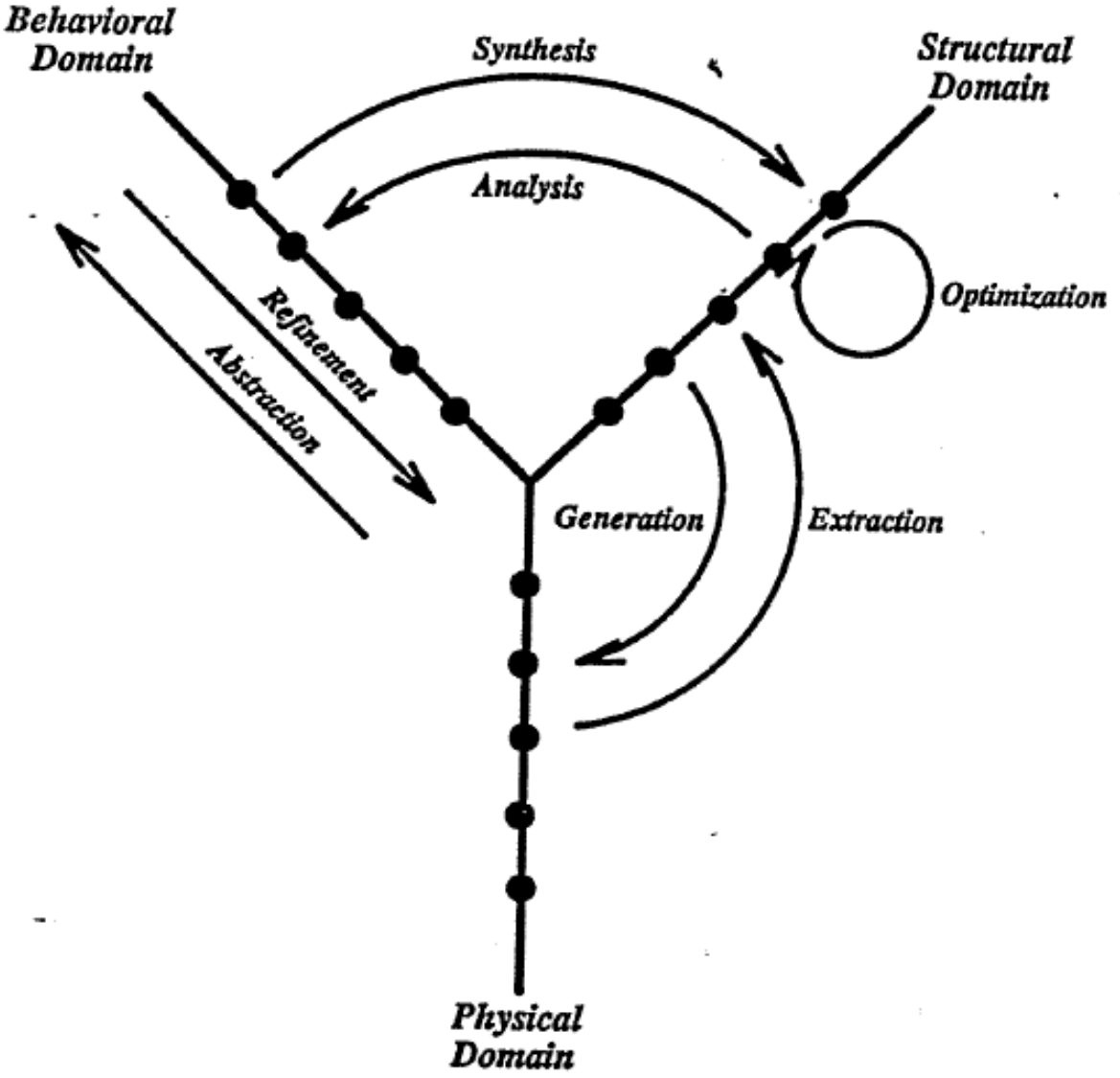
Modeling Types

- Behavioral model
  - —Explicit definition of mathematical relationship between input and output
  - —No implementation information
  - —It can exist at multiple levels of abstraction
    - – Dataflow, procedural, state machines, …
- Structural model
  - —A representation of a system in terms of interconnections (netlist) of a set of defined component
  - —Components can be described structurally or behaviorally

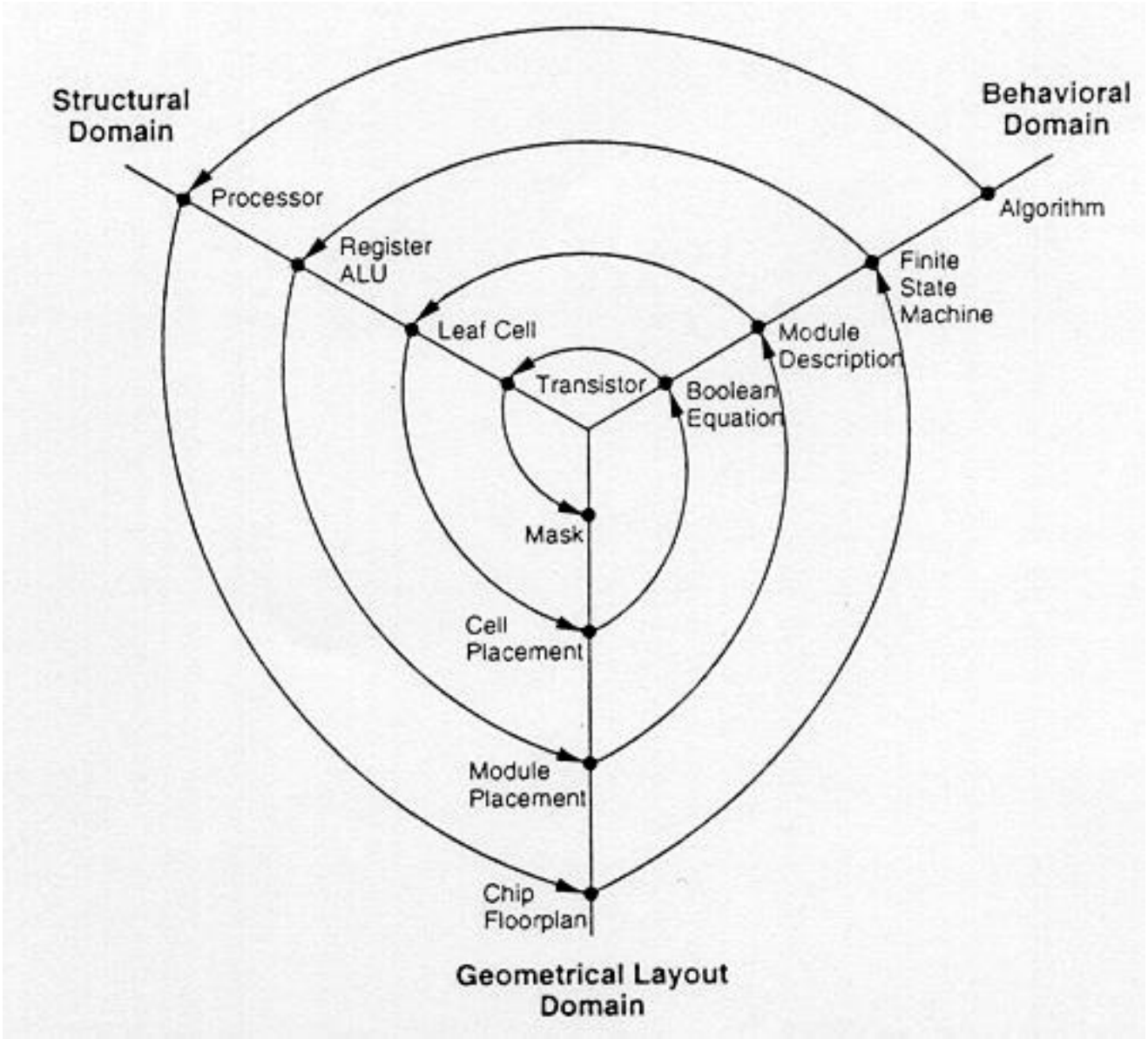
The Y-Chart - Levels of Abstraction



The Y-Chart - Terminology



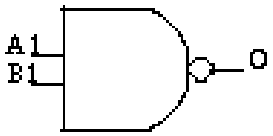
The Y-Chart – Design Flow



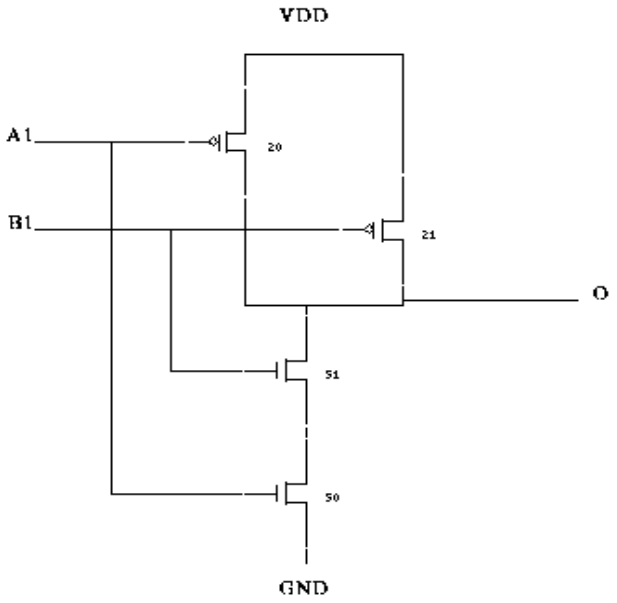
Example: Various Models or Views of a NAND Gate

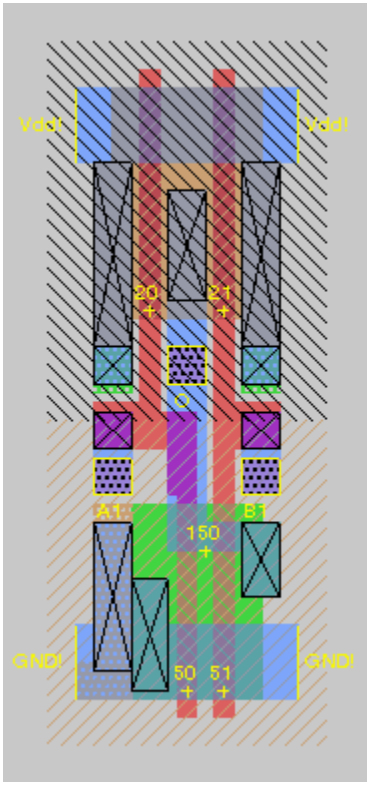
O <= NOT (A1 AND B1);

Behavioral Model:
(Boolean Equation)



Structural Model:
(Logic Gate)

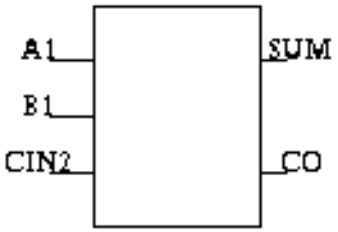




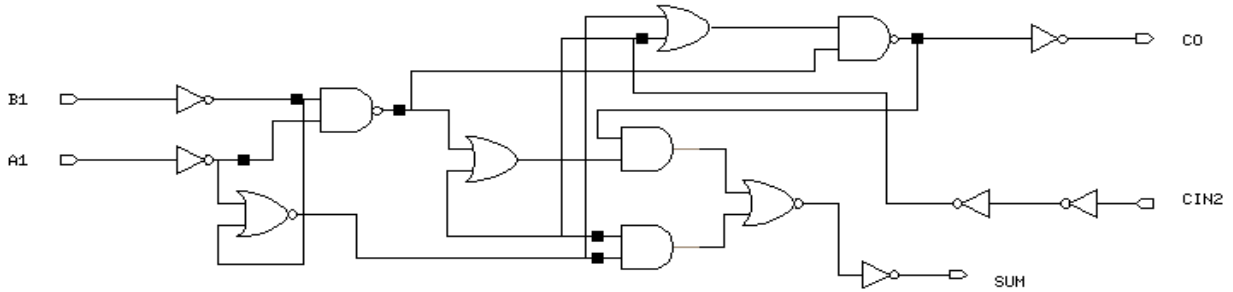
Physical Model:
(Transistors or Layout Mask)

Example: Various Views of Full Adder

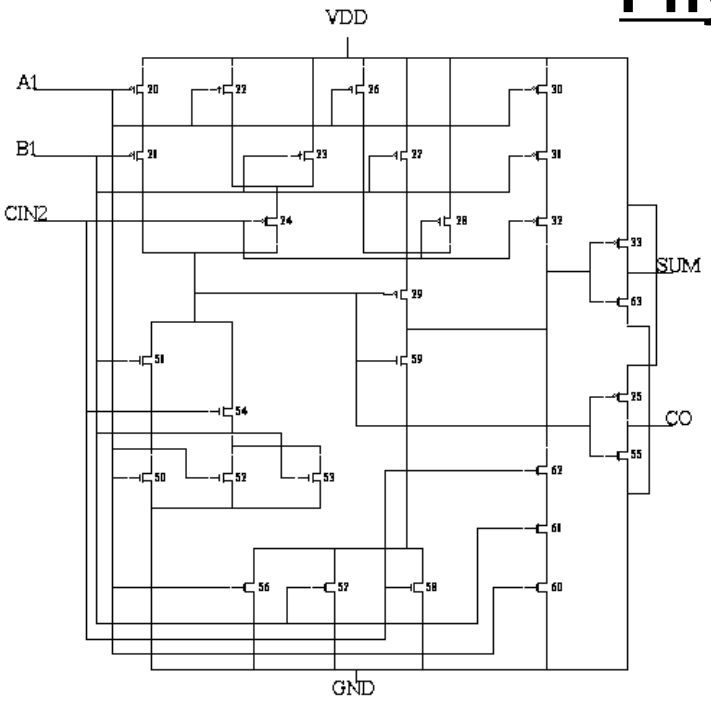
Behavioral model

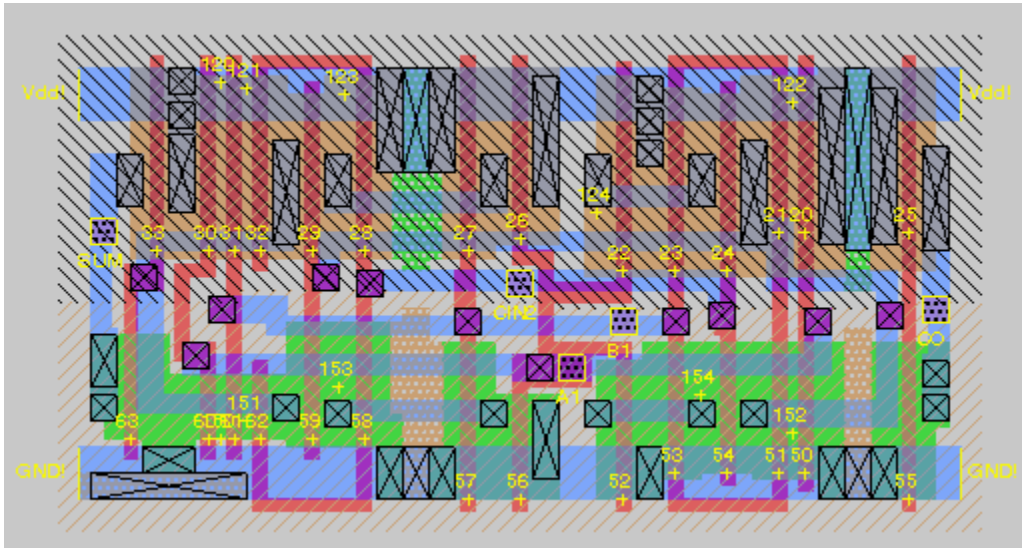


Structural model



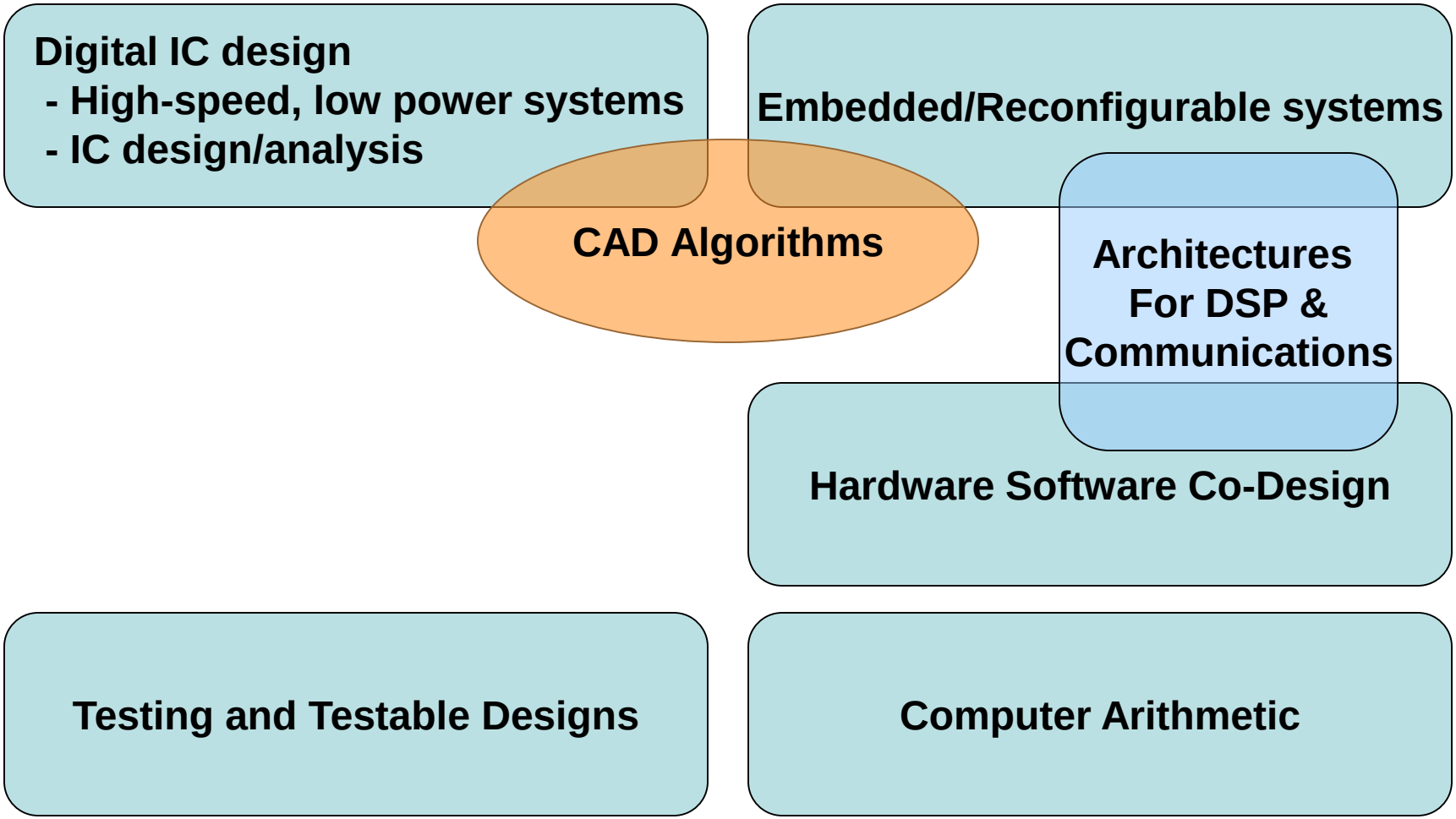
Physical model





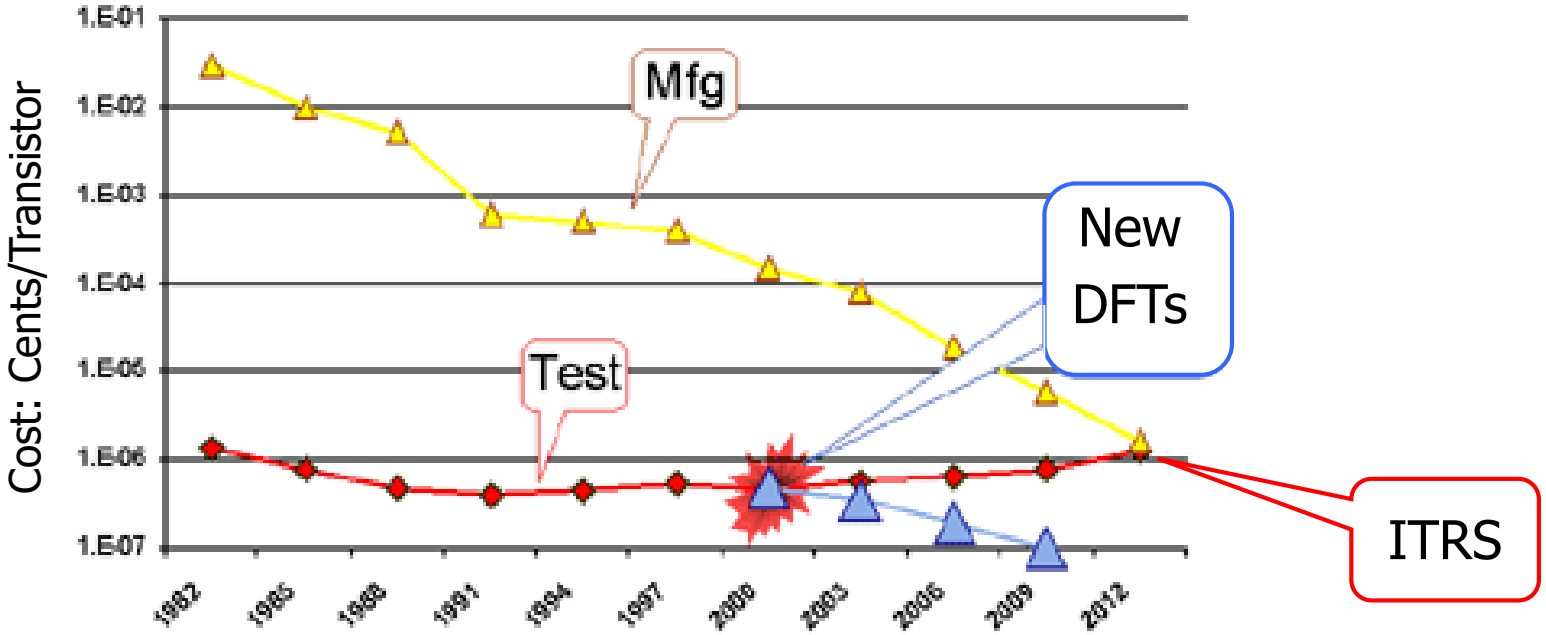
Importance of VLSI Test

Key Research Issues



Importance of VLSI Testing

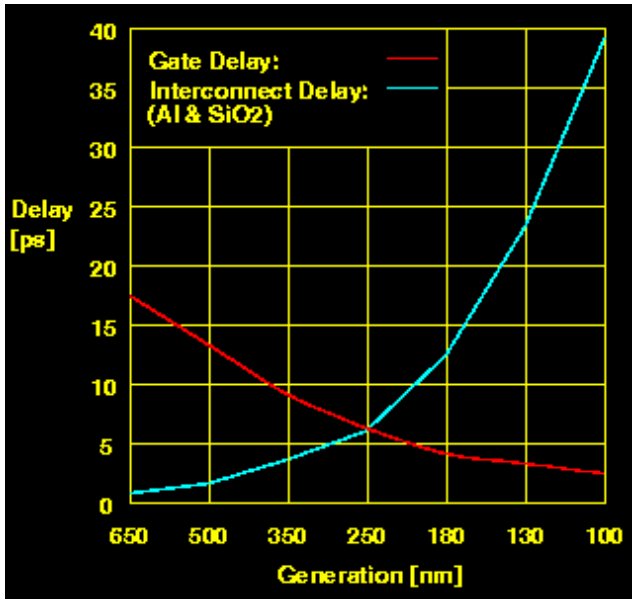
- Test cost will be dominant in this decade [ITRS'01]



Result of Technology Scaling

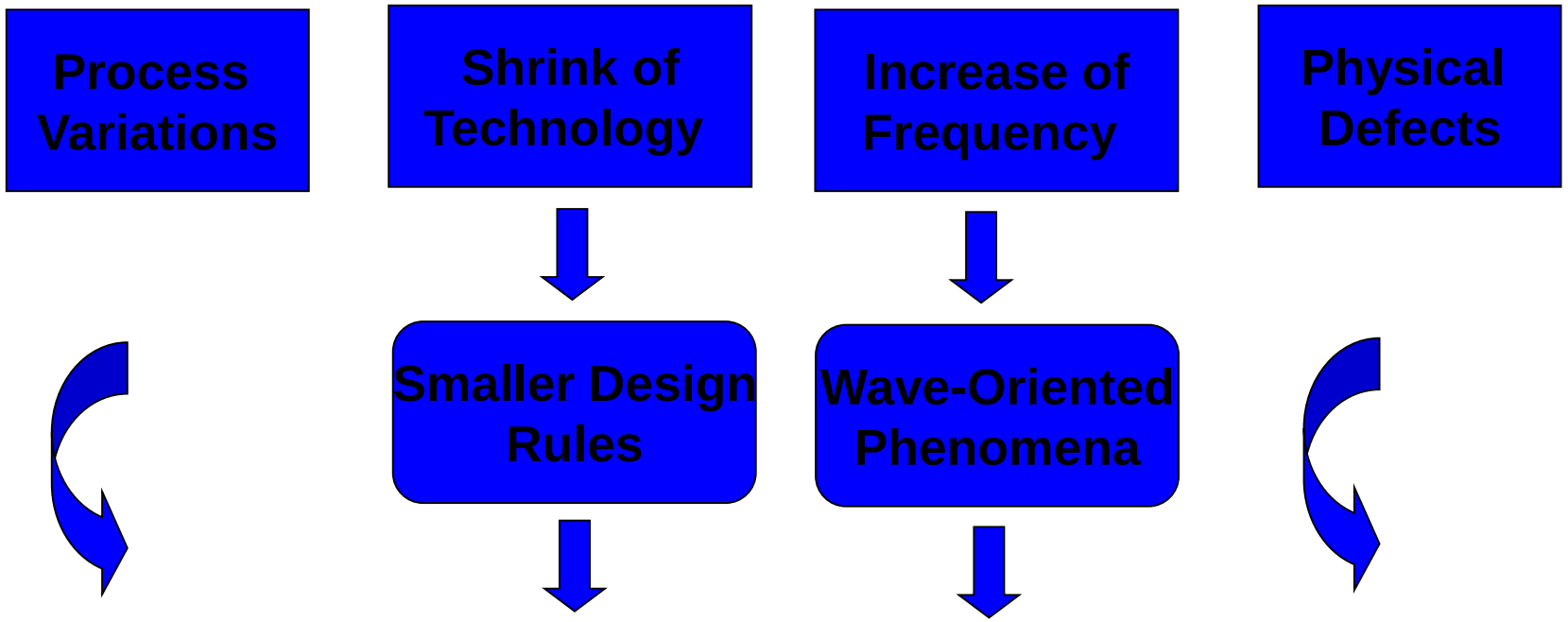
Source:

[ITRS'01 Roadmap]



Factors	Technology				
Technology [nm]	0.35	0.25	0.18	0.13	0.10
Coupling C [pF]	41.59	49.73	56.93	64.17	70.54
Ground C [pF]	12.89	10.06	9.65	7.30	6.42
Mutual L [nH]	0.80	0.84	0.88	0.93	0.97
Self L [nH]	1.17	1.17	1.18	1.21	1.23

Testing for Signal Integrity

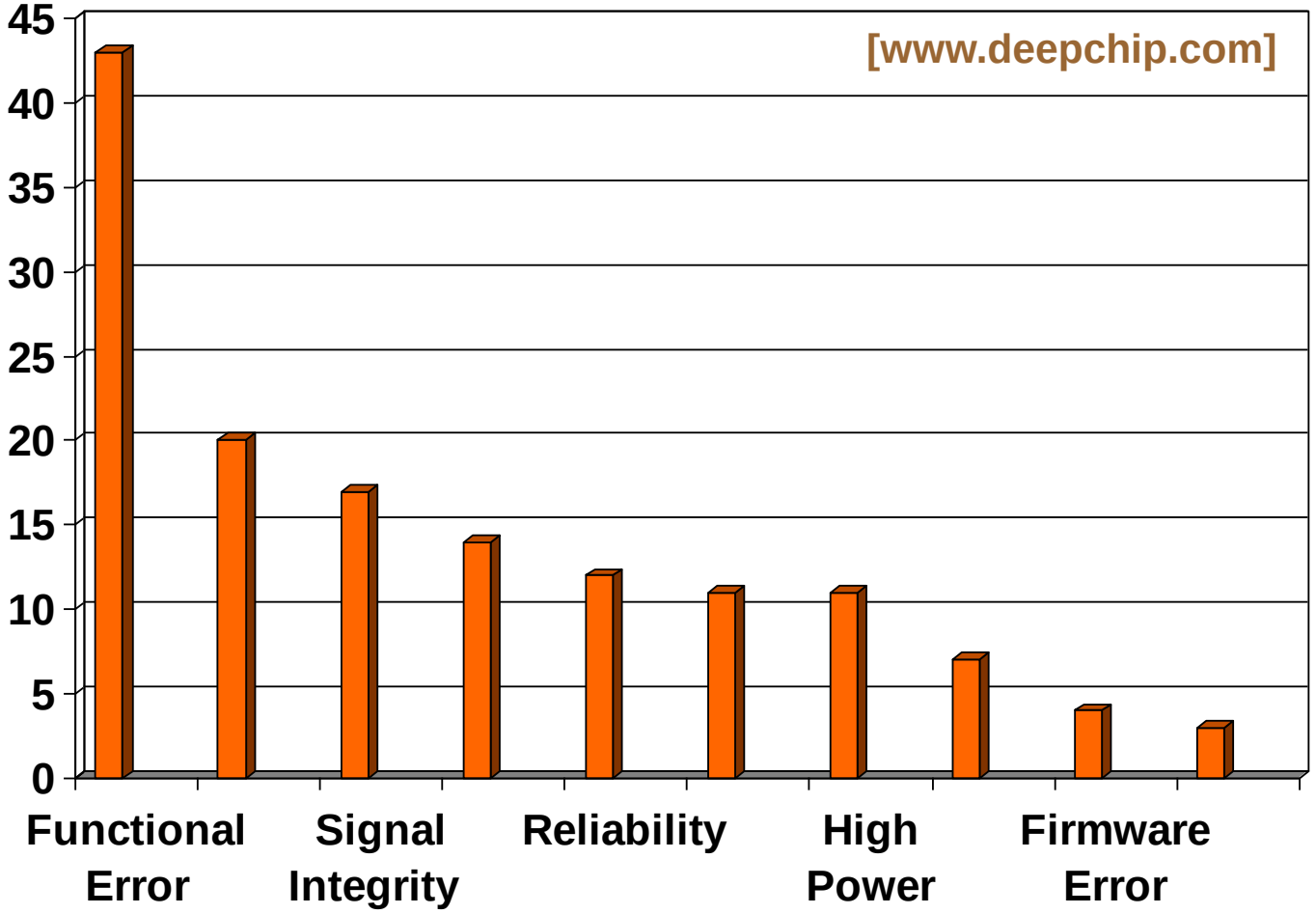


"There are only two kinds of designers: the ones who have signal integrity problems, and the ones who will."

[www.chipcenter.com]

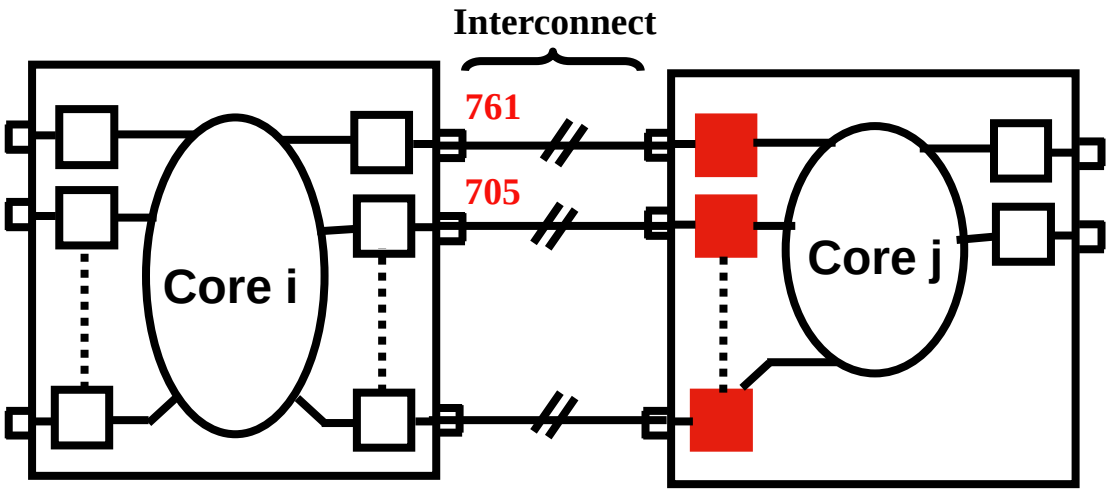
Fatal Problems on First Spin

- Overall 61% of new ICs require at least one re-spin



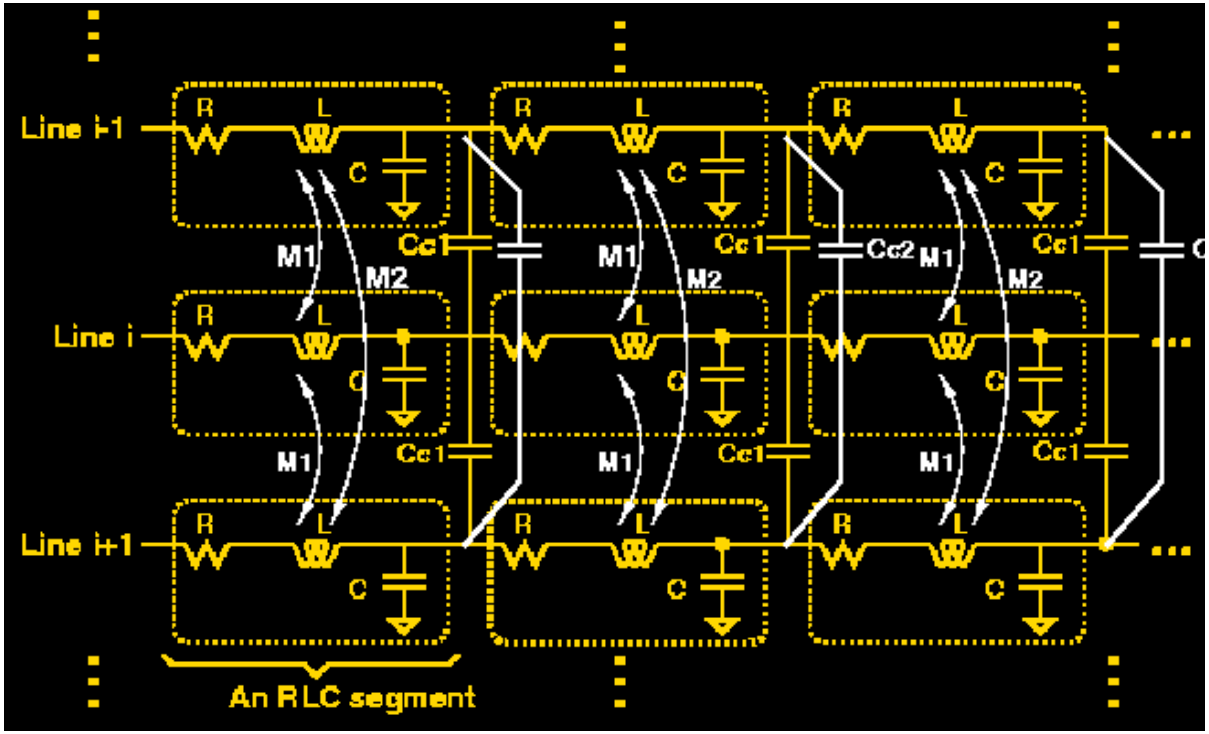
The Bottom Line

- Signal integrity loss occurs due to process variations, manufacturing defects, the parasitic and coupling C/L. Integrity loss leads to failure.
- Signal integrity problem is both design & test issue. A systematic approach for testing is needed.



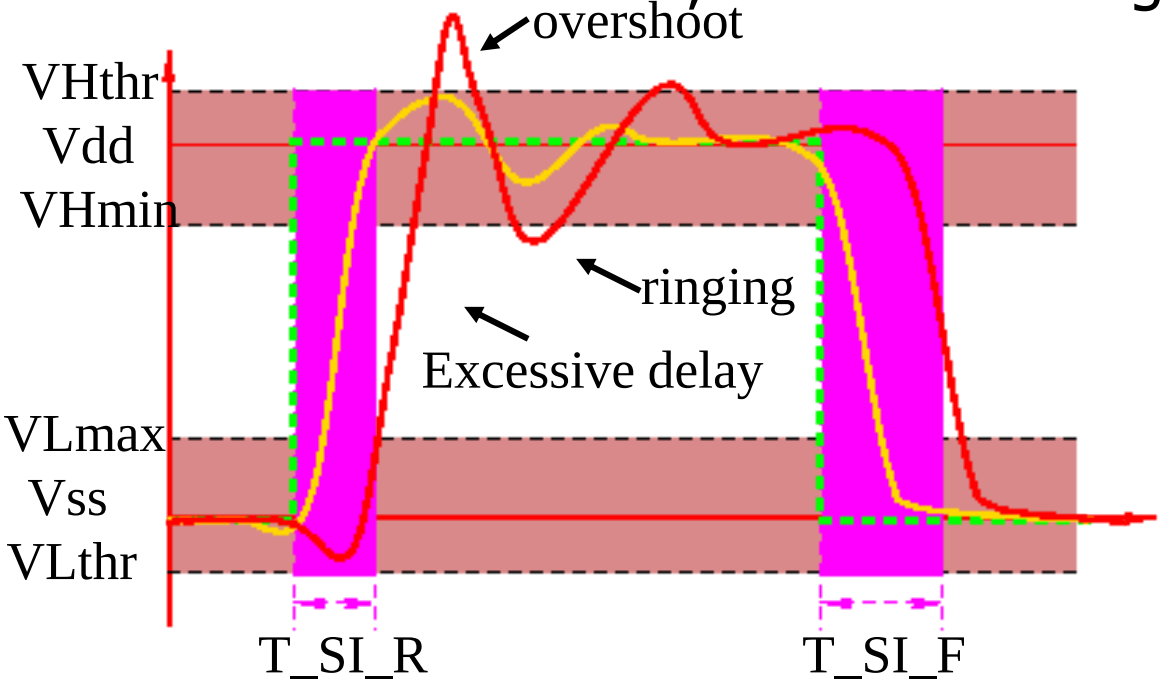
Interconnect Model

- Signal integrity problems originate from interconnects.
- Distributed RLC model is too complicated.



Integrity Loss Model

- Excessive delay degrades performance and causes functional error.
- Ringing causes functional error.
- Overshoot contributes to noise, delay, hot carrier, time-dependent dielectric breakdown, and electromigration.

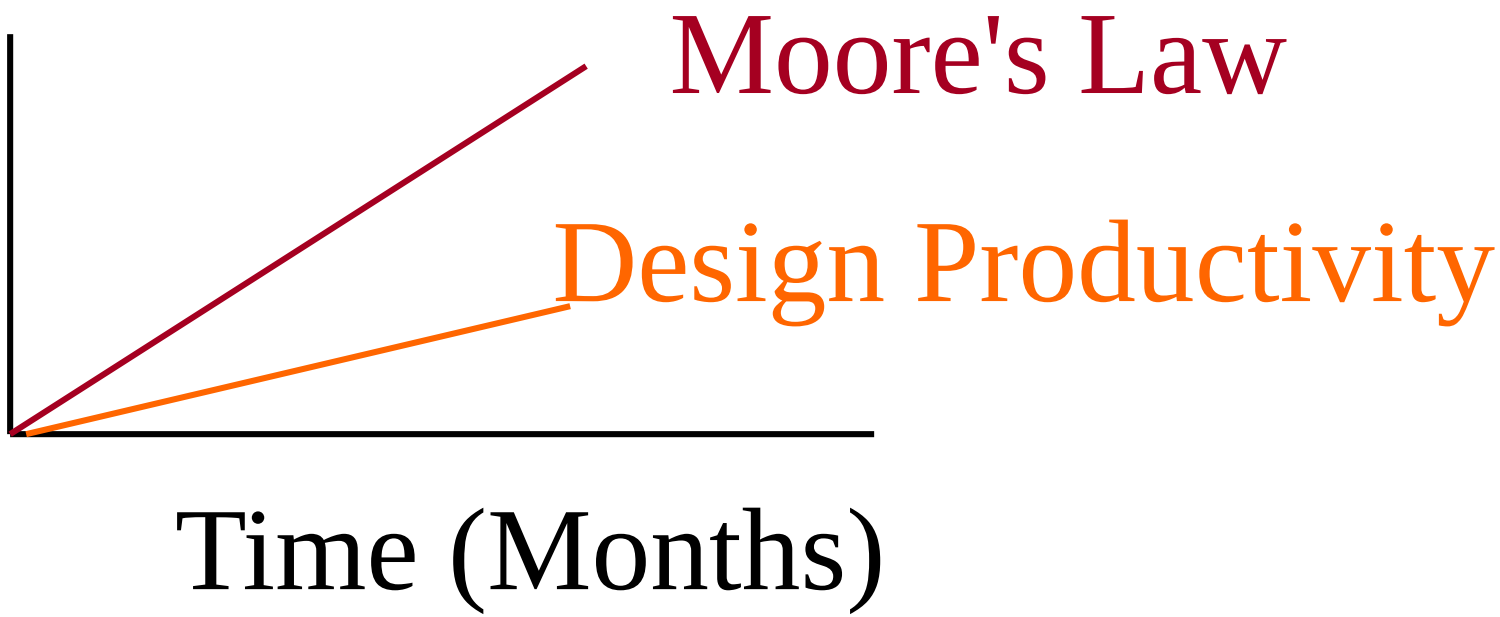


Importance of CAD

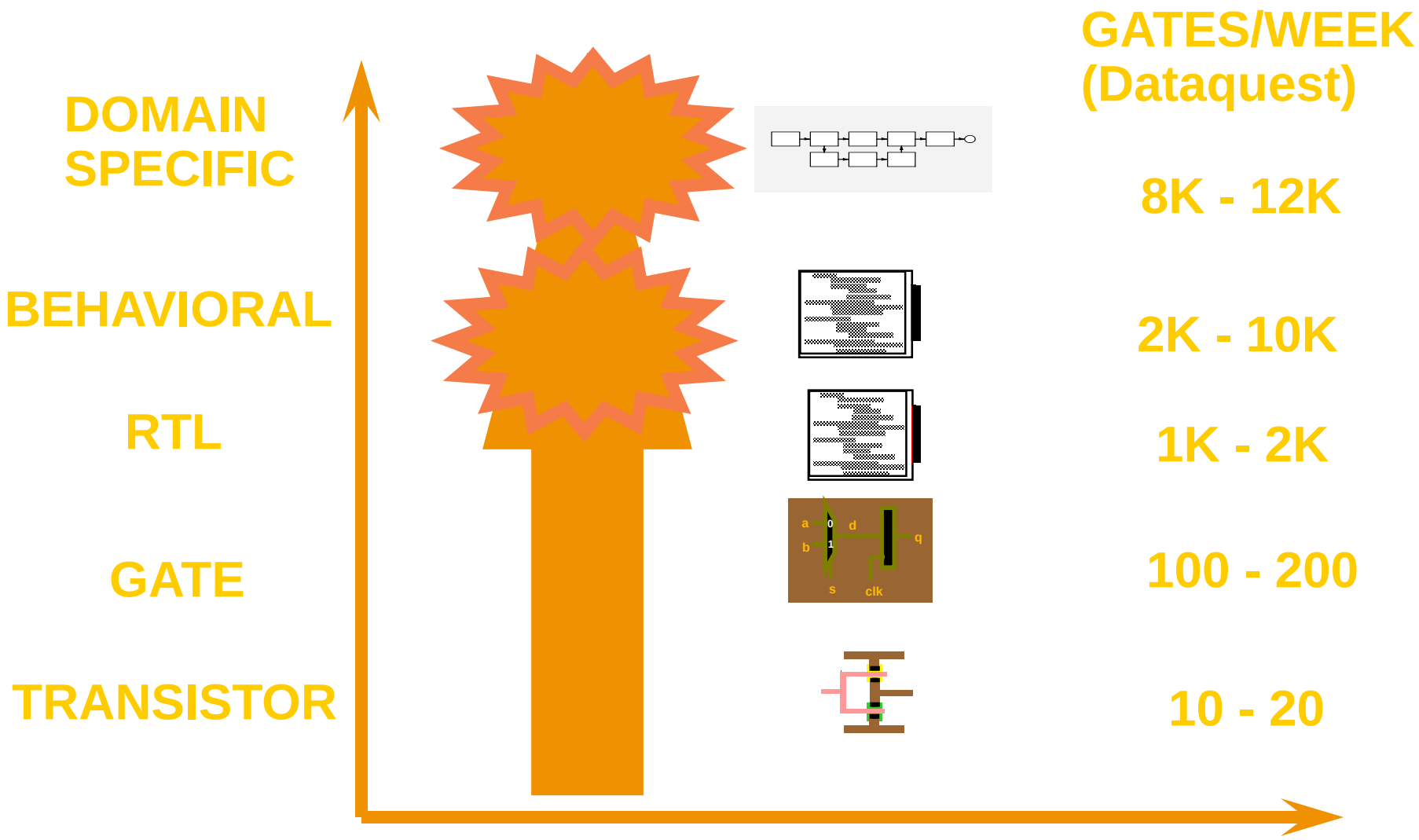
Role of CAD Tools

- CAD tools improve productivity
- Definition: A software program which assists in performing or automates a particular design function
- Major types:
  - Schematic capture
  - Analyzers/Simulators
  - Synthesis

Design Complexity and Productivity



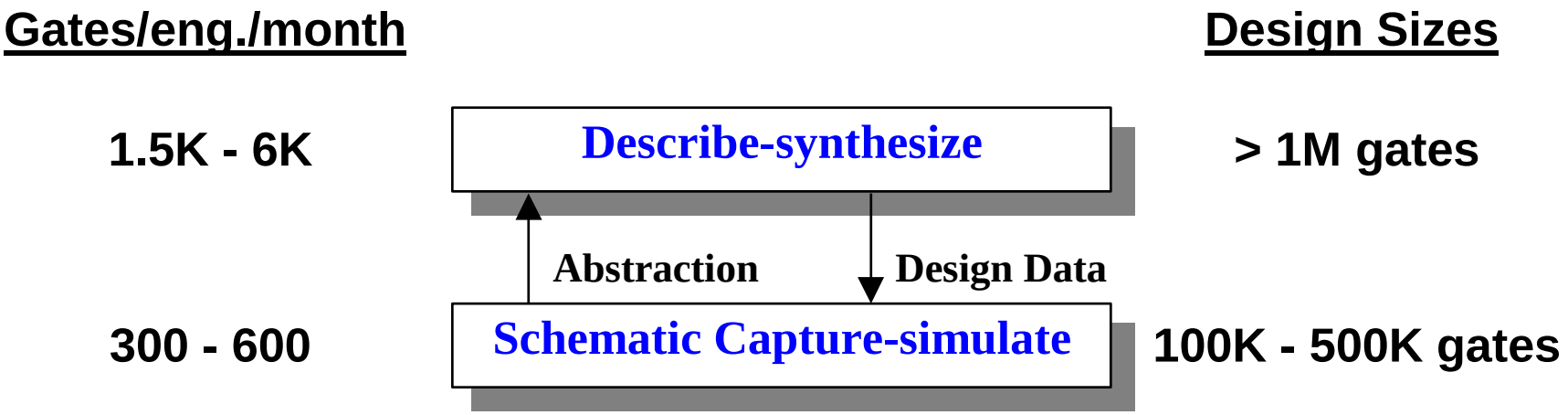
Design Productivity by Approach



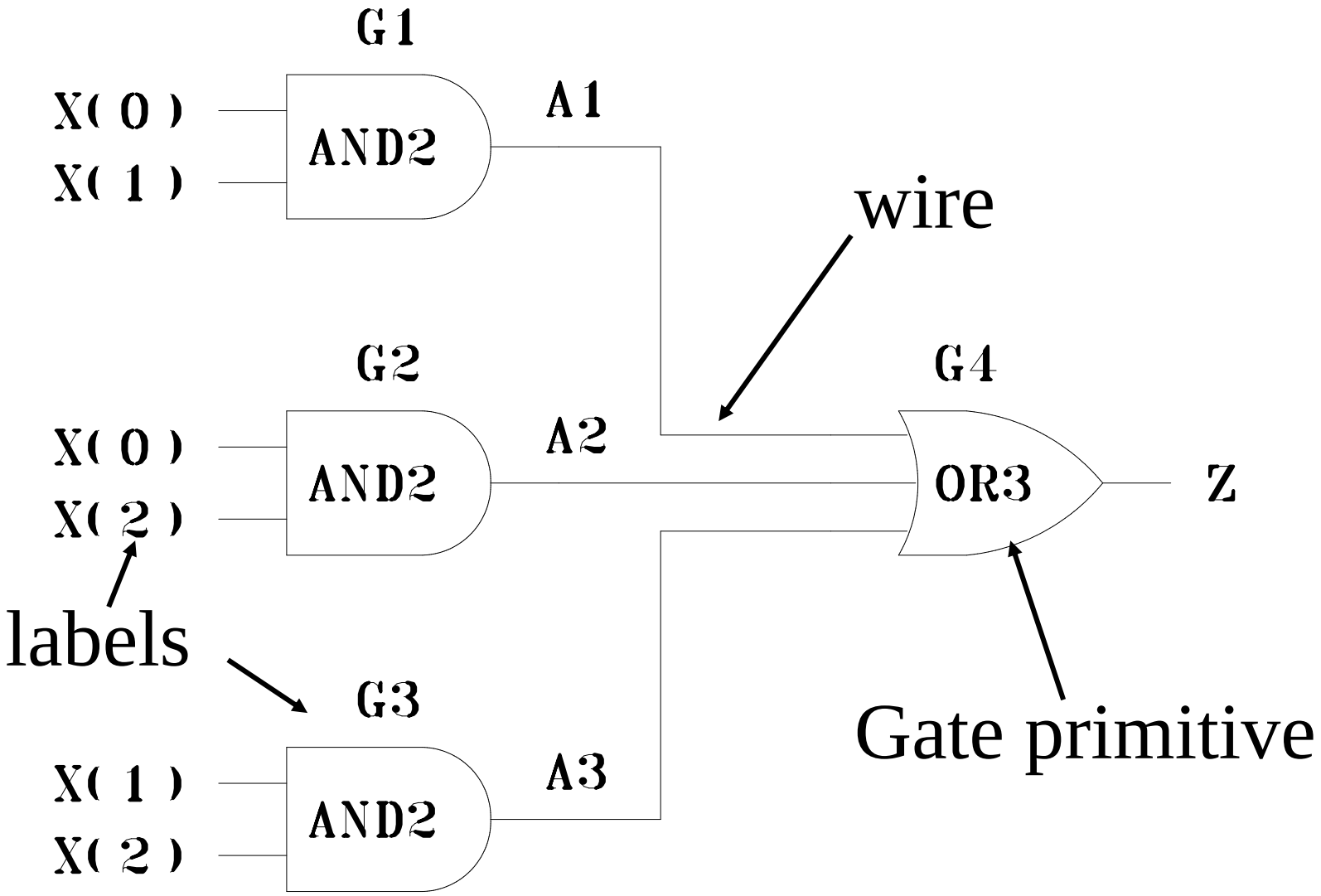
Source: Keutzer (UCB EE 244)

CAD Design Approaches

- Goal of each CAD design flow methodology is to increase productivity of the design engineer
- Increasing the abstraction level of the design methodology and tools is one approach:



Schematic Capture



Schematic Capture Editor

- Definition: An editor which can be used to create and display an interconnected set of graphic tokens.
- Graphic token types:
  - —primitives (built-in)
  - —new models
- Uses of schematics
  - —simulation
  - —wiring

Simulators

- Definition: A program which models the response of a system to input stimuli.
- Types: deterministic and stochastic.
- Simulation is used to establish design correctness (70% of design time).
- A model underlies simulation.

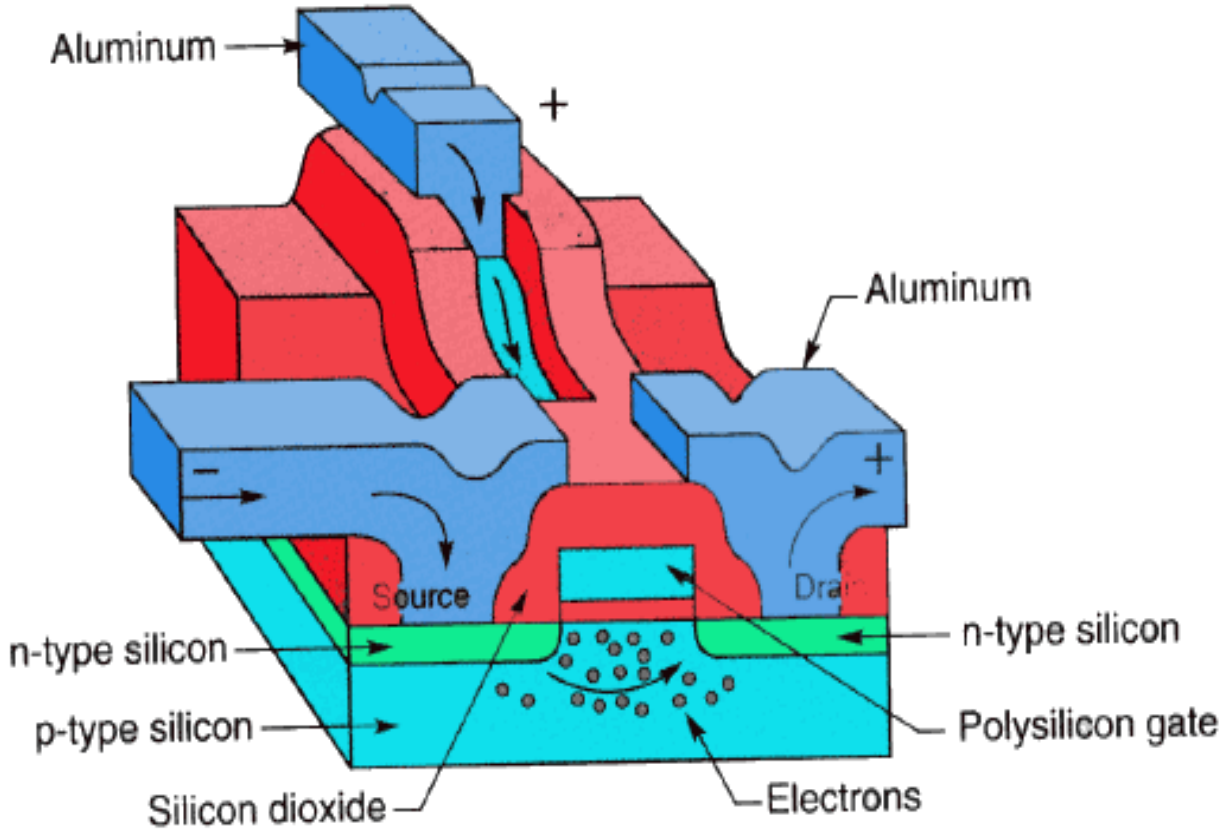
Factors Affecting Design Efficiency

- Programming Method
- Computer Architecture
- Level of Abstraction
- Rule: Simulate at the highest level you can, and still get desired information.
- Rule-of-10: It will be 10 times more costly if the problem is discovered in the next level.

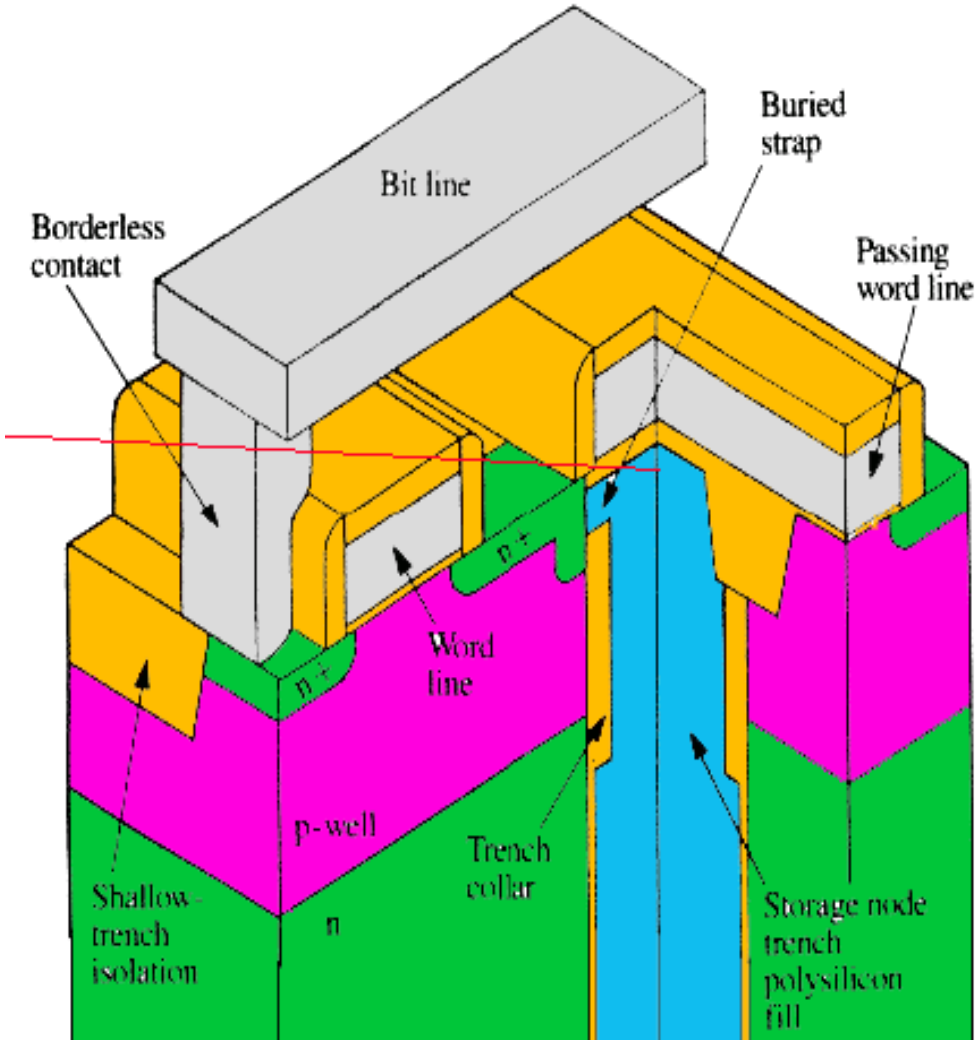
Why System (High) Level Design?

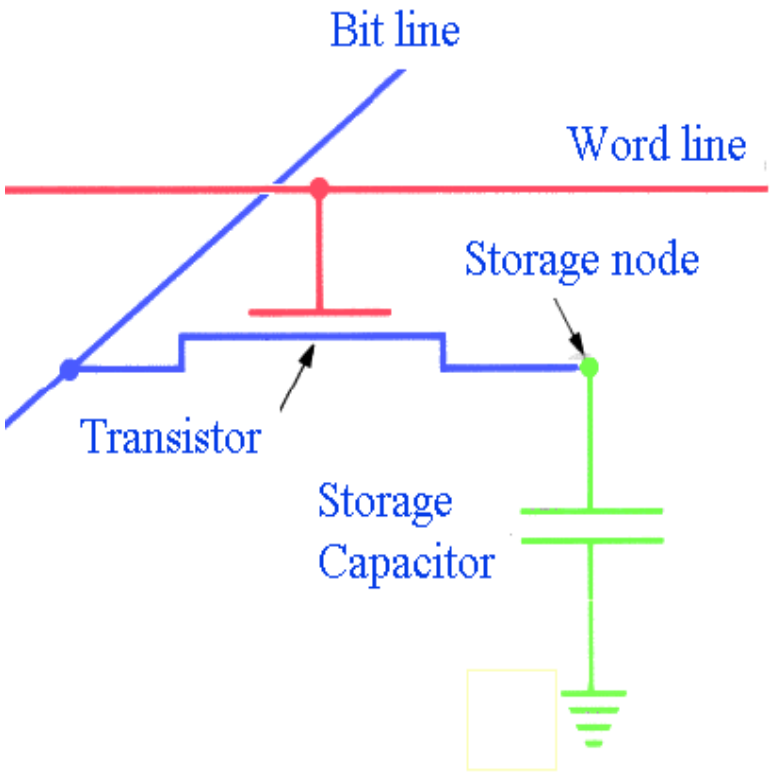
- To answer, we need to look over the past 30 years of chip development and their growing complexity
- To appreciate why we need high level design techniques, let's take a look at complexities in the lower level of abstractions (e.g. transistor/ layout levels).

Complexity of Real Devices – A Transistor



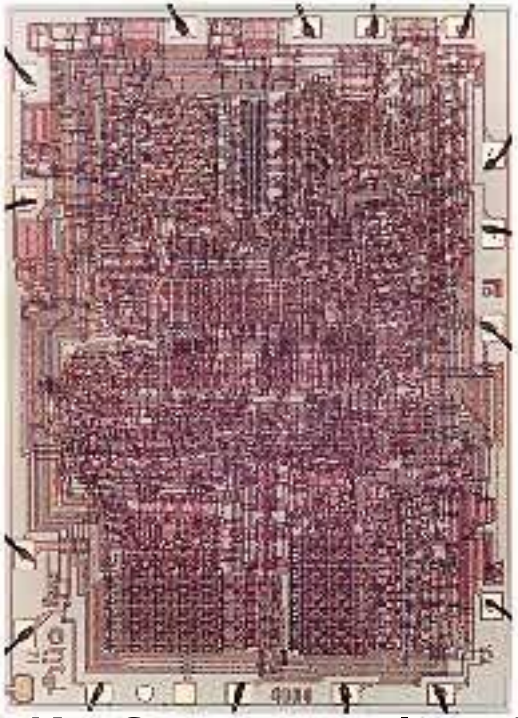
Complexity of Real Devices – A DRAM Cell





SoC: Intel Microprocessor History: 4004

- 1971 Intel 4004, 4-bit, 0.74 Mhz, 16 pins, 2250 Transistors

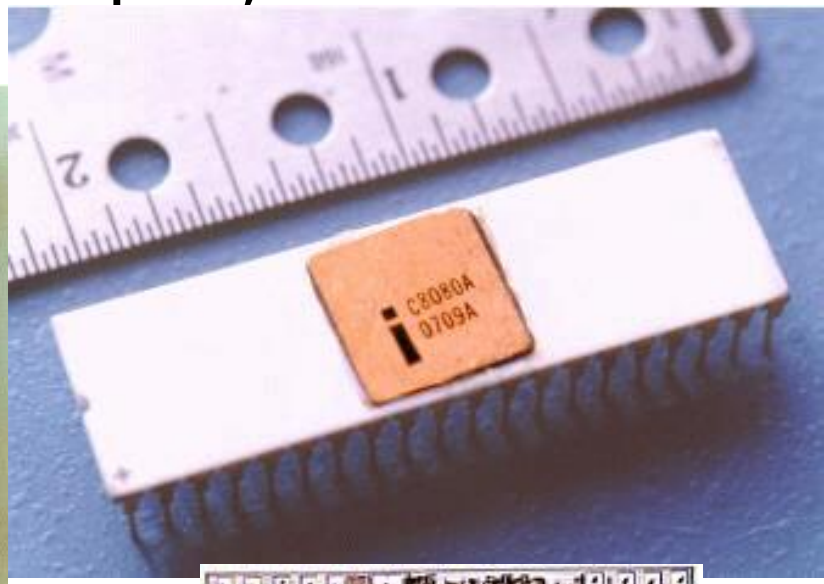


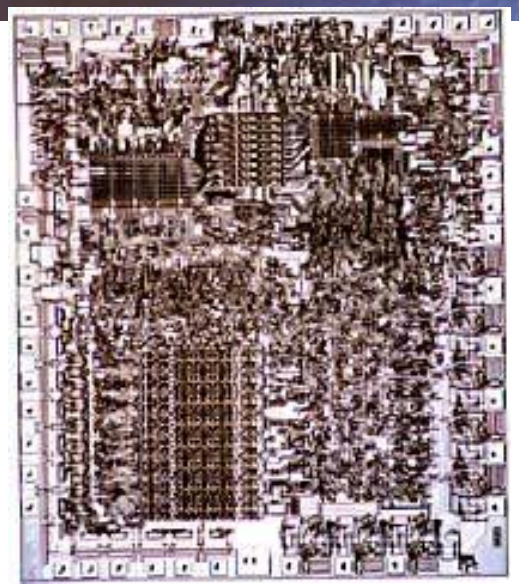
- Intel publicly introduced the world's first single chip microprocessor: U. S. Patent #3,821,715.
- Intel took the integrated circuit one step further, by placing CPU, memory, I/O on a single chip

SoC: Intel Microprocessor History: 8080

- 1974 Intel 8080, 8-bit, 2 Mhz, 40 pins, 4500 Transistors

Altair 8800 Computer



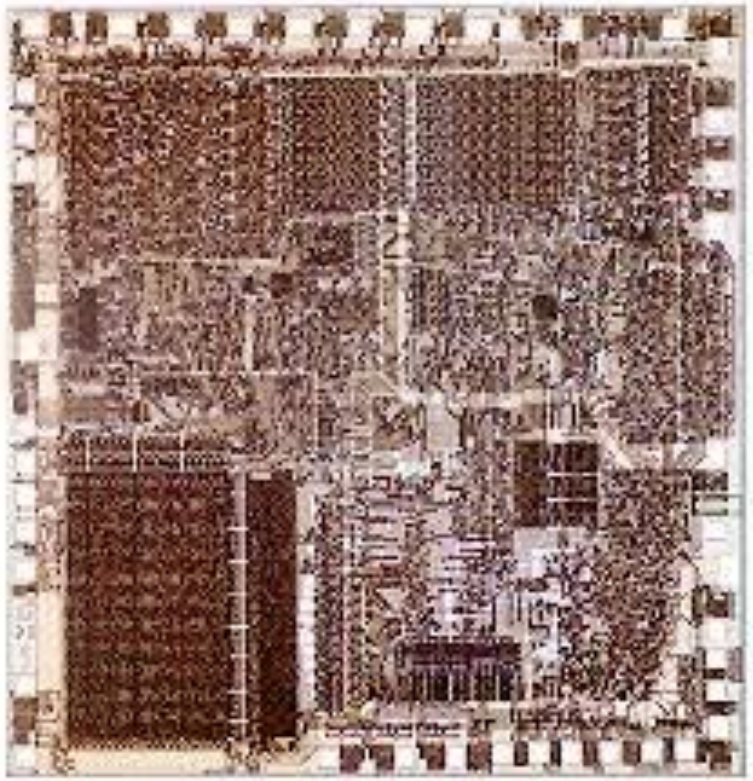


Bill Gates & Paul Allen

write their first Microsoft software product: Basic

SoC: Intel Microrocessor History: 8088

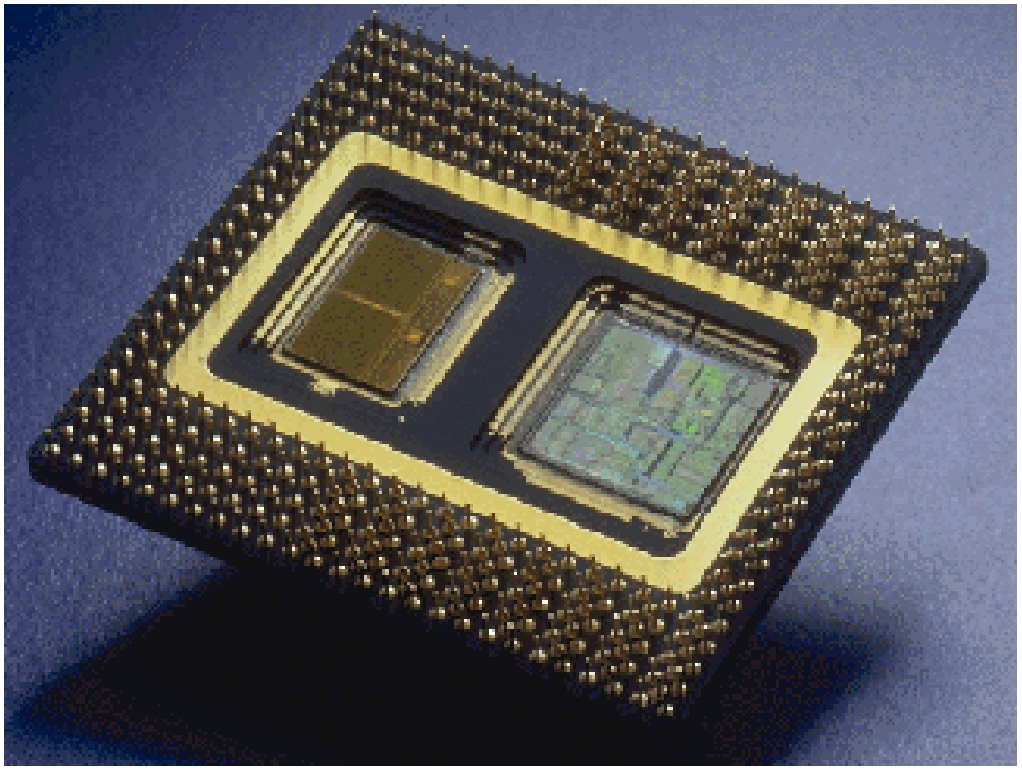
- 1979 Intel 8088, 16-bit internal, 8-bit external, 4.77 Mhz, 40 pins, 29000 Transistors

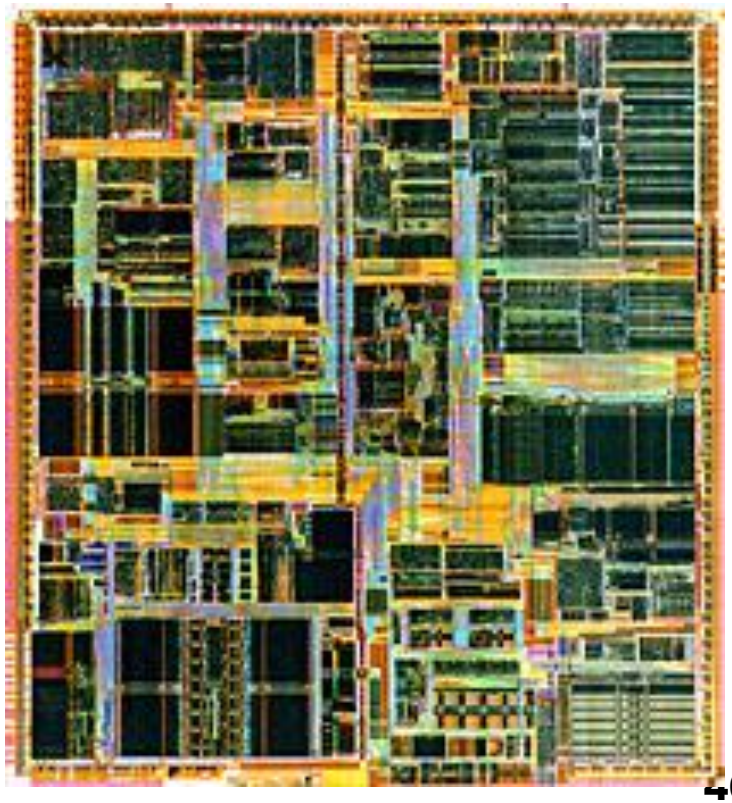


- 0.128M - 0.640M RAM
- 0.360Kb, 5.25” Floppy
- 10M Hard Disk

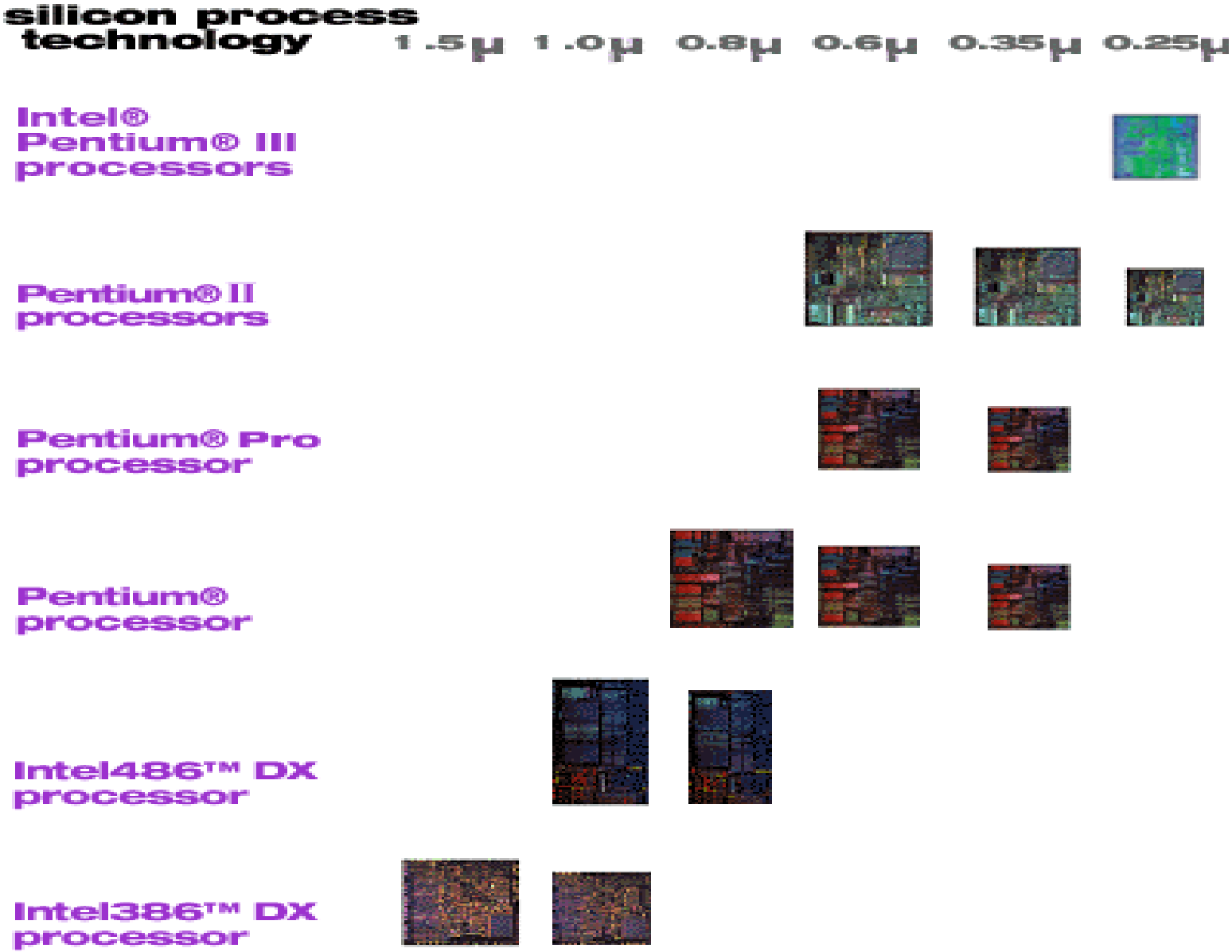
SoC: Intel Processor History: Penitum Pro

- 1995 Intel Pentium Pro, 32-bit ,200 Mhz internal clock, 66 Mhz external, Superpipelining, 16Kb L1 cache, 256Kb L2 cache, 387 pins, 5.5 Million Transistors



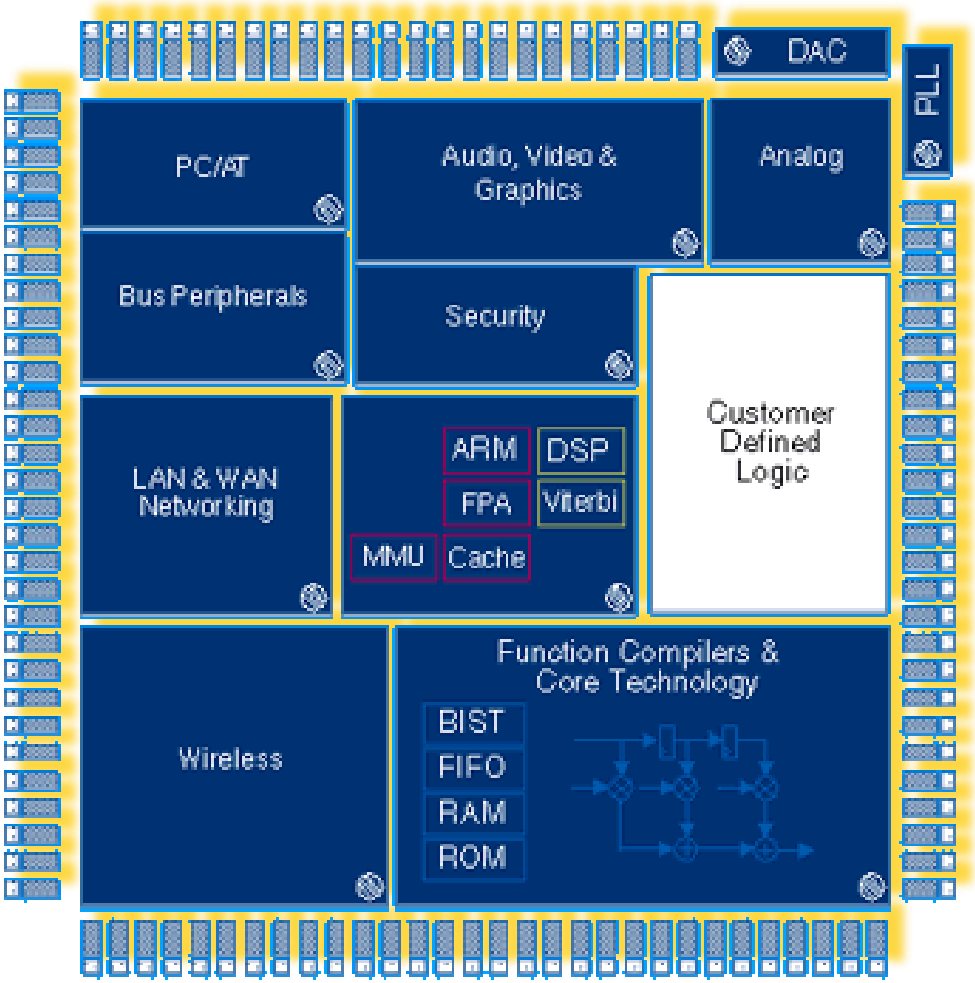


Effect of Technology



SoC: System on a chip (beyond Processor)

- The 2005 prediction: SoC's will be > 500M gates

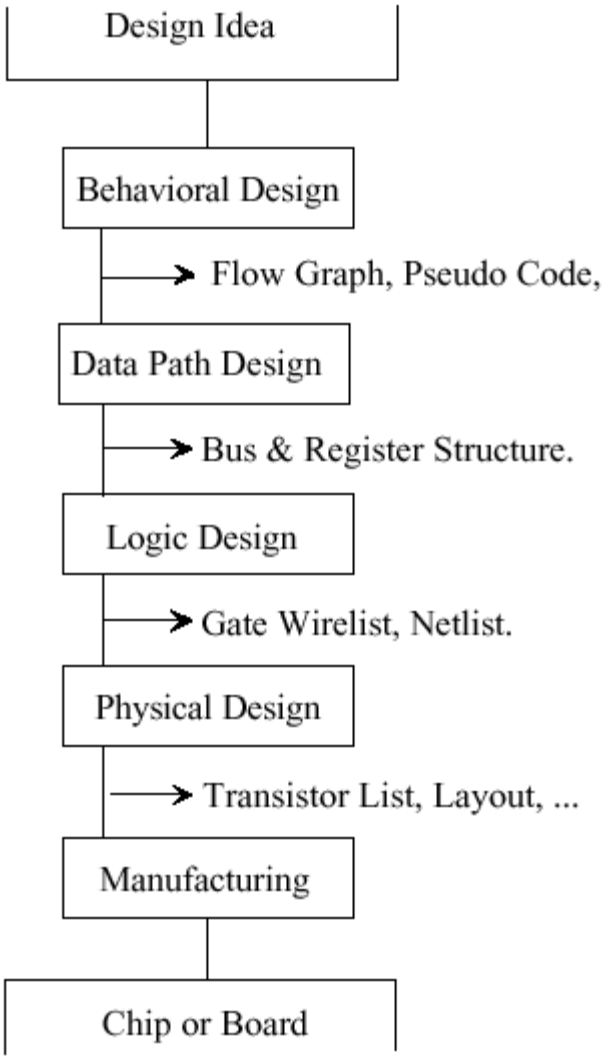


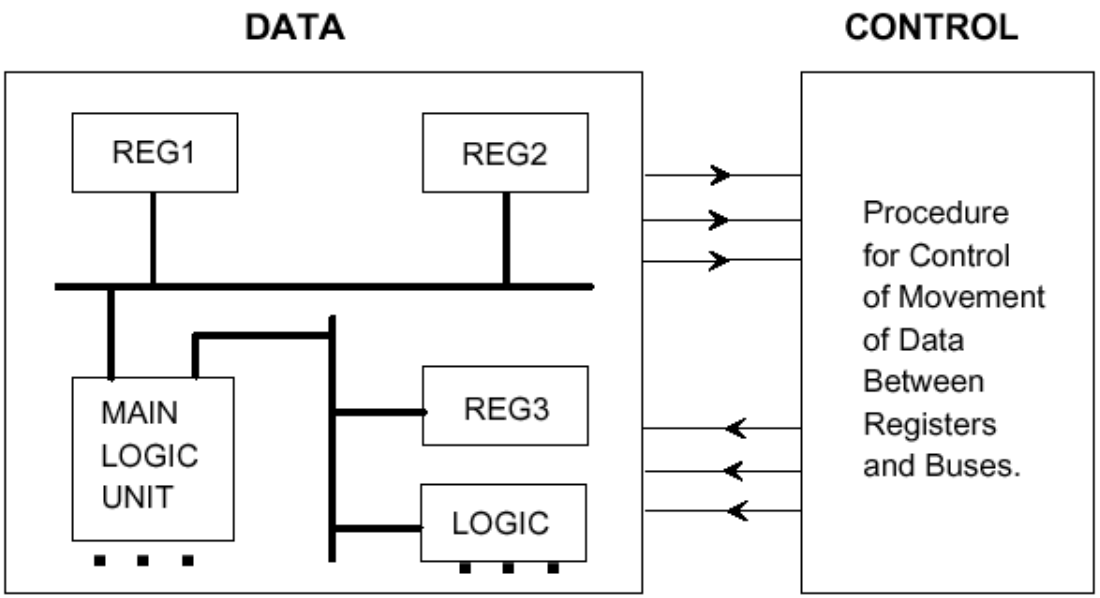
Importance of HDL

Effect of Hardware Description Language (HDL)

- The Complexity and Size of Digital Systems leads to
  - —Breadboards and prototypes which are too costly
  - —Software and hardware interactions which are difficult to analyze without prototypes or simulations
  - —Difficulty in communicating accurate design information
  - —Want to be able to target design to a new technology while using same descriptions or reuse parts of design (IP)

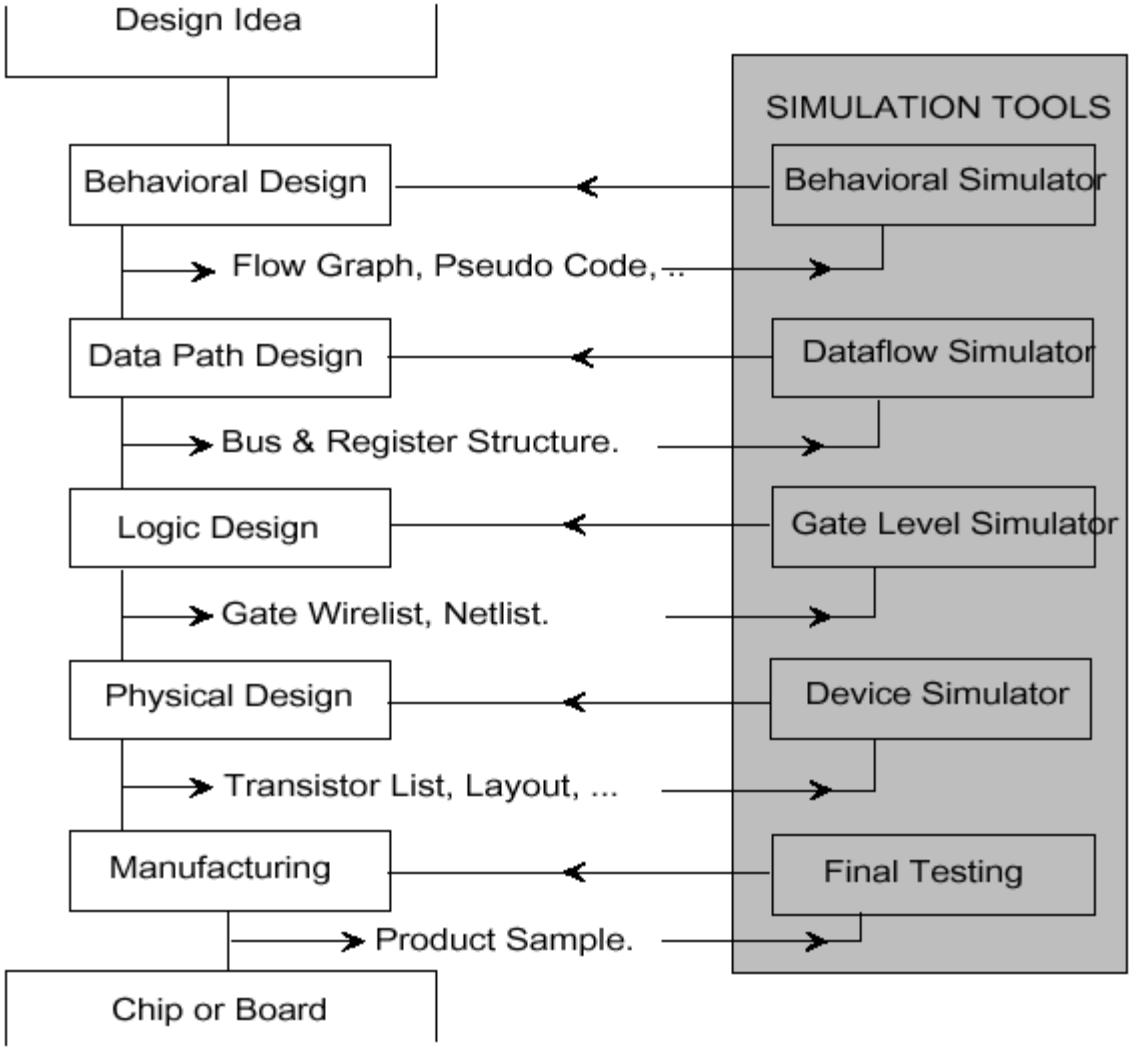
Using HDL in Design





Source: VHDL (Z. Navabi - McGraw Hill)

Using HDL in Verification

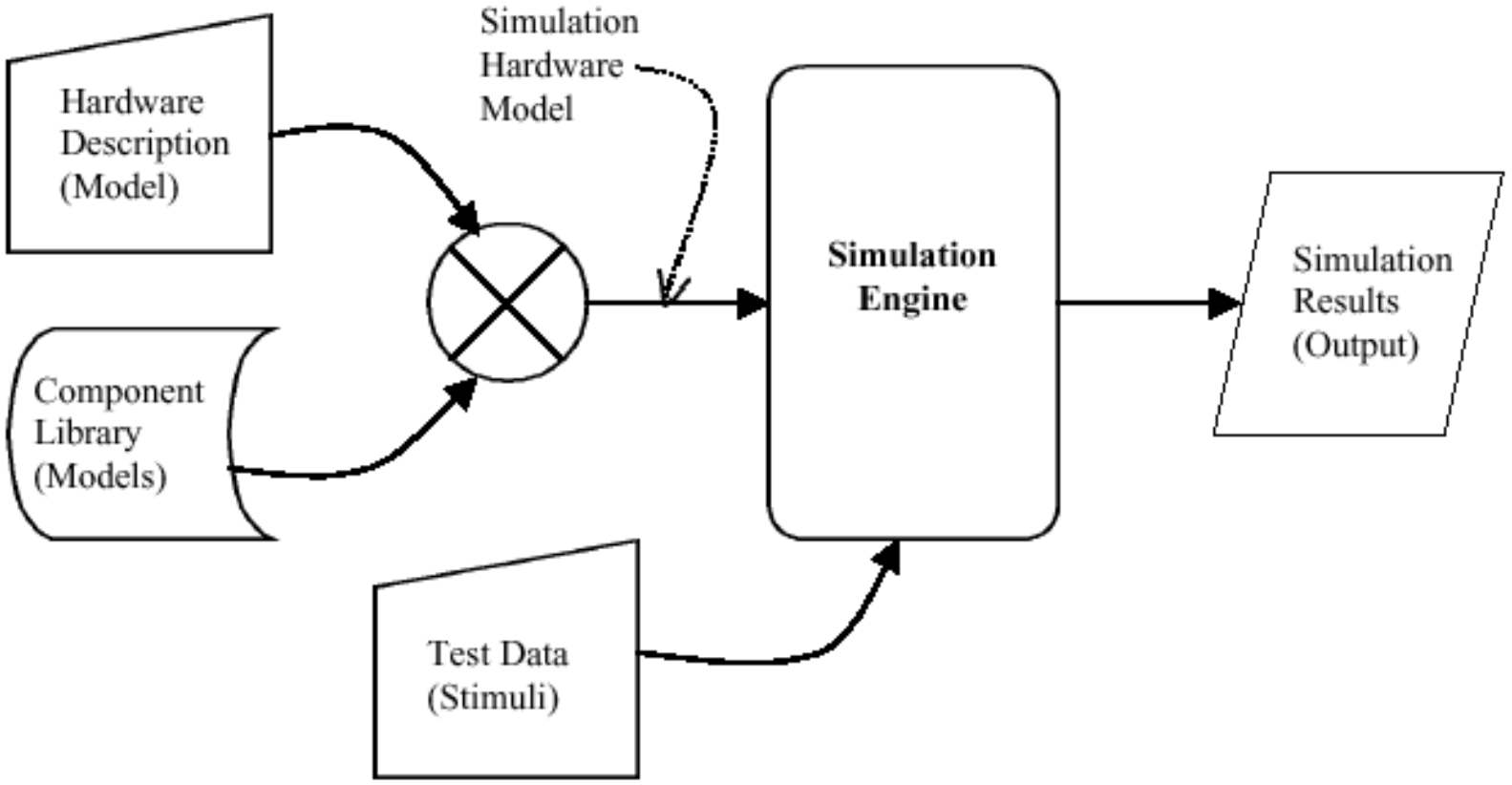


Source: VHDL (Z. Navabi - McGraw Hill)

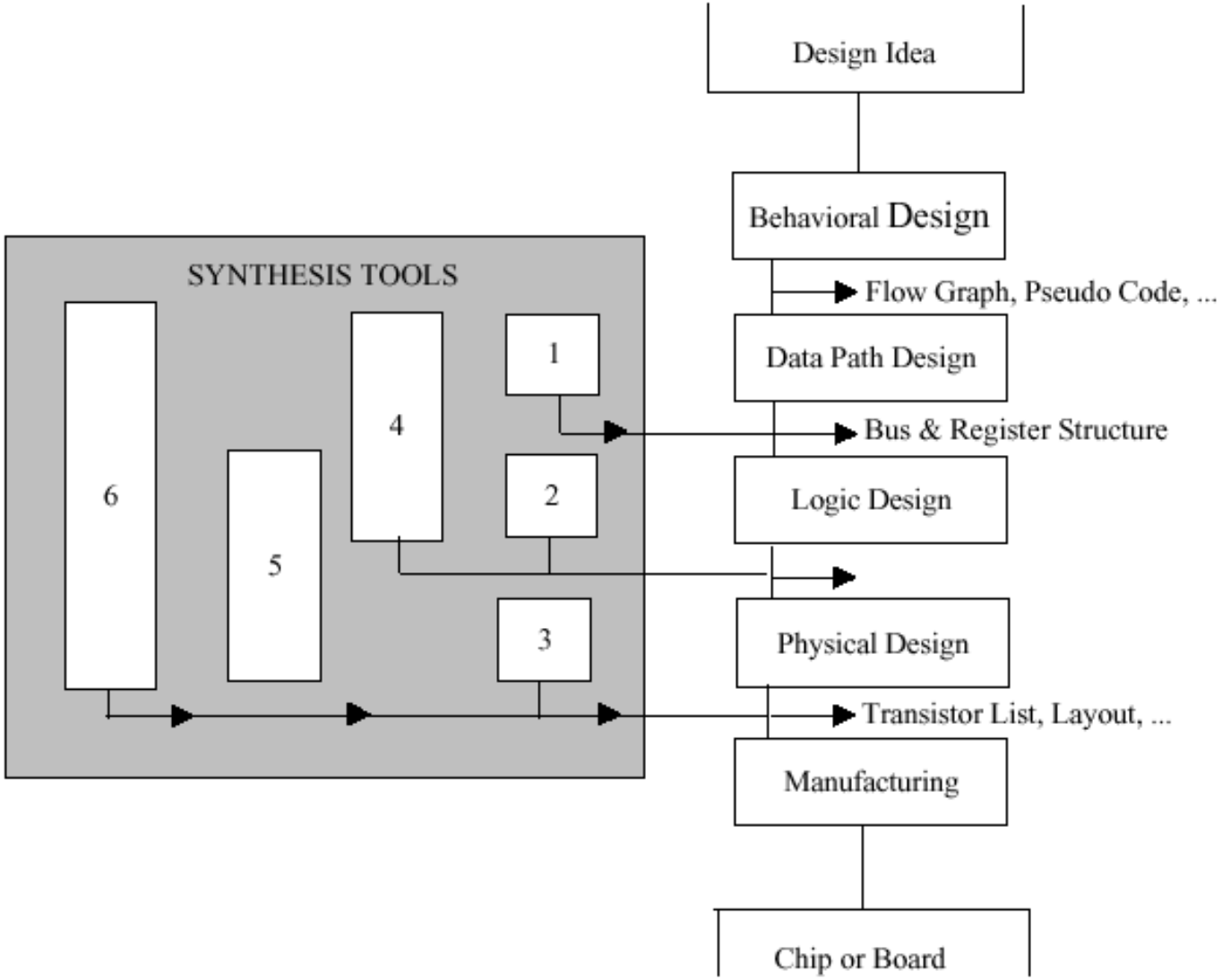
Role of CAD Tools

- CAD tools improve productivity
- Definition: A software program which assists in performing or automates a particular design function
- Major types:
  - Schematic capture
  - Analyzers/Simulators
  - Synthesis

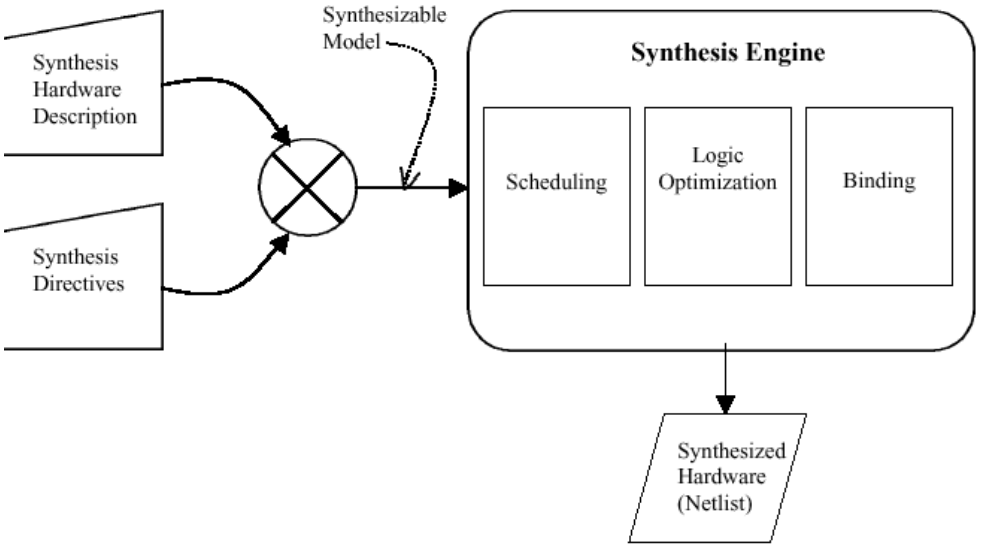
Using HDL in Simulation



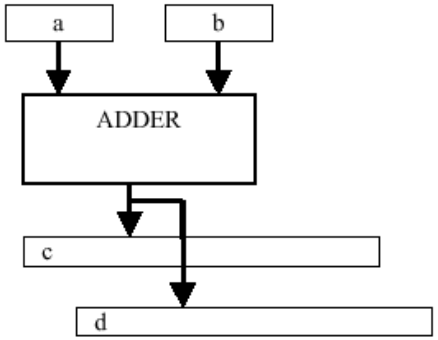
Using HDL in Synthesis Tools



Using HDL in Synthesis & Optimization




```
c <= a + b;
d <= a + b;
```




```
c <= a + b;
c <= x + y;
```