Question 2:

For f(6) = 0

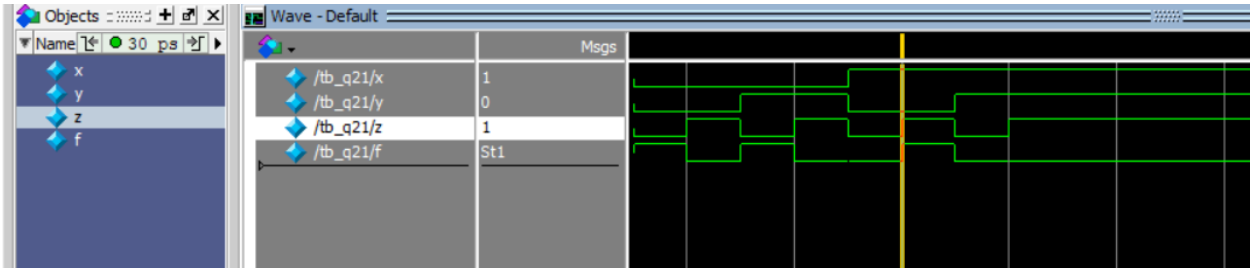
Module:

```
module q21(x,y,z,f);
input x,y,z;
output f;
wire w1,w2,w3,w4;
xor g1(w1,z,1'b1);
xor g2(w2,w1,x);
and g3(w3,x,y);
and g4(w4,w3,z);
xor g5(f,w2,w4);
endmodule
```

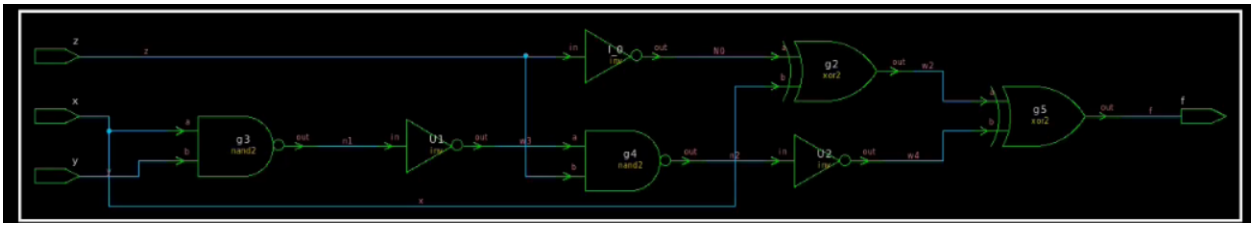
Test Bench:

```
module tb_q21();
reg x,y,z;
wire f;
q21 uut(.x(x),.y(y),.z(z),.f(f));
initial
begin
$monitor($time,"x=%b,y=%b,z=%b,f=%b",x,y,z,f);
#5;
x=1'b0;y=1'b0;z=1'b0;
#5;
x=1'b0;y=1'b0;z=1'b1;
#5;
x=1'b0;y=1'b1;z=1'b0;
#5;
x=1'b0;y=1'b1;z=1'b1;
#5;
x=1'b1;y=1'b0;z=1'b0;
#5;
x=1'b1;y=1'b0;z=1'b1;
#5;
x=1'b1;y=1'b1;z=1'b0;
#5;
x=1'b1;y=1'b1;z=1'b1;
end
endmodule
```

Output waveform:



Circuit:



For f(6) =1

Module:

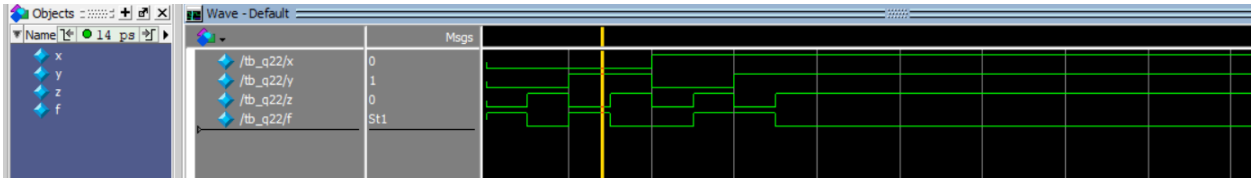
```
module q22(x,y,z,f);
input x,y,z;
output f;
wire w1,w2,w3;
xor g1(w1,z,1'b1);
xor g2(w2,w1,x);
and g3(w3,x,y);
xor g5(f,w2,w3);
endmodule
```

Test bench:

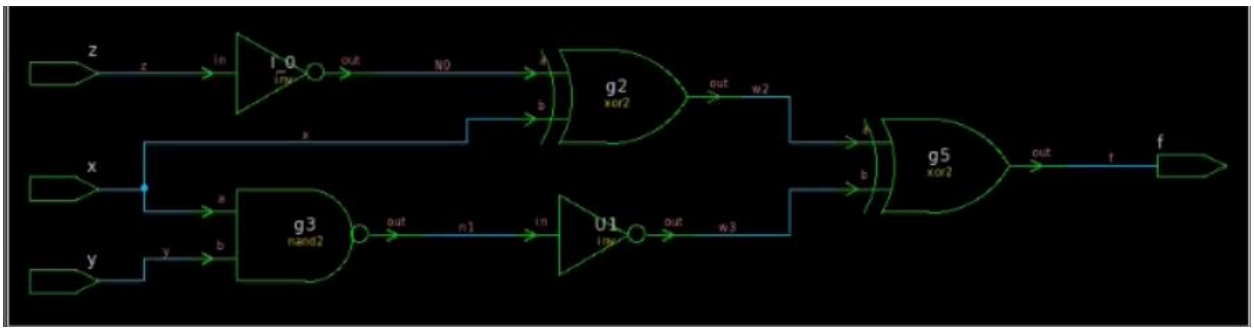
```
module tb_q22();
reg x,y,z;
wire f;
q22 uut(.x(x),.y(y),.z(z),.f(f));
initial
begin
$monitor($time,"x=%b,y=%b,z=%b,f=%b",x,y,z,f);
x=1'b0;y=1'b0;z=1'b0;
#5;
x=1'b0;y=1'b0;z=1'b1;
#5;
```

```
x=1'b0;y=1'b1;z=1'b0;
#5;
x=1'b0;y=1'b1;z=1'b1;
#5;
x=1'b1;y=1'b0;z=1'b0;
#5;
x=1'b1;y=1'b0;z=1'b1;
#5;
x=1'b1;y=1'b1;z=1'b0;
#5;
x=1'b1;y=1'b1;z=1'b1;
end
endmodule
```

Output waveform:



Circuit:



Conclusion:

When implemented with f(6) =1; f(x,y,z) has less number of gates so it is better than other circuit.