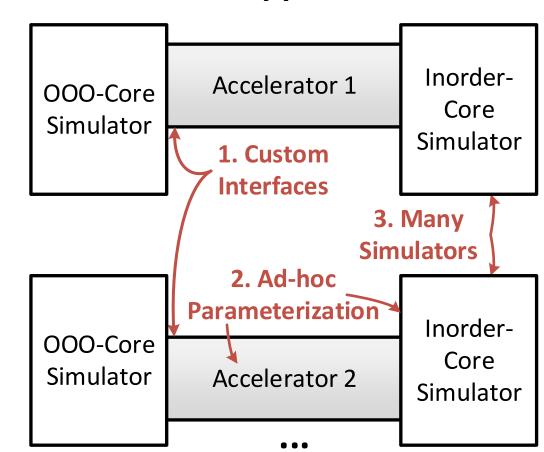
(a) Understanding Accelerator **Limits & Opportunities**

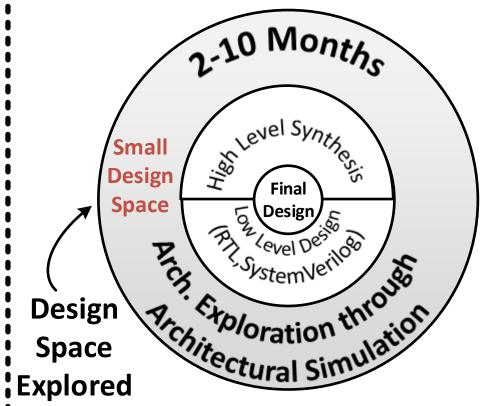


Current Approach

Proposed Approach

Problem: Design Effort is Impractical

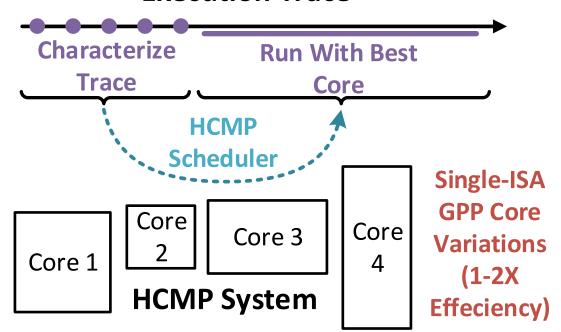
(b) Effective Processes/Practices for Accelerator Design



Problem: Time-Consuming, Restricted Design Space Search

(c) Flexible Acceleration for **Multiple Code Types**

Execution Trace



Problem: Limited-Benefit, Uniform-ISA Systems Targetted

Loop

Accelerator-

Granularity

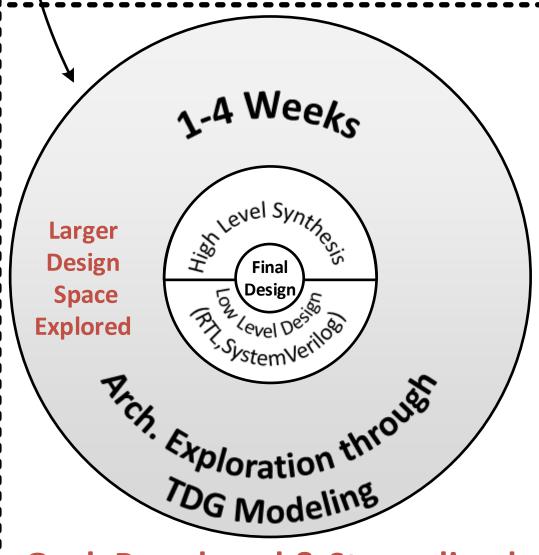
Challenges

(2-50X)

Effeciency)

2. Intuitive/Abstract **Parameterization** Accel Core Model . Simple Core Interface 3. Single Environment **For Assessing Tradeoffs**

Goal: Fundamental Study of Accelerators



Goal: Broadened & Streamlined Accelerator Design

Execution Trace Loop Loop **Function Function Multi-Accelerator Scheduler**

Accelerators Accel 3 Accel 1 Accel 2 General **Purpose Core**

Multi-Accelerator System

: Goal: Practical Multi-Acceleration for **Order-Of-Magnitude Efficiency Gain**

TDG Abstraction Enables